参考資料

TI Designs: TIDA-060013
I2C 通信距離を延長するリファレンス・デザイン:I2C と CAN の組み合わせ

概要

このリファレンス・デザインは、CAN トランシーバを使用して、I2C の範囲をオンボードからオフボード (伝送ケーブル経由) に拡張した後、その信号を I2C に再変換するものです。この手法では、CAN トランシーバの差動信号伝達により、信号品質が向上します。差動信号を使うと、I2C バッファのみによる I2C ラインの延長と比較して、EMI 除去性能が向上する、消費電力を低減できる、ボード間のグランド電位差の心配が少ない、終端を使用できるという利点があります。こうした利点から、ファクトリ・オートメーションや溶接など、EMI が懸念されるノイズの多い環境に最適です。

リソース

TIDA-060013	デザイン・フォルダ
TCAN1042HGV-Q1	プロダクト・フォルダ
P82B96	プロダクト・フォルダ

TI E2E™ Community

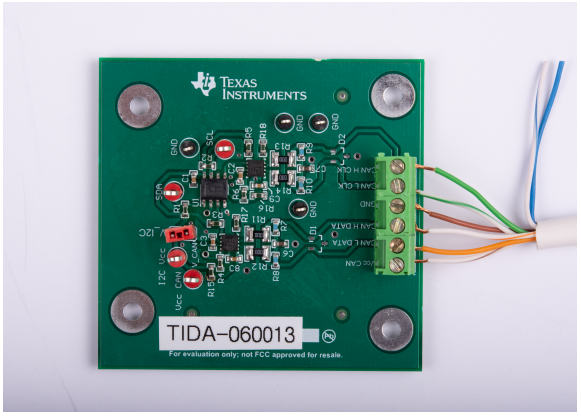
E2E™エキスパートに質問

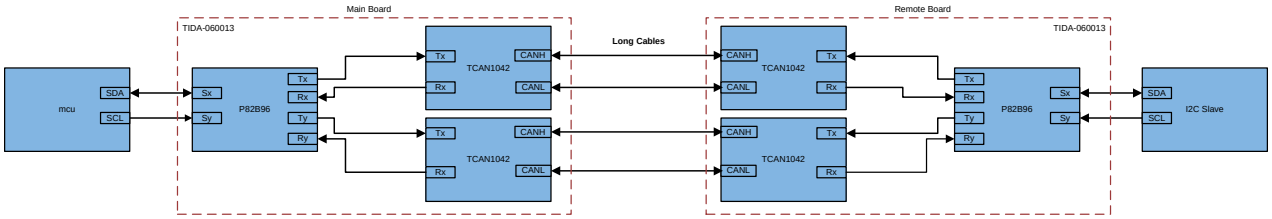
特長

- IEC ESD 保護:±15kV まで
- バス・フォルト保護:±58V (H バージョン以外) および ±70V (H バージョン)
- 電源端子の低電圧保護:VCC および VIO (V バージョンのみ)
- サーマル・シャットダウン保護 (TSD)
- 機能を維持したまま最大 ±30V の同相シフトに対応できるため、異なるグランド基準を使用するシステム間の通信が可能
- I/O 電圧範囲:3.3V～5V
- 100kHz の I2C 周波数に対応
- 双方向通信

アプリケーション

- アーク溶接機
- 射出成形機





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1 System Description

I2C is typically thought of as an on-board solution and is not typically used for long distance communication due to some inherent limitations such as restrictions on bus capacitance. Conventional buffers can be used to extend the communication range across cables, but these solutions typically only support about 8 meters maximum. Specialized buffers can extend this range further but have some disadvantages due to I2C being an open drain single ended signaling protocol. The disadvantages these specialized buffers experience are:

1. High power dissipation due to having to sink more current to pass low signals between the buffers (open drain architecture requires current to sink to pull down FETs to pass lows)
2. Potentially seeing reflections in the signal.
3. Possibility of different ground potentials due to a long ground return path.
4. Susceptibility to EMI.

For example, TCA9803 and TCA9517 are conventional buffers typically meant to separate an I2C bus onboard. They can potentially be used for cable transmission, but are limited to buffering 400 pF. Specialized buffers such as P82B96 and P82B715 are designed for cable transmission by allowing for much larger current sinking capabilities; thus, allowing for larger capacitance buffers (4000 pF and 3000 pF respectively).

This reference design use two CAN transceivers (TCAN1042) and one specialized I2C buffer (P82B96) per node (or four CAN transceivers and two P82B96s for point to point communication) to convert the single ended I2C lines into differential lines which are more suitable for long distance communication and do not suffer the same drawback as the single ended lines. Overcoming the drawbacks of single ended signaling with long distance differential signaling means I2C can now be used for long distance communication in noisy environments such as factory automation.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Vcc	3.3 V to 5 V
Supported I2C Frequency	Standard mode
TXD DTO (Dominant Time Out)	1.2 ms minimum
SDA/SCL ViL	600 mV

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2 System Overview

2.1 Block Diagram

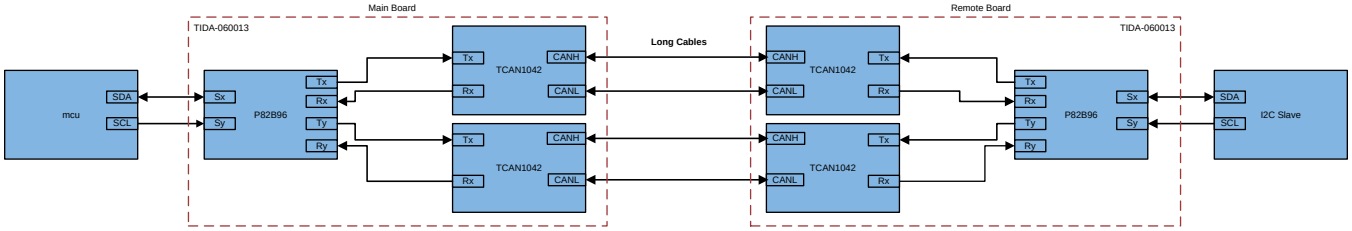

図 1. TIDA-060013 Block Diagram

2.2 Design Considerations

2.2.1 TXD Dominant Time Out (DTO)

Modern CAN transceivers typically come with a feature called TXD dominant time out which looks for a falling edge on the TXD line and tracks how long the TXD line is held low. If the TXD pin does not see a rising edge before the time out period, the CAN device disables the CAN drivers until a rising edge is present. In normal CAN applications this is useful for fault confinement as the CAN protocol uses bit stuffing which requires bits to be flipped if too many consecutive bits are either all high or all low so, the TXD DTO should not occur during normal operation.

In this application, this is not desirable because the I2C protocol does not require bits to be flipped if too many consecutive bits are sent. This means clock stretching must be limited to last less than the TXD dominant time out. For this reference design, clock stretching must be limited to be less than 1.2 ms. Normal I2C communication should not be affected, even if the data being transmitted/received is a long consecutive byte of zeros. The reason for this is due to the 9th clock pulse requiring an ACK from the receiving I2C device which allows for the device transmitting to see a rising edge because of the propagation delay from one Sx/Sy pin of P82B96 to the other and back again.

In some cases, the master-slave transaction may have a long period of zeroes which could trigger the TXD DTO feature of the CAN driver (such as a clock stretching event). The designer must be aware of this and ensure the I2C bus does not transmit too many 0's in a row. This also includes a read event where the slave can transmit 0's while the master ACKs (drives line low). Clock stretching can also cause a dominant time out event to occur. Slaves which support clock stretching should not exceed the dominant time out of the CAN transceiver.

2.2.2 P82B96 VoL and ViL requirement

The P82B96 is an I2C buffer which uses a static voltage offset. This is done to prevent driving itself low and remaining stuck low. The static voltage offset this device generates is typically 880 mV; this VoL meets the I2C standard for devices on 3.3 V logic due to the fact ViL at 3.3 V is 990 mV. This voltage is present when receiving a signal (a read transaction for a master and a write for a slave) and after releasing an I2C communication line. 図 2 and 図 3 show P82B96 VoL under two different IoL conditions.

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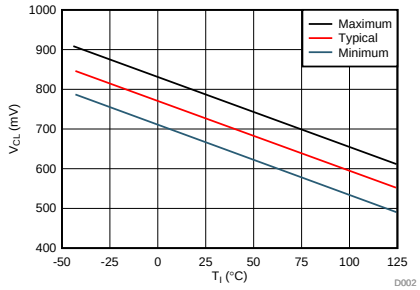

図 2. P82B96 VoL Across Temperature at IoL = 0.2 mA

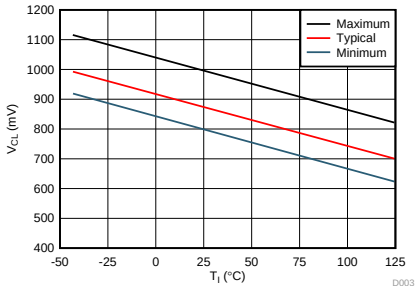

図 3. P82B96 VoL Across Temperature at IoL = 3 mA

This also means this device needs to see a lower voltage on its I2C line in order to send a low; this ViL voltage is 650 mV (typical). If the master/slave on the Sx/Sy pin of this device does not produce a voltage lower than the required ViL of this device, then this device is not able to send a low to the CAN transceiver's RXD pin and communication is not possible. 図 4 shows P82B96 ViL across temperature.

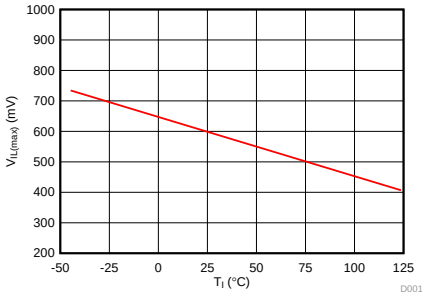

図 4. P82B96 ViL Across Temperature

2.3 Highlighted Products

2.3.1 P82B96

The P82B96 is an I2C buffer normally used for conventional single ended long distance communication. In this reference design, the P82B96 acts as the bridge between I2C and CAN. The Sx/Sy pins of this device interface with the I2C lines while the Tx/Ty pins drive the RXD line of a CAN transceiver and the Rx/Ry pins receive the output of the TXD of a CAN transceiver. This bridge allows for bidirectional communication across the data line.

2.3.2 TCAN1042

The TCAN1042 is a CAN transceiver which is used to drive the signals across cables differentially. This device can be swapped out with any other TI CAN transceiver though this device was chosen because it does not require a common mode choke for EMI reduction which saves on cost and board space of an inductor.

TCAN1046 is also a suitable option which would save on cost and space because it is a dual channel CAN transceiver which is necessary to transmit two I2C signals (SDA and SCL). This would remove one CAN transceiver for each board.

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2.4 System Design Theory

2.4.1 I2C Definition of Set Up Time

To test this reference design, measurements of the data set up time are taken while making the transmission cable longer. The measurement are during the handoff of a master releasing the data line and a slave taking control of it to send an ACK to the master. This results in the shortest data set up time. The data set up time needs to be above a set minimum threshold to be I2C compliant. Data set up time is normally defined as the difference between 30% of the SDA line with respect to 30% of SCL which can be seen in 図 5. I2C standard version 6 specifies the minimum set up time is 250 ns for standard mode and 100 ns for fast mode.

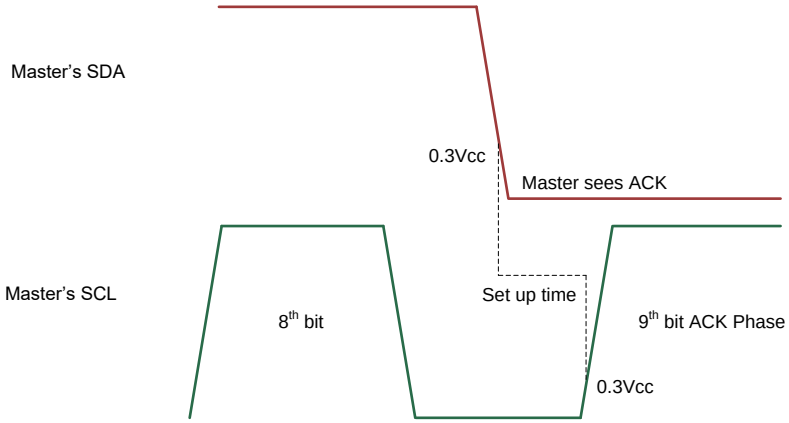

図 5. I2C Standard Set Up Time Definition

2.4.2 Release Delay

There is an issue with using the standard data set up time definition for this reference design because of how the P82B96 Rx/Ry pin connected to the TCAN1042 TXD pin causes propagation delay. When SDA or SCL is released on the Sx/Sy pins of P82B96, the SDA/SCL lines do not immediately get pulled high but rather hang at the static voltage offset which is seen in sequence 1 of 図 6. After some propagation delay, the P82B96 releases Tx/Ty and the pull up resistor pulls the signal up to V_{CC}, seen by TCAN1042 RXD in sequence 2 of 図 6. After some delay TCAN1042 TXD pin releases and pulls the P82B96 Rx/Ry pin to a logic high, seen in sequence 3 of 図 6. Finally the Sx/Sy pin is released from the static voltage offset and gets pulled high to V_{CC} through the pull up resistor, seen in sequence 4 of 図 6. The time it takes for a logic high signal to travel from Sx/Sy to Tx/Ty/ to Rx/Ry and finally back to Sx/Sy (original node which released the line high) are referred to as the release delay.

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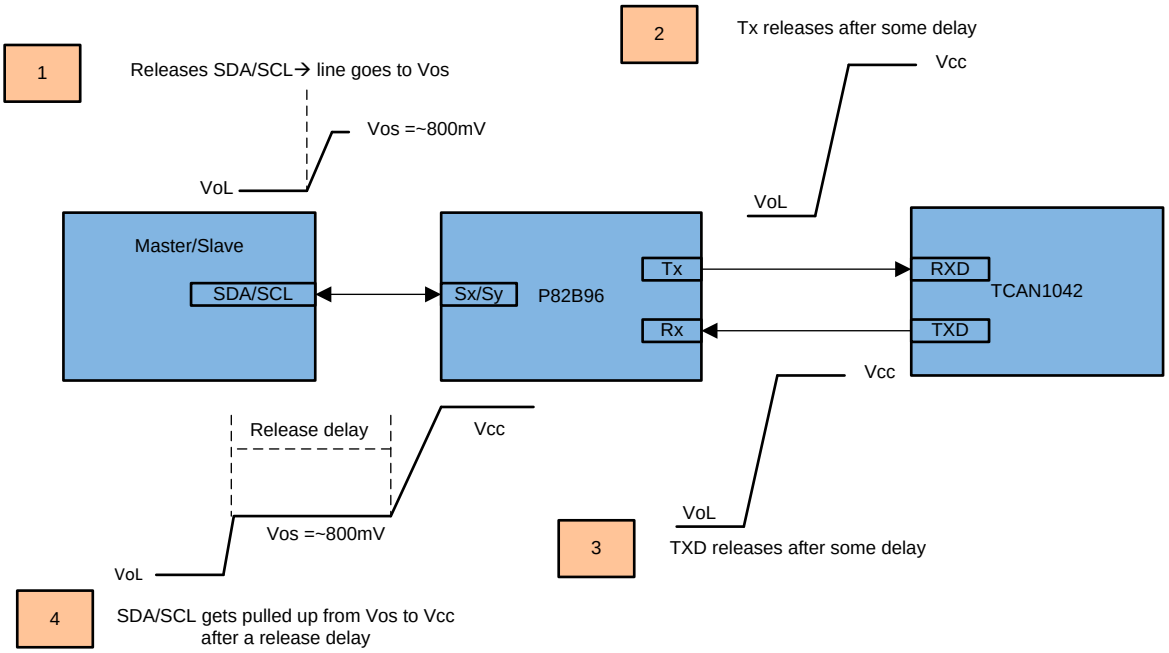

図 6. Explanation of Release Delay

2.4.3 Reference Design's Definition of Set Up Time

Due to the release delay, measuring the data set up time at 30% of SDA to 30% of SCL is not an accurate representation of data set up time because any measurements using this definition includes the release delay which was never specified in the I2C standard. Therefore, the standard data set up time definition needs to be changed to exclude the release delay. This reference design redefines the data set up time from 30% of SDA to when SCL begins to release shown in 図 7.

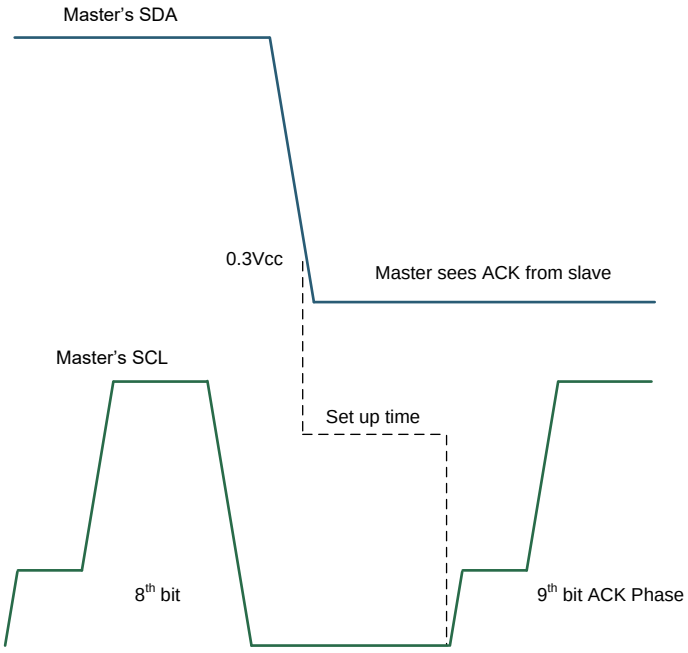

図 7. Reference design's Redefined Set Up Time Definition

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The release delay can be seen in 図 8. The transaction below shows an ACK event from a slave to a master. The purple signal is the master SDA, light green is the slave's SDA, and dark green is the master SCL. The release delay is about 520 ns and through testing was found to be fairly constant at both 100 kHz, 400 kHz, and various transmission cable lengths.

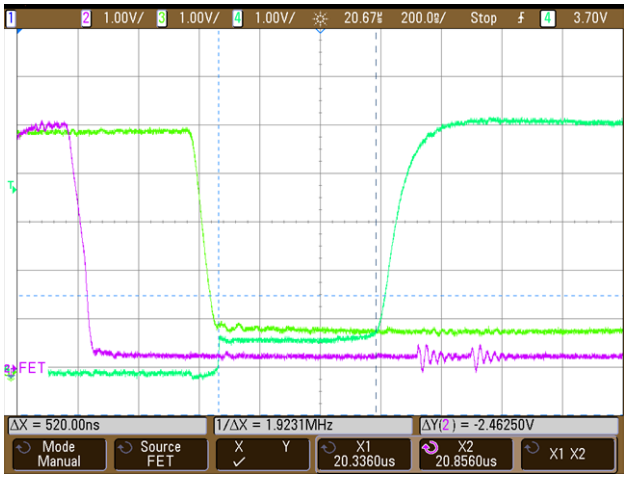

図 8. Release Delay Measured at Approximately 520 ns

The data set up time is expected to change due to the propagation delay, as increasing the transmission cable length introduce more parasitic capacitance into the system and the time it takes for the signal to travel across the cable. The propagation delay is also a limiting factor in this design as it delays when the clock and data arrives to the slave. It also delays when the master receives data back from the slave (remember both master and slave see different clock signals due to the delay so the slave responds later in reference to the master clock).

The release delay can be avoided on the SCL signal by disconnecting the Rx pin of P82B96 to TXD of TCAN1042 and tying Rx to a pull up resistor on the main board (with the master) if clock stretching is not intended to be used. This makes the SCL line unidirectional which is the case in most applications.

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3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

- Two TIDA-060013 boards
- Oscilloscope
- 5-V power supply
- Microcontroller
- Slave device (temperature sensor in this test)
- CAT5 cable
- Ethernet male to male adapter connectors

3.1.2 Software

May use any I2C library which supports 100 kHz communication between a master and slave.

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3.2 Testing and Results

3.2.1 Test Setup

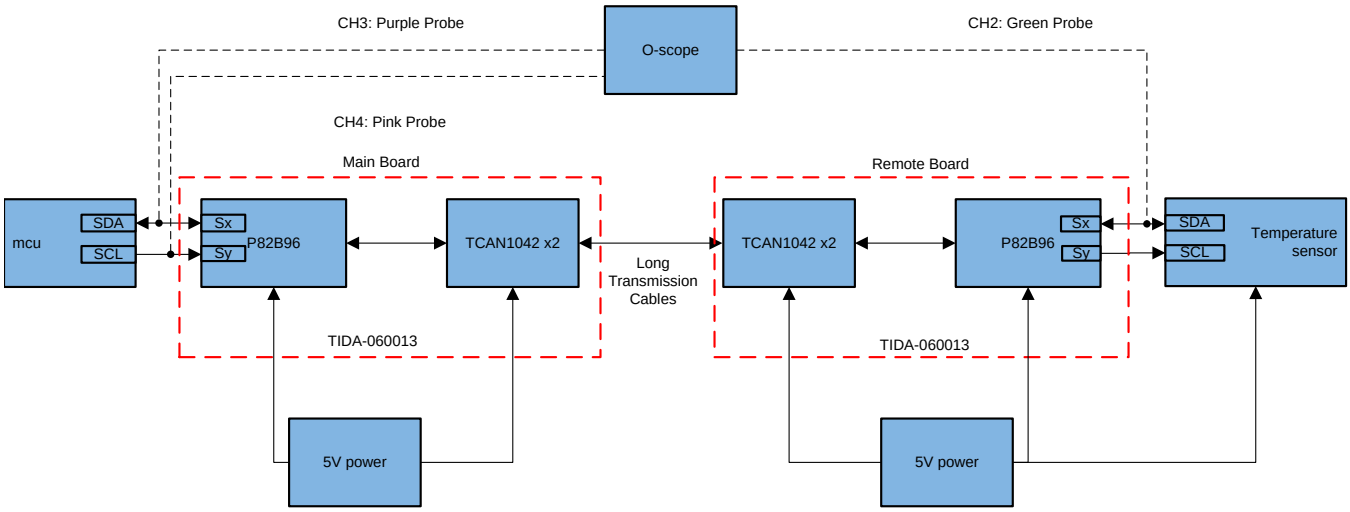

図 9. Simplified Block Diagram of System

図 9 above is a simplified block diagram which shows the test set up in regards to the power supply and the oscilloscope channels. The long transmission cables begins at 200 feet and increase by about 100 feet each measurement until the minimum I2C specified data set up time has been reached. After taking data set up time measurements for the first I2C transaction, the I2C communication was tested by reading a temperature sensor 10 times in succession multiple times to verify communication. If invalid data was received or a NACK was received (not during the 10th byte) then communication is considered unstable and results in failure. Set up time and I2C communications all were done at standard mode (100 kHz) and fast mode (400 kHz).

Testing found the data set up time was lower when the slave device was ACKing to the master rather than the master ACKing to the slave during read transactions. Measuring the data set up time between a read ACK from the slave and a write ACK from the slave resulted in a lower set up time from the slave reacting to a read bit. Therefore, all data set up times hereafter are measured from the slave ACKing to the master immediately after the read bit is received.

図 10 and 図 11 show the set up time differences for a read and a write. The left image is the write while the right image is a read. The write takes 314 ns while a read is 254 ns, this means the worst case data set up time occurs during a read ACK from slave to master (the lower of the two numbers means it is slower to respond).

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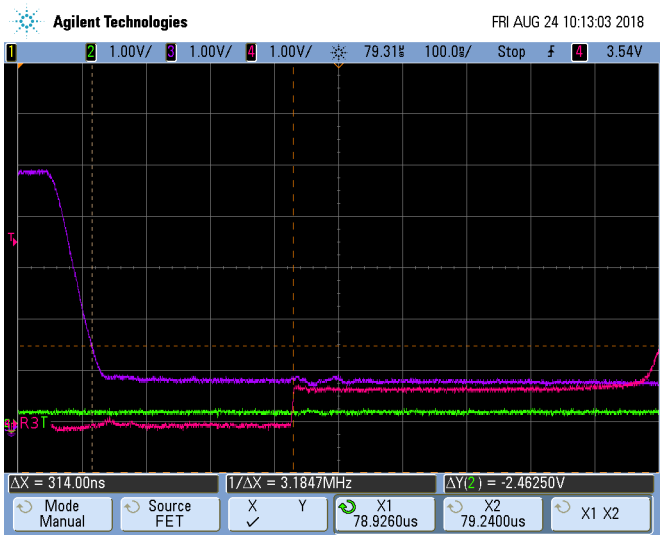

図 10. Set Up Time for Write Transaction

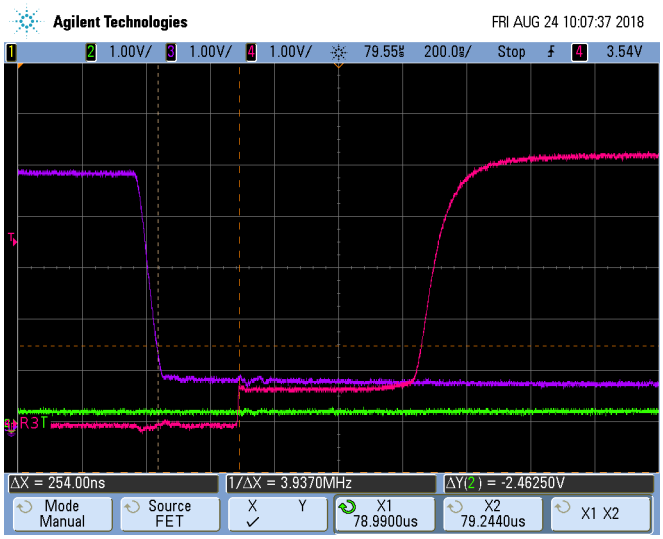

図 11. Set Up Time for Read Transaction

注: the response time for other I2C slave devices may be different and the worst case set up time for other devices could occur during a write and not a read. The designer needs to be aware of this and also understand that some slaves may respond quicker or slower in which case the max distance for this reference design for I2C communication may not be the same as other systems.

3.2.2 Test Results

3.2.2.1 Standard Mode (100 kHz) Results

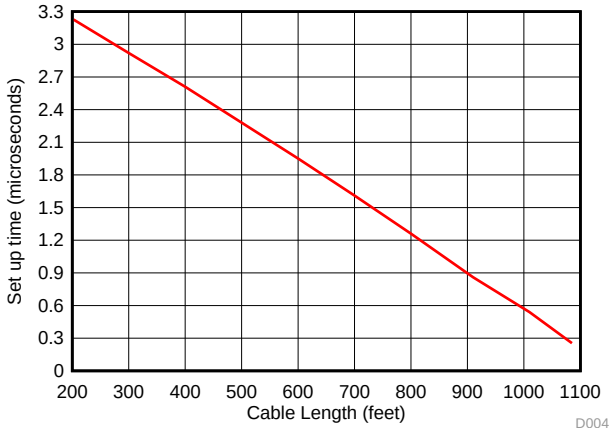

図 12. Set Up Time Versus Cable Length at 100 kHz

Data shows communication from 200 feet to 1085 feet of cable works without error at 100 kHz. Testing also shows the set up time has a linear relationship with the cable length. At 1085 feet, the set up time is about 254 ns, shown in 図 13, which meets the I2C minimum time of 250 ns.

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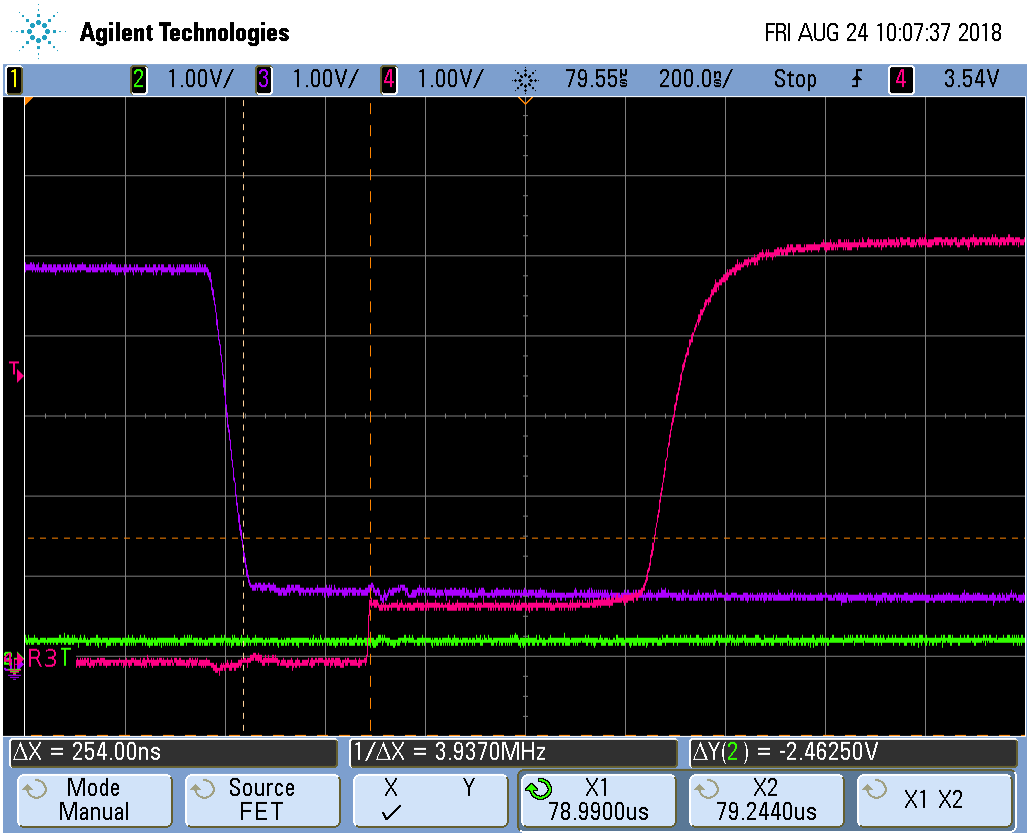

図 13. 100 kHz Set Up Time at 1085 Feet

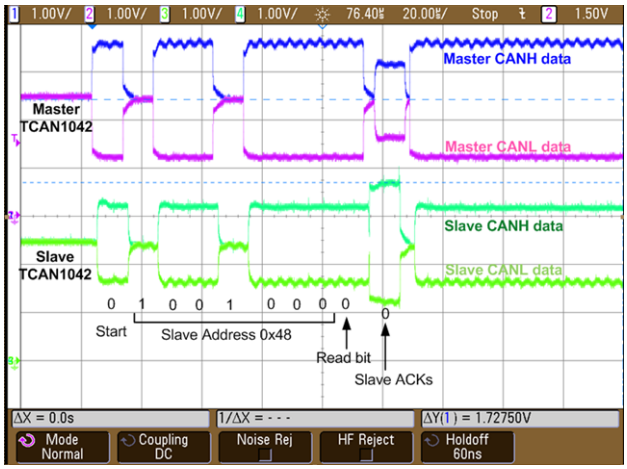

図 14. CAN Signals

The CAN signal from the master and the slave transceiver can be seen in 図 14 above. The master dominant signal has about a voltage difference of 2.5 V while the slave transceiver sees about 1.5 V. This difference between the transmitter and receiver is normal and a result of the parasitic resistance of the transmission cable causing the voltage drop across the cable. The ISO 11898 CAN standard states a CAN transceiver must accept 0.9 V or larger as a dominant signal. In the case of the reference design at a

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distance of 1085 feet, 1.5 V meets the requirement to be considered a dominant signal and is interpreted as dominant by the CAN transceiver. Notice in 図 14 the slave momentarily takes control of the data line when the slave ACKs which causes the receiver to become the transmitter and the master now becomes the receiver. During this occurrence, the master also sees a 1.5 V dominant signal which still meets the requirements of a differential of 0.9 V or greater.

Due to the release delay discussed in the previous section, any received signals has waveform deformation. This deformation makes high periods shorter by the release delay time which in this reference design is about 520 ns. For example, a 400-kHz clock typically has a 50% duty cycle and a period of 2.5 µs; the high period and low period would normally both be about 1.25 us. With the effect of the release delay, the slave high period is not 1.25 µs but rather 0.73 µs seen in 図 15 below. This means the waveform's duty cycle is now about 29% instead of 50%. At 100 kHz this distortion is much less noticeable, as the duty cycle changes to only about 45%.

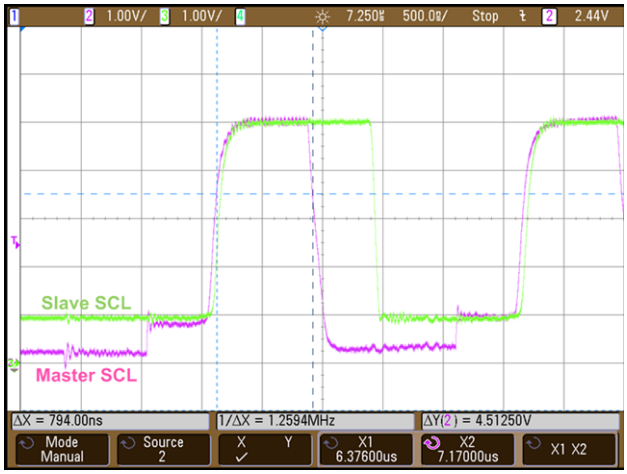

図 15. 400 kHz SCL Duty Cycle Distortion

Collecting data for 400 kHz communication showed that even a direct connection between the main board and remote board violated the data set up time requirement to meet I2C standard of 100 ns. For a direct connection, the data set up time was 34 ns. The micro-controller was still able to read the temperature value correctly from the temperature sensor. At 100 feet the data set up time was found to be negative at a value of 280 ns. 図 15 shows this measurement. The temperature read from this transaction was also accurate and multiple temperature reads in a row could be done without error. Communication at 400 kHz is possible, but is not I2C compliant. Communication is expected to remain possible as long as the ACK on the master's data line reaches the low threshold (ViL) before half of the high period of the clock where data is sampled. The high period mentioned here is if the release delay were not present. When the fast mode is using a high period of 600 ns on the clock line, the maximum value the data set up time can be before the ACK is missed is –300 ns.

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-060013.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-060013.

4.3 PCB Layout Recommendations

SDA and SCL traces should not be placed too close to each other due to potential cross talk during fast fall times or rise times if strong pull up resistors are used.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-060013.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-060013.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-060013.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-060013.

5 Software Files

To download the software files, see the design files at TIDA-060013.

6 Related Documentation

1. *Why,When,and Howto use I2C Buffers*

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7 Terminology

VoL- Voltage output Low

ViL- Voltage input Low

ACK- Acknowledge

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NACK- Not Acknowledge

8 About the Author

DUY (BOBBY) NGUYEN is an applications engineer at Texas Instruments where he is responsible for supporting I2C products and generating content for I2C products.

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