参考資料

TI Designs: TIDA-060017
LVDSインターフェイス上のSPI信号伝送のリファレンス・デザイン

概要

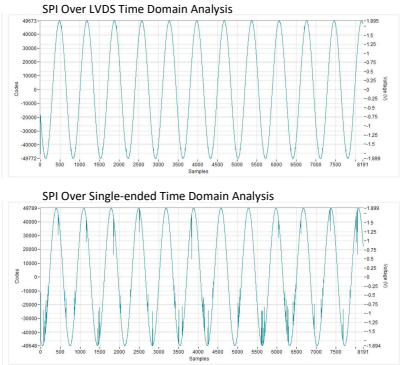
このTI Designでは、ノイズの多い環境でSPI信号を同じPCB上、またはPCBから別の基板へ長距離にわたって送信するとき一般的に発生する信号の整合性の課題を、LVDSインターフェイス上でSPI信号を伝送することにより解決し、最適化する方法について説明します。この概念により高いノイズ耐性、EMI放射の低減、より広い同相入力許容範囲を実現できます。このTI Designには次の特長があります。

- 低電圧差動信号処理(LVDS)インターフェイス経由でSPI信号を送信することにより信号品質を大幅に向上
- 距離およびLVDSインターフェイスがSPI通信速度に及ぼす影響に関する詳細なタイミング分析
- SCLKをSPIマスタに返送、または一部のTIデバイスで提供されている拡張SPI機能を使用して、SPIタイミングの課題を解決するソリューションのデモンストレーション
- 各種のSPIペリフェラルと、LVDSドライバおよびレシーバーを評価するためのオプションを提供

リソース

TIDA-060017	デザイン・フォルダ
SN65LVDS31-33EVM	ツール・フォルダ
ADS8910BEVM-PDK	ツール・フォルダ

TI E2E™ Community　E2E™ エキスパートに質問

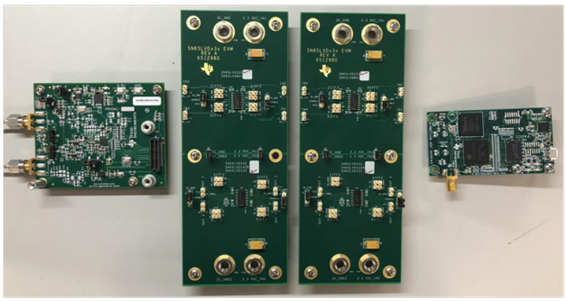


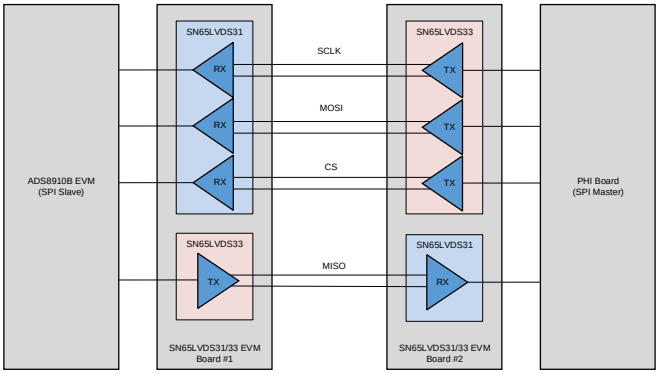
特長

- LVDSインターフェイスの使用によるSPIバスのノイズ耐性強化と距離の拡大
- 標準SPIを使用した場合の距離0.5mと比較して、SPI over LVDSを使用した場合の通信距離は最低3m
- SCLKをSPIマスタに返送することにより、伝搬遅延を短縮し、SPIの通信速度または距離を向上する技法
- 他の差動信号(RS-422/RS-485)ソリューションと比較して1/10の消費電力
- -4V～5Vの同相入力電圧範囲により、高いグランド・バウンス耐性を実現

アプリケーション

- 半導体試験用機器
- データ収集
- ラボ計測機器
- 超音波スキャナ
- CTスキャナ
- 保護リレー
- 端末装置





1 System Description

Serial peripheral interface (SPI) is found in numerous applications as the communication method between processor and peripheral devices. SPI was initially designed for short distance communication between devices on the same PCB. However, there is increasing demand for longer range SPI communication on the same PCB or from board to board. As distance increases, external noise and crosstalk between SPI signals becomes an issue. Furthermore, increased distance limits the data rate due to propagation delay, and affects the signal quality due to potential ground shift between boards. In this design guide, designer shows how to migrate the challenge posed when trying to extend SPI communication range and send SPI signals from board to board over long distance.

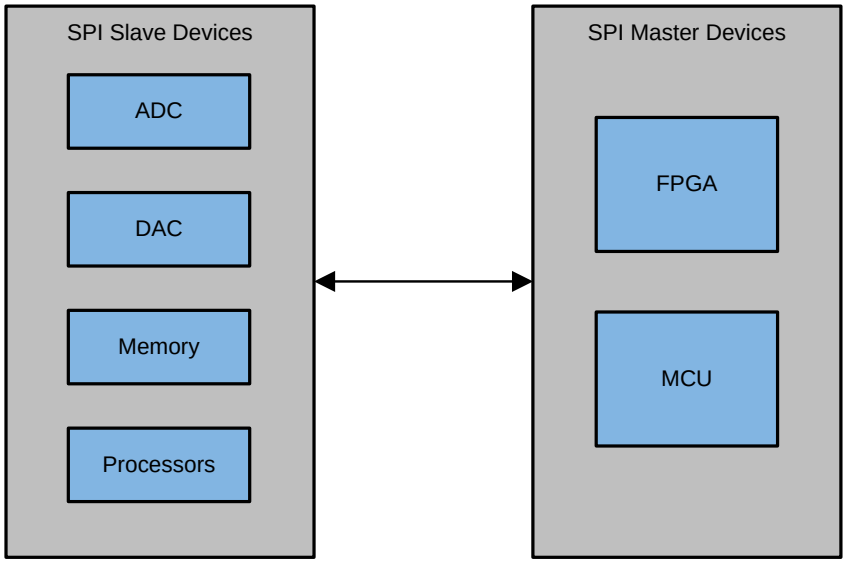


図 1. System Diagram

1.1 Key System Specifications

This reference design is configured to transmit single-ended SPI signals through LVDS driver and receiver. An ADC ADS8910B is used as the SPI slave device, and the PHI Controller is used as the SPI master device. Two quad channel LVDS drivers and two quad channel LVDS receivers are selected to drive the single-ended SPI signals from board to board.

表 1 gives the key system specifications. Following the system design consideration in 2.3, this reference design can be easily configured and extended for different applications using SPI interface.

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Power Supply for SN65LVDS31-33EVM	3.3V
Power Supply for ADS8910B	5.5V and 3.3V
SN65LVDS31-33EVM Information	
Standard	ANSI TIA/EIA -644 Standard
Number of LVDS Drivers	4
Number of LVDS Receivers	4
Driver Input Type	LVTTL/LVCMOS
Receiver Output Type	LVTTL/LVCMOS
Typical Output Voltage Rise and Fall Times	500 ps (400 Mbps)
Operating temperature	–40°C to +85°C
Power Consumption	25 mW Typical at 200 MHz
Form Factor	10-mm × 6-mm SOIC16
ADS8910B Information	
Number of Channels	Single
Input Type	Differential
Input Range	+/- 5V differential
Resolution	18 bits
Sample Rate	1-MSPS
SPI Clock Speed	Up to 70MHz
Operating temperature	–40°C to +125°C
Power Consumption	21-mW at 1-MSPS
Form Factor	4-mm × 4-mm VQFN

2 System Overview

2.1 Block Diagram

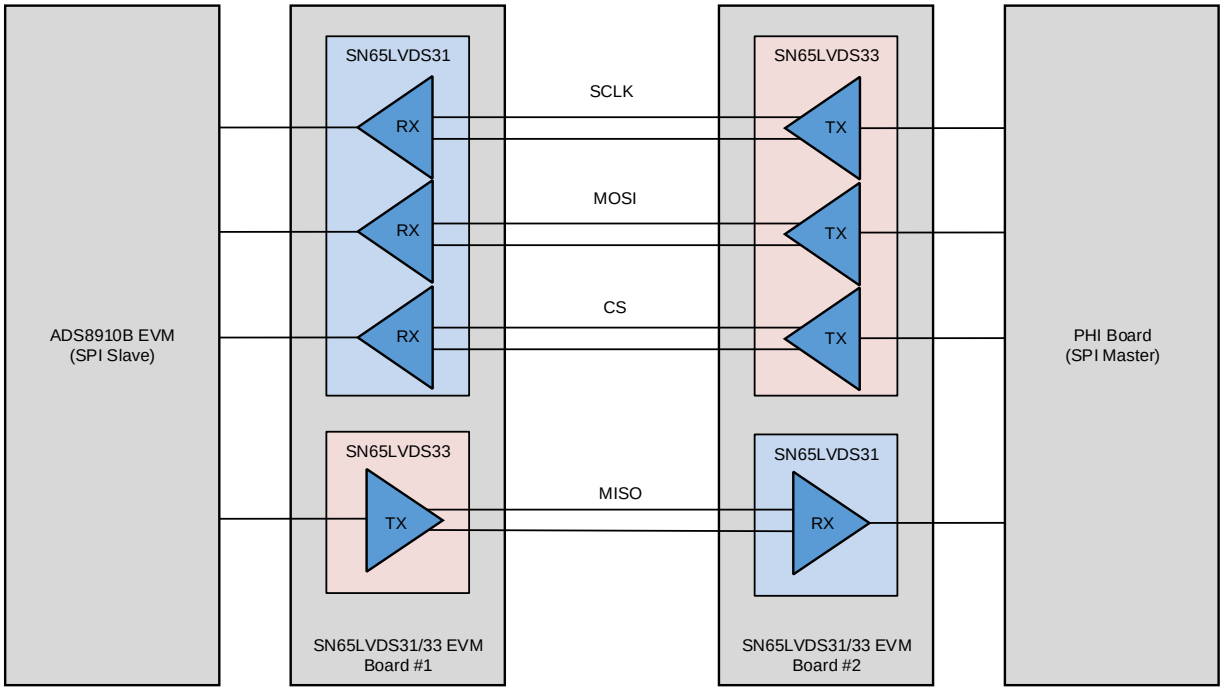


図 2. TIDA-060017 Block Diagram

図 2 shows the setup block diagram of this design.

2.2 Highlighted Products

The system features the device SN65LVDS31/SN65LVDS33 EVM, and ADS8910B EVM.

2.2.1 SN65LVDS31 and SN65LVDS33 EVM

SN65LVDS31 and SN65LVDS33 EVM includes a pair of LVDS quad channel driver SN65LVDS31 and receiver SN65LVDS33. Both devices are TIA/EIA-644 standard compliant LVDS driver and receiver. The SN65LVDS33 receiver incorporates an enhanced common-mode input voltage range of -4 V to 5 V, as well as an active-failsafe circuit that provides operation over the entire input common-mode range. This wide common-mode input feature is showcased in the design as a solution to combat potential ground shift present in high noise, high power switching environments.

2.2.2 ADS8910B EVM

The ADS8910B EVM includes both the SPI master device (PHI controller) and the SPI slave device (ADS8910B). The ADS8910B is a high-speed, single-channel, high-precision, 18-bit successive approximation register (SAR) analog to digital convertors (ADCs) with an integrated reference buffer and integrated low-dropout (LDO) regulator. The ADS8910B boost analog performance while maintaining high-resolution data transfer by using TI's enhanced-SPI feature, thereby making this device an excellent choice for applications involving FPGAs, DSPs.

2.3 System Design Theory

This design guide uses analog to digital converter, a common device that uses SPI interface, as an example, and focuses on maximizing the signal integrity of SPI interface by sending SPI signals over LVDS interface. As the signal integrity improvement is provided by the LVDS interface and is independent of the SPI peripherals, other SPI host and the SPI peripheral could be used to fit different application needs. Alternative LVDS driver and receiver such as DS90LV011A, DS90LV012A, DS90LV047A, and DS90LV048A can be used as well if wide common-mode input range is not necessary. These four LVDS drivers and receivers offer lower propagation delay compare to SN65LVDS31/33.

2.3.1 detail the timing challenges presented by extending the SPI communication distance. When these performance limiting characteristics are understood, two solutions are highlighted, one using novel design consideration for general SPI interfaces and another one using key feature of TI's ADC device.

With the elimination of timing challenges, solution for improving signal integrity when transmitting SPI signals from board to board is presented in 2.3.3.

2.3.1 Timing Analysis

SPI is a preferred communication method between processor and peripheral devices due to its high speed and bidirectional nature; however, it was intended for very short distance applications. There is an inherent timing challenge when implementing a long distance SPI solution. This challenge and a detailed analysis of its impact with examples are described in the following sections.

2.3.1.1 Effect of Propagation Delay on SPI Clock Speed

図 3 shows a generic SPI block diagram. The processor is generally the SPI master that decides the sampling rate and data transfer rate. In typical SPI communication, the SPI master sends data at rising edge and receives data on the falling edge within the same clock cycle.

As depicted in 図 4, the SPI master expects the valid data before the clock falling edge. The total round trip propagation delay must be less than half the SCLK period to avoid missing bits. Hence, the theoretical maximum SPI clock can be calculated as:

$$SCLK_{Max} = \frac{1}{2 \times t_{Period}}$$

The equation assumes that there is no change in the waveform shape. However, digital signals are analog in nature as they have finite rise-fall times, which result in waveform deformities that cause pulse width distortion (PWD) as they propagate through different signal chain elements. The pulse width of the clock or the data line changes due the different threshold voltages and rise-fall times of the digital devices in the path. 図 5 shows a datasheet example of propagation delay and PWD that can be found in various devices.

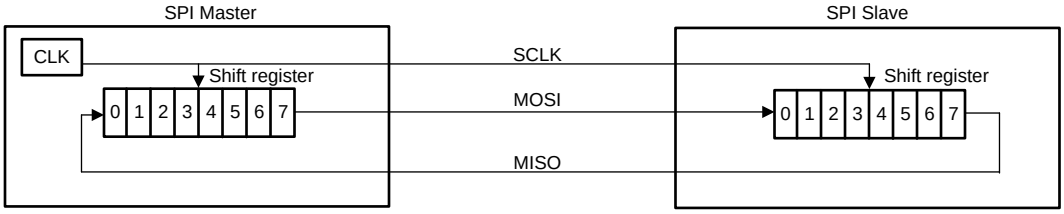


図 3. SPI Block Diagram

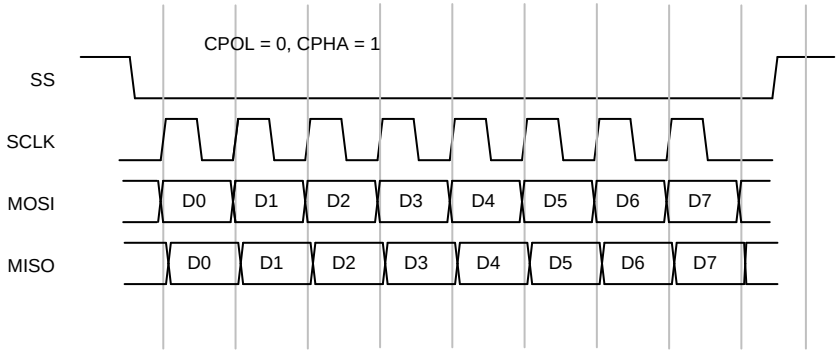
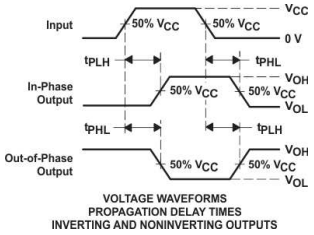


図 4. SPI Timing Diagram



6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	OUTPUT CAPACITANCE	T_A = 25°C			–40°C to 85°C		–40°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	C_L = 15 pF		5	7.1	1	8.5	1	9.5	ns
t_{PHL}					5	7.1	1	8.5	1	9.5	
t_{PLH}	A	Y	C_L = 50 pF		7.5	10.6	1	12	1	13	ns
t_{PHL}					7.5	10.6	1	12	1	13	

図 5. Propagation Delay and PWD

A detailed timing analysis is required to calculate the maximum SPI clock rate by considering the SPI propagation delay and PWD.

2.3.1.2 Determining Maximum SPI Clock (SCLK) vs. Distance

In a low latency system, the data in peripheral device should be made available to the host system with minimum delay. There are three major delay contributors in a typical system — SPI peripheral, data link device, and transmission media. Both the SPI peripheral and the data link device have fixed delay; however, the delay in transmission media increases as communication distance increases. In this section, an example on determining the maximum SPI clock speed vs communication distance is shown.

The individual devices used in the calculation are listed in 表 2

表 2. Devices Used in Example

No.	Device	Description
1	SN65LVDS31	LVDS Driver
2	SN65LVDS33	LVDS Receiver
3	ADS8910B	ADC

表 3 lists the associated timing parameter values taken from respective device datasheet.

表 3. Timing Parameters

Parameter	Delay(ns)	Comments
SN65LVDS31	4	
SN65LVDS33	3.5	
ADS8910B	6.4	70MHz clock with 45% duty cycle
Cable/PCB trace	5	Delay per meter

The equation on finding the maximum SPI clock speed is:

$$SCLK_{Max} = \frac{1}{\left(\left(TX_{Delay} + RX_{Delay} + Cable_{Delay} \times \text{Cable Length}\right) \times 2 + ADC_{Delay}\right) \times 2}$$

図 6. Max SPI Speed vs Cable Length

Without LVDS interface and if 10cm PCB trace is assumed, then the maximum SPI clock speed achievable for ADS8910B is 67.6MHz. If the distance is increased to 3m for longer range communication, the maximum SPI clock speed is lowered to 13.74MHz under worst conditions.

With LVDS interface and 10cm PCB trace, the maximum SPI clock speed is 22.3MHz. If the distance is increased to 3m for longer range communication, the maximum SPI clock speed is lowered to 9.7MHz under worst conditions.

As distance increase, the propagation delay contributed from cable or trace cannot be ignored.

2.3.2 Eliminating Round-Trip Delay

In this section, two solutions are presented to effectively eliminate round trip delay. One solution is a novel design that feeds the SCLK back to the SPI master. The other solution utilize enhanced SPI interface offered in selective TI devices such as ADS8910B ADC.

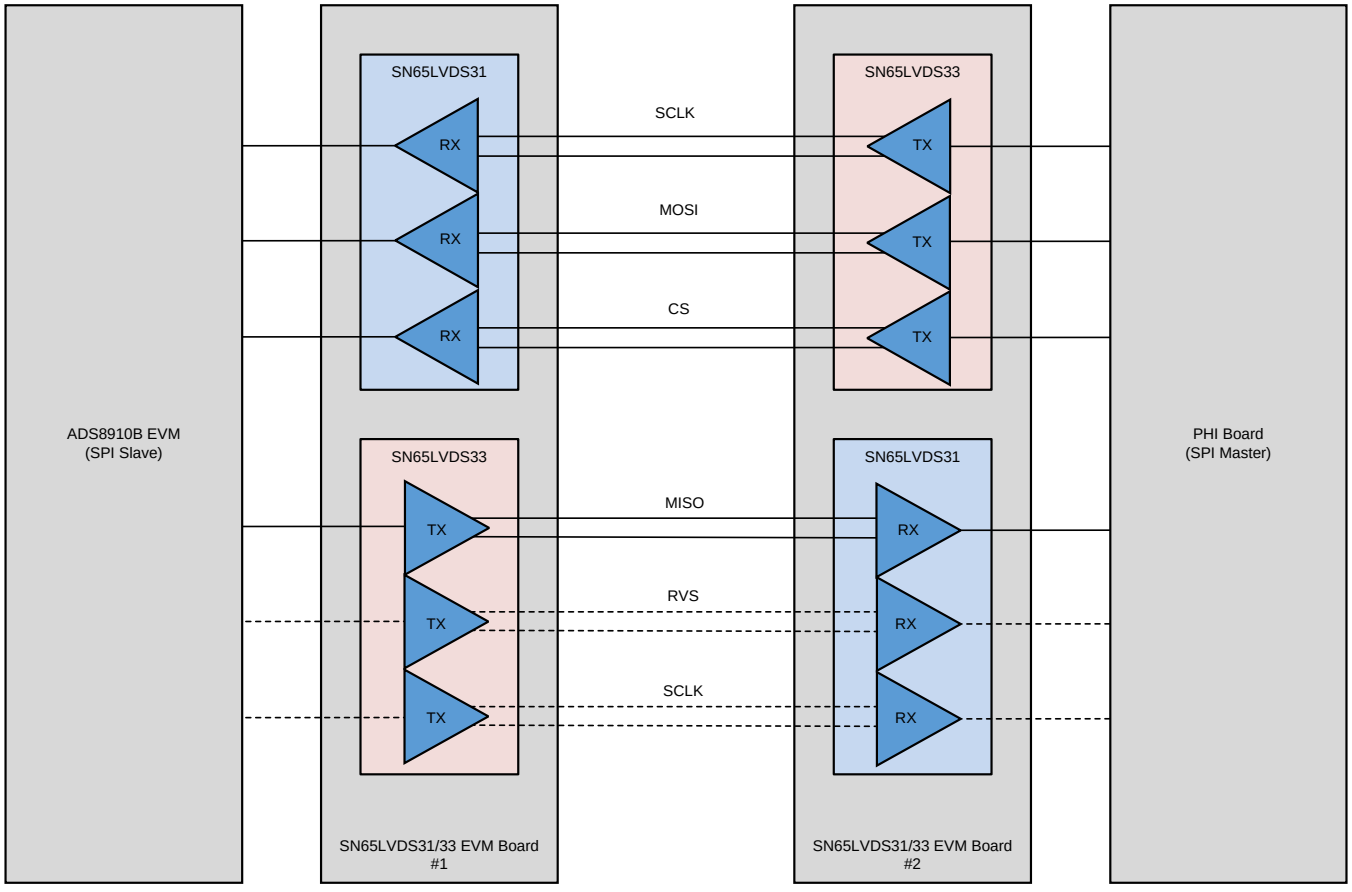


図 7. Eliminating Round-Trip Delay Block Diagram

2.3.2.1 Feed SCLK back to SPI Master

As the SPI host expect to receive data within the same clock cycle, longer propagation delay will cause the returned slave data out of sync with the clock. The solution for restoring synchronicity between the slave data and the clock while maintaining a high data rate is to feed the clock signal from the slave back to the SPI master. 図 8 clarifies the benefit of this solution. Here t_0 represents the first rising clock edge, or the start of a data transmission, and t_P is the data-link propagation delay. After traversing the data link, both the master clock (SCLK) and the master data (MOSI) remain in sync. Feeding back the master clock signal synchronizes the clock with the slave data so that both arrive equally delayed at the master. The only requirement is that the master provide two independent SPI ports, one configured as a master (SPI1) and the other configured as a slave (SPI2). Most modern microcontrollers possess two or more SPI ports, so this requirement poses no problem.

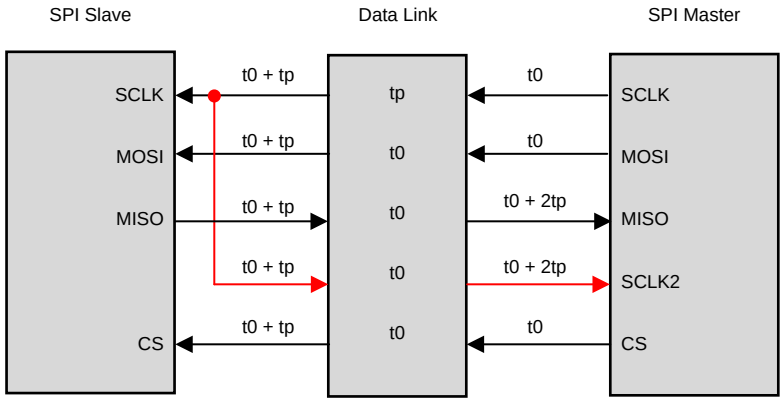


図 8. Feed SCLK back to SPI Master

2.3.2.1.1 Timing Analysis when SCLK is routed back to SPI master

If the user can route the returned SCLK signal and the MISO signal at equal length, the delay from cable or trace is effectively eliminated. The equation on calculating the maximum SPI clock speed becomes:

$$SCLK_{Max} = \frac{1}{\left(\left(TX_{Delay} + RX_{Delay}\right) + \text{Cable Length Mismatch} + ADC_{Delay}\right) \times 2}$$

Using the same parameter detailed in 2.3.1.2, the maximum SCLK speed achievable with LVDS interface is 37MHz under worst condition.

2.3.2.2 Enhanced SPI feature offered by Selective TI Devices.

Selective TI Devices such as ADS8910B ADC offers an enhanced SPI interface that offers multiple solutions to effectively eliminate the timing challenge posed by long distance SPI applications.

There are several ways that the enhanced SPI feature could help solving the SPI propagation delay issue.

- Early Data Launch (EDL)
- Increase SPI Bus Width
- Source-Synchronous Protocol

In Early Data Launch mode, the device launches the output data on MISO data pins half a clock earlier compared to the standard SPI protocol, therefore reduce the total delay present in the SPI bus.

ADS8910B also has the option to increase the MISO data bus width from one bit to two bits or four bits. By increasing the MISO data bus, same data rate can be achieved with lower SCLK rate which in turn increases the SPI communication distance. Free LVDS driver and receiver pairs in the quad channel LVDS devices can be used to support the increased data bus width.

In Source-Synchronous mode, the ADS8910B is able to generate clock signal that's synchronize to the SCLK signal and transmit the generated clock signal back to the SPI master. This mode further eliminates the delay by synchronizing the data on MISO bus and the clock signal.

Further detailed implementation of enhanced SPI interface can be viewed in ADS8910B datasheet.

2.3.3 Signal Integrity Considerations

In the previous sections, we have detailed ways to extend SPI communication range. As range increase, sending SPI signals from board to board become possible. However, now signal integrity becomes a big concern due to reflections caused by unterminated signal lines. The characteristic impedance of the transmission media and termination impedance will differ substantially, causing an impedance mismatch on the bus. Due to the nature of single-ended signals lines, any external noise will be coupled on the signal line which causes communication errors. Electromagnetic interference (EMI) is also a concern as the high-frequency portion of the SPI signal radiates outward, allowing the signal to couple onto adjacent signals.

This TI design guide presents a solution to address the signal integrity and EMI issue by sending SPI signal over Low Voltage Differential Signaling (LVDS) interface. LVDS has great advantages for handling noise and EMI issue due to its differential signaling nature. Typically the differential pair connecting LVDS driver and receiver is closely coupled. When external noise is present in the environment, both wires will receive nearly equal amount of noise. Since the receiver only cares about the voltage difference between the two wires, the external noise will be canceled out. This is a very important advantage over single ended technology. This property enables LVDS to have a very high signal to noise ratios, and is one of the reasons why LVDS technology is robust.

As a differential circuit, LVDS driver and receiver radiate substantially less electromagnetic wave to the environment than single-ended circuits. As complementary current runs in the differential pair, both line will generate magnetic fields but in the opposite direction. In turn, the magnetic field partially cancels each other. The SN65LVDS31 and SN65LVDS33 LVDS driver and receiver also offers wide common-mode input range from -4V to 5V. It allows a +/-3V ground potential difference to combat ground bounce typically found in high power, high switching environment.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

This reference design is realized by combining two SN65LVDS31-33 EVM and one ADS8910B EVM. 図 9 shows the setup diagram.

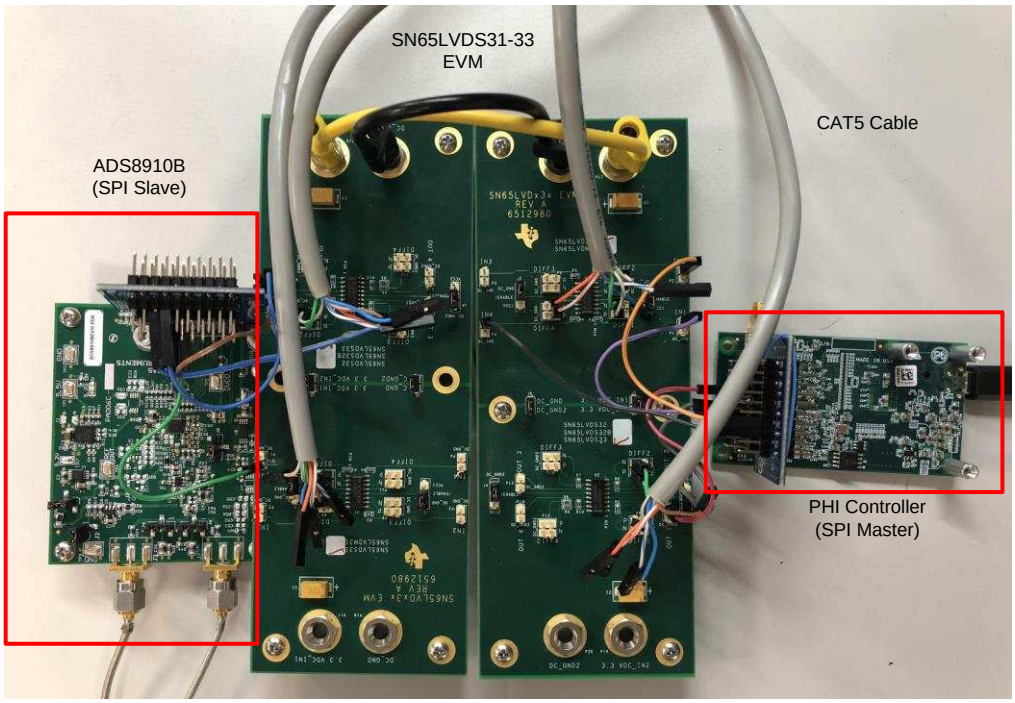


図 9. Hardware Setup

3.1.2 Software

The PHI GUI software, which is based on the LabVIEW™ platform, validates the TIDA-060017. 図 10 shows the available test options in the PHI GUI.

PHI GUI software can be found at http://www.ti.com/tool/ads8910bevm-pdk

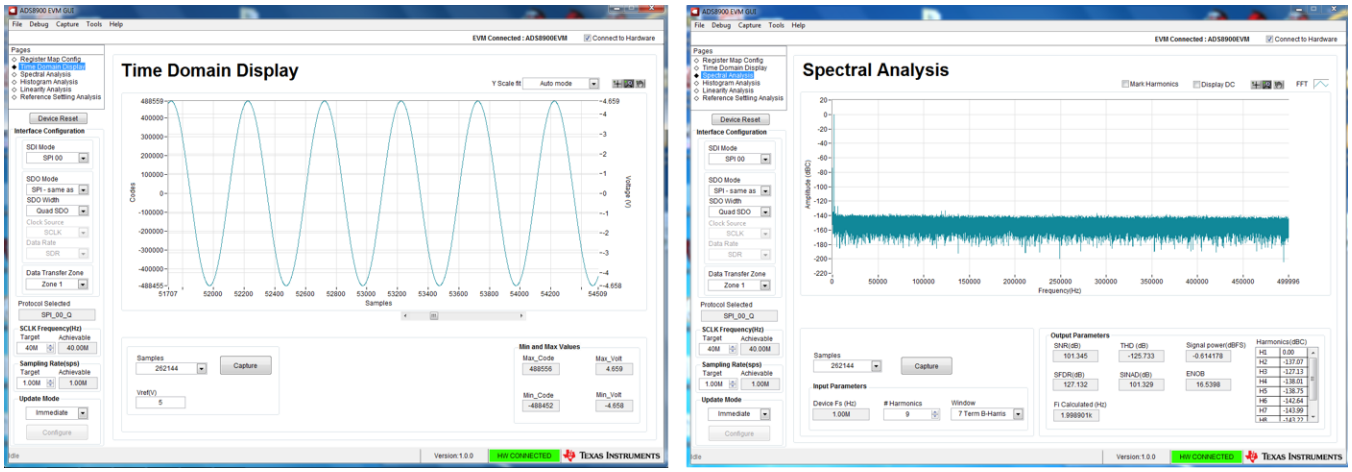


図 10. PHI GUI

3.2 Testing and Results

3.2.1 Test Setup

Three testings was performed to evaluate and compare the performance difference between single-ended SPI communication and SPI communication over LVDS Interface. The input differential source to the ADS8910B ADC is a 2KHz, 2V differential sine wave. The overall test setup for SPI over LVDS is shown as 図 11. The overall test setup for single-ended SPI is shown as 図 12. A set of breakout boards are used connect Samtec QTH/QSH connectors on ADS8910B EVM to SN65LVDS31/33 EVM. CAT5 cable are used to connect the two SN65LVDS31/33EVM.

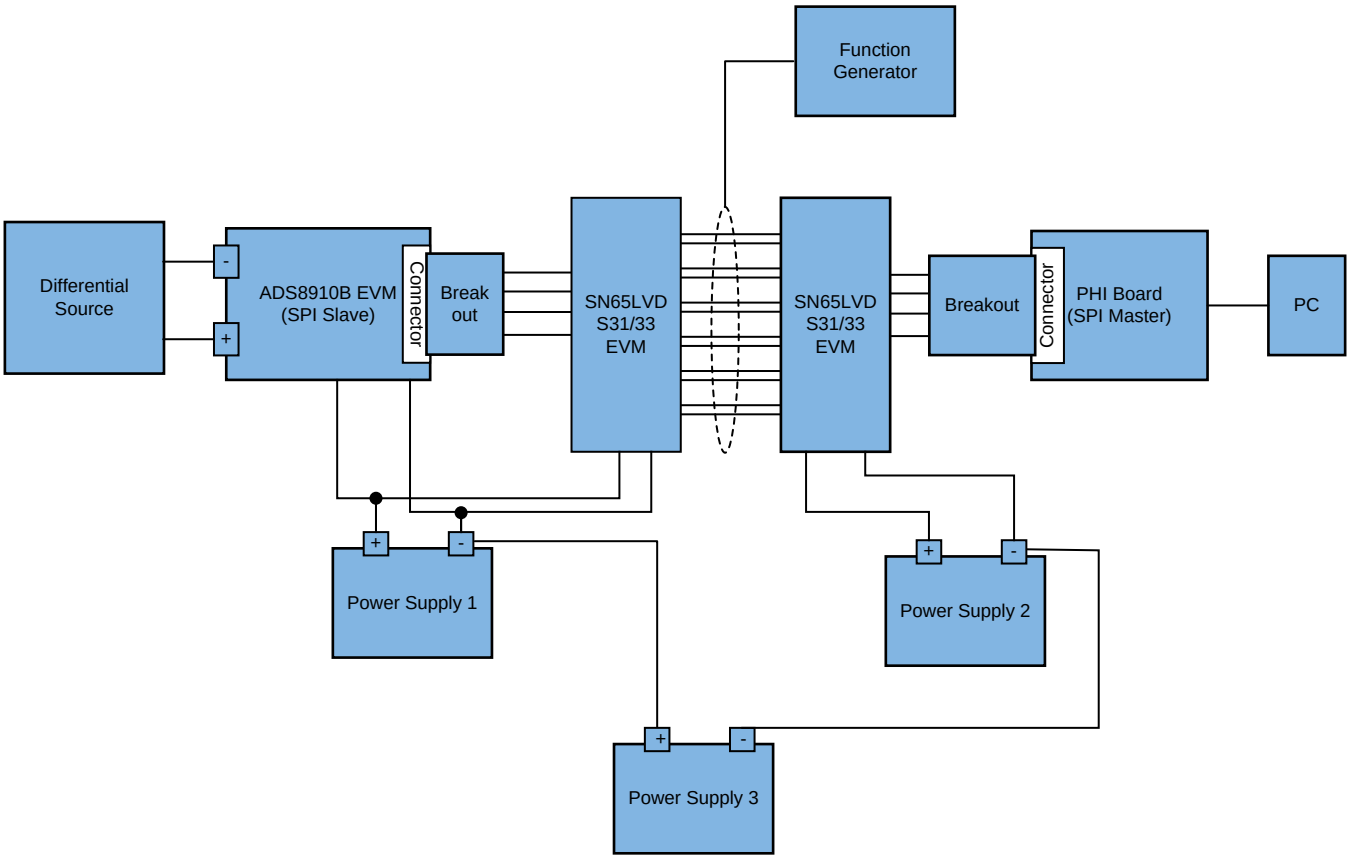


図 11. SPI Over LVDS Test Setup

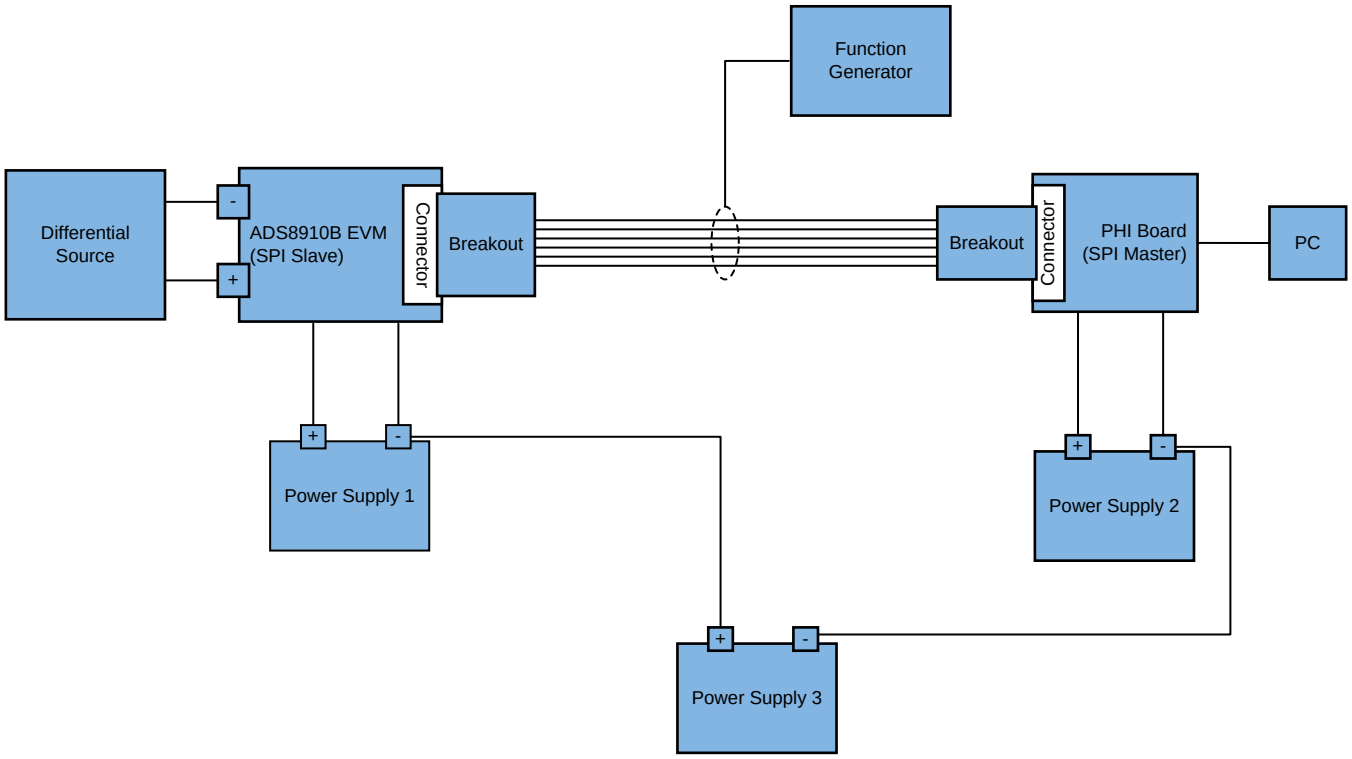


図 12. Single-ended SPI Test Setup

3.2.1.1 *Noise Immunity Test*

The goal of this test is to compare the performance difference between single-ended application, and with LVDS driver and receivers when external noise is coupled on the SPI bus. A signal generator is used to generate controlled transient noise. The amplitude of the generator is adjusted so that the noise applied is kept at 1Vpp, and the frequency is varied. The results are show in 表 4, and sample time domain analysis and spectral analysis are shown in 図 13.

表 4. Noise Immunity (varying noise frequency)

Noise Coupled	Cable Length(m)	Single-ended SPI SNR (dB)	SPI over LVDS SNR (dB)
No Noise	0.5	101	101
	3	Fail (1)	101
10KHz	0.5	99	99
	3	Fail	97
100KHz	0.5	82	83
	3	Fail	71
500KHz	0.5	67	69
	3	Fail	67
1MHz	0.5	58	68
	3	Fail	59
5MHz	0.5	39	61
	3	Fail	49
10MHz	0.5	31	52
	3	Fail	45

(1) Single-ended SPI application cannot support 3m cable length.

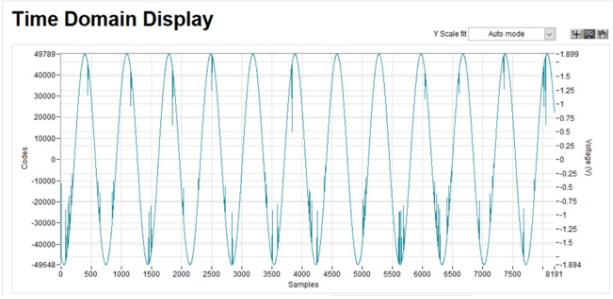


図 13. Single-ended Time Domain Analysis

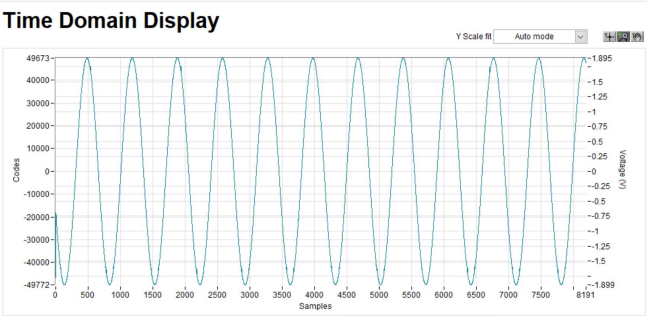


図 14. LVDS Time Domain Analysis

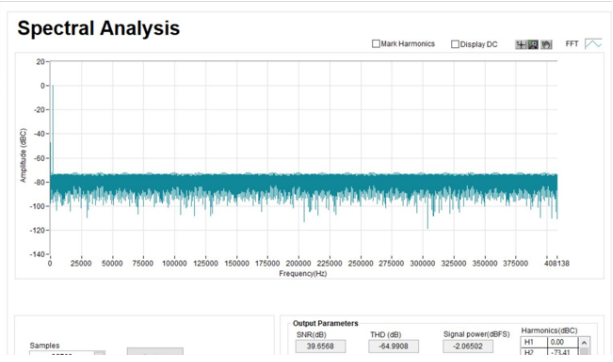


図 15. Single-ended Spectral Analysis Sample

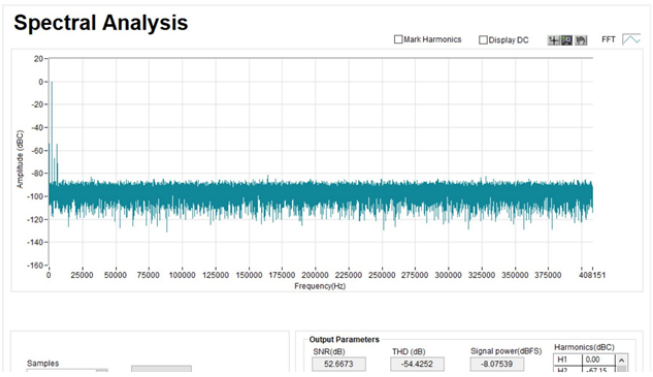


図 16. LVDS Spectral Analysis Sample

A similar test was performed, only this time noise amplitude is increased to 2Vpp, and the frequency is fixed at 10KHz. SPI over LVDS application is able to withstand the higher noise amplitude with a minimum of 45dB SNR. Single-ended SPI application cannot support the increased noise amplitude.

3.2.1.2 Ground Bounce Immunity Test

The goal of the test is to compare ground bounce immunity between single-ended SPI application and LVDS SPI application. The LVDS receiver SN65LVDS33 has a common-mode input range of -4V to 5 V. The test creates a ground potential difference between the ADC board, and the host board. The potential difference is increased while monitoring the signal SNR.

表 5. Ground Bounce Immunity Results

	Single-ended SPI	SPI Over LVDS
Ground Bounce Tolerance	-0.1V to +0.1V	-4V to 5V

3.2.1.3 SPI Interface Range Extension Test

The goal of this test is to extend the SPI communication distance, and compare the performance difference between single-ended cables and with LVDS driver and receivers. The effect of cable length on SPI communication is observed by monitoring the signal SNR, and a minimal of 40dB SNR is considered pass. Four different length of CAT5 cables are used to perform this test. Both single-ended and LVDS application transmit data successfully over 0.2m and 0.5m CAT5 cable, and SPI over LVDS application can support 1m and 3m CAT5 cable. However, single-ended SPI application cannot support 1m and 3m cable length due to crosstalk from adjacent signals and energy reflection from unterminated lines.

表 6. Cable Length Tested

Cable Length	Single-ended SPI	SPI over LVDS
0.2m	Pass	Pass
0.5m	Pass	Pass
1m	Fail	Pass
3m	Fail	Pass

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-060017.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-060017.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-060017.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-060017.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-060017.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-060017.

5 Related Documentation

1. Texas Instruments, *LVDS Owner's Manual*, Application Report (SNLA187)
2. Texas Instruments, *LVDS Design Notes*, Application Report (SLLA014)
3. Texas Instruments, *SN65LVDS31-33EVM User's Guide*, Application Report (SLLU016)
4. Texas Instruments, *ADS8910B EVM User's Guide*, Application Report (sbau268)
5. Texas Instruments, *SN65LVDS31 Data Sheet*, Application Report (SLLS261)
6. Texas Instruments, *SN65LVDS33 Data Sheet*, Application Report (SLLS490)
7. Texas Instruments, *ADS8910B Data Sheet*, Application Report (SBAS707)

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