参考資料

TI Designs: TIDA-01572
PC用ステレオ・オーディオのリファレンス・デザイン

概要

このステレオ・オーディオ・サブシステムは、TAS2770デバイスを使用して、PCアプリケーションのコーデック・ドライバ・ソリューションにおいて高品質のオーディオを生成します。このデバイスではスマート・アンプ・アルゴリズムを使用できるため、スピーカーの物理的な状況をリアルタイムで監視し、スピーカーの保護とともに音圧レベル(SPL)を最大化できます。このデザインには、実際に動作するレイアウトと、デザインに関する考慮事項が記載されているため、ソリューションを短時間で適用できます。

リソース

TIDA-01572	デザイン・フォルダ
TAS2770	プロダクト・フォルダ
TAS2770EVM-STEREO	ツール・フォルダ
TL760M33-Q1	プロダクト・フォルダ
TPS736	プロダクト・フォルダ
TPS62085	プロダクト・フォルダ

TI E2E™ Community

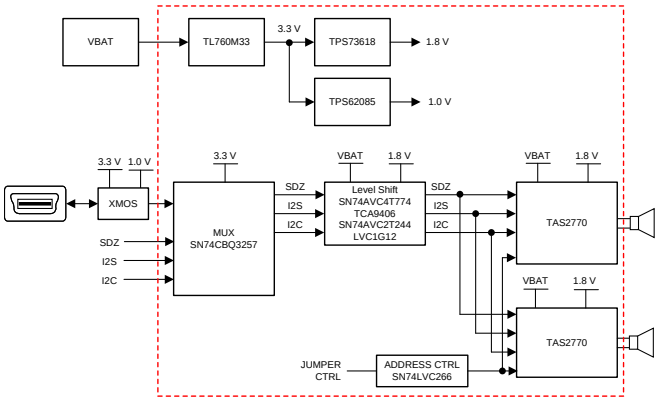
E2E™エキスパートに質問

特長

- 高性能のClass-Dアンプで、4.5V～16VのVBAT電源電圧範囲に対応
- 12.6Vにおいて4Ωに15Wの連続電力を供給 (1% THD+N)
- 診断用の電圧および電流検出機能を搭載
- アイドル時のチャネル・ノイズ32µV、拡散スペクトラム低EMIモードを搭載
- I²Sおよび SoundWire™入力に対応
- 小型の26ピンQFN (3.5mm×4mm)
- 入力多重化により複数の入力ソースをサポート

アプリケーション

- PCとノートPC
- ワイヤレス(BT)スピーカー
- サーモスタット
- ビデオ・ドアベル
- ビデオ通信システム



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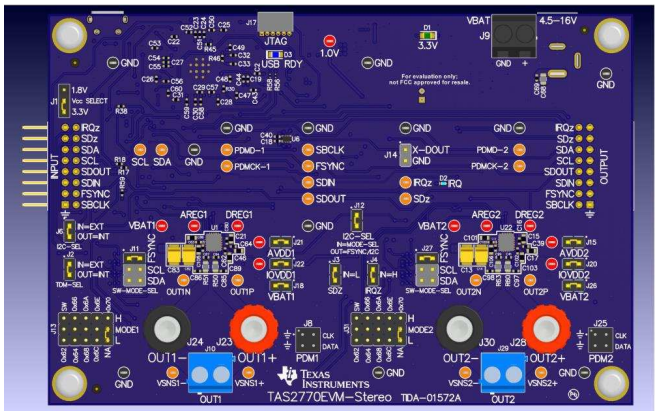

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1 System Description

This stereo audio subsystem uses two TAS2770 devices for improved audio capabilities over CODEC solutions. The TAS2770 is highly configurable to various audio input formats and has integrated speaker voltage and current sensing, which can be used to determine the maximum audio signal while simultaneously protecting against thermal and mechanical failure mechanisms.

This design incorporates a simple power solution to provide the necessary rails to operate and interface with the TAS2770 device. The user is only required to provide VBAT with a supply ranging from 4.5 V to 16 V.

For ease of use, this design incorporates an XMOS device, which allows for testing and development using a USB interface. If desired, however, the board can be set to accept external I^2C and I^2S bus connections to test using another system, such as an audio analyzer.

After connecting the device to a PC running PurePath™ Console 3 with the TAS2770-specific application, the user can quickly and easily configure the device. Among the many features of the TAS2770 is a battery protection output limiter. This limiter controls the automatic gain control to help maintain a quality audio output while preventing excessive demand on the battery system. Brownout protection is also included to protect the system from failing due to potential demands generated by the audio system. In addition, the designer can configure the inter-chip limiter alignment (ICLA) to ensure that, while in a multichannel configuration, all the channels that are actively grouped together attack equally to maintain audio continuity and balance.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETERS	SPECIFICATIONS
Power supply	4.5-V to 16-V DC
Digital interfaces	I^2S, I^2C, SoundWire, pulse desnity modulation (PDM)
TAS2770EVM stereo power consumption	3.2.2.1
SPL	3.2.2.2
Idle channel noise	3.2.2.2
THD+N versus frequency	3.2.2.2
THD+N versus power	3.2.2.2

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2 System Overview

2.1 Block Diagram

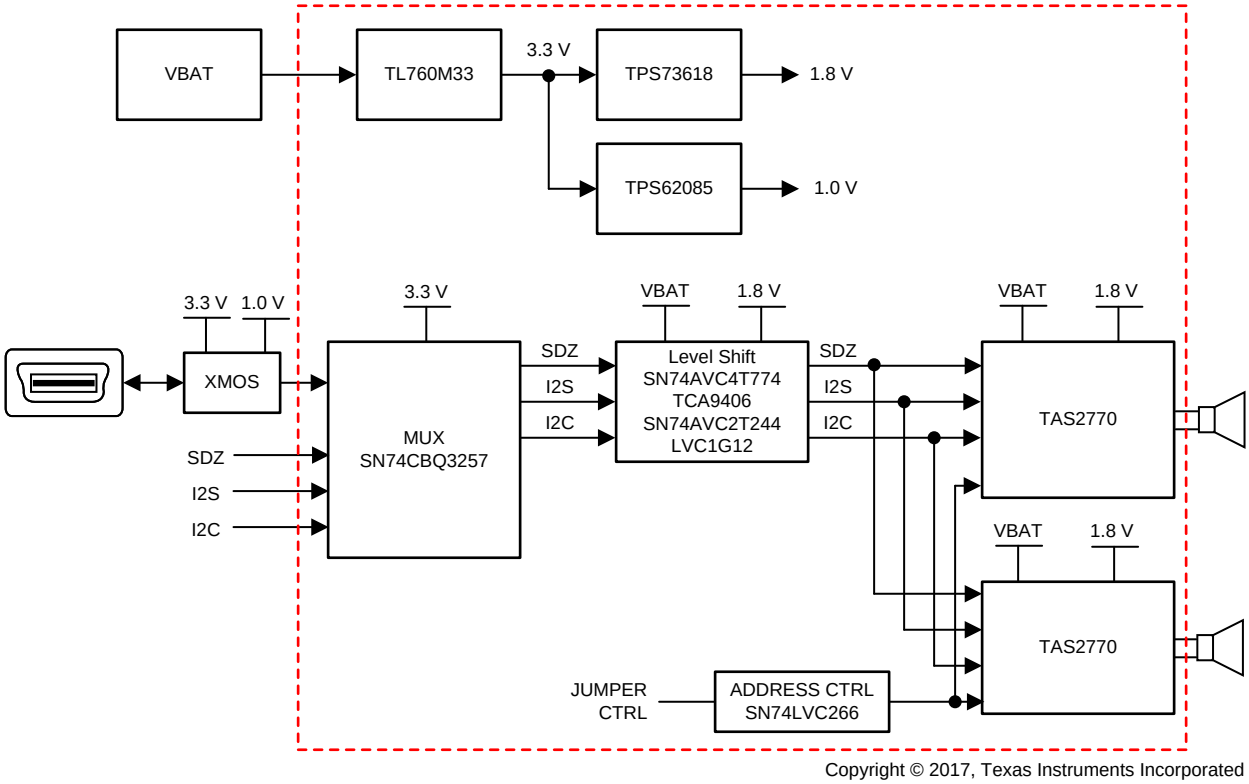

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図 1. TIDA-01572 Block Diagram

2.2 Design Considerations

2.2.1 RJQ Layout

The quad-flatpack, no-lead (QFN) HotRod™ package allows for improved connections to the die by eliminating wire bonds by attaching the die directly to the lead frame. This configuration has better electrical and thermal characteristics than standard QFN packages, which improves the overall power delivery and audio performance. The leads in this package type are customizable to best suit the requirements of the device. However, due to the unique shape of the pads and relative pitch available in this package, some caution must be exercised to ensure proper installation. Due to the relative proximity, shape, and size of pins 1 and 26 and pins 9 and 10, pins may become shorted through a solder bridge if too much solder is used to attach the device. Leave some margin near the inner extremities of the pads where the spacing is tight to help eliminate this risk. For more details regarding the use of this package and layout best practices, see *HotRod QFN Package PCB Attachment Application Report*. 図 2 shows an example layout. See the Gerber files in *Gerber Files* .

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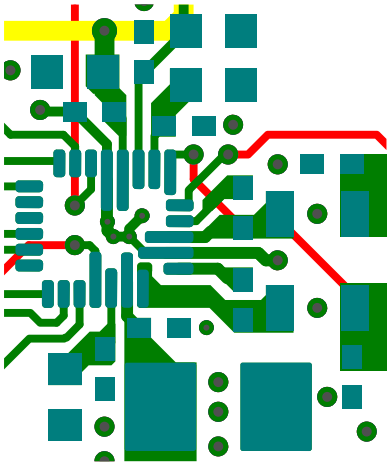

図 2. TIDA-01572 Reference Layout

Follow these guidelines during layout:

- Do not use vias for traces that carry high current. Such examples include the traces for VBAT, PGND, SPK_P, and SPK_M.
- Use epoxy-filled vias for the interior pads.
- Connect VSENSE+ and VSENSE– as close as possible to the speaker. VSENSE+ and VSENSE– must be connected between the electromagnetic interference (EMI) ferrite filter and the speaker if EMI ferrites are used on SPK_P and SPK_M.
- Use a ground plane with multiple vias for each terminal to create a low-impedance connection to GND for minimum ground noise.
- Use supply decoupling capacitors as shown in the schematics (see *Schematics*).
- If using EMI ferrites, place them close to the device.

2.2.2 Power

This device operates from a 4.5-V to 16-V VBAT supply where each channel is capable of driving a 4-Ω load with up to 15 W. A barrel jack connection is available on this evaluation module (EVM) for convenience; however, when using this connection, note the importance of selecting a supply with an appropriate current limit for the desired power levels. This connection is ideal for use in portable demonstrations.

Screw-down terminals that can accommodate other supplies are also available. This terminal is ideal for lab testing while using a programmable bench top supply.

The onboard power supplies accept voltages within the specified operating range to generate 1-V, 1.8-V, and 3.3-V rails. These rails drive the various peripherals to the TAS2770 and drive the AVDD and IOVDD pins of the device.

2.2.3 Digital Audio Inputs

For ease of use, this design implements a USB controller to host I^2S and I^2C interfaces. When connected to a PC with PurePath™ Console 3 (PPC3) installed, a convenient and easy-to-use graphical user interface (GUI) is available to assist the user in configuring the device.

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In addition, there is onboard multiplexing that allows the user to provide inputs for both of these buses from an external source. If desired, multiple boards may be connected together to create a four-, six-, or eight-channel configuration. The user can configure the TAS2770 device for ICLA, which allows each device that shares the same SDOUT data line to monitor the state of other channels. Devices that are programmed to monitor each other's limiter settings act together to provide consistent audio levels among all channels.

For more information, see 3.1.3.3.

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2.3 Highlighted Products

2.3.1 TAS2770

The TAS2770 is a mono, digital input Class-D audio amplifier optimized for efficiently driving high peak power into small loudspeakers. The Class-D amplifier is capable of delivering 14.2 W of peak power into a 4-Ω load while sustaining 11.6 W continuously with less than 0.03% THD+N at a battery voltage of 12.6 V.

Integrated speaker voltage and current sense allows for real-time monitoring of loudspeaker behavior. A battery-tracking, peak-voltage limiter with brownout prevention optimizes amplifier headroom over the entire charge cycle of 2S or 3S battery systems.

Up to eight devices can share a common bus using either I^2S or test data management (TDM) + I^2C.

The TAS2770 device is available in a 26-pin, 0.4-mm pitch QFN for a compact printed-circuit board (PCB) footprint.

2.3.2 TL760M33

The TL760 is an integrated linear-voltage regulator featuring operation from an input as high as 30 V. The TLV760 has a maximum dropout of 1.2 V at the full 100-mA load across the operating temperature. Standard packaging for the TLV760 is the three-pin, SOT-23 package.

The TL760 is available in 3.3 V, 5 V, 12 V, and 15 V. The SOT-23 packaging of the TL760 series allows the device to be used in space-constrained applications. The TL760 is a small-size alternative to the LM78Lxx series and similar devices. This application uses the 3.3-V version of this device.

The TL760 is designed to bias digital and analog circuits in applications that are subject to voltage transients and spikes up to 30 V—for example, appliances and automation applications. The device has robust internal thermal protection, which protects itself from potential damage caused by conditions like short to ground, increases in ambient temperature, high load, or high dropout events.

2.3.3 TPS73618

The TPS736xx family of LDO linear voltage regulators uses a new topology—an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low equivalent series resistance (ESR) and allows operation without a capacitor. The topology also provides high reverse blockage (low reverse current) and ground-pin current that is nearly constant over all values of output current.

The TPS736xx uses an advanced BiCMOS process to yield high precision while delivering low dropout voltages and low ground-pin current. Current consumption, when not enabled, is under 1 µA and ideal for portable applications. The low output noise (30 μV_{RMS} with 0.1-µF CNR) is ideal for powering voltage-controlled oscillators (VCOs). These devices are protected by a thermal shutdown and foldback current limit.

The TPS73618 generates a 1.8-V supply in this application to provide AVDD and IOVDD.

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2.3.4 TPS62085

The TPS62085 device is a high-frequency synchronous step-down converter optimized for a small solution size and high efficiency. With an input voltage range of 2.5 V to 6 V, this device supports common battery technologies. The device focuses on high-efficiency step-down conversion over a wide output current range. At medium-to-heavy loads, the converter operates in pulse-width modulation (PWM) mode and automatically enters power save mode operation at light load to maintain high efficiency over the entire load current range.

To address the requirements of system power rails, the internal compensation circuit allows a large selection of external output capacitor values ranging from 10 µF to 150 µF. Together with DCS-Control architecture, excellent load transient performance and output voltage regulation accuracy are achieved. The device is available in a 2-mm × 2-mm QFN package.

2.4 System Design Theory

TAS2770 is a mono, digital input Class-D amplifier. To achieve stereo or higher channel-count configurations, multiple devices can share the I^2S data bus to provide ICLA. This design pairs two units to accomplish the stereo application, but the designer may pair multiple boards to create four-, six-, or eight-channel solutions.

The VBAT supply range of TAS2770 pairs well into the PC and notebook space. The built-in limiter helps with battery tracking to automatically adjust gain to keep the outputs within the user-specified limits. When ICLA is implemented, the paired devices respond to changes in each other's gain settings to provide balanced control while smoothly adjusting to stay within the operating limits of the battery supply.

This design is intended to accommodate uses for evaluating performance in a controlled environment and to easily provide access to audio streaming over USB. The design also allows the user to drive the inputs from an audio analyzer or other system with accessible I^2S or I^2C signals.

Suitable onboard power is also provided to simply integration and testing. The user is only required to provide a VBAT voltage in the range of 4.5 V to 16 V.

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3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

- TAS2770EVM stereo board
- 4.5-V to 16-V wired DC bench top supply or barrel jack
- Speakers rated at or above expected output power
- USB-A to USB-B micro cord

3.1.2 Software

- PurePath Console 3 (PPC3)—available from MySecureSoftware
- TAS2770 PPC3 App—downloaded within PPC3
- Media player

3.1.3 User Configuration

3.1.3.1 Stereo Setup

1. Install PurePath Console 3 with the TAS2770EVM-STEREO plug-in.
2. Connect the first speaker to J10 on the EVM. Alternatively, J23 and J24 can be used for speaker connections.
3. Connect a second speaker to J29 on the EVM. Alternatively, J28 and J30 can be used for speaker connections (see 図 3).
4. Attach a power supply to connector J9. There is also an alternate barrel jack connector (J19) adjacent to this connector.
5. Set jumper J13 to select the desired I^2C address for channel 1.
6. Set jumper J31 to select the desired I^2C address for channel 2.
7. Connect the EVM to a Windows® 7+ PC with a micro-USB cable (J16).

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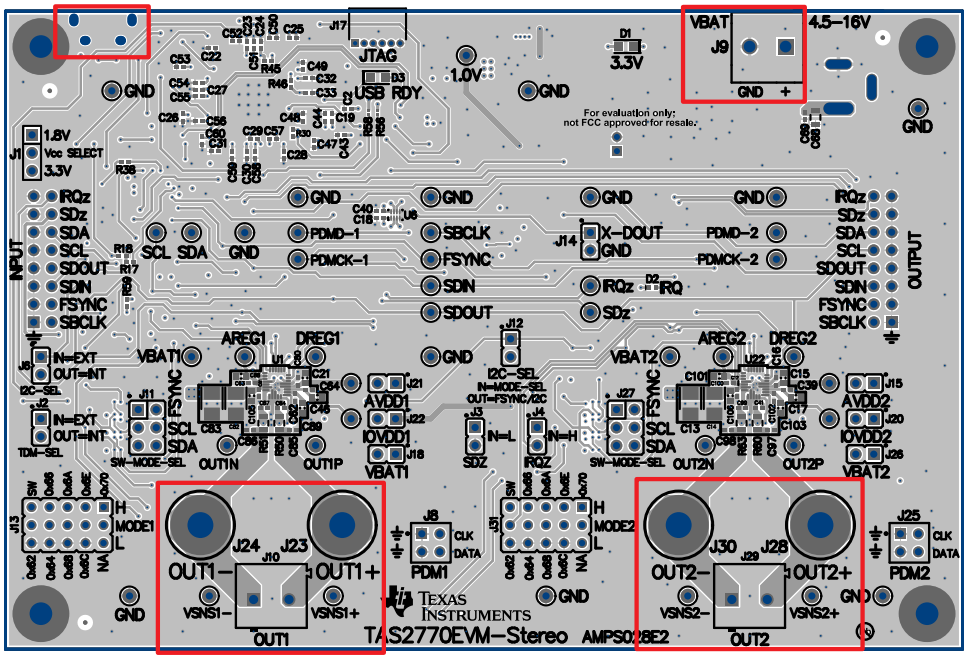

図 3. TAS2770EVM-STEREO Stereo Configuration

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8. Verify that the EVM is the default playback device by opening the sound dialog from the Windows Control Panel (see 図 4).

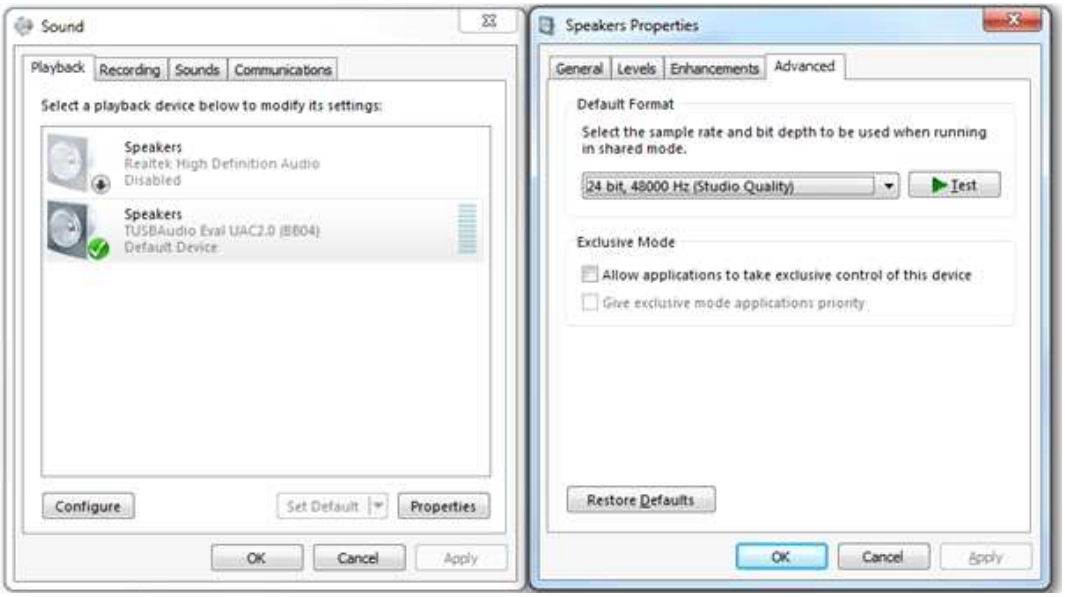

図 4. Playback Device Settings

9. Set the sampling rate using the Windows setting by opening *Properties → Advanced*. The TAS2770EVM-STEREO supports 44.1-KHz and 48-KHz sampling rates.
10. Set the bit depth as desired using the *Texas Instruments Audio Control Panel*, which is accessible from the system tray shown in 図 5.
11. Proceed to configure the device using PPC3.

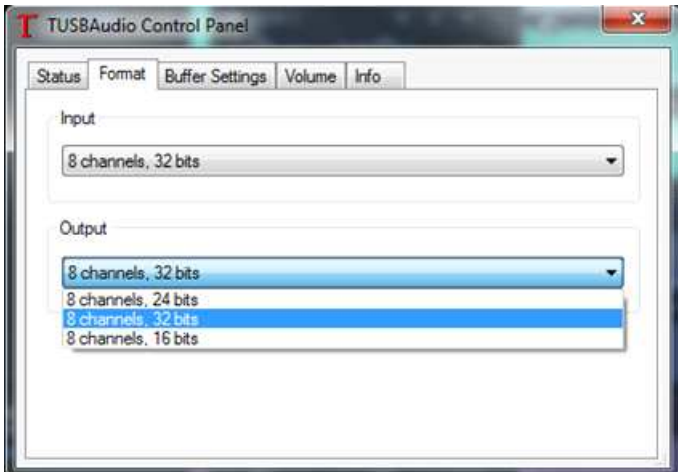

図 5. Texas Instruments Audio Control Panel

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3.1.3.2 Mono Setup

1. Install PurePath Console 3 with the TAS2770EVM-STEREO plug-in.
2. Connect the first speaker to J10 on the EVM (see 図 6). Alternatively, J23 and J24 can be used for speaker connections.
3. Attach a power supply to connector J9. There is also an alternate barrel jack connector (J19) adjacent to this connector.
4. Set jumper J13 to select the desired I^2C address for channel 1.
5. Connect the EVM to a Windows 7+ PC with a micro-USB cable (J16).

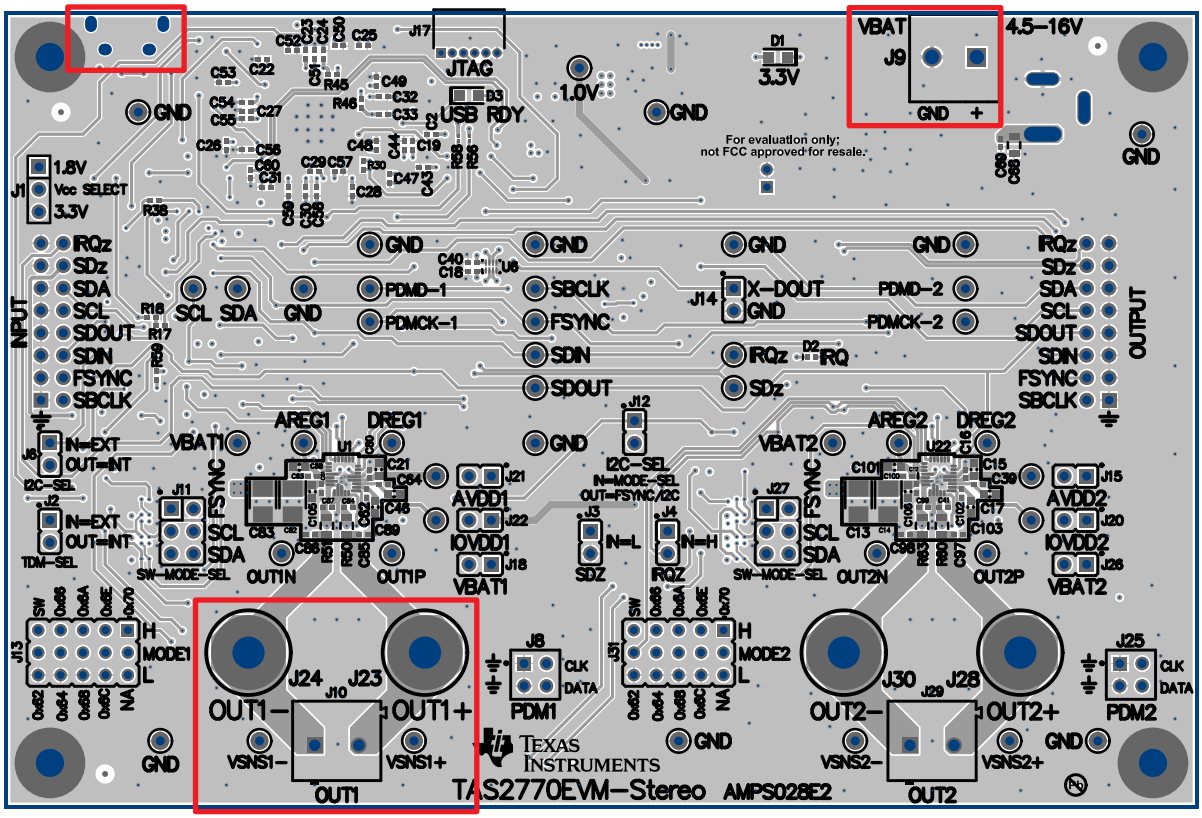

図 6. TAS2770EVM-STEREO Mono Configuration

6. Verify that the EVM is the default playback device by opening the sound dialog from the Windows Control Panel, as shown in 図 4.
7. Set the sampling rate using the Windows setting by opening *Properties* → *Advanced*. The TAS2770EVM-STEREO supports 44.1-KHz and 48-KHz sampling rates.
8. Set the bit depth as desired using the Texas Instruments Audio Control Panel accessible from the system tray shown in 図 5.
9. Proceed to configure the device using PPC3.

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3.1.3.3 Multichannel Setup

1. Install PurePath Console 3 with the TAS2770EVM-STEREO plug-in
2. Connect up to four TAS2770EVM-STEREOs together using connectors J5 and J7 (see 図 7).
3. Attach a power supply to each board.
4. The left-most board must have jumpers set to match the stereo configuration. On all other boards, insert a jumper on J2 and J6 (see 図 7 for details).
5. Set jumpers J13 and J31 on each board to a unique address.
6. Configure the sampling rate and bit depth as discussed in 3.1.3.2 steps six through eight.
7. Proceed to configure the device using PPC3.
8. Connect the left-most EVM to a Windows 7+ PC with a micro-USB cable (J16).

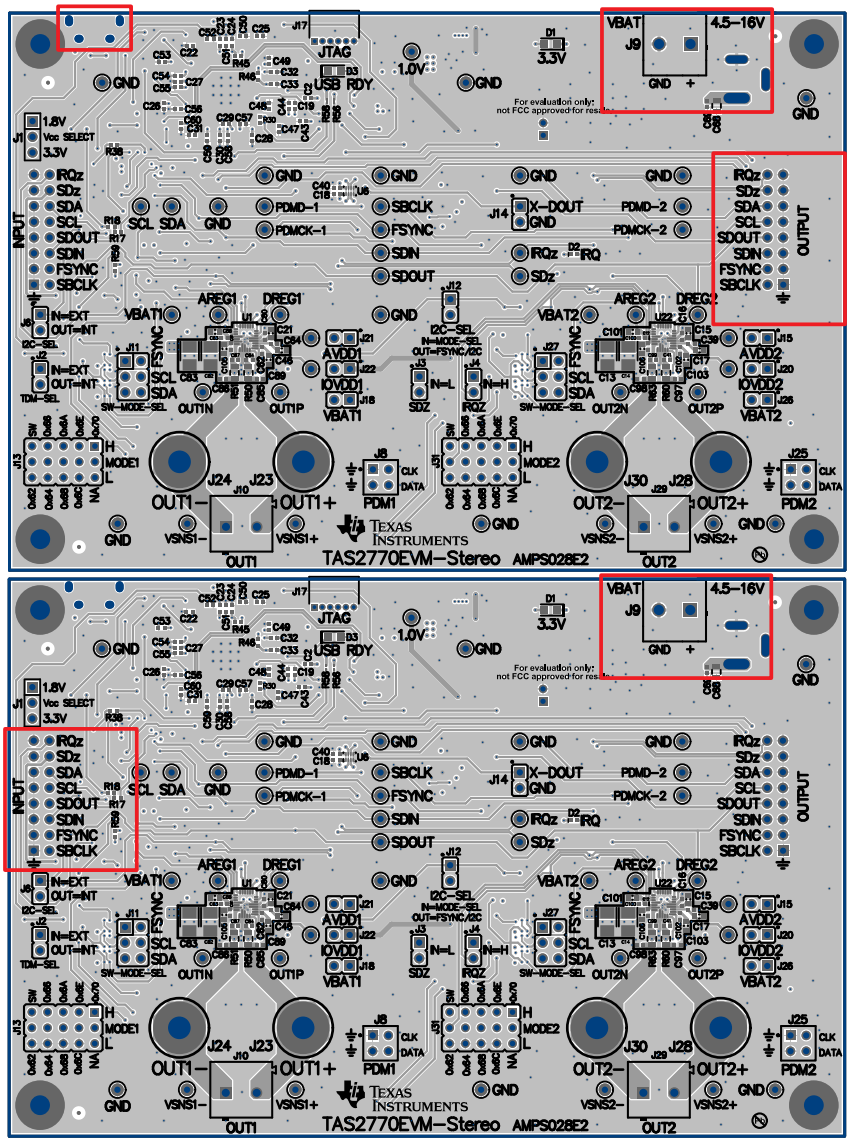

図 7. Multichannel Setup

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3.1.3.4 Digital Audio Interfaces

The various digital audio interfaces on the TAS2770 reference board can be selected through hardware settings and software settings. Several headers close to the TAS2770 device allow access to the following digital audio signals:

- I^2S Data Out (SDOUT) from the TAS2770 (for example, current and voltage sense data)
- I^2S Data In (SDIN) to the TAS2770
- I^2S Word Clock or frame sync (FSYNC)
- I^2S Bit Clock (SBCLK)
- PDM Clock (PDMCLK0)—Optional input source for TAS2770
- PDM Clock (PDMCLK1)—Optional input source for TAS2770
- PDM Data (PDMD0)—Optional input source for TAS2770
- PDM Data (PDMD1)—Optional input source for TAS2770
- I^2C Clock (SCLK)
- I^2C Data (SDA)

TAS2770 can be configured for SoundWire mode:

- SoundwireSM clock—SBCLK
- SoundwireSM data—SDOUT
- SoundwireSM address—SDA
- SoundwireSM address—FSYNC
- SoundwireSM address—SCL

A jumper inserted in the SW slot of J13 sets the TAS2770 device to SoundWire mode. Then, the designer can set J11 as desired to configure the device address.

Jumpers J2 and J6 control the selection between the USB (internal) and external inputs. These jumpers set the TDM and I^2C, respectively.

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3.1.3.4.1 Digital Audio Interface Selection

3.1.3.4.1.1 USB

The TAS2770 reference board contains an XMOS microcontroller (MCU) that acts as a USB human interface device (HID) and USB-class audio interface. To select USB, remove jumpers J6 and J2. Insert a jumper in J12.

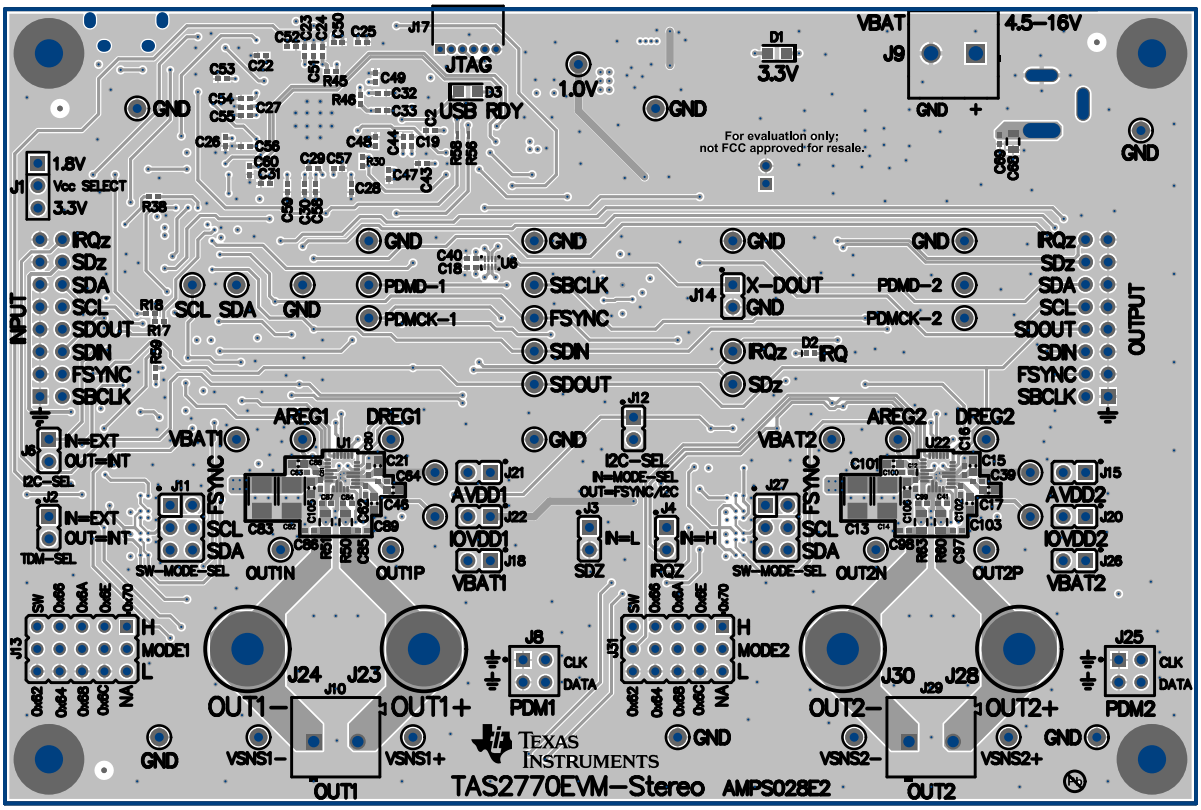

図 8. USB Audio Input Configuration

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3.1.3.4.1.2 Direct (AP/PSIA)

Insert a jumper on J2 and connect the external digital audio source (for example AP or PSIA) to the external input header pin. The odd-numbered pins on this header provide a ground for each signal. 図 9 shows this configuration. Note that the jumper setting for J1 must reflect the logic level of the external source.

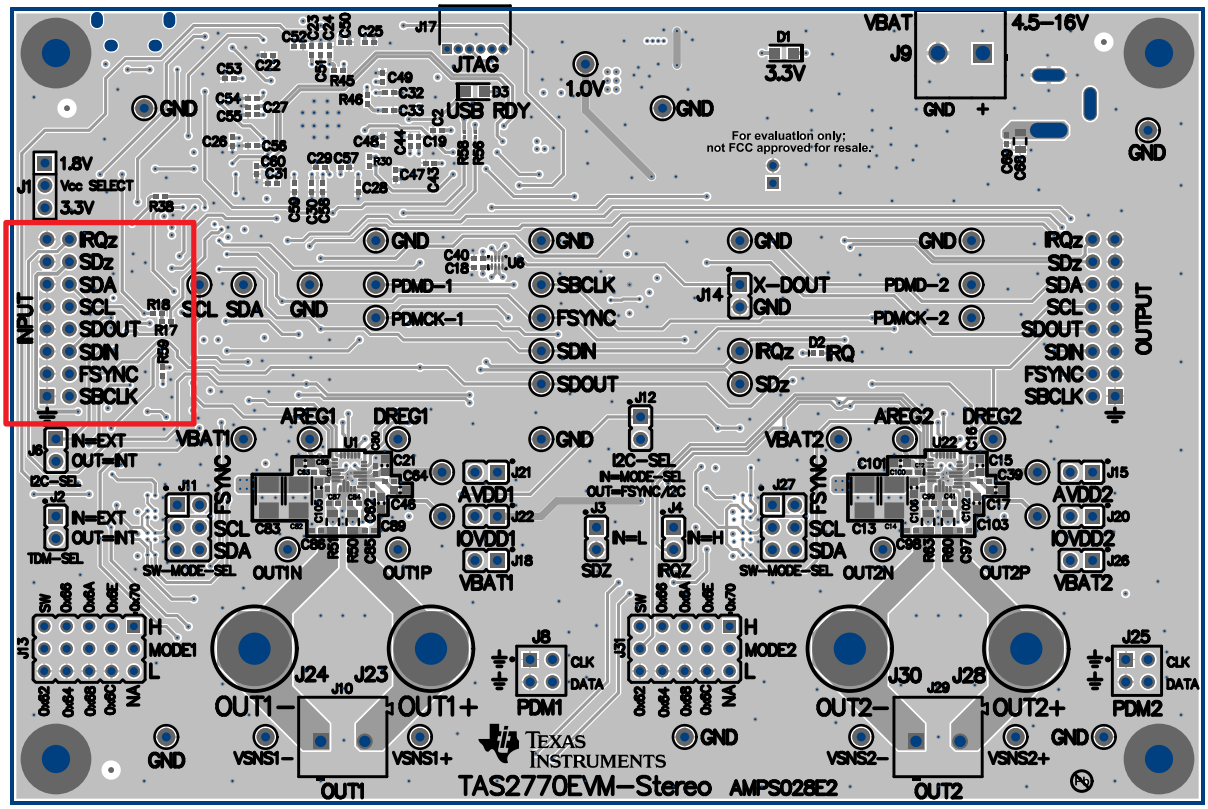

図 9. AP/PSIA Input Configuration

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3.2 Testing and Results

3.2.1 Test Setup

Stereo audio for PC design testing was carried out using the TAS2770EVM-STEREO configured for external I^2S inputs while using I^2C inputs controlled over USB and the PPC3 audio.

Acoustic tests were performed using 8-Ω compatible speakers with a recommended operating power of 25 W at a distance of 1 m.

Electrical tests were performed using an Audio Precision® 2700 series analyzer with the accompanying AUX-0025 passive filter. The TAS2770 was loaded with an 8-Ω resistor in series with 33-µH inductance to emulate a real speaker. All typical characteristics for the devices are measured using the bench EVM and an Audio Precision SYS-2722 Audio Analyzer. A PSIA interface allows the I^2S interface to be driven directly into the SYS-2722. The *SPEAKER OUT* terminal is connected to the Audio Precision Analyzer inputs as shown in 図 10. A differential to single-ended (D2S) filter with a first-order passive pole at 120 kHz is added. This addition ensures that the high-performance Class-D amplifier detects a fully-differential-matched loading at its outputs and while detecting no measurable degradation in performance due to the loading effects of the AUX filter on the Class-D outputs.

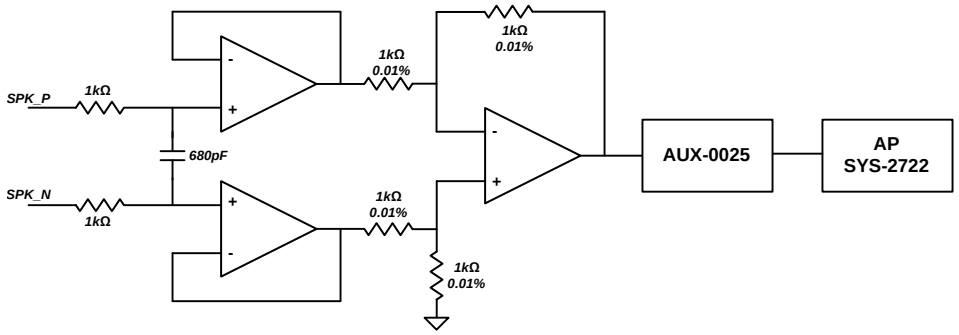

図 10. Differential to Single-Ended (D2S) Filter

The design was powered using an Agilent® bench top supply set to 16 V. Current measurements were taken using an Agilent digital multimeter.

3.2.2 Test Results

3.2.2.1 Power Consumption

表 2. TIDA-01572 Power Consumption

PARAMETER	CONDITIONS	SUPPLY	VALUE	UNITS
TAS2770 EVM-Stereo current consumption	Hardware shutdown	EVM supply	178	mA
	Software shutdown		180	
	Idle channel		208	mA

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表 2. TIDA-01572 Power Consumption (continued)

PARAMETER	CONDITIONS	SUPPLY	VALUE	UNITS
TAS2770 current consumption	Hardware shutdown	VBAT	0.2	µA
		AVDD	0.1	
		IOVDD	0.1	
	Software shutdown	VBAT	0.5	µA
		AVDD	9.1	
		IOVDD	0.1	
	Idle channel	VBAT	5.25	mA
		AVDD	9.72	
		IOVDD	8.9	µA

3.2.2.2 Amplifier Performance

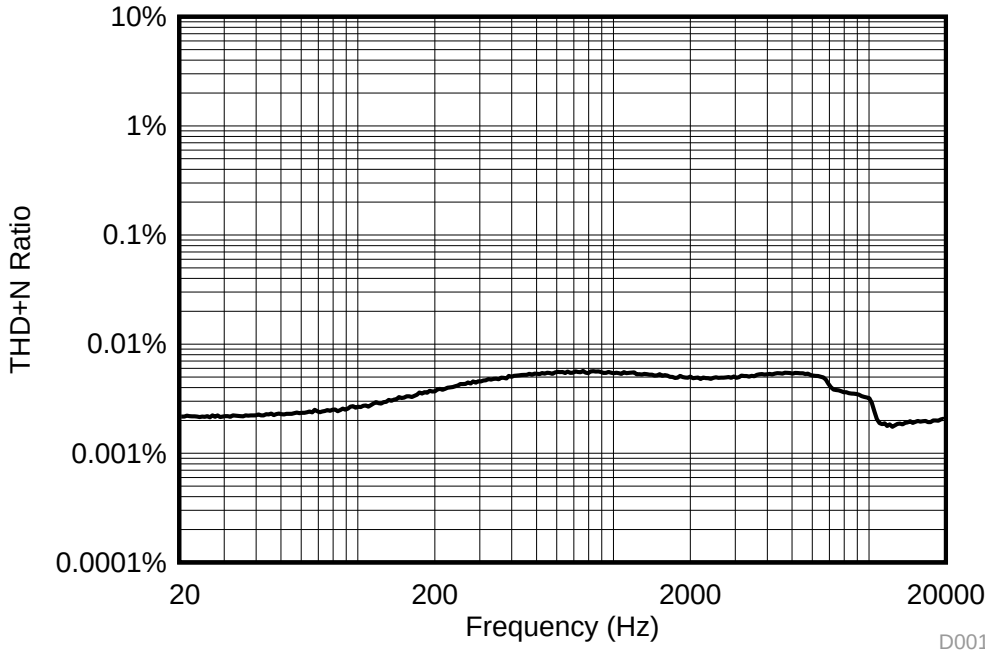

図 11. TIDA-01572 THD+N versus Frequency at 1 W, VBAT = 12 V

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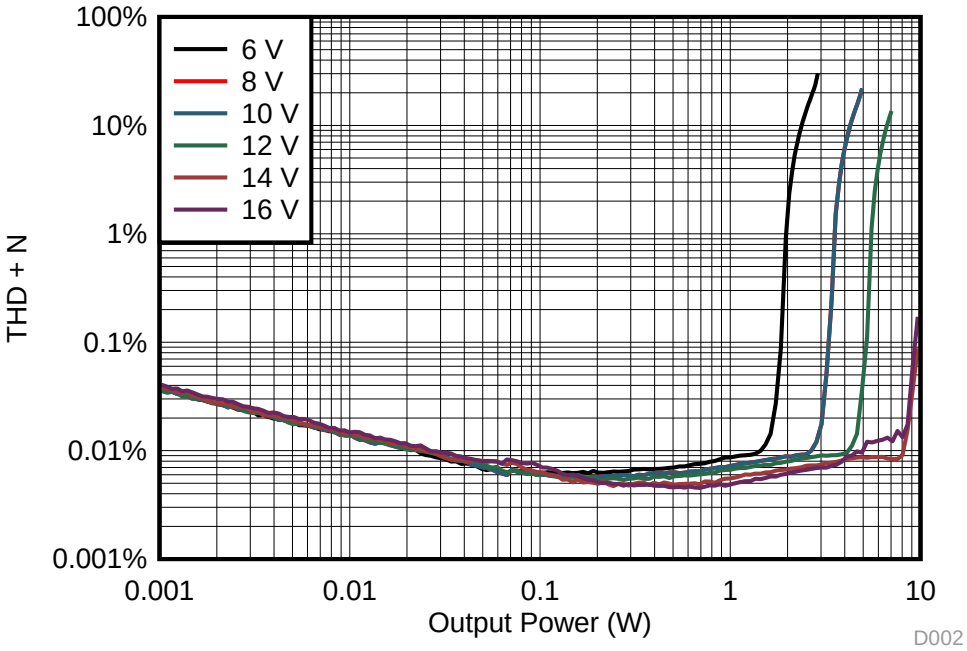

図 12. TIDA-01572 THD+N versus Output Power at 1 kHz

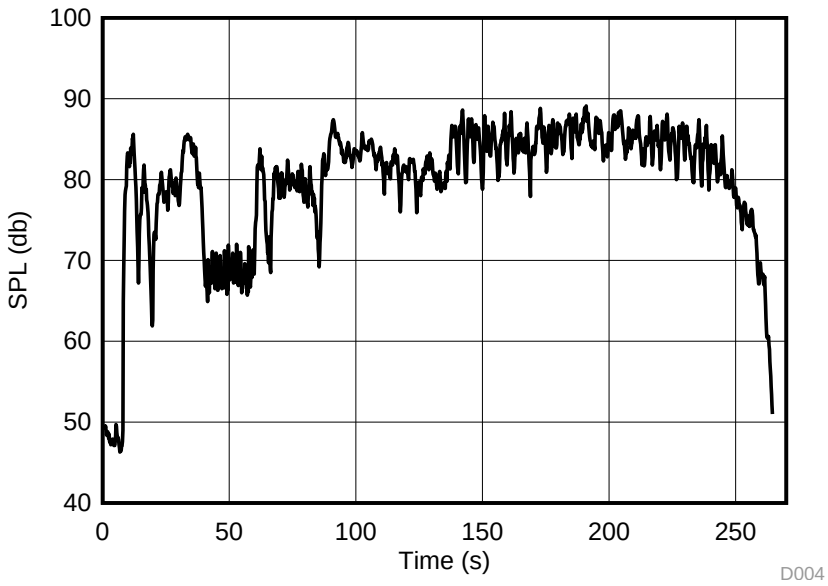

図 13. TIDA-01572 SPL at 1 m, VBAT = 12 V, While Playing Music

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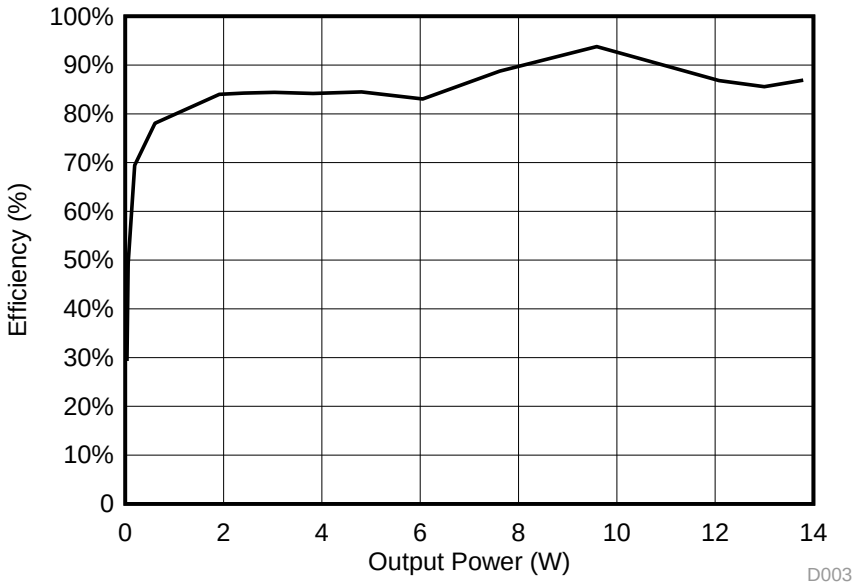

図 14. TIDA-01572 Power Efficiency, VBAT = 16 V

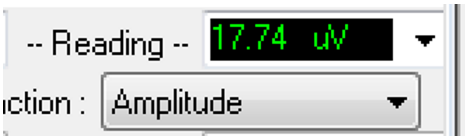

図 15. Idle Channel Noise, VBAT = 12 V (1)

(1) The final, correct measurement is 35.48 µV; however the test circuit divides this value in half. Note that a value of 17.74 µV is too low.

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01572.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01572.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

4.3.1.1 TAS2770 Reference Board PCB Layout

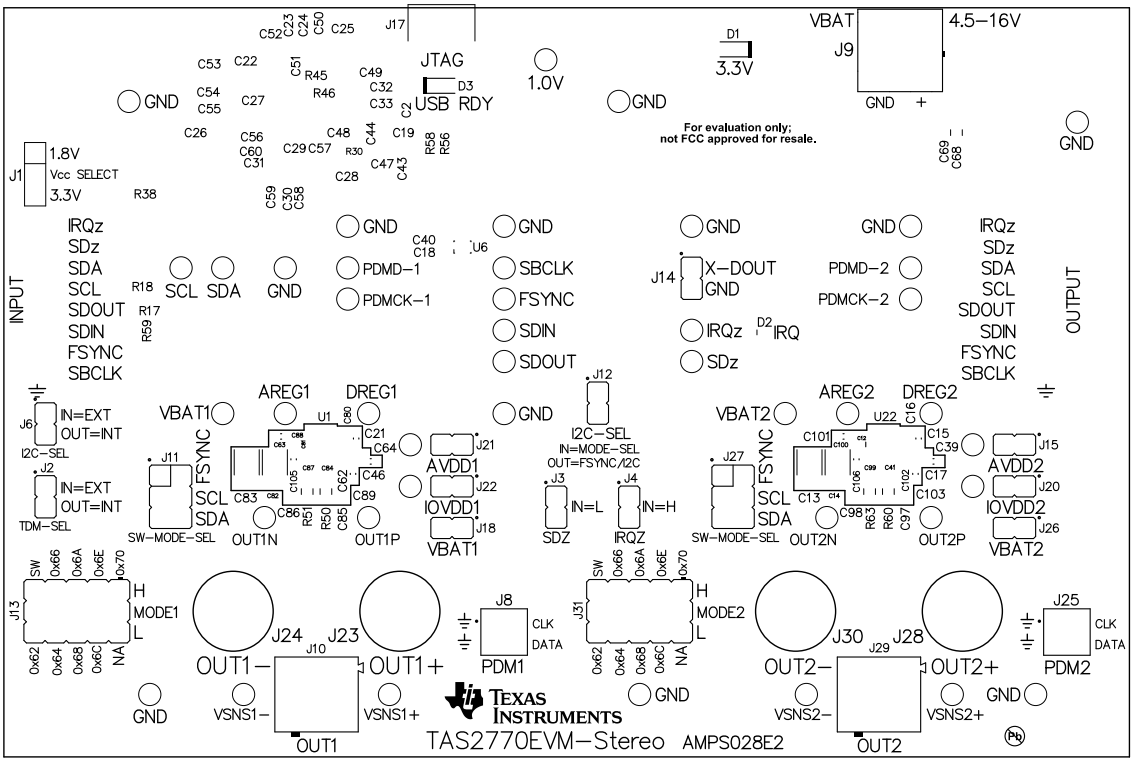

図 16. PCB: Top Silkscreen

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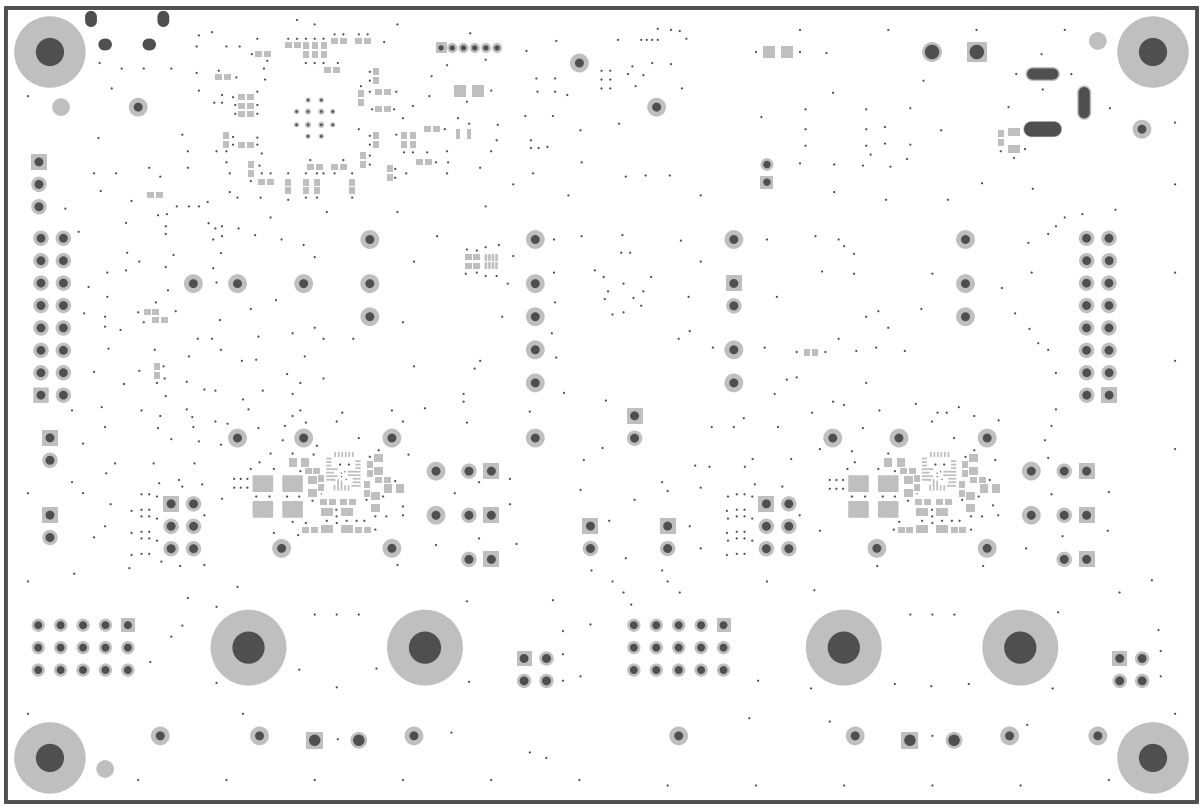

図 17. PCB: Top Solder Mask

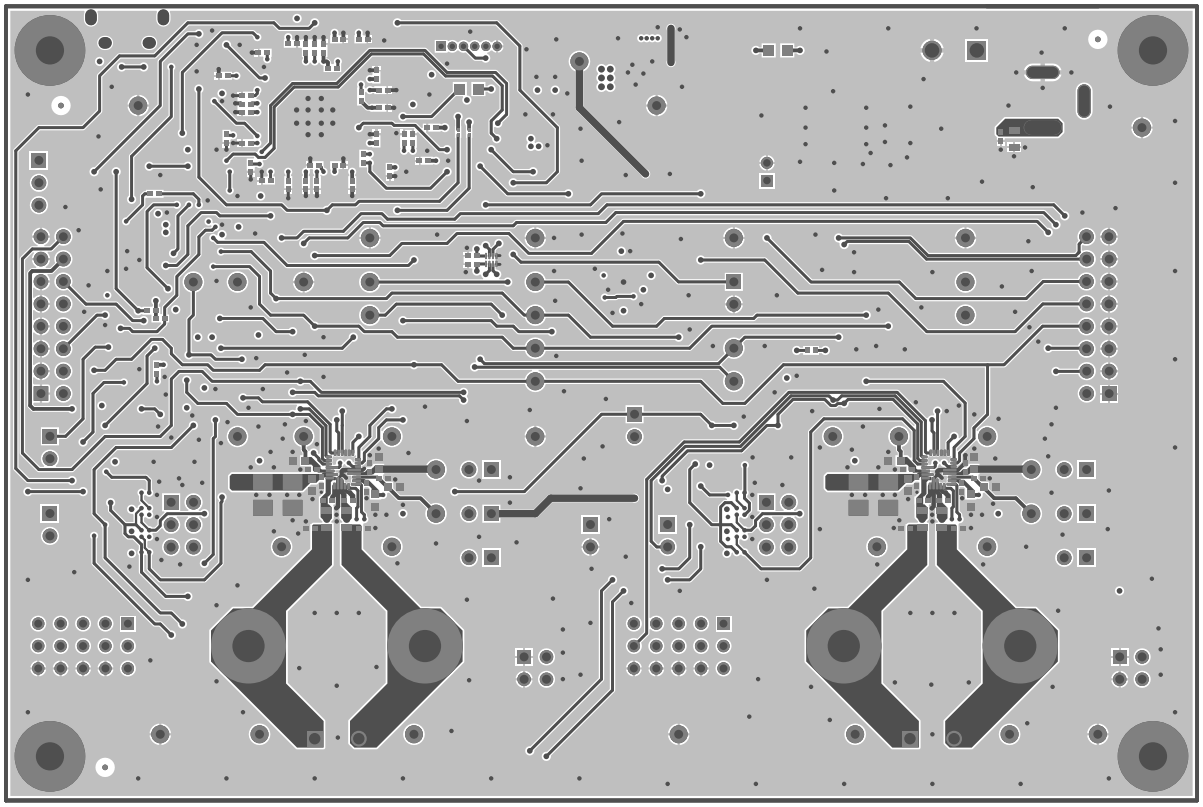

図 18. PCB: Top Copper

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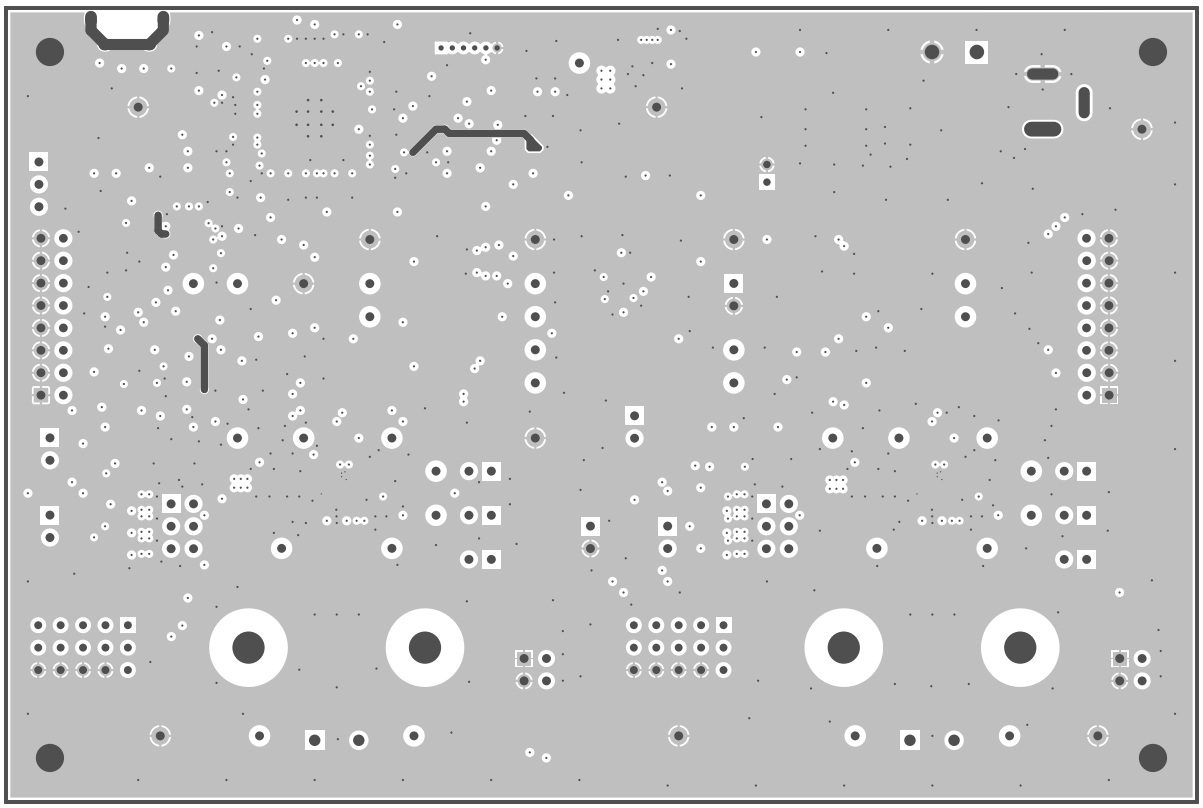

図 19. PCB: Copper Layer 2

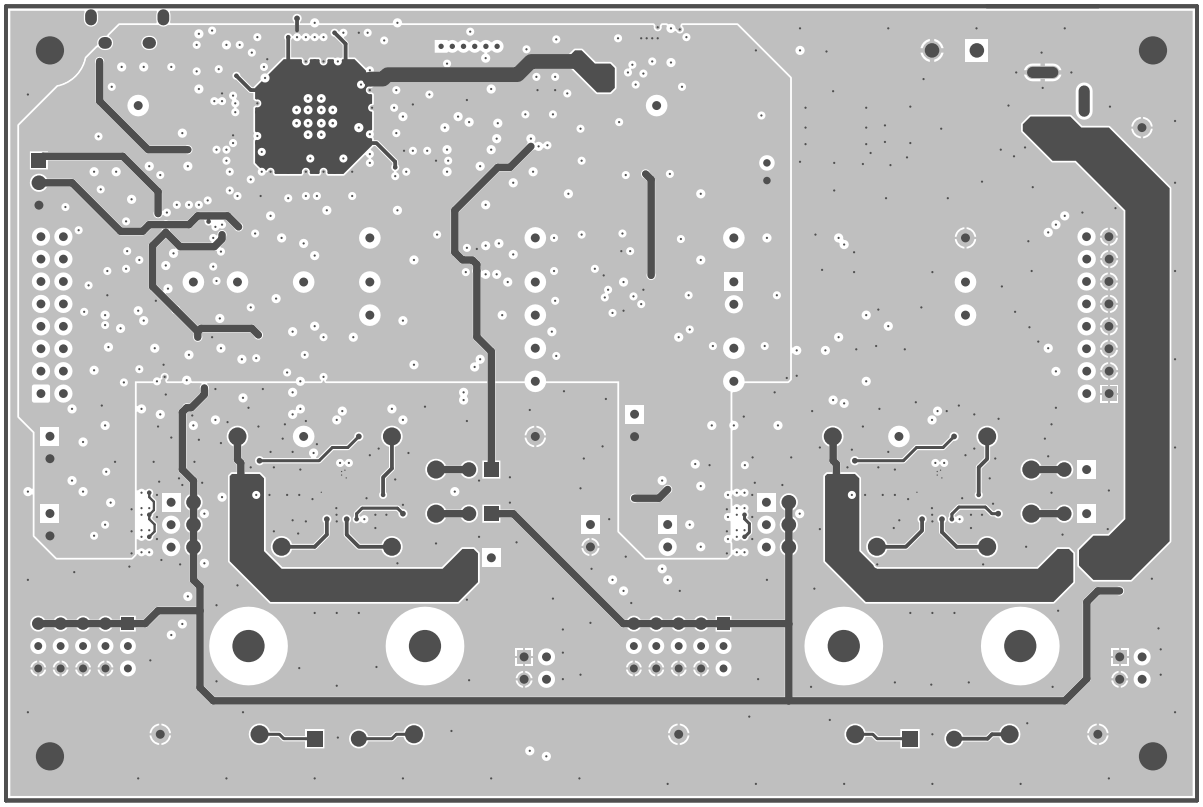

図 20. PCB: Copper Layer 3

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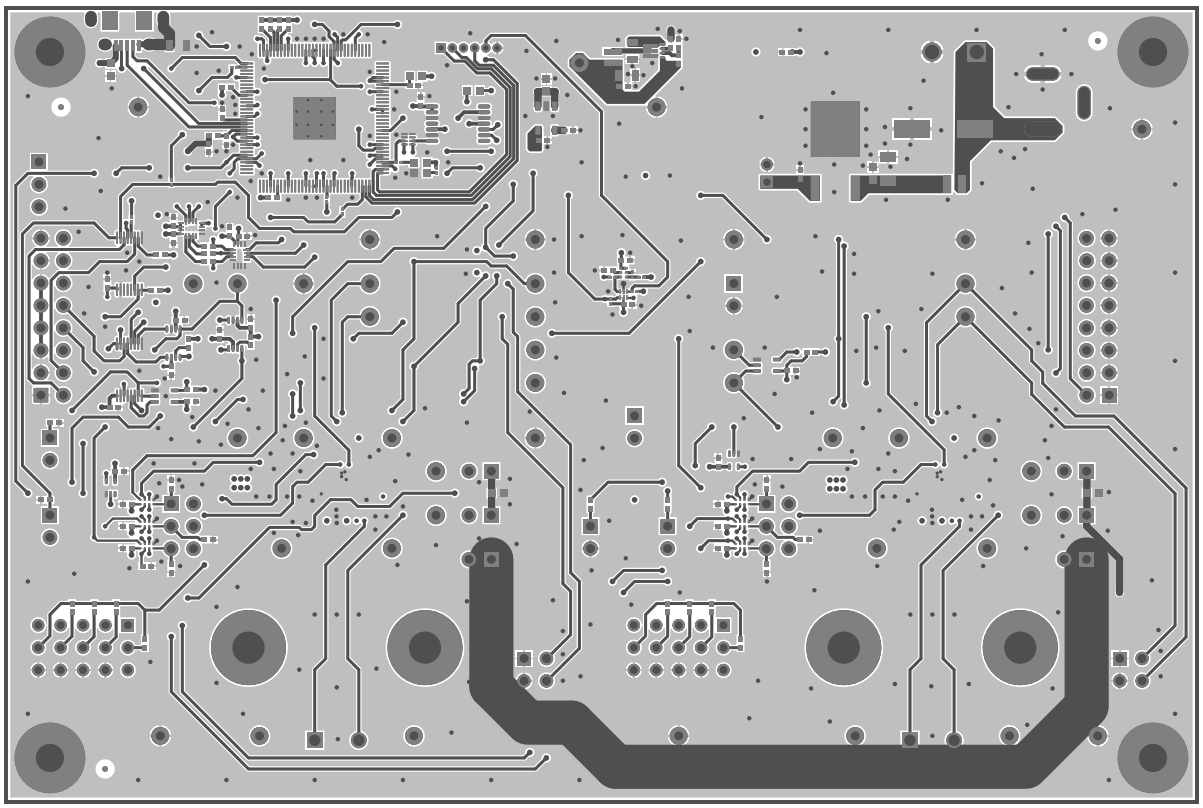

図 21. PCB: Bottom Copper

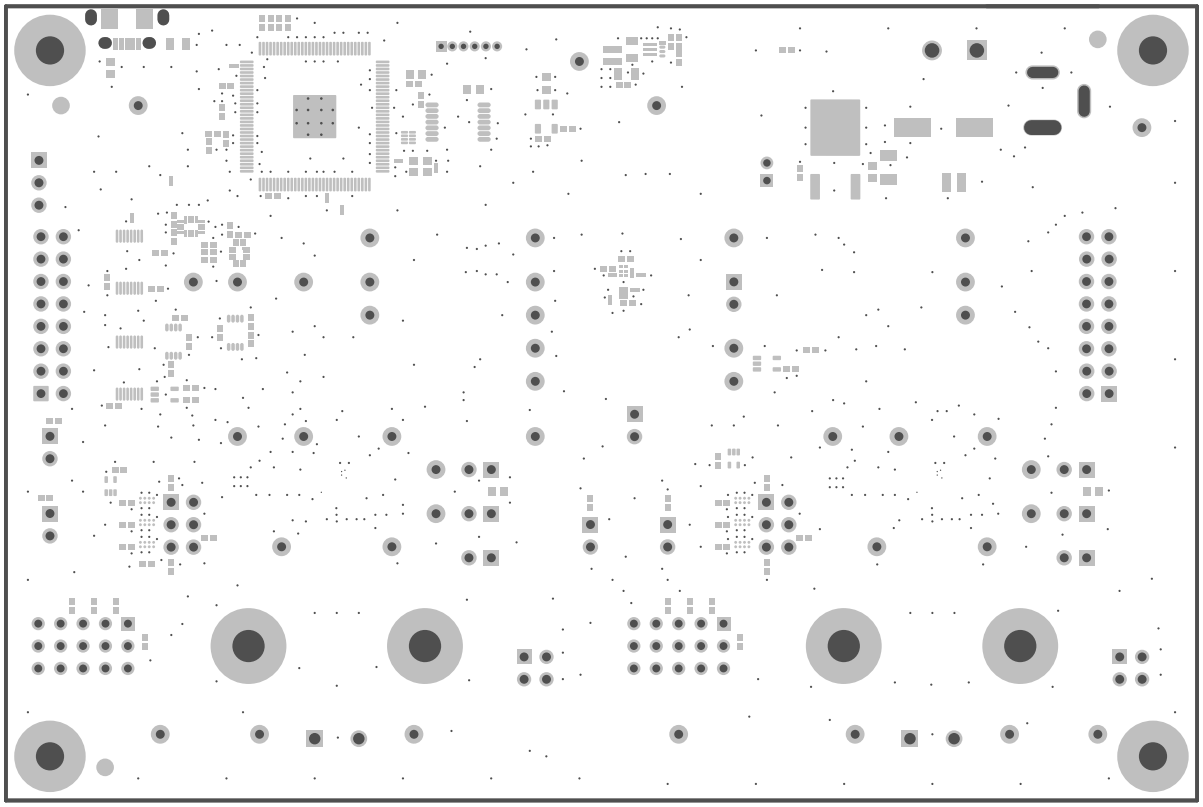

図 22. PCB: Bottom Solder Mask

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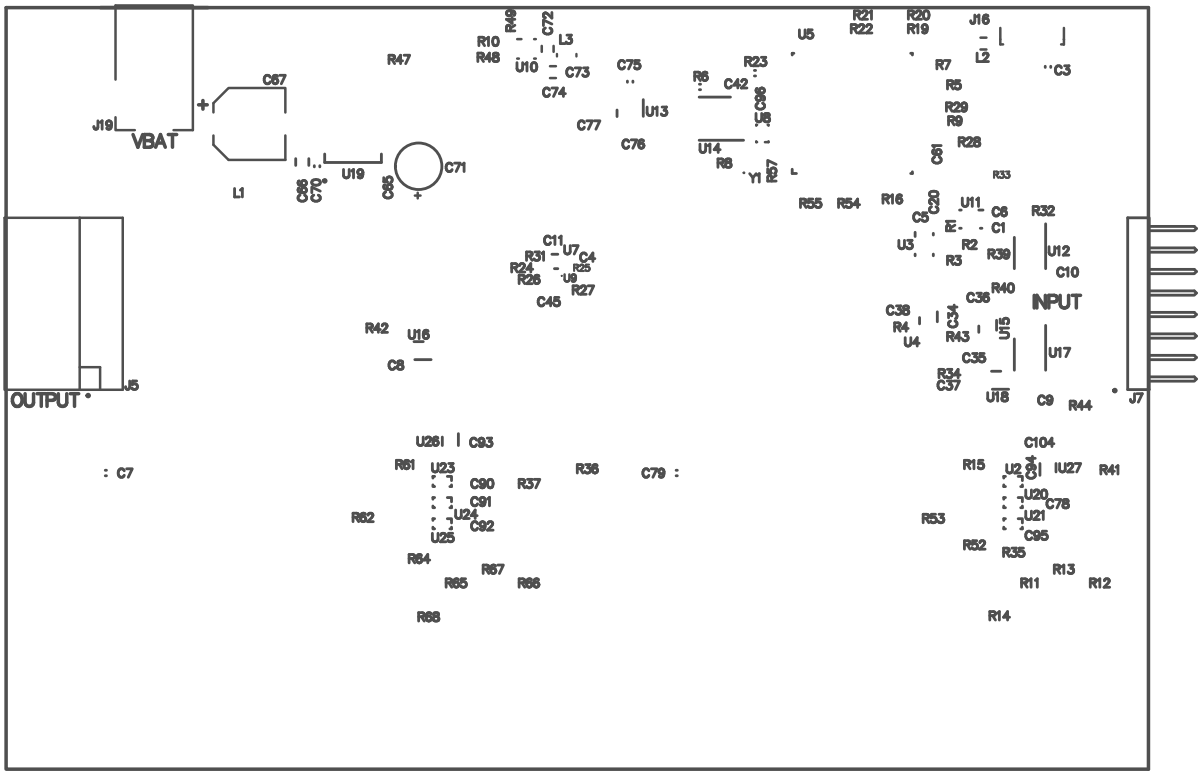

図 23. PCB: Bottom Silk Screen

To download the layer plots, see the design files at TIDA-01572.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01572.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01572.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01572.

5 Software Files

To access to the TAS2770 PPC3 App, please submit a request to MySecureSoftware.

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6 Related Documentation

1. Texas Instruments, *HotRod QFN Package PCB Attachment Application Report*

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