参考資料

TI Designs: TIDA-01634
高速DC/DCコンバータ用のマルチMHzのGaN電力段のリファレンス・デザイン

概要

このリファレンス・デザインは、LMG1210ハーフブリッジGaNドライバとGaNパワーHEMTをベースとする、マルチMHz電力段のデザインを実装します。このデザインは、高効率のスイッチとフレキシブルなデッドタイム調整機能を採用しており、電力密度を大幅に改善するとともに、良好な効率や広い制御帯域幅も実現します。この電力段のデザインは、5Gテレコム電源、サーバー、産業用電源など、スペース制約が厳しく高速な応答が求められる多くのアプリケーションに広く活用できます。

リソース

TIDA-01634	デザイン・フォルダ
LMG1210	プロダクト・フォルダ

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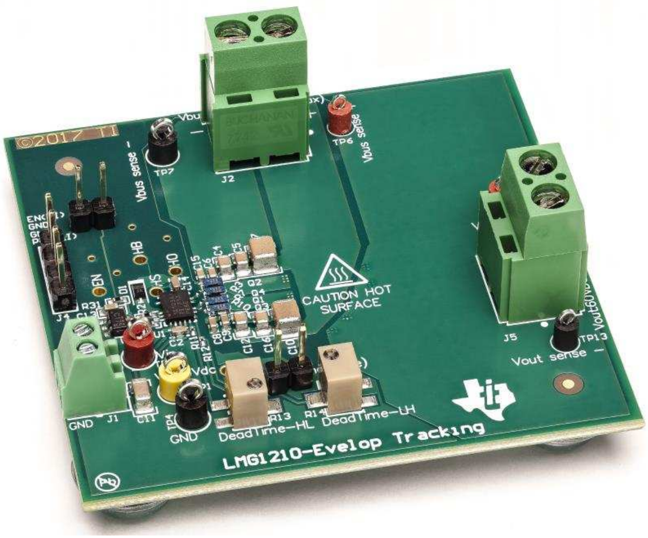
E2E™エキスパートに質問

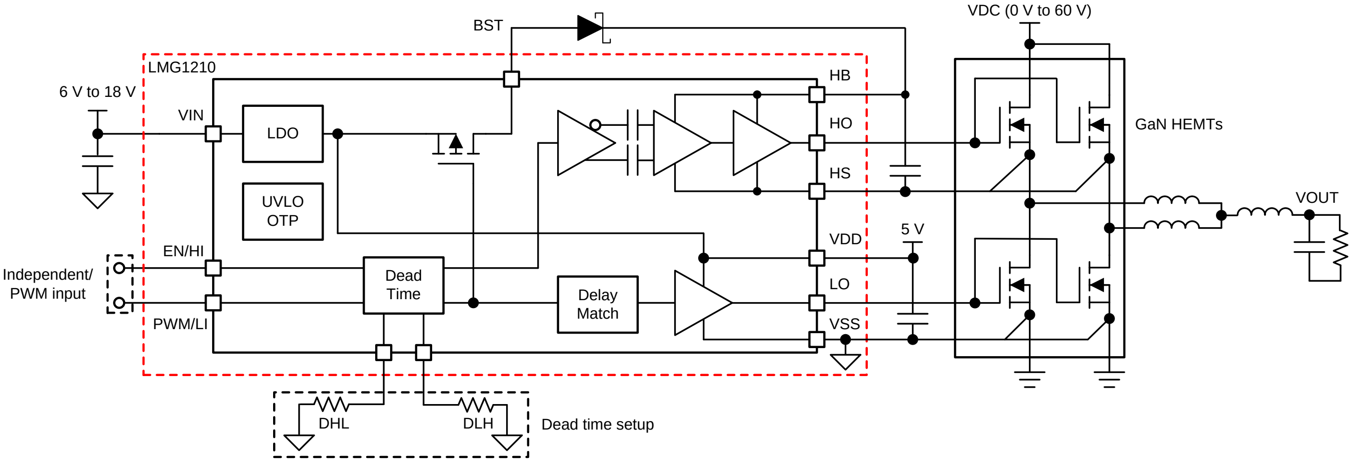
アプリケーション

- 高速な同期整流降圧コンバータ
- エンベロープ追跡
- Class-Dオーディオ・アンプ
- サーバーおよびネットワーク用電源
- 産業用電源

特長

- 小型のGaNベースの電力段デザインで、最高50MHzのスイッチングが可能
- ハイサイドとローサイドに独立のPWM入力、またはデッドタイムを調整可能な単一のPWM入力
- 最小パルス幅: 3ns
- 高いスルー・レート耐性: 300V/ns
- ドライバのUVLOおよび過熱保護





TIDUE47 翻訳版 — 最新の英語版資料 http://www-s.ti.com/sc/techlit/TIDUE47

1 System Description

Switching-mode power supply designers are always pursing higher power density, which requires higher frequency and efficiency. Compared to silicon FETs, gallium nitride (GaN) and high electron mobility transistors (HEMTs) exhibit a lower figure of merit, smaller gate charge, faster switching, and no reverse recovery loss.

This reference design uses GaN power HEMTs and the LMG1210 GaN half-bridge driver to realize a multi-MHz power stage with high efficiency. The half-bridge driver allows a single PWM input with configurable dead time or two independent inputs for high-side and low-side gate drive. Dead-time adjustment can be realized with two resistors for low-to-high and high-to-low transition settings from 0 ns to 20 ns. In addition, the bootstrap switching action also prevents overvoltage of high-side gate due to large third quadrant voltage drop of GaN HEMTs.

This power stage can realize 3 ns of minimum on-time and up to a 50-MHz operation frequency. This design can stand a slew rate of 300 V/ns of common mode transient and provides driver UVLO and overtemperature protection.

This design can be applied to many space-constrained and fast response required applications such as 5G telecom power, 48-to-POL server power, and industrial power supplies.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT AND OUTPUT CHARACTERISTICS					
Input and output voltage		0		60	V
Input and output current		0	4	5	A
Bias voltage		6	7	18	V
Maximum bias current		100			mA
SYSTEM CHARACTERISTICS					
Switching frequency		0.1	1	50	MHz
Slew rate			70		V/ns
Full load efficiency	V_{IN} = 45 V, V_{OUT} = 38 V, I_{OUT} = 4 A, f_{SW} = 10 MHz(1)	96	96.5	97	%

(1) With 200 LFPM of airflow on the board to ensure good thermal stability. No additional heat sink used.

2 System Overview

2.1 Block Diagram

図 1 shows the block diagram of this design. One half-bridge driver LMG1210 with an external boot strap diode drives two paralleled half bridges. Four 65-V rated GaN FETs are used as switching devices.

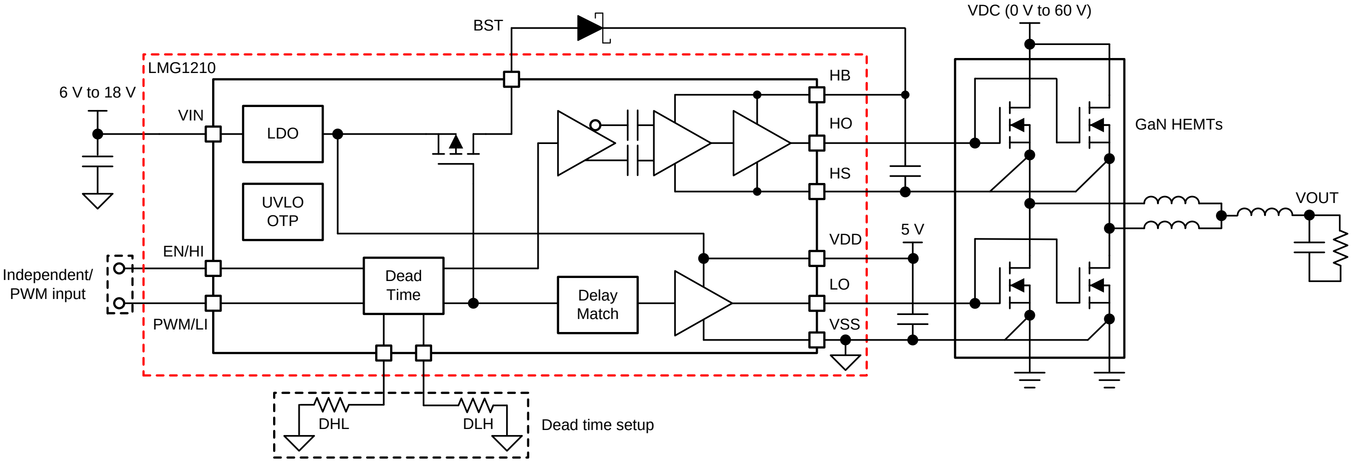


図 1. TIDA-01634 Block Diagram

2.2 Design Considerations

2.2.1 FET Selection

Switching related losses increase linearly with frequency and can become dominate at multi-MHz operation. Based on the targeted switching frequency and power level, switching devices should be carefully selected to realize a balance between $R_{DS(on)}$ and switching related loss.

In this application, GaN HEMT is chosen due to its significant advantages in switching. Typical Si MOSFETs exhibit high switching loss, including I/V overlap, C_{OSS} loss, and reverse recovery loss. With no reverse recovery, small C_{OSS}, and fast switching speed, GaN FETS are ideally suited for high-frequency applications. The switching related characteristics are listed as the table below to compare GaN and Si.

Furthermore, it is critical to choose the appropriate GaN HEMT for the specific switching frequency and load current. With similar figure of merit, smaller C_{OSS} is preferred for high-frequency switching as switching loss can be dominating under multi-MHz switching. For example, in 表 2, the two GaN FETs have a similar figure of merit but one of them (EPC2039) has a larger C_{OSS} loss. In this design, two FETs with small C_{OSS} are paralleled to achieve both small C_{OSS} loss and conduction loss for the targeted load current.

表 2. Key Parameter Comparison of Switching FETs

PARAMETER	EPC8009 (GaN)	EPC2039 (GaN)	BSP320S (Si)
Max V_{DS} (V)	65	80	60
$R_{DS(on)}$ (mΩ)	130	25	120
Q_g (nC)	0.37	1.91	12
Q_{gs} (nC)	0.12	0.76	1
Q_{gd} (nC)	0.055	0.42	4.7
Q_{oss} (nC)	0.94	7.64	2.25

表 2. Key Parameter Comparison of Switching FETs (continued)

PARAMETER	EPC8009 (GaN)	EPC2039 (GaN)	BSP320S (Si)
Q_{rr} (nC)	0	0	80
FOM (Q_g × $R_{DS(on)}$) (nC × mΩ)	48.1	47.75	1440

2.2.2 Capacitor Selection

2.2.2.1 Gate Loop Capacitor

The bypass capacitor for the LMG120 must be located on the top layer with ground return on the layer immediately adjacent with a recommended minimal spacing of 5 mils. Also, the placement must be as close as possible to the IC and connected to both VDD and GND using large power planes. This bypass capacitor has to be at least a 0.1 µF (up to 1 µF) with a temperature coefficient of X7R or better. For this particular application, it is highly recommended to use low-inductance body types such as LICC, IDC, feed-though, and LGA. Add another 1-µF to 10-µF bulk VDD decoupling capacitor as well.

In addition, place the V_{IN} decoupling capacitor as close to the device as possible, but this is a lower priority than the VDD decoupling capacitor.

2.2.2.2 Power Loop Capacitor

The selection of the high-frequency capacitors for the power loop is critical to help minimize the loop stray inductance. The capacitors have to be selected to allow for the maximum bus voltage and to provide both enough charge to sustain the current and to provide a minimal inductive path. X7R or better material is needed to provide stability and low ESR. A mix of 0603 and 0805 is used, where the 0603 capacitors are in the closest proximity to the power loop and the 0805 capacitors are adjacent to those first capacitors. Low-inductance, wide-body packages are preferred.

The layout of this section is critical and will be discussed later in this document.

2.2.3 FETs Paralleling

When FETs with smaller C_{OSS} and switching loss are selected, switching related loss can be minimized to allow a high operation frequency of the DC/DC converter. At the same time, conduction loss also needs to be considered with respect to load condition. When load current is high, two half-bridges can be paralleled together to increase the current capability of the power stage.

Due to the fast switching of GaN FETs, small parasitic inductance needs to be achieved even when paralleling the FETs. In this case, a "pseudo-parallel" structure is preferred, which means two half-bridges are designed with shared gate drive with minimal parasitics. A small inductor is recommended between the two switching nodes. If no inductor is between the two nodes, small part-to-part variations in the threshold voltage of the GaN can cause one FET to turn on earlier and absorb a disproportionate share of the switching losses, thus causing a thermal imbalance.

In addition, it is critical to keep identical layout loops between the two legs to achieve similar delay and gate voltage profile in the switching transient.

2.2.4 Layout Considerations

The layout of the GaN-based power stage requires specific attention to the loop inductance for both the power loop and gate drive loop. If two half-bridges are paralleled, it is also highly suggested to make the layout symmetric to achieve a similar performance and parasitics for the two loops.

図 2 shows a general view of the layout.

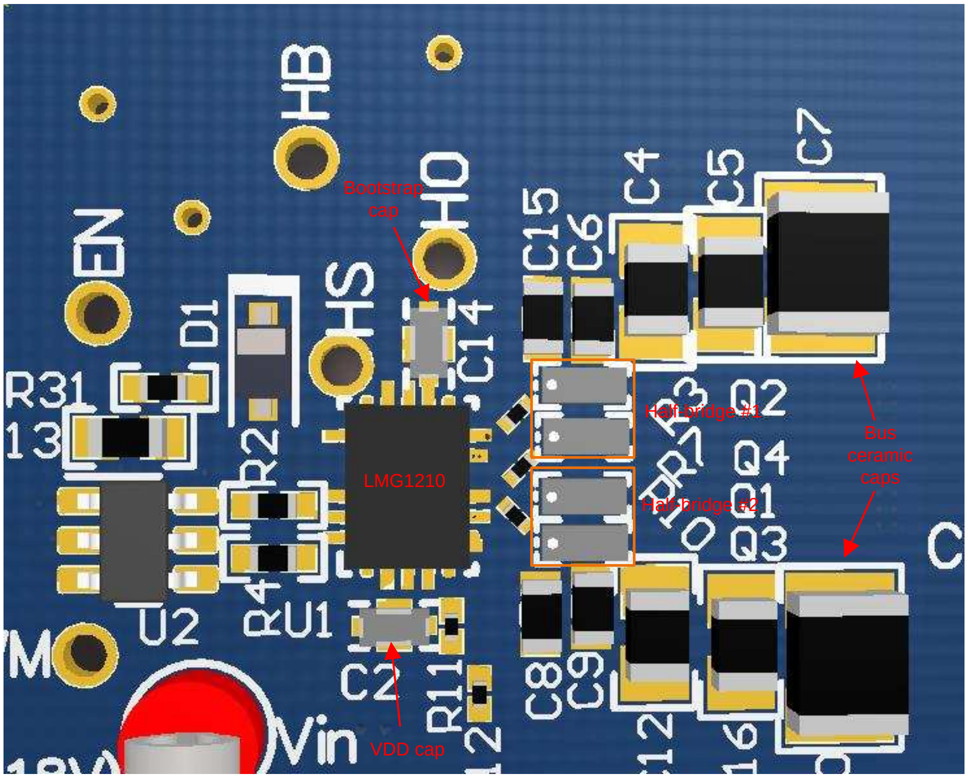


図 2. Layout General View

2.2.4.1 Gate Drive Loop Layout

The following figures show the layout of the gate loop of the upper and lower FETs. To achieve the minimum loop inductance, the layout of gate loop must follow these rules:

- Have the VDD capacitor or bootstrap capacitor as close as possible to the gate driver because these traces will be part of the gate loop.
- Use a dedicated Kelvin source or minimum sharing of source trace between the gate loop and main power loop to achieve the minimum common source inductance. The high di/dt on the main loop can be easily be coupled to the gate loop to cause decreased switching speed and other negative effects.
- To minimize the gate loop inductance, the ground return path has to be on the adjacent layer with minimum inter-layer dielectric thickness, and have as much overlap as possible to the driver output. In this case, the current flow on the input of FET gate is the opposite of the ground current return, which offsets the magnetic field and reduces PCB stray inductance.
- To keep the return loops as short as possible, micro-vias in pads are used extensively in this design to further reduce the parasitic inductances and improve the vertical current extraction from components.

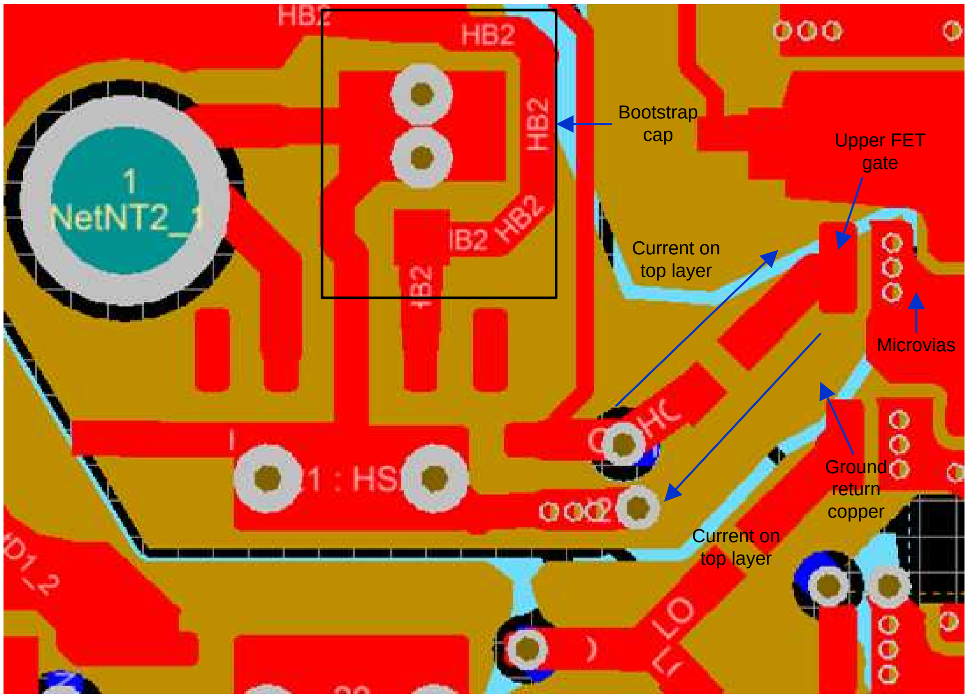


図 3. Gate Drive Loop Layout for High-Side FET

In certain circumstances that require paralleled FETs, the following rules help achieve better symmetry and at the same time minimize the gate loop inductance.

- Place the paralleled FETs with similar distance to the output of the driver. Have the FET gate loop traces laid out on different layers to keep the traces with identical length to the FETs.
- Keep the identical return paths on different layers, and make sure that for each FET, the return ground layer is on the adjacent layer of its dedicated gate path to minimize the stray inductance.

図 4 and 図 5 show the gate loop layout of this reference design with two FETs paralleling.

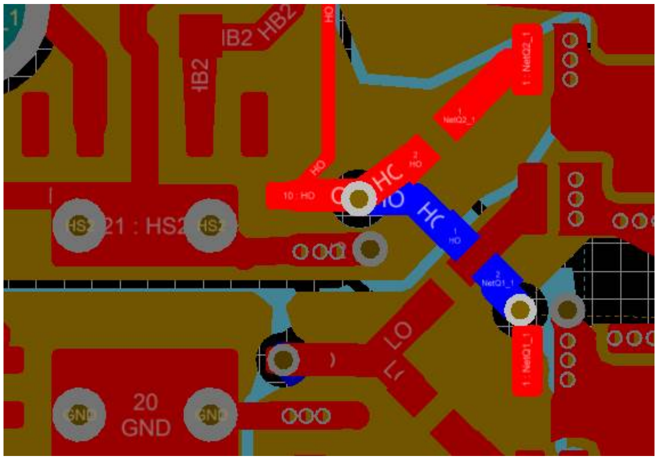


図 4. Gate Drive Path for Paralleled FETs

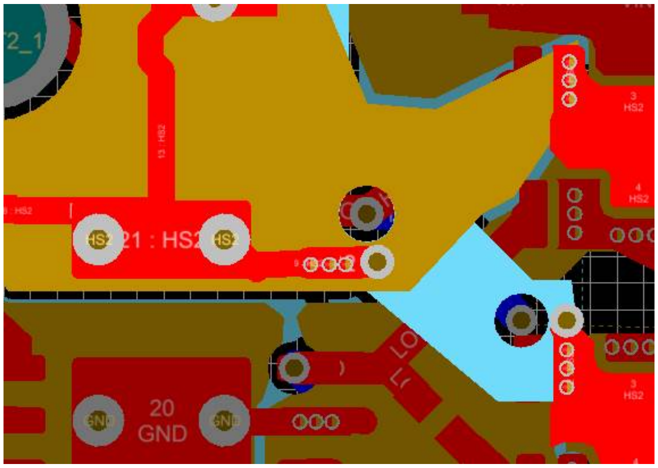


図 5. Return Path of Paralleled FETs Gate Drive

2.2.4.2 Power Loop Layout

The layout of power loop is also aimed at minimizing stray inductance. To realize a small power loop:

- Place ceramic capacitors with a small package as close to the devices as possible. These capacitors are usually better in frequency response and have a high bandwidth to absorb high-frequency noise generated during switching.
- A very compact component placement is needed. Place the upper and lower FETs side by side, and use the layer immediately beneath for the return path. Use micro-vias (filled) in the pads to help keep the loop short.
- Have the return pass overlapped with the topside current path to create an opposite magnetic field. This field helps cancel the magnetic field in the loop and reduce the inductance.
- Minimize the overlap between switching node and ground/Vin copper. This overlap avoids the extra parasitic capacitance, which adds to C_{OSS} of FETs. If not designed well, the parasitic capacitors can generate significant loss at high switching frequency.

図 6 shows the size of the power loop is 2.5 mm × 4.3 mm. The 6800-pF capacitors are placed closest to the FETs, while other larger capacitors are placed further in a line. The return path is placed right underneath the top layer trace through micro-vias, spaced by the inter-layer dielectric thickness.

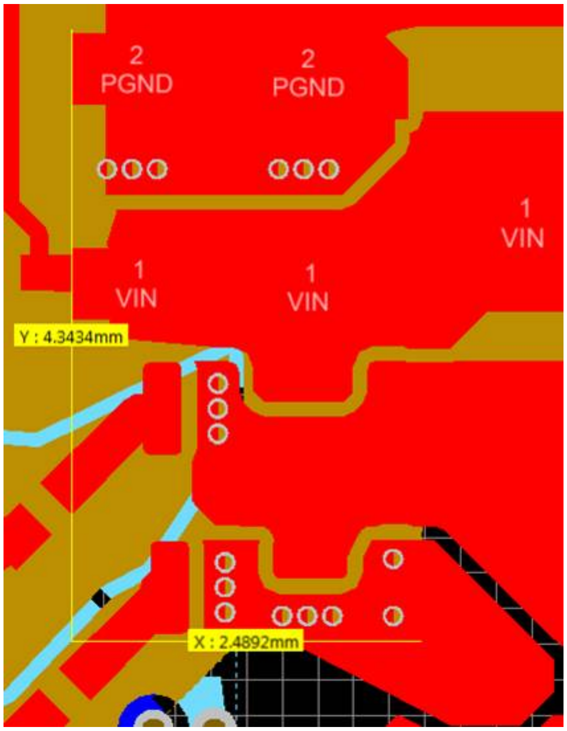


図 6. Power Loop Layout For a Half-Bridge

When paralleled FETs are used, they are laid out in a "pseudo-parallel" structure to have a minimized loop. This structure means two legs are laid out separately but share the same gate driver. The power loops of both half-bridges are laid out in a very symmetric pattern. The component placement and copper shapes are all symmetric. This structure helps achieve very similar loop characteristics in switching and conduction.

The switching nodes are connected with some PCB trace as small inductors in between (for more information, see 2.2.4.1). Depending on the selected FETs and operation voltage, the needed inductance between the two nodes can be varied. In this case, PCB trace inductors are used. In a practical design, these inductors can be replaced by external wires to obtain more flexibility on inductance values.

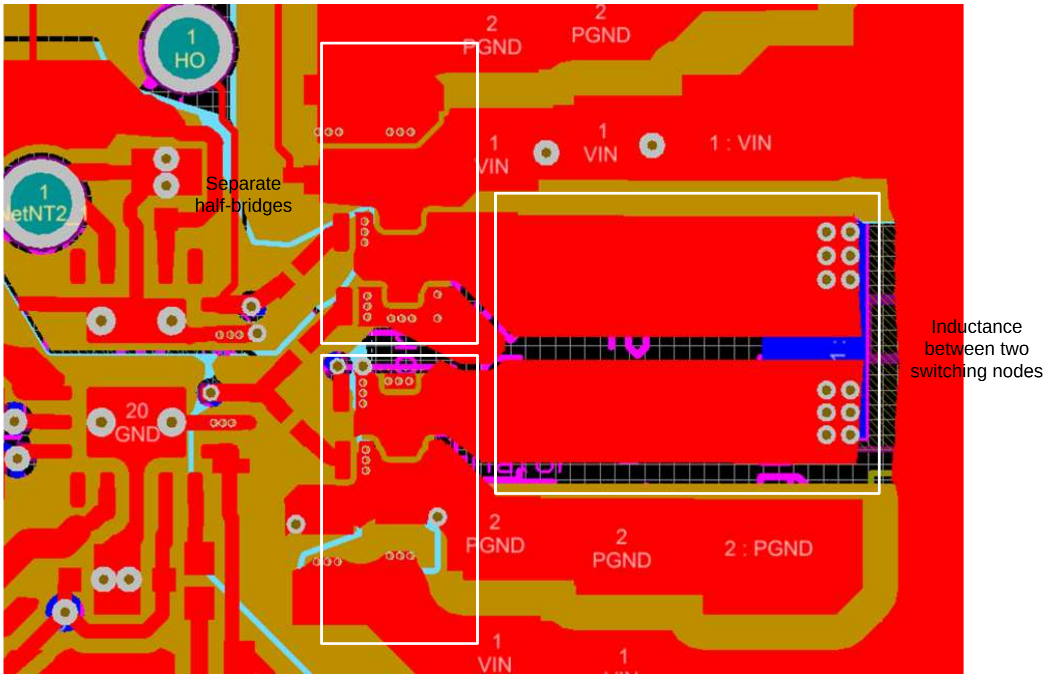


図 7. Symmetric Power Loop Layout for Paralleled Half-Bridges

2.2.5 Dead Time Optimization

There are two modes of inputs to enable the HS and LS outputs of the driver LMG1210: PWM mode and independent mode.

For PWM mode, two separate resistors set up the high-to-low and low-to-high transition dead times from 0 ns to 20 ns. With one input, two output signals can be generated. For independent mode, two independent signals are used to control the HS and LS switches.

An appropriate dead time is critical in a multi-MHz power stage design. GaN HEMTs are majority carrier devices, which lack the typical body diode present in MOSFETs. The conduction in the third quadrant is still possible through internal gate biasing, which causes a higher voltage drop in the channel due to the activation voltage and the channel resistance (while in linear mode). This drop is what is experienced during dead time. The voltage drop produces a loss, which is directly proportional to frequency, current, and time spent in the dead time. This loss can significantly degrade efficiency, especially in converters operating at high frequency and low input or output voltages. For example, in a 12-V to 1.8-V buck converter operating at 5 MHz and 10-A output, going from a dead time of 1 ns to 10 ns can degrade efficiency by 8.5%.

To minimize the dead time and its associated loss, the low-side and high-side propagation delay mismatch of the driver must be predictable and unaffected by part-to-part variation, temperature, bootstrap voltage, HS pin voltage, or HS slew rate. 表 3 summarizes the mismatch variations of the LMG1210 for these parameters. With the minimum variation of delay time in different effects with the LMG1210, the smallest dead time can be achieved, which results in much improved efficiency in the multi-MHz power stage.

In most converters, one edge is soft-switched. To avoid hard switching and maintain a small effective dead time on this soft-switched edge, the dead time must be varied depending on load current. For the other hard-switched edge, it is optimal to pursue the fixed minimum dead time when considering these variations.

表 3. Variation of Dead Time by Different Factors for LMG1210

EFFECT	EDGE			
	HIGH-OFF TO LOW-ON (HARD-SWITCHING EDGE)		LOW-OFF TO HIGH-ON (SOFT-SWITCHING EDGE)	
	PARAMETER VARIATION	LMG1210 VARIATION (ns)	PARAMETER VARIATION	LMG1210 VARIATION (ns)
Variation of HS	None (V_{IN})	0	Minimal	0
Variation of Vbst	4 V to 4.5 V	0.3	4 V to 4.5 V	0.3
Variation of CMTI	None	0	10 V/ns to 100 V/ns	0.2
Intrinsic driver variation		0.7		0.7
Total variation in dead time		1		1.2

2.2.6 Inductor Selection

The EVM comes equipped with a 1-µH, 9-A inductor. If a different operating point in frequency, voltage, or current ripple is desired, it is likely that a new value of inductor will be more suited.

When selecting the new inductor, the value of the inductor must respect the value found from 式 1:

$$Iind \geq VBUSmin\ (IL\_sat,\ IFET\_DCmax) \cdot ton \tag{1}$$

where:

- V_{BUS} is the bus voltage across the power stage
- t_{on} is the on-time of the upper FET (active FET)
- I_{L_sat} is the inductor saturation current
- I_{FET_DCmax} is the allowed maximum DC current of switching FETs

2.3 Highlighted Products

2.3.1 LMG1210

The LMG1210 is a 200-V, half-bridge, high-performance GaN FET driver designed for applications that require high switching speed, low dead time, and high efficiency. The drive voltage is precisely controlled by an internal linear regulator to 5 V when higher auxiliary voltages are used.

The LMG1210 is optimized to operate at very high frequencies. The extremely small mismatch and propagation delay of this device allows reduced dead time requirements. Additional parasitic capacitance across the GaN FET is minimized to less than 1 pF to reduce additional switching losses. An external bootstrap diode is used to charge the high-side driver to allow optimal selection for the circuit operating conditions. An internal switch turns off the bootstrap diode when the low side is not on, effectively preventing the high-side bootstrap from overcharging and minimizing the reverse recovery charge when a silicon diode is used as the bootstrap diode.

The driver can operate either with dual inputs with independent control of each driver or can be operated with a single PWM input with an independently adjustable dead time from 0 ns to 20 ns for each edge. The LMG1210 operates over a wide temperature range from –40°C to +125°C and is offered in a low-inductance QFN package.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware

- DC voltage source: Capable of supplying the input of the board up to 60 V as desired; capable of supplying 10 A and supports current limiting
- DC bias source: Capable of 6-V to 18-V output at up to 0.3 A
- Oscilloscope: Capable of at least a 200-MHz operation, using oscilloscope probes with a "pigtail" spring ground clip instead of the standard alligator clip
- DC multimeters: Capable of 100-V measurement, suitable for determining operation and efficiency (if desired)
- DC load: Capable of 100-V operation at up to 10 A in constant current-mode operation
- Function generator: Single output for PWM mode, dual synchronous output for independent mode; capable of at least 0-V to 3-V signal (operating maximum digital input is 5 V)
- Fan: 200LFM minimum airflow is recommended to cool the PCB when operating above a 10-A output current
- (Optional) Power meter: Capable of 100-V operation at up to 10 A

3.2 Testing and Results

3.2.1 Test Setup

Connect the input and bias supplies and DC electronic load as shown in 図 8.

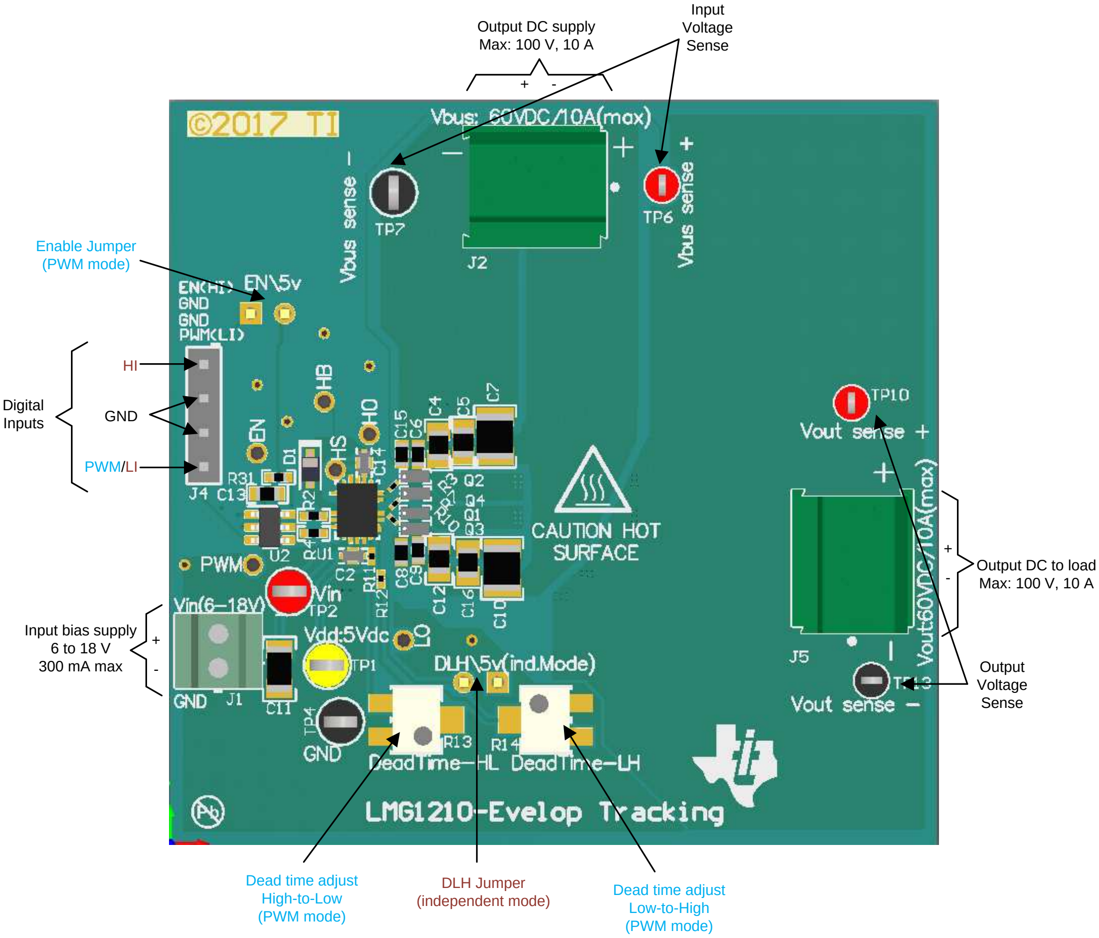


図 8. Top View of TIDA-01634 Hardware

To get rid of the high-frequency noise induced by the probe parasitics, use the small pigtails without the probe clips. This minimizes measurement error and produces a cleaner signal with the fast switching GaN devices used on this reference design. The data shown in this design guide is obtained using this method.

図 9. Low Parasitic Measurement Setup

To obtain the best performance of this board:

- Thermal: The parts used on this board are extremely small. If the dissipation exceeds 2 W, actively cool the board (as it has no heat-sink) using a fan or a similar device.
- Voltage spikes: As the test is running, whenever increasing the voltage and the current, it is important to monitor the voltage on the switched node to ensure the peak voltage does not exceed the 65-V rating of the EPC8009 FETs as those could damage the components.
- Additional capacitance on switched nodes: Typically, the method to observe the voltage at the high-side gate and the switched node is using a voltage probe. These probes come with several tens of pF of capacitance, which given the frequency can negatively impact efficiency. For precise efficiency measurements, remove all probes connected to switching nodes.

3.2.2 Test Results

3.2.2.1 *Efficiency*

図 10 shows the efficiency results in this section, which exclude driver losses. The power stage is running at 10 MHz with a 85% duty cycle with respect to different output current.

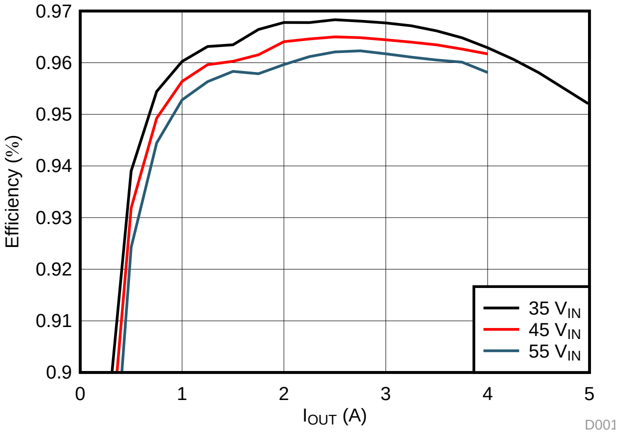


図 10. Power Stage Efficiency With EPC8009 1-µH Inductor, Running at 10 MHz 85% Duty Cycle vs Output Current

3.2.2.2 *Dead-Time Tuning*

Tuning the dead time correctly for high-speed application can greatly improve performance. Pay attention when tuning the dead time of the two FETs before applying the input voltage.

図 11 shows the effect of changing the dead time on a sub-optimal design. The values refer to the transitions high-to-low first (first number) and low-to-high (second number).

It is possible to see a direct impact of any dead time on the low side turning on (as this contributes to third-quadrant conduction losses). For the high-side turnon dead time, there is an optimal value (that is dependent on components variation across boards), which is typically between 0 ns and 2 ns.

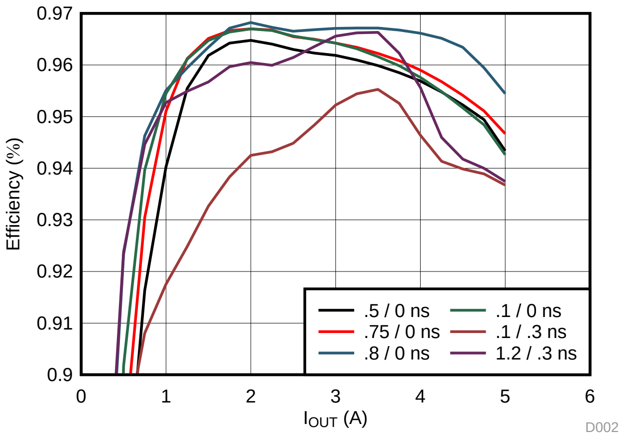


図 11. Effect of Dead-Time Tuning on Efficiency

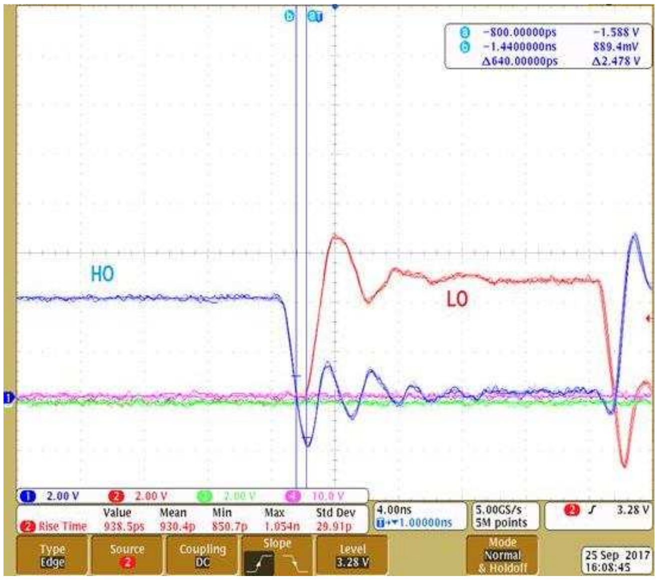


図 12. Dead Time Measurement Done at V_{IN} = 0 Showing High-to-Low Transition Dead Time of 640 ps

3.2.2.3 Switching Waveforms

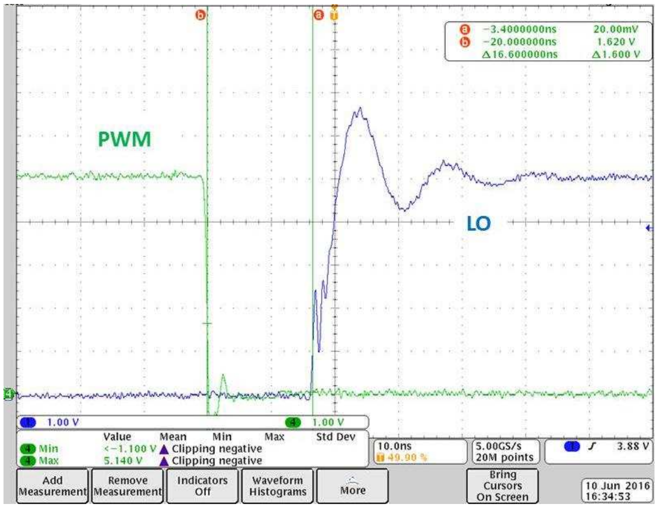


図 13. PWM High-to-Low Delay Time

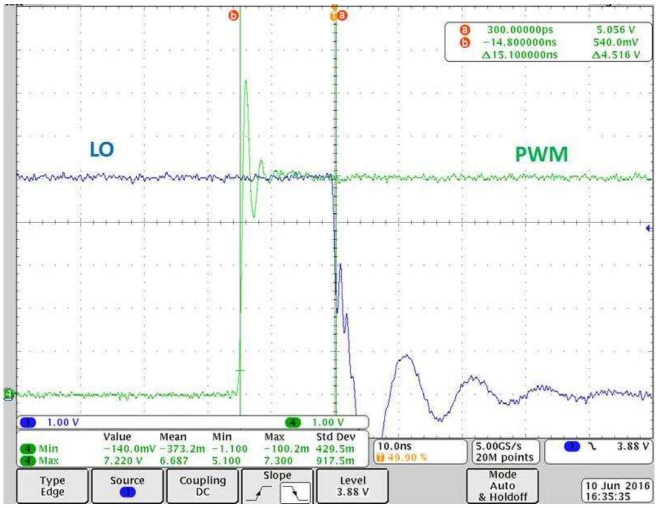


図 14. PWM Low-to-High Delay Time

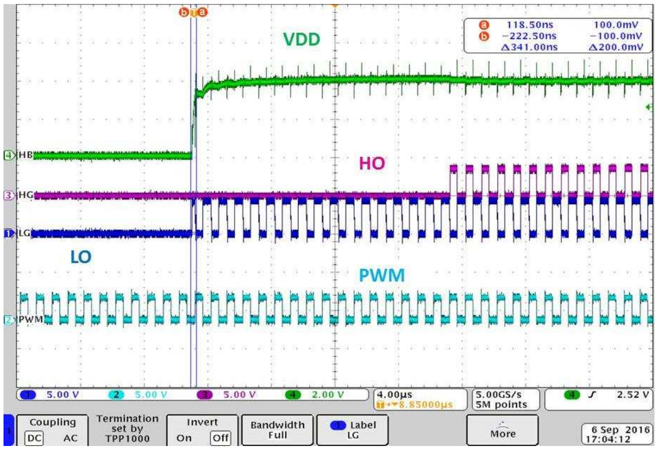


図 15. HO and LO Outputs of LMG1210 During Startup

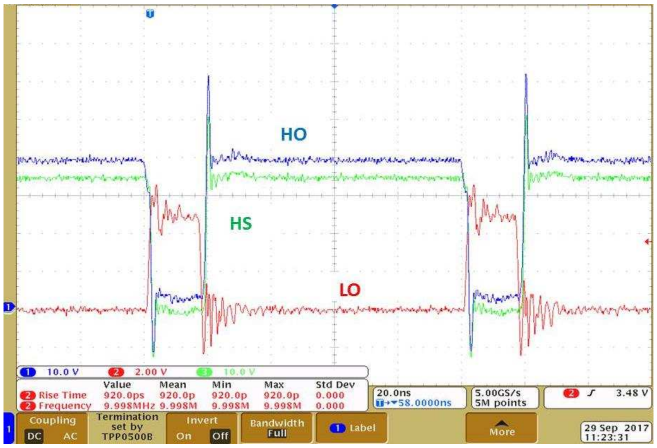


図 16. Power Stage Switching at 10 MHz, 35 V

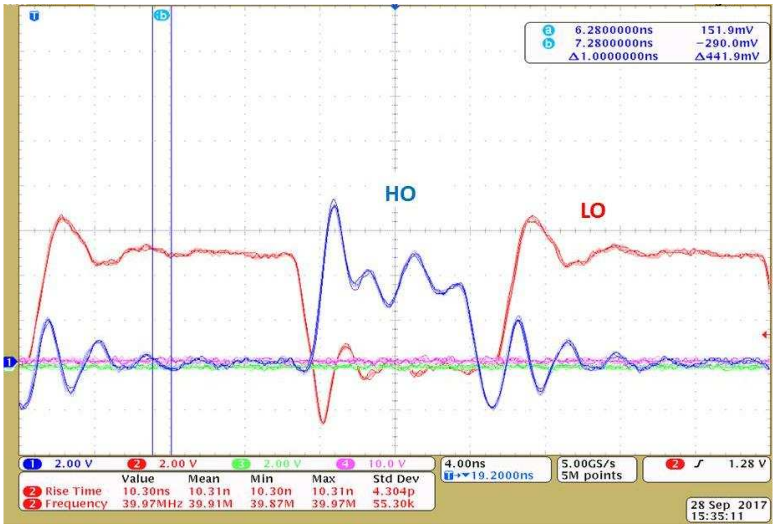


図 17. HO and LO Signals When Switching at 40 MHz With No DC Bus Voltage

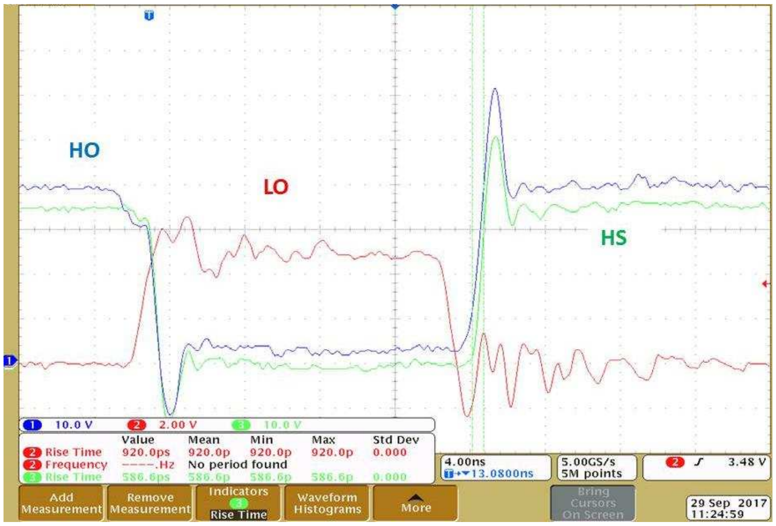


図 18. Switching Transient With 70 V/ns on Switching Node

4 Design Files

4.1 *Schematics*

To download the schematics, see the design files at TIDA-01634.

4.2 *Bill of Materials*

To download the bill of materials (BOM), see the design files at TIDA-01634.

4.3 *PCB Layout Recommendations*

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01634.

4.4 *Altium Project*

To download the Altium project files, see the design files at TIDA-01634.

4.5 *Gerber Files*

To download the Gerber files, see the design files at TIDA-01634.

4.6 *Assembly Drawings*

To download the assembly drawings, see the design files at TIDA-01634.

5 Related Documentation

1. Texas Instruments, *Using the LMG1210EVM-012 300 V Half-Bridge Driver for GaN User's Guide*
2. Texas Instruments, *LMG1210 200-V, 1.5-A, 3-A Half-Bridge GaN Driver With Adjustable Dead Time Data Sheet*
3. Texas Instruments, *Optimizing Efficiency Through Dead Time Control With the LMG1210 GaN Driver Application Report*

5.1 *商標*

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すべての商標および登録商標はそれぞれの所有者に帰属します。

TIの設計情報およびリソースに関する重要な注意事項

Texas Instruments Incorporated ("TI")の技術、アプリケーションその他設計に関する助言、サービスまたは情報は、TI製品を組み込んだアプリケーションを開発する設計者に役立つことを目的として提供するものです。これにはリファレンス設計や、評価モジュールに関係する資料が含まれますが、これらに限られません。以下、これらを総称して「TIリソース」と呼びます。いかなる方法であっても、TIリソースのいずれかをダウンロード、アクセス、または使用した場合、お客様(個人、または会社を代表している場合にはお客様の会社)は、これらのリソースをここに記載された目的にのみ使用し、この注意事項の条項に従うことに合意したものとします。

TIによるTIリソースの提供は、TI製品に対する該当の発行済み保証事項または免責事項を拡張またはいかなる形でも変更するものではなく、これらのTIリソースを提供することによって、TIにはいかなる追加義務も責任も発生しないものとします。TIは、自社のTIリソースに訂正、拡張、改良、およびその他の変更を加える権利を留保します。

お客様は、自らのアプリケーションの設計において、ご自身が独自に分析、評価、判断を行う責任がお客様にあり、お客様のアプリケーション(および、お客様のアプリケーションに使用されるすべてのTI製品)の安全性、および該当するすべての規制、法、その他適用される要件への遵守を保証するすべての責任をお客様のみが負うことを理解し、合意するものとします。お客様は、自身のアプリケーションに関して、(1) 故障による危険な結果を予測し、(2) 障害とその結果を監視し、および、(3) 損害を引き起こす障害の可能性を減らし、適切な対策を行う目的での、安全策を開発し実装するために必要な、すべての技術を保持していることを表明するものとします。お客様は、TI製品を含むアプリケーションを使用または配布する前に、それらのアプリケーション、およびアプリケーションに使用されているTI製品の機能性を完全にテストすることに合意するものとします。TIは、特定のTIリソース用に発行されたドキュメントで明示的に記載されているもの以外のテストを実行していません。

お客様は、個別のTIリソースにつき、当該TIリソースに記載されているTI製品を含むアプリケーションの開発に関連する目的でのみ、使用、コピー、変更することが許可されています。明示的または黙示的を問わず、禁反言の法理その他どのような理由でも、他のTIの知的所有権に対するその他のライセンスは付与されません。また、TIまたは他のいかなる第三者のテクノロジまたは知的所有権についても、いかなるライセンスも付与されるものではありません。付与されないものには、TI製品またはサービスが使用される組み合わせ、機械、プロセスに関連する特許権、著作権、回路配置利用権、その他の知的所有権が含まれますが、これらに限られません。第三者の製品やサービスに関する、またはそれらを参照する情報は、そのような製品またはサービスを利用するライセンスを構成するものではなく、それらに対する保証または推奨を意味するものでもありません。TIリソースを使用するため、第三者の特許または他の知的所有権に基づく第三者からのライセンス、もしくは、TIの特許または他の知的所有権に基づくTIからのライセンスが必要な場合があります。

TIのリソースは、それに含まれるあらゆる欠陥も含めて、「現状のまま」提供されます。TIは、TIリソースまたはその仕様に関して、明示的か暗黙的かにかかわらず、他のいかなる保証または表明も行いません。これには、正確性または完全性、権原、続発性の障害に関する保証、および商品性、特定目的への適合性、第三者の知的所有権の非侵害に対する黙示の保証が含まれますが、これらに限られません。

TIは、いかなる苦情に対しても、お客様への弁護または補償を行う義務はなく、行わないものとします。これには、任意の製品の組み合わせに関連する、またはそれらに基づく侵害の請求も含まれますが、これらに限られず、またその事実についてTIリソースまたは他の場所に記載されているか否かを問わないものとします。いかなる場合も、TIリソースまたはその使用に関連して、またはそれらにより発生した、実際的、直接的、特別、付随的、間接的、懲罰的、偶発的、または、結果的な損害について、そのような損害の可能性についてTIが知らされていたかどうかにかかわらず、TIは責任を負わないものとします。

お客様は、この注意事項の条件および条項に従わなかったために発生した、いかなる損害、コスト、損失、責任からも、TIおよびその代表者を完全に免責するものとします。

この注意事項はTIリソースに適用されます。特定の種類の資料、TI製品、およびサービスの使用および購入については、追加条項が適用されます。これには、半導体製品(http://www.ti.com/sc/docs/stdterms.htm)、評価モジュール、およびサンプル(http://www.ti.com/sc/docs/sampterms.htm)についてのTIの標準条項が含まれますが、これらに限られません。