参考資料

TI Designs: TIDA-01592
超音波送信用の25W、高電圧、プログラム可能電源のリファレンス・デザイン

概要

このリファレンス・デザインは、超音波送信回路に電力を供給する、デジタル・プログラム可能な非絶縁電源のソリューションです。フライバック電源トポロジと単一の変圧器を使用して、絶対値で100Vまでのプログラム可能な2つの高電圧を生成します。このデザインは、低消費電力の携帯用超音波スキャナを対象としています。このデザインは、各レールで12.5W、最大で25Wの電力を連続的に供給できます。高電圧(HV)レールは、設定dc電圧により、0V～±100Vにプログラム可能です。12ビットのDACを使用して、DACによるプログラム機能を実装できます。すべての電源レールは、マスタ・クロックと同期可能です。このデザインはスケーラブルでモジュール化されているため、チャネルの数やパルサーのレベル数に応じて、同じ電源を追加または除去できます。

リソース

TIDA-01592	デザイン・フォルダ
TIDA-01352	デザイン・フォルダ
LM3481	プロダクト・フォルダ
CSD19532Q5B	プロダクト・フォルダ
TLVx171	プロダクト・フォルダ

TI E2E™ Community

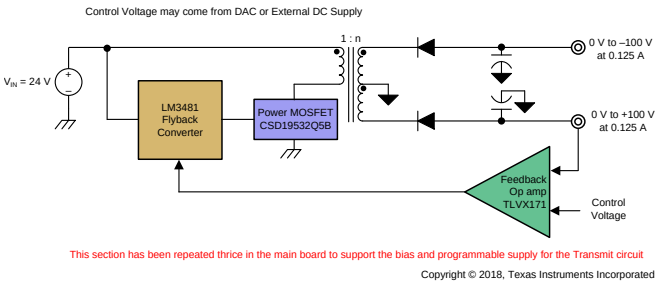
E2E™エキスパートに質問

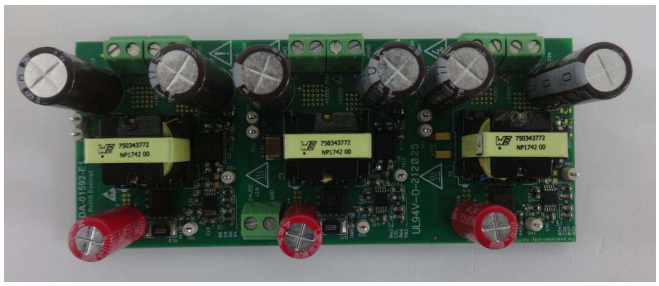
特長

- 24V電源で動作し、100kHz～500kHzの広い動作周波数範囲、0V～±100Vの範囲でデジタルにプログラム可能なデュアル出力、100V全負荷で87%のピーク効率
- バイアスおよびパルサー・ドライバ用の、非絶縁の共通電源(B-Mode、CW-Mode、エラストグラフィー・モードのサポート用)
- 最大192のデジタル・パルサー・チャネルに電力を供給可能 - フライバック・トポロジによりチャネル数の増減に応じてスケーリング可能
- 超音波マスタまたはシステム・クロック周波数との周波数同期 - より優れた高調波除去が可能
- モジュール化設計により、パルサーのレベル数に応じて同じ電源を追加または除去可能
- 電流モード制御により、優れた帯域幅と過渡応答を持ち、サイクル単位の電流制限が可能

アプリケーション

- 医療用超音波スキャナ
- ソナー・イメージング機器
- 非破壊検査機器





1 System Description

This reference design enables modular and efficient power scaling capabilities by providing a solution for digitally programmable non-isolated power supplies for ultrasound transmit circuits. Medical ultrasound imaging is a widely used diagnostic technique that enables visualization of internal organs, their size, structure, and estimation of blood flow. Ultrasound imaging uses high-voltage ultrasound signals to actuate the sensor, transmits those signals inside human body, and receives the echo on the same line. This process requires a high-voltage, dual power supply that is programmable, scalable, and able to drive more channels to output a better quality image.

In typical sonar imaging applications, the image of an object is digitally constructed from the information received from the reflected waves after they hit the target. This image can provide information regarding the location, shape, and other properties of the object even in low visibility conditions. Because the principle of operation is the same as ultrasound scanners, the power supply requirements are also similar.

Nondestructive evaluation is a contactless analysis technique used to study the properties of a material, its composition, and so on without damaging it. In this technique, ultrasonic waves pass through the object and the results provide information about the object like internal flaws or characteristics. Typically, the range of frequencies in evaluations is 0.1 MHz to 15 MHz. An example of ultrasonic testing is measuring the thickness of pipelines to monitor corrosion.

This reference design is intended for low-power ultrasonic applications and is designed for portable ultrasound machines where the power requirements are typically 5 W to 10 W on each high-voltage line. The system can deliver a regulated variable output from 0 V to ±100 V, which can be set by an external DC source. Typically, DAC is implemented to program the output voltage. The design uses one transformer to provide symmetrical outputs that reduces the form factor of the solution. Hence, symmetrical load must be put at the output. The design has a non-isolated output feedback with an externally programmable control voltage pin to set the output voltage to the desired value. Thus, the design caters to a variety of applications to deliver power in a controlled way.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input voltage (V_{IN})	24 V ± 15%
Output voltage (V_{OUT})	0 V to ±100 V (programmable)
Output power (P_{OUT})	12.5-W maximum per rail
Peak efficiency (η)	87% (100-V full load)
Output voltage regulation	±5 %
Switching frequency (f_{SW})	100 kHz to 500 kHz
External frequency synchronization	Yes

2 System Overview

In an ultrasound system, the transmitter must generate HV signals for the transducer to work effectively. There are semiconductor devices available that can generate HV signals to ensure the penetration depth of ultrasonic signals. 表 2 lists the different configurations for the ultrasound high-voltage transmit systems, which include cart-based, smart probe, and portable ultrasound scanners. Ultrasound systems require a bias supply or high-voltage multiplexer supply. The reference design caters to the requirements of portable scanners and the bias supply, as listed in 表 2. The reference design gives modularity in the system because the same circuitry can be used to generate the fixed supply, the biased supply, or the programmable supply.

表 2. Ultrasound High-Voltage Power-Supply Configurations

S/N	APPLICATION	INPUT VOLTAGE	OUTPUT VOLTAGE	POWER PER RAIL	CONSTRAINTS
1	Smart probe	+12 V (after boost). Typical input is battery or USB type C	DAC-controlled variable ±2.5 V to ±75 V	Maximum of 2 W	• Very small size (area and height) • Ultra-high efficiency; light load efficient • Frequency sync (100 kHz to 500 kHz) • Low noise • Constant power mode (should not shut down if overloaded)
2	Portable system	+12 V or 24 V	DAC-controlled variable ±2.5 V to ±85 V	Maximum of 5 W to 10 W	• Very small size (area and height) • High efficiency; light load efficient • Frequency sync (100 kHz to 500 kHz) • Low noise • Constant power mode (should not shut down if overloaded)
3	Cart system	+12 V	DAC-controlled variable ±2.5 V to ±100 V	Maximum of 15 W to 30 W	• High efficiency; light load efficient • Frequency sync (100 kHz to 500 kHz) • Low noise • Constant power mode (should not shut down if overloaded)
4	Cart system	+24 V	DAC-controlled variable ±2.5 V to ±100 V	Maximum of 15 W to 30 W	• High efficiency; light load efficient • Frequency sync (100 kHz to 500 kHz) • Low noise • Constant power mode (should not shut down if overloaded)
5	Bias or HV mux supply	+12 V	Fixed voltage ±80 V to ±120 V	2 W	• Frequency sync (100 kHz to 500 kHz) • Low noise • High efficiency; light load efficient • Constant power mode (should not shut down if overloaded)
6	Bias or HV mux supply	+24 V	Fixed voltage ±80 V to ±105 V	5 W	• Frequency sync (100 kHz to 500 kHz) • Low noise • High efficiency; light load efficient • Constant power mode (should not shut down if overloaded)

図 1 shows a generic system level block diagram of the portable ultrasound scanner. The beamformer circuitry that is employed in typical ultrasound systems consists of the following:

- HV power supply section to generate power to the other blocks
- TX/RX circuit to transmit and receive the ultrasound waves
- Beamformer circuit

図 1 shows only the transmit section of the block diagram.

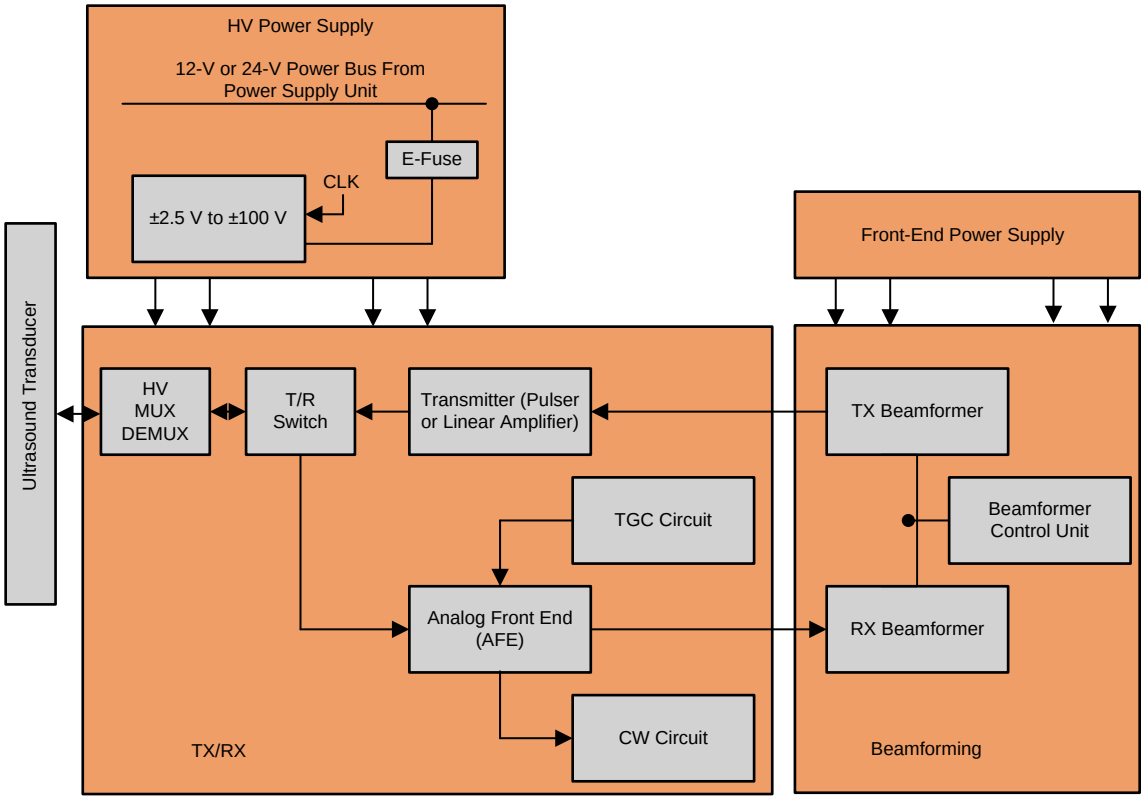


図 1. System-Level Block Diagram for Portable Ultrasound Scanners (Full Block Diagram is Not Shown)

The high-voltage pulses are applied to the piezoelectric crystals in the transducer, which generate ultrasound waves that traverse through the body. The reflected echo consists of information, such as blood flow, organs, tissues, and so on. These applied pulses are generated by transmit devices and are usually bipolar in nature.

There are two modes of operation:

- Pulse mode (also known as B- or M-mode) where high-voltage pulses (typically up to ±100 V) are transmitted for only a short time
- Continuous (CW) mode where low-voltage pulses (typically ±2.5 V to ±10 V) are continuously transmitted by half the piezoelectric elements in the transducer while the other half act as receiver

Note that the same power supply is used for both the modes, which means that the output of power supply ranges from ±2.5 V to ±100 V. Such a powering scheme is typically implemented using a switched mode power supply (SMPS) followed by regulators, as shown in 図 2. The voltage noise on the output signal is very important when CW mode is used because the signal amplitudes are low. Within Pulse mode, there is a special mode called Elastography (or Shear Wave) mode. The current requirements are huge for a short period of time (can be tens of microseconds). It is challenging to deliver such a high current at high voltages without dropping the output voltage. To compensate for the drop in output voltage, high-value capacitors are also used at the output of the SMPS.

注: The focus of this document is the SMPS only.

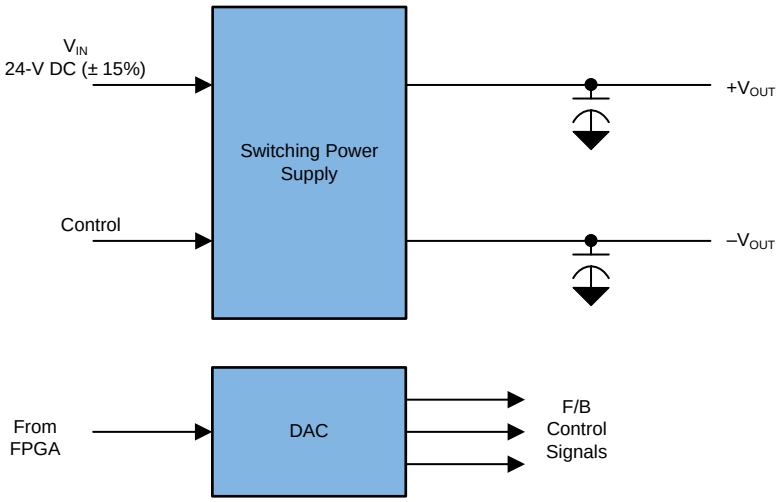


図 2. Typical Power Supply Scheme in Medical Ultrasound Application

2.1 Block Diagram

図 3 shows the block diagram of the reference design. The design is powered by an input supply of 24 V ± 15%, and the output lines generate dual positive and negative outputs using one transformer with a turns ratio (n) of 5.5. The output voltage can be varied from 0 V to ±100 V through the feedback control loop. The output can be set by applying a DC control voltage (0 V to 5 V) at the inverting terminal of the TVL171IDBVR operational amplifier (op amp). The control voltage can also be implemented through DAC output from the FPGA in the system that is controlled by software. The reference for DAC implementation can be accessed from the *400-W Continuous, Scalable, ±2.5- to ±150-V, Programmable Ultrasound Power Supply Reference Design*.

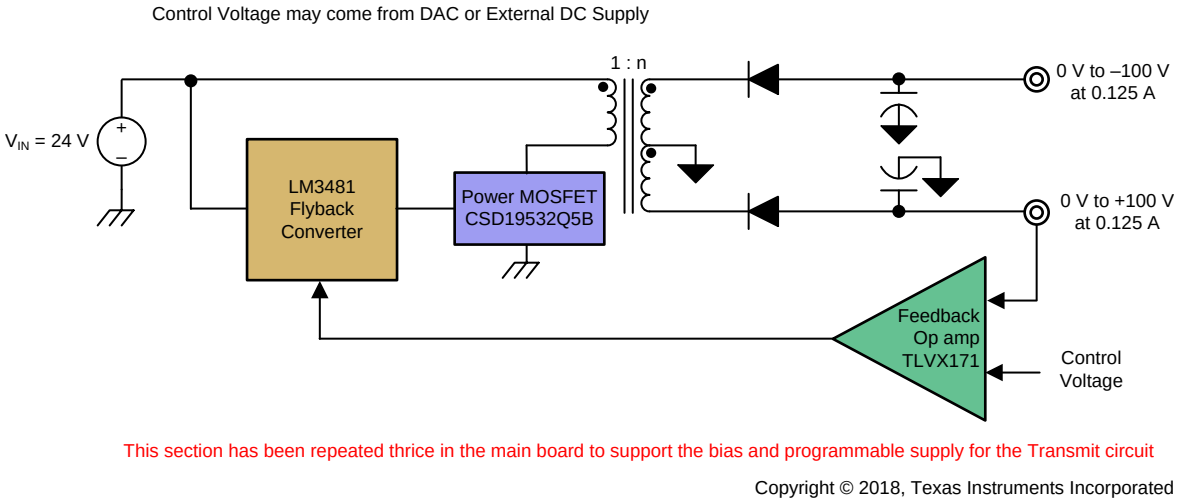


図 3. Block Diagram of Reference Design

The load applied at the output for this reference design must be symmetrical in nature; therefore, the feedback is taken from only one output rail that is the positive HV rail. The SMPS is designed in the flyback topology, and the LM3481 power controller device is used to drive the gate of the MOSFET. The feedback loop has an op amp that acts as a high gain error amplifier. The set voltage (from 0 V to 5 V) can be applied at the inverting input where the required output voltage is set. The op amp drives the COMP (3) pin of the LM3481 device (図 7) through a transistor that modulates the output voltage by pulling current from the LM3481 device.

2.2 Highlighted Products

2.2.1 LM3481 High-Efficiency Controller for Boost, SEPIC, and Flyback DC/DC Converters

The LM3481 device is a versatile low-side N-FET high-performance controller for switching regulators. The device is designed for use in boost, single-ended primary-inductor converter (SEPIC), flyback converters, and topologies that require a low-side FET as the primary switch. The LM3481 device can be operated at very high switching frequencies to reduce the overall solution size. The switching frequency of the LM3481 device can be adjusted to any value from 100 kHz to 1 MHz with one external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit can be programmed with one external resistor.

The LM3481 device has built-in protection features such as thermal shutdown, short-circuit protection, and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 5 µA and allows for power supply sequencing. Internal soft-start limits the inrush current at start-up. Integrated current-slope compensation simplifies the design and can be increased using a single resistor, if needed for specific applications.

2.2.2 CSD19532Q5B N-Channel Power MOSFET

The CSD19532Q5B device is a 100-V N-Channel NexFET™ power MOSFET that is available in a VSON-CLIP package that has a thermal pad for better dissipation of heat. The device has an $r_{DS(on)}$ of 4.9 mΩ that helps minimize losses in power-conversion applications. The device has a gate-source threshold voltage ($V_{GS(th)}$) of 2.6 V. It is widely used in synchronous rectifier for offline and isolated DC/DC converters, motor control, and so on.

2.2.3 TLVx171 Single-Supply, Low-Power, Operational Amplifier

The 36-V TLVx171 device family provides a low-power option for cost-conscious industrial systems that require an electromagnetic interference (EMI) hardened, low-noise, single-supply op amp that operates on supplies ranging from 2.7 V (±1.35 V) to 36 V (±18 V). The single-channel TLV171, dual-channel TLV2171, and quad-channel TLV4171 devices provide low offset, low drift, and low quiescent current balanced with high bandwidth for the power. This series of op amps has rail-to-rail input and output.

2.3 System Design Theory

2.3.1 Operation Principle of the Flyback Converter

A flyback converter is the most commonly used SMPS circuit for low output power applications where the output voltage must be isolated from the input main supply. The flyback topology is essentially the buck-boost topology that is isolated by using a transformer as the storage inductor. 図 4 shows the practical flyback converter circuit. The snubber circuit consists of a fast recovery diode in series with a parallel combination of a snubber capacitor and a resistor. The leakage-inductance current of the primary winding finds a low impedance path through the snubber diode to the snubber capacitor. The power that is lost in the snubber circuit reduces the overall efficiency of the flyback-type SMPS circuit.

The flyback converter operation is divided into two steps.

1. In the first step, the switch Q is turned on and energy is stored (from the input) in the primary winding of the flyback transformer. On the secondary side, diode D is reverse-biased and the load is supplied through energy stored in output capacitor (C).
2. In the second step, the switch is turned off and the energy stored in primary winding is transferred to secondary. The diode D is forward-biased, and the energy is delivered to charge the output capacitor (C) and supply the load.

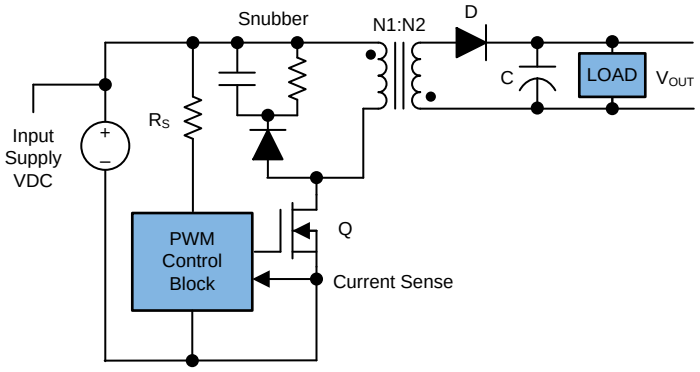


図 4. Power Transfer Topology of Flyback Converter

There are three basic modes of operations in the flyback converter:

- Continuous conduction mode (CCM)
- Discontinuous conduction mode (DCM)
- Critical conduction mode (CRM)

In CCM, part of the energy stored in the flyback transformer remains in it when next time the switch turns on. The primary current starts from a value greater than zero at the beginning of each cycle because all the stored energy is not transferred when switch is OFF. 図 5 shows all the important waveforms for CCM.

In DCM, all the stored energy from the primary of the transformer is transferred to the output when the switch is OFF. As a result, the primary current starts from zero at the beginning of each switching cycle. The CRM (also called transition mode [TM]), occurs at the boundary between DCM and CCM, precisely when the stored energy reaches zero at the end of the switching period.

During the ON time, the inductor current through primary winding (N_1) can be calculated using 式 2.

$$V_L = \frac{L dI_L}{dt}; V_L = \frac{L \Delta I_L}{\Delta t}$$
$$\Delta I_L = \frac{V_L \times \Delta t}{L} \quad (1)$$

where

- ΔI_L is the change in the primary inductor current
- Δt is the ON duration of the switch, Q
- V_L is the voltage across the inductor
- $\Delta t = Dt_S$
- D is the duty cycle
- t_S is the switching period of the flyback converter (2)

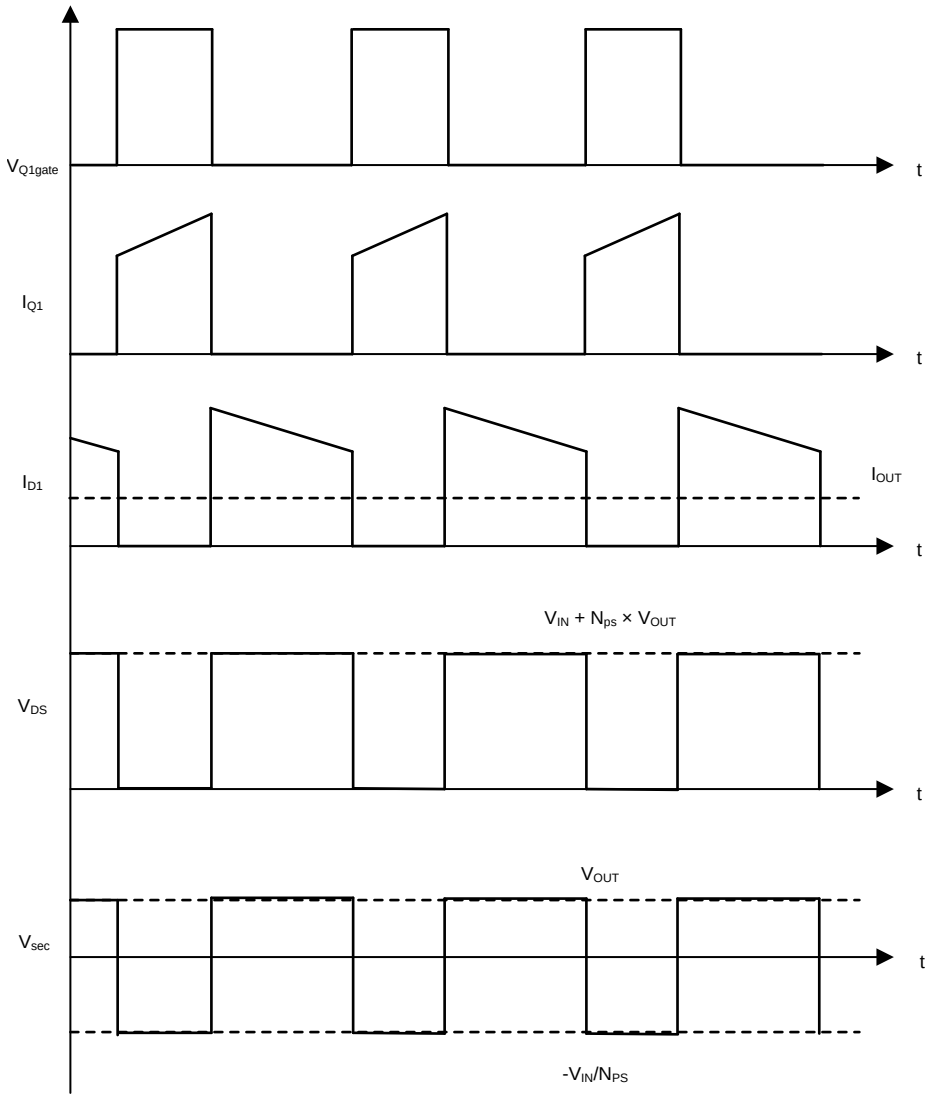


図 5. Flyback Current-Voltage Waveforms in Continuous Conduction Mode

$$\Delta I_{L(on)} = V_{IN} \times \left(\frac{D \times t_S}{L_{pri}} \right)$$

where

- L_{pri} is the primary inductance of the transformer (3)

Similarly, the decrease in inductor current in the secondary winding during the off duration of the flyback converter can be calculated using 式 4.

$$\Delta I_{L(off)} = V_{OUT} \times N_{PS} \times (1 - D) \times \frac{t_S}{L_{pri}} \quad (4)$$

In steady-state conditions, the current increase ($\Delta I_{L(on)}$) during the ON time and the current decrease during the OFF time ($\Delta I_{L(off)}$) must be equal. Otherwise, the inductor current will have a net increase or decrease from cycle-to-cycle. The outcome is the transfer function that is calculated using 式 5.

$$V_{OUT} = \frac{V_{IN}}{N_{PS}} \times \frac{D}{1-D} \quad (5)$$

where

- $N_{PS} = N_1 / N_2$

2.3.2 Design of the Flyback Converter

This section explains the theory, component selection, and design details for the power converter using the LM3481 device. The reference design has three identical sections of the power converter that are repeated to provide the power supply for the portable ultrasound scanner system, which consists of fixed and programmable outputs. 図 6 shows the block-level implementation in the reference design where three sections are repeated to provide multiple supply configurations as described in 表 2. 図 7 show the full schematic of one such section implemented on the board; the other sections are similar.

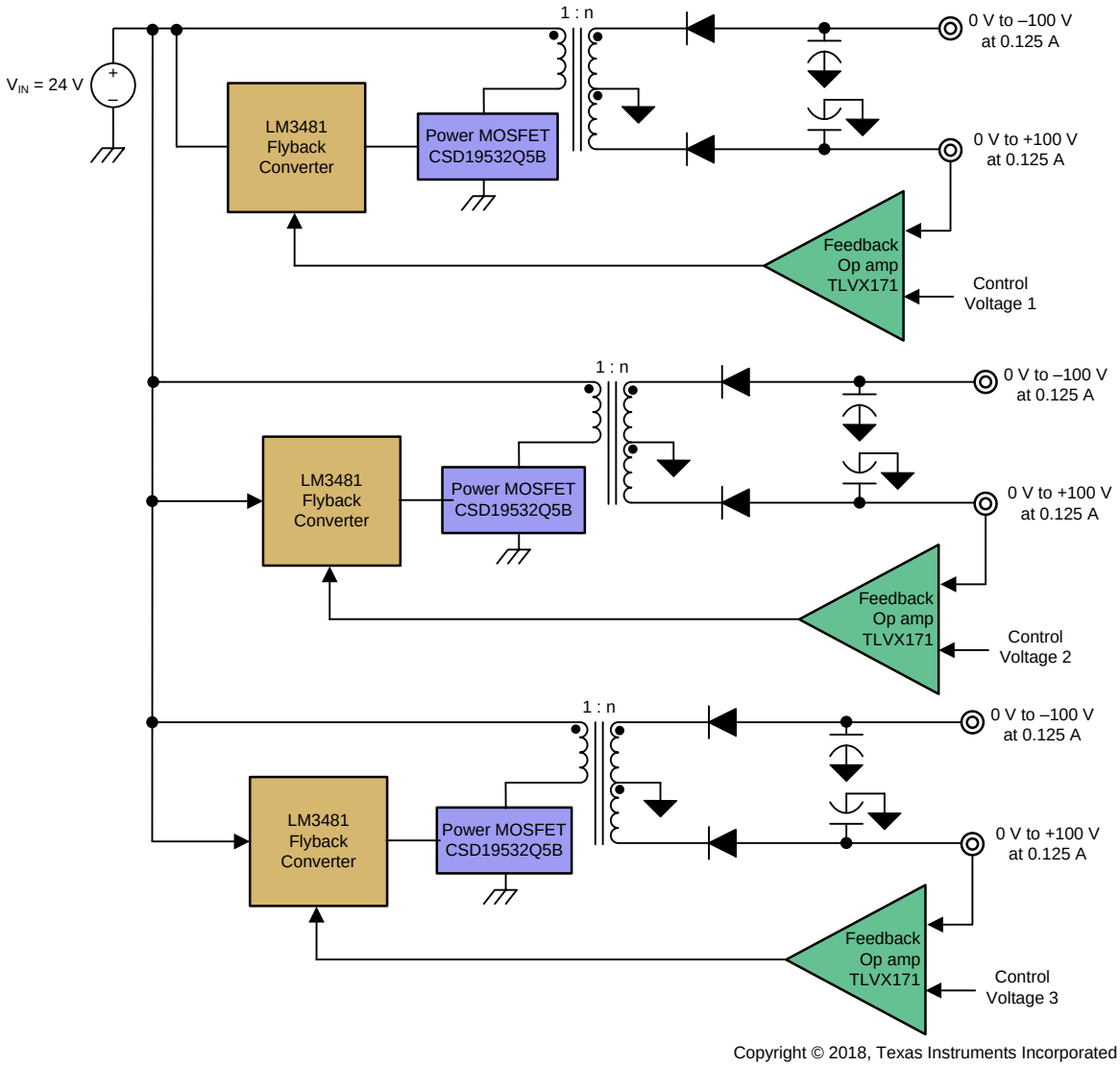


図 6. Full System Level Diagram of the Reference Design Implemented on the Board

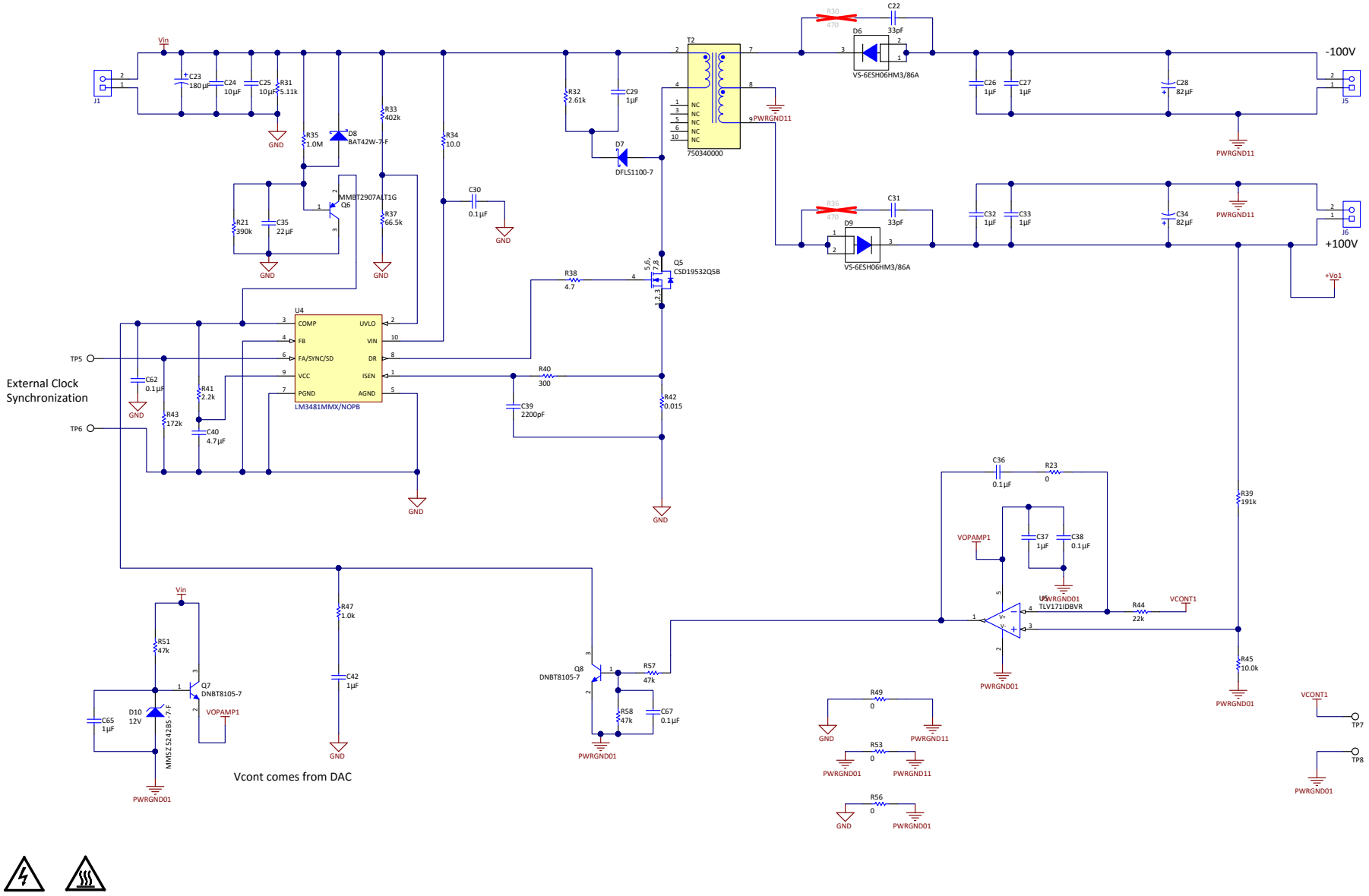


図 7. Full Schematic of the Reference Design

2.3.2.1 Input Section and Turnon Mechanism

The reference design is intended to be operated with an input DC supply of 24 V ± 15%. The LM3481 device is powered through a 10-Ω resistor (R34) from the input supply to the supply pin V_{IN} (pin 10 of the LM3481 device), as shown in 図 8. The C30 supply decoupling capacitor goes from the V_{IN} pin of the LM3481 device to GND.

2.3.2.1.1 Input Capacitor Selection

The input section in the reference design consists of an input capacitor with a value of 200 µF with a 180-µF electrolytic capacitor in parallel with two 10-µF ceramic capacitors to reduce ESR, as shown in 図 8. This specific capacitor selection provides the ripple in input voltage that can be calculated using 式 6.

$$V_{IN,ripple} = I_{avg} \times \frac{t_{on}}{C_{in}} = 45\,mV \quad (6)$$

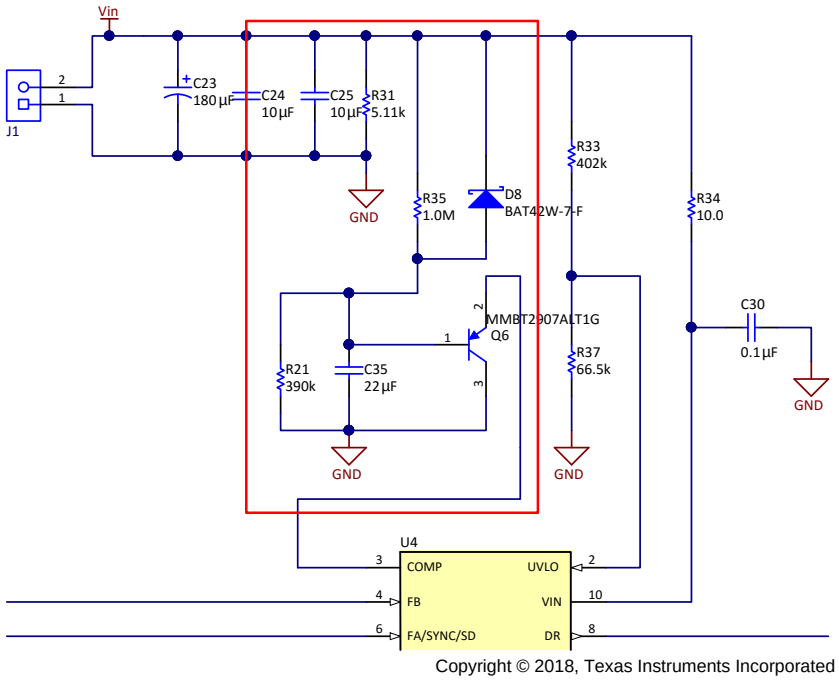
where

- I_{avg} is the average input current, which is 2 A (as calculated using 式 14)

2.3.2.1.2 Soft Start (SS)

At the start when the input voltage is applied, the output voltage is 0 V and it begins to rise to the set value. To avoid sudden surges or spikes in voltage that could damage the components, the output is configured to slowly rise to the desired value. The input section has an external circuit to provide a soft start when the system is turned on. The pin 3 (COMP) of the LM3481 device is pulled down by the PNP transistor, which pulls current from the pin when the system turns on. The 22-µF capacitor (C35) slowly charges up to 6.7 V, which cuts off the transistor, and the feedback system initiates to bring the output voltage up to the required value. 図 8 shows the soft start (SS) circuit in the input section that is highlighted in red. The SS circuit consists of an RC network (R35, R21, and C35) coupled with transistor (Q6).

The R31 resistor provides a path to quickly discharge the C35 capacitor through diode D8 in case the power is turned off.



The SS circuitry is highlighted by the red rectangle.

図 8. Input Section of the Reference Design

2.3.2.1.3 Undervoltage Lockout (UVLO)

Pin 2 (UVLO) of the LM3481 device provides the user with programmable enable and shutdown thresholds. The UVLO pin is compared to an internal reference of 1.43 V generated by the LM3481 device, and a resistor divider programs the enable threshold (V_{EN}). When the device is enabled, the UVLO pin sources a 5-µA current, which effectively causes a hysteresis. Now the UVLO shutdown threshold (V_{SH}) is lower than the enable threshold. Two resistors (R33 and R37) are required to set these thresholds. 図 8 shows R33 and R37 connected from the V_{IN} pin to the UVLO pin and from the UVLO pin to GND. The values of these resistors is calculated using 式 7 and 式 8.

$$R_{37} = \frac{1.43}{I_{UVLO}} \times \left(1 + \frac{1.43 - V_{SH}}{V_{EN} - 1.43}\right) \quad (7)$$

where

- V_{SH} = 8 V
- R37 = 66.5 kΩ

$$R_{33} = R_{37} \times \left(\frac{V_{EN}}{1.43} - 1\right) \quad (8)$$

where

- V_{EN} = 10 V
- V_{SH} = 8 V
- R33 = 402 kΩ

2.3.2.2 Transformer Design

Depending on the application, flyback converters can be designed in the modes CCM, DCM, or CRM.

CCM mode provides the following benefits:

- Lower ripple
- Lower root-mean-square (rms) current
- Lower MOSFET conduction and turn-off losses
- Better efficiency at full load

DCM provides better switching conditions for the rectifier diode because it is operating at zero current just before becoming reverse biased; therefore there are no recovery losses. The form factor is also smaller because the average energy storage is relatively small. However, DCM has high rms current that translates into higher conduction losses in MOSFET and stress on the output capacitor. DCM is therefore recommended for high-voltage and low-current applications.

The flyback parameters are designed considering the worst condition possible at maximum load and minimum input voltage. The turns ratio required is derived using 式 5 and can be calculated with 式 9.

$$N_{SP} = \frac{N_2}{N_1} = \frac{V_{OUT}}{V_{IN,min}} \times \frac{1 - D_{max}}{D_{max}}$$

where

- N_{SP} is the turns ratio of the secondary winding to the primary winding
- D_{max} is the maximum duty cycle (chosen to be 0.45) at which the system is allowed to operate (9)

With $V_{IN,min}$ = 20.4 V, the calculated turns ratio is $N_{SP} \approx 6$. The transformer turns ratio value of 5.5 is used in the design.

The reflected voltage (V_{RO}) on the primary side when the switch is OFF is calculated using 式 10.

$$V_{RO} = \frac{N_1}{N_2} \times V_{OUT} = \frac{100}{6} \approx 17\ V \quad (10)$$

Assuming the efficiency (η) of the design is 85%, the following relation between the input power and the output power at maximum load brings the total output power to 25 W (12.5 + 12.5), which can be calculated using 式 11.

$$P_{IN} = \frac{P_O}{\eta} \approx 30\,W \quad (11)$$

Therefore, the primary inductance of the transformer can be calculated using 式 12.

$$L_{pri} = \frac{\left(V_{IN,min} \times D_{max}\right)^2}{2 \times P_{IN} \times f_S \times K_{RF}}$$

where

- K_{RF} is the ripple factor, which is 1 in the case of DCM (12)

At the switching frequency of 125 kHz, the value of the primary inductance (L_{pri}) is 11.2 µH. The selected value in this reference design is 13 µH. The peak input current is calculated using 式 13.

$$I_{Peak,pri} = I_{EDC} + \frac{\Delta I}{2} = \frac{P_{IN}}{V_{IN,min} \times D_{max}} + V_{IN,min} \times \frac{D_{max}}{L_{pri} \times f_S} = 5.04\ A \quad (13)$$

$$I_{RMS,pri} = \sqrt{\left(3 \times I_{EDC}\right)^2 + \left(\frac{\Delta I}{2}\right)^2 \times \frac{D_{max}}{3}} \approx 2\,A \quad (14)$$

$$I_{RMS,sec} = I_{RMS,pri} \sqrt{\frac{1 - D_{max}}{D_{max}}} \times \frac{V_{RO}}{2 \times \left(V_{OUT} + V_F\right)} \approx 0.183\,A$$

where

- V_F is forward drop of the diode
- I_{EDC} is the value of current at the start of every cycle in primary winding (15)

2.3.2.3 MOSFET and Output Diode Selection

The maximum stress on the MOSFET occurs immediately when the switch is turned off. This stress is caused by the components (namely the input voltage, reflected voltage on the primary, and the spike that is due to the leakage inductance of the primary winding of the transformer). The voltage rating of the MOSFET and the diode must be chosen with appropriate margin because both components suffer from high voltage spikes. In the case of the MOSFET, the primary leakage inductance resonates with the output capacitance of the MOSFET. Similarly in the case of the diode, secondary leakage inductance resonates with the diode capacitance and results in high voltage spikes. Considering these potential spikes in voltage, TI recommends choosing a voltage rating from 1.5× to 2× than the obtained value to ensure a sufficient margin.

式 16 and 式 17 are used to calculate the voltage stress across the MOSFET and the diode, which is 88.6 V and 398.4 V, respectively. Similarly, the maximum current in these devices is 5 A and 1.5 × 0.183 A, which is 0.275 A, respectively. Therefore, the devices must be rated above the values indicated here. The CSD19532Q5B MOSFET is rated for 100 V, 100 A. The diode in the design is rated for 600 V, 6 A.

$$V_{DS,MOS} = (\text{from 1.5 to 2}) \times (V_{IN,max} + V_{RO}) \quad (16)$$

$$V_{Rev,Diode} = (\text{from 1.2 to 1.5}) \times (V_{OUT} + V_{IN,max} \times N_{SP}) \quad (17)$$

2.3.2.4 Current Sensing

Pin 1 (I_{SEN}) of the LM3481 device provides protection from short circuit situations and generates the duty cycle for the PWM controller by sensing the current through the MOSFET. In case of a short circuit when the short-circuit current limit is activated, there is an internal comparator that compares the voltage on the I_{SEN} pin to 220 mV. A comparator inside the LM3481 device reduces the switching frequency by a factor of 8 and maintains this condition until the short is removed.

The value of the current sense resistor is chosen such that the maximum limit voltage for I_{SEN} is 100 mV. For the peak current of 6 A, the maximum limiting resistance (R_{SEN}) for I_{SEN} is calculated using 式 18.

$$R_{SEN} = \frac{100\,mV}{6\,A} = 16.7\,m\Omega \quad (18)$$

The value used in this reference design is 15 mΩ, which makes the peak current limit of 6.6 A.

2.3.2.5 Snubber Circuit Design

When the FET is turned off, due to less-than-optimal coupling between the primary and secondary side of the transformer, some energy is trapped in the leakage inductance of the windings. This energy must then be dissipated in the external snubber circuit. Otherwise, there will be a voltage spike across the windings that can destroy the circuit.

The snubber circuit that is shown in 図 9 should not take mutual flux. Therefore, the voltage across the C_{SN} capacitor (C29) is kept higher than what is reflected from the secondary side. TI recommends choosing a proper snubber resistor R_{SN} (R32) that has a large RC time constant as compared to the switching period.

The leakage inductance (L_{Leak}) can be modeled in series with MOSFET. When MOSFET turns OFF, L_{Leak} induces a voltage spike that could damage the FET if the voltage rating is exceeded. Therefore after the FET is turned OFF, the snubber circuit provides a path for the current and dissipates the energy.

Energy stored in L_{Leak} after Q5 is turned OFF gets transferred to C_{SN}, which can be calculated using 式 19.

$$E_{SN} = \frac{1}{2} L_{Leak} \times I_{Peak}^2 = 8.89\ \mu J \quad (19)$$

where

- L_{Leak} is assumed to be 5% of the L_{pri}, which is 5% of 14 µH, which is calculated as 0.7 µH
- I_{Peak} = 5.04 A

Therefore, the average power can be calculated with 式 20.

$$P_{SN} = E_{SN} \times f_S = 1.1\ W \text{ at } f_S = 125\ kHz \quad (20)$$

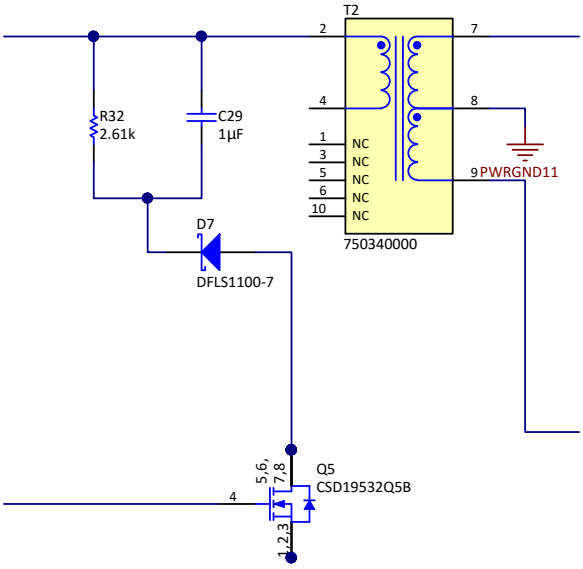


図 9. Snubber Circuit for the Reference Design

The peak voltage that the transistor is clamped to can be calculated with 式 21.

$$V_Q = V_{SN} + V_{IN,max} > V_{IN,max} + \frac{V_{OUT}}{n}$$

where

- n is the turns ratio of the transformer
- V_Q > 27.6 + 100 / 44.2 V (21)

Assuming that V_{SN} is 42 V (30 to 40% higher than the input voltage), the outcome is $V_Q \approx 70$ V.

Choose the value of C_{SN} and R_{SN} based on the two criteria calculated with 式 22 and 式 23.

$$C_{SN} >> \frac{t_S}{R_{SN}} \quad (22)$$

$$\frac{V_{SN}^2}{R_{SN}} = \frac{1}{2} L_{Leak} \times I_{Peak}^2 \times f_S \geq R_{SN} > 1.98\ k\Omega \quad (23)$$

図 9 shows the snubber circuit schematic of the reference design. The value used for C_{SN} (C29) is 1 µF, and the value used for R_{SN} (R32) is 2.61 kΩ.

2.3.2.6 Setting Output Using Feedback Circuit

The output of this reference design can be set by applying a DC voltage (V_{cont}) to the inverting input of the TLV171IDBVR op amp. This application compares the fraction of the output voltage to the set voltage (V_{cont}) and sends the feedback to the COMP pin of the LM3481 device, which increases or decreases the duty of the PWM to match the output to the set value. The control voltage can be supplied directly through a DC supply or can come from DAC through the software command. The implementation of DAC can be referenced through the 400-W Continuous, Scalable, ±2.5- to ±150-V, Programmable Ultrasound Power Supply Reference Design.

図 10 shows the implemented feedback circuit for the non-isolated power supply configuration in the reference design. The output voltage ($+V_{O1}$) varies from 0-V to 100-V DC. The gain for the feedback input is set to 0.0497 (= 10 k / 201 k). The gain at maximum output voltage is 4.97 V. This gain is then compared with the control voltage (V_{CONT1}) and the output of the op amp drives the Q8 transistor. The R57 and the R58 resistors (both are 47 kΩ) are used for scaling the output of the op amp to drive Q8. The collector of Q8 is used to pull down or pull up the voltage on pin 3 (COMP) of the LM3481 device (U4) based on the result of comparison between output and control voltage. Together, the 1-kΩ resistor R47 and the 1-µF capacitor C42 form the compensation network for the COMP pin.

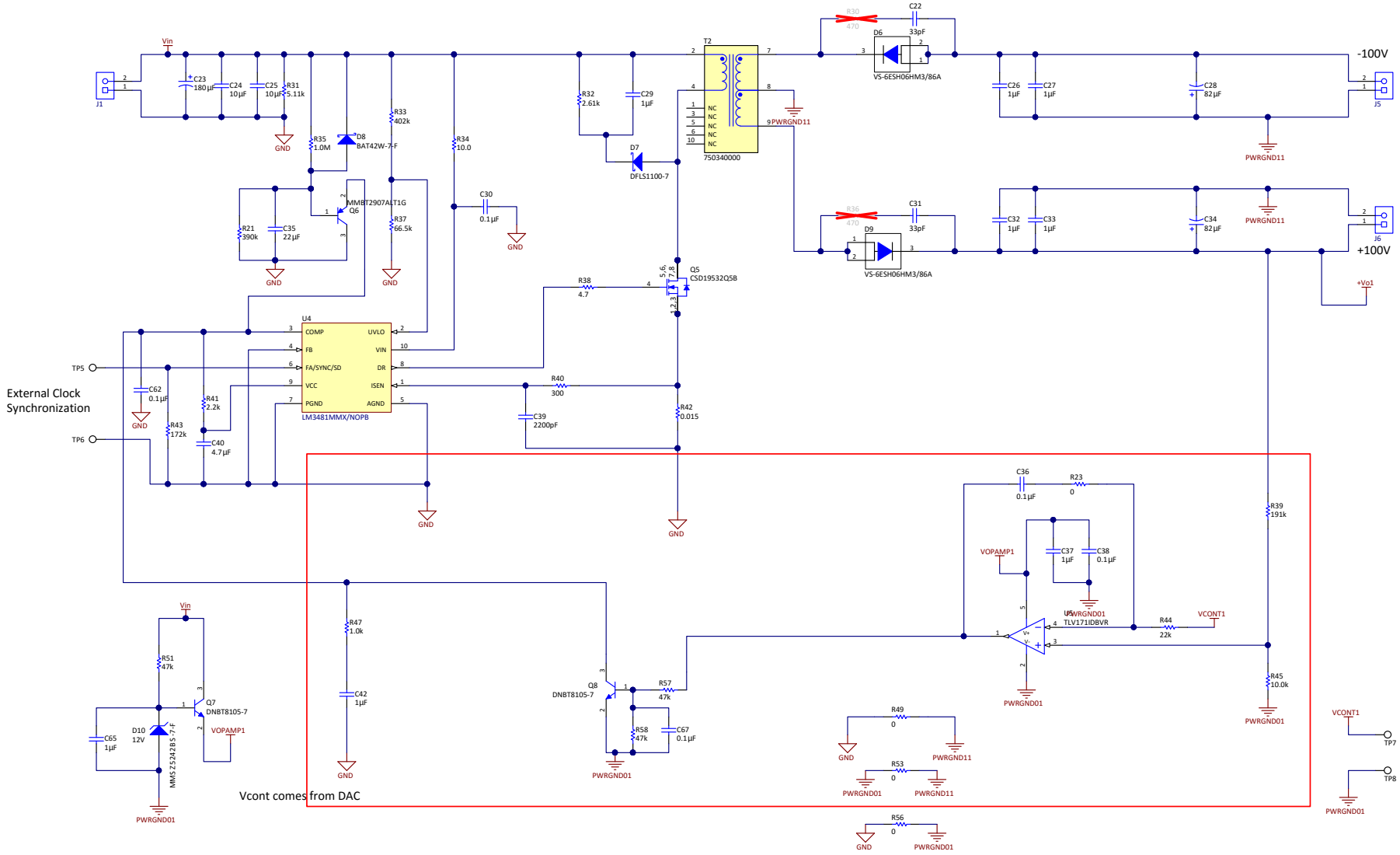


図 10. Feedback Circuit for Non-Isolated Power Supply Configuration in the Reference Design

図 11 shows the TINA-TI™ simulation software. 図 12 shows the waveforms for V_{OUT} from 0 V to 100 V for the feedback circuit implemented in 図 10. The control voltage is set to 2.5 V, which corresponds to an output voltage of 50 V. At a 50-V output voltage, the feedback shows a steep step at the output of the op amp device. Similarly, 図 13 shows the feedback action as a function of control voltage. Step response is observed at the output voltage of 50 V (V_{CONT} = 2.5 V).

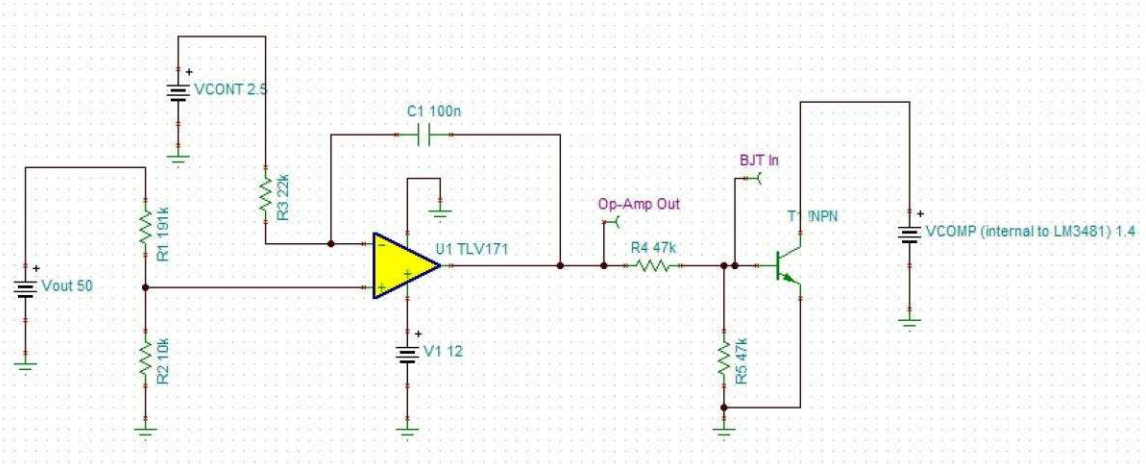


図 11. TINA-TI™ Simulation for the Feedback Circuit of the Non-Isolated Configuration

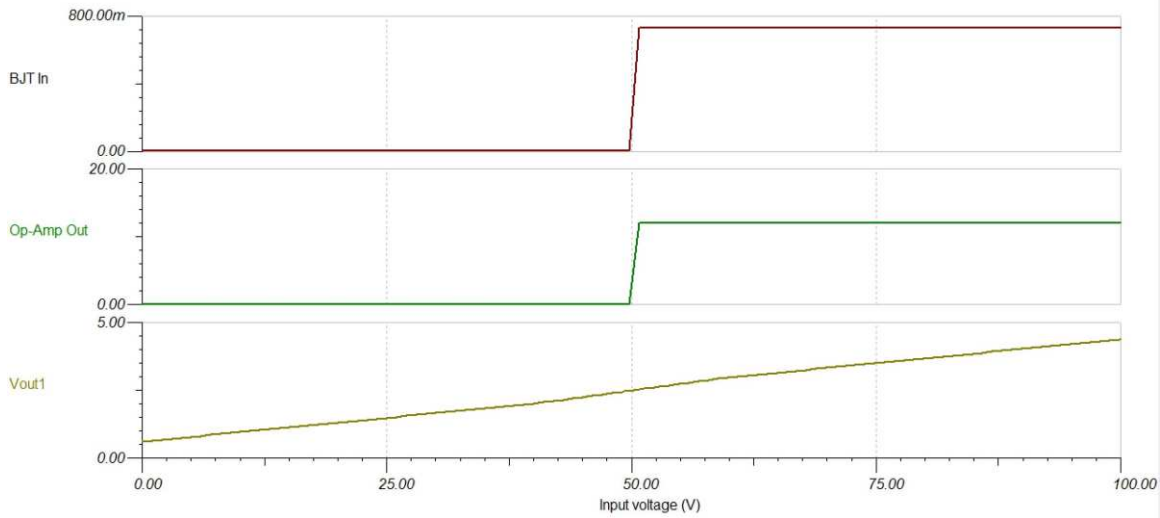


図 12. Simulation Waveforms Showing Linearity in the Feedback of High Voltage Output (Control Voltage = 2.5 V)

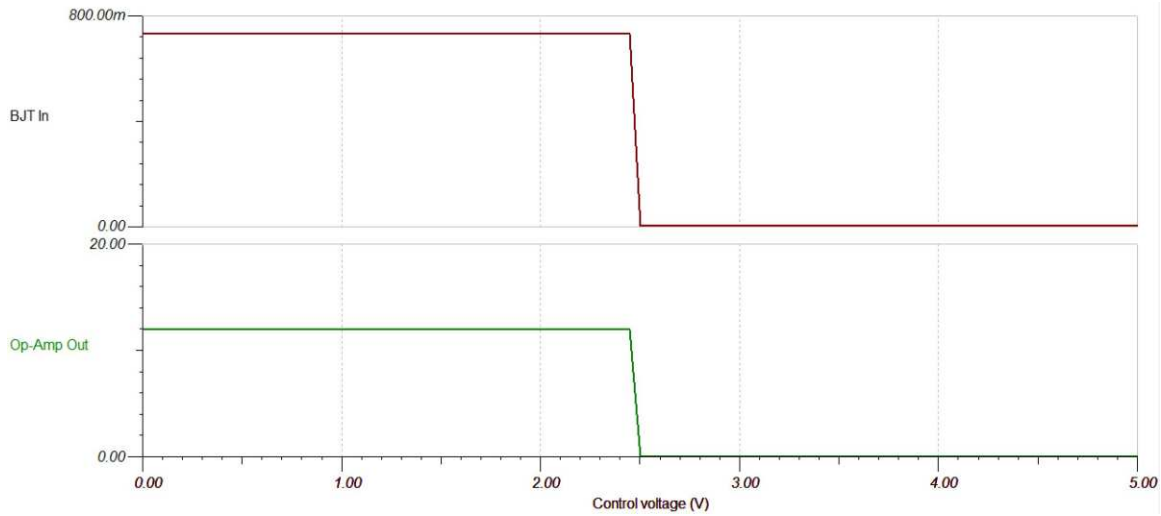


図 13. Simulation Waveforms Showing the Feedback Action With Control Voltage at Output Voltage of 50 V

2.3.2.7 Frequency Synchronization and Sync to External Clock

The switching frequency of the LM3481 device can be adjusted between 100 kHz and 1 MHz using one external resistor. The LM3481 device can also be synchronized to an external clock. The external clock must be connected between the FA/SYNC/SD pin and ground. The frequency adjust resistor can remain connected while synchronizing a signal. Therefore, if there is a loss of signal, the switching frequency will be set by the frequency adjust resistor. The width of the synchronization pulse must be wider than the duty cycle of the converter and the synchronization pulse width must be ≥ 300 ns.

The FA/SYNC/SD pin also functions as a shutdown pin. If a high signal appears for more than 30 µs on the FA/SYNC/SD pin, the LM3481 device stops switching and goes into a low current mode. The total supply current of the device reduces to typically 5 µA under these conditions. In frequency adjust mode, connecting the FA/SYNC/SD pin to ground through an external resistor forces the clock to run at a certain frequency, the value of the required resistor can be calculated with 式 24.

$$R_{FA} = 22 \times \frac{10^3}{f_{SW}} - 5.74 \quad (24)$$

where

- R_{FA} (R43) is the external resistor between the FA/SYNC/SD (pin 6) and ground
- For the switching frequency (f_S) of 125 kHz, the value of R_{FA} is 172 kΩ

2.3.2.8 Selection of Driver Supply Capacitor

For proper operation, a high-quality ceramic bypass capacitor must be connected from the V_{CC} pin to the PGND pin. This capacitor supplies the transient current required by the internal MOSFET driver, and it filters the internal supply voltage for the controller. TI recommends using a value from 0.47 µF to 4.7 µF. A 4.7-µF capacitor is chosen in this reference design.

2.3.2.9 Selection of Output Capacitor and Generation of Feedback Power Supply

The output section in the reference design consists of an 84-µF output capacitor and an 82-µF electrolytic capacitor in parallel with two 1-µF ceramic capacitors that reduce ESR, as shown in 図 6. If the load is at the maximum (that is, 12.5 W at 100 V, which requires a current of 0.125 A), these capacitors provide the ripple in output voltage, which can be calculated with 式 25.

$$V_{OUT,ripple} = I_{avg} \times \frac{t_{on}}{C_{out}} = 5mV \tag{25}$$

The specifications have a more relaxed condition on the output ripple, but a higher value for the output capacitance is chosen to sustain other modes (such as elastography where the current requirement is much higher).

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware: Reference Design Board Pictures

図 14 and 図 15 show the top and bottom views of the reference design PCB, respectively.

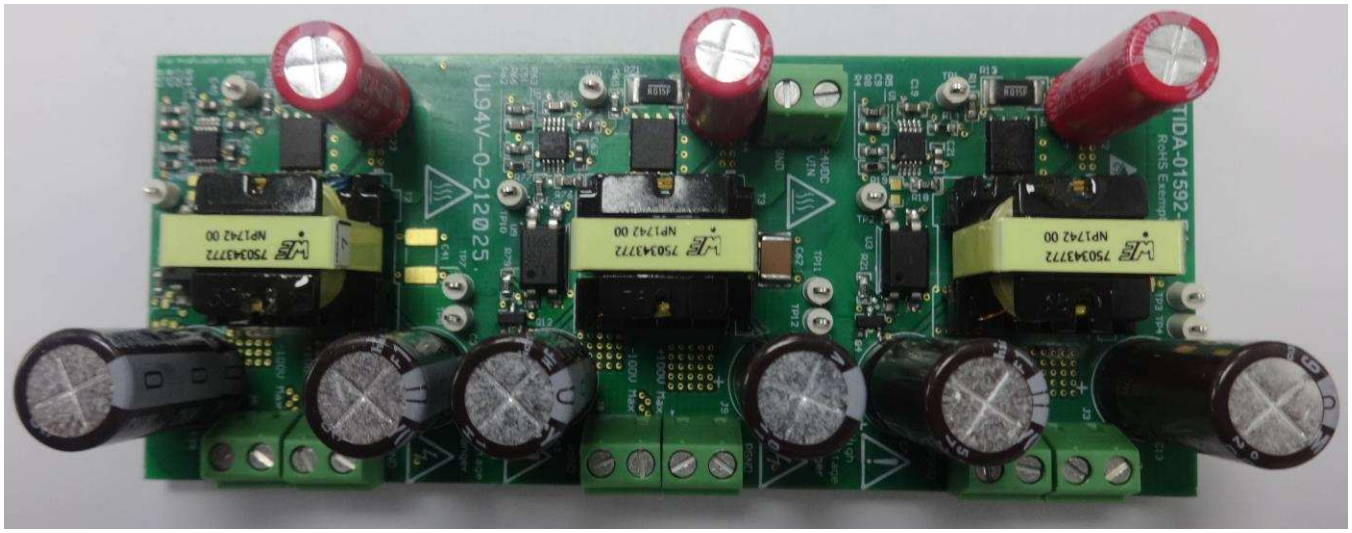


図 14. Reference Design PCB (Top View)

図 15. Reference Design PCB (Bottom View)

3.2 Testing and Results

3.2.1 Test Setup

The positive and negative output sections are tested for different imaging modes. The load profile changes with the imaging mode (see 図 16 and 表 3).

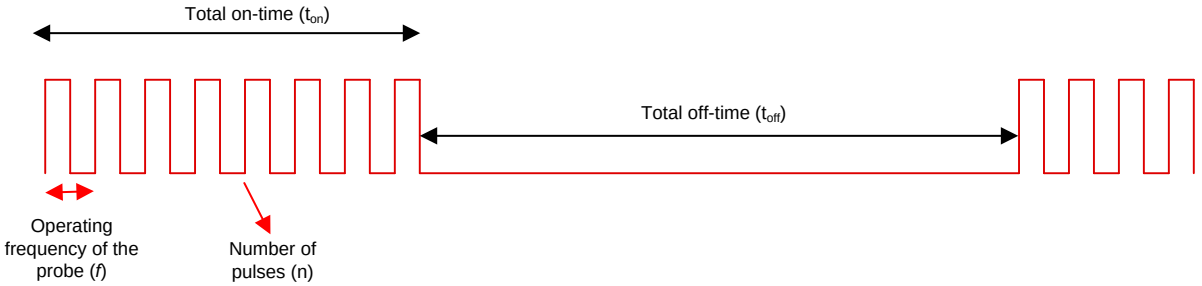


図 16. Load Profile for Testing the Reference Design in Different Imaging Modes

表 3. Conditions for Different Imaging Modes

MODE	t_{on}	t_{off}	t_S
B-Mode	20 µs	180 µs	200 µs
Elastography Mode	20 ms	180 ms	200 ms

WARNING

This reference design produces high voltages that can cause injury. Ensure that all safety procedures are followed when working on the reference design board. Never leave a powered board unattended.

3.2.2 Test Results

3.2.2.1 Control Voltage versus Output Voltage

The output voltage of the reference design can be set through a DC source (0 V to 5 V), which can be applied to the test point provided on the board. Three separate pairs of test points (TP1 and TP2, TP3 and TP4, TP7 and TP8) are provided to independently control each output section. 図 17 shows the output voltage at the positive rail and the negative rail as a function of input control voltage. The control voltage varies from 0 V to 5 V, and the output voltage (positive and negative) follows a linear increase from 0 V to ±100 V.

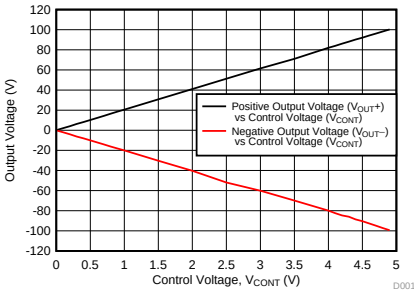


図 17. Control Voltage vs Output Voltage of the Reference Design

3.2.2.2 Load Regulation Performance at Continuous Load

This test evaluates the functional behavior and the performance of the reference design. This reference design is tested in various output and load conditions, and the efficiency of the design is evaluated. The output voltage is fixed and the load current is varied from no-load to full-load conditions. The negative voltage has good regulation with respect to the positive output. 3.2.2.2.1 through 3.2.2.2.4 show the performance of the board at different output voltages. The switching frequency is set to 125 kHz through an external resistor, as described in 2.3.2.7.

3.2.2.2.1 Performance at 100-V Output Voltage

The output voltage is set to 100 V. 図 18 and 図 19 show the regulation of the output voltage when the load current is varied for the positive and negative output rails, respectively.

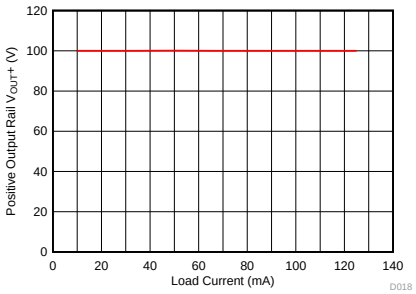


図 18. Regulation of Positive Output Voltage at 100 V With Load Current

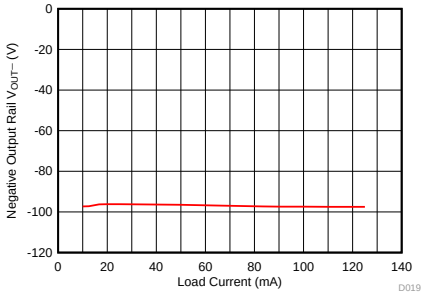


図 19. Regulation of Negative Output Voltage at 100 V With Load Current

図 20 shows the efficiency of the design at a 100-V output voltage as a function of load current. The peak efficiency at full load (12.5 W per rail) is 87%. 図 21 shows the stress on the drain of the MOSFET, and 図 22 shows current sense waveforms with the gate drive at full load (V_{OUT}= 100 V, I_{OUT}= 125 mA at V_{IN}= 24 V).

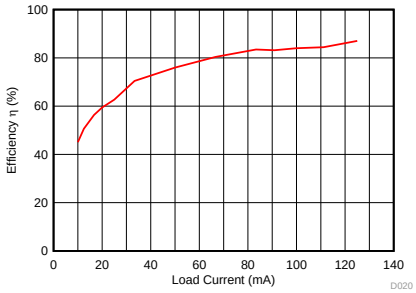


図 20. Efficiency With Load Current at V_{OUT} = 100 V

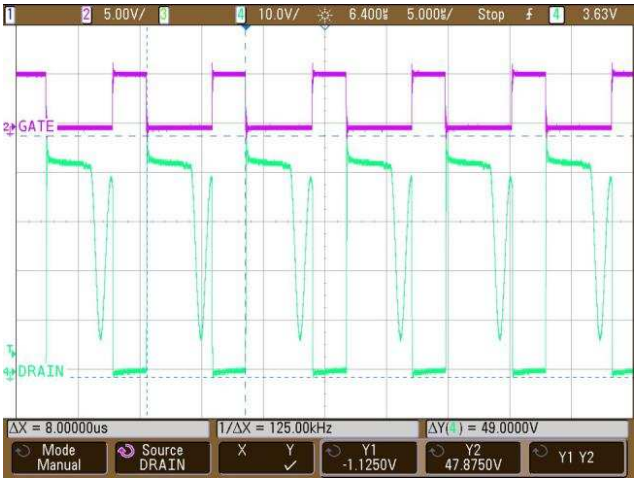


図 21. Stress on the Drain of the MOSFET With Gate Drive at Full Load (V_{OUT} = 100 V, I_{OUT} = 125 mA)

図 22. Current Sense Waveform With Gate Drive at Full Load (V_{OUT} = 100 V, I_{OUT} = 125 mA)

図 23 and 図 24 show the output ripple voltage for the positive rail and the negative rail at 100-V full load, respectively. The measured value of the peak-to-peak ripple is 87 mV for the positive rail and 107.5 mV for the negative rail.

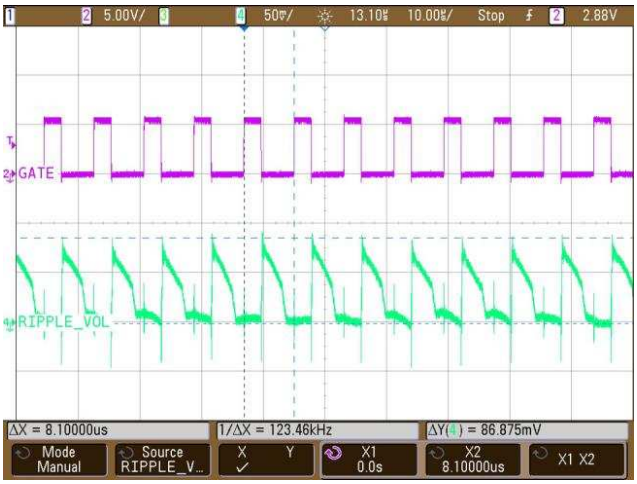


図 23. Output Voltage Ripple at the Positive Rail at 100-V Full Load

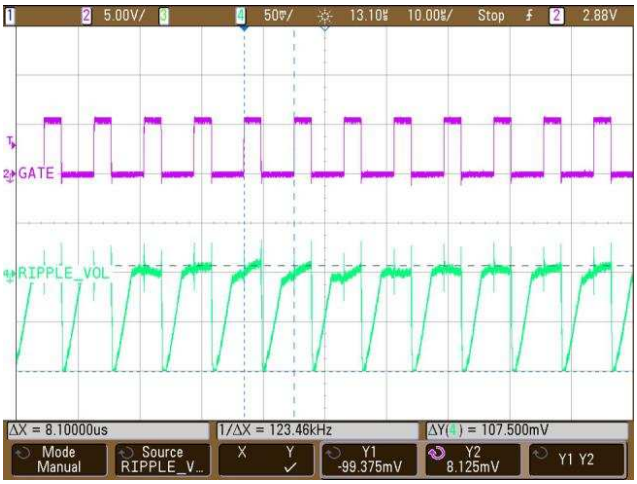


図 24. Output Voltage Ripple at the Negative Rail at 100-V Full Load

3.2.2.2.2 Performance at 80-V Output Voltage

The output voltage is set to 80 V. 図 25 and 図 26 show the regulation of the output voltage when the load current is varied for the positive and negative output rails, respectively.

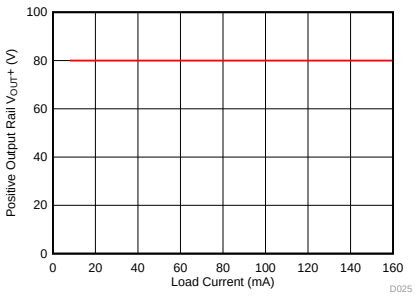


図 25. Regulation of Positive Output Voltage at 80 V With Load Current

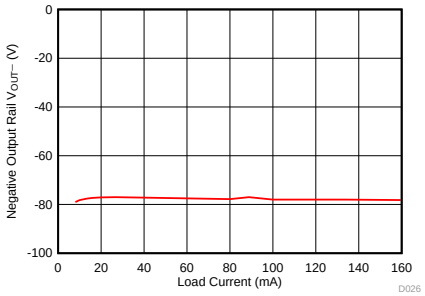


図 26. Regulation of Negative Output Voltage at 80 V With Load Current

図 27 shows the efficiency of the design at a 80-V output voltage as a function of load current. The peak efficiency at full load (12.5 W per rail) is 86%. 図 28 and 図 29 shows the stress on the drain of the MOSFET and current sense waveforms with the gate drive at full load (V_{OUT}= 80 V, I_{OUT}= 160 mA at V_{IN}= 24 V), respectively.

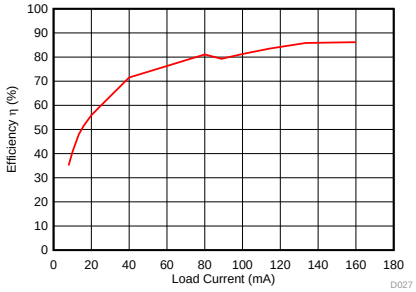


図 27. Efficiency With Load Current at V_{OUT} = 80 V

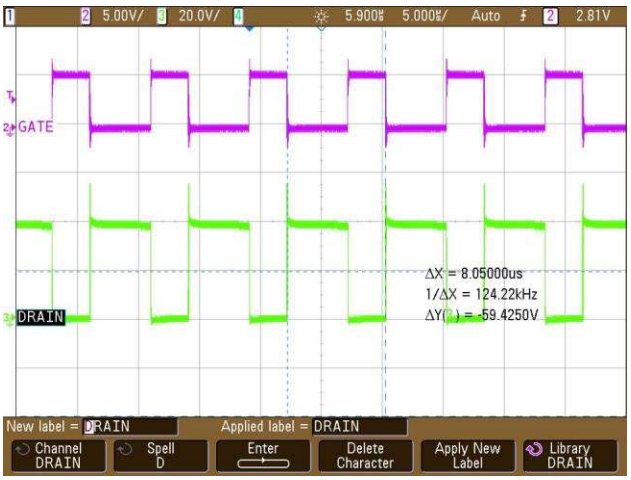


図 28. Stress on the Drain of the MOSFET With Gate Drive at Full Load (V_{OUT} = 80 V, I_{OUT}= 160 mA)

図 29. Current Sense Waveform With Gate Drive at Full Load (V_{OUT}= 80 V, I_{OUT}= 160 mA)

図 30 and 図 31 show the output ripple voltage for the positive rail and the negative rail at a 80-V full load, respectively. The measured value of the peak-to-peak ripple is 88.75 mV for the positive and 119.4 mV for the negative rail.

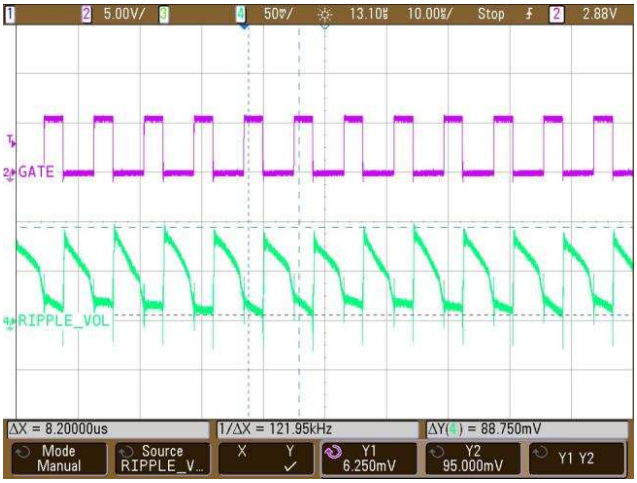


図 30. Output Voltage Ripple at the Positive Rail at 80-V Full Load

図 31. Output Voltage Ripple at the Negative Rail at 80-V Full Load

3.2.2.2.3 Performance at 50-V Output voltage

The output voltage is set to 50 V. 図 32 and 図 33 show the regulation of the output voltage when the load current is varied for positive and negative output rails, respectively.

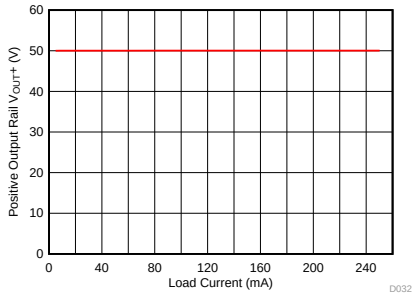


図 32. Regulation of Positive Output Voltage at 50 V With Load Current

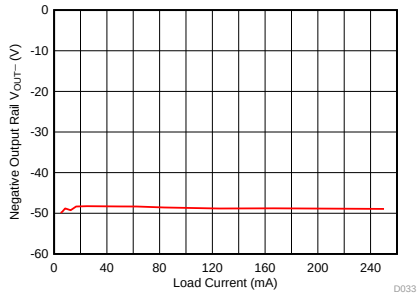


図 33. Regulation of Negative Output Voltage at 50 V With Load Current

図 34 shows the efficiency of the design at a 50-V output voltage as a function of load current. The peak efficiency at full load (12.5 W per rail) is 85.03%. 図 35 and 図 36 shows the stress on the drain of the MOSFET and current sense waveforms with the gate drive at full load (V_{OUT} = 50 V, I_{OUT} = 250 mA at V_{IN} = 24 V), respectively.

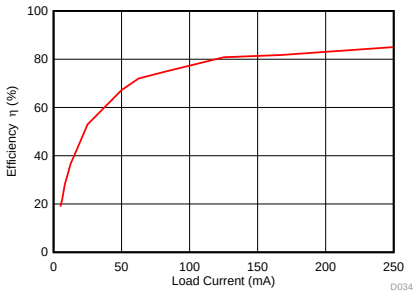


図 34. Efficiency With Load Current at V_{OUT} = 50 V

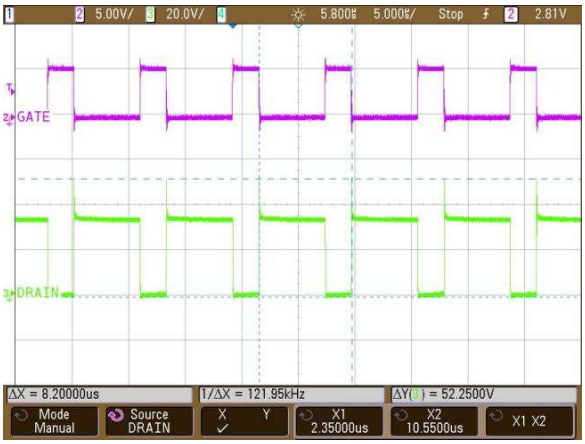


図 35. Stress on the Drain of the MOSFET With Gate Drive at Full Load (V_{OUT} = 50 V, I_{OUT} = 250 mA)

図 36. Current Sense Waveform With Gate Drive at Full Load (V_{OUT} = 50 V, I_{OUT} = 250 mA)

図 37 and 図 38 show the output ripple voltage for the positive rail and the negative rail at a 50-V full load, respectively. The measured value of the peak-to-peak ripple is 82.5 mV for the positive rail and 116.25 mV for the negative rail.

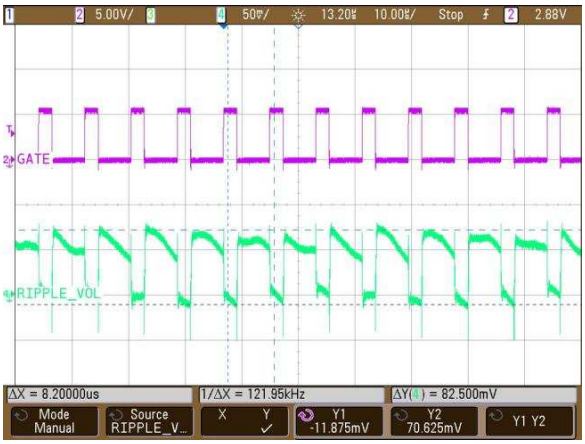


図 37. Output Voltage Ripple at the Positive Rail at 50-V Full Load

図 38. Output Voltage Ripple at the Negative Rail at 50-V Full Load

3.2.2.2.4 Performance at 10-V Output Voltage

The output voltage is set to 10 V. 図 39 and 図 40 show the regulation of the output voltage when the load current is varied for the positive and negative output rails, respectively.

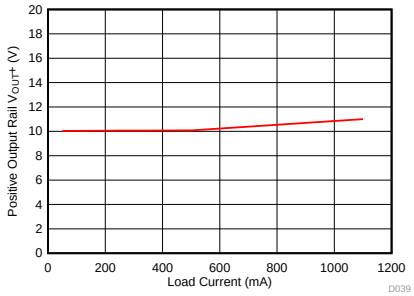


図 39. Regulation of Positive Output Voltage at 10 V With Load Current

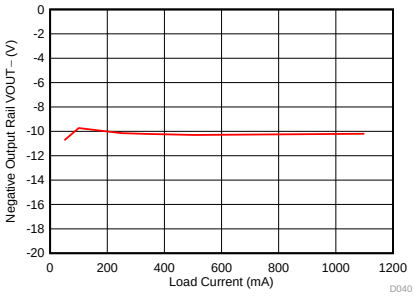


図 40. Regulation of Negative Output Voltage at 10 V With Load Current

図 41 shows the efficiency of the design at 10-V output voltage as a function of load current. The peak efficiency at full load (11 W per rail) is 70%. 図 42 and 図 43 shows the stress on the drain of the MOSFET and current sense waveforms with the gate drive at full load (V_{OUT} = 10 V, I_{OUT} = 300 mA at V_{IN} = 24 V), respectively.

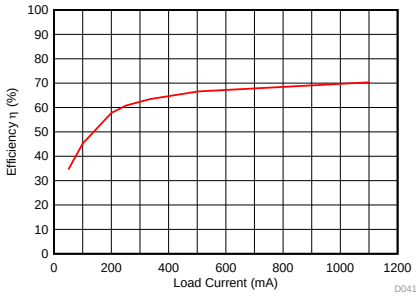


図 41. Efficiency With Load Current at V_{OUT} = 10 V

図 42. Stress on the Drain of the MOSFET With Gate Drive at 300-mA Load (V_{OUT} = 10 V, I_{OUT} = 300 mA)

図 43. Current Sense Waveform With Gate Drive at 300-mA Load (V_{OUT} = 10 V, I_{OUT} = 300 mA)

図 44 and 図 45 show the output ripple voltage for the positive rail and the negative rail at a 10-V full load, respectively. The measured value of the peak-to-peak ripple is 63.75 mV for the positive rail and 104.375 mV for the negative rail.

図 44. Output Voltage Ripple at the Positive Rail at 10 V, 300-mA Load

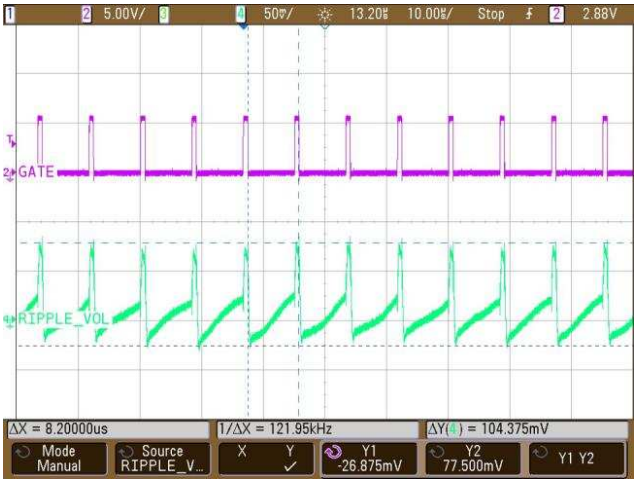


図 45. Output Voltage Ripple at the Negative Rail at 10 V, 300-mA Load

3.2.2.3 Load Mismatch Performance

This reference design uses only one transformer to generate dual outputs and hence the symmetricity at the load side is very critical. This section explores the performance of the reference design with an unsymmetrical load placed at the outputs. The load at the negative terminal is varied between ±15% of the full load value. The variation is observed in terms of regulation at the negative voltage as the load varies and the efficiency is obtained. The positive voltage is kept fixed at 100 V, 80 V, and 50 V. 図 46 through 図 51 show the regulation and efficiency plots for the positive output voltage of 100 V, 80 V, and 50 V, respectively.

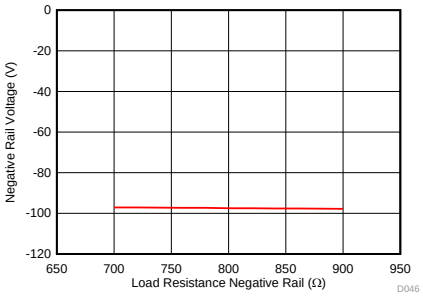


図 46. Load Mismatch at the Negative Rail at 100 V (Full Load at Positive Rail is 800 Ω)

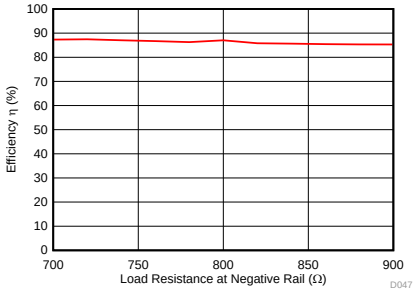


図 47. Efficiency of the System With Unsymmetrical Loads at Output at 100 V

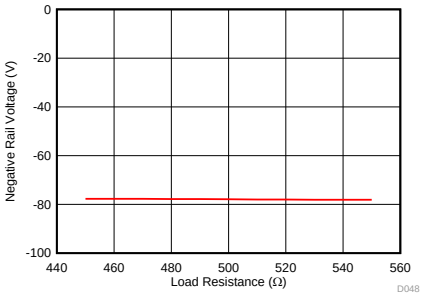


図 48. Load Mismatch at the Negative Rail at 80 V (Full Load at Positive Rail is 500 Ω)

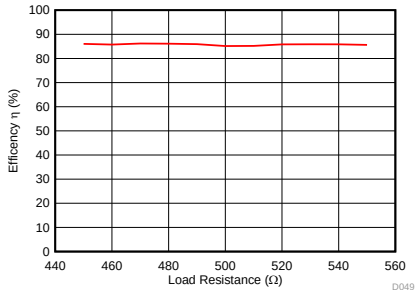


図 49. Efficiency of the System With Unsymmetrical Loads at Output at 80 V

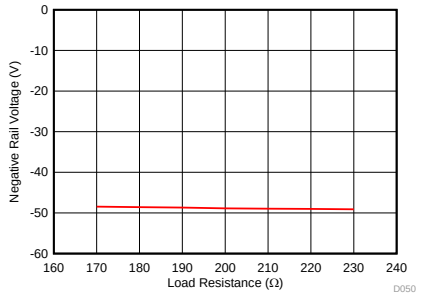


図 50. Load Mismatch at the Negative Rail at 50 V (Full Load at Positive Rail is 200 Ω)

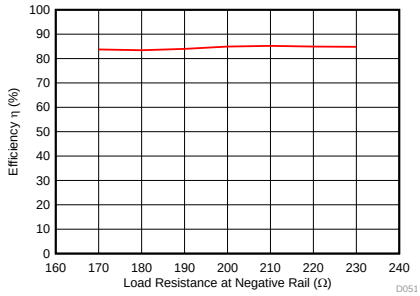


図 51. Efficiency of System With Unsymmetrical Loads at Output at 50 V

3.2.2.4 *Full Load Performance at Continuous Load*

図 52 and 図 53 show the voltage regulation with full load current and efficiency of the reference design at full load across the range of output, respectively. The total continuous power delivered is 25 W (12.5 W + 12.5 W).

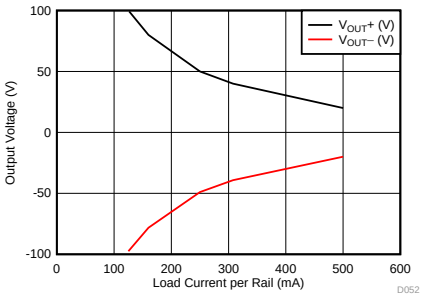


図 52. Voltage Regulation Between Both Rails With Full Load Current

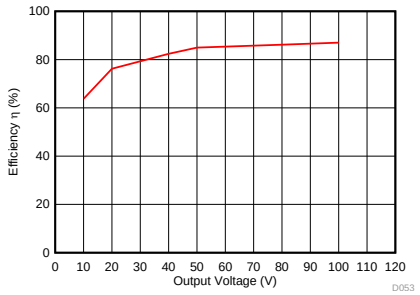


図 53. Full Load Efficiency vs Output Voltage

3.2.2.5 Voltage Ripple at Pulsed Load

The loads in ultrasound applications are typically applied for a fixed duration and then removed, as described in 3.2.1. When the switching load turns OFF and ON, there is ripple at the output voltage that must be as minimal as possible. This board is tested at a 100-V output with a switching load of 125 mA at the output. 表 3 shows the timing parameters. At V_{OUT} = 100 V, the measured value of the peak-to-peak ripple for B-Mode and Elastography Mode is 100 mV and 1.975 V, respectively. Similarly at V_{OUT} = 10 V and I_{OUT} = 300 mA, the measured value of the peak-to-peak ripple voltage for B-Mode and Elastography Mode is 107.5 mV and 2.375 V, respectively. 図 54 through 図 57 show the corresponding waveforms for both the modes at output voltages of 100 V and 10 V.

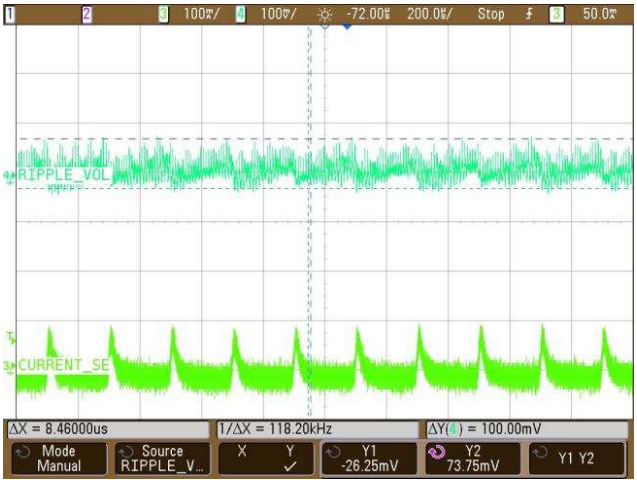


図 54. Ripple Voltage for B-Mode at V_{OUT} = 100 V, I_{OUT} = 125 mA

図 55. Ripple Voltage for Elastography Mode at V_{OUT} = 100 V, I_{OUT} = 125 mA

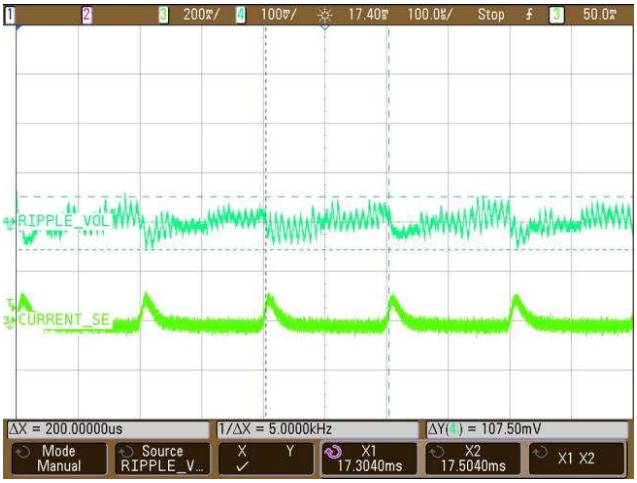


図 56. Ripple Voltage for B-Mode at V_{OUT} = 10 V, I_{OUT} = 300 mA

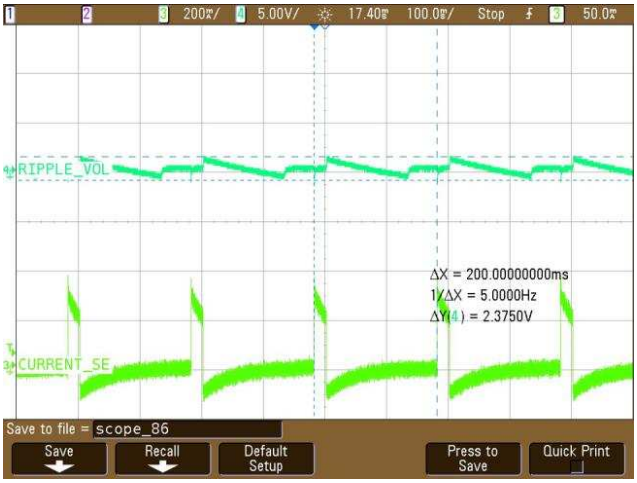


図 57. Ripple Voltage for Elastography Mode at V_{OUT} = 10 V, I_{OUT} = 300 mA

3.2.2.6 Soft Start Performance

When turning on the board, the output voltage should ramp up slowly to the desired value to protect against sudden surges that could damage the components on the board. At start-up, the output voltage increases to the set value, it overshoots by a certain amount, and then it settles at the set voltage. 図 58 and 図 59 show the waveform at the startup when the output voltages are set to 100 V and 50 V, respectively. The waveform in green show the output voltage while the waveform in pink show the gate pulse with time. The rise time for the 100 V output is 240 ms, and the rise time for the 50 V the output is 143 ms. The overshoot in the output voltage at the set voltage of 100 V is 106.77 V, while at 50 V the set voltage is 59.7 V.

図 **58. Soft Start at Set Voltage of 100 V**

図 **59. Soft Start at Set Voltage of 50 V**

3.2.2.7 Synchronizing With External Clock Signal

One of the important features of this design is that the power supply can synchronize to an external clock signal. The design is tested for such clock synchronization with an external clock signal with an amplitude of 3 V and switching frequency that varies from 150 kHz to 500 kHz. 図 60 through 図 67 show the corresponding waveforms for the external synchronization from 150 kHz to 500 kHz at the set output voltage of 50 V. The magenta waveforms show the gate drive pulse of the MOSFET at the indicated switching frequency, the blue and green waveforms show the stress on the drain (V_{DS}) of the FET device and the output voltage of 50 V, respectively.

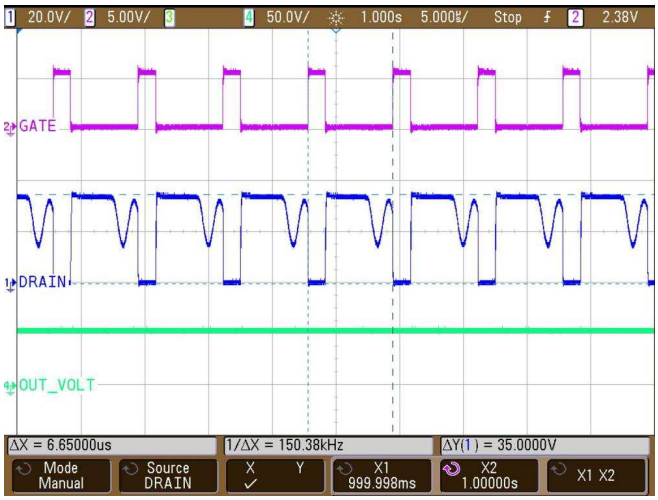


図 60. Gate, Drain, and Output Voltage Waveforms for Synchronization to 150-kHz External Clock

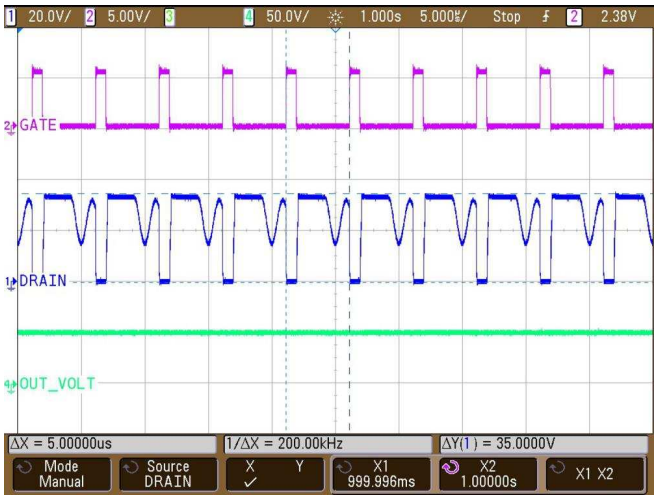


図 61. Gate, Drain, and Output Voltage Waveforms for Synchronization to 200-kHz External Clock

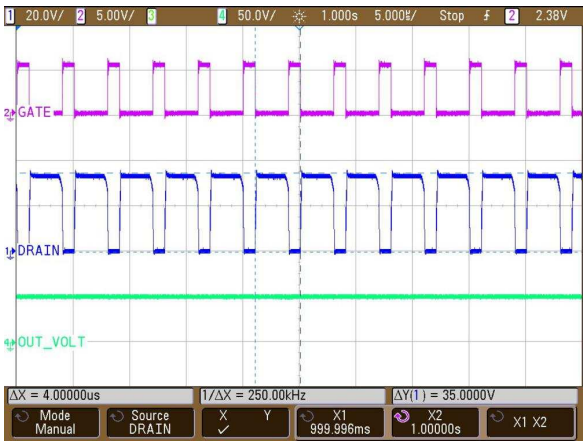


図 62. Gate, Drain, and Output Voltage Waveforms for Synchronization to 250-kHz External Clock

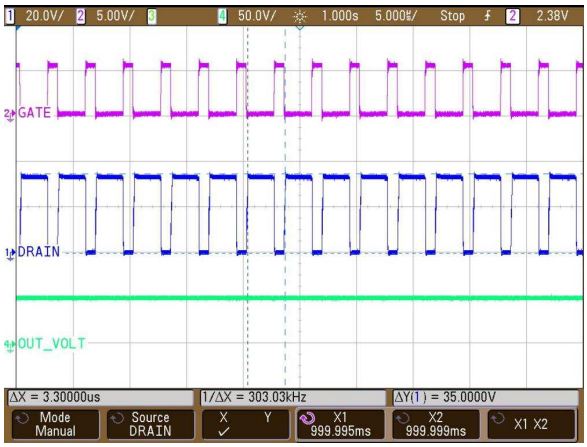


図 63. Gate, Drain, and Output Voltage Waveforms for Synchronization to 300-kHz External Clock

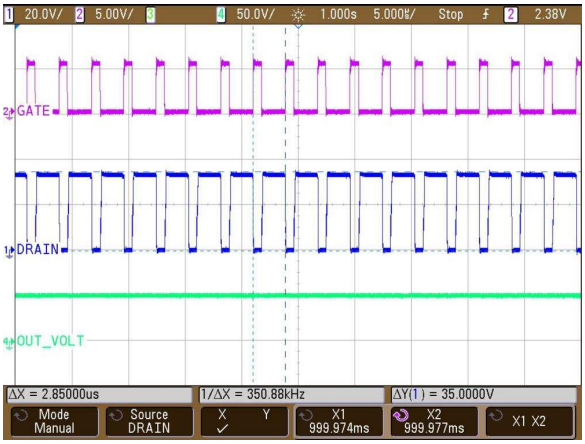


図 64. Gate, Drain, and Output Voltage Waveforms for Synchronization to 350-kHz External Clock

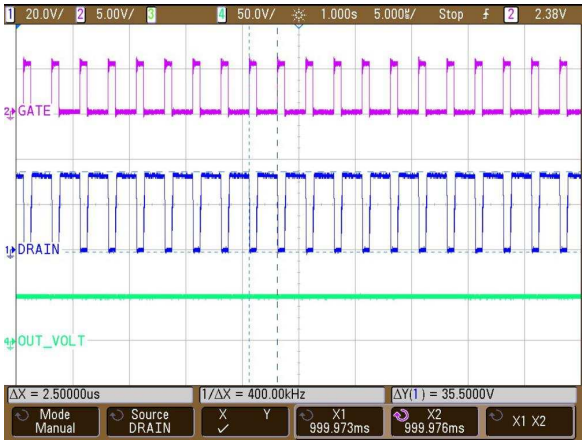


図 65. Gate, Drain, and Output Voltage Waveforms for Synchronization to 400-kHz External Clock

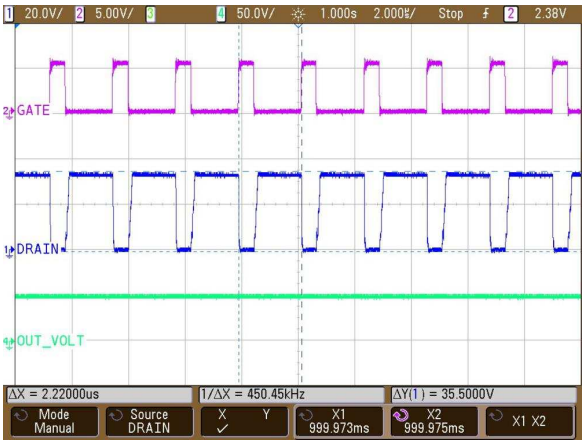


図 66. Gate, Drain, and Output Voltage Waveforms for Synchronization to 450-kHz External Clock

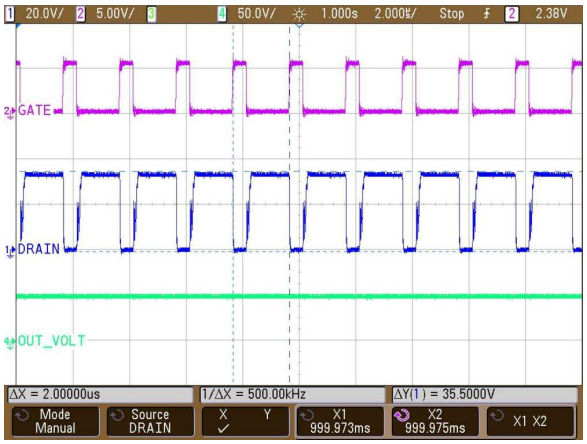
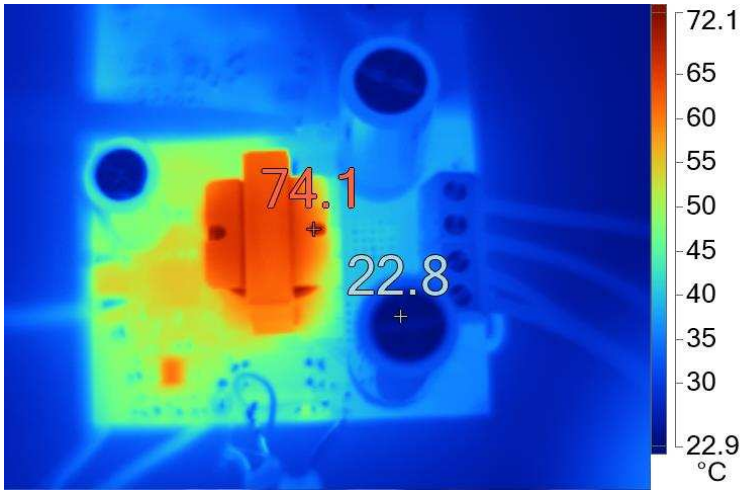


図 67. Gate, Drain, and Output Voltage Waveforms for Synchronization to 500-kHz External Clock

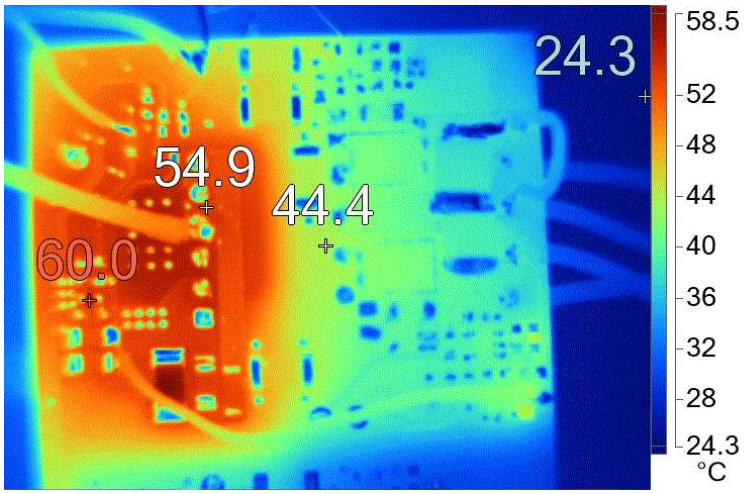
3.2.2.8 Thermal Images of the Board

図 68 and 図 69 show the thermal images of the top and bottom sections of the board at a 100-V full load condition (V_{OUT} = 100 V, I_{OUT} = 125 mA).



(1) Minimum = 22.8
(2) Average = 45.4
(3) Maximum = 74.1

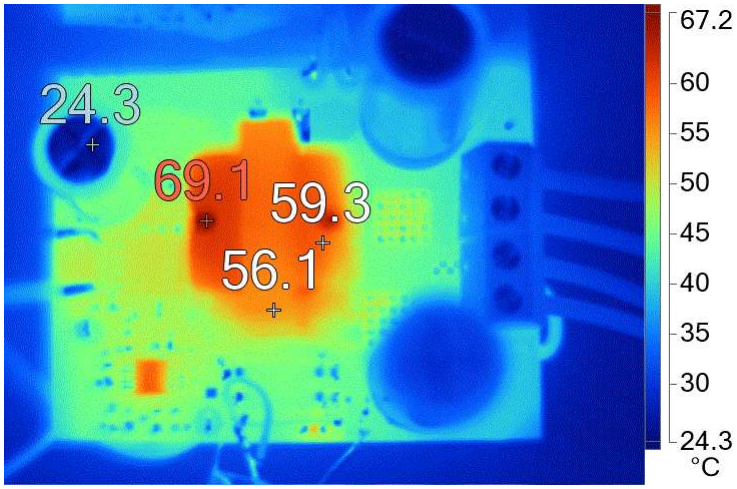
図 68. Thermal Image of the Top Section at 100-V Full Load



(1) Minimum = 25.2
(2) Average = 44.9
(3) Maximum = 60.0

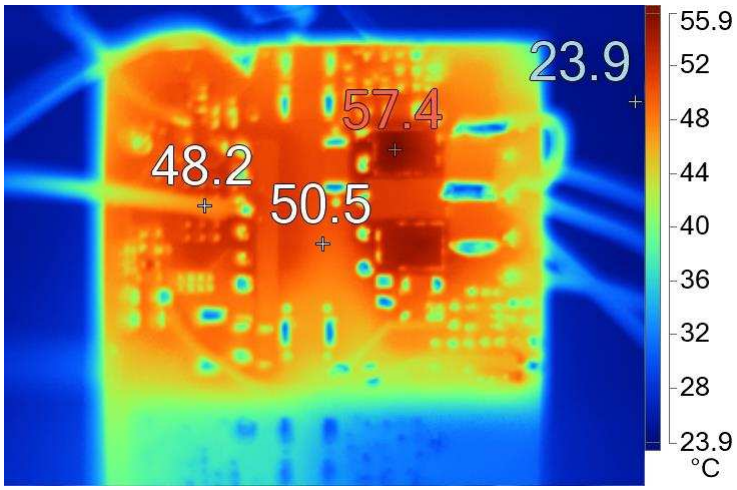
図 69. Thermal Image of the Bottom Section at 100-V Full Load

図 70 and 図 71 show the thermal images of the top and bottom sections of the board at 10 V with 300 mA of load current.



(1) Minimum = 28.7
(2) Average = 49.0
(3) Maximum = 69.1

図 70. Thermal Image of the Top Section at 10 V (300-mA Load Current)



(1) Minimum = 29.7
(2) Average = 49.4
(3) Maximum = 57.4

図 71. Thermal Image of the Bottom Section at 10 V (300-mA Load Current)

4 Design Files

4.1 Schematics

To download the schematics, see the design files listed in the reference design folder.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files listed in the reference design folder.

4.3 PCB Layout Recommendations

Find device-specific layout guidelines for each individual TI device used in this reference design in the corresponding data sheets. 図 14 and 図 15 show the top and the bottom views of the reference design PCB, respectively.

4.3.1 Ground and Power Planes

図 72 shows the ground plane on the middle layer 1 (referred to as the Ground layer) and 図 73 shows the power plane on the middle layer 2 (referred to as the Power layer) on the reference design board.

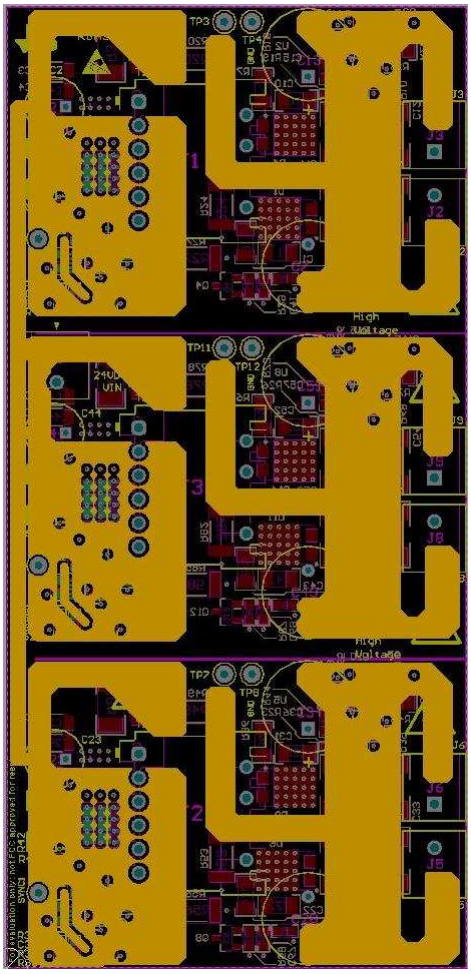


図 72. Ground Planes of the Reference Design Board

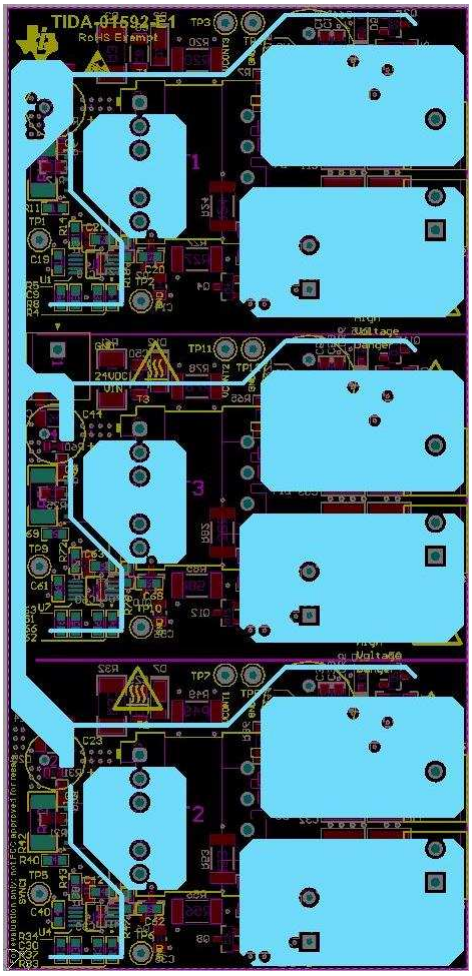
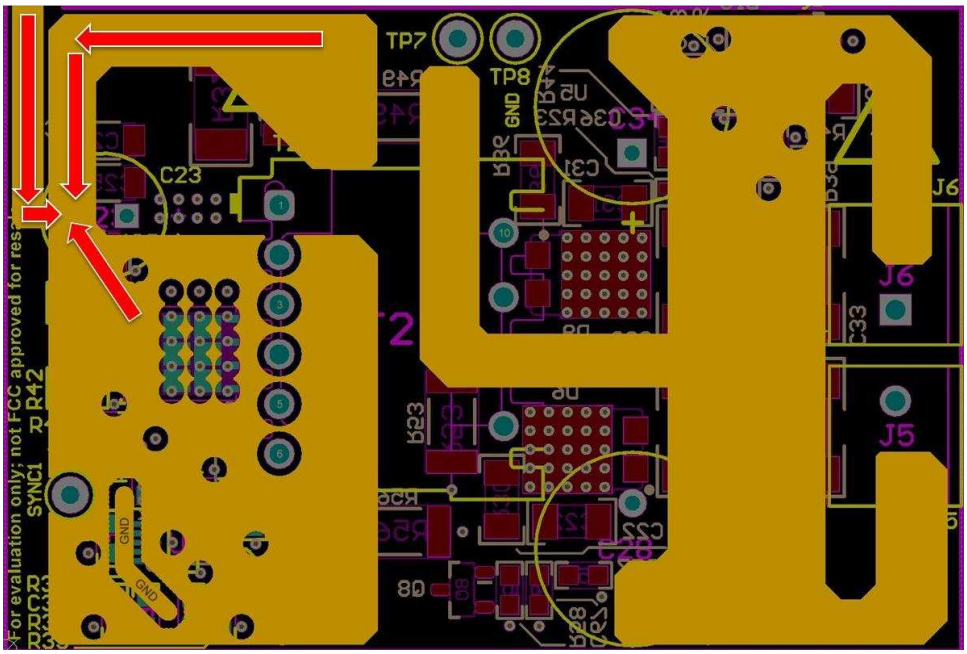


図 73. Power Planes of the Reference Design Board

4.3.2 Star Topology Ground

In any power supply design, grounding has a very critical role. Proper grounding is essential for a good power-supply design. Therefore, star topology ground is used to connect all the grounds in the design specifically power ground, analog ground, and digital ground. In star grounding, the grounds meet at a common position, which is typically the ground of the input electrolytic capacitor.

There are several signal paths that conduct fast changing currents or voltages, which can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. Therefore, the grounds are tied together at the input electrolytic ground. 図 74 shows the star topology ground where all the individual ground planes terminate at the negative terminal of the input bulk capacitor.

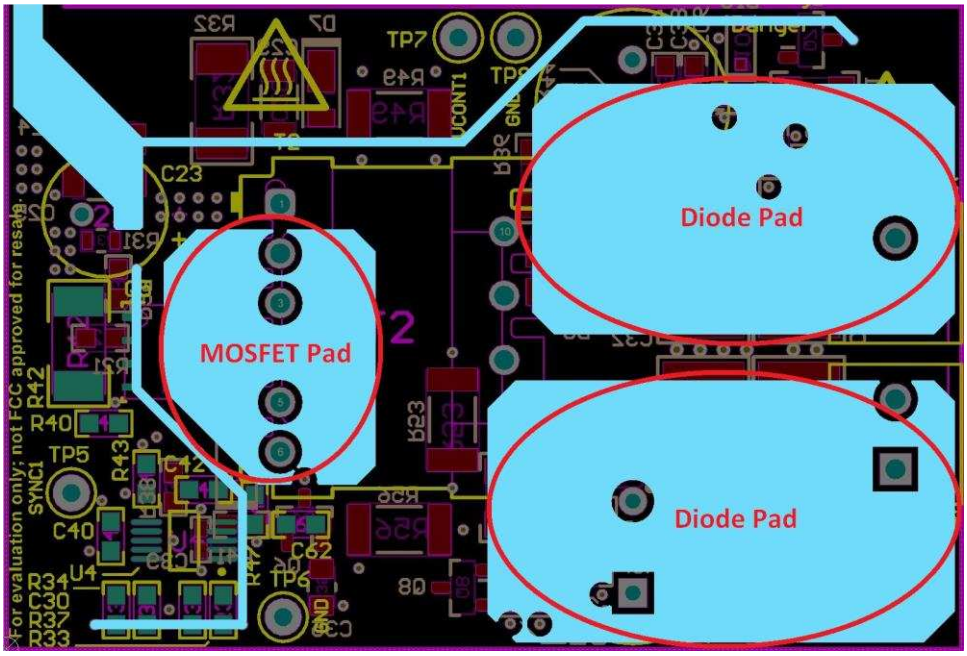


NOTE: The arrows in red point toward the star point.

図 74. Star Topology Ground for Power Supply

4.3.3 Power Dissipation Pads for FET and Diodes

There are losses involved in the switching MOSFET and the diodes in a typical power supply, which heat up the board. Efficient thermal dissipation is an absolute necessity in such designs. 図 75 shows the thermal pads that dissipate power for the FET and the diodes. These pads are highlighted with red circles.



NOTE: The red circles show the pad locations.

図 75. Thermal Pads for FET and the Output Diodes

4.3.4 Layout Prints

To download the layer plots, see the design files listed in the reference design folder.

4.4 Altium Project

To download the Altium Designer® project files, see the design files listed in the reference design folder.

4.5 Gerber Files

To download the Gerber files, see the design files listed in the reference design folder.

4.6 Assembly Drawings

To download the assembly drawings, see the design files listed in the reference design folder.

5 Related Documentation

1. Texas Instruments, *How to Design Flyback Converter With LM3481 Boost Controller Application Report*
2. Texas Instruments, *Power Topologies Handbook*
3. Texas Instruments, *LM3481/LM3481-Q1 High-Efficiency Controller for Boost, SEPIC, and Flyback DC/DC Converters Data Sheet*
4. Texas Instruments, *AN-1756 LM3481 Evaluation Board User's Guide*
5. Texas Instruments, *LM3481-FlybackEVM User's Guide*
6. Texas Instruments, *TINA-TI™ Simulation Software*

5.1 商標

6 About the Authors

ABHISHEK VISHWA is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Medical Healthcare and Fitness sector. Abhishek joined TI in July 2017. Abhishek brings to this role his experience in analog design, mixed signal design, industrial interfaces, and power supplies. Abhishek completed his B. Tech in Electrical Engineering and M. Tech in Microelectronics from IIT Bombay.

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