Design Guide: TIDA-01599

産業用ドライブ **(IEC 61800-5-2)** *向け、***TÜV** *評価済みセーフ・トルク・オフ* **(STO)** *のリファレンス・デザイン*

概要

このリファレンス・デザインは、CMOS 入力の絶縁型 IGBT ゲート・ドライバを使った三相インバータ向けセーフ・トルク・オフ (STO) サブシステムの概要を示します。この STO サブシステムは、2 チャネル構造を採用し (1oo2：1 out of 2、冗長化の目的で 2 つのうち少なくとも一方が動作)、ハードウェア障害耐性 1 (HFT = 1) を実現しています。無励磁化トリップの概念に従う実装を採用しています。デュアル STO 入力 (STO 1 および STO _2) がアクティブ LOW になった場合、6 個の絶縁型 IGBT ゲート・ドライバの 1 次側と 2 次側のそれぞれに対応する電源がロード・スイッチを通じてオフになり、モーターを制御および励磁する可能性を排除します。この STO リファレンス・デザイン (1oo2) は、TÜV SÜD による評価済みであり、全般的に SIL 3 および PL e/Cat.3 に適合しています。

リソース

TIDA-01599、TIDA-00199	デザイン・フォルダ
ISO1211、ISO5852S	プロダクト・フォルダ
TPS27S100、TPS22919	プロダクト・フォルダ
ISO5452、ISO7710	プロダクト・フォルダ
UCC21750、UCC5350	プロダクト・フォルダ
TIOS1013	プロダクト・フォルダ

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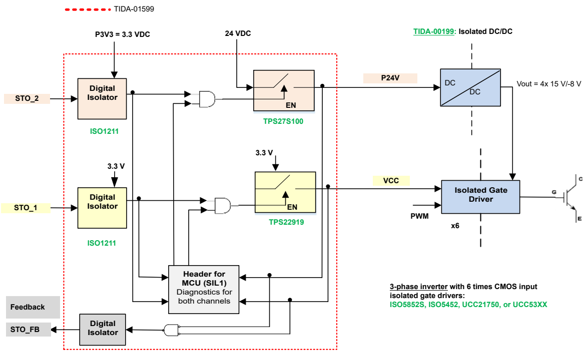
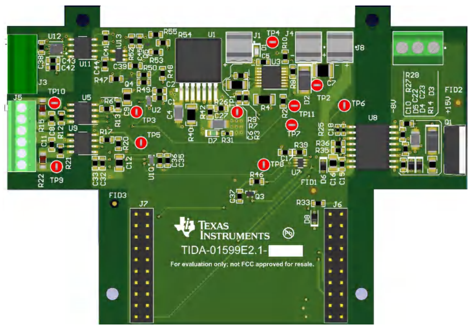
特長

- TÜV SÜD 評価済みのデュアルチャネル STO (セーフ・トルク・オフ) アーキテクチャ (1oo2)、SIL 3 (IEC 61508) および PL e/Cat.3 (ISO 13849) に適合
- STO サブシステムを実装する設計者に有益な、TÜV レポート、安全コンセプト文書、定性的システム FMEA を提供可能
- ISO5852S、UCC21750、UCC53x0 など、CMOS 入力の絶縁型 IGBT ゲート・ドライバを使った三相インバータ用のセーフ・トルク・オフ (STO) サブシステム
- 24V 絶縁型入力レシーバ ISO1211 は、IEC 61131-2 に準拠しているほか、±60V 入力を許容し、逆極性保護機能も搭載
- STO サブシステムにあるロード・スイッチの診断率 (diagnostic coverage) を確保するための MCU (SIL 1) とのインターフェイス
- RDY ピンを使用して ISO5852S ゲート・ドライバの入力および出力電源の UVLO を監視するオプション
  - アナログから PWM へ信号を変換する絶縁型センサを内蔵した UCC21750 による追加の監視機能
- 24V 絶縁 STO_FB 出力が駆動状態を通知：セーフ状態 (STO)、または通常動作

アプリケーション

- モーター・ドライブ・システム
- サーボ・ドライブの電力段モジュール
- AC ドライブの電力段モジュール
- ロボット向けサーボ・ドライブ





English Document: TIDUDS9

1 System Description

Motor drives are used in a wide range of applications, such as computer numerical control (CNC), robotics, grinders, process control, and so forth. These applications often require drive-based safety functions to reduce the risk from unexpected and hazardous movement. The integrated safety functions within a drive can replace the time-consuming and expensive installation of external safety components like mains contactors or motor contacts. In addition, electronic switching times are significantly quicker than electromechanical devices, such as contactors or relays. The integrated safety functions reduce the risk of personal damage in hazard areas and reduce installation requirements.

The *safe torque off* (STO) function is one such functional safety provision. The STO can be requested or triggered in case of a system fault. The IEC 61800-5-2 defines STO as a function that prevents torque-producing power from supplying the motor. This safety sub-function corresponds to an uncontrolled stop according to stop category 0 of IEC 60204-1. The STO safety function is also useful where power removal is required to prevent an unexpected start-up.

This STO reference design implements a dual-channel architecture (1oo2) with a hardware fault tolerance of 1 (HFT = 1) according to IEC|EN 61800-5-2. As long as a logic 1 (+24-V DC) is present at both STO inputs, the motor is operational. If there is a logic 0 (0-V DC) at one or both of the STO inputs, the corresponding power supplies to the primary and the secondary side of the six isolated IGBT gate drivers are cut through load switches. Removing the supply voltage to the gate driver IC disables the insulated-gate bipolar transistors (IGBTs) and thus the torque-producing energy.

This reference design deals with the circuit-level implementation of the two isolated STO signals to turn off the VCC1 and VCC2 supply of the isolated gate drivers with CMOS input. Monitoring has been provided at various points for diagnostics and fault detection. A microcontroller (SIL 1 MCU) is assumed to run the diagnostics of the STO hardware by monitoring the STO inputs signals as well as the diagnostic feedback signals. The MCU and the related diagnostics software are not part of this reference design. A feedback of the drive state is provided with the STO_FB signal.

This design guide validates the functionality of the design specifications through data extracted from various test results.

This STO reference design hardware architecture (1oo2) was assessed by the TUEV SUED to be generally suitable for SIL 3 and PL e | Cat. 3. A TUEV report(6), a qualitative system FMEA and system description(7) are available to further help designers implement the STO subsystem.

1.1 Key System Specifications

表 1-1. Key System Specifications

PARAMETER	VALUE	COMMENT
Safety function	STO	Safe torque off per IEC 61800-5-2
Hardware fault tolerance (HFT)	HFT = 1 (1oo2)	
IEC 61508 SIL level	SIL 3	
ISO 13849	Category 3, PL e	
Demand mode	Continuous	
SFF/DC	≥ 90% (HFT = 1)	Cat. 3 PL e, medium DC is ≥ 90%
PFH	$< 10^{-7}$	**The quantitative analysis is not part of this concept study**
STO response time	10 ms (nominal), 200 ms (maximum)	The time between active low STO and gate drive output (V_{GS}) low, which means power IGBTs are OFF. **The quantitative analysis is not part of this concept study.**
DTI (Diagnostics test interval)	100 ms (10 Hz)	**The quantitative analysis is not part of this concept study. Diagnostics runs at least 10 Hz (load switch STO_1 and load switch for STO_2).**
FRT (Fault response time)	< 200 ms	
Mission time (TM)	20 years	
STO input voltage range	24-V DC ±15% (nominal) ±60-V DC absolute maximum	
STO input logic level, valid > 2 ms	15- to 30-V DC: STO function not engaged < 10-V DC: STO function engaged	STO is active low logic input. Input is low-pass filtered to remove OSSD pulses. Valid STO is > 2 ms.
Support of OSSD test pulses	Test pulse duration < 1 ms, maximum repetition frequency 500 Hz	Added low-pass filter to remove (filter-out) the test pulses to avoid trigger STO. Diagnostics for OSSD pulses to run at 250 Hz (4-ms rate).
STO feedback (STO_FB)	24-V DC, isolated	Indicates the status of the drive (safe state or normal operation) and can be used to feedback status to a safety PLC for additional diagnostics, if desired
DC supply voltage	24-V DC ±15% (nominal)	
Isolated gate driver supply voltages	Logic supply: 3V3 to 5 V (nominal) Output supply: +15 V/–8 V (nominal)	**It is expected that the supply rails are protected to remain below the recommended maximum operating voltage of the selected isolated gate drivers**
Operating ambient temperature	–40°C to 85°C	
Interface to MCU	3.3 V I/O	See 表 3-1 to 表 3-4

2 System Overview

2.1 Block Diagram

図 2-1 shows the overall system. The system includes the TIDA-01599 reference design, a diagnostics MCU (SIL 1), which is not part of the TIDA-01599 design, an isolated DC|DC gate drive power supply TIDA-00199(1) and a three-phase IGBT power stage with CMOS input isolated gate drivers, as for example implemented with TIDA-00195(2).

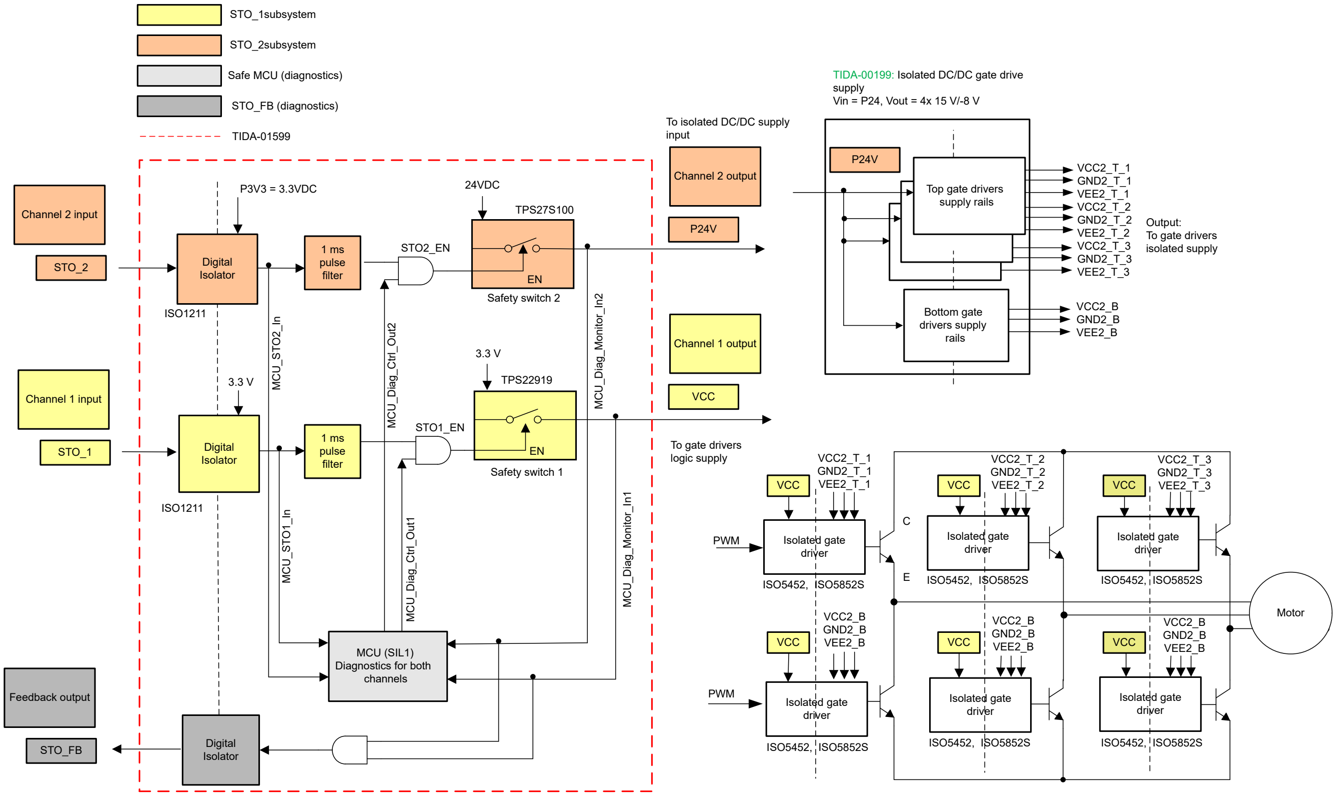


図 2-1. System Block Diagram With TIDA-01599

The TIDA-01599 reference design incorporates dual 24-V isolated inputs through ISO1211 for the STO_1 and STO_2 signals. OSSD pulses are supported through low-pass filters which should reject STO pulses of less than 1 ms. The outputs of the STO_1 and STO_2 subsystem provide the corresponding supply voltage P24V and VCC. The STO_1 and STO_2 signals control the primary (VCC) and secondary (P24-V) side power supply to the six isolated IGBT gate drivers through a power switch TPS22919 and a high-side switch TPS27S100, respectively. P24V is the 24-V input voltage to the isolated DC|DC converter TIDA-00199. The TIDA-00199 board accepts 24 V with a tolerance of ±20% and provides four isolated sets (15 V, –8 V) of bias voltages. In this design, the TIDA-00199 is used to provide the bipolar supply to the secondary side of the six isolated IGBT gate drivers. VCC is the supply voltage to the primary logic side of the six isolated gate drivers.

As long as a logic 1 (+24-V DC) is present at both STO inputs, the motor is operable. If there is a logic 0 (0 V) at one or both of the STO inputs, the power supplies to the gate drivers are disconnected and the motor coasts down to zero. The use of 1oo2 architecture helps achieve HFT = 1 and only the occurrence of two simultaneous faults can cause failure of the safety function.

An STO_FB signal is provided to indicate the status of the drive (safe state or normal operation) and can be used to feedback the status of the drive to a safety PLC for additional diagnostics, if desired.

The diagnostic signals are routed to a 3.3-V LaunchPad™ compatible interface to connect an MCU (SIL 1) such as a C2000 MCU to run the corresponding diagnostic and monitoring software. The MCU (SIL 1) and the software are not part of this design.

2.2 Design Considerations

2.2.1 Conditions of Use: Assumption

Refer to 図 2-1 for a high-level system block diagram of the safety elements, which are the STO_1 and STO_2 safety subsystems and the diagnostics software running on a MCU (SIL 1). The following list outlines the assumptions, which are out of scope with this design.

2.2.1.1 Generic Assumptions

- PCB design: The common cause failure on PCB design is out of scope for this design guide.
- Over- and undervoltage protection circuits must be assessed in the implementation of this design. Out of the scope of this activity.
- Diagnostic and any firmware must be assessed in the implementation of this design. Out of the scope of this activity.
- Common cause factors and determination of beta-factor and CCF must be assessed in the implementation of this design. Out of the scope of this activity.
- Quantitative analysis (PFH, MTTFd, and so forth) must be assessed in the implementation of this design. Out of the scope of this activity.

2.2.1.2 Specific Assumptions

- Input signals STO_1 and STO_2.

1. Input voltage is between 0-V and 24-V nominal with worst case of 3.6-V as logic low and 20.4-V as logic high. No intermediate voltage is expected.
2. The logic low (diagnostic pulse) in the STO signal is assumed either to be less than 1ms or greater than 2ms. No intermediate values are allowed.

- Diagnostic coverage of STO_1 and STO_2 and STO_FB subsystems

1. The MCU and the related diagnostic software is excluded in the analysis and is assumed to be developed in accordance with functional safety requirements. The MCU is assumed SIL 1 certified and the software implemented accordingly to meet at least SIL 1.

- Output signal STO_FB:

1. The output voltage is assumed to be between 0-V and 24-V nominal with worst case of 3.6-V as logic low and 20.4-V as logic high. The external supply voltage to the 24V STO_FB is assumed to be protected against over-voltage and is required to remain within 24V ±20% tolerance.

- Power supply rails of STO_1 and STO_2 subsystem

1. P3V3 supply: Assumed to be protected against fault, remains within ±20% tolerance (3.9 V maximum, 2.7 V minimum. If out of spec, it will be shut down to 0V. When a single protected power supply is used for both STO_1 and STO_2 subsystems, it shall employ two independent protection circuits (HFT = 1).
2. 24-V supply: The 24V input supply for the P24V is assumed to be protected against fault and remains within ±20% tolerance. If out of spec, it will be shut down to 0V.

- Isolated gate drive supply TIDA-00199

1. It is assumed that the quad output rails (VCC2 = +15 V, VEE2 = –8 V) decay to 0 V within less than 10 ms, after the P24V DC input voltage was disconnected.
2. It is assumed that all faults with TIDA-00199 are safe and yield to a 0V output voltage for all quad output rails VCC2 and VEE2.

- Temperature

1. It is assumed the components operate within the recommended operating temperature range. A temperature sensor is required to be added and if the ambient temperature is outside the recommended operating range all safety relevant supplies will be shutdown. This circuit is not part of this design.

2.2.2 Diagnostics Coverage

2.2.2.1 Dual-Channel Monitoring

The STO function is realized through dual channels STO_1 and STO_2, respectively, to de-energized the power to the gate driver (See 図 2-2). In a safety unit, if one of the STO signals is removed, then the status changes to *STO triggered* (See 表 2-1). The unit then waits for a fixed amount of monitoring time to check if both inputs are switched off. If the same signal is not present on both the inputs after the session, then the system signals an error. The PLC performs the monitoring by periodically checking the two stop paths for errors through 1-ms OSSD pulses (See 表 2-2).

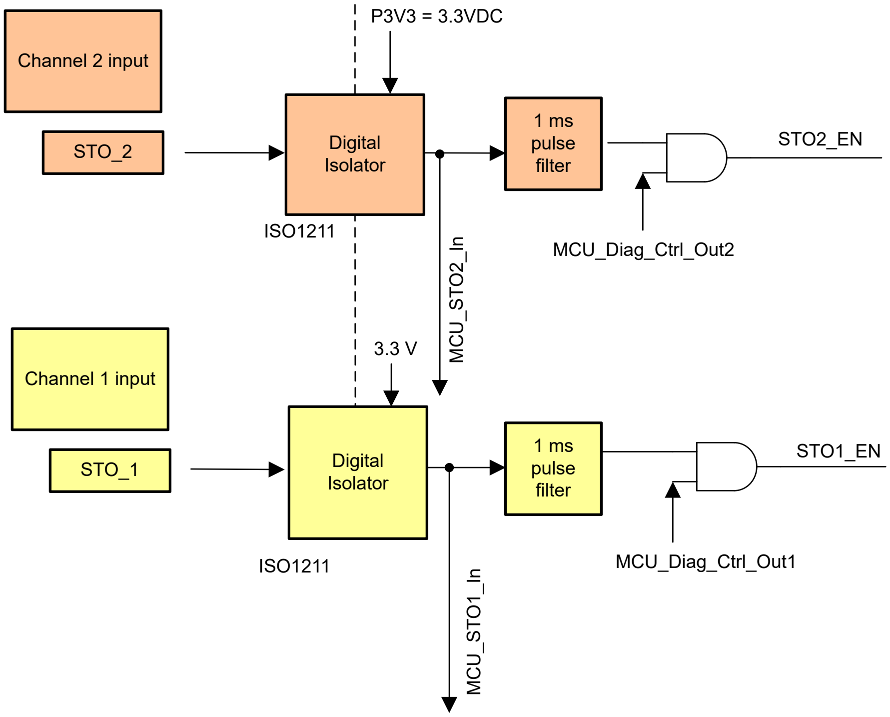


図 2-2. Dual-Channel Isolated STO

表 2-1. Dual-Channel Isolated STO

STO_1	STO_2	DESCRIPTION OF STATE
0	0	STO state is triggered and there is no error in STO function
0	1	STO state is triggered and monitoring for error starts. After some time, error is signaled
1	0	STO state is triggered and monitoring for error starts. After some time, error is signaled
1	1	STO state not triggered

In the TIDA-01599, an MCU (SIL 1) is assumed to do the diagnostic coverage. The MCU is not part of the analysis. A hardware based diagnostic coverage is possible too. 表 2-2 shows the diagnostic logic and state. Note that STO related signals are active low.

表 2-2. MCU Diagnostics Logic Table

STO_1 | STO_2	MCU_STO_1_in | MCU_STO_2_in	MCU DIAGNOSTICS : FAULT DETECTED	MCU_Diag_Cntrl_Out1 | MCU_Diag_Cntrl_Out2	IGBT GATE DRIVER OUTPUT	STATE
1 | 1	1 | 1	No	Normal operation	Normal operation	Normal operation
1 | 1	1 | 1	Yes (for example, Load switch stuck high)	0	0	Safe state
1 | 1	1 | 1	Yes (for example, No OSSD pulse)	0	0	Safe state
0 | 0	0 | 1	Yes (for example, ISO1211 stuck high)	0	0	Safe state
0 | 0	1 | 0	Yes (for example, ISO1211 stuck high)	0	0	Safe state
0 | 0	0 | 0	No	0	0	STO

2.2.2.2 Checking ISO1211 Functionality With MCU (SIL1)

As previously addressed, the PLC sends OSSD test pulses with 1-ms logic low to the input of the ISO1211 device. The signals MCU_STO1_In and MCU_STO2_In from the corresponding ISO1211 outputs are periodically monitored to ensure that the digital isolator is functioning properly. If no logic low is detected for more than 4 ms, the MCU concludes the corresponding ISO1211 output is stuck high or shorted to VCC and puts the 3-phase IGBT inverter into a safe state by driving both diagnostic pulses MCU_Diag_Ctrl_Out1 and MCU_Diag_Ctrl_Out2 continuously low. This in turns will disable the six gate drivers, the six IGBT will be turned off and the drive will enter the safe state.

2.2.2.3 Checking TPS22919 Functionality With MCU (SIL1)

For diagnostic purposes, the MCU interface periodically sends 200-µs pulses MCU_Diag_Ctrl_Out1 with logic low. The output of the switch is connected to the GPIOs of the MCU (Monitor_1) and the STO_FB subsystem as STO_1_FB input, as 図 2-3 shows.

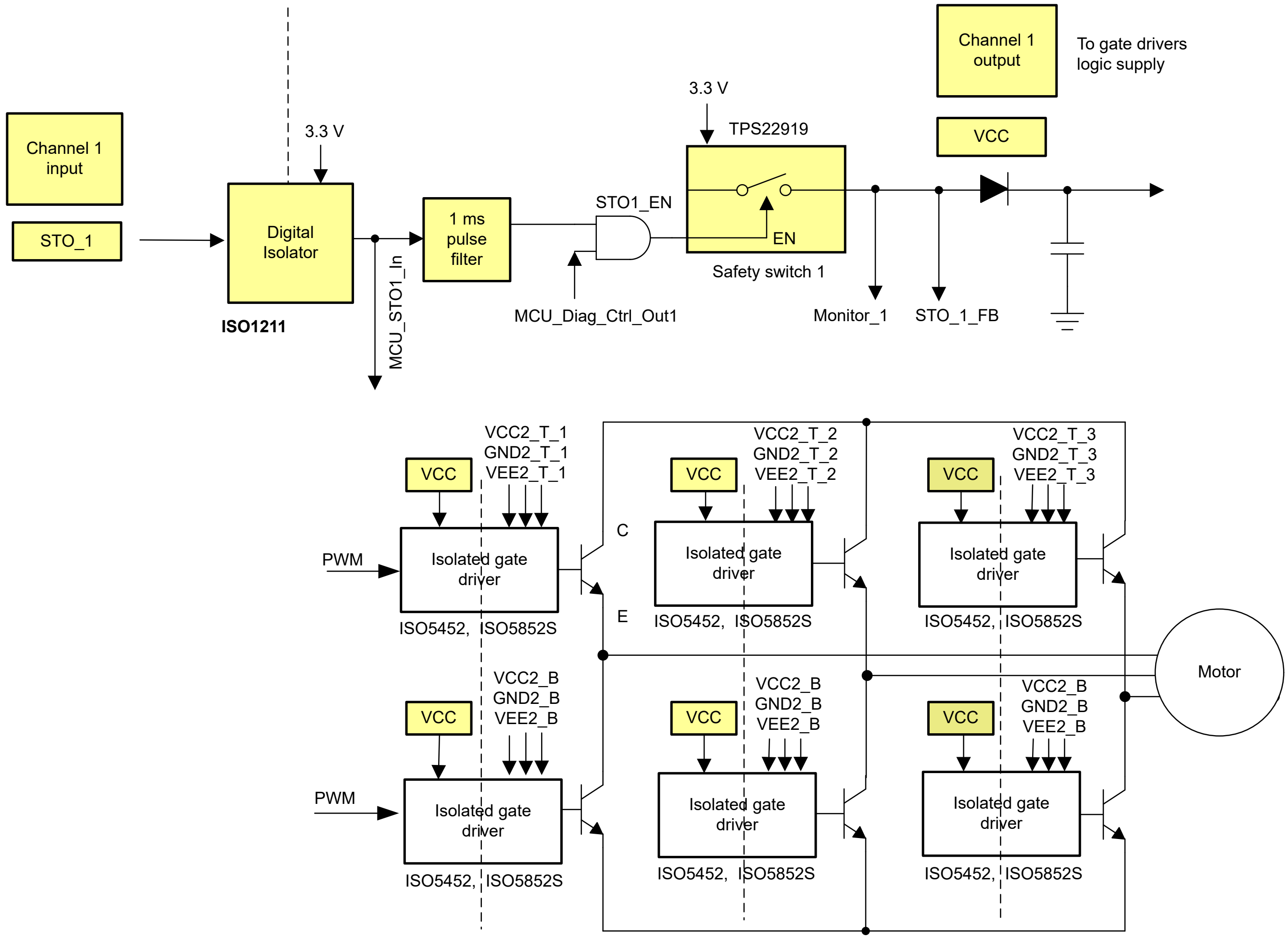


図 2-3. STO_1 Signal Flow Path

The gate driver not power off during these periodic pulses. A 0.47-µF capacitor is used to hold the 3.3-V primary supply voltage. Monitor_1 represents the status of the TPS22919 switch which is fed back to the MCU. If a short or stuck high was found, the MCU puts the 3-phase IGBT inverter into a safe state by driving both diagnostic pulses MCU_Diag_Ctrl_Out1 and MCU_Diag_Ctrl_Out2 continuously low. This in turns will disable the six gate drivers, the six IGBT will be turned off and the drive will enter the safe state.

Moreover, STO_1_FB is an active low signal and indicates the load switch state which works with the other channel STO_2_FB together to indicate the drive state. This state can be used for example by an external safety PLC to recognize a single fault in either STO_1 or STO_2 systems and take appropriate actions. The safety PLC and related action are out of scope for this reference design.

2.2.2.4 Checking TPS27S100 Functionality With MCU (SIL1)

The MCU interface periodically sends 200-µs pulses MCU_Diag_Ctrl_Out2 with logic low for diagnostic purposes. The output of the switch is connected to the general-purpose input/outputs (GPIOS) of the MCU (Monitor_2), as 図 2-4 shows by using a resistor divide network. And also connect to the STO_FB subsystem as STO_2_FB input.

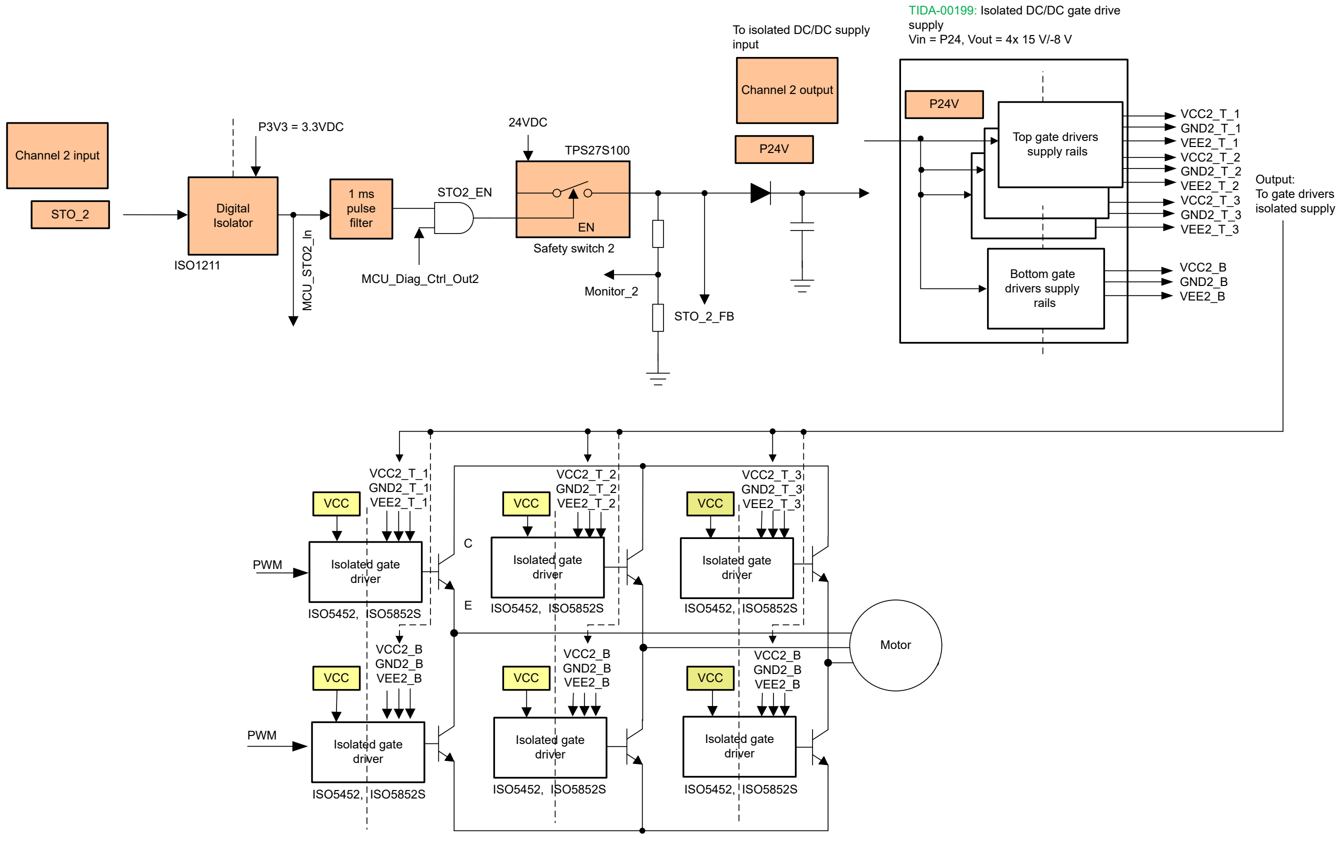


图 2-4. STO_2 Signal Flow Path

The gate driver does not power off during these periodic pulses. This reference design uses a 20-µF capacitor to hold the 24-V secondary supply voltage. The TPS27S100 switch provides full diagnostics by accurately monitoring the output current. The output current is translated into volume, which is then fed back to the MCU, this feature enables intelligent control of the load. If a short or stuck high was found, the MCU puts the 3-phase IGBT inverter into a safe state by driving both diagnostic pulses MCU_Diag_Ctrl_Out1 and MCU_Diag_Ctrl_Out2 continuously low. This in turn disables the six gate drivers, the six IGBT will be turned off and the drive will enter the safe state.

Moreover, STO_2_FB is an active low signal and indicates the load switch state which works with the other channel STO_1_FB together to indicate the drive state. This state can be used for example by an external safety PLC to recognize a single fault in either STO_1 or STO_2 systems and take appropriate actions. The safety PLC and related action are out of scope for this reference design.

2.2.2.5 Optional Monitoring Using RDY Pin of ISO5452, ISO5852S or UCC21750 Integrated Analog-to-PWM Isolated Sensor

The I/O circuitry of the ISO5452, ISO5852S device interfaces with an MCU and consists of gate drive control (IN+/IN–) inputs, RESET (RST) input, READT (RDY) alarm output, and FAULT (FLT) alarm output. The output of the gate driver turns off if the VCC1 supply drops below VIT – (UVLO1), irrespective of IN+, IN – , and RST inputs, until VCC1 rises above VIT+ (UVLO1). In a similar manner, the output of the gate driver is turns off if the VCC2 supply drops below VIT – (UVLO2), irrespective of IN+, IN –, and RST inputs, until VCC2 rises above VIT+ (UVLO2).

The ready (RDY) pin indicates the status of the UVLO internal protection feature for the input and output sides. If either side of the device has an insufficient supply (VCC1 or VCC2), the RDY pin output goes low; otherwise, the RDY pin output is high.

In addition to the RDY pin, the UCC21750 features an isolated analog to PWM signal function from AIN to APWM pin, which allows additional system monitoring for example isolated temperature sensing, high voltage dc bus voltage sensing, and so forth.

2.2.3 Drive State

The safe-state is triggered by the following events:

1. Active low STO_1 input signal requesting safe torque off
2. Active low STO_2 input signal requesting safe torque off
3. Diagnostic coverage of STO_1 or STO_B subsystems (ISO1211 and corresponding load switches) detects a dangerous fault
4. Safe power supply voltages P24V, P3V3 or the corresponding logic supply voltages of the STO_1 and STO_2 subsystem are cutoff

Drive State Feedback STO_FB Subsystem

The STO_FB signal is an active low signal and indicates the drive state. A high signal (logic level 1) indicates normal drive operation, while a low signal (logic state 0) indicates the drive is in the safe state. The schematic is shown in 図 2-5. The output signals STO_1_FB and STO_2_FB of the corresponding STO_1 and STO_2 safe subsystems are logically combined to a single active low feedback signal STO_FB through an isolated 24-V digital output. The corresponding logic states are shown in 表 2-3.

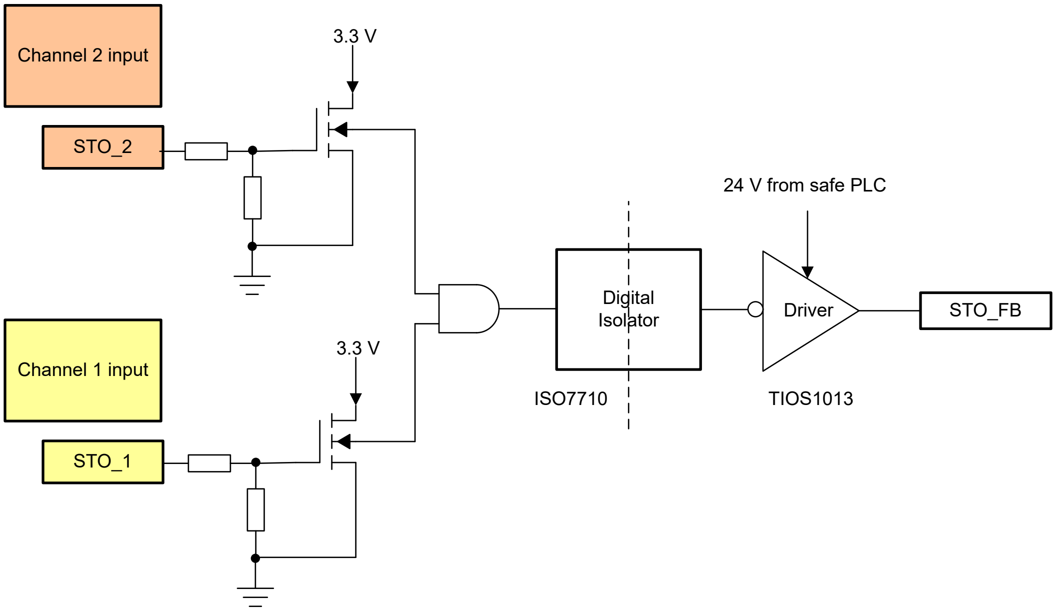


図 2-5. STO_FB Feedback Monitor Subsystem

表 2-3. STO Feedback Diagnostics Logic Table

INPUT 1: STO_1	INPUT 2: STO_2	OUTPUT 1: STO_1_FB	OUTPUT 2: STO_2_FB	DRIVE STATE	STO_FB	COMMENT
1	1	1	1	Normal operation	1	
0	0	0	0	Safe state (off)	0	
1	1	0	1 (stuck high fault)	Safe state (off)	0	(1) The MCU has detected a single dangerous fault (stuck high) in subsystem STO_2 and has triggered the safe state through STO_1 subsystem.
1	1	1 (stuck high fault)	0	Safe state (off)	0	(2) The MCU has detected a single dangerous fault (stuck high) in subsystem STO_1 and has triggered the safe state through STO_2 subsystem.
0	0	0	1	Safe state (off)	0	Single detected fault could be detected earlier already, see (1) in above row.
0	0	1 (stuck high fault)	0	Safe state (off)	0	Single detected fault could be detected earlier already, see (2) in above row.
0	0	1 (stuck high fault)	1 (stuck high fault)	Normal operation	1	Dangerous state, due to two dangerous faults, one in each safe subsystem STO_1 and STO_2. *Note: The system is designed for single fault tolerance (HFT=1), but not two faults, one in each in each subsystem.*

The STO_FB signal can be active low (logic state 0), while both STO_1 and STO_2 are inactive high (logic state 1). This state occurs when the diagnostics MCU (SIL 1) detects a single dangerous fault in one of the STO_1 or STO_2 subsystems. If a short or stuck high was found, the MCU puts the 3-phase IGBT inverter into a safe state by driving both diagnostic pulses MCU_Diag_Ctrl_Out1 and MCU_Diag_Ctrl_Out2 continuously low. This state can be used for example by an external safety PLC to recognize a single fault in either STO_1 or STO_2 systems and take appropriate actions. The safety PLC and related action are out of scope for this design.

2.3 Highlighted Products

2.3.1 ISO1211

図 2-6 shows the pin diagram of the ISO1211. The ISO1211 devices are isolated, 24- to 60-V digital input receivers These receivers are compliant to IEC 61131-2 Type 1, 2, and 3 characteristics and suitable for programmable logic Controllers (PLCs) and motor-control digital input modules. Unlike traditional optocoupler solutions with discount, impair current-limiting circuit, the ISO121x devices provide a simple, low-power solution with an accurate current limit to enable the design of compact and high-density I/O modules. These devices do not require field-side power.

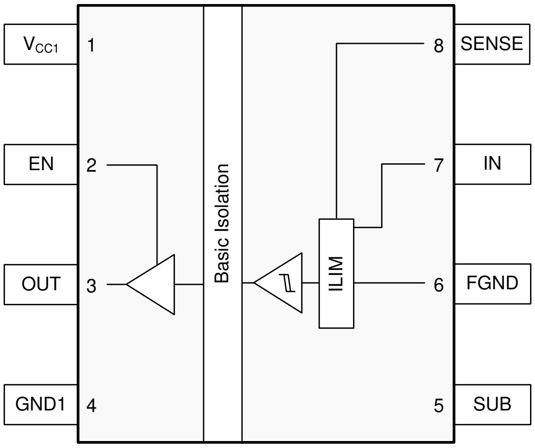


図 2-6. ISO1211 Pin Diagram

2.3.2 TPS27S100

図 2-7 shows the TPS27S100 functional block diagram. The TPS27S100 is a single-channel, fully-protected, high-side switch with an integrated NMOS and charge pump. An adjustable current-limit function greatly improves the reliability of the whole system. The device diagnostic reporting has two versions to support both digital fault status and analog current monitor output. Accurate current monitor and adjustable current limit features differentiate this device from alternatives in the market.

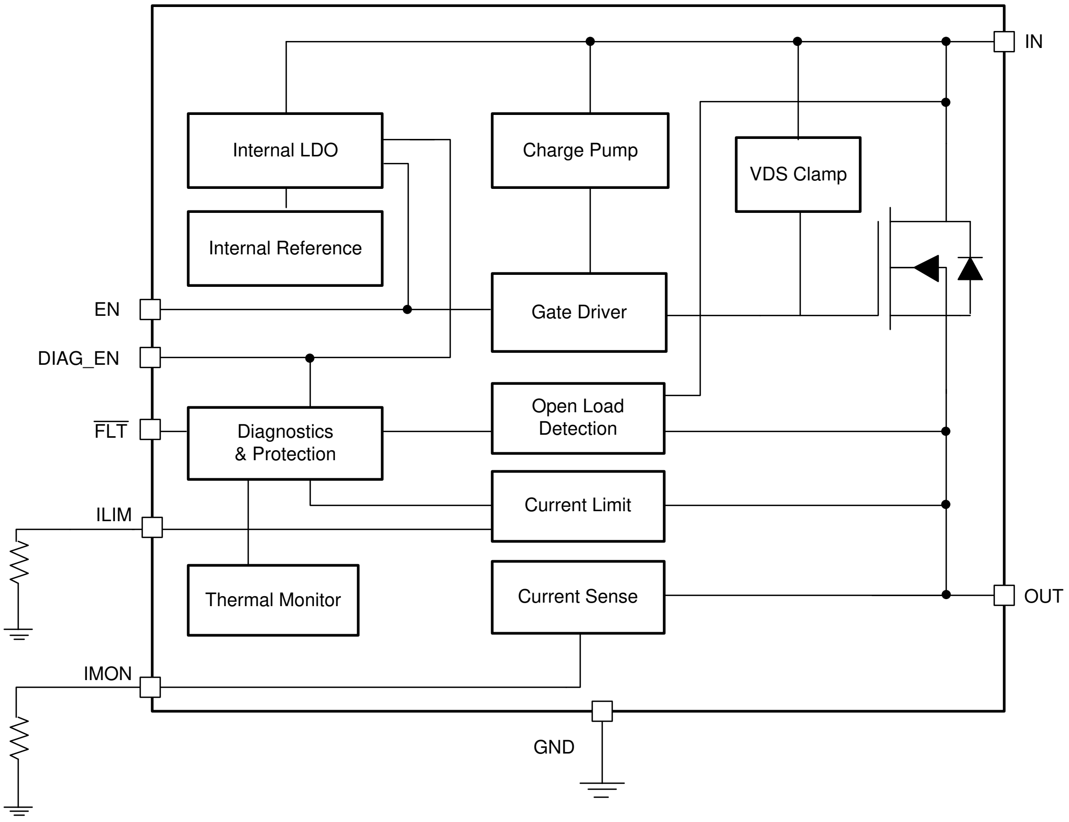


図 2-7. TPS27S100 Functional Block Diagram

2.3.3 TPS22919

図 2-8 shows the TPS22919 functional block diagram. The TPS22919 is a small, single channel load switch with controlled slew rate. The device can support a maximum continuous current of 1.5 A with short-circuit protection. The switch is controlled by an ON and OFF input (ON pin), which is capable of interfacing directly with low-voltage control signals.

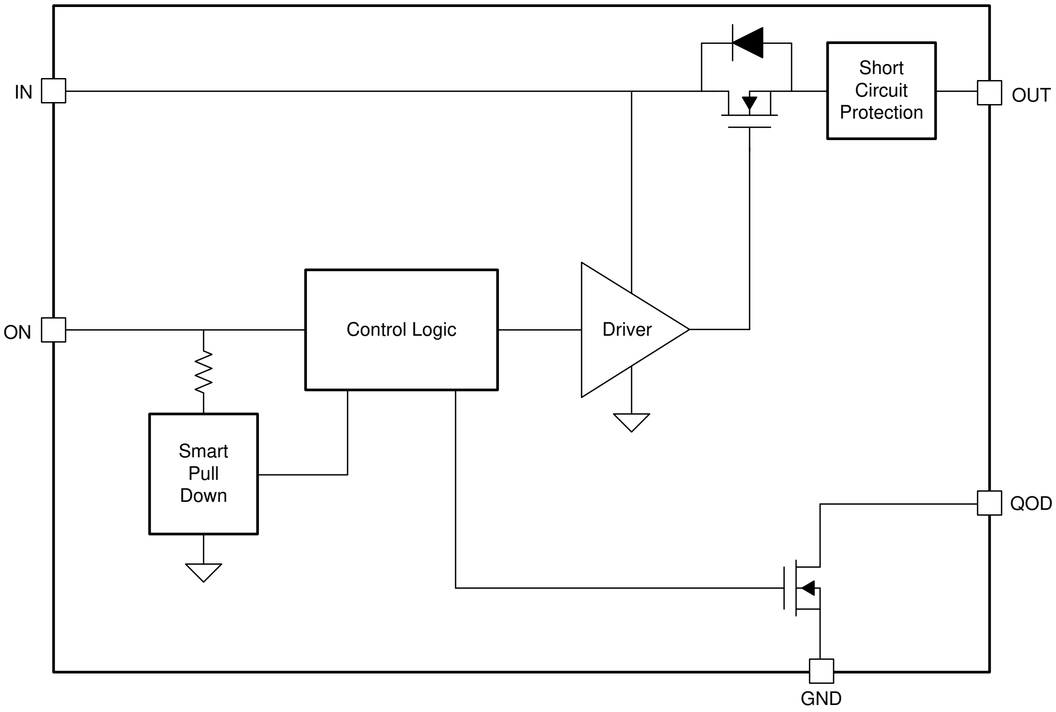


図 2-8. TPS22919 Functional Block Diagram

2.3.4 ISO5852S, ISO5452

The ISO5852S and ISO5452 are isolated smart gate driver for IGBTs and MOSFETs. The input CMOS logic and output power stage are separated by a silicon dioxide (SiO_2) capacitive isolation. 図 2-9 shows the functional block diagram.

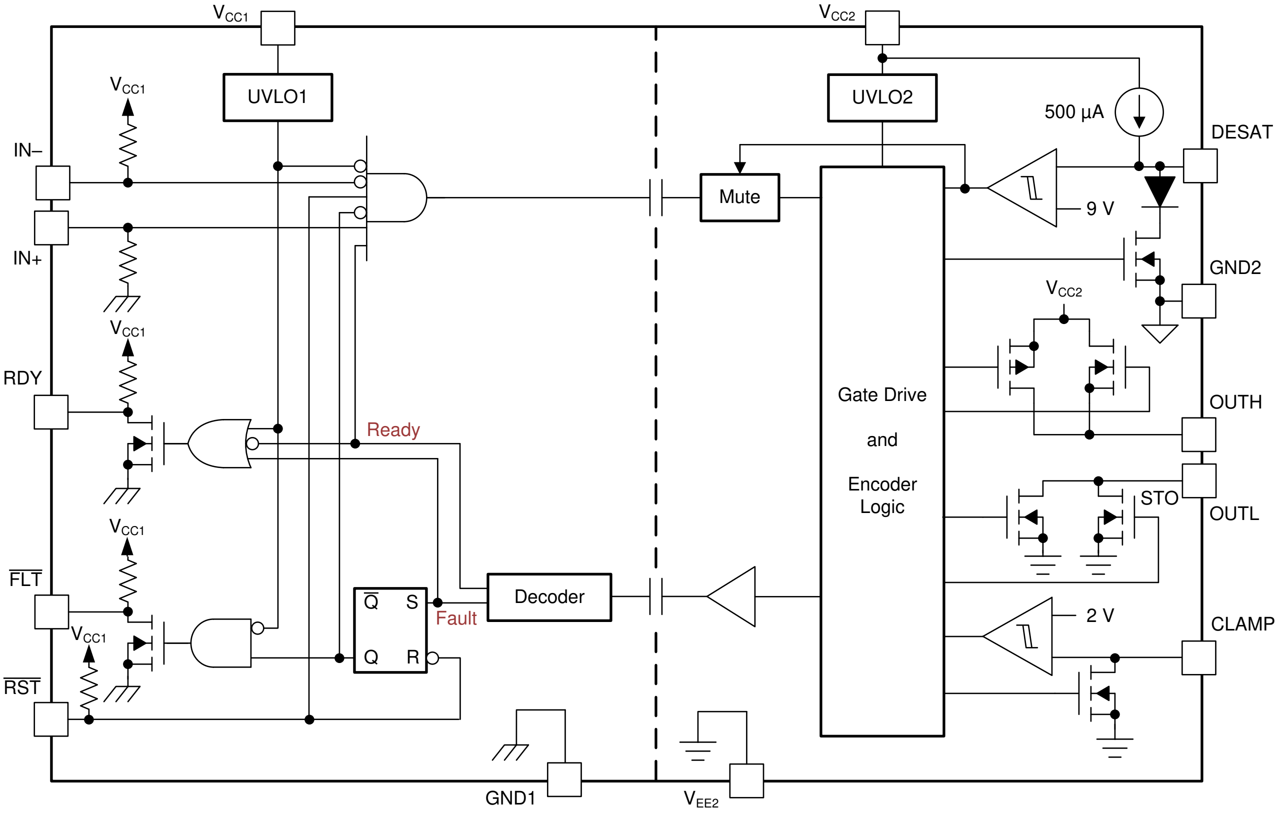


図 2-9. ISO5852S, ISO5452 Functional Block Diagram

The I/O circuit on the input side interfaces with an MCU and consists of gate drive control (IN+|IN–) inputs, RESET (RST) input, READY (RDY) alarm output, and FAULT (FLT) alarm output. The power stage consists of power transistors which supply 2.5-A pullup and 5-A pulldown currents to drive the capacitive load of the external power transactions, as Well as the DESAT detection circuit to monitor the IGBT for collector-emitter overvoltage during short-circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier and receive the circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5852S, ISO5452 also contains undervoltage lockout (UVLO) circuitry to prevent insufficient gate drive to the external IGBT. Additionally, it offers an active output pulldown feature, which ensures that the gate-driver Output is held low if the output supply voltage is absent. The ISO5852S, ISO5452 also has an active Miller clamp function which can be used to prevent parasitic turn-on of the external power transistor, due to the Miller effect, for unipolar supply operation.

2.4 System Design Theory

2.4.1 Digital Input Receiver for STO

The ISO1211 receives 24-V digital signals and provides isolated digital outputs, without the requirement of a field-side power supply. External resists on the input signal path (R12 and R21) precisely set the limit for the current drawn from the field input. This current limit helps to minimize the power dissipated in the system. The current limit can be set for Type 1, 2, or 3 operation. The voltage transition thresholds are compliant with Type 1, 2, and 3 and can be increased further using an external resistor, R22 and R15. These two resistors are carbon MELF (pulse-proof) type used to prevent surge. For detailed test results, see the *How to Design Isolated Digital Input Modules for Surge Immunity* application brief.

図 2-10 shows a schematic of the ISO1211 receivers.

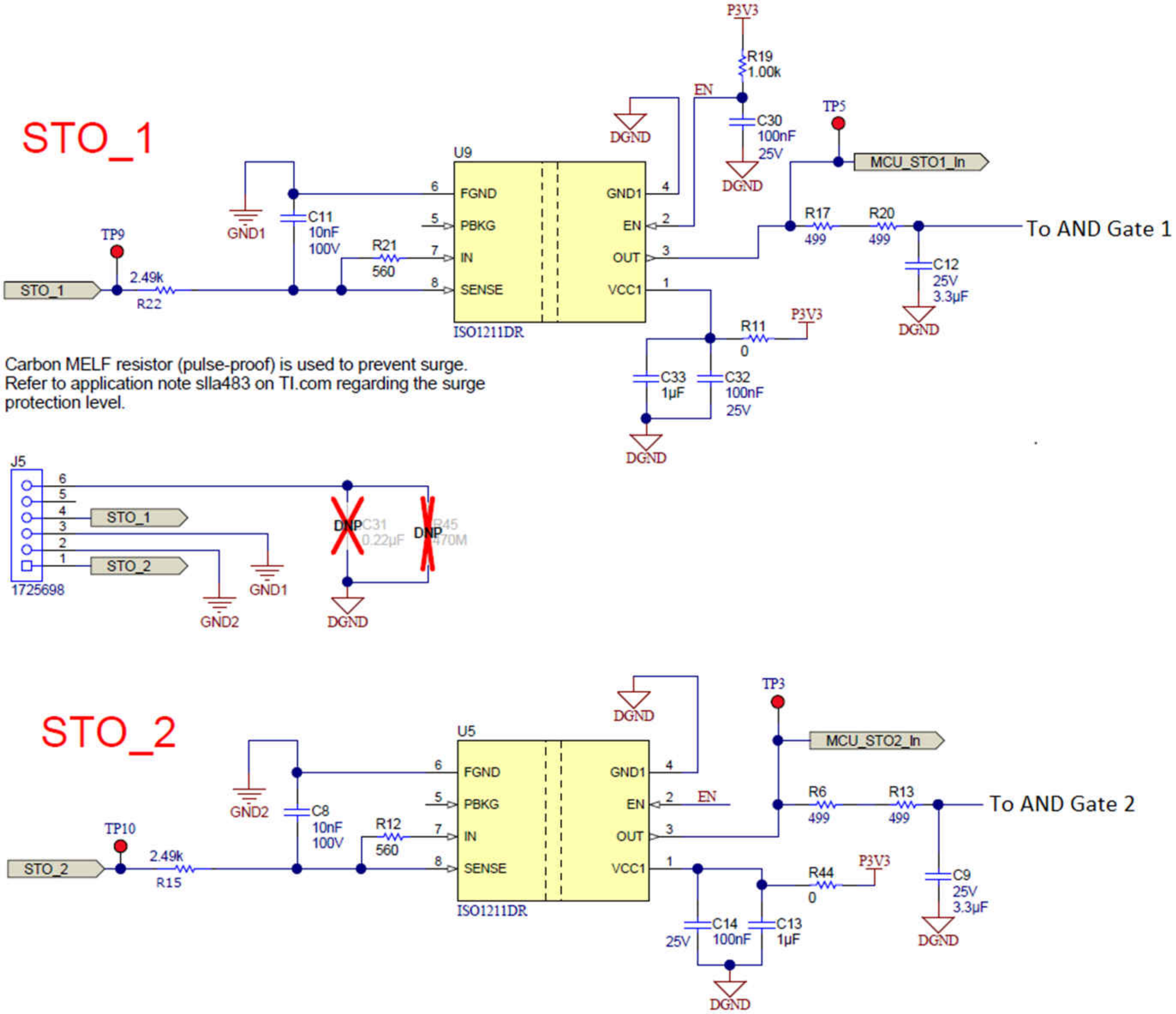


図 2-10. ISO1211 Schematic

English Document: TIDUDS9

As per the specifications of the design, the voltage limits defined for an input voltage of 24 V is as follows:

1. 15- to 30-V DC: STO function not engaged (motion allowed)
2. 0- to 5-V DC: STO function engaged (motion inhibited)

These design requirements comply with Type 1 characteristics.

As 図 2-10 shows, Type 1 operation uses a value of 560 Ω for R12 and R21 and results in a current limit of 2.25 mA (typical). The relationship between the R_{SENSE} resistor and the typical current limit (I_L) is given by 式 1.

$$I_L = \frac{2.25\ \text{mA} \times 562\ \Omega}{R_{SENSE}} = \frac{2.25\ \text{mA} \times 562\ \Omega}{560\ \Omega} = 2.25\ \text{mA} \tag{1}$$

Resistors R22 and R15 set the voltage thresholds (V_{IH} and V_{IL}) in addition to limiting the surge current. Use a resistor of 2.5 kΩ for R22 and R15 for a Type 1 system. 式 2 and 式 3 are used to calculate the typical V_{IH} and V_{IL} values, respectively.

$$V_{IH(TYPICAL)} = 8.25\ V + R22 \times \frac{2.25\ mA \times 562\ \Omega}{R21} = 8.25\ V + 2.5\ k\Omega \times \frac{2.25\ mA \times 562\ \Omega}{560\ \Omega} = 13.875\ V \tag{2}$$

$$V_{IL(TYPICAL)} = 7.1\ V + R22 \times \frac{2.25\ mA \times 562\ \Omega}{R21} = 7.1\ V + 2.5\ k\Omega \times \frac{2.25\ mA \times 562\ \Omega}{560\ \Omega} = 12.725\ V \tag{3}$$

Note that the specific assumption of input signals STO_1 and STO_2 is that the input voltage is between 0-V and 24-V nominal with worst case of 3.6-V as logic low and 20.4-V as logic high. Logic high range is 24-V DC ±15% (nominal) with ±60-V DC absolute maximum. No intermediate voltage is expected.

As per the design specifications, low STO pulses that are less than 1 ms are rejected. Address this rejection by placing a low-pass filter at the output signals of the ISO1211 device. To meet the design requirements, place an RC combination with R = 1 k and C = 3.3 μF (see 式 4).

$$\text{Time Constant} = R \times C = 1\,K \times 3.3\ \mu F = 3.3\ \mu sec \tag{4}$$

The cutoff frequency of this filter is 48 Hz, where:

- V(t) = 3.3
- At t = 1 ms
- V(t) = 2.8 V, which is within the logic threshold high range of the AND gate.

For implementation, use 2 × 499 Ω R17 and R20 in series for STO 1 and use 2 × 499 Ω R6 and R13 in series for STO 2. This is to get rid of the short or change value failure mode of resistor which will bypass the filter for logic gate input.

2.4.2 STO_1 Signal Flow Path for Controlling VCC1

The TPS22919 is a small, ultra-low leakage current, single-channel load switch. 図 2-11 shows the schematic design of the TPS22860.

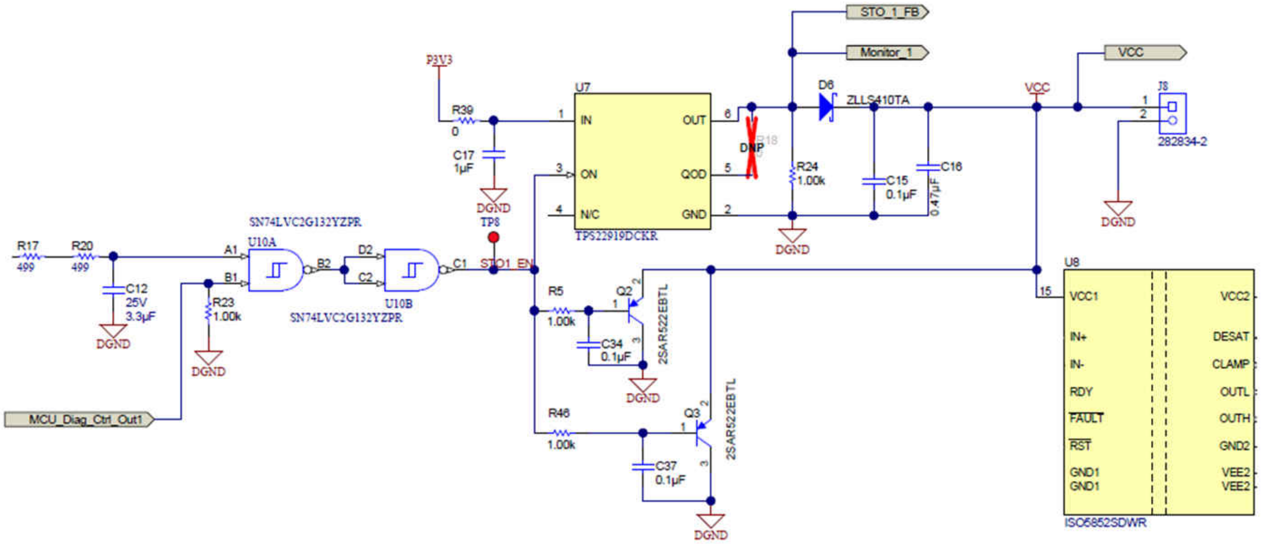


図 2-11. TPS22919 Schematic

The device power supply is 3.3 V which is assumed to be protected against fault and remains within ±20% tolerance. To limit the voltage drop on the input supply, which is caused by transient inrush currents when the switch turns on into a discharged load capacitor, a ceramic capacitor of 1 µF is placed between the V_{IN} and GND pins.

The ON pin which is compatible with standard GPIO logic threshold controls the state of the switch by signal STO1_EN. The QOD pin is left open, the output will be floating when ON pin is logic low.

Use 式 5 to calculate the inrush current during turn on for a given capacitance and slew rate:

$$I_{INRUSH} = \text{Slew Rate} \times C_{LOAD} = 2.3\text{mV}/\ \mu\text{s} \times 0.57\mu\text{F} = 1.311\text{mA} \tag{5}$$

The output of the switch is connected to the primary 3.3-V supply (VCC) of the gate driver. Dual redundant PNP bipolar junction transistors Q2 and Q3, actively clamp the logic side gate drive supply VCC to GND when STO_1 is activated. This prevents reverse bias of the VCC supply through the CMOS input gate driver ISO5852S (or ISO5452) in case the PWM signals are still active high (3V3).

2.4.3 STO_2 Signal Flow Path

2.4.3.1 High-Side Switch for Controlling Secondary-Side Supply Voltage of Gate Driver

The TPS27S100x is a single-channel, fully-protected, high-side switch with an integrated NMOS and charge pump. An external adjustable current limit improves the reliability of the whole system by clamping the inrush or overload current. 図 2-12 shows the schematic design of the TPS27S100.

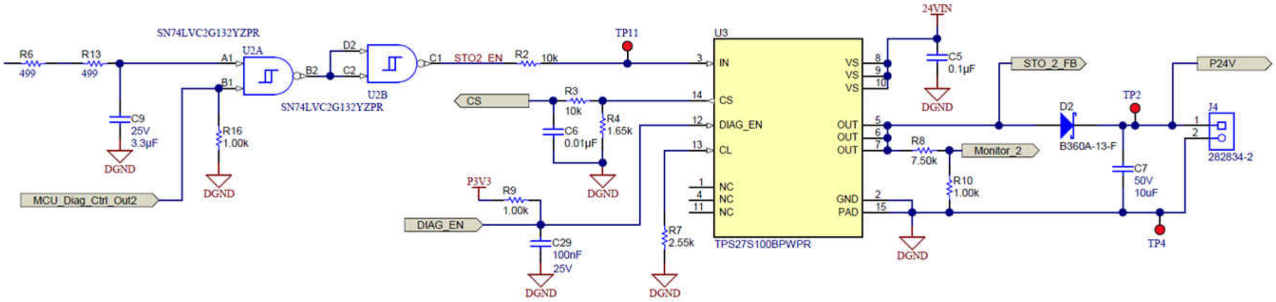


図 2-12. TPS27S100 Schematic

The device power supply is 24-V which is assumed to be protected against fault and remains within ±20% tolerance. Pin 3 Enable the control for channel activation by signal STO2_EN.

式 6 calculates the value of resistor R4, which is required to keep the 1-A nominal current in the 0- to 3.3-V current-sense range. To achieve better current-sense accuracy, a 1% tolerance or better resistor is preferred.

$$R4 = \frac{V_{(IMON)} \times K_{(IMON)}}{I_{OUT}} = \frac{3.3\ \text{V} \times 500}{1\ \text{A}} = 1.65\ \text{k} \tag{6}$$

The value of resistor R4 is selected as 1.65 K. The current-sense (CS) pin is connected to the ADC input of the diagnostic MCU (SIL 1) with a low-pass filter (R3 and C6).

To set the adjustable current limit value at 1 A, calculate R7 using 式 7.

$$R7 = \frac{VLIM_{(TH)} \times K_{(ILIM)}}{I_{OUT}} = \frac{1.233\ \text{V} \times 2000}{1\ \text{A}} = 2.47\ \text{K} \tag{7}$$

The value of resistor R7 is selected as 2.55 kΩ.

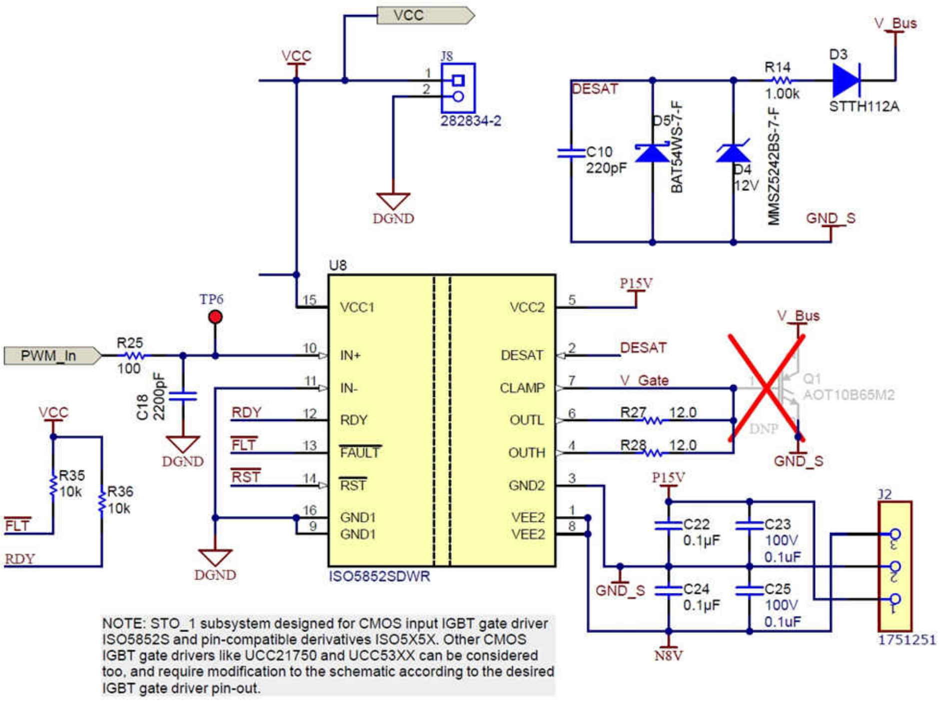
The enable pin is permanently connected to 3.3 V to enable continuous diagnostic monitoring and also send back to the diagnostic MCU (SIL 1).

2.4.3.2 Powering up Secondary Side: VCC2 of Gate Driver

The output of the smart switch is connected to J4 for powering up the TIDA-00199 board. The TIDA-00199 design generates a bipolar supply of +15 V, 0 V and –8 V, which powers up the secondary side of the isolated gate driver, ISO5852S on the TIDA-01599 board. For a detailed design procedure, see the *Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for Three-Phase Inverters* design guide.

2.4.4 Gate Driver Design

図 2-13 shows the schematic design of the isolated gate driver. VCC1 and GND1 are the supply pins for the input side of the ISO5452 or ISO5852S device. The supply voltage at VCC1 can range from 3.0 V to 5.5 V with respect to GND1. VCC2 and GND2 are the supply pins for the output side of the ISO5452 or ISO5852S device. VEE2 is the supply return for the output driver and GND2 is the reference for the logic circuitry. The supply voltage at VCC2 can range from 15 V up to 30 V with respect to VEE2. The PWM is applied across the IN+ and IN– pins of the gate driver.



NOTE: STO_1 subsystem designed for CMOS input IGBT gate driver ISO5852S and pin-compatible derivatives ISO5X5X. Other CMOS IGBT gate drivers like UCC21750 and UCC53XX can be considered too, and require modification to the schematic according to the desired IGBT gate driver pin-out.

図 2-13. ISO5852S Schematic

On the secondary-side of the gate driver, gate resistors R27 and R28 control the gate current of the switching device. The DESAT fault detection prevents any destruction resulting from excessive collector currents during a short-circuit fault. To prevent damage to the switching device, the ISO5452, ISO5852S slowly turns off the IGBT in the event of a fault detection. A slow turnoff ensures the overcurrent is reduced in a controlled manner during the fault condition. The DESAT diode D3 conducts the bias current from the gate driver, which allows sensing of the IGBT-saturated collector-to-emitter voltage when the IGBT is in the ON condition. D1 blocks high voltage when the IGBT is in the OFF Condition. In this reference design, D1 blocks a maximum of 1200 V during the IGBT OFF condition. Switching inductive loads causes large, instantaneous forward-voltage transients across the freewheeling diodes of IGBTs. These transients result in a large negative spike in the DESAT pin, which draws substantial current out of the device. To Limit this current below damaging levels, a 1-kΩ resistor is connected in series with the DESAT diode. A 220-pF blanking capacitor C10 is required, which disables the DESAT detection during the OFF-to-ON transition of the power device. For a detailed design procedure, see the *Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for Three-Phase Inverters* design guide.

2.4.5 STO_FB Signal Flow Path

The ISO7710 is a reinforced digital isolator which receives the input signal STO_FB_EN and operates with TIOS1013 (a push-pull driver) to provide feedback signal STO_FB (Logic high = 24 V) to safe PLC. STO_FB_EN is the output signal of the OR gate SN74AHC1G32 which receives the dual-channel feedback signal STO_1_FB and STO_2_FB. 図 2-14 shows the schematic.

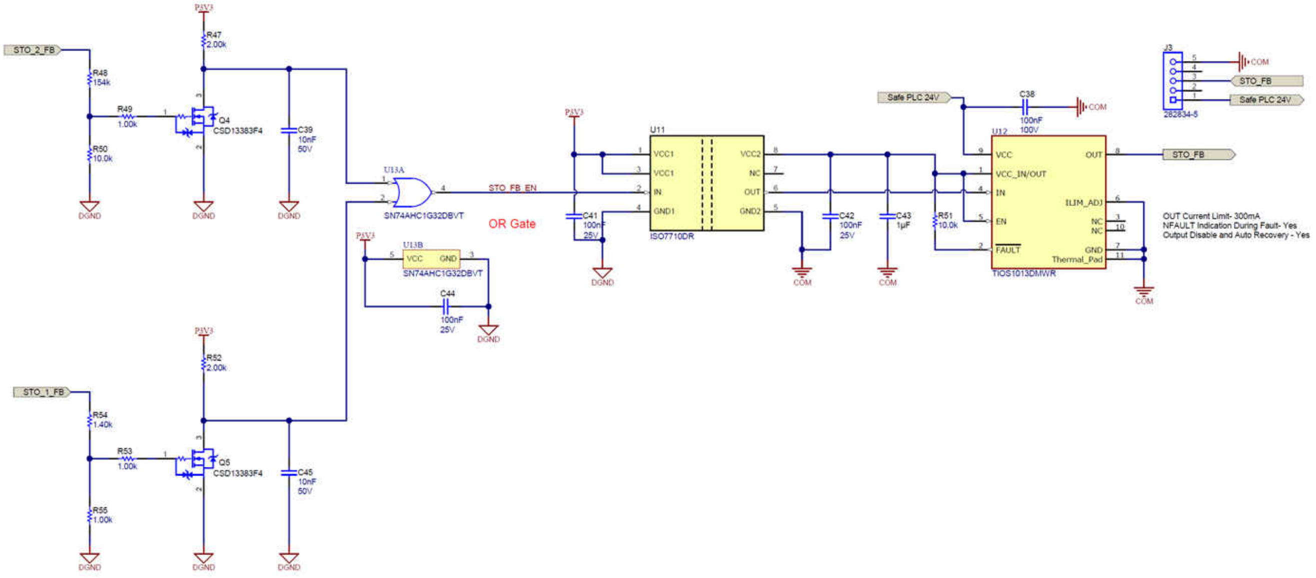


図 2-14. STO_FB Feedback Monitor Schematic

The STO_1_FB is the output of the load switch TPS22919 (controls the primary side VCC1 of the gate driver) and the STO_1_FB connects to the gate of Q5 with the resistors divided network (R54|R55 – 1.4 kΩ|1 kΩ) to synchronize the switching threshold of STO_1_FB with maximum UVLO1 threshold-voltage of gate driver ISO5852S (or ISO5452). According the data sheet of FET Q5 CSD13383F4 and gate driver ISO5852S (or ISO5452), the $V_{GS\ (th)\ min}$ = 0.7 V, $V_{IT+(UVLO1)}$ = 2.25 V, then to simulate the switching threshold. The logic 0 (OFF) for STO_1_FB is from 0-V to 2-V and Logic 1 (ON) is from 2 V to 3.9 V (3.9 V is maximum voltage of P3V3). The V_{GS} = 1.37 V during ON state with 1.6-mA I_{DS} current thanks to the limit resistor R52 (2 kΩ).

The STO_2_FB is the output of the load switch TPS27S100 (controls the secondary side VCC2 of gate driver via TIDA-00199 safe power supply) and the STO_2_FB connects to the gate of Q4 with the resistors divided network (R48|R50 – 154 kΩ|10 kΩ) to synchronized the switching threshold of STO_2_FB with maximum UVLO threshold-voltage of the TIDA-00199 design. According the data sheet of FET Q4 CSD13383F4 and TIDA-00199 design guide, the $V_{GS\ (th)\ min}$ = 0.7 V, $V_{OFF(UVLO)}$ = 14 V, then to simulate the switching threshold. The logic 0 (OFF) for STO_2_FB is from 0 V to 14 V and Logic 1 (ON) is from 14 V to 28.8 V (28.8 V is maximum voltage of P24-V). The V_{GS} = 1.46 V during ON state with 1.65 mA I_{DS} current due to the limit resistor R47 (2 kΩ).

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Getting Started Hardware

3.1.1 PCB Overview

図 3-1 shows a top view of the printed-circuit board (PCB) with RevE2.1

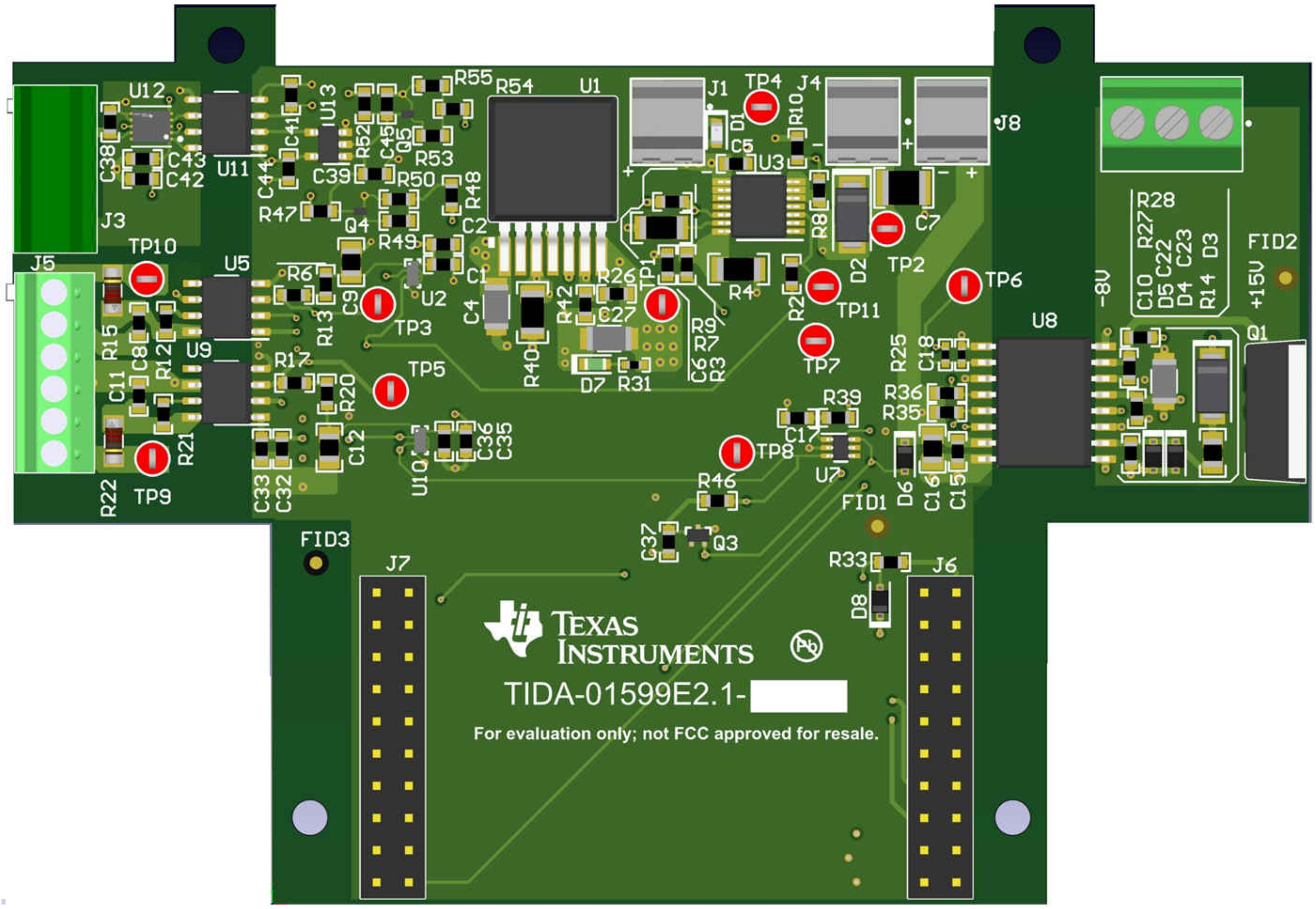


図 3-1. TIDA-01599 PCB - Top View

J5 is a six-pin connector, which provides an input to the two 24-V STO signals. J3 is a five-pin connector, which provides the 24-V power supply from safe PLC and also feedback the STO_FB signal to safe PLC. J1 is a 24-V connector, which powers up the high-side load switch. The 3.3-V rail is generated on the board, which supplies power to the digital isolator, AND Gate, low-side switch, and MCU. J4 and J8 are the connectors which supply 24 V and 3.3 V, respectively, from the output of the two switches.

J6 and J7 are female connectors, which have been set 52-mm apart for interfacing to the C2000™ MCU LaunchPad™ Development Kit.

表 3-1 through 表 3-4 list the pin assignments, pin description and levels of all the connectors used in TIDA-01599 reference design.

表 3-1. Pin Assignment Connector J5 (STO)

PIN	SIGNAL	SPECIFICATION	COMMENT
J5-1	STO_2	24-V for STO_2 input	
J5-2	GND2	24-V input GND2	
J5-3	GND1	24-V input GND1	
J5-4	STO_1	24-V for STO_1 input	
J5-5	NC		
J5-6	NC		

表 3-2. Pin Assignment Connector J3 (STO_FB)

PIN	SIGNAL	SPECIFICATION	COMMENT
J3-1	Safe PLC 24V	24-V power supply from safe PLC	
J3-2	NC		
J3-3	STO_FB	STO feedback signal with logic high 24-V and logic low 0-V	
J3-4	NC		
J3-5	COM	Reference GND of safe PLC 24-V	

表 3-3. Pin Assignment Connector J1, J4, J8

PIN	SIGNAL	SPECIFICATION	COMMENT
J1-1	DGND	24-V input DGND	
J1-2	24VIN	24-V input	
J4-1	P24V	24-V output	STO_2 output
J4-2	DGND	24-V output DGND	
J8-1	VCC	3.3-V output	STO_1 output
J8-2	DGND	3.3-V output DGND	

表 3-4. Pin Assignment Connector J6, J7 MCU Interface

PIN	SIGNAL	SPECIFICATION	COMMENT
J6-1	P3V3	3.3-V output	
J6-2	NC		
J6-3	NC		
J6-4	DGND	DGND for 3.3-V amd I/Os	
J6-5	MCU_STO2_In	3.3-V output from ISO1211 for STO_2 channel	For ISO1211 diagnostic
J6-6	Monitor_1	3.3-V output from TPS22919 for STO_1 channel	For TPS22919 diagnostic
J6-7	MCU_Diag_Ctrl_Out1	3.3-V logic high pulse from SIL 1 MCU	Diagnostic pulse to turn off the safety switch 1
J6-8	Monitor_2	2.8-V output from TPS27S100 for STO_2 channel	For TPS27S100 diagnostic
J6-9	MCU_Diag_Ctrl_Out2	3.3-V logic high pulse from SIL 1 MCU	Diagnostic pulse to turn off the safety switch 2
J6-10	NC		

表 3-4. Pin Assignment Connector J6, J7 MCU Interface (continued)

PIN	SIGNAL	SPECIFICATION	COMMENT
J6-11	NC		
J6-12	NC		
J6-13	RDY	Power-good output of gate driver, connect to 3.3-V with pull up resistor	Active high when both supplies are good
J6-14	NC		
J6-15	FLT	Fault output of gate driver, connect to 3.3-V with pull up resistor	Active-low during DESAT condition
J6-16	NC		
J6-17	RST	Reset input of gate driver (Logic high 3.3-V)	Apply a low pulse to reset fault latch
J6-18	NC		
J6-19	CS	Current-monitor output of TPS27S100, connect to MCU ADC input with voltage range 0-V to 3.3-V	
J6-20	NC		
J7-1	PWW_In	PWM Pulse from MCU (Logic low 0-V, Logic high 3.3-V)	
J7-2	DGND	DGND for I/Os	
J7-3	NC		
J7-4	NC		
J7-5	NC		
J7-6	NC		
J7-7	NC		
J7-8	NC		
J7-9	NC		
J7-10	NC		
J7-11	NC		
J7-12	NC		
J7-13	MCU_STO1_In	3.3-V output from ISO1211 for STO_1 channel	For ISO1211 diagnostic
J7-14	NC		
J7-15	DIAG_EN	Enable and disable pin of TPS27S100 for diagnostic functions	The enable pin is permanently connected to 3.3-V to enable continuous diagnostic monitoring and also send back to the diagnostic MCU (SIL 1)
J7-16	NC		
J7-17	NC		
J7-18	NC		
J7-19	NC		
J7-20	NC		

3.2 Testing and Results

注

The test results in this chapter were all tested based on RevE1.0 board. 表 3-5 lists all the design change from Rev E1.0 to Rev E2.1.

表 3-5. Design Change Log for Rev E2.1

NUMBER	REVISION	DOC. REF.	CHANGE DESCRIPTION
1	E2.1	Schematic and BOM	Change U5 (dual channel isolator ISO1212) to 2 single channel isolator U5 and U9 (ISO1211) to achieve a hardware fault tolerance of 1 (HFT=1).
2	E2.1	Schematic and BOM	Remove U4, U6 (TVS3300) on the input of isolator since ISO1211 with R_{sense}=562W and R_{th}=2.5kW supports ±1kV surge. Refer to ISO1211 data sheet Table 3.
3	E2.1	Schematic and BOM	Add 2nd clamp circuit (R46, C37, Q3) for the STO 1 output VCC (Gate driver logic power). This prevents reverse bias of the VCC supply through the CMOS input gate driver ISO5852S (or ISO5452) in case the PWM signals are still active high (3V3).
4	E2.1	Schematic and BOM	Add isolated 24 STO_FB output circuit to provide indication of the drive's status (safe state or normal operation). Can be used to feedback the drive's status to a safety PLC for additional diagnostics, if desired.
5	E2.1	Schematic and BOM	Change all the capacitors (MLCC) which design state is" obsolete" or" not for new design" to the parts with" Active" status.
6	E2.1	Schematic and BOM	Change indication LED D7 which design state is" obsolete" to the part with" Active" status. Change R31 from 50ohm to 200ohm according to new D7 rated current.
7	E2.1	Schematic and BOM	Load switch U7 change from TPS22860 to TPS22919 to overcome the input pin open fault: • TPS22860 input open|Hiz --> will lead un-determinate state of the output. • TPS22919 input open|Hiz --> will not pass through voltage to OUT.
8	E2.1	Schematic and BOM	Change single U2 (4 channels logic gate SN74HC7001DT) to dual separate logic gates U2 and U10 (SN74LVC2G132YZPR) to achieve HFT=1.
9	E2.1	Schematic and BOM	Separate R13 (1kohm) to R6 and R13 (2*499ohm). Separate R20 (1kohm) to R17 and R20 (2*499ohm). To get rid of the short|change value failure mode of resistor which will bypass the filter for logic gate.
10	E2.1	Schematic and BOM	Change J2 from OST ED555/3DS to PHX 1751251. Easier for assembly cables with bigger screw holes.
11	E2.1	Schematic	Add line around the STO_1 and STO_2 circuits and exclude the power supply. Add note for PSU that not part of the TUEV concept review, needs to be a protected supply. (refer to TIDA-01599_STO_Concept_FMEA_1v6.docx)
12	E2.1	Schematic	Add requirements for power rails to schematic (refer to TIDA-01599_STO_Concept_FMEA_1v6.docx)
13	E2.1	Schematic and BOM	Change R15, R22 to surge proof MELF, change C8, C11 voltage rating to 100V
14	E2.1	Layout	Change layout and board dimension according to above modification.
15	E2.1	Layout	Swap POWER layer (mid layer 2) and Ground layer (mid layer 1) to have a proper return ground for the high-speed signals on TOP layer.

3.2.1 Logic High and Logic Low STO Thresholds

図 3-2, 図 3-3, and 図 3-4 show the input logic high and low thresholds of the ISO1212. Note that the VIH (min) is 14.20 V and VIL (max) is 11.20 V, which correlates with the typical values calculated in セクション 2.4.1.

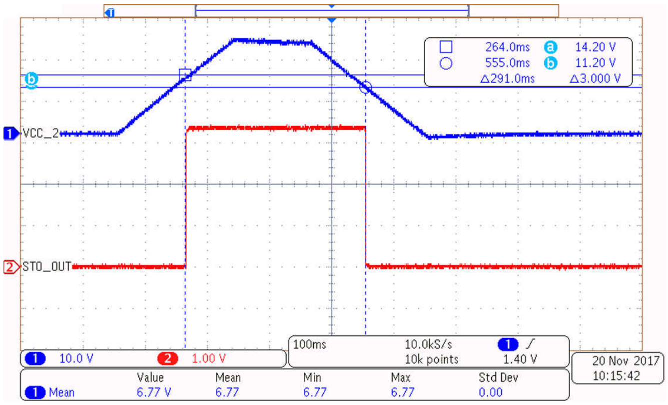


図 3-2. Logic Threshold for Digital Isolator

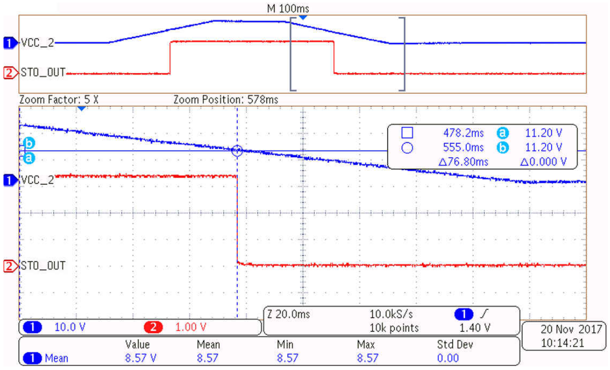


図 3-3. Logic Thresholds for Digital Isolator—Falling Edges

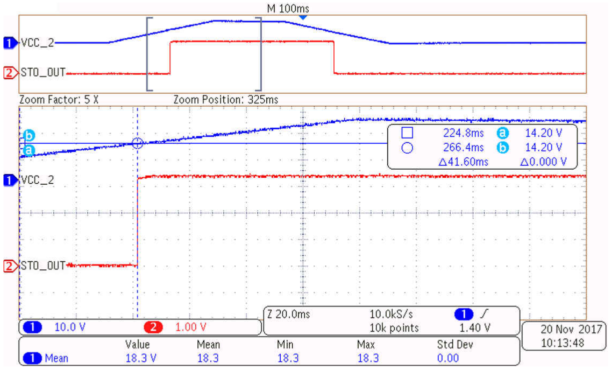


図 3-4. Logic Thresholds for Digital Isolator—Rising Edges

3.2.2 Validation of STO1 Signal

3.2.2.1 Propagation of STO1 to VCC1 of Gate Driver

The STO1 signal goes low for a period of 15 ms. As 図 3-5 and 図 3-6 show, the response time measured between the STO signal going low to the activation of the RDY pin is 2.7 ms. The response time is a function of the capacitance C16 at the output of the load switch. Vary the response time by changing the value of capacitance. As the VCC1 goes below the UVLO threshold, the RDY pin is activated. The UVLO+ threshold for ISO5852S is 2.25 V.

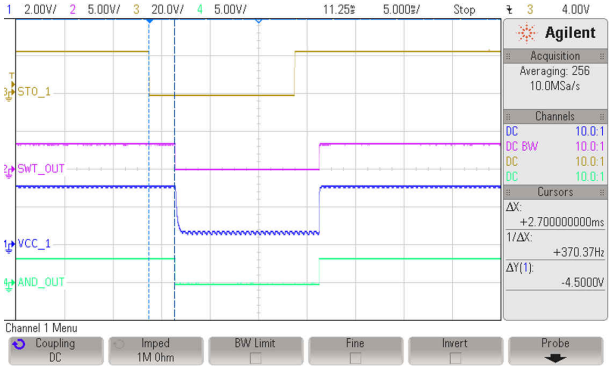


図 3-5. Propagation of STO1 to VCC1 of Gate Driver

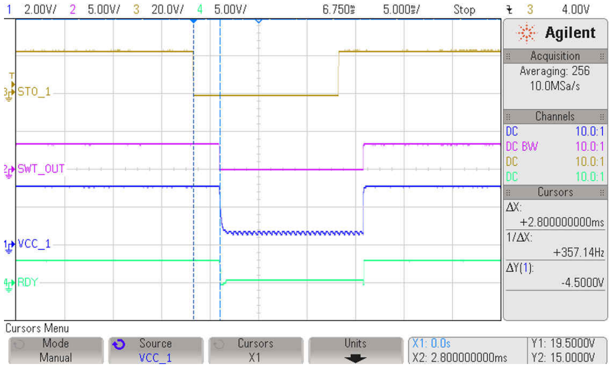


図 3-6. Indication of RDY Signal (Active Low) When VCC_1 Turns OFF

3.2.2.2 1-ms STO Pulse Rejection

図 3-7 and 図 3-8 show that the low-pass filter at the output of the digital isolator rejects the STO low pulse of 1 ms.

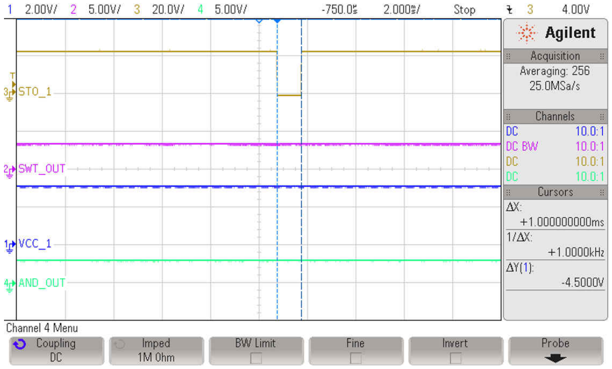


図 3-7. Rejection of 1-ms Pulse by LPF on STO1 Signal Path

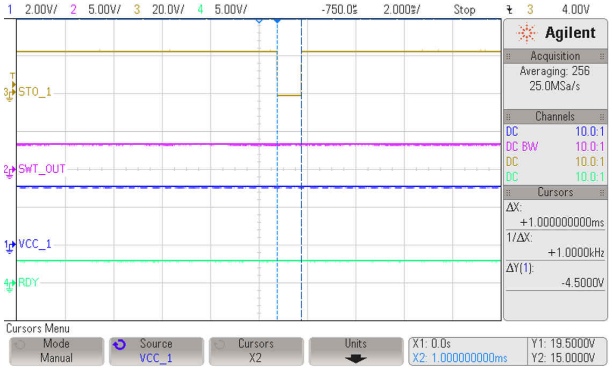


図 3-8. Rejection of 1-ms Pulse by LPF on STO1 Signal Path—RDY Pin Remains High

3.2.2.3 *Diagnostic Pulses From MCU Interface*

The MCU periodically sends low pulses of 100 µs. The VCC1 does not fall much below the UVLO of the gate driver during this time period. A capacitor of 0.47 µF ensures that VCC_1 does not fall below the UVLO threshold. Use a higher value of capacitance to minimize the voltage drop in VCC1 during the 100-µs STO pulses. 図 3-9 shows the test results.

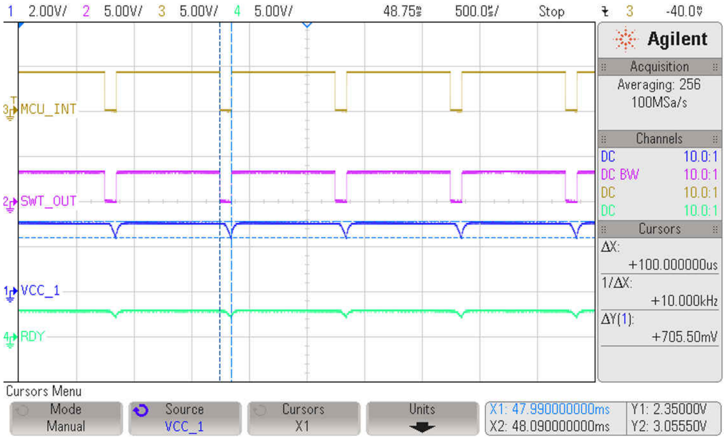


図 3-9. Effect of Diagnostic Pulses From MCU Interface on STO1 Signal Path

3.2.3 Validation of STO2 Signals

3.2.3.1 *Propagation of STO2 to VCC2 of Gate Driver*

The STO2 signal goes low for a period of 15 ms. As 図 3-10 and 図 3-11 show, the response time measured between the STO signal going low to the activation of the RDY pin is 7.4 ms. As the VCC2 goes below the UVLO threshold, the RDY pin is activated. The UVLO+ threshold for ISO5852S is 12 V. The response time is a function of the capacitance C7 at the output of the smart switch. Vary the response time by changing the value of capacitance.

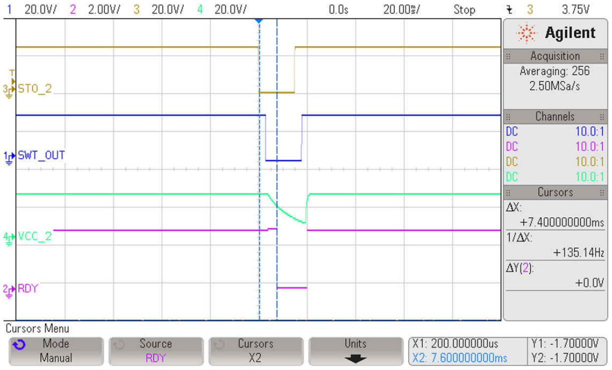


図 3-10. Indication of RDY Signal (Active Low) When VCC_2 Turns OFF

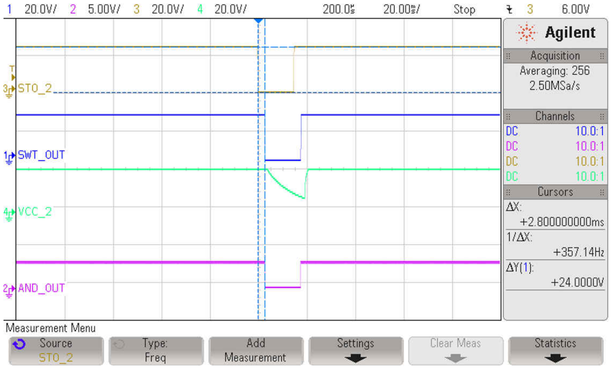


図 3-11. Propagation of STO2 to VCC2 of Gate Driver

3.2.3.2 1-ms Pulse Rejection

図 3-12 and 図 3-13 shows that the low-pass filter at the output of the digital isolator rejects the STO low pulse of 1 ms.

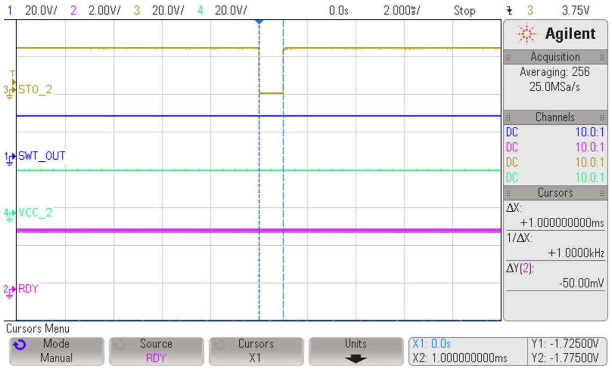


図 3-12. Rejection of 1-ms Pulse by LPF on STO2 Signal Path—RDY Pin Remains High

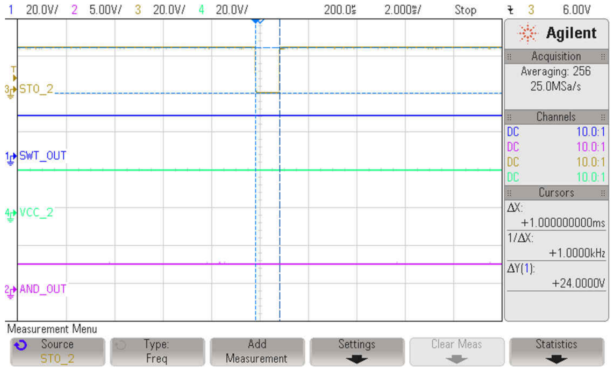


図 3-13. Rejection of 1-ms Pulse by LPF on STO2 Signal Path

3.2.3.3 Diagnostic Pulses From MCU

The MCU periodically sends low pulses of 100 µs. The VCC1 does not fall much below the UVLO of the gate driver during this time period. This is taken care of by using a capacitor C7 of 10 µF at the output of the switch. 図 3-14 shows the test results. Use a higher value of capacitance to minimize the voltage drop in VCC2 during the 100-µs STO pulses.

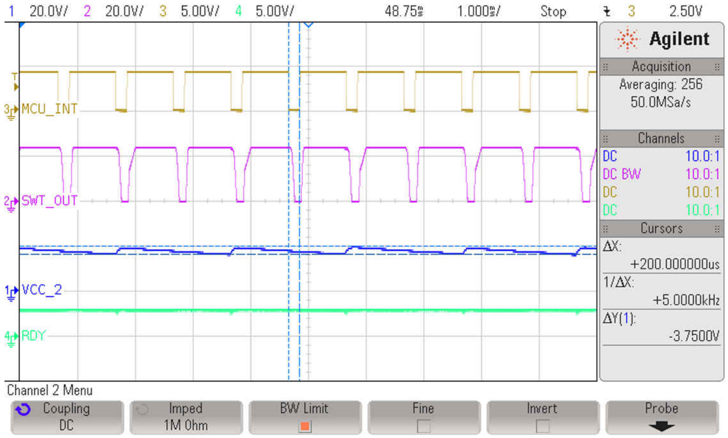


図 3-14. Effect of Diagnostic Pulses From MCU Interface on STO2 Signal Path

3.2.3.4 Inrush Current Measurement

Set the current limit with the TPS27S00 device. As mentioned in セクション 2.4.3, the current limit is set to 1 A. The current during the peak is limited to 1 A, as calculated in 式 8.

$$I_{OUT} = \frac{V_{(IMON)} \times K_{(IMON)}}{R4} = \frac{3.3\ \text{V} \times 500}{1.65\ \text{K}} = 1\ \text{A} \tag{8}$$

Calculate the current in the switch during the ON state using 式 9.

$$I_{OUT} = \frac{V_{(IMON)} \times K_{(IMON)}}{R4} = \frac{0.3\ \text{V} \times 500}{1.65\ \text{K}} = 90\ \text{mA} \tag{9}$$

This calculated value for I_{OUT} matches well with the value measured by the multimeter (see 図 3-15 and 図 3-16).

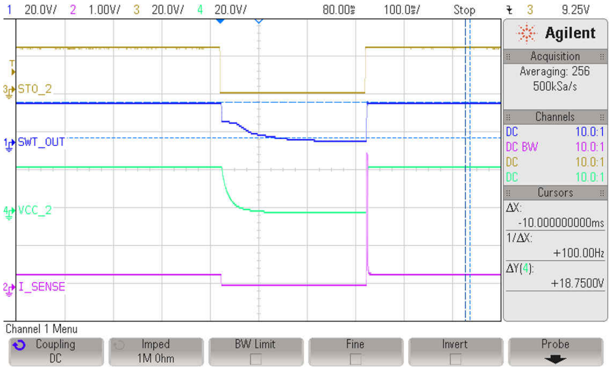


図 3-15. Inrush Current Measurement From TPS27S100

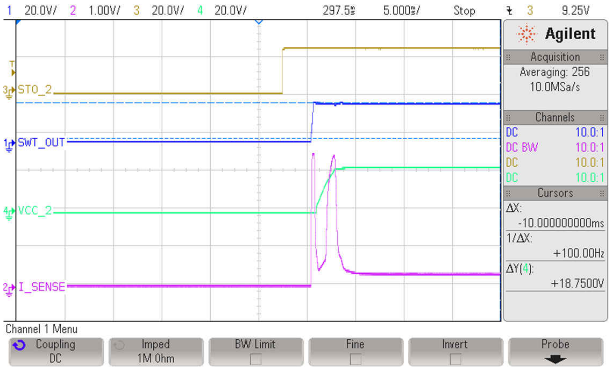


図 3-16. Zoomed-In Shot of Inrush Current Measurement From TPS27S100

The two peaks that 図 3-15 and 図 3-16 show during the transition state corresponds to the current limit due to the input and output capacitance of the TIDA-00199 board. Path 1 and path 2 in 図 3-17 show the two capacitances charging on the TIDA-00199 board.

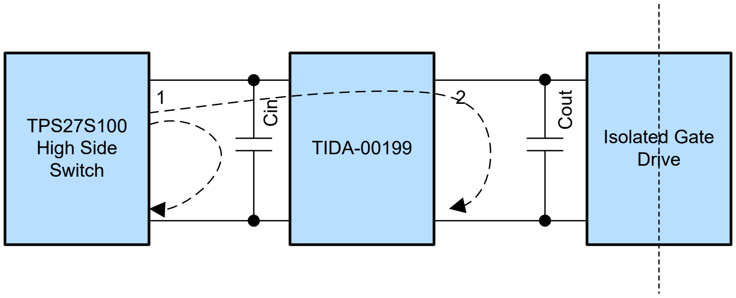


図 3-17. Charging of Input and Output Capacitors of TIDA-00199

3.2.4 3.3-V Voltage Rail From Switcher

図 3-18 and 図 3-19 show the ripple voltage on the 3.3-V rail at a load current of 13 mA. The peak-to-peak ripple voltage at 13 mA is 27.75 mV.

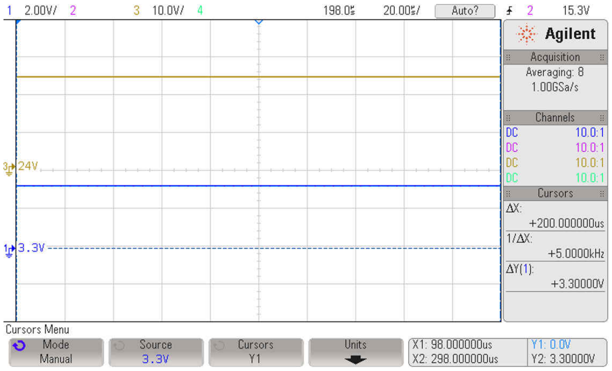


図 3-18. Ripple Voltage at Load Current of 13 mA

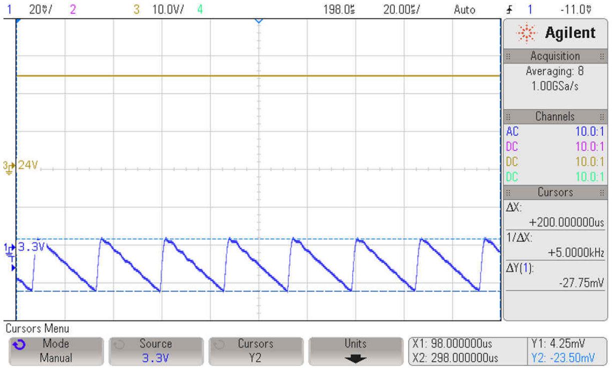


図 3-19. Zoomed-in Ripple Voltage at Load Current of 13 mA

図 3-20 and 図 3-21 show the ripple voltage on the 3.3-V rail at a load current of 40 mA. The peak-to-peak ripple voltage at 40 mA is 33 mV.

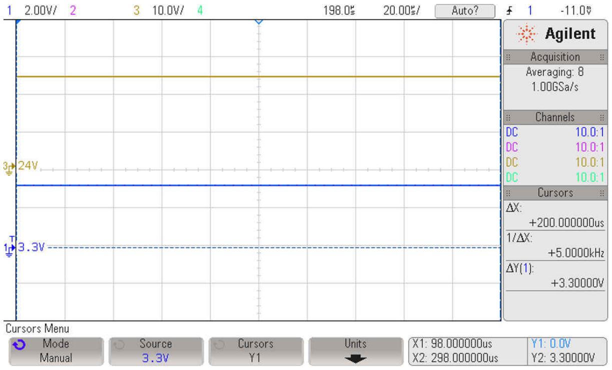


図 3-20. Ripple Voltage at Load Current of 40 mA

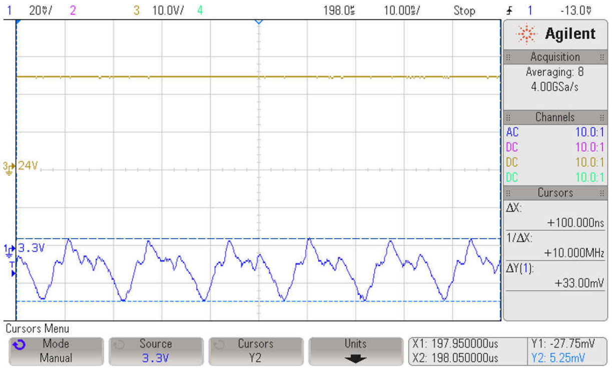


図 3-21. Zoomed-in Ripple Voltage at Load Current of 40 mA

3.2.5 60-V Input Voltage and Reverse Polarity Protection

図 3-22 and 図 3-23 show that, when a positive and negative voltage of 60 V is applied at the input of the digital isolator, the output remains unaffected.

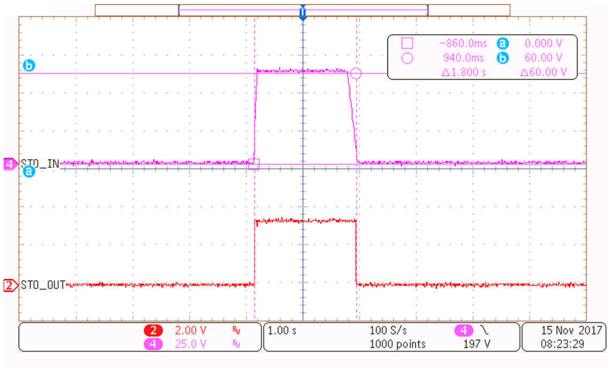


図 3-22. 60-V Input Voltage Protection

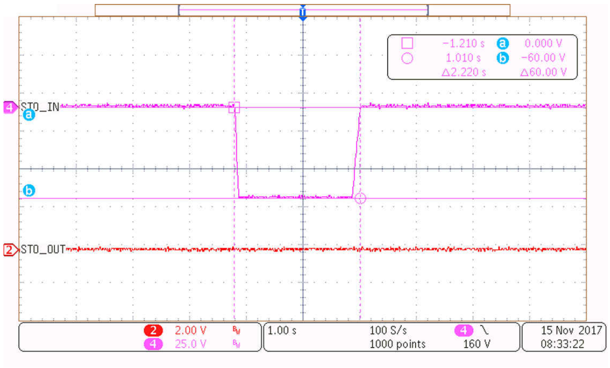


図 3-23. 60-V Reverse Polarity Protection

3.2.6 Validation of Trip Zone Functionality

図 3-24 shows the implementation of the trip feature. As the STO goes low, the trip starts to fall. Within 1.52 ms, the input PWM to the gate driver (and hence the output to the gate of the switching device) is terminated.

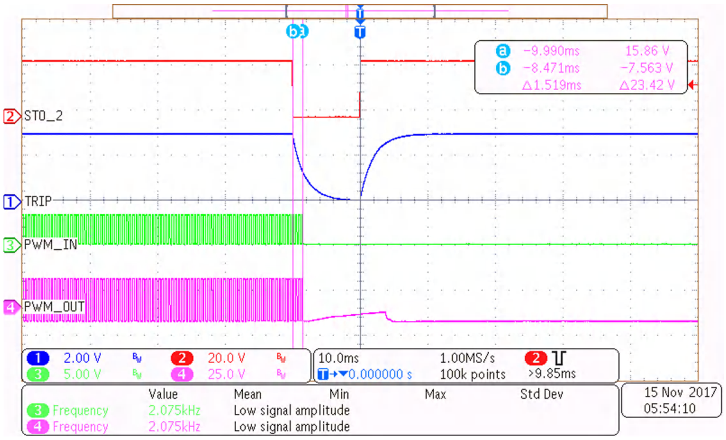


図 3-24. Validation of Trip Zone Functionality Through STO2

図 3-25 shows the rejection of a 1-ms STO low pulse by the design.

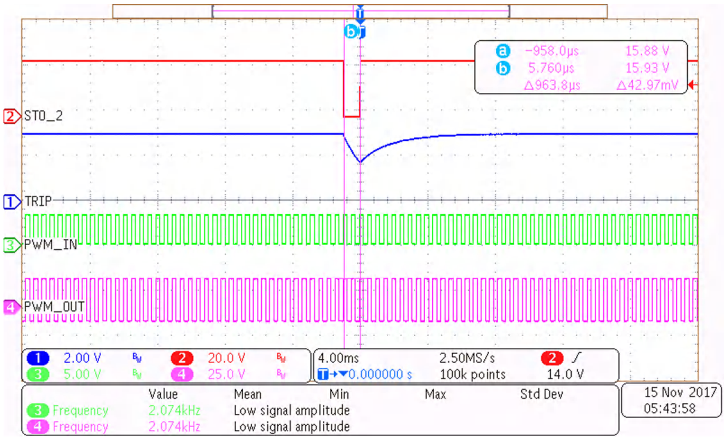


図 3-25. Effect of Rejection: 1-ms Pulse on Trip

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01599.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01599.

4.3 Layer Plots

To download the layer plots, see the design files at TIDA-01599.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01599.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01599.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01599.

5 Related Documentation

1. Texas Instruments, TIDA-00199 *Wide-Input Isolated IGBT Gate-Drive Fly-Buck™ Power Supply for Three-Phase Inverters* design guide
2. Texas Instruments, TIDA-00195 *Three-Phase High PWM Frequency GaN Inverter Reference Design for 200-V AC Servo Drives* design guide
3. IEC 61800-5-2, Adjustable speed electrical power drive systems – Part 5-2: Safety requirements – Functional
4. IEC 61508, Functional safety of electrical | electronic | programmable electronic safety-related systems
5. ISO13849-1 | 2, Safety of machinery - Safety-related parts of control systems - Part 1: General principles for design, - Part 2: Validation
6. Texas Instruments, TIDA-01599 *STO Concept TUEV Report TF97657T Rev.1.1*
7. Texas Instruments, *Overview STO Concept TIDA-01599* functional safety information

5.1 Trademarks

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6 About the Author

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7 Recognition

The authors would like to recognize the excellent contributions from **NELSON ALEXANDER** during the design, test, and documentation phases of the TIDA-01599 design.

8 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

重要なお知らせと免責事項

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