参考資料

Design Guide: TIDA-01022

DSO、レーダー、5G ワイヤレス・テスト・システム用の、柔軟な 3.2GSPS マルチチャネル AFE のリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このリファレンス・デザインは、マルチチャネルの高速アナログ・フロントエンドに特化したもので、デジタル・ストレージ・オシロスコープ (DSO)、ワイヤレス通信テスト機器 (WCTE)、レーダーなどの最終機器で一般に使用されます。このデザインでは、マルチチャネル・アナログ・フロントエンドで重要となる設計仕様と設計上の課題、たとえば高いサンプリング・レート、チャネル間スキュー、確定的レイテンシ、入力ダイナミック・レンジなどを取り入れています。このデザインは、3.2Gbps のデュアル・チャネル・アナログ/デジタル・コンバータ (ADC) である ADC12DJ3200 を使用しています。この製品には、チャネルごとに 5GSPS までのサンプリング・レートを持つピン互換のロードマップ・デバイスが存在します。

このデザインでは、確定的レイテンシと、5ps 未満の最小チャネル間スキューが示されます。このデザインのアクティブ・バランは、1.5GHz のシステム帯域幅を達成しています。また、このデザインにはオプションの変圧器入力があり、アクティブおよびパッシブのアナログ・フロントエンドの性能を評価できます。

特長

- 3.2GSPS、1.5GHz、マルチチャネル、高速のアナログ・フロントエンド
- チャネル間のクロック・スキューは 5ps 未満
- マルチチャネルに対応した JESD204B 準拠のクロック
- 確定的レイテンシ
- TI の高速キャプチャ・カードをサポート (FMC+ to FMC アダプタ付きの TSW14J56 と、TSW14J57)
- 8、16、32 JESD レーン：最大 12.8Gbps で動作し、12Gbps でテスト済み
- ピン互換の ADC12DJxx00 ファミリ用のスケーラブルなプラットフォーム
- 理論、計算、コンポーネントの選択、PCB の設計、測定結果を記載

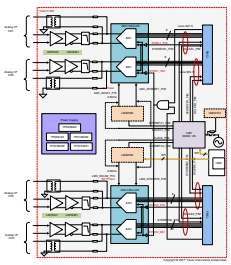
アプリケーション

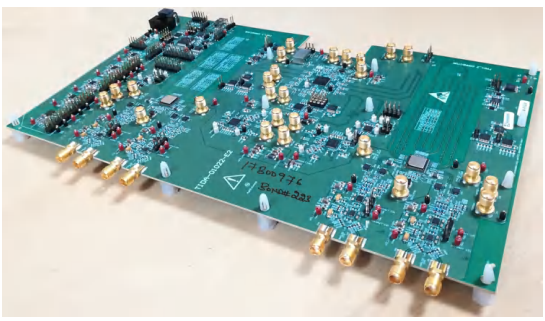
- 高性能オシロスコープ
- ワイヤレス通信のテスト機器
- ソフトウェア無線
- レーダー

Resources

TIDA-01022			Design Folder
ADC12DJ3200			Product Folder
LMK04828	LMX2594	LMK61E2	Product Folder
LMH6401	LMH5401	BUF802	Product Folder
TPS82130	TPS259261		Product Folder
TPS7A8400	TPS7A8300	TPS7A3301	Product Folder

ASK Our E2E Experts





1 System Description

The objective of this reference design is to demonstrate a multichannel analog front end (AFE) with a pin-compatible analog-to-digital-converter (ADC) family for different sampling rates requirements. The system signal-to-noise ratio (SNR) measures the AFE performance, which is then compared with the onboard passive balun and active balun and an LMH5401 fully differential amplifier (FDA) with an LMH6401 programmable variable gain amplifier (PVGA). The onboard, complete multichannel clocking solution is designed based on TI high-performance clocking parts LMK61E2, LMK4828, and LMX2594. 表 1-1 lists the key system-level specifications from the AFE with a multichannel clocking perspective.

Multichannel, high-speed, giga-sample acquisition applications such as a digital storage oscilloscope (DSO), phased-array radio detection and ranging (RADAR), multiple-input multiple-output (MIMO) for wireless communication, and 5G wireless testers all require accurate phase coherence between channels for accurate data acquisition with a high-input signal bandwidth.

Most high-speed digitizers (DSOs) feature only a few channels. Synchronizing the sample clock in a multichannel system is necessary in applications that require tens or hundreds of channels and time correlation between these channels. Clock synchronization in a system with just a few channels is very challenging in and of itself and even more complex when working with an increased channel count.

1.1 Key System Specifications

表 1-1. Key System Specifications

PARAMETER	SPECIFICATIONS	
Input channels	Four	
Input type	Single ended or differential ended	
Input analog band width (–3 dB)	DC 1.5 GHz	
Maximum input voltage	7.6 V_{P-P}	
Maximum sample rate	3.2 GSPS	
Resolution	12 bit	
Maximum system voltage gain	24.4 dB or 16.5 V/V	
Channel-to-channel skew (F_s = 2700 MHz)	< 5 ps	
System SNR(1) (–1 dB full scale) F_s = 3000 MHz	Transformer input	FDA input: (LMH5401 = 12 dB, LMH6401 = 10 dB)
	56.2 dB at 757 MHz	51.6 dB at 757 MHz
	55.5 dB at 997 MHz	51.6 dB at 997 MHz
	55.0 dB at 1497 MHz	51.1 dB at 1497 MHz
Operating temperature	0°C to 60°C	
Storage temperature	–40°C to 85°C	
Connectors	560-pin FMC interface connector, supports TSW14J56/57 high-speed capture card	
Power	12-V DC, 4 A	
Form factor (L × W)	295 mm × 176 mm	

(1) See *Testing and Results* for more details.

2 System Overview

2.1 Block Diagram

図 2-1 shows the system-level block diagram of the TIDA-01022 design interface with two high-speed capture cards (TSW14J56) in master slave mode. This reference design uses an FMC+ to FMC adapter printed circuit board (PCB) to interface the TIDA-01022 board with the capture cards.

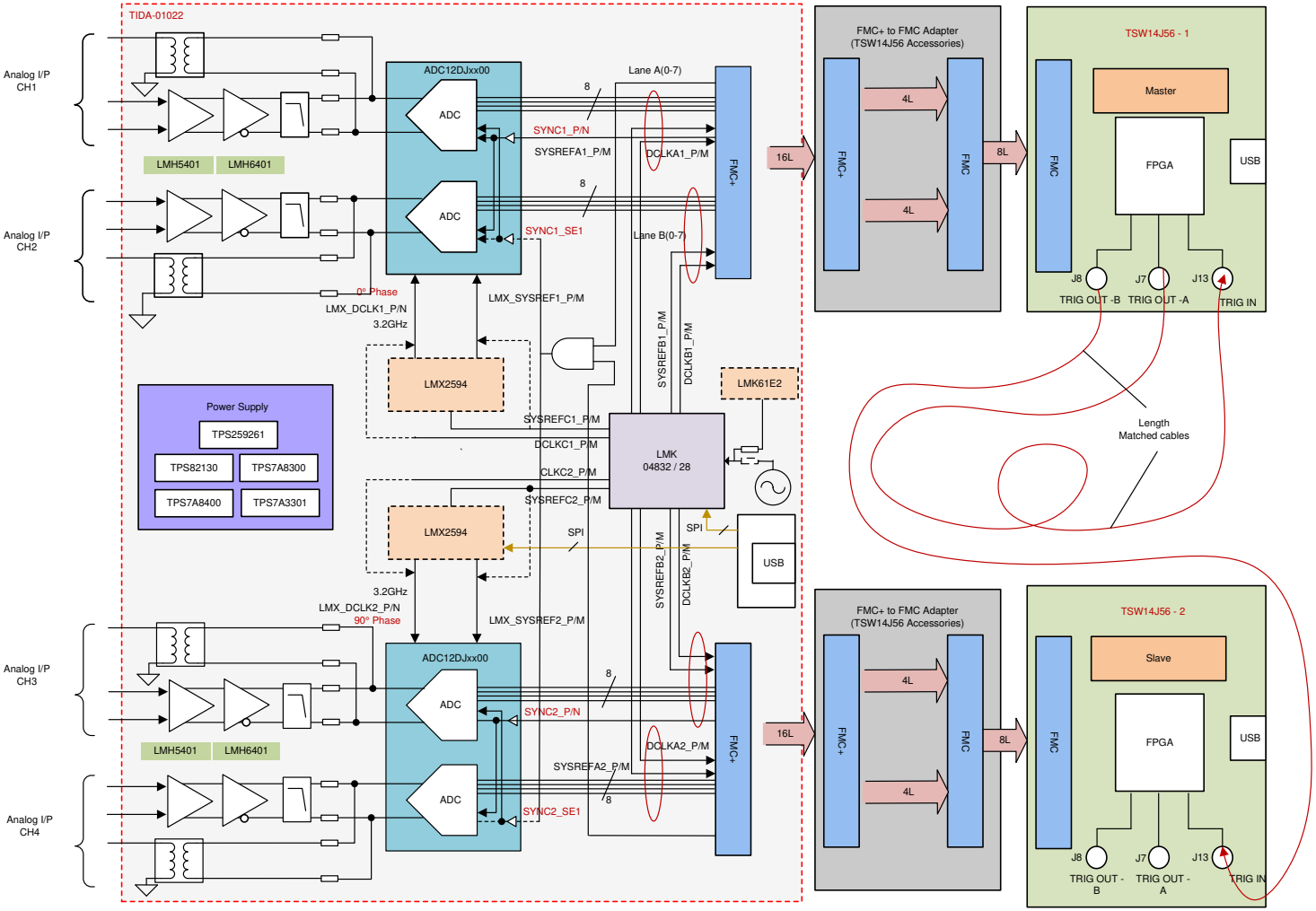


図 2-1. TIDA-01022 System Block Diagram

2.2 System-Level Description

図 2-2, 図 2-3, and 図 2-4 show the subsystem block diagrams of the high-performance DSO, phase-array RADAR, and wireless tester, respectively. The AFE and system clocking architecture are highlighted in each diagram and are common across all three pieces of end equipment.

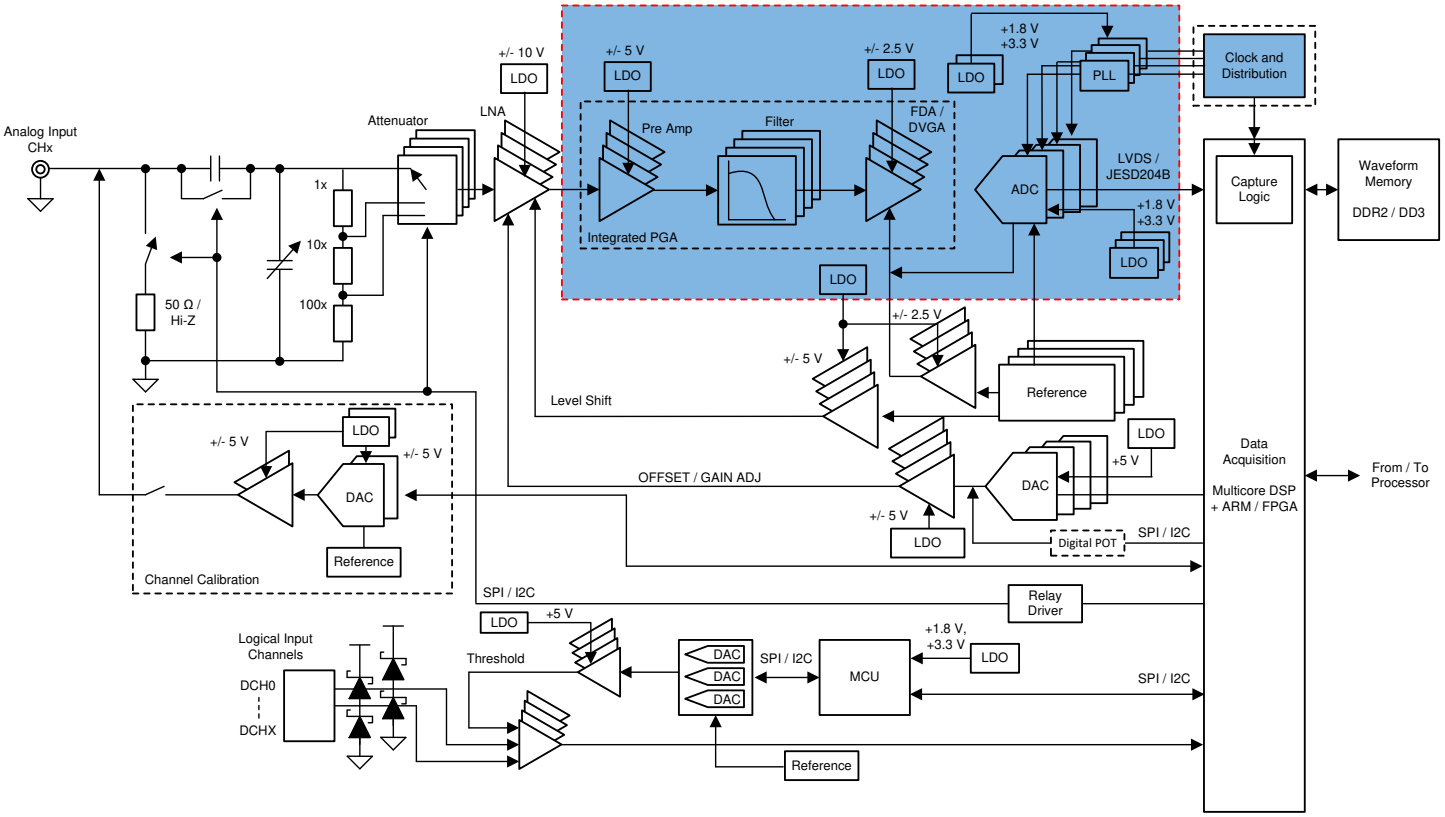


図 2-2. High-Performance DSO AFE Subsystem

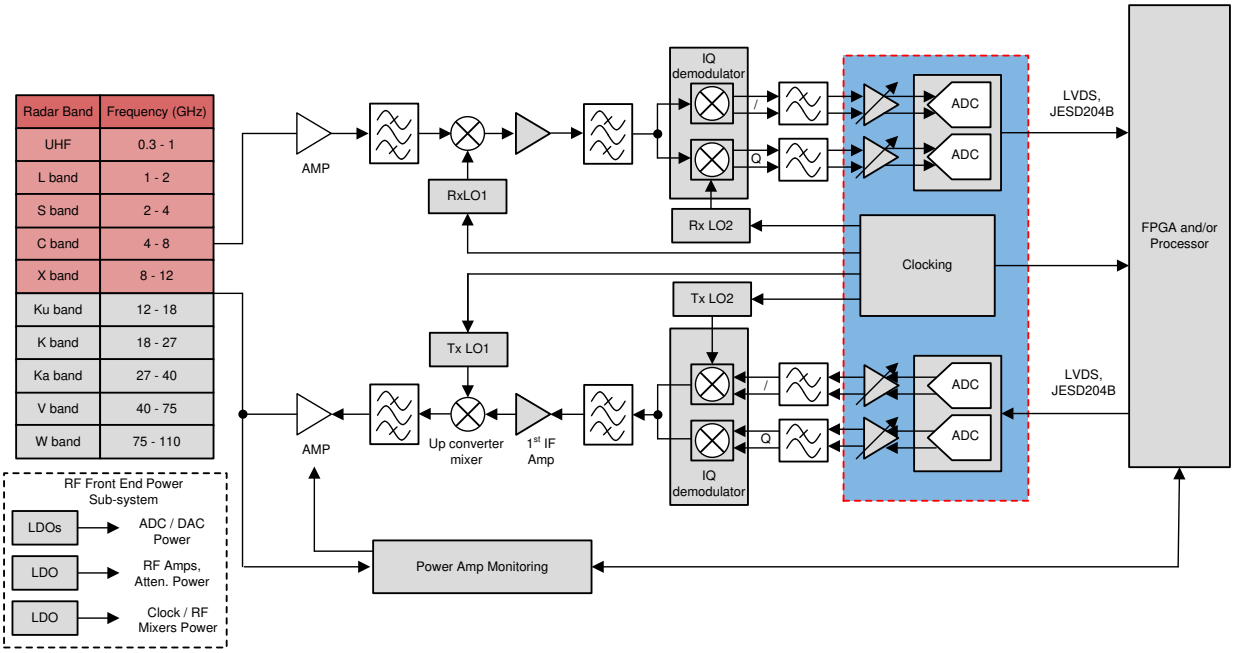


図 2-3. RADAR RF Front-End Subsystem

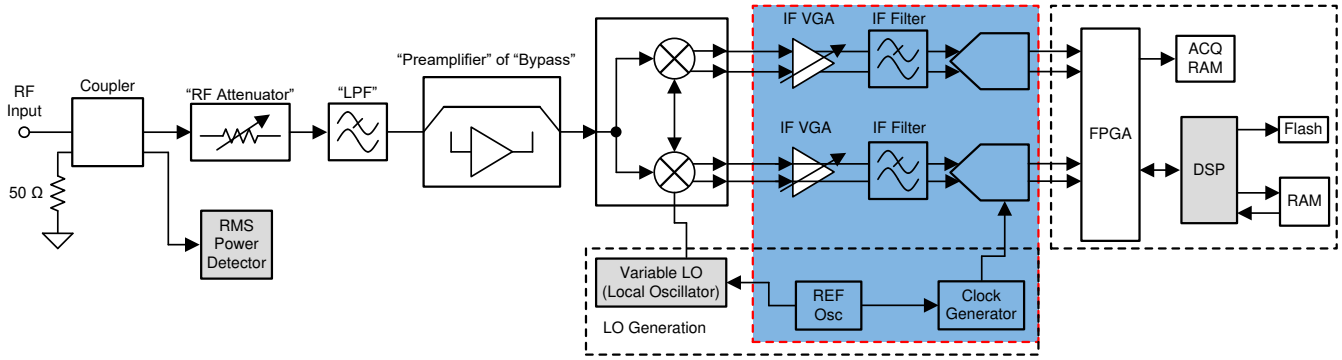


図 2-4. Wireless Tester AFE Subsystem

High-performance, multichannel digital storage oscilloscopes require a signal chain with a wideband AFE, high dynamic range, high SNR, and low channel-to-channel skew. The analog bandwidth is in the order of a 200-MHz to 5-GHz range and the sampling rate requires 5 Gsps to 10 Gsps.

Wireless testers require high dynamic range and wideband receivers to test 5G and later standards for wireless compliant equipment. These testers require a new high-performance DAC and ADC to obtain the true performance for high accuracy. The requirement of higher data capacity and user data demands a higher carrier frequency compared to the cellular implementation below 6 GHz of today. At the time of this writing, the final specifications for the 5G standard is not available; however, a bandwidth around 500 MHz to 2 GHz is currently under consideration.

Phased-array radar applications require a high dynamic range, wide receiver bandwidth, low latency, and good synchronization between the channels. This reference design front end covers the RADAR lower-band range from 0.3 GHz to 4 GHz (UHF, L band, and S band).

2.3 Highlighted Products

The system contains the number of highlighted parts, which determine the overall system performance. These parts are grouped in the following subblocks:

- Analog signal chain
- Clock
- Power

2.3.1 Analog Signal Chain

2.3.1.1 LMH5401

The LMH5401 is a very-high performance, differential amplifier optimized for radio frequency (RF), intermediate frequency (IF), or high-speed, DC-coupled, time domain applications. The device is an ideal choice for single-ended to differential conversion (SE-DE), which replaces balun up to a 2-GHz usable bandwidth. The device offers excellent linearity performance DC- 2 GHz at a 12-dB gain. The device operates at both single- and dual supply with low power consumption. Enable the common-mode reference pin to match the ADC common-mode input requirements. This characteristic enables the designer to drive GSPS ADCs for use in applications such as test and measurement, broadband communication, and high-speed data acquisition.

2.3.1.2 LHM6401

The LMH6401 is a wideband, digitally-controlled variable gain amplifier (DVGA) designed for DC-to-radio frequency applications. The noise and distortion performance are optimized to drive ultra-wideband ADCs. The device offers DC 4.5-GHz bandwidth at a 26-dB gain and gain range from –6 dB to 26 dB in 1-dB steps. The gain control can be done using a standard serial peripheral interface (SPI) and the user can power down the device by using either the power down pin or SPI.

2.3.1.3 BUF802

The BUF802 device is an open-loop, unity gain buffer with a junction-gate field-effect transistor (JFET) input stage that offers low-noise, high-impedance buffering for data acquisition system (DAQ) front-ends. The device supports DC to 3.1 GHz of bandwidth while offering excellent distortion and noise performance across the frequency range.

The BUF802 can be used as a standalone buffer, Buffer Mode (BF Mode), or in a composite loop with a precision amplifier, Composite Loop Mode (CL Mode), to achieve DC precision and a wide, large-signal bandwidth. The low output impedance and high output current drive strength enables the BUF802 to drive loads as high as 50 Ω. The BUF802 comes with adjustable quiescent current to optimize system level power and performance.

2.3.2 Clock

2.3.2.1 LMK61E2

The LMK61E2 programmable oscillator has the following features:

- Ultra-low noise, high performance (90-fs RMS jitter at > 100 MHz)
- Frequency tolerance ±50 ppm
- Frequency output 10 MHz to 1 GHz
- I^2C interface

2.3.2.2 LMK04828

The LMK04828 is ultra-low noise JESD204B-compliant clock jitter cleaner with dual phase-locked loops (PLLs). The 14 outputs drive seven JESD204B devices or other logic devices. The dual VCOs, dynamic digital delay, and glitch-less analog delay provide a flexible high-performance clocking solution. The LMK04828 supports two ranges of VCOs, from 2370 MHz to 2630 MHz and 2920 MHz to 3080 MHz.

2.3.2.3 LMX2594

The LMX2594 is a high-performance, wideband PLL with integrated VCOs that can generate frequency from 10 MHz to 15 GHz without using an internal doubler. The high-performance PLL with figure of merit of –236 dBc/Hz and high-phase detector frequency can attain very-low in-band noise and integrated jitter. The high-speed N-divider has no pre-divider, thus significantly reducing the amplitude and number of spurs. There is also a programmable input multiplier to mitigate integer boundary spurs. The LMX2594 adds support for generating or repeating SYSREF (compliant to JESD204B standard), which make it an ideal low-noise clock source for high-speed data converters. Fine delay adjustment (9-ps resolution) is provided in this configuration to account for delay differences of board traces. The output drivers within the LMX2594 delivers output power as high as 7 dBm at a 15-GHz carrier frequency. The device runs from a single 3.3-V supply and has integrated LDOs that eliminate the requirement for onboard, low-noise LDOs.

2.3.3 Power

2.3.3.1 TPS82130

The TPS82130 is a 17-V input, 3-A step-down converter MicroSiP™ power module optimized for a small solution size and high efficiency. The module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components, and save printed-circuit board (PCB) area. The adjustable output voltage is specified from 0.9 V to 6 V.

2.3.3.2 TPS7A84

The TPS7A84 is a low-noise (4.4 μV_{RMS}) LDO which is capable of sourcing 3 A with only 180 mV of maximum dropout. The device output voltage is pin-programmable from 0.8 V to 3.95 V and adjustable from 0.8 V to 5.0 V using an external resistor divider. The power supply rejection is 40 dB at 500 kHz.

2.4 System Design Theory

Channel-to-channel delay is critical in multichannel systems. Applications such as high-speed data acquisition, phase-array radar, and test and measurement require simultaneous measurement of high-frequency signals over many channels. The sampling clocks for the channels must be synchronized to achieve a low skew between the channels.

Achieve synchronous sampling by using proprietary trigger and clock distribution systems within digitizers; do note, however, that this implementation supports a limited number of channels and is not suitable for large-scale multichannel systems.

The distribution of a common high-stability, low-frequency clock reference to all the possible modules and instruments to achieve synchronous sampling across a number of channels presents a major technical challenge at high frequencies. For example, the backplane type of interface busses and connectors may not be suitable for high-frequency signals. A clock pulse deteriorates significantly beyond 100 MHz and introduces jitter. The use of a high-frequency coaxial cable leads to a complex and costly system.

2.4.1 High-Speed, Low-Phase Noise Clock Generation

High-performance data converters require high-precision clocking with ultra-low phase noise. The generation of these clocks and their distribution to various components through PCBs, connectors, and other devices requires impedance matching, signal power isolation, and high fan-out clock buffering to drive a receiver from a long distance. The clock generation architecture can vary depending on system requirements. Clock generation and distribution are typical in low-channel-count systems such as oscilloscopes and can be performed using a single device; however, careful routing and clock-to-clock matching is necessary to obtain optimum performance.

Most high-speed digitizers or DSOs feature only a few channels. Synchronizing the sample clock in a multichannel system is necessary in applications that require tens or hundreds of channels and time correlation between these channels. Clock synchronization in a system with just a few channels is very challenging in and of itself and even more complex when working with an increased channel count.

This reference design uses the clocking solution provided in *Multichannel JESD204B 15-GHz Clocking Reference Design for DSO, Radar, and 5G Wireless Testers*.

2.4.2 Channel-to-Channel Skew

The delay (channel-to-channel skew) or phase relationship between channels is a very important specification for high-speed multichannel acquisitions. The sample clock delay includes delay lines, data path delay, and ADC aperture delay. An accurate sampling across channels with a sub-picosecond delay presents design challenges. Use an acquired signal as a time reference to measure the sample clock delay. Extract the timing information through fast-Fourier transform (FFT) by using the MathLab program. Adjust this information in any one of the clock chain path components (clock generation, distribution path, and receiver end) or a combination of them.

The ADC12DJ3200 offers noiseless aperture delay adjustment (t_{AD} adjust) features to shift the sampling instance of the ADC in precise steps to synchronize multiple ADC12DJ3200 devices or to fine-tune system latency and channel-to-channel skew.

This reference design uses the ADC t_{AD} to match channel-to-channel delays less than 5 ps. See セクション 7.3 for the test setup to measure the channel-to-channel skew of the TIDA-01022 design. The designer can also use the LMX2594 device to meet the delay requirement in sub nanoseconds depending on the system requirements and the delay adjustment features available in the LMK4828 device.

2.4.3 Deterministic Latency

Latency is the duration of time that passes when traveling from point A to B. A system deterministic latency means that a system has a fixed delay from point A to point B during every system start-up and during each subsequent system power-up. Process variations in the system such as temperature and supply voltage cause variations in the delay between the transmission and receiver link, as well as delays between multiple linked establishments in a multichannel system.

2.4.3.1 Importance of Deterministic Latency

Any system that requires a feedback loop for digital capture or automatic process control is sensitive to latency variations. Latency variation affects the phase and gain margins and stability of a closed-loop control system. The presence of the delay potentially decreases stability and degrades the quality of control due to unavoidable gain reduction.

The JESD204B interface addresses these requirements and how to establish the deterministic latency of the link between a logic device and multiple data converters. Establishing this link is possible by using subclass 1 or 2. Depending on the subclasses, JESD uses SYSREF or the SYNC timing signal as a reference.

The ADC12DJ3200 device has a JESD204B interface feature that uses the DEV CLK and SYSREF signal to achieve multichannel synchronization and deterministic latency.

The subclass 1 requirements are as follows:

- Subclass 1 uses an external SYSREF signal to act as a common timing reference for multiple devices in a JESD204B system to achieve deterministic latency. The SYSREF signal is source synchronous to the device clock.
- For correct alignment, the SYSREF signal must meet the setup and hold time requirements of the device clock and must be distributed to each TX/RX device with a matched trace length and signal type relative to the device clock (see 図 2-5). The TX/RX device must specify the setup and hold time requirements of the SYSREF signal with respect to the device clock at the input.

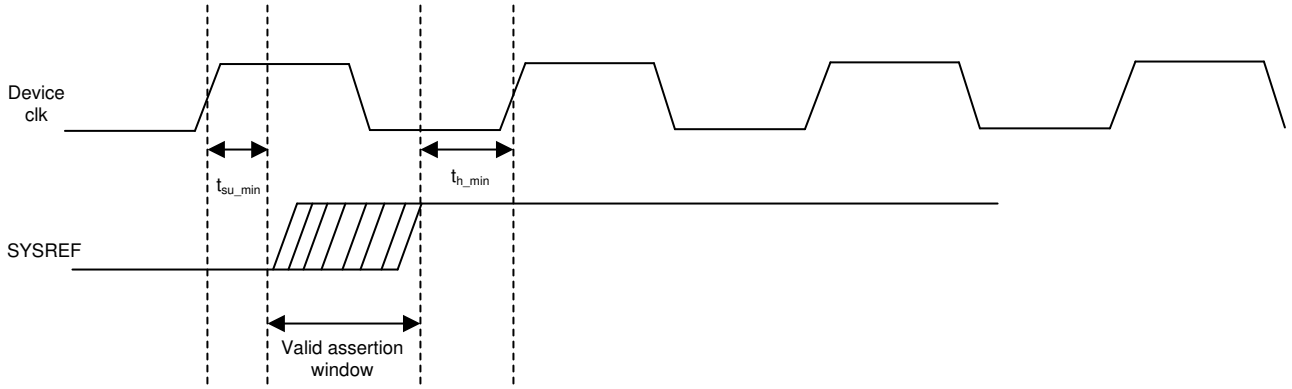


図 2-5. JESD DEVCLK and SYSREF Timing

- The next requirement to meet is phase aligning the device clock (sampling clock) and SYSREF signal with all data converter and logical devices. This phase alignment requires trace length matching the DEVCLK and SYSREF signals for all the devices. The SYNC signals from multiple logic devices combine together as AND logic, which then transmit to the ADCs (see 図 2-6).

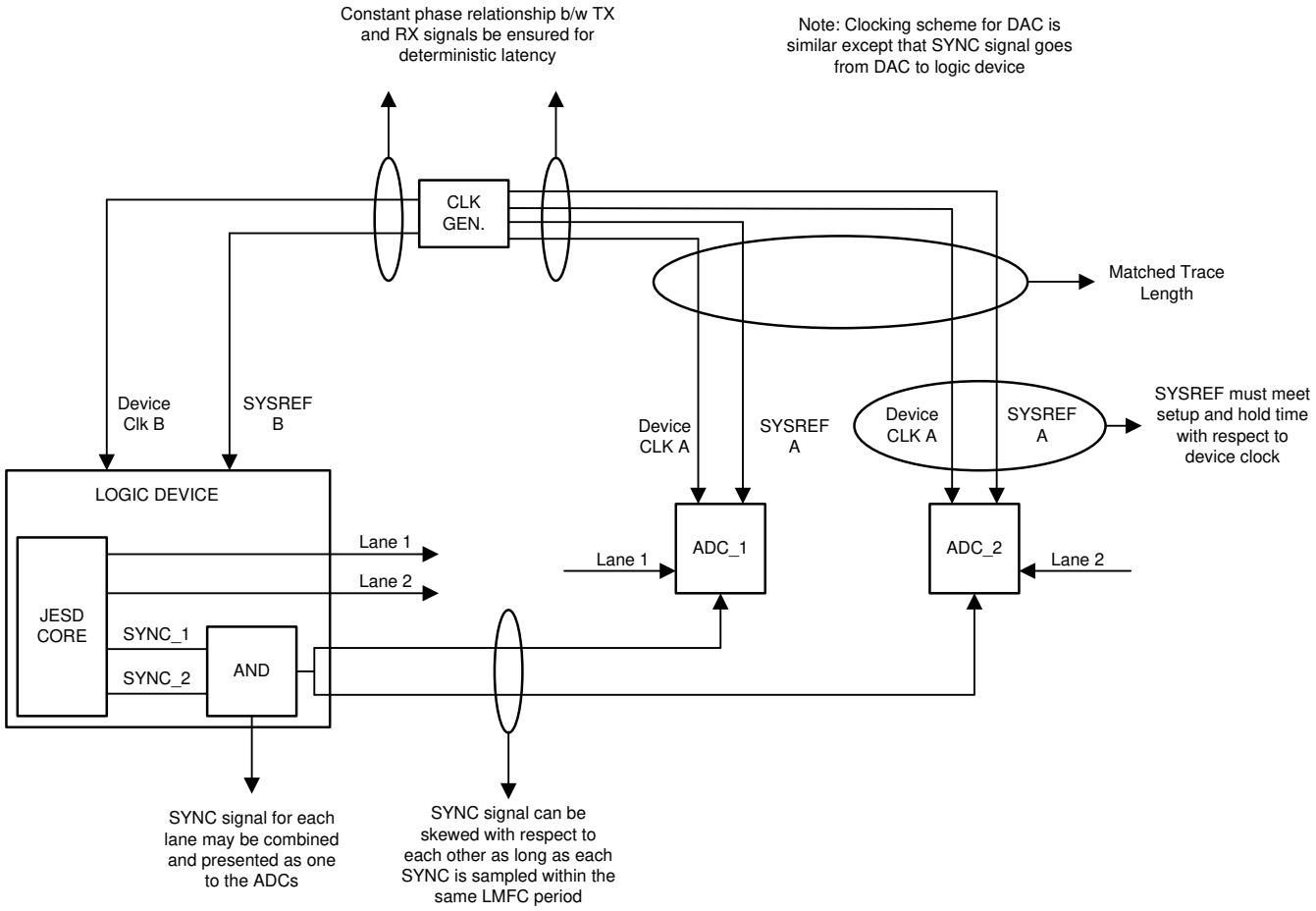


図 2-6. JESD System Level DEVCLK, SYSREF, and SYNC Interface

- Choose the appropriate elastic buffer release points in the JESD204B receivers to guarantee deterministic latency.

The TIDA-01022 reference design addresses these requirements for achieving deterministic latency and a minimum channel-to-channel skew. See the following resource for more details: *JESD204B Deterministic Latency*.

2.4.4 Analog Front End

The front-end analog signal chain determines the performance in a multichannel receiver or data capture system, for which the SNR and SFDR are critical. The front-end gain and the attenuation block over the input signal bandwidth determine the overall system dynamic range.

図 2-7 shows the typical AFE block for a high-speed digitizer and DSO. The front end contains a preamplifier, analog- or digital-variable gain amplifier (DVGA), and a multiple-order band-pass filter. The preamplifer and DVGA determine the system dynamic range and the filter improves the system harmonic distortion of a single-tone frequency. The signal chain SNR is designed such that it is greater than 10 dB of the ADC SNR.

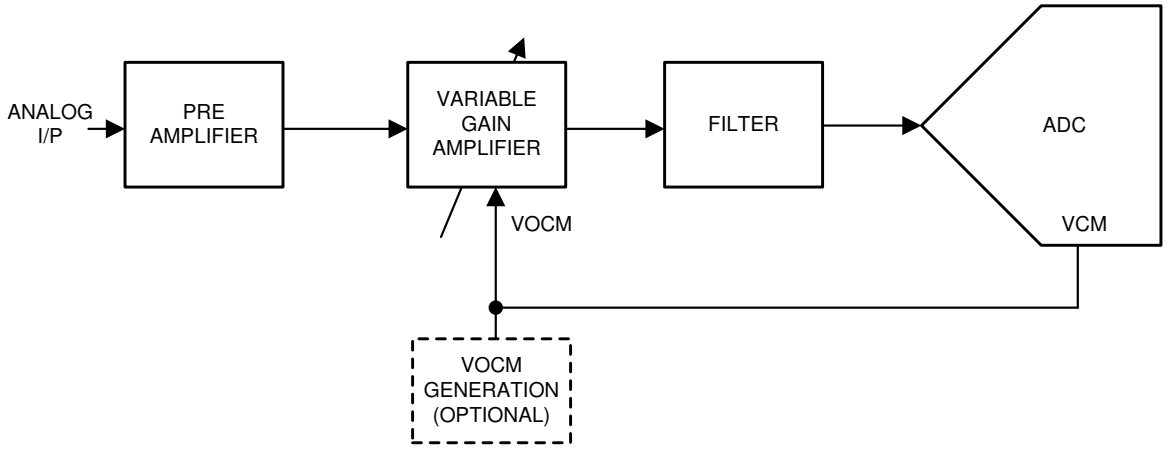


図 2-7. Typical AFE

Ensure that the front end is properly biased to achieve the ADC-rated performance at the full-scale input. The integrated buffer of the ADC has a common-mode bias output that the user can implement to directly drive the front-end amplifier without requiring an external circuit. The inputs of the unbuffered ADC require an external bias, which the designer can generate using various methods. This bias voltage is typically half of the supply voltage, so a simple resistor divider is enough to generate this external bias. See the relevant device data sheets for the recommended VCM generation guidelines.

A failure to maintain the common-mode voltage leads to ADC offset and gain error, which degrade the full-scale dynamic performance of the system.

2.4.5 Multichannel System Power Requirement

A typical multichannel system requires multiple rails to power the analog-, digital-, and mixed-signal circuits. The total system power requirement increases depending on the number of channels required. 図 2-8 and 図 2-9 show the power supply trees for a typical multichannel system and subsystem.

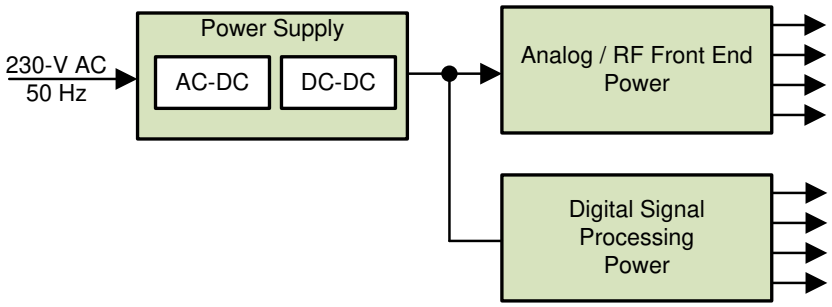


図 2-8. System Power Supply

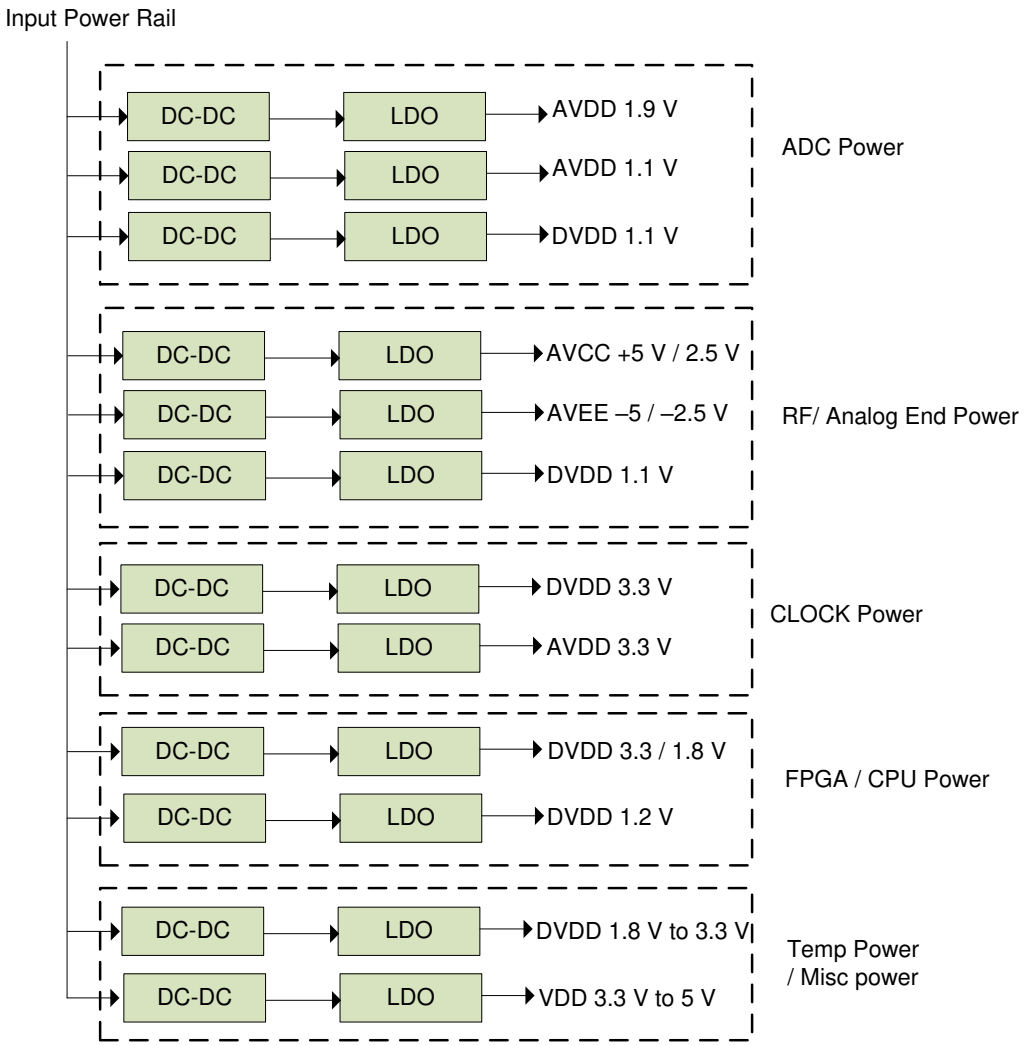


図 2-9. Subsystem Power Rails

To improve system efficiency, downconvert the input DC rail using a DC-DC buck switching regulator and then regulate the voltage using an LDO. The ripple and noise are critical in RF or analog subsystems where low-ripple LDOs are in use. Depending on the system requirements, digital subsystems such as field-programmable gate arrays (FPGAs) or central processing units (CPUs) receive power directly from a switching regulator or through LDOs.

2.4.6 Hardware Programming

The TIDA-01022 hardware has an onboard FTDI-brand USB controller, which is for programming the LMK61E2, LMK4828, and LMX2594 clocking devices and the LMH6401 amplifier using an SPI or I^2C interface. The High-Speed Data Converter (HSDC TID) graphical user interface (GUI) supports low-level pages, which can be used to program these devices.

The board also features a USB2ANY programming interface, which helps the user to evaluate hardware by using the respective evaluation module (EVM) GUI. 表 2-1 lists the connector details with jumper settings for external programming using the USB2ANY programmer.

表 2-1. External Programming Interface

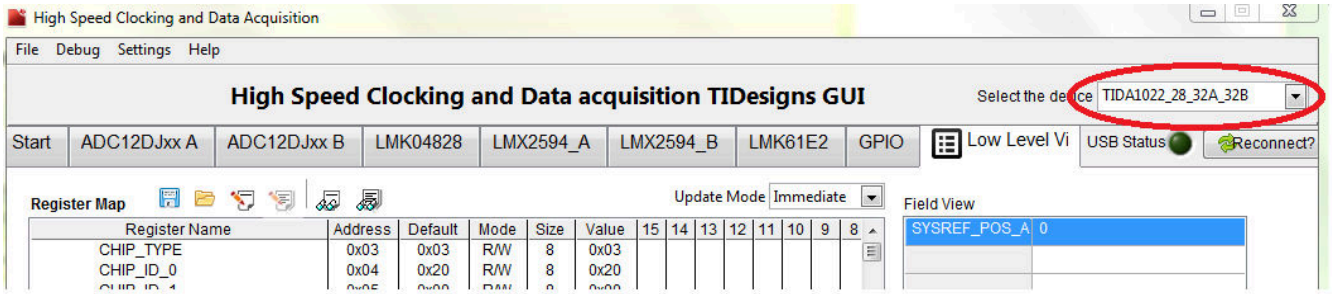
INTERFACE CONNECTOR	MODE SELECTION	INTERFACE	DEVICE REFERENCE	DEVICE	CHIP SELECT
J31	J36 = open J38 = open	SPI	U2, U5, U11, U14	LMH6401	J34 is used to select chip
J32	—	I^2C	U9, U18, U25	LM95233, LMK61E2	—

表 2-1. External Programming Interface (continued)

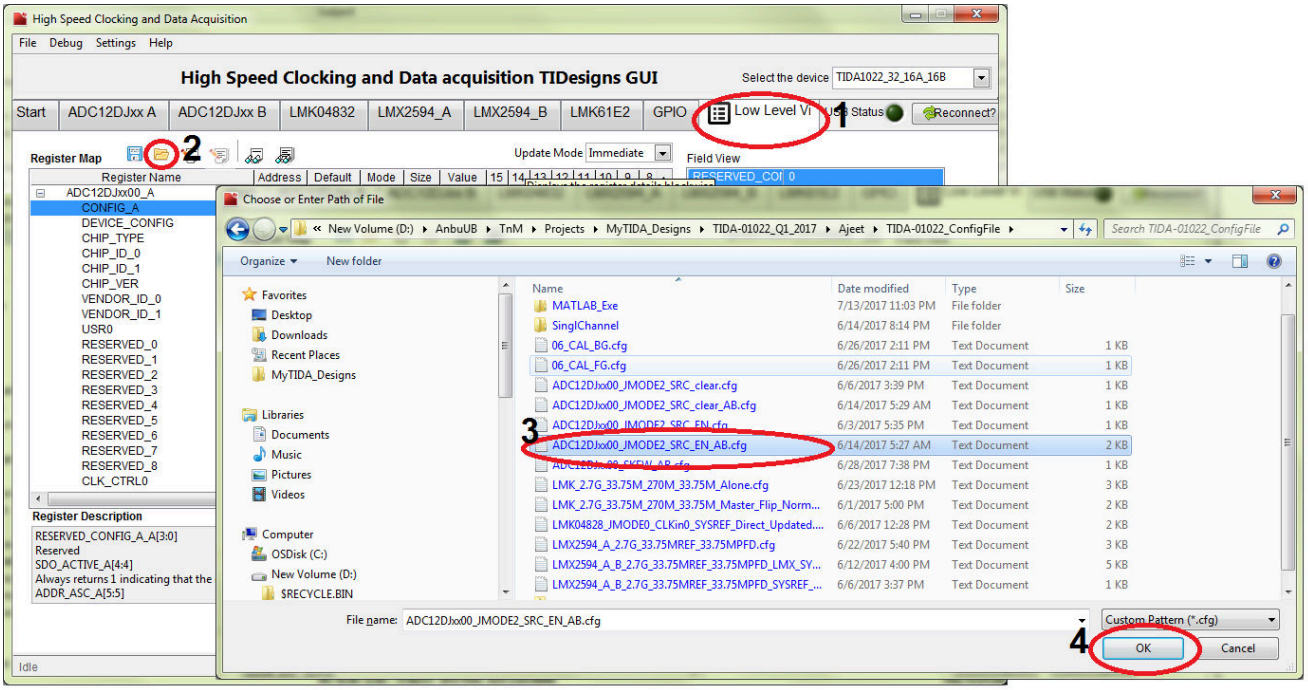
INTERFACE CONNECTOR	MODE SELECTION	INTERFACE	DEVICE REFERENCE	DEVICE	CHIP SELECT
J32	J35 = open J37 = open	SPI	U17, U18	ADC12DJ3200	J33 used to select U17 or U18
J39	Remove resistor R445, R447, R449, R451, R452, R454	SPI	U24A, U19, U21	LMK04828, LMX2594	J40 used to select chip select

The programming procedure for the built-in programming interface is as follows:

1. Open the HSDC TID GUI and select “TIDA1022_28_32A_32B” from the device selection drop-down menu.



2. Navigate to the "Low Level" tab, select the configuration files to be programmed, and click the *OK* button. Follow these steps as numbered and encircled in the following screenshot.



3 Circuit Design

3.1 Analog Input Front End

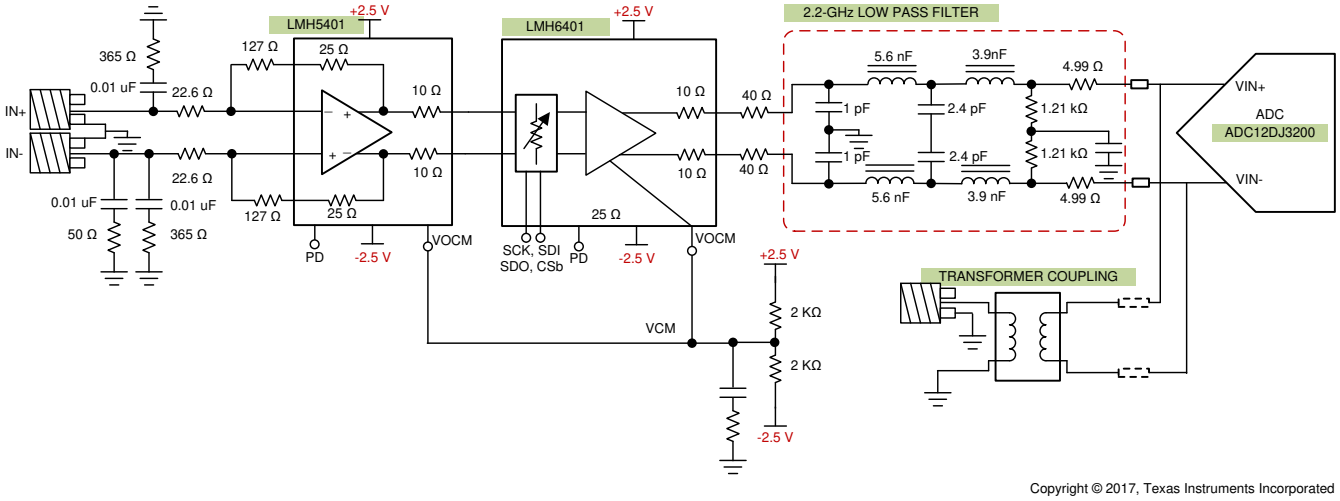
The TIDA-01022 platform has flexible analog inputs to validate system performance with two different input paths:

- Transformer coupling:

  The transformer coupling consists of an onboard Marki balun, which supports a 500-kHz to 6-GHz input bandwidth with 6-dB insertion loss. The transformer coupling functions to validate the ADC12DJ3200 device performance at the AC input signal.
- Fully differential amplifier (LMH5401 + LMH6401):

  The LMH5401+LMH6401 path that drives the ADC12DJ3200 can either be DC coupled or AC coupled at the inputs. A typical DC-coupled configuration uses an LMH6401 device to produce a balanced differential output signal for the ADC12DJ3200 input. In general, the use of transformers is to provide SE-DE conversion; however, these transformers are inherently band-pass in nature and are not for use in DC-coupled applications. As a result, a common solution is to use a high-speed amplifier to enable DC-coupling without affecting the ADC performance at higher frequencies. Amplifiers offer a flexible and cost-effective solution when the application requires gain, a flat pass-band with low ripple, DC-level shifts, or a DC-coupled signal path. To DC couple the LMH6401 input path, take care to ensure that the common-mode voltage is set within the input common-mode range of the LMH6401 device.

図 3-1 shows the design AFE, which is capable of supporting both AC and DC applications for use in a high-performance digital oscilloscope, direct RF input, multichannel radar, and 5G wireless tester. The front-end design consists of a combination of LMH5401 and LMH6401 devices in cascade mode. In the TIDA-01022 reference design, the LMH5401 device is SE-DE configured to accept 50-Ω input signals. The LMH5401 output drives the LMH6401 (DVGA) for the precise gain adjustment which, in turn, drives a fifth-order 2.2-GHz low-pass filter. An ADC (ADC12DJ3200) digitizes the filtered signal output.



Copyright © 2017, Texas Instruments Incorporated

図 3-1. TIDA-01022 AFE

In the first stage of this cascade configuration, the LMH5401 device presents a gain of 4 V/V (12 dB). However, the highest signal bandwidth is 6 GHz in an SE-DE configuration. The 3-dB bandwidth of the LMH6401 is 4.5 GHz, which limits the overall signal bandwidth and allows it to function as a low-pass filter to filter out the harmonics of LMH5401. The LMH6401 gain ranges from –6 dB to 26 dB in 1-dB steps and achieves a 32-dB dynamic range. The LMH6401 device exhibits constant input impedance across the gain setting, which makes it suitable for driving a wideband data converter.

A ±2.5-V dual power supply provides power to both of the LMH5401 and LMH6401 devices. The ADC12DJ3200 requires a zero common-mode input voltage, which the simple resistor divider circuit generates. See the detailed design procedure and calculation for cascaded LMH5401+LMH6401 amplifiers in *Cascaded LMH5401 and LMH6401 Reference Design*.

3.1.1 High-Input Impedance Buffer Implementation Using the BUF802

This reference design focuses on design of an analog front end with 50-Ω input as previously discussed, however in some use cases like that of DSO it is often desired to have a capability of a high-input impedance input to the tune of 1 MΩ. BUF802 helps implement this requirement by use of a JFET input unity gain buffer.

Data acquisition systems that require a high-input impedance mode usually follow one of two approaches; a custom front-end ASIC or a discrete JFET implementation. Either of these approaches incur either a high cost of developing and manufacturing a custom ASIC or a complex discrete circuit that comes with its own set of design challenges. The BUF802 provides a single chip alternative to both ASIC and FET-based implementations by providing an all-in-one solution that provides a simpler and more cost-effective solution without sacrificing performance.

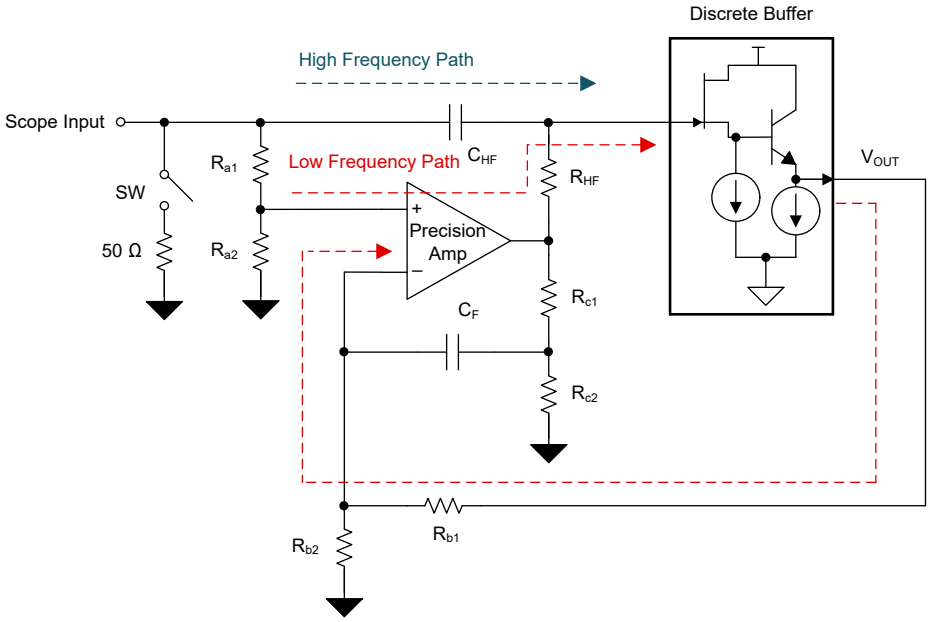


図 3-2. Discrete JFET Architecture

The typical discrete implementation, Figure 3-2, uses a precision amplifier and a discrete JFET configured in a composite loop. The purpose of the composite loop architecture is to split the input signal into low- and high-frequency signal paths, pushing through two different circuits and recombining them at the output. One of the main challenges with the composite loop architecture shown in Figure 3-3 is achieving smooth interleaving of the two paths to ensure a flat frequency response. Any mismatch in the transfer function of the two paths leads to discontinuity in the net transfer function frequency response resulting in a loss of signal fidelity, see 図 3-3.

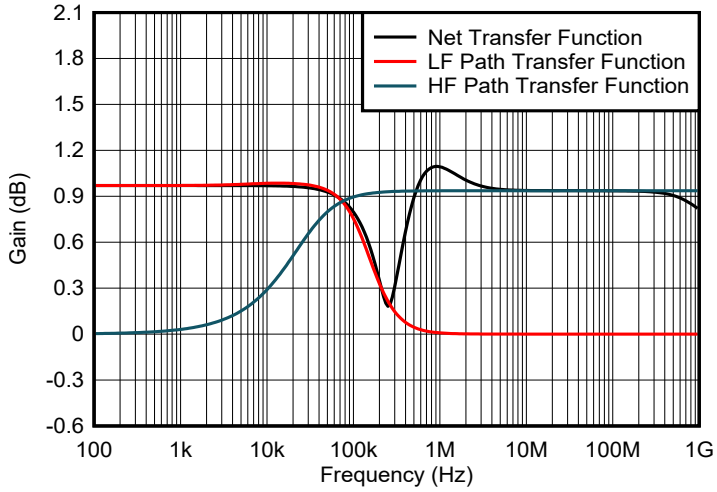


図 3-3. Crossover Frequency Region

Additional drawbacks with implementing a discrete design include, but are not limited to: dealing with a complex system response, higher supply rails, component and channel mismatch, additional compensating for input and output protection. For a more in-depth look on discrete design challenges and how the BUF802 helps overcome these problems, see the *Simplify analog front-end designs with Hi-Z buffers* E2E™ forum.

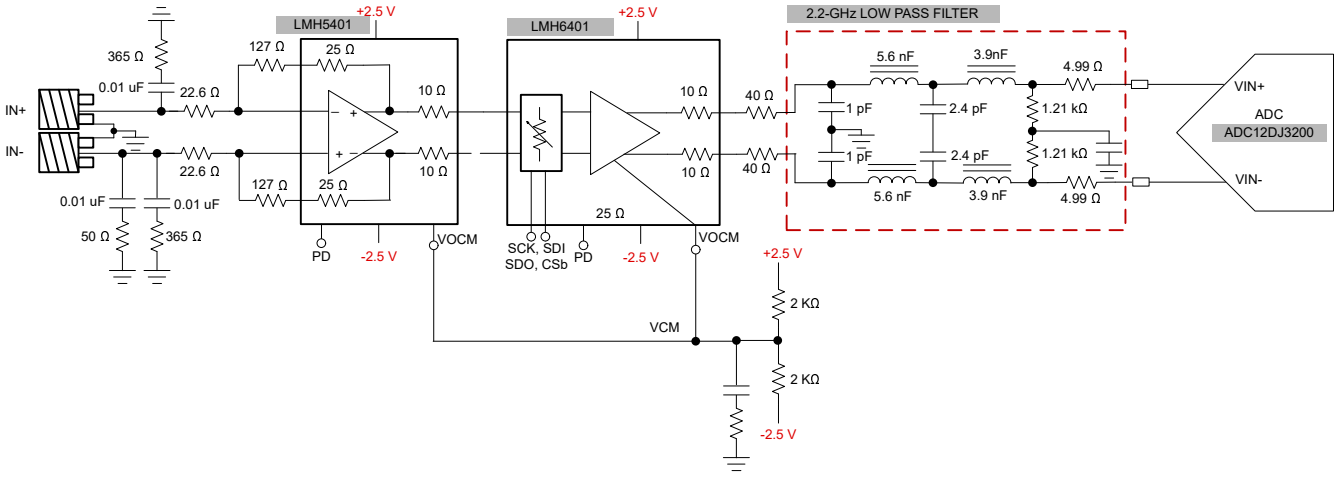


図 3-4. TIDA-01022 Analog Front End

Figure 3-4 shows the TIDA-01022 fully differential AFE that is configured for a 1.5-GHz BW (bandwidth) application and a 50-Ω input impedance. In the default configuration the AFE cannot be used to achieve high-Z mode for lower frequencies. By implementing the BUF802 composite loop at the beginning of the AFE signal chain, the functionality of a high-input impedance mode can be added.

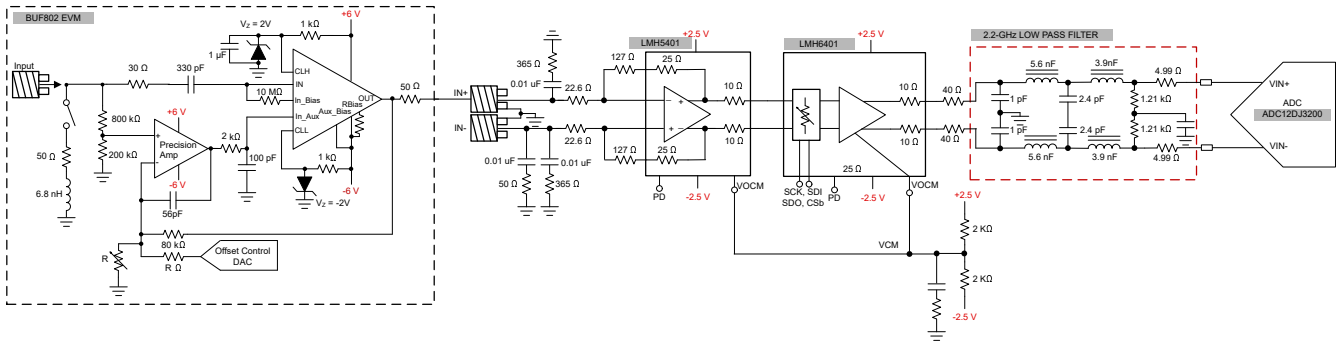


図 3-5. Analog Front End With BUF802

Figure 3-5 features a 1-GHz front-end design incorporating the BUF802 to the existing reference design. Adding the BUF802 into the signal chain provides the system with a high input impedance of 50 GΩ || 2.4 pF, while maintaining the performance of the original design up to 1 GHz. The ability to switch between high-Z and 50-Ω impedance mode is achieved with a switch or relay at the input.

Using the BUF802 EVM and the TIDA-01022 hardware, the performance of the signal chain with and without the BUF802 can be measured. 図 3-6 through 図 3-8 show different performance metrics.

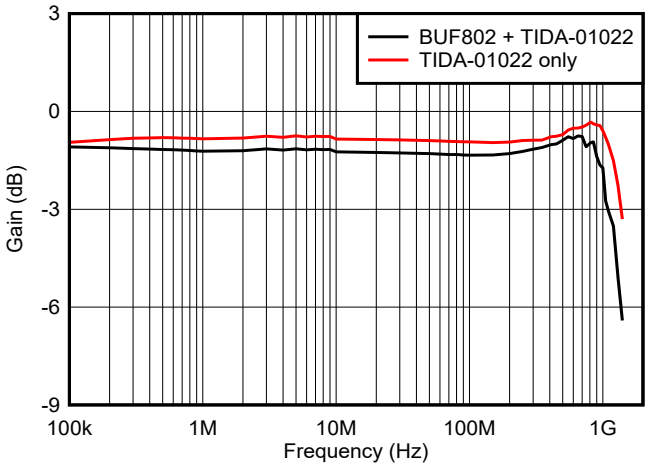


図 3-6. Frequency Response Comparison

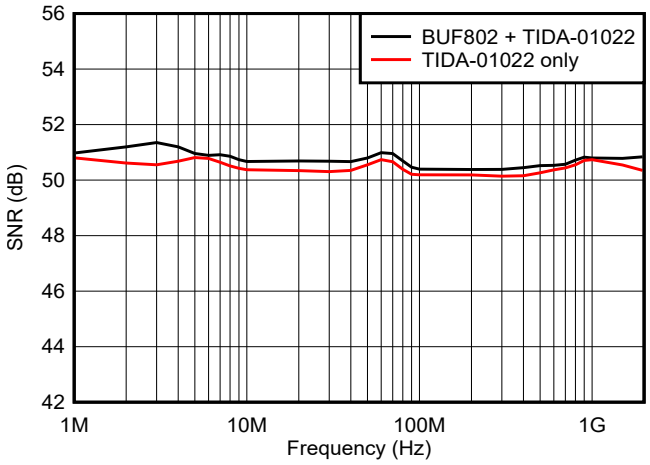


図 3-7. Signal-to-Noise Ration (SNR) vs Frequency

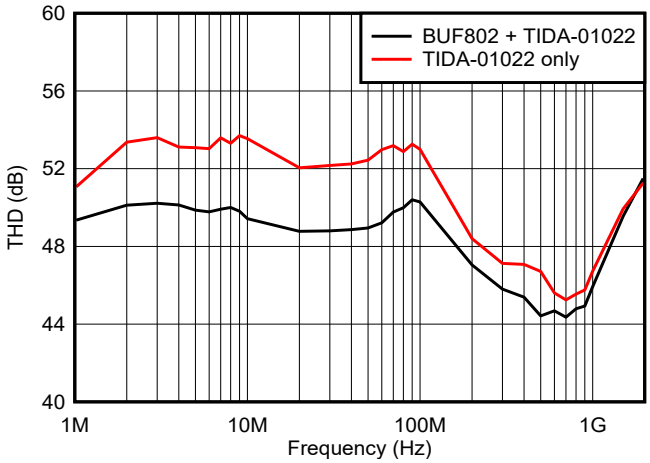


図 3-8. Total Harmonic Distortion (THD) vs Frequency

3.2 High-Speed Multichannel Clocking

図 3-9 shows the clock tree of the TIDA-01022 design. The clock source is an essential component in signal chain design, specifically when driving the ADC sample clock. Clock jitter directly impacts ADC SNR performance and becomes proportionally greater at higher input signal frequencies. When clocking multiple channels, channel-to-channel skew is an important design consideration. Clock jitter and phase mismatch leads to deviation from the ideal sampling instant of a channel, which results in channel-to-channel skew. The LMX2594 synthesizers that this design uses have an excellent phase noise performance at high frequencies, which brings down the clock jitter to approximately 45 fs. Additionally, the phase synchronization feature of the LMX2594 helps to improve the channel-to-channel skew.

This flexible clocking platform helps the designer validate system performance with various input clock paths and sources. The TIDA-01022 design has three different clocking features to clock the ADC12DJ3200 device using any one of the clocking devices such as the LMK4828, LMX2594, and external clock input. In this design, the LMK4828 device is configured in distribution mode and generates the 33.75-MHz reference clock for the LMX2594 device and FPGA_SYSREF signal. The LMK4828 divider also generates 270-MHz FPGA clocks for FPGA DCLK, FPGA CORE CLK, and 33.75 MHz for the TSW14J56 capture card.

The output of the LMK4828 drives the clock buffer to distribute the reference to two LMX2594 devices, at which point both LMX devices are running in dual PLL mode to generate a low-phase noise clock of 2700 MHz for DEVCLK and a 33.75-MHz SYSREF for the ADC (ADC12DJ3200).

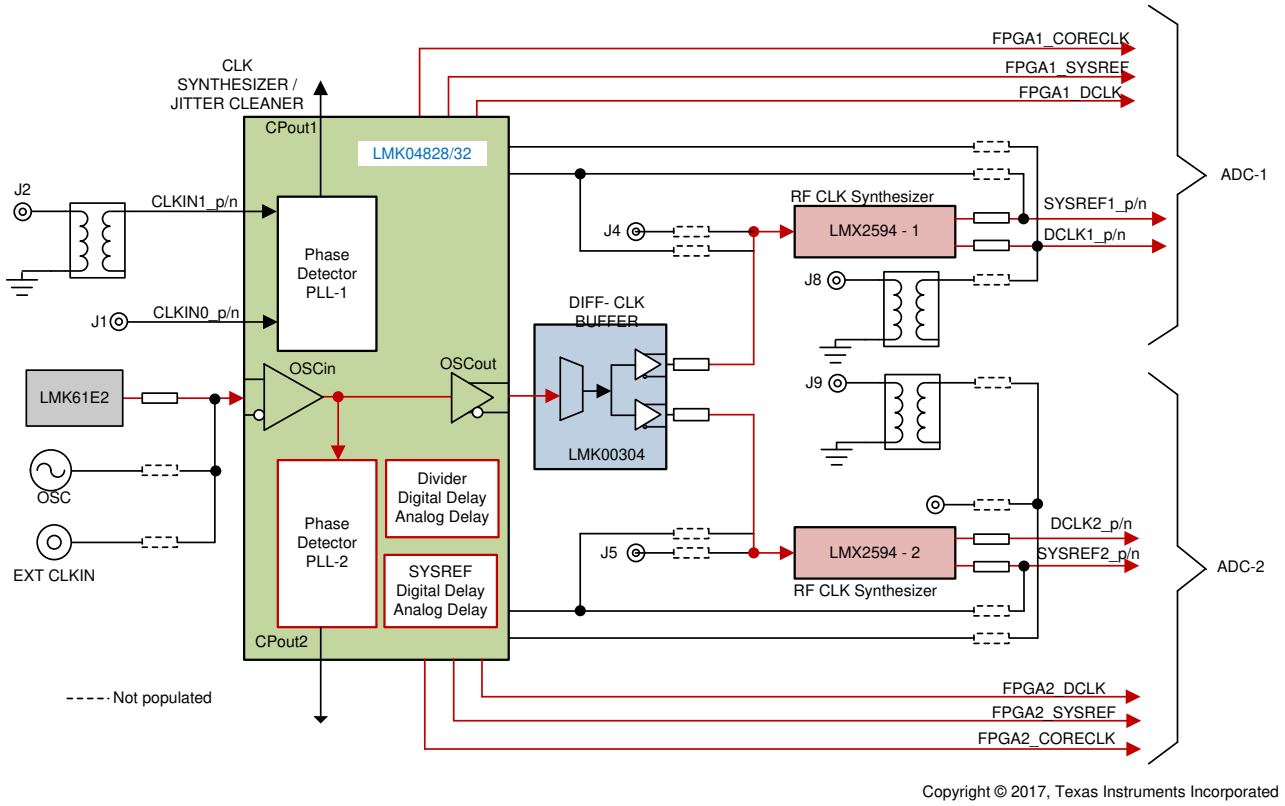


図 3-9. TIDA-01022 Clock Tree

3.3 Power Supply Section

図 3-10 shows the power supply tree of the reference design. The design requires an external +12-V DC power to generate 1.9 V and 1.1 V for the ADC; 3.3 V for the clocking devices (LMK61E2, LMK4828, and LMX2594); and ±2.5 V for the LMH5401 and LMH6401 amplifiers. This design has input overvoltage, overcurrent, high inrush current protection through eFuse (TPS259261), and an external bidirectional transient-voltage-suppression (TVS) diode (SMBJ15CA).

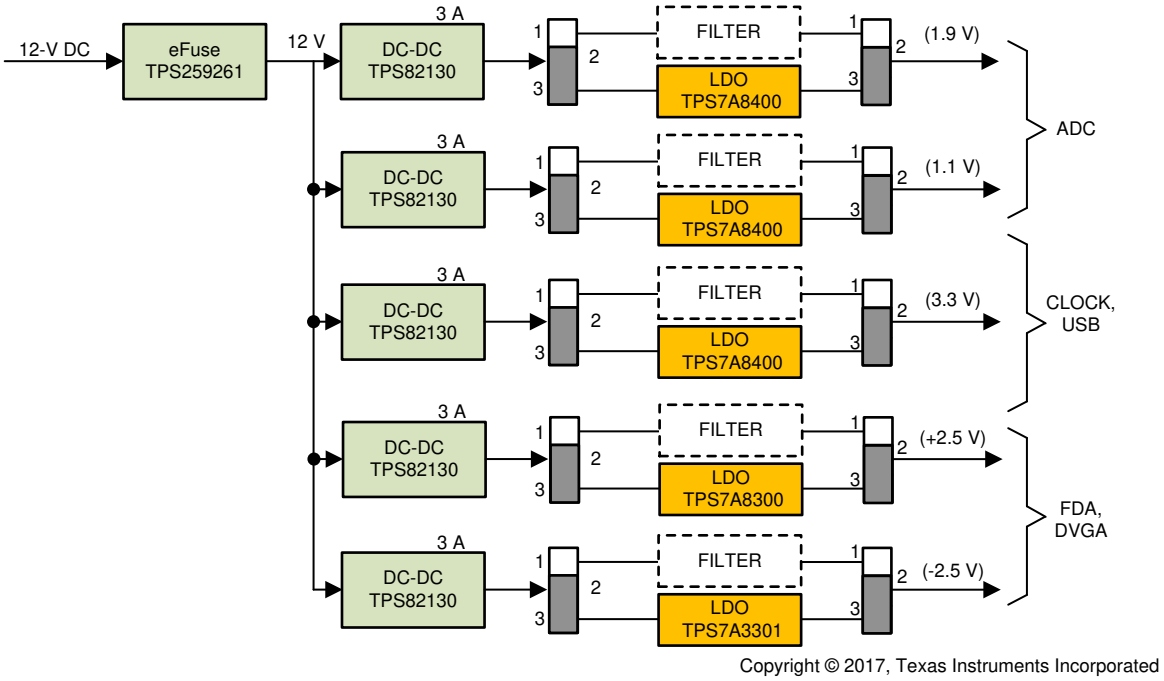


図 3-10. TIDA-01022 Power Supply Block

The DC-DC converter and LDO generate the power supply rail, as 表 3-1 details.

表 3-1. Power Supply Rail

SI NUMBER	TYPE	PART NUMBER	SUPPLY RAIL
1	DC-DC	TPS82130	Intermediate rails for 3.3 V, 1.9 V, and 1.1 V
2	LDO	TPS7A8400	3.3 V, 1.9 V, and 1.1 V
3	LDO	TPS7A8300	+2.5 V
4	LDO	TPS7A3301	–2.5 V

The following subsections detail the design procedure for the various power supply rails.

3.3.1 DC-DC

The TPS82130 is a 3-A step downconverter MicroSiP™ module with an integrated inductor that accepts a 3- to 17-V DC input and delivers a 0.9- to 6-V output with high efficiency. The LDO requires a minimum 2.1-V input voltage to generate 1.9 V. 図 3-11 shows a circuit diagram of the 2.1-V generation.

3.3.1.1 How to Set 2.1-V Output Voltage

Use resistor R_{FBT} (R491) and R_{FBB} (R492) to determine the output voltage of the TPS82130 device, as the following 式 1 through 式 3 show.

$$\frac{R_{FBT}}{R_{FBB}} = \left(\frac{2.15}{0.8}\right) - 1 \tag{1}$$

$$\frac{R_{FBT}}{R_{FBB}} = 1.687 \tag{2}$$

$$R_{FBT} = \frac{13700}{1687} = 8118\ \Omega \tag{3}$$

Based on these calculations, the nearest values chosen are R491 = 13.7 kΩ and R492 = 8.06 kΩ.

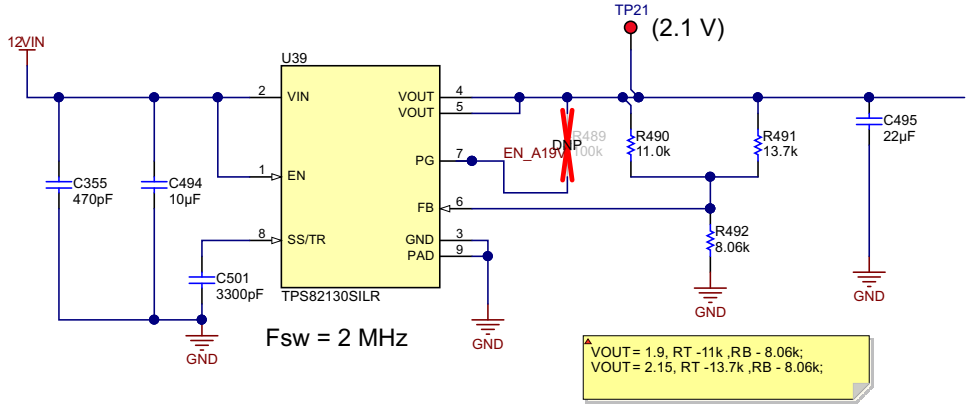


図 3-11. DC-DC Power Supply

表 3-2 lists the values for the other intermediate power rails, which DC-DC TPS82130 converter generates.

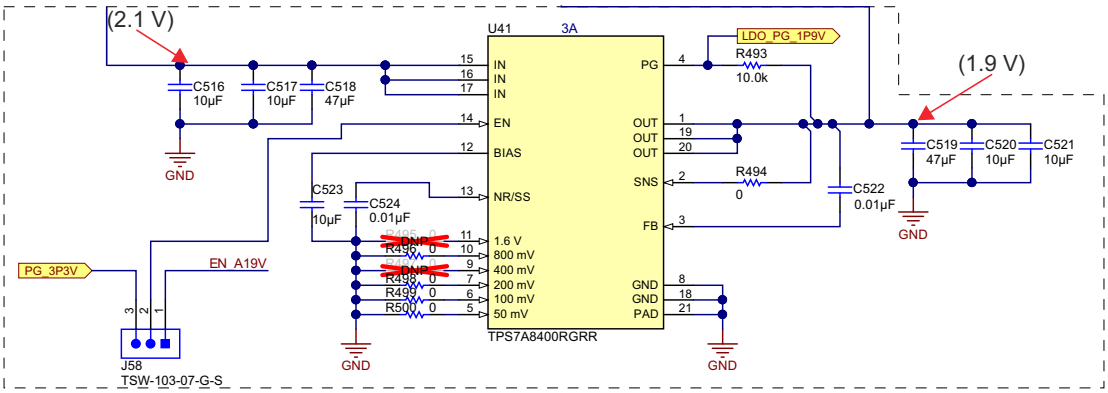
表 3-2. Intermediate Power Rail

SI NUMBER	OUTPUT POWER RAIL	INTERMEDIATE POWER RAIL
1	1.9 V	2.15 V
2	1.1 V	1.35 V
3	3.3 V	3.55 V
4	+2.5 V	3.00 V
5	–2.5 V	–3.30 V

3.3.2 LDOs

The TPS7A8400 is a positive-voltage (5-V), ultra-low-noise (4.4-μV_{RMS}) LDO capable of sourcing a 3-A load with a low drop of 180 mV (see 図 3-12). The TPS7A8x00 is designed primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers (op amps), ADCs, DACs, and other high-performance analog circuitry.

The TPS7A8400 has ANY-OUT™ programmable pins to program the desired output voltage. The sum of the internal reference voltage (V_{REF} = 0.8 V) plus the accumulated sum of the respective voltage is assigned to each active pin. The ANY-OUT pins (pins 10, 7, and 6) are programmed to active low to obtain 1.9 V at the output. Other positive rails (1.1 V, 3.3 V, and 2.5 V) are similarly generated.



$V_{OUT(NOM)}$ (V)	50 mV	100 mV	200 mV	400 mV	800 mV	1.6 V
1.90	Open	GND	GND	Open	GND	Open

図 3-12. LDO Power Supply Circuit (1.9-V Rail)

The TPS7A33 series of linear regulators are negative voltage (–36 V), ultra-low-noise (16-μV_{RMS}, 72-dB power supply rejection ratio (PSRR)) linear regulators capable of sourcing a maximum load of 1 A. The output set resistors generate the –2.5 V.

4 Host Interface

Evaluate the design system performance using TI's TSW14J56 JESD204B high-speed data capture and pattern generator card. Using Altera FPGA JESD204B intellectual property (IP) cores, the TSW14J56 is dynamically configurable to support lane speeds from 600 Mbps to 12.5 Gbps, from one to eight lanes, 1 to 16 converters, and 1 to 4 octets per frame with one firmware build. Together with the accompanying HSDC Pro GUI, the TSW14J56 is a complete system that captures and evaluates data samples from the TIDA-01022 design. The TIDA-01022 design can interface with the TSW14J56 EVM by using an FMC+ to FMC adapter PCB.

For more information on the TSW14J56 EVM, see *TSW14J56 JESD204B High-Speed Data Capture/ Pattern Generator Card User's Guide*.

5 Hardware Functional Block

図 5-1 shows the various hardware functional blocks of the TIDA-01022 design and the function of each block:

1. A 12-V DC power supply input connector accepts the 9- to 12-V DC input to power the TIDA-01022
2. Power supply section has switching regulator (DC-DC) and LDOs to generate multiple rails (1.1 V, 1.9 V, 3.3 V, +2.5 V, and –2.5 V) from the 12-V input
3. Four analog input channels which the designer can configure to accept 50-Ω single-ended or differential inputs
4. AFE block contains combination of LMH5401+LMH6401, which accepts both AC and DC coupled inputs up to 1.5 GHz; optional transformer-coupled inputs are also available for an AC-coupled application up to 6 GHz
5. FMC+ connector interfaces with TI High-Speed Data Capture card to the TSW14J56 using an FMC+ to FMC adapter PCB
6. Clock subblock which contains high-performance clocking solution native to LMK04828, LMK2594, LMK00304, and LMK61E2 clocking devices
7. Mini-USB interface connector helps to configure ADCs and clocking devices for various modes

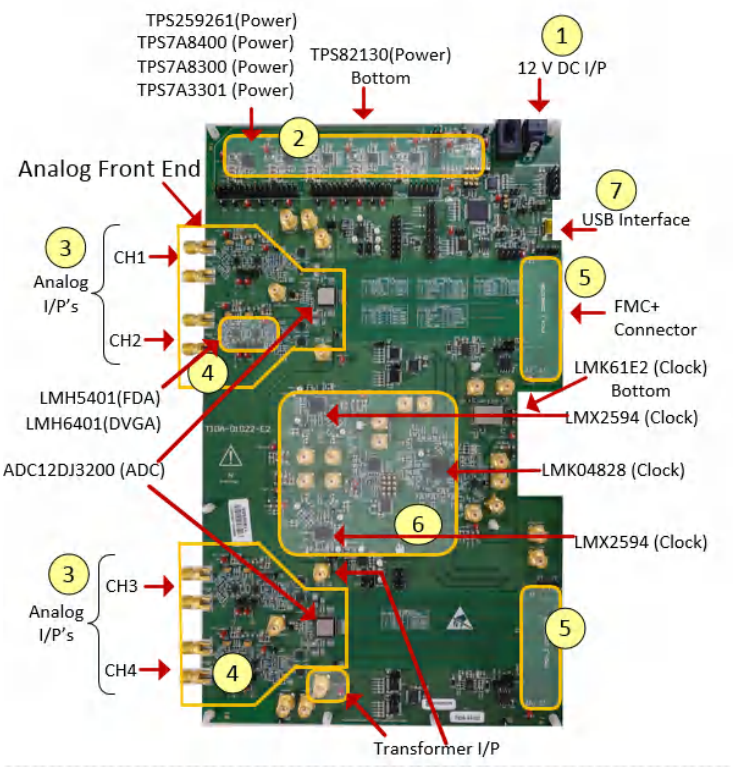


図 5-1. TIDA-01022 Hardware Functional Block

6 Getting Started Application GUI

The TIDA-01022 board requires three application software GUIs for validation: HSDC TID GUI, HSDC Pro GUI, and the LMK61xx Oscillator Programming Tool.

1. Use the HSDC TID GUI to configure the data converter (ADC12DJ3200), clocking devices (LMK4828, LMX2594, and LMK61E2), and digital VGA (LMH6401). Use the low-level page to program the device with the respective configuration file. Download the latest HSDC TID GUI software at: http://www.ti.com/lit/zip/tidcdr5.
2. Use the HSDC Pro GUI to capture the digitized data with the assistance of a TSW14J56 capture card and provide a spectrum and time domain plot. Download the latest HSDC Pro GUI software at: http://www.ti.com/tool/dataconverterpro-sw.
3. Use the LMK61xx Oscillator Programming Tool to program the LMK61E2 device. Download the latest LMK61xx software at http://www.ti.com/lit/zip/snac074.

図 6-1 and 図 6-2 show screenshots of starting the HSDC TID GUI configuration and the programming tab for the low-level view, respectively.

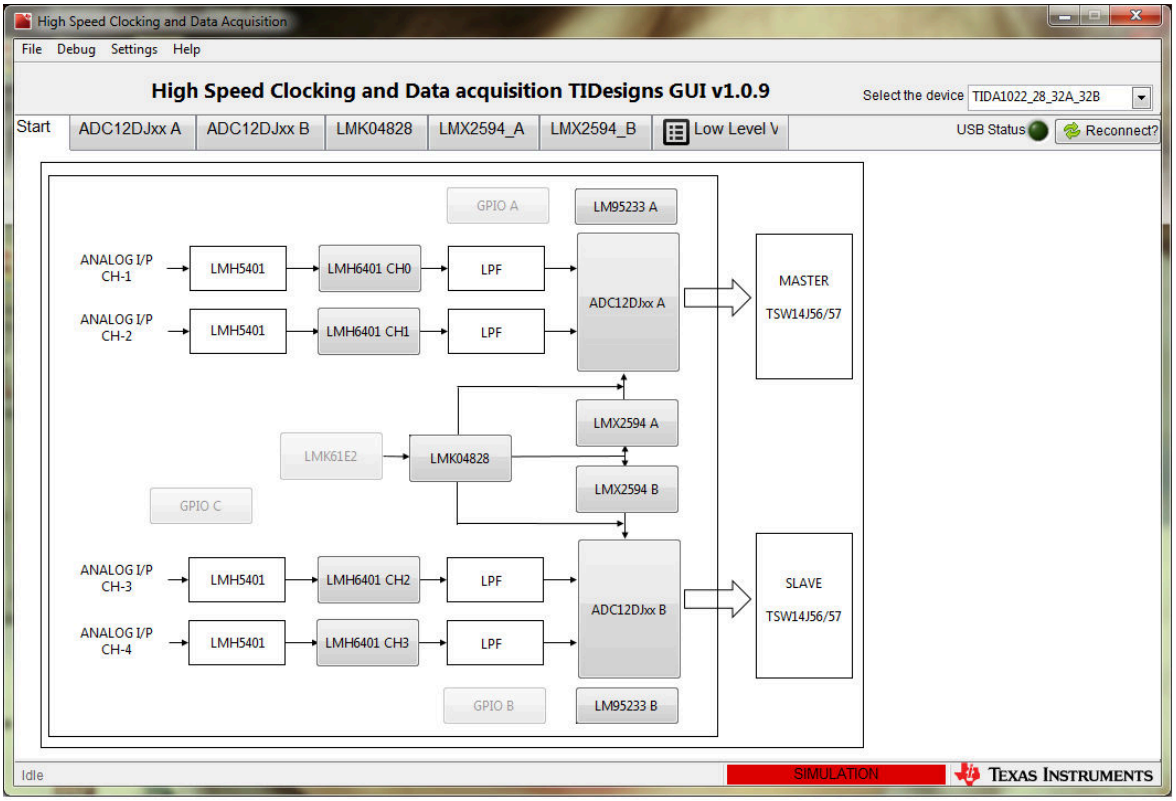


図 6-1. HSDC TID GUI—Top Level Navigation View

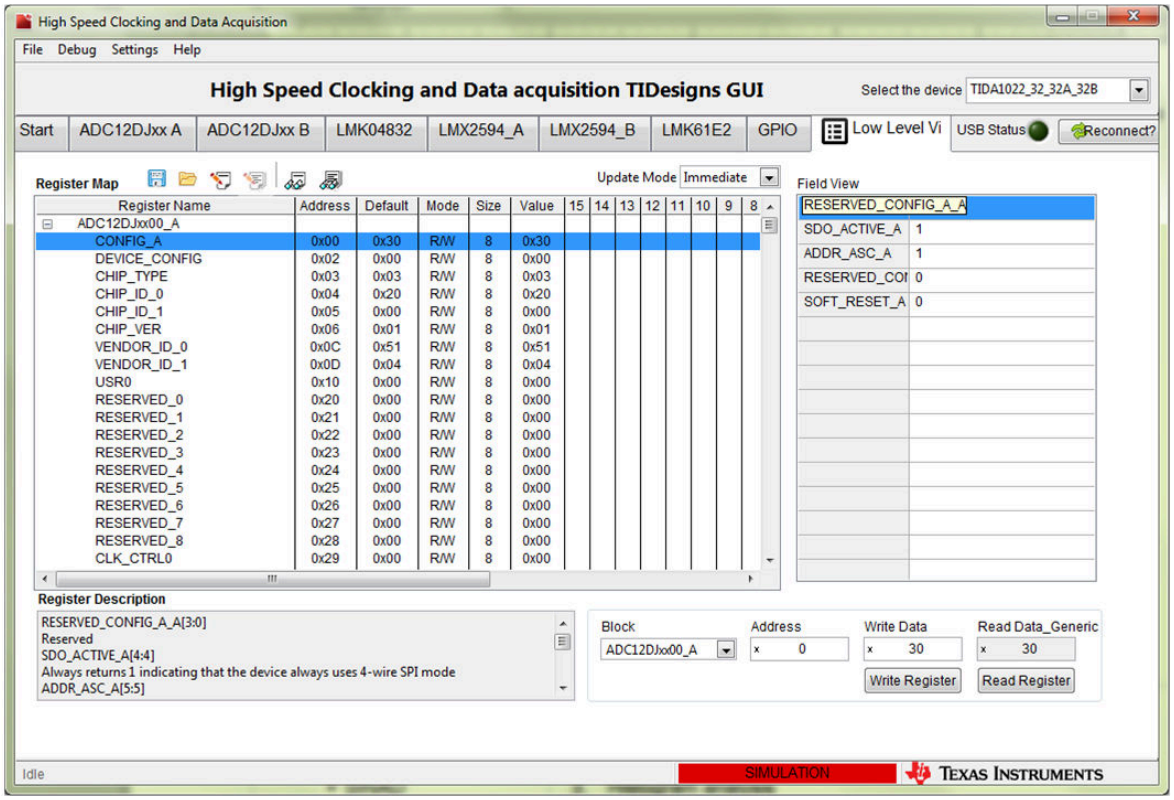


図 6-2. HSDC TID GUI—Low-Level Programming View

図 6-3 shows the ADC capture screen in the HSDC Pro GUI.

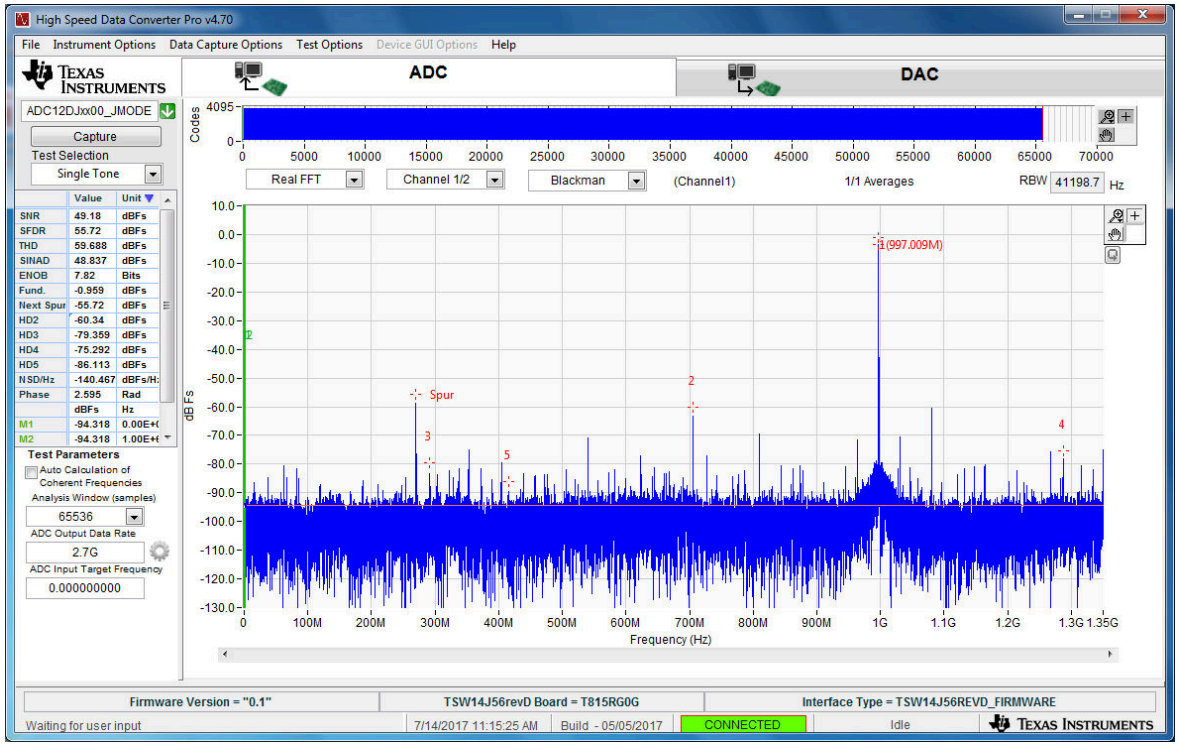


図 6-3. HSDC Pro ADC Capture GUI (Spectrum, Time Domain)

7 Testing and Results

7.1 Test Setup and Test Plan

図 7-1, 図 7-2, and 図 7-3 show the test setup for performing signal chain SNR measurements for the transformer input, the LMH inputs, and the channel-to-channel clock skew, respectively.

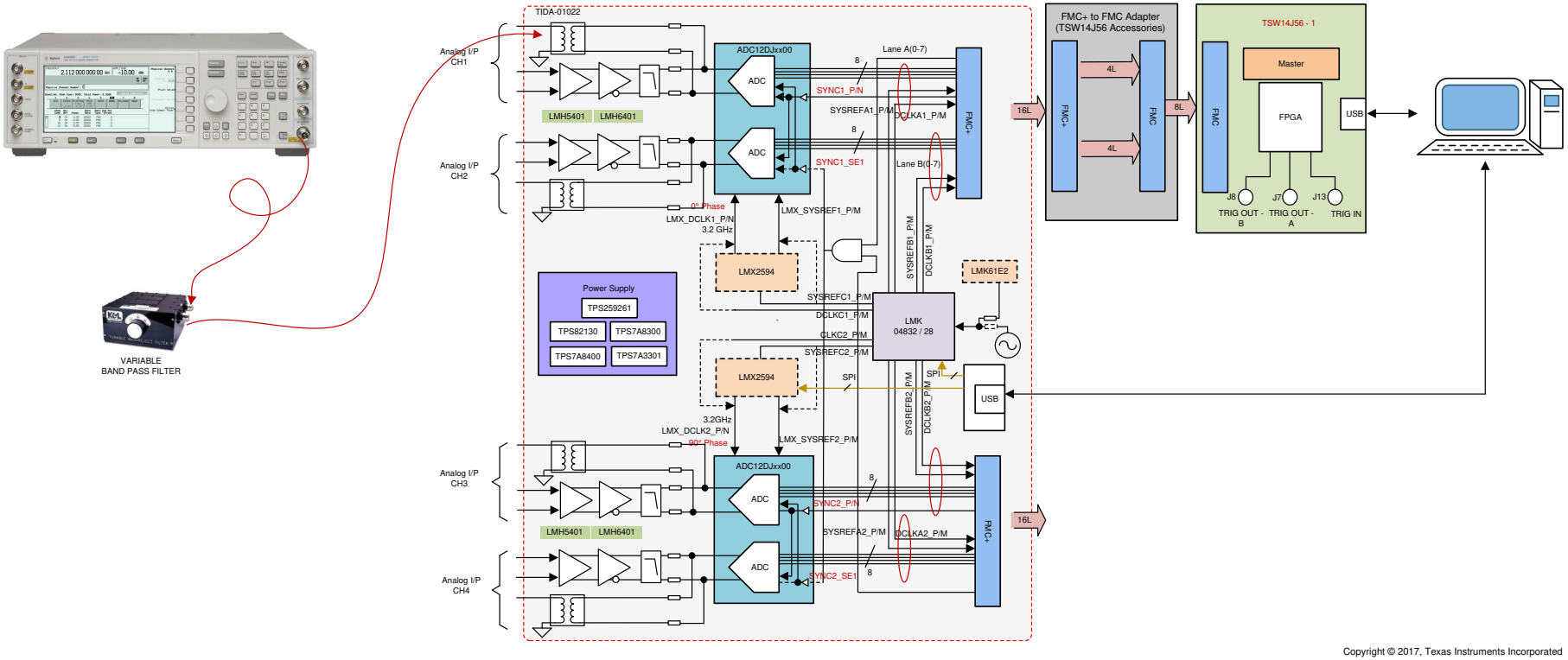


図 7-1. Test Setup for SNR Measurement (Transformer Input)

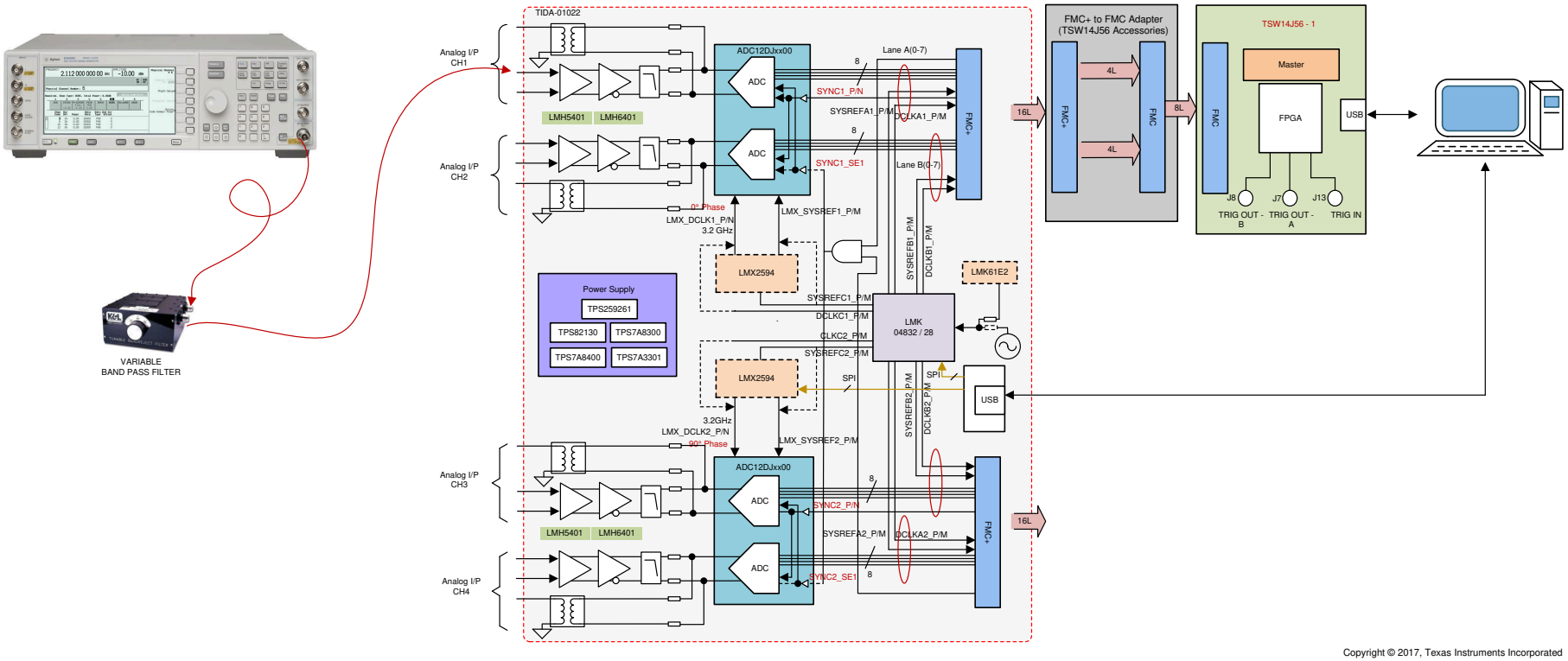


図 7-2. Test Setup for SNR Measurement (LMH6501+LMH5401 Input Path)

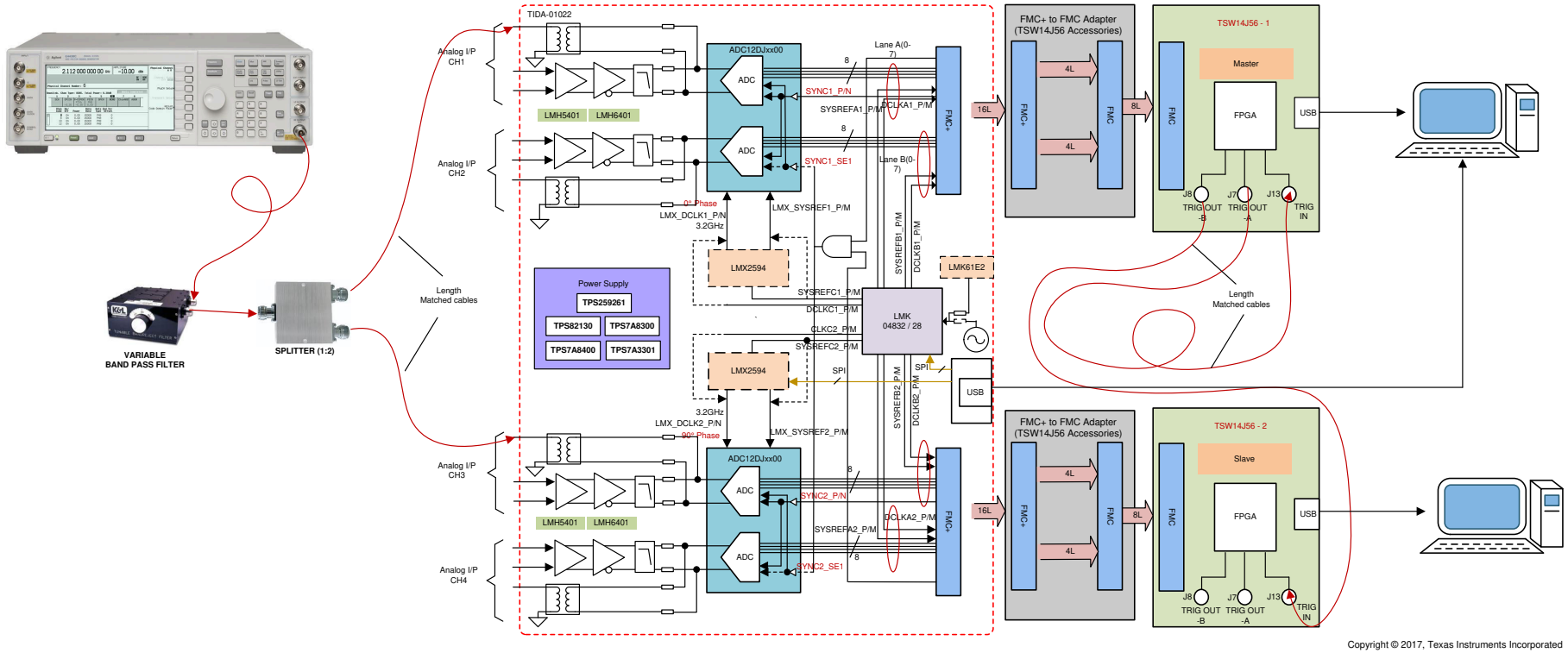


図 7-3. Test Setup for Channel-to-Channel Skew Measurement

表 7-1 shows the analog input types and corresponding resistor jumper configurations.

表 7-1. TIDA-01022 Input Coupling Type Selection

ANALOG INPUTS	INPUT COUPLING	RESISTOR JUMPER SETTING
CH1	Transformer	R551, R552 – Populate
		R592, R604 – Not populated
CH1	FDA	R551, R552 – Not populated
		R592, R604 – Populated
CH2	Transformer	R560, R561 – Populate
		R605, R606 – Not populated
CH2	FDA	R560, R561 – Not populated
		R605, R606 – Populated
CH3	Transformer	R569, R570 – Populate
		R607, R608 – Not populated
CH3	FDA	R569, R570 – Not populated
		R607, R608 – Populated
CH4	Transformer	R578, R579 – Populated
		R609, R610 – Not populated
CH4	FDA	R578, R579 – Not populated
		R609, R610 – Populated

7.2 SNR Measurement Test

The steps for testing the SNR measurement for a 2.7-GHz sample rate are as follows:

1. Emulate the hardware setup as shown in 図 7-1, then provide the input signal to the J12 SMA connector of channel 1 of the TIDA-01022 design through a variable band-pass filter.
2. Connect the high-speed USB3.0 and USB2.0 cables to the capture PC.
3. Provide a 12-V, 4-A DC supply to the power connector of J55 and provide a 5-V supply to the TSW14J56 capture card.

To measure the signal chain SNR, configure the following using the HSDC TID GUI:

1. Use the J32 connector to program the LMK61E2 device at 33.75 MHz using the USB2ANY programmer associated with the LMK61E2 Oscillator Programming Tool. Set the device address as 0x5A before programming.
2. Program the LMK04828 in 0-delay PLL mode at a 33.75-MHz SYSREF frequency to provide the SYSREFREQ and SYNC signals along with this 33.75-MHz OSCout as a reference to the LMX2594.
3. The LMK04828 also generates the FPGA reference at 270 MHz, the FPGA core clock at 270 MHz, and the FPGA SYSREF at 33.75 MHz for the FPGA capture card.
4. Program the LMX2594_A for a 2.7-GHz DEVCLK and SYSREF at 33.75 MHz.
5. Configure ADC12DJ3200 JMODE-2 (dual-channel mode) by loading the configuration file in the low-level page.

Establish the JESD204B link using HSDC Pro GUI:

1. After powering the TSW14J56, establish a connection with the dual-channel mode (JMODE2).
2. Provide the data rate sampling frequency of the ADC output data and the ADC input target frequency.
3. Afer establishing the JESD204B connection, feed the input signal to J12 from the signal generator.
4. Capture the spectrum and note the SNR performance.
5. Repeat the test with different inputs and sampling frequencies and tabulate the results.

Note

The TIDA-01022 design folder contains the necessary configuration files for generating the different sample rates: 2.7 GHz and 3 GHz.

7.3 Channel-to-Channel Skew Measurement Test

The steps for testing the channel-to-channel skew measurement are as follows:

1. Emulate the hardware setup as shown in 図 7-3, then provide the input signal to the J12 and J29 SMA connectors of channel 1 and 3 of the TIDA-01022 design through a variable band-pass filter and 2:1 splitter.
2. Connect the high-speed USB3.0 and USB2.0 cables to the capture PCs.
3. Configure the TSW14J56 capture card as master and slave configuration mode:
   - Connect the master TSW14J56, J7 (TRIG OUT –A) to J13 (TRIG IN) using a high-speed SMA cable for master self-triggering.
   - Connect the master TSW14J56, J8 (TRIG OUT –B) to J13 (TRIG IN) of the slave TSW14J56 module using a high-speed SMA cable.
4. Provide a 12-V, 4-A DC supply to the power connector (J55) of TIDA-01022 and provide a 5-V supply to the TSW14J56 capture card.

Note

As 図 7-3 shows, the length of the cable must be length matched

To measure the multichannel skew, configure the following using the HSDC TID GUI:

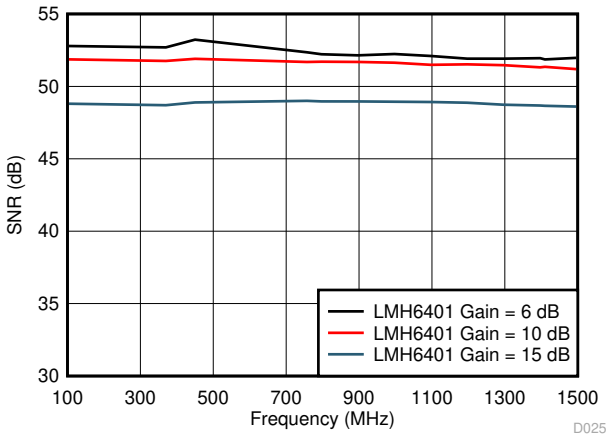
1. Use the J32 connector to program the LMK61E2 device at 33.75 MHz using the USB2ANY programmer associated with the LMK61E2 Oscillator Programming Tool. Set the device address as 0x5A before programming.
2. Program the LMK04828 in 0-delay PLL mode at a 33.75-MHz SYSREF frequency to provide the SYSREFREQ and SYNC signals along with this 33.75-MHz OSCout as a reference to the LMX2594.
3. The LMK04828 also generates the FPGA reference at 270 MHz, the FPGA core clock at 270 MHz, and the FPGA SYSREF at 33.75 MHz for the FPGA capture card.
4. Program the LMX2594_A and LMX2594_B for a 2.7-GHz DEVCLK and 33.75-MHz SYSREF at 33.75 MHz.
5. Configure ADC12DJ3200 JMODE-2 (dual-channel mode) by loading the configuration file in the low-level page.

Establish the JESD204B link using HSDC Pro GUI:

1. After powering the TSW14J56, establish a connection with the dual-channel mode (JMODE2).
2. Provide the data rate sampling frequency of the ADC output and the ADC input target frequency.
3. After establishing the JESD204B connection, feed the input signal to channel 1 (J13) and channel 3 (J76).
4. Apply a trigger at the slave capture board and then click the capture button on the master board.
5. Export both ADC1 and ADC2 data then extract the phase and amplitude information from the spectrum using the MathLab® program and plot the data in the time domain for a channel-to-channel skew measurement.

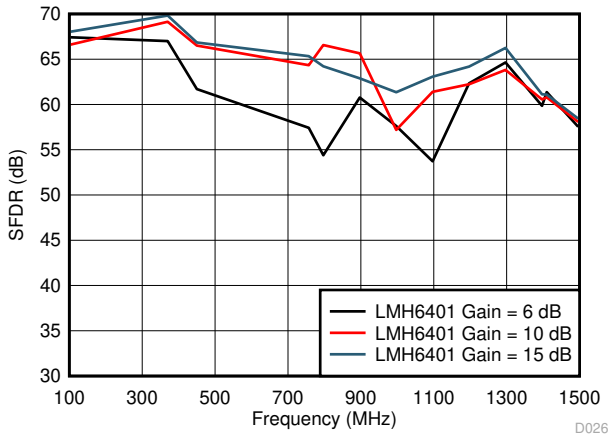
7.4 Performance Test Result

図 7-4, 図 7-5, and 図 7-6 show the analog signal chain performance of the cascaded LMH5401+LMH6401 path. 図 7-7 shows the transformer coupling input performance with the ADC12DJ3200 ADC.



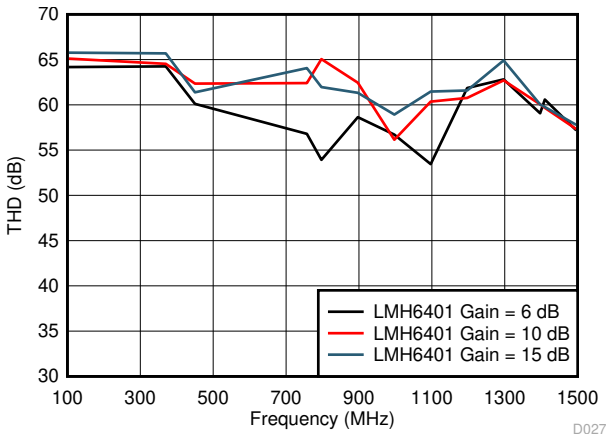
A. LMH5401 Gain = 12 dB

図 7-4. SNR versus FREQ (LMH6401 I/P Path)



A. LMH5401 Gain = 12 dB

図 7-5. SFDR versus FREQ (LMH6401 I/P Path)



A. LMH5401 Gain = 12 dB

図 7-6. THD versus FREQ (LMH6401 I/P Path)

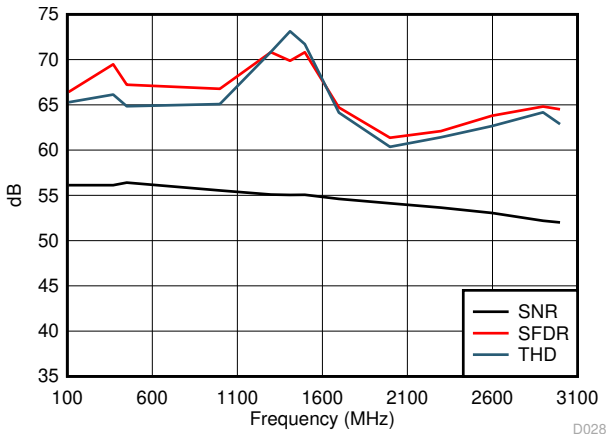


図 7-7. SNR, SFDR, THD versus FREQ (TRANSFORMER I/P)

図 7-8 and 図 7-9 show the measured spectrum of the TIDA-01022 design at a 997-MHz input signal for the LMH5401+LMH6401 combination and transformer coupling, respectively.

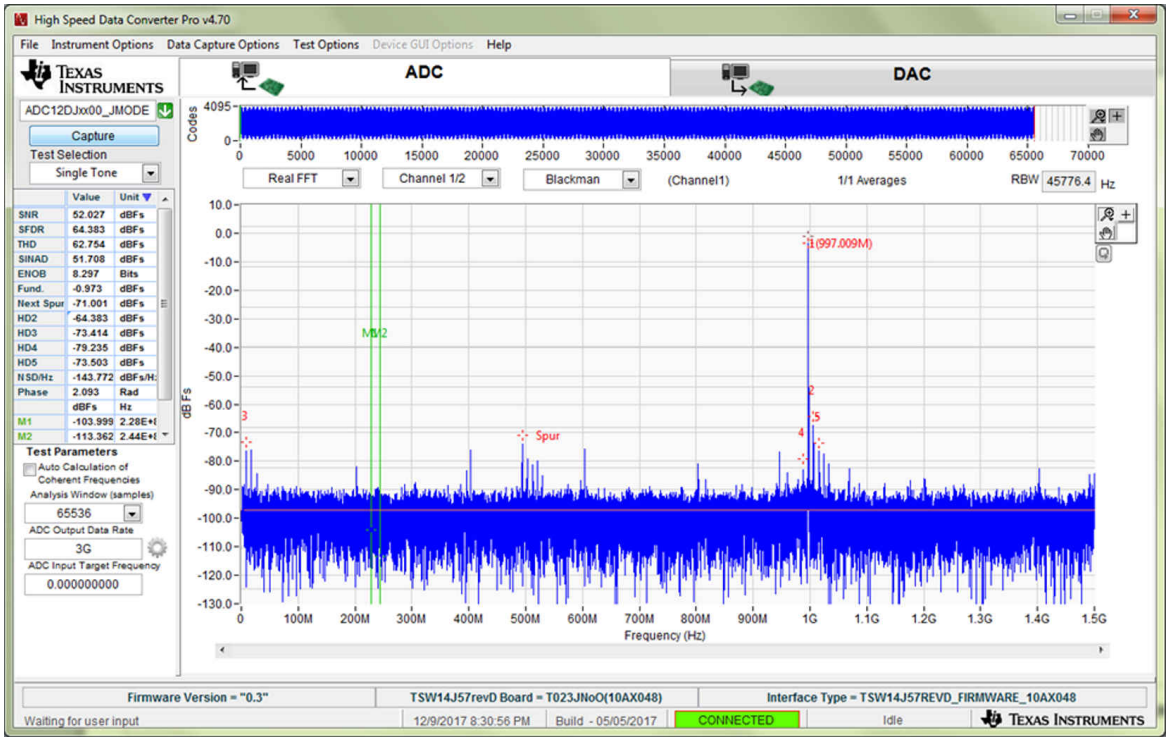


図 7-8. 997-MHz Spectrum (LMH5401+LMH6401)

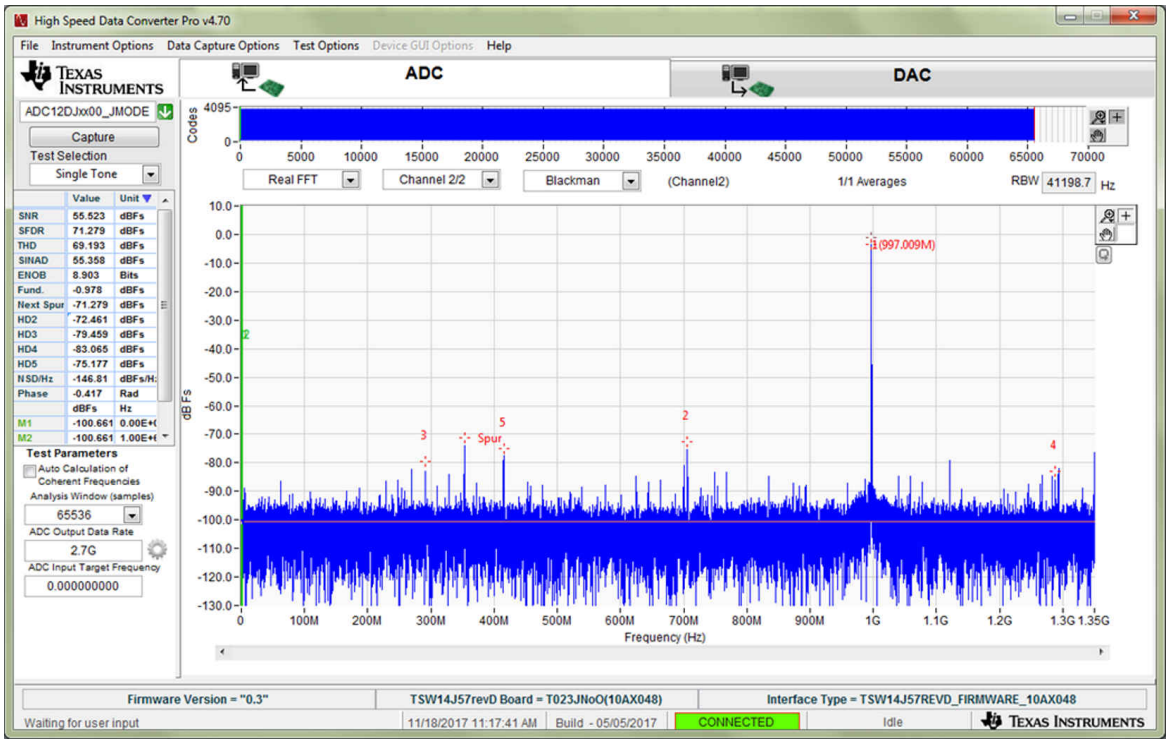


図 7-9. 997-MHz Spectrum (Transformer Coupling)

7.5 Multichannel Skew Measurement

表 7-2 lists the measured time skew between two channels (CH1 and CH3) of the TIDA-01022 design at room temperature with a 997-MHz input signal and at a sampling frequency of 2700 MHz. Evaluate this skew by calculating the phase difference between signals captured from each ADC. This measurement for both signal chain inputs and the measured time skew was less than 5 ps. 表 7-2 shows the skew measured between two channels for both the transformer input and FDA input path. 図 7-10 shows the corresponding skew measurement data plot and 図 7-11 shows the sampled signals in the time domain plot.

表 7-2. TIDA-01022 CH1 to CH3 Skew Measurement

SAMPLE CYCLE	TRANSFORMER COUPLING INPUT	FDA INPUT (LMH5401+6401)
1	0.243 ps	0.623 ps
2	0.156 ps	0.695 ps
3	0.575 ps	0.749 ps
4	0.511 ps	0.265 ps
5	0.824 ps	0.484 ps
6	0.669 ps	0.339 ps
7	0.83 ps	1.04 ps
8	0.623 ps	0.795 ps
9	0.72 ps	0.712 ps
10	0.629 ps	0.835 ps

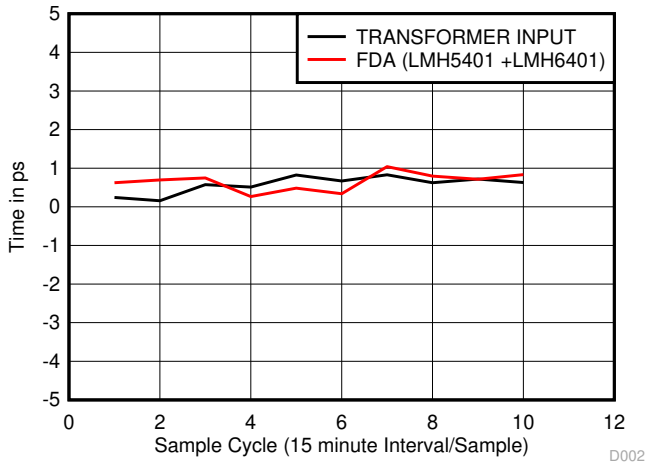


図 7-10. Channel-to-Channel Measurement Plot

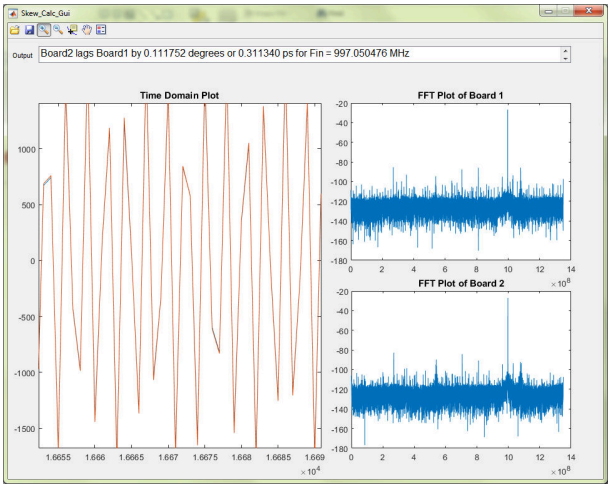


図 7-11. Channel-to-Channel Skew Measurement GUI

図 7-12 shows that the time domain measured plot of the ADC1 and ADC2 corresponds to CH1 and CH3 of the TIDA-01022 design.

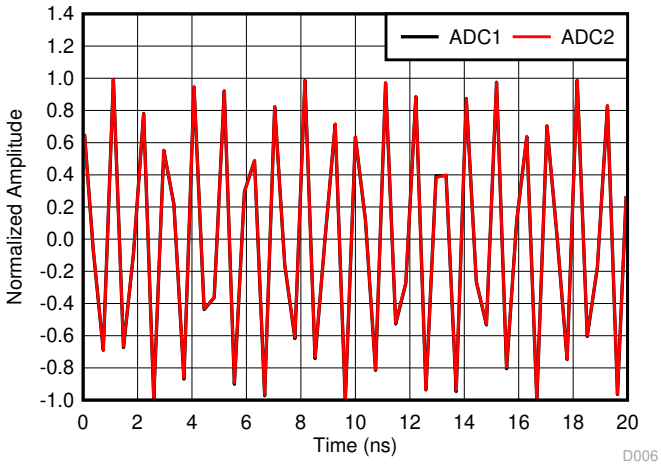


図 7-12. Sampled Signal at 997 MHz

7.6

In summary, the TIDA-01022 is a multichannel AFE reference design with a 3.2-GHz onboard high-performance clocking solution that can be used for DSO, RADAR, and 5G wireless test systems. This reference design demonstrates a DC-coupled wideband DVGA using the LMH5401+LMH6401, which meets the requirements for a high-speed digital oscilloscope AFE. This design also demonstrates deterministic latency and achieves a channel-to-channel skew of < 5 ps by tuning the t_{AD} adjust.

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-01022.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01022.

8.3 Altium Project

To download the Altium project files, see the design files at TIDA-01022.

8.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01022.

8.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01022.

9 Software Files

To download the software files, see the design files at TIDA-01022.

10 Related Documentation

1. Texas Instruments, *Cascaded LMH5401 and LMH6401 Reference Design*
2. Texas, Instruments, *JESD204B Deterministic Latency*
3. Texas Instruments, *JESD204B multi-device synchronization: Breaking down the requirements*
4. Texas Instruments, *Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers*
5. Texas Instruments, *50-Ohm 2-GHz Oscilloscope Front-end Reference Design*
6. Texas, Instruments, *ADC12DJ3200 Evaluation Module*
7. Texas, Instruments, *TSW14J56 JESD204B High-Speed Data Capture and Pattern Generator Card*
8. Texas, Instruments, *TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card User's Guide*

10.1 Trademarks

11 About the Authors

ANBU MANI is a systems engineer in the Industrial Systems Engineering team at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Anbu has fifteen years of experience in analog circuit design and digital circuit design for the Automatic Test Equipment in Modular platform. He is also engaged with the design and development of embedded products. Anbu earned his bachelor of engineering (BE) in electronic and communication from the Anna University, Chennai.

SANKAR SADASIVAM is a system architect in the Industrial Systems Engineering team at Texas Instruments, where he is responsible for designing and developing reference design solutions for the industrial systems with a focus on Test and Measurement. Sankar brings to this role his extensive experience in analog, RF, wireless, signal processing, high-speed digital, and power electronics. Sankar earned his master of science (MS) in electrical engineering from the Indian Institute of Technology, Madras.

11.1 Acknowledgment

The authors would like to thank their colleagues Bryan Bloodworth, Taras Dudar, Ajeet Pal, Timothy Toroni, Jim Brinkhurst, Ken Chan, Chis Glaser, Oliver Nachbaur and Rohit Bhat for their unconditional support and critical feedback during the development of this design.

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2017) to Revision A (January 2022)	Page
• Added *BUF802* to the *Resources* section	1
• Added the *BUF802* section	6
• Added the *High-Input Impedance Buffer Implementation Using the BUF802* section	15

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265