参考資料

TI Designs: TIDA-01485
三相BLDCモータ用の36V/1kW、99%効率、18cm^{2}の電力段のリファレンス・デザイン

概要

この1kW電力段のリファレンス・デザインは、電動工具などの産業用アプリケーションで使用される三相、36VのブラシレスDC (BLDC)モータで99%の効率を実現し、10セルのリチウムイオン・バッテリで動作します。このデザインでは、この電力レベルで最小のインバータ電力段を紹介し、センサ・ベースの台形制御を実装し、25A_{RMS} (2秒間のピーク電流60A、400ミリ秒のピーク電流100A)の連続巻線電流をサポートします。このデザインのMOSFETパワー・ブロックおよび電流制御のゲート・ドライバでは、スルー・レート制御および低い寄生インダクタンスにより、クリーンなMOSFETスイッチングと最小のEMIを実現できます。

リソース

TIDA-01485	デザイン・フォルダ
CSD88599Q5DC	プロダクト・フォルダ
DRV8323R	プロダクト・フォルダ
MSP430F5132	プロダクト・フォルダ
LMT87	プロダクト・フォルダ

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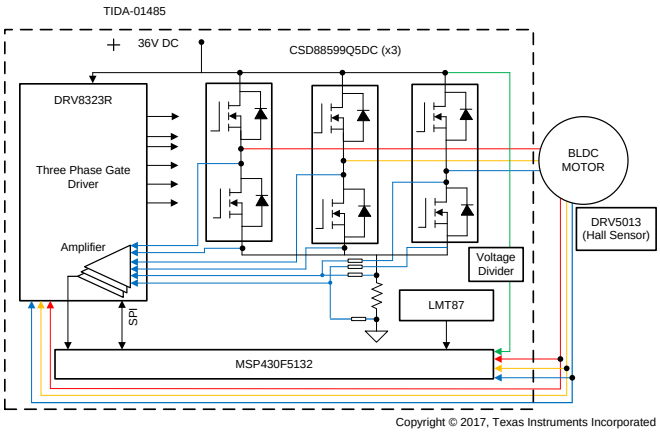

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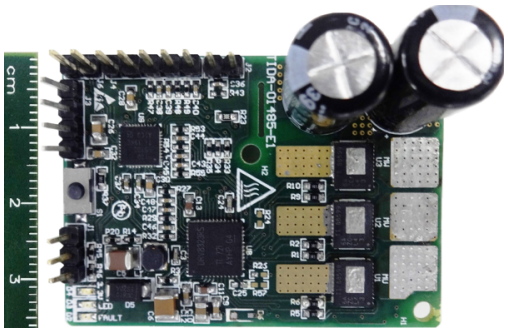
特長

- BLDCモータ用の1kWドライブで、センサ・ベースの台形制御をサポート
- 8～42Vで動作する設計
- 最大25A_{RMS}の連続出力電流
- 60Aで2秒、100Aで400ミリ秒のピーク電流能力
- 60V/400A_{PEAK}、1.7mΩ R_{DS_ON}、SON5x6パッケージのハーフブリッジ・パワー・ブロックを使用し、50mm×36mmの小さなPCB占有面積を実現
- 100%デューティ・サイクル時に99%を超える効率
- ヒートシンクなしで36V/700W、18A_{RMS}を実現
- MOSFETのV_{DS}を監視してモータ電流センシングを行うため、シャント抵抗が不要
- サイクル単位の過電流およびモータのストール電流の非ラッチ制限、およびV_{DS}センシングによる短絡ラッチ保護
- 貫通電流、低電圧、過熱、およびロータのブロックに対する保護
- 単一PWM制御のオプション
- 動作時周囲温度: -20℃～+55℃

アプリケーション

- コードレス・ハンドヘルド電動工具
- コードレス・ハンドヘルド・ガーデニング・ツール
- 電動アシスト自転車
- ロボット芝刈り機



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1 System Description

Power tools are used in various industrial and household applications such as drilling, grinding, cutting, polishing, driving fasteners, and so on. The most common types of power tools use electric motors while some use internal combustion engines, steam engines, or compressed air. Power tools can be either corded or cordless (battery powered). Corded power tools use the mains power (the grid power) to power up the AC or DC motors.

Cordless tools use battery power to drive DC motors. Most cordless tools use lithium-ion batteries, the most advanced in the industry offering high energy density, low weight, and greater life. Power tools are available in different power levels and battery voltage levels. Power tools such as cordless chainsaws and circular saws and different garden tools like cordless wood and branch cutters require a very high torque and need a very high peak current.

Cordless tools use brushed or brushless DC (BLDC) motors. The BLDC motors are more efficient and have less maintenance, low noise, and longer life. Power tools have requirements on form factor, efficiency, peak current, reliability, and thermal performance. Therefore, high-efficient power stages with a compact size are required to drive the power tool motor. The small form factor of the power stage enables flexible mounting, better PCB layout performance, and low-cost design. High efficiency provides maximum battery duration and reduces cooling efforts. The high-efficiency requirement in turn asks for switching devices with a low drain-to-source resistance (R_{DS_ON}). The power stage must also take care of protections like motor stall or any other chances of high current.

This reference design uses the CSD88599 NexFET™ power block featuring a very low R_{DS_ON} of 1.7 mΩ in a SON5×6 SMD package. The power block with high-side and low-side FETs in a single package helps to achieve very small form factor and better switching performance. The three-phase gate driver DRV8323 is used to drive the three-phase MOSFET bridge, which can operate from 6 to 60 V and support programmable gate current with maximum setting of 2-A sink / 1-A source. The DRV8323 includes three current shunt amplifiers, which helps in measuring and amplifying the V_{DS} of the FET for motor current measurements that support bidirectional current sensing with adjustable gain and eliminates the use of shunt.

The SPI of the DRV8323 provides detailed fault reporting and flexible parameter settings such as gain options for the current shunt amplifier, slew rate control of the gate drivers, and various protection features. The LMT87 temperature sensor is used to sense the FET temperature and the results is used to calibrate the current sensing by V_{DS} monitoring. The MSP430F5132 microcontroller is used to implement the control algorithm.

The test report evaluates the RMS current capability, peak current capability, efficiency and thermal performance of the board, FET switching waveforms, and overcurrent protection features such as cycle-by-cycle control and latch control of the DRV8323. The test results also show the improved RMS current capability of the board with different external cooling.

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1.1 Key System Specifications

表 1. Key System Specifications

PARAMETERS	SPECIFICATIONS
Input voltage	36-V DC (8-V min to 42-V max), 10-cell Li-Ion
Rated output power	1 kW
RMS winding current	25 A
Peak winding current	60 A (for 2 s), 100 A (for 400 ms), 200 A (100 ms), 400 A (10 ms)
Control method	Sensor-based trapezoidal
Inverter switching frequency	20 kHz (adjustable from 5 to 100 kHz)
Feedback signals	DC bus voltage, Hall sensor, inverter leg currents, low-side DC bus current
Protections	Cycle-by-cycle overcurrent, input undervoltage, overtemperature, and blocked rotor
Cooling	With heat sink
Operating ambient	–20°C to 55°C
Board specification	50 mm × 36 mm, four-layer, 2-oz copper
Efficiency	> 98.5%

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2 System Overview

2.1 Block Diagram

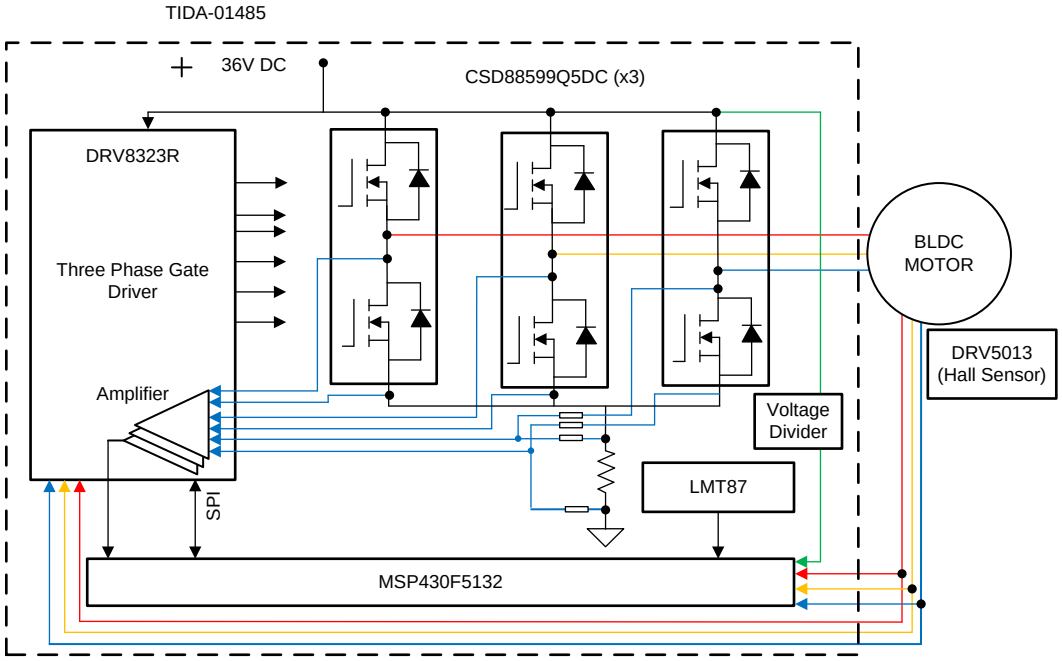

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図 1. Block Diagram of TIDA-01485

2.2 Highlighted Products

2.2.1 CSD88599Q5DC

The key requirements in selecting the MOSFET are:

- High efficiency (MOSFET with low losses under operating condition)
- Small size to reduce the solution form factor
- Better heat dissipation
- High peak current capability
- Better switching performance to ensure reliable operation under short circuit or worst case switching conditions.

The CSD88599Q5DC 60-V power block is the best option meeting these requirements to suit in high-current motor control applications such as handheld cordless garden and power tools. This device uses TI's patented stacked die technology in order to minimize parasitic inductances while offering a complete half bridge in a space saving thermally enhanced DualCool® 5×6-mm package. With an exposed metal top, this power block device allows for simple heat sink application to draw heat out through the top of the package and away from the PCB. This metal top provides superior thermal performance at the higher currents demanded by many motor control applications.

2.2.2 DRV8323

The key requirements in selecting the gate driver are:

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- Three-phase gate driver with a high level of integration to reduce the form factor
- Sufficient source and sink current to reduce the switching losses
- Sufficiently high gate drive voltage to enable the MOSFET conducts at the minimum R_{DS_ON}
- High level of overcurrent and other protections to enable a reliable system operation under worst case conditions like motor stall, short circuit, and so on

The DRV8323 three-phase gate driver can be used to meet these requirements. The device provides three half-bridge drivers, each capable of driving one high-side and one low-side N-channel MOSFET. The DRV8323 generates the proper gate voltage drive for both the high-side and low-side FETs using a charge pump. The DRV8323 supports up to a 1-A source and 2-A sink peak gate drive current capability. The DRV8323 can operate from a single power supply and supports a wide input supply range from 6 to 60 V. The DRV8323 includes three current shunt amplifiers for accurate current measurements, support a 100% duty cycle, and have multiple levels of protection.

2.2.3 MSP430F5132

The TI MSP430™ family of ultra-low-power MCUs consists of several devices featuring different sets of peripherals targeted for various applications. The architecture is combined with five low-power modes. The device features a powerful 16-bit reduced instruction set computing (RISC) CPU, 16-bit registers, and constant generators that contribute to the maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in less than 5 µs.

The MSP430F5132 series are microcontroller configurations with two 16-bit high-resolution timers, two universal serial communication interfaces (USCIs) USCI_A0 and USCI_B0, a 32-bit hardware multiplier, a high-performance 10-bit 200-ksps analog-to-digital converter (ADC), an on-chip comparator, a three-channel direct memory access (DMA), 5-V tolerant I/Os, and up to 29 I/O pins. The timer event control module connects different timer modules to each other and routes the external signals to the timer modules. The device is capable of working up to a system frequency of 25 MHz. The operating temperature of the device is –40°C to 85°C.

2.2.4 LMT87

The LMT87 is a precision CMOS integrated-circuit temperature sensor with an analog output voltage that is linearly and inversely proportional to temperature. The device can operate down to a 2.7-V supply with 5.4-µA power consumption. Package options including surface mounted and through-hole TO-92 package allow the LMT87 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations. The LMT87 has accuracy specified in the operating range of −50°C to 150°C.

2.3 System Design Theory

The three-phase BLDC motor needs a three-phase electronic drive to energize the motor, based on the rotor position. The electronic drive consists of:

- Power stage with a three-phase inverter having the required power capability
- MCU to implement the motor control algorithm
- Position sensor for accurate motor current commutation
- Gate driver for driving the three-phase inverter
- Power supply to power up the MCU

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For more details about BLDC trapezoidal control, see the application report *Sensorless Trapezoidal Control of BLDC Motors* (SPRABQ7).

2.3.1 Power Stage Design: Battery Power Input to Board

The battery power input section is shown in 図 2. The input bulk aluminum electrolytic capacitors C14 and C15 provide the ripple current and its voltage rating is de-rated by 20% for better life. These capacitors are rated to carry high ripple current. C17 is used as a high-frequency bypass capacitor. D1 is the transient voltage suppression (TVS) with a breakdown voltage of 58 V.

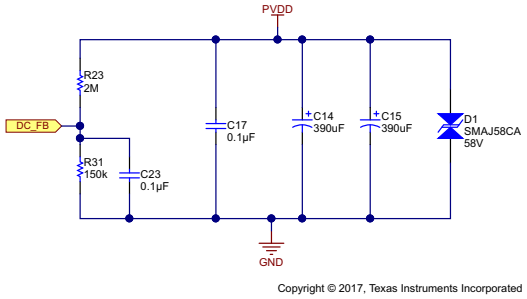

図 2. Schematic of Battery Power Input Section

The input supply voltage PVDD is scaled using the resistive divider network, which consists of R23, R31, and C23, and fed to the MCU. Considering the maximum voltage for the MCU ADC input as 3.3 V, the maximum DC input voltage measurable by the MCU is calculated as in 式 1.

$$V_{DC}^{max} = V_{ADC\_DC}^{max} \times \frac{(150\,k\Omega + 2000\,k\Omega)}{150\,k\Omega} = 3.3 \times \frac{(150\,k\Omega + 2000\,k\Omega)}{150\,k\Omega} = 47.3\ V \quad (1)$$

Considering a 10% headroom for this value, the maximum recommended voltage input to the system is 25.3 × 0.9 = 42.5. So for a power stage with maximum operating voltage of 42 V, this voltage feedback resistor divider is ideal. Also, this choice gives optimal ADC resolution for a system operating from 8 to 42 V.

2.3.2 Power Stage Design: Three-Phase Inverter

The three-phase inverter is realized using three MOSFET power blocks. Each power block consists of two MOSFETs connected as a high-side and low-side FET, which can be used as one leg of the inverter. 図 3 shows one leg of the power stage, which consists of one power block and the decoupling capacitor C19 placed close across power blocks. This decoupling capacitor reduces the ringing in the supply lines because of the parasitic inductance added by the sense resistor and the power track.

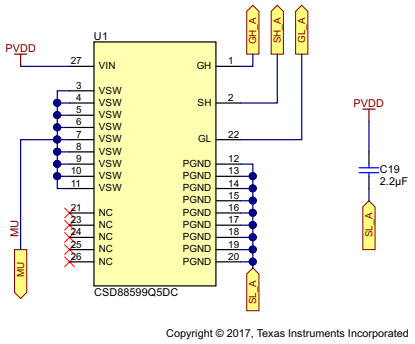

図 3. Schematic of One Leg of Three-Phase MOSFET Inverter

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注: Connect the decoupling capacitors very near to the corresponding MOSFET legs for better decoupling. An improper layout or position of the decoupling capacitors can cause undesired V_{DS} switching voltage spikes.

The reference design uses MOSFET V_{DS} monitoring to measure the inverter current. The design also has an option to measure DC bus current using the shunt resistors R13 and R15 mounted on the DC bus return path. The sensed currents are fed to the MCU through the current shunt amplifiers. The sense resistor is mainly used to measure the average battery current. The peak current in MOSFET is measured by monitoring the V_{DS}.

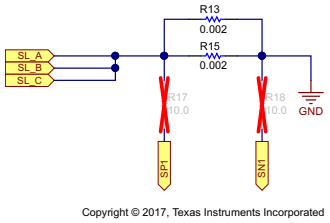

図 4. Schematic of External Shunt for Current Sensing

2.3.3 Selecting Sense Resistor

Power dissipation in sense resistors and the input offset error voltage of the op amps are important in selecting the sense resistance values. The sense resistors are designed to carry a total nominal RMS current of 30 A with a peak current of 60 A for 2 seconds. A high sense resistance value increases the power loss in the resistors. The internal current shunt amplifiers of the DRV8323 have an input offset error of 3 mV. The DRV8323 has the DC offset voltage calibration feature. If the amplifier is used without offset calibration, it is required to select the sense resistor such that the sense voltage across the resistor is sufficiently higher than the offset error voltage to reduce the effect of the offset error. Selecting a 1-mΩ resistor as the sense resistor, the power loss in the resistor at 30-A_{RMS} is given by 式 2:

$$\text{Power loss in the resistor} = I_{RMS}^2 \times R_{SENSE} = 30^2 \times 0.001 = 0.9\,\text{W} \quad (2)$$

At a 60-A peak current, using 式 2, the power loss in the resistor = 3.6 W (for 2 seconds) In the reference design two 2-mΩ, 3-W resistors are used in parallel.

注: Consider reducing the sense resistor further down to reduce the power loss and use the current sense amplifier in maximum gain.

2.3.4 Power Stage Design: DRV8323 Gate Driver

図 5 shows the schematic of the DRV8323 gate driver. C13 is the DVDD decoupling capacitor that must be placed close to DRV8323. PVDD is the DC supply input; in this case, it is the battery voltage of 36 V. A 4.7-µF capacitor (C10) is used as the PVDD capacitor. The diode D6 helps to isolate the gate driver power supply in case the battery voltage dips during short-circuit conditions. The presence of D6 enables the PVDD capacitor C10 to hold the voltage under small-duration battery voltage dips and make sure that the gate driver does not enter an undesired undervoltage lockout (UVLO). C11 and C12 are charge pump capacitors. The EN_GATE of the DRV8323 is connected to the MCU. This connection helps the MCU to enable or disable the gate drive outputs of the DRV8323. For the voltage rating and selection of the capacitors, see the DRV8323 datasheet.

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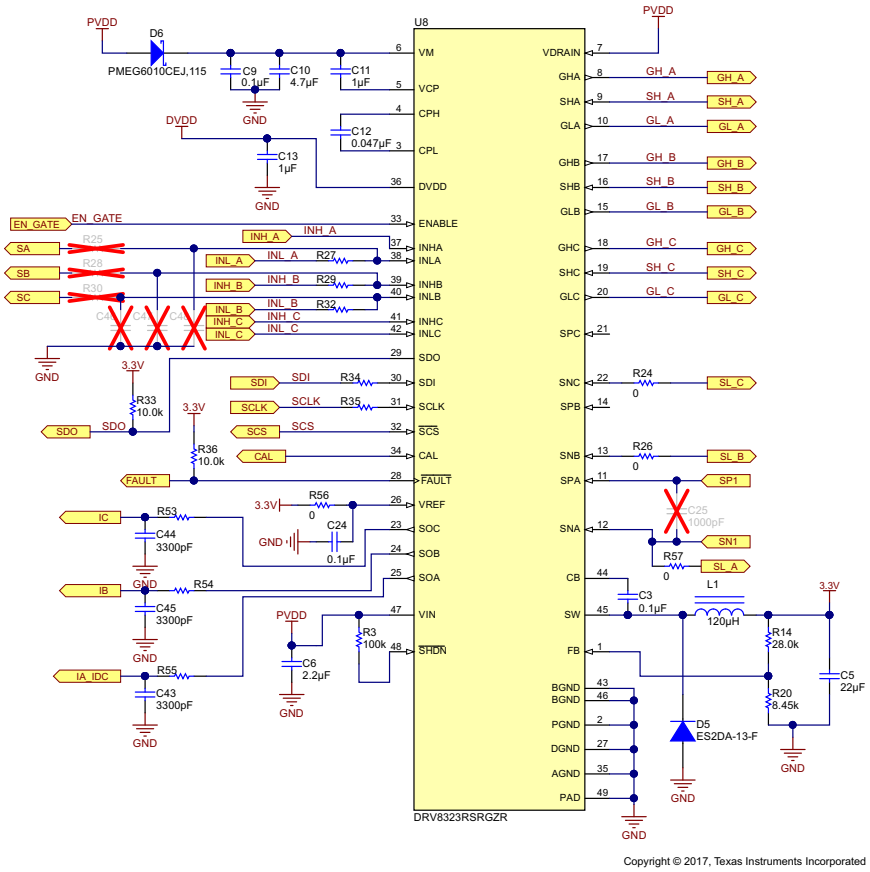

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図 5. Schematic of DRV8323 Gate Driver

2.3.4.1 Features of DRV8323

The DRV8323 integrates three half-bridge gate drivers, each capable of driving high- and low-side N-channel MOSFETs. A doubler charge pump provides the proper gate bias voltage to the high-side MOSFET across a wide operating voltage range, in addition to providing 100% duty cycle support. An internal LDO provides the gate bias voltage for the low-side MOSFETs. The DRV8323 implements a smart gate drive, which allows the user to adjust the gate drive current on the fly without requiring current-limiting gate drive resistors. Current is adjustable through the SPI or on the IDRIVE pin for the hardware interface.

The DRV8323 gate drivers use an adjustable, complimentary push-pull topology for both the high- and low-side drivers. This topology allows for strong pullup and pulldown of the external MOSFET gate. The gate drivers support adjustable peak current and duration settings through the IDRIVE and TDRIVE settings. These settings allow the user to adjust the external MOSFET slew rate and provide additional system protection.

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The peak source and sink current of the DRV8323 gate drivers is adjustable either through the device registers or by an external pin, IDRIVE. Control of the MOSFET V_{DS} slew rates is an important parameter for optimizing emitted radiations and system efficiency. The rise and fall times also influence the energy and duration of the diode recovery spikes and dV/dt related turn on. When changing the state of the gate driver, the peak current (IDRIVE source or sink) is applied for a fixed period of time (TDRIVE), during which the gate capacitances are charged or discharged completely. After TDRIVE has expired, a fixed holding current (I_{HOLD}) is used to hold the gate at the desired state (pulled up or pulled down). During high-side turnon, the low-side gate is pulled low with a strong pulldown. This pulldown prevents the gate-to-source capacitance of the low-side MOSFET from inducing turnon.

The fixed TDRIVE time ensure that under abnormal circumstances like a short on the MOSFET gate or the inadvertent turnon of a MOSFET V_{GS} clamp, the high peak current through the DRV8323 gate drivers is limited to the energy of the peak current during the TDRIVE. Limiting this energy helps to prevent damage to the gate drive pins and external MOSFET.

The TDRIVE time must be selected to be longer than the time need to charge or discharge the MOSFET gate capacitances. IDRIVE and TDRIVE must be initially selected based on the parameters of the external MOSFET used in the system and the desired rise and fall times. TDRIVE does not increase the PWM time and will terminate if a PWM command is received while it is active. A recommended starting point is to select a TDRIVE that is approximately two times longer than the switching rise and fall times of the external MOSFET. See the DRV8323 product page for more details.

The DRV8323 integrates the following protections that help in making a reliable power stage:

- DC supply undervoltage lockout
- Charge pump undervoltage lockout
- V_{DS} overcurrent protection
- SENSE overcurrent protection
- Thermal shutdown
- Thermal warning

For more details, see the DRV8323 datasheet.

2.3.5 Current Shunt Amplifier on DRV8323

The sense amplifiers on the DRV8323 can be configured to amplify the voltage across the low-side FETs. During this mode of operation, the SPX pins must be left unconnected. The positive input of the amplifier is internally connected to the SHX pin. An internal clamp prevents high voltage on the SHX pin from damaging the sense amplifier inputs.

When the CSA_FET bit is set to ‘1’, the negative reference for the low-side V_{DS} monitor is automatically set to SNX, regardless of the state of the LS_REF bit. This logic is implemented to prevent the low-side V_{DS} monitor from being disabled. If the system is intended to operate in FET sensing mode, take care to route the SHX an SNX pins to kelvin connections across the drain and source of the low-side FETs.

When operating in FET sensing mode, the amplifier is enabled at the end of TDRIVE. At this time, the amplifier input is connected to SHX, and the SO_X output will be valid. Whenever a low-side FET receives a signal to turn off, the amplifier inputs are shorted together. When GLX is low, SPX and SNX are internally shorted.

The current shunt amplifiers have the following features:

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- Can be programmed and calibrated independently
- Can support bidirectional and unidirectional current sensing
- Four programmable gain settings through SPI registers (5, 10, 20, and 40 V/V)
- Has programmable output bias scale (V_{REF} or $V_{REF}/2$)
- Has programmable blanking time of the amplifier outputs
- The amplifier can be used to monitor the current through the half-bridges and the current is approximately calculated as in 式 3.

$$SO_X = \frac{VREF}{2} - \left(I \times CSA\_GAIN \times R_{DS\_ON}\right) \quad (3)$$

図 6 shows the current sense amplifier simplified block diagram.

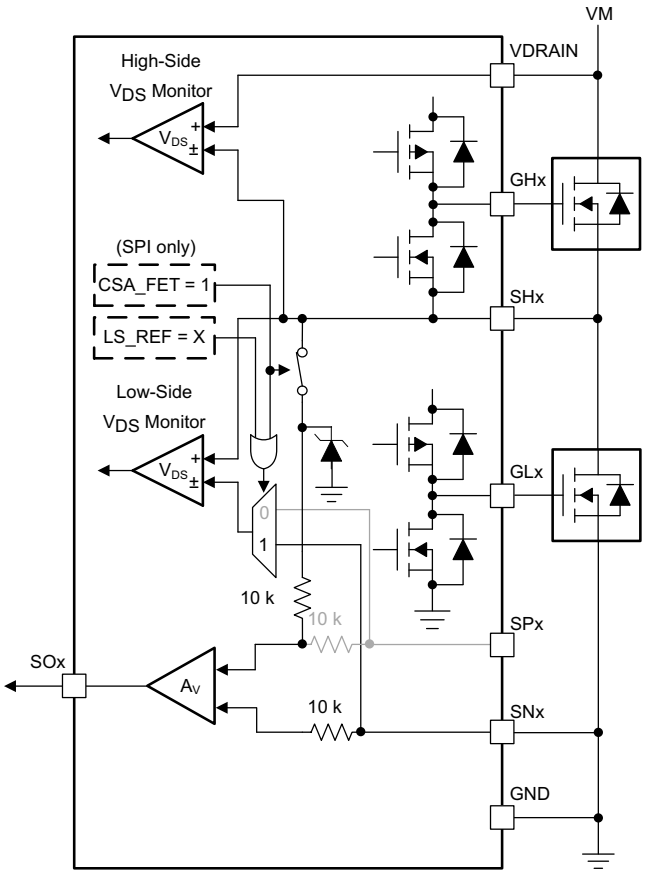

図 6. DRV8323 Current Shunt Amplifier Simplified Block Diagram

2.3.6 Step-Down Buck Regulator

The DRV8320R and DRV8323R have an integrated buck regulator (LMR16006) to supply power for an external controller or system voltage rail. The LMR16006 device is a 60-V, 600-mA, buck (step-down) regulator. The buck regulator has a very-low quiescent current during light loads to prolong battery life. 表 2 shows the specifications of the buck converter used for this reference design.

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表 2. Specifications of Buck Converter

PARAMETER	SPECIFICATION
Conduction mode	Fixed frequency PWM control
Output voltage	3.3 V
Transient response 50- to 150-mA load step	ΔV_{OUT} = 4%
Maximum output current	150 mA
Input voltage	36 V nom. (6 to 42 V)
Output voltage ripple	0.5% of V_{OUT}

For the detailed design of the buck converter, see the DRV8323 datasheet.

2.3.7 Power Stage Design: MSP430 Microcontroller

図 7 shows the schematic for configuring the MSP430F5132 MCU. The resistor R37 is used to limit the dV/dt at the supply pin of the MSP430F5132. This reference design uses 10-µF decoupling capacitors. A 0.1-µF capacitor has been added to obtain the best performance at a high frequency. The Timer D of the MCU is used for PWM generation. The TD0.1 instance of the timer and the corresponding pins are mapped to the high-side switch PWM. The TD0.2 instance of the timer and the corresponding pins are mapped to the low-side switch PWM.

The reference design uses unipolar, trapezoidal BLDC control where the high-side switches switching at a high frequency. The low-side switches switch at the electrical frequency of the motor current, which is much lower and the same will switch at a high frequency (complimentary to high-side switch) during the freewheeling period to enable active freewheeling and hence low losses. All the feedback signal voltages including the DC bus voltage, current sense amplifier output, potentiometer voltage for speed control, and temperature sensor output are interfaced to the 10-bit successive approximation (SAR) ADC channels of the MCU. The current sense amplifier output is also connected to the comparator input.

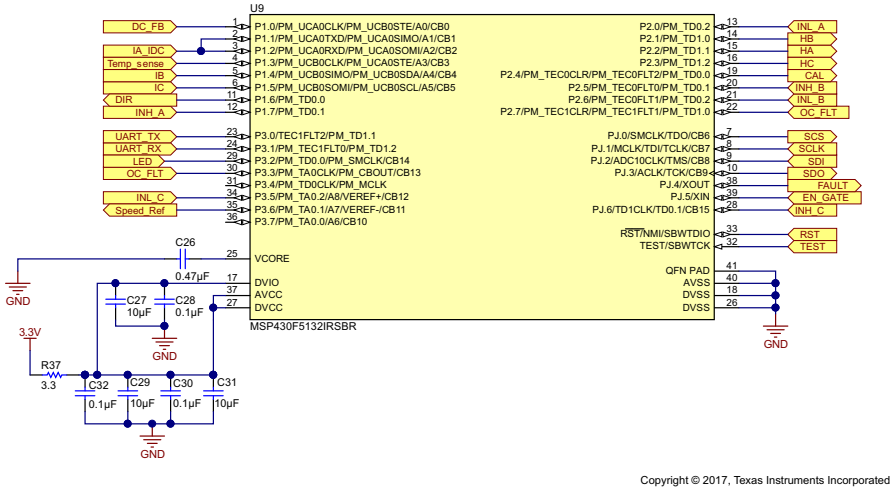

図 7. MSP430F5132 Schematic

2.3.8 Power Stage Design: Hall Sensor Interface

図 8 shows the Hall sensor interface from the motor to the board. The 3.3 V is used as the power supply for the Hall sensor. Usually, the Hall sensors have an open drain or open collector configuration. R47, R48, and R49 are used as the pullup resistors. R50, R51, and R52, along with C38, C39, and C40, form noise filters at the Hall sensor input.

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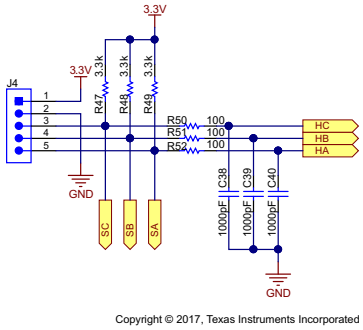

図 8. Schematic of Hall Sensor Connector

注: The Hall sensor connection should match with the winding connection for proper operation of the BLDC motor.

2.3.9 Temperature Sensing

図 9 shows the temperature sensor circuit used to measure the PCB temperature. The LMT87 is an analog output temperature sensor. The temperature sensing element is comprised of a simple base-emitter junction that is forward biased by a current source. The temperature sensing element is then buffered by an amplifier and provided to the OUT pin. The amplifier has a simple push-pull output stage, thus providing a low-impedance output source. The average output sensor gain is 13.6 mV/°C. The temperature sensor placed near the MOSFET and the output of the temperature sensor is used to calibrate the V_{DS} sense signal. The R_{DS_ON} of the MOSFET varies with temperature and hence the V_{DS} measured across the FET for current sensing has to be calibrated to measure the current accurately by sensing V_{DS}.

注: The temperature gradient in the board has to be considered to properly calibrate the V_{DS} of multiple FETs against R_{DS_ON} variation with temperature.

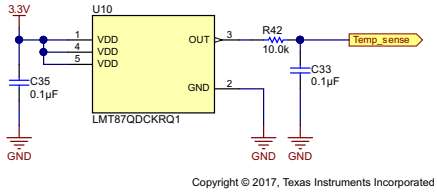

図 9. Schematic of Temperature Sensor

2.3.10 Power Stage Design: External Interface Options and Indications

2.3.10.1 Speed Control of Motor

The speed control is done using a potentiometer (POT), and the POT voltage is fed to the ADC of the MCU. The circuit is shown in 図 10. The POT is supplied from the 3.3 V. A 20k POT can be connected externally to the jumper J1. Connect the fixed terminals of the POT to terminal 1 and 3 of J1 and mid-point to terminal 2 of J1.

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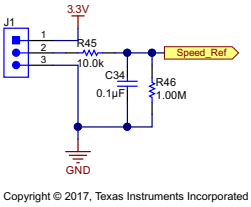

図 10. Schematic of Potentiometer Connection for Speed Control

The resistor R46 is used to ensure that the speed control reference is zero if the POT terminal is open.

2.3.10.2 Direction of Rotation: Digital Input

The jumper J2 (shown in 図 11 is used to set the direction of rotation of the motor. Close or open the jumper to change the direction of rotation.

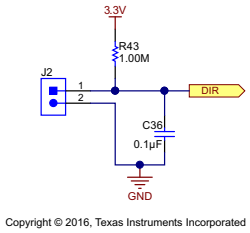

図 11. Schematic of Digital Input to Change Direction of Rotation

2.3.10.3 LED Indications

図 12 shows the LED indications provided in the board. The LED D4 indicates the 3.3 V in the board, D2 is tied to FAULT signal from DRV8323, and D3 is driven by a digital I/O in the MCU.

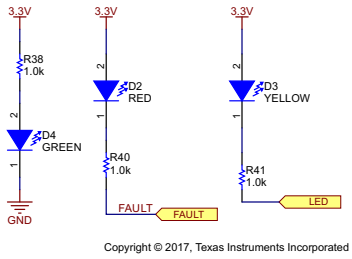

図 12. Schematic of LED Indications

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3 Hardware, Firmware, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 Getting Started Hardware

3.1.1.1 Connector Configuration of TIDA-01485

図 13 shows the connector configuration of this reference design, which features the following:

- Two-terminal input for power supply: This pin is used to connect the input DC supply from the battery. The positive and negative terminals can be identified as shown in 図 13.
- Three-terminal output for motor winding connection: The phase output connections for connecting to the three-phase BLDC motor winding, marked as PHASE W, PHASE V, and PHASE U as shown in 図 13.
- 3-pin connector J1: This connector can be used to interface an external potentiometer for speed reference. The two fixed terminals of the potentiometer should be connected to 3V3 pin and GND pin. The mid-point of the potentiometer must be connected to the POT pin of the connector.
- 2-pin connector J2: This connector is used for the motor direction change. Externally shorting or opening this connector changes the direction of the rotation of the motor.
- 4-pin connector J3: This is the programming connector for the MSP430F5132 MCU. The two-wire Spy-Bi-Wire protocol is used to program the MSP430F5132.
- 5-pin connector J4: This is the interface for connecting the Hall position sensors from the motor.
- 2-pin connector J6: This connector is used for external UART communication interface. The RX and TX pins are available enabling the communication with external *Bluetooth*® low energy or Wi-Fi®.

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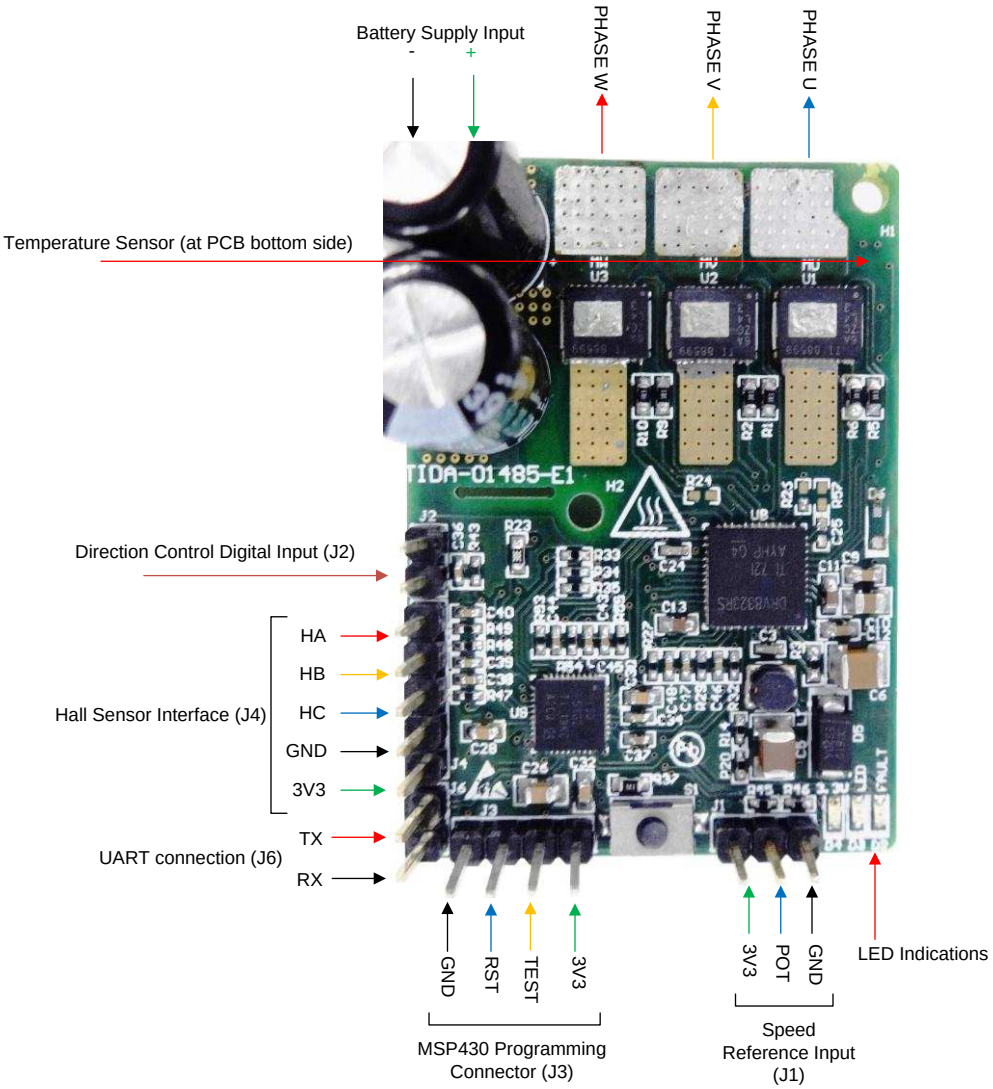

図 13. TIDA-01485 PCB Connectors

3.1.1.2 Programming the MSP430

The two-wire Spy-Bi-Wire protocol is used to program the MSP430F5132 MCU. 図 14 shows the four-pin programming connector provided in the reference design board.

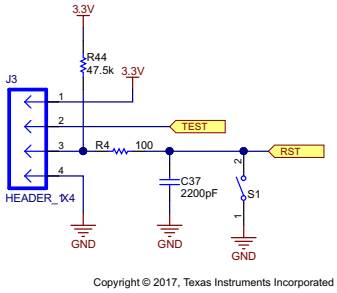

図 14. Schematic of MSP430F5132 Programming Connector

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See the development tools of the MSP430F5132 for programming options with an external JTAG interface.

Follow these steps to program the MSP430F5132 MCU when the programming supply voltage is provided by the board itself:

1. Remove the motor connections from the board, and power on the input DC supply. Make sure that a minimum of 8-V DC input is applied and 3.3 V is generated in the board.
2. Connect the programmer to the board.
3. Open the CCS software, and then build and debug the code to program the MCU.

3.1.1.3 Procedure for Board Bring-up and Testing

Follow this procedure for board bring-up and testing:

1. Remove the motor connections from the board, and power on the input DC supply. Make sure that a minimum of a 8-V DC input is applied and the 3.3 V is generated in the board.
2. Program the MCU as detailed in 3.1.1.2.
3. Remove the programmer, and switch off the DC input supply.
4. Connect the inverter output to the motor winding terminals. Connect the position Hall sensor inputs to the connector J4, and make sure that the winding connection and Hall sensor connections match.
5. Connect the POT at the interface J1 and set the speed reference.
6. Use a DC power supply with current limit protection and apply 8-V DC to the board. If the Hall sensors and winding are connected properly in the matching sequence, then the motor starts running at a speed set by the POT.
7. If the motor is not rotating and takes high current, or rotates and draws a distorted peak winding current waveform (a proper waveform shape is shown in 図 26), then check the winding and Hall sensor connection matching and, if wrong, correct it.
8. Adjust the POT voltage for change in speed.
9. To change direction, switch off the DC input, close the jumper J2, and switch on the DC input.

3.1.2 Firmware

3.1.2.1 System Features

The firmware of this reference design offers the following features and user controllable parameters:

- Trapezoidal control of BLDC motor using digital position Hall sensor feedback
- Overcurrent cycle-by-cycle protection and latch protection using the V_{DS} sensing feature of the DRV8323RS

The firmware system components of this reference design are listed in 表 3.

表 3. TIDA-01485 Firmware System Components

SYSTEM COMPONENT	DESCRIPTION
Development and emulation	Code Composer Studio™ v6.0
Target controller	MSP430F5132
PWM frequency	20-kHz PWM (default), programmable for higher and lower frequencies
PWM mode	Asymmetrical
Interrupts	Port 2 Interrupt for hall sensor change. CPU Timer D: Implements 20-kHz ISR execution rate ADC interrupt

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表 3. TIDA-01485 Firmware System Components (continued)

SYSTEM COMPONENT	DESCRIPTION
PWM generation: Timer configuration	High-side PWM: TIMER TD0.1, Clock = 25 MHz, OUTMOD[2:0] = 2, PWM frequency set for 20 kHz Low-side PWM: TIMER TD0.2, Clock = 25 MHz, OUTMOD[2:0] = 6, PWM frequency set for 20 kHz
Position feedback: Hall sensor signals	P2.2 → HA P2.1 → HB P2.3 → HC
Comparator configuration for overcurrent protection	CB2/P1.2 → CSA output (–ve input of comparator) Internal V_{REF} (+ve input of comparator) CBOUT/P3.3 → Comparator output PM_TEC1FLT1 → PWM shut-off input
ADC channel assignment	A0 → DC bus voltage sensing A1 → Low-side DC bus current sensing/PHASE U low-side MOSFET V_{DS} sensing A3 → PCB or FET temperature feedback A4 → PHASE V low-side MOSFET V_{DS} sensing amplifier output A5 → PHASE W low-side MOSFET V_{DS} sensing amplifier output A7 → Speed reference from the external potentiometer
DRV8323: SPI programming pins connection	PJ.0 → SCS PJ.1 → SCLK PJ.2 → SDI PJ.3 → SDO
DRV8305: Digital inputs/outputs	PJ.5 → EN_GATE PJ.4 → FAULT P2.4 → CAL
MCU digital inputs/output	P1.6 → Direction of motor rotation P3.2 → LED3

3.1.2.2 Customizing the Reference Code

Select the "main.c" file. Parameters exist at the top of the file that can be optimized and are included as the configuration variables. The following section of code shows these parameters:

```
#define PWM_PERIOD 625 //PWM Frequency (Hz) = 25MHz/((2*PWM_PERIOD)-1)
#define MAX_DUTYCYCLE 625 //relative to PWM_PERIOD
#define MIN_DUTYCYCLE 50 //relative to PWM_PERIOD
#define ACCEL_RATE 320 // Ramp up time to full scale duty cycle = (Full scale duty
            cycle) * ACCEL_RATE * PWM_PERIOD/PWM_Frequency
#define DEAD_TIME 1 // Dead time from MSP430 = DEAD_TIME * 0.04 uS (for 25MHz clock)
#define Block_Rotor_Duration 1250 //Blocked_rotor shut off time(s) =
            Block_Rotor_Duration*30000/clock frequency
```

3.1.2.2.1 PWM_PERIOD

PWM_PERIOD sets the value in capture and compare register 0 of Timer_D0. The Timer_D is initialized to operate at 25 MHz; see 式 4 to calculate the PWM frequency. The TIMER_D PWM is configured in up-down mode.

$$\text{PWM frequency}(\text{Hz}) = \frac{25\ \text{MHz}}{((2 \times \text{PWM\_PERIOD}) - 1)} \quad (4)$$

For example, with PWM_PERIOD = 625, PWM frequency = 20 kHz.

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3.1.2.2.2 MAX_DUTYCYCLE

MAX_DUTYCYCLE sets the maximum duty cycle the user can set. Every time, the duty cycle input command is compared to the MAX_DUTYCYCLE. If the duty cycle input command exceeds the MAX_DUTYCYCLE, the target duty cycle is set to the MAX_DUTYCYCLE. This number is relative to the PWM_PERIOD.

3.1.2.2.3 MIN_DUTYCYCLE

MIN_DUTYCYCLE sets the minimum duty cycle that can be applied to the motor. This number is relative to the PWM_PERIOD.

3.1.2.2.4 ACCEL_RATE

ACCEL_RATE defines how fast the motor will accelerate. For a motor with greater inertia or if it needs a longer time to accelerate, set this number to a high value such as 2000. Motors that can quickly ramp up can use a smaller ACCEL_RATE to decrease the startup time. In the application program, the start ramp-up time and the ACCEL_RATE required can be calculated using 式 5 and 式 6.

$$\text{Ramp-up time to full-scale duty cycle} = \frac{\text{Full-scale duty cycle} \times \text{ACCEL\_RATE} \times \text{PWM\_PERIOD}}{\text{PWM frequency}} \quad (5)$$

$$\text{ACCEL\_RATE} = \frac{\text{Ramp-up time to full-scale duty cycle} \times \text{PWM frequency}}{\text{Full-scale duty cycle} \times \text{PWM\_PERIOD}} \quad (6)$$

For example: To ramp up from a 0% to 100% duty cycle (full-scale duty cycle = 1) in 10 seconds, provided the PWM frequency = 20 kHz, the ACCEL_RATE can be calculated as ACCEL_RATE = 320.

3.1.2.2.5 Block_Rotor_Duration

Block_Rotor_Duration defines the time duration in which the motor blocked rotor condition is allowed before the controller turns off all the PWM. The time taken to turn off all the PWM when the motor is blocked can be calculated using 式 7.

$$\text{Blocked rotor PWM turnoff time}\,(\text{s}) = \frac{\text{Block\_Rotor\_Duration} \times 30{,}000}{25\,\text{MHz}} \quad (7)$$

Where:

- 25 MHz is the TIMER_D clock frequency

For example, if the user wants to turn off the motor if a blocked rotor condition is observed for 1.5 seconds, then:

$$\text{Block\_Rotor\_Duration} = \frac{1.5 \times 25\,\text{MHz}}{30{,}000} = 1250$$

3.1.2.3 Configuring the DRV8323 Registers (drv8323.c)

The register settings of the DRV8323 can be modified by selecting and modifying the file "drv8323.c". See the function "DRV8x_Analog_Init()" to initialize the DRV8323 with modified values. The code snippet of the function is given as follows:

```
void DRV8x_Analog_Init(void)
{
SPI_Write(0x03, 0x03BF);
delay_1ms(1);
SPI_Write(0x03, 0x03BF);
delay_1ms(1);
```


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```
SPI_Write(0x02, 0x0100);
delay_1ms(1);
SPI_Write(0x04, 0x06FF);
delay_1ms(1);
SPI_Write(0x05, 0x0160);
delay_1ms(1);
SPI_Write(0x06, 0x0683);
delay_1ms(1);
}
```

See the DRV8323 datasheet for a detailed understanding of register settings.

3.1.2.4 Initializing SPI Communication Between DRV8323 and MSP430 (drv8323.h)

The register initialization for the DRV8323 is done by means of SPI communication. The SPI communication pins are connected to the ports of the MSP430 MCU. See "drv8323.h" to assign and initialize the ports of the MSP430 MCU for SPI communication. The TIDA-01485 reference design uses port connections as given in 表 4.

表 4. SPI Communication Interface Between DRV8323 and MSP430

DRV8323 PIN	MSP430G2553 PIN
SCS	PJ.0
SCLK	PJ.1
SDI	PJ.2
SDO	PJ.3

Modify the SPI GPIO settings as per the hardware mapping. For this reference design, the mapping is shown in the following code snippet:

```
#define CPU_FREQ_MHZ (25)
/*****************************************************************************
* SPI GPIO Settings (Modify according to hardware mapping)

*****************************************************************************/
#define M1_SCLK_HIGH (PJOUT |= BIT1)
#define M1_SCLK_LOW (PJOUT &= ~BIT1)
#define M1_SDI_HIGH (PJOUT |= BIT2)
#define M1_SDI_LOW (PJOUT &= ~BIT2)
#define M1_SDO_LEVEL ((PJIN &= BIT3)?(1):(0))
#define M1_nSCS_HIGH (PJOUT |= BIT0)
#define M1_nSCS_LOW (PJOUT &= ~BIT0)
/*****************************************************************************/
```

3.1.2.5 Running Project in CCS

To run this project in CCS:

1. Install CCS and import the project "TIDA-01485_Firmware _V1.0".
2. Read through 3.1.2.1 to 3.1.2.4 to customize the code.
3. Power up the board with an external supply as described in 3.1.1 and connect the programmer.
4. Build and debug the modified project to download the code to the MSP430F5132.

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3.2 Testing and Results

3.2.1 Test Setup

図 15 shows the load setup used to test the motor. The load is an electrodynamometer-type load by which the load torque applied to the motor can be controlled.

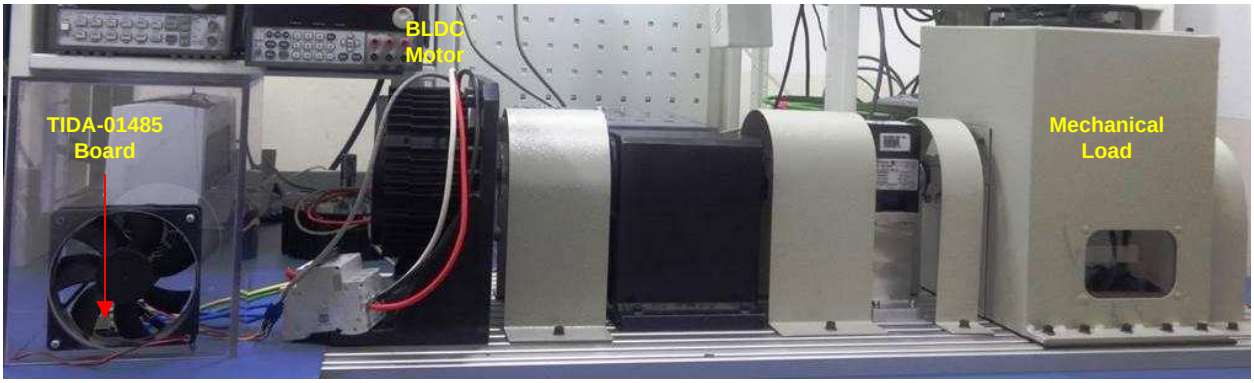

図 15. Board and Motor Test Setup

3.2.2 Functional Tests

3.2.2.1 3.3-V Power Supply Generated by Step-Down Converter

図 16 shows the 3.3 V generated from the step-down converter and the ripple in the 3.3-V rail.

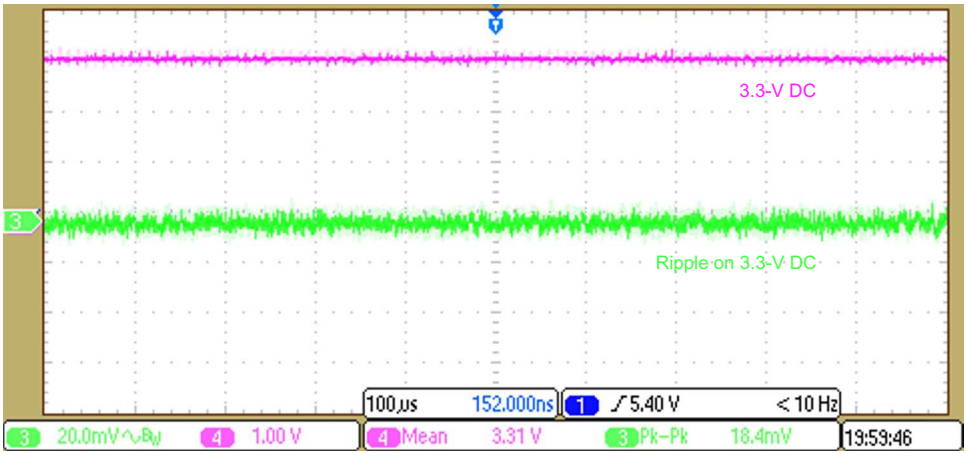

図 16. Output Voltage of 3.3 V From Step-Down Converter and 3.3-V Voltage Ripple

3.2.2.2 Microcontroller PWM and Gate Driver Output

図 17 shows the PWM scheme used in the board for trapezoidal control of the BLDC motor. The controls is a six-step block commutation where PWM is applied to top switch and bottom switch is operated in active freewheeling.

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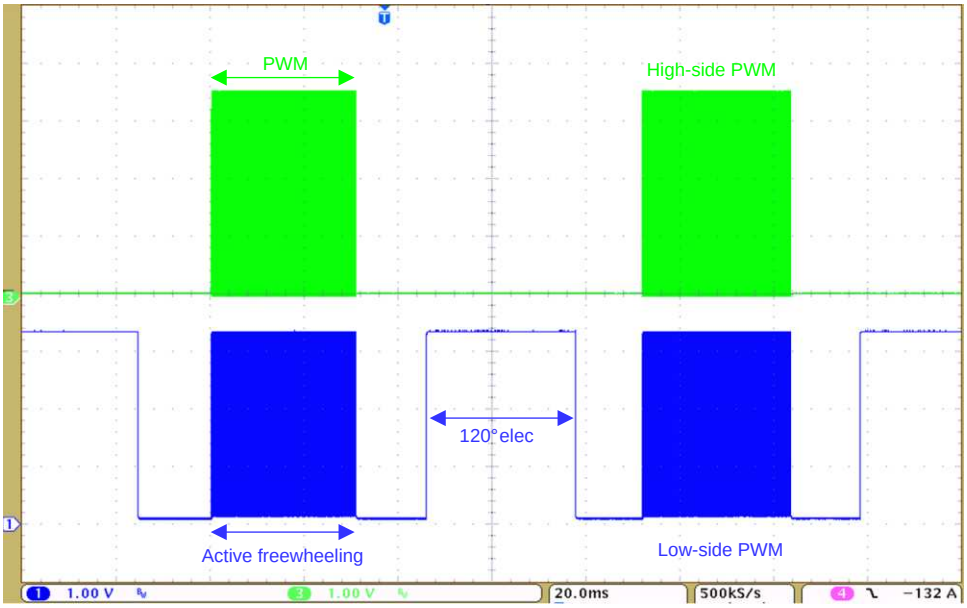

図 17. Low- and High-Side FET PWM Generated by MCU for Trapezoidal Control

図 18 shows the gate drive output voltage of the DRV8323 and the corresponding MCU PWM signals at a DC bus voltage of 36-V DC. The gate drive voltage is approximately 11 V, which means effective gate driving of standard MOSFETs. 図 19 shows the gate drive voltage of the DRV8323 at a DC bus voltage of 8 V. The gate drive output voltage is approximately 6.5 V.

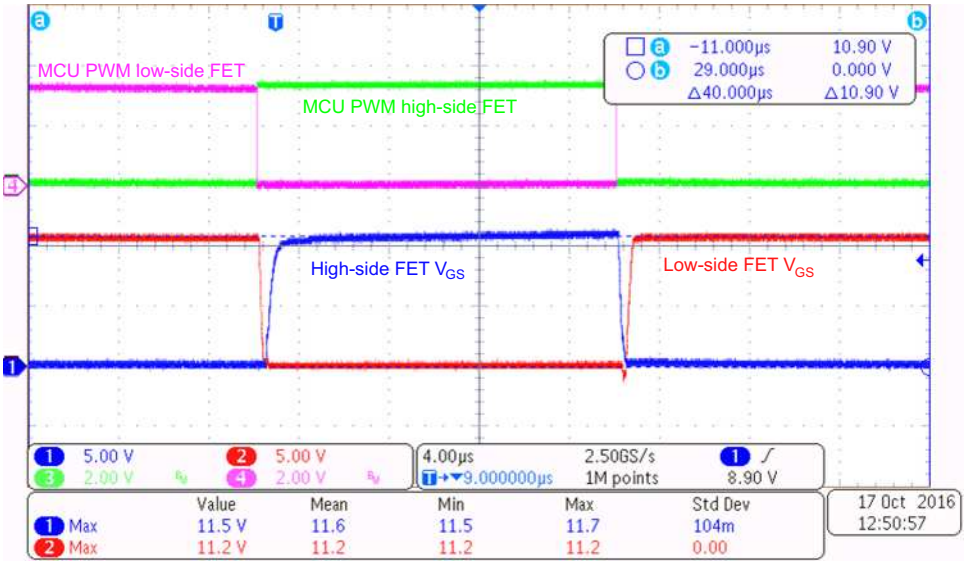

図 18. Low- and High-Side Gate Drive Voltage at 36-V DC

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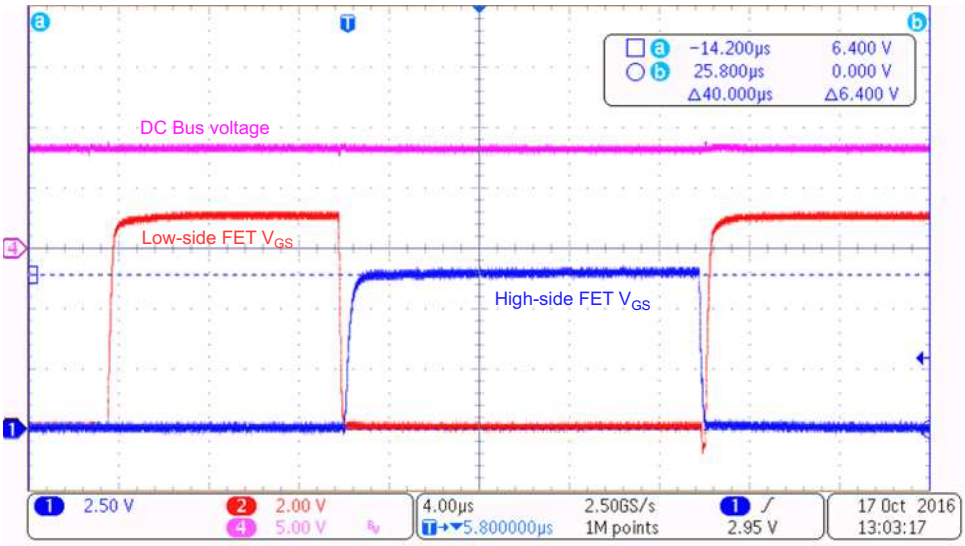

図 19. High- and Low-Side Gate Drive Voltage at 8-V DC

3.2.2.3 Dead Time From DRV8323

図 20 and 図 21 shows the high-side and low-side gate source voltage from the DRV8323, which shows the dead time inserted by the DRV8323 at the both the edges of the PWM. The dead is programmed to 100 ns. The DRV8323 inserts the dead time after the V_{GS} handshake.

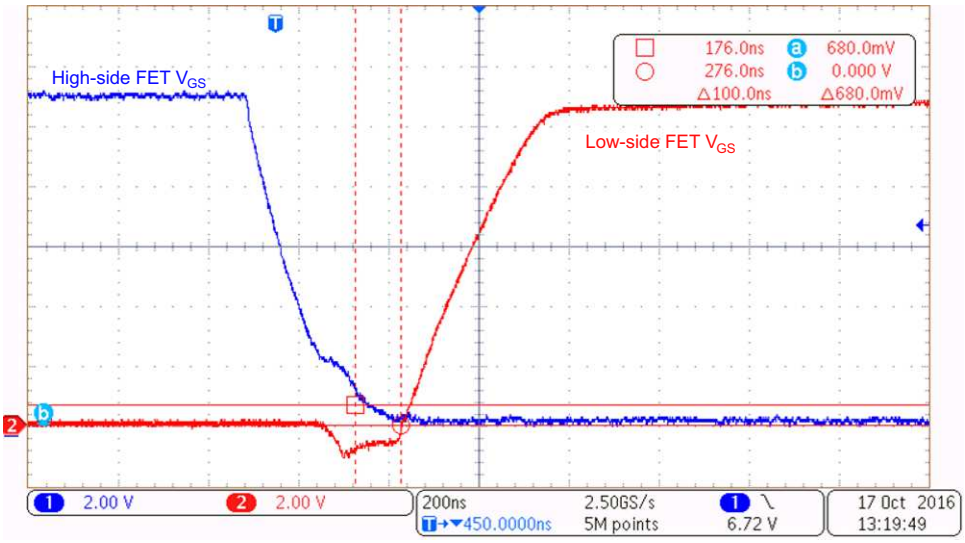

図 20. Dead Time at Rising Edge of Low-Side V_{GS}

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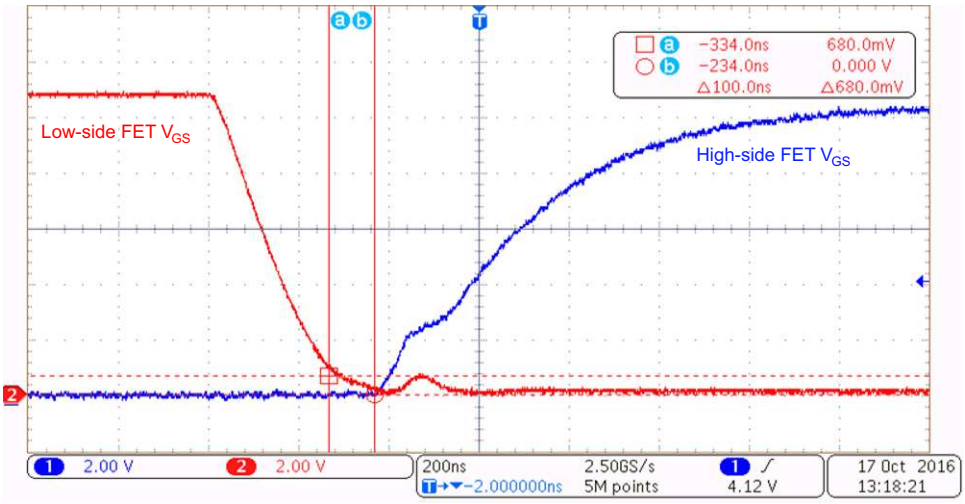

図 21. Dead Time at Trailing Edge of Low-Side V_{GS}

3.2.2.4 MOSFET Switching Waveforms

図 22 to 図 25 show the V_{DS} and V_{GS} waveforms of the low-side and high-side MOSFETs at a gate current of the DRV8323 (IDRIVE) is set at a 120-mA source (the low gate charge of the CSD88599 allows low source current) and a 2-A sink current. Switching waveforms are clean without much overvoltage ringing due to the following:

- The power block has both the high-side and low-side switches in same package, which reduces the parasitic inductance and hence reduces the phase node voltage ringing.
- The current controlled gate driver with slew rate control helps to optimize the switching.
- The IDRIVE and TDRIVE features of the gate driver helps to shape the gate current to optimize the switching.

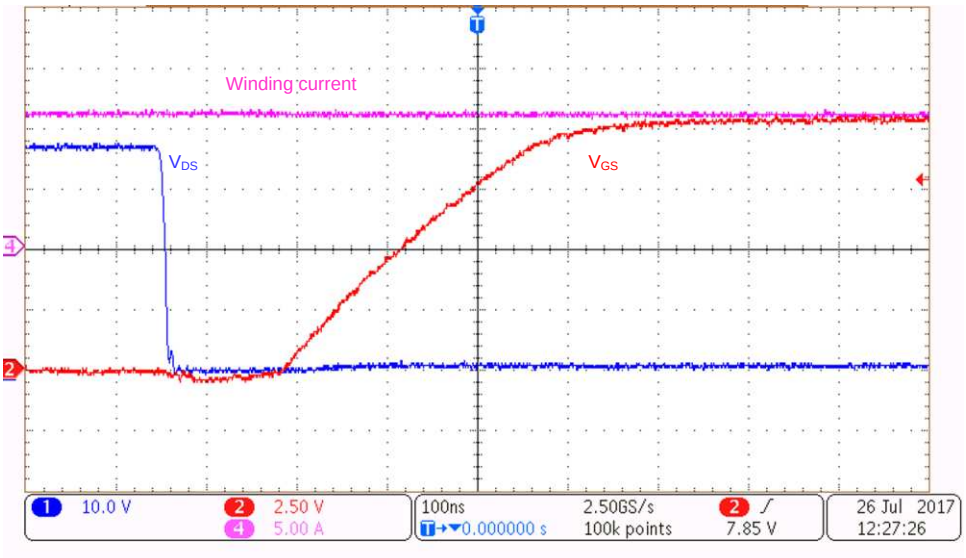

図 22. Turnon: Low-Side V_{GS} and V_{DS} at 12-A Winding Current

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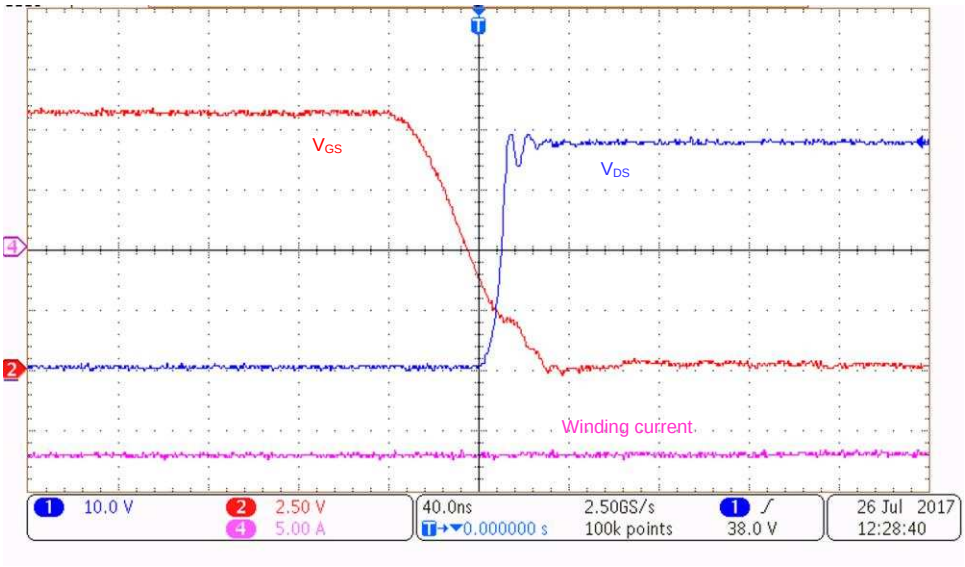

図 23. Turnoff: Low-Side V_{GS} and V_{DS} at 18-A Winding Current

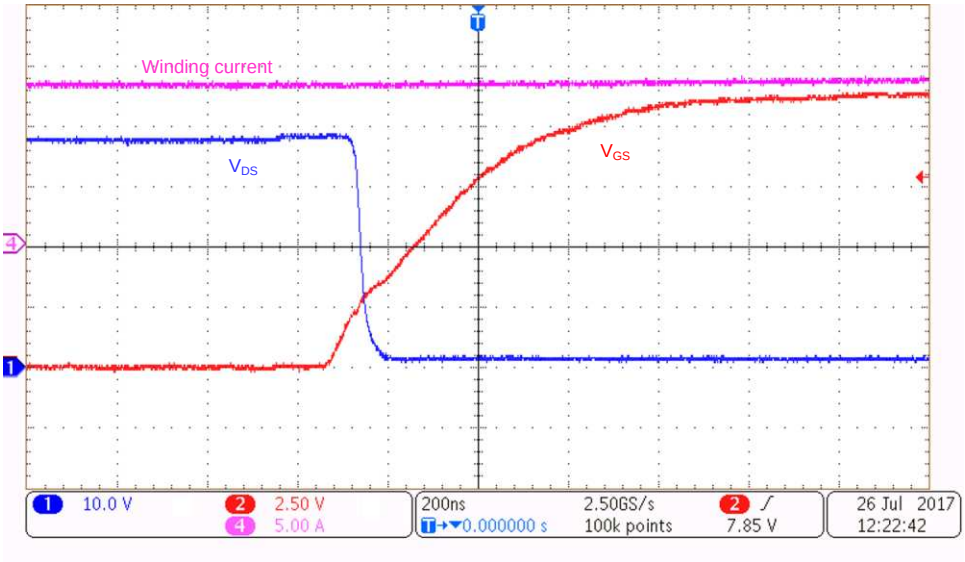

図 24. Turnon: High-Side V_{GS} and V_{DS} at 14-A Winding Current

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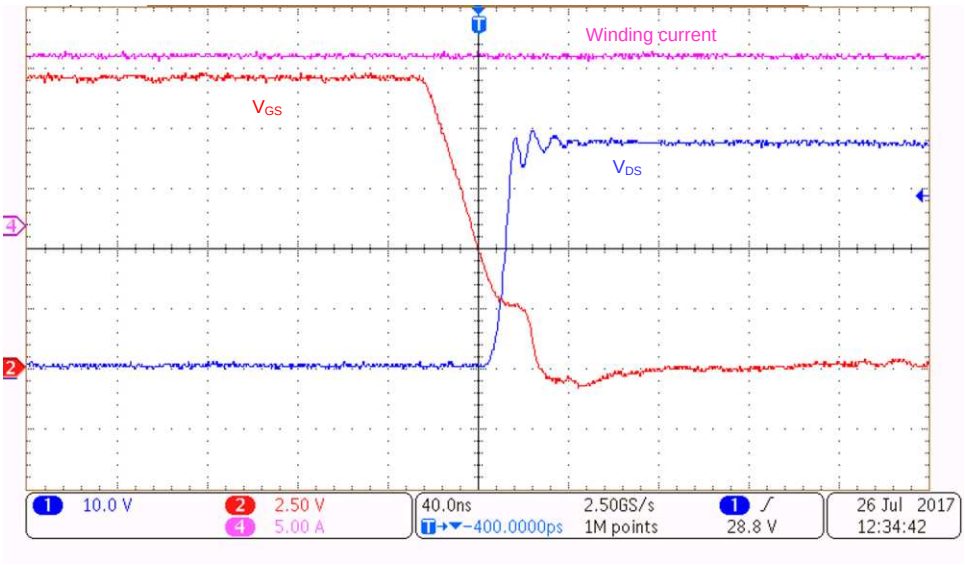

図 25. Turnoff: High-Side V_{GS} and V_{DS} at 16 A Winding Current

3.2.3 Load Test

The reference design board is tested with an external BLDC motor and load using the test setup in 図 15. The testing is done with and without heat sink at different airflow conditions and different duty cycles. The key results are summarized in 3.2.3.1 through 3.2.3.3.

3.2.3.1 Load Test Without Heat Sink

図 26 shows the motor winding current and winding voltage waveforms at a 36-V DC input and a 17.4-A_{RMS} winding current. The result is listed in 表 5. The testing is done at 100% duty cycle. 図 27 shows the steady state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 88°C.

表 5. Load Test Results at 100% Duty Cycle Without Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	MAXIMUM FET TEMPERATURE
36	19.4	17.4	698	88°C

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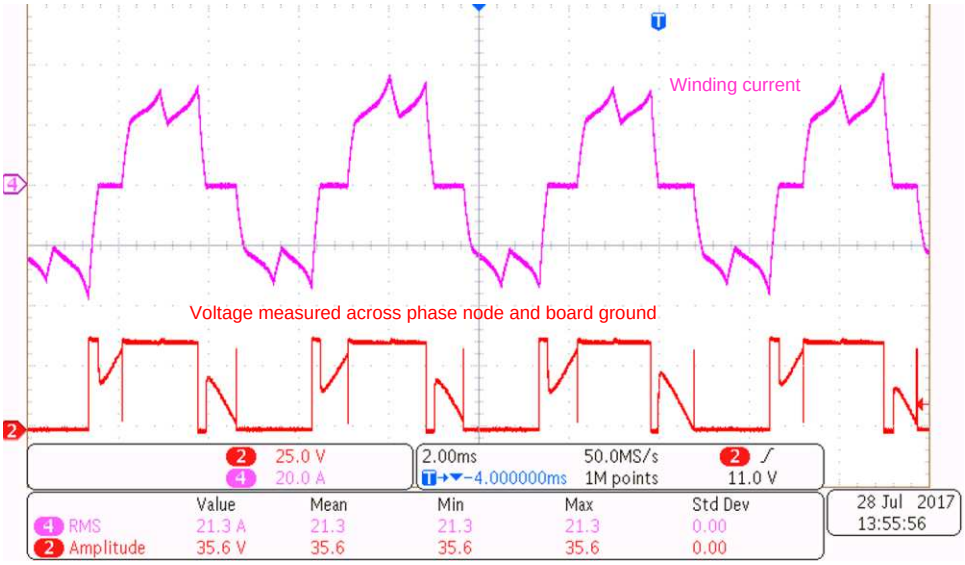

図 26. Load Test Results at 36-V DC Input, 17.4-A_{RMS} Winding Current, 100% Duty Cycle

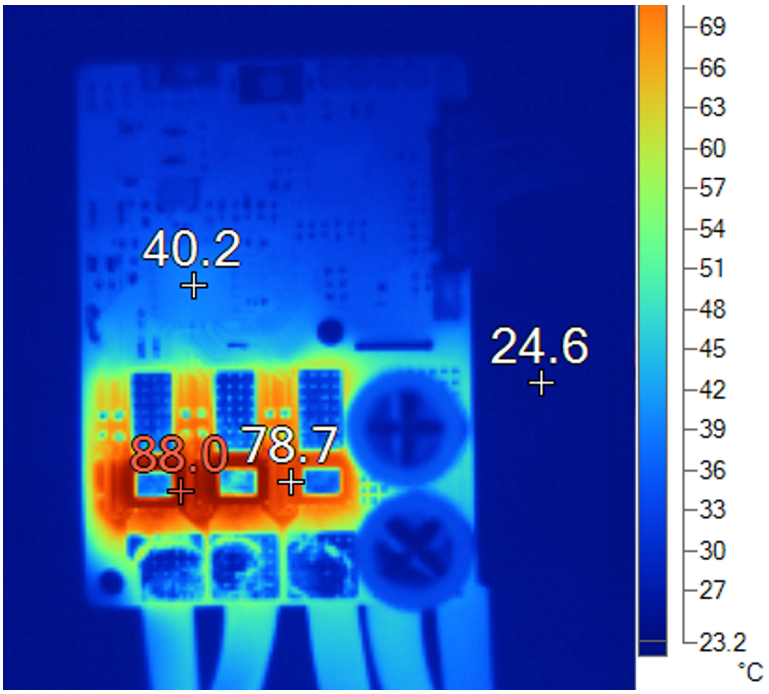

図 27. Thermal Image at 36-V DC Input, 17.4-A_{RMS} Winding Current, 100% Duty Cycle

図 28 shows the motor winding current and winding voltage waveforms at a 36-V DC input and a 18.6-A_{RMS} winding current at 95% duty cycle. The result is listed in 表 6. The testing is done at 95% duty cycle. 図 29 shows the steady state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 102°C.

表 6. Load Test Results at 95% Duty Cycle Without Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	MAXIMUM FET TEMPERATURE
36	19.3	18.6	695	102°C

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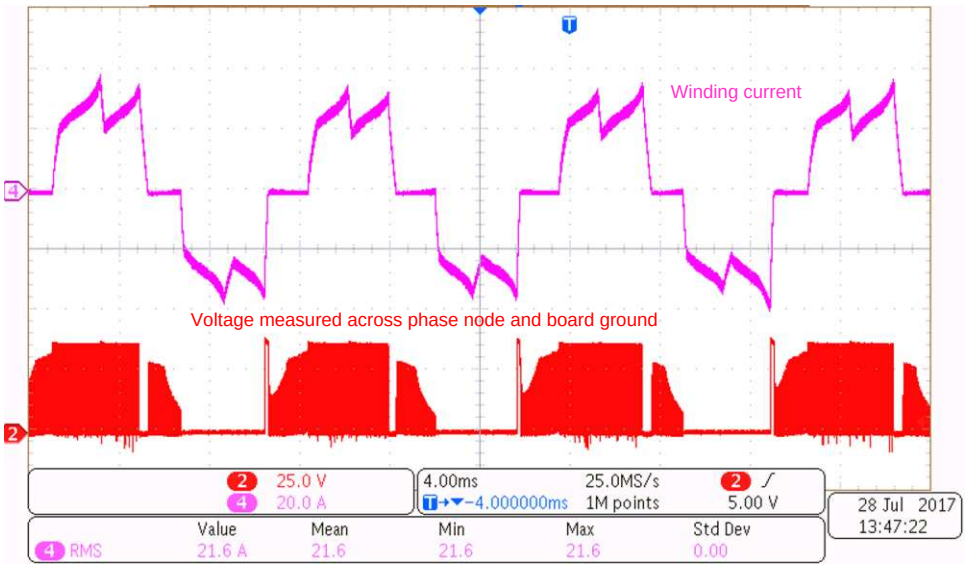

図 28. Load Test Results at 36-V DC Input, 18.6-A_{RMS} Winding Current, 95% Duty Cycle

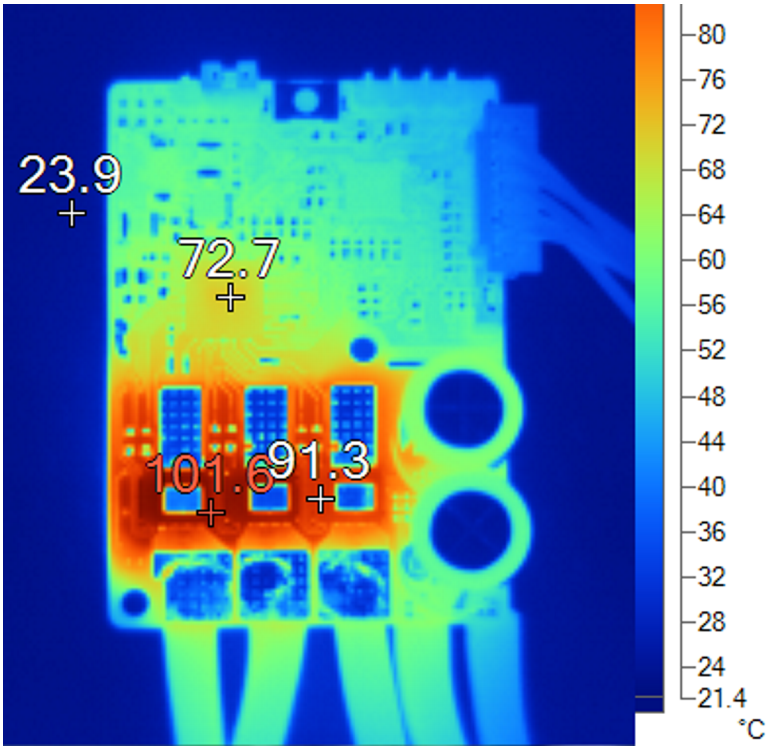

図 29. Thermal Image at 36-V DC Input, 18.6-A_{RMS} Winding Current, 95% Duty Cycle

3.2.3.2 Load Test With Heat Sink

図 30 shows a board image with the heat sink connected. The testing is done at a 95% duty cycle with the top-side heat sink connected. The result is listed in 表 7. 図 31 shows the steady-state thermal image of the board at the same condition, captured after 10 minutes of continuous running. The maximum FET temperature observed is 98°C.

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表 7. Load Test Results at 95% Duty Cycle With Heat Sink

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	MAXIMUM FET TEMPERATURE
36	26.2	25.3	943	98°C

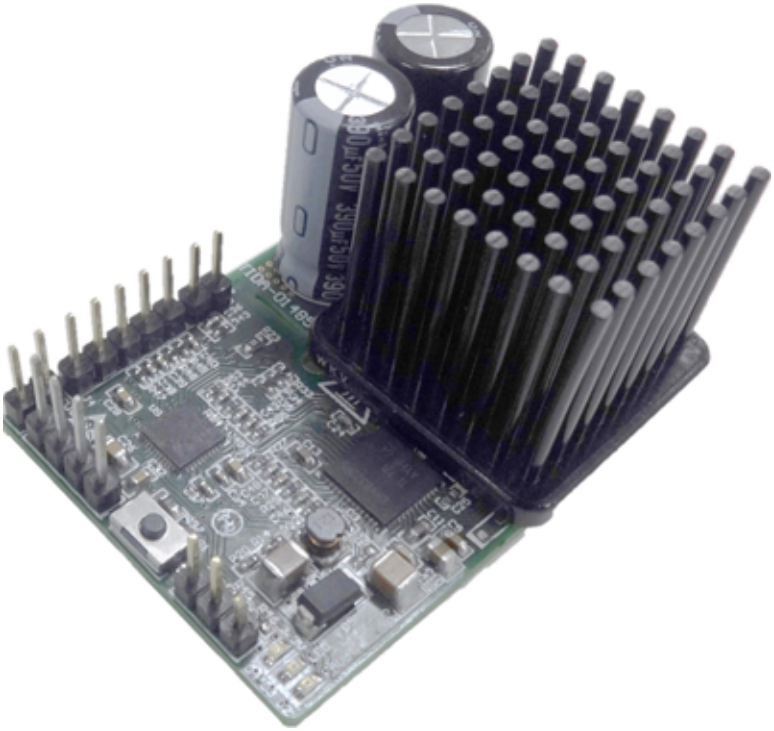

図 30. Board Image With Heat Sink

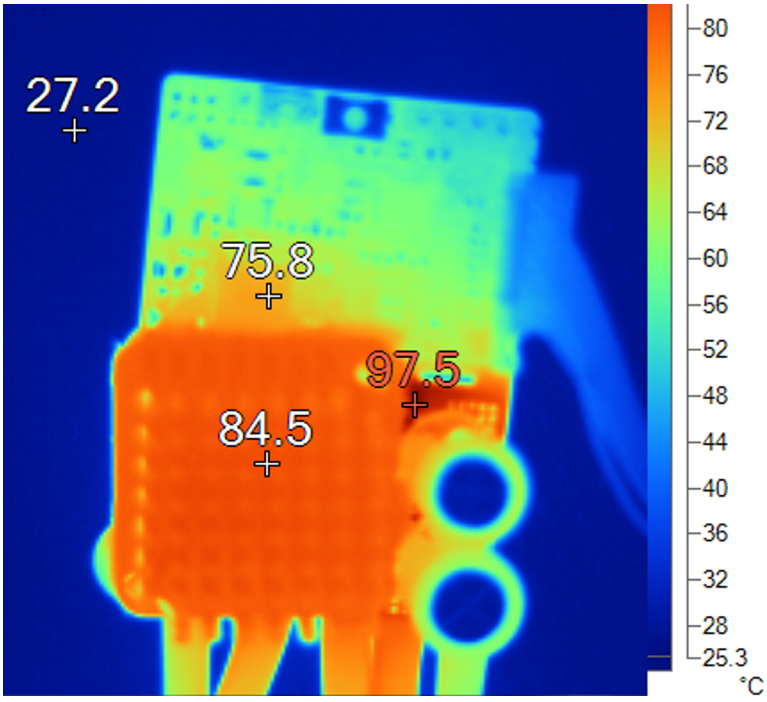

図 31. Thermal Image at 36-V DC Input, 25.3-A_{RMS} Winding Current, 95% Duty Cycle

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3.2.3.3 Load Test at Different Airflow Conditions

The testing is done with and without the heat sink at different airflow conditions and different duty cycles. The key results are summarized in 表 8 and the effect of airflow at different test conditions are plotted in 図 32 to 図 35.

表 8. Summary of Load Test Results at Different Conditions

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	INPUT POWER (W)	MAXIMUM FET TEMPERATURE	DUTY CYCLE	AIRFLOW (LFM)	TEST CONDITION
TESTING WITHOUT HEAT SINK AT DUTY CYCLE = 1							
36	19.4	17.4	698.0	90.0°C	1	0	No heat sink
36	24.8	22.6	892.8	89.0°C	1	300	No heat sink
36	26.6	24.4	957.6	90.4°C	1	400	No heat sink
36	28.0	25.7	1008.0	93.0°C	1	500	No heat sink
TESTING WITHOUT HEAT SINK AT DUTY CYCLE = 0.95							
36	19.3	18.6	693.036	102°C	0.95	0	No heat sink
36	26.1	25.2	938.952	103°C	0.95	400	No heat sink
TESTING WITHOUT HEAT SINK AT DUTY CYCLE = 1							
36	30.1	27.1	1085	107°C	1	0	With heat sink
36	30.0	27.1	1080	84°C	1	100	With heat sink
TESTING WITH HEAT SINK AT DUTY CYCLE = 0.95							
36	26.2	25.3	942.678	99.0°C	0.95	0	With heat sink
36	28.5	27.5	1024.650	81.0°C	0.95	100	With heat sink
36	28.5	27.5	1024.650	70.2°C	0.95	200	With heat sink

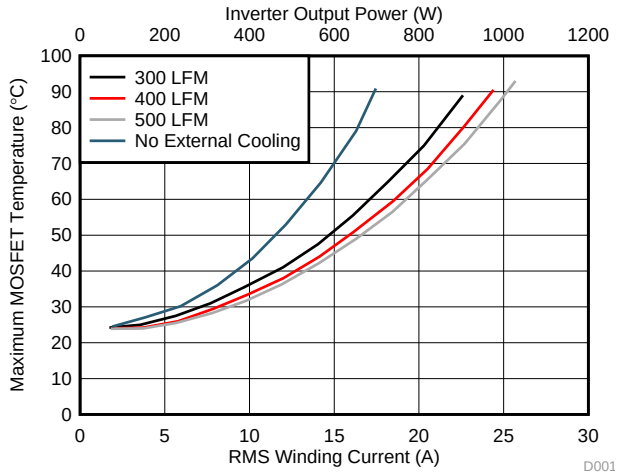

図 32. Load Test Results at 36-V DC Input, 100% Duty Cycle Without Heat Sink at Different Airflow

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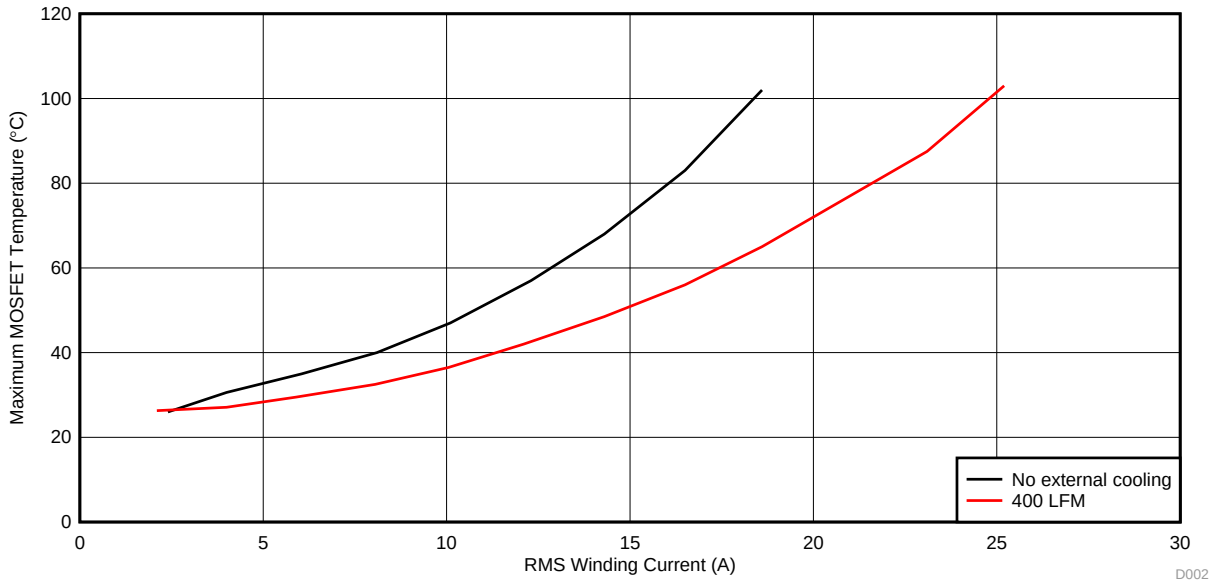

図 33. Load Test Results at 36-V DC Input, 95% Duty Cycle Without Heat Sink at Different Airflow

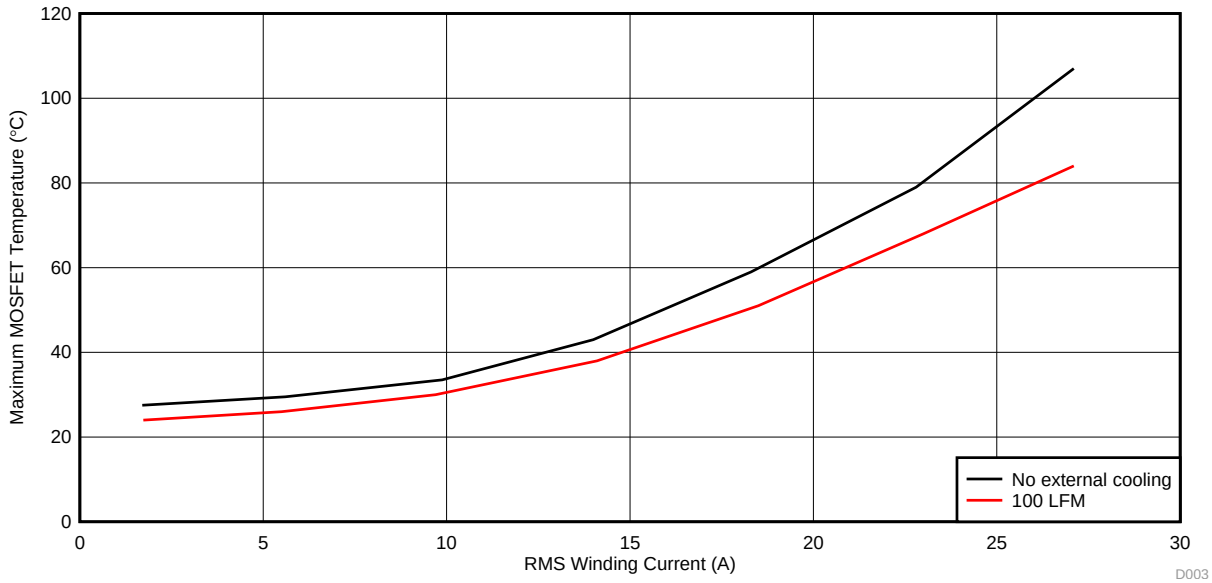

図 34. Load Test Results at 36-V DC Input, 100% Duty Cycle With Heat Sink at Different Airflow

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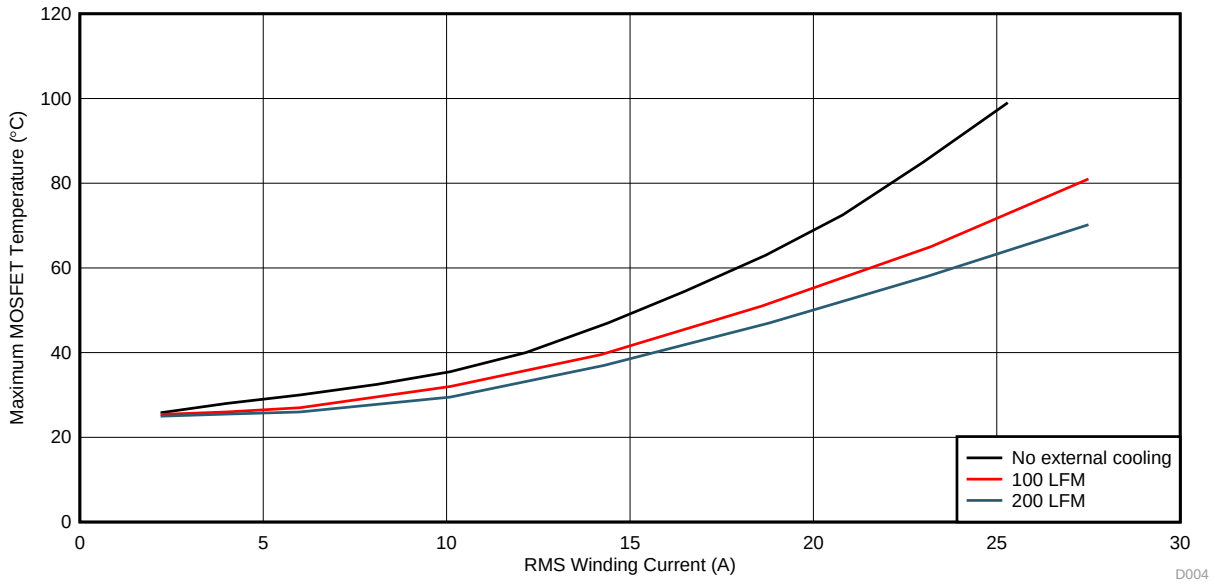

図 35. Load Test Results at 36-V DC Input, 95% Duty Cycle With Heat Sink at Different Airflow

3.2.4 Inverter Efficiency

The inverter efficiency is experimentally tested with a load setup as shown in 図 15. The test results without a heat sink and at a 100% duty cycle are listed in 表 9. The test results without a heat sink and at a 95% duty cycle are listed in 表 10.

表 9. Inverter Efficiency Test Results at 100% Duty Cycle Without Heat Sink and Without Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY	INVERTER LOSS (W)
36.11	2.53	2.12	91.44	90.99	99.51%	0.45
35.95	7.10	5.99	255.32	254.46	99.66%	0.86
35.91	11.77	10.13	422.76	420.81	99.54%	1.95
35.92	16.34	14.31	586.91	582.81	99.30%	4.10
35.81	20.83	18.57	745.80	739.10	99.10%	6.70
35.75	25.33	22.87	905.51	895.15	98.86%	10.36

表 10. Inverter Efficiency Test Results at 95% Duty Cycle Without Heat Sink and Without Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY	INVERTER LOSS (W)
36.06	2.21	1.93	79.72	79.03	99.14%	0.69
35.90	6.65	5.85	238.76	237.51	99.48%	1.25
35.84	11.12	10.04	398.66	396.08	99.35%	2.58
35.97	15.48	14.25	556.81	551.60	99.06%	5.21
35.99	19.76	18.53	711.37	702.68	98.78%	8.69
36.02	24.00	22.86	864.37	851.69	98.53%	12.68

The test results without a heat sink but with a 300LFM airflow and at a 100% duty cycle are listed in 表 11. The test results without a heat sink but with a 300LFM airflow and at a 95% duty cycle are listed in 表 12.

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表 11. Inverter Efficiency Test Results at 100% Duty Cycle Without Heat Sink and at 300LFM Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY	INVERTER LOSS (W)
36.19	2.35	1.95	85.12	84.69	99.49%	0.43
35.75	7.02	5.89	251.02	250.26	99.70%	0.76
35.95	11.85	10.08	426.11	424.50	99.62%	1.61
35.96	16.62	14.30	597.50	594.17	99.44%	3.33
36.00	21.35	18.56	768.51	763.08	99.29%	5.43
35.88	26.06	22.91	935.30	927.18	99.13%	8.12
35.88	28.45	25.40	1020.54	1010.78	99.04%	9.76

表 12. Inverter Efficiency Test Results at 95% Duty Cycle Without Heat Sink and at 300LFM Airflow

INPUT DC VOLTAGE (V)	INPUT DC CURRENT (A)	RMS WINDING CURRENT (A)	DC INPUT POWER (W)	INVERTER OUTPUT POWER (W)	INVERTER EFFICIENCY	INVERTER LOSS (W)
36.16	2.07	1.81	74.77	74.10	99.11%	0.67
36.04	6.59	5.80	237.45	236.29	99.51%	1.16
36.02	11.08	10.02	399.27	397.02	99.43%	2.26
36.00	15.46	14.26	556.34	552.22	99.26%	4.12
35.94	19.73	18.57	708.96	702.00	99.02%	6.96
35.90	24.07	22.89	864.20	853.33	98.74%	10.87
35.98	26.13	25.13	940.30	927.55	98.64%	12.74

The efficiency curve of these test conditions are plotted in 図 36.

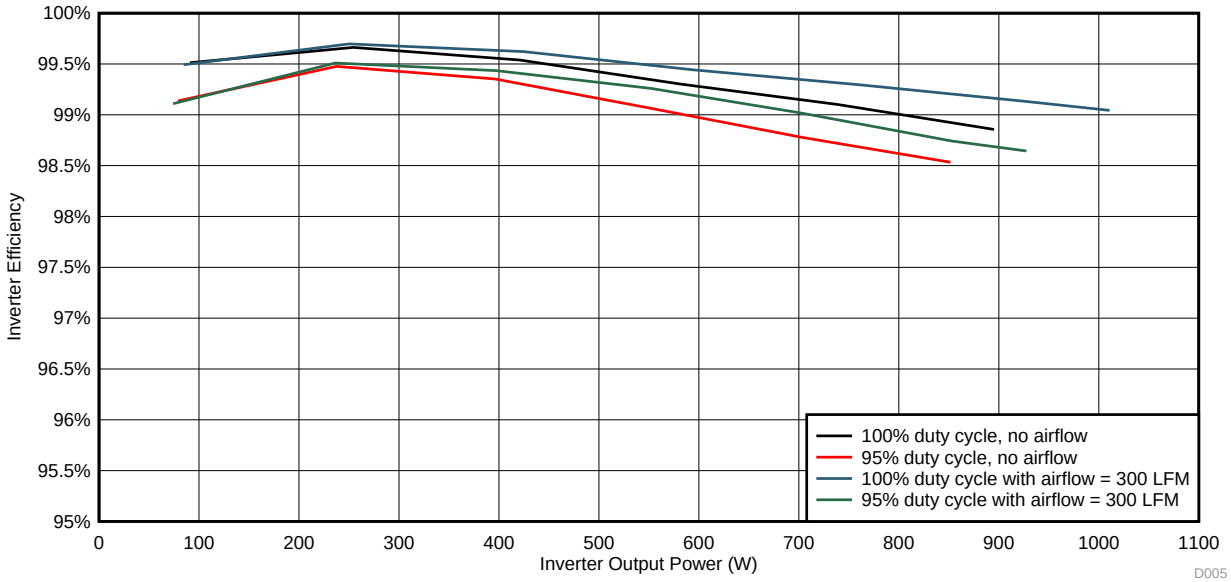

図 36. Inverter Efficiency versus Output Power

The reference design could achieve the high efficiency due to the following key factors:

- Low R_{DS_ON} of the MOSFET power block reducing the conduction losses
- Clean FET switching reducing the switching losses and diode losses
- Power block allows small PCB form factor and hence enable low PCB track resistance leads to

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minimum PCB losses

- The V_{GS} handshake feature of the gate driver allows minimum dead time, reducing the diode loss.

3.2.5 Inverter Current Sensing by V_{DS} Amplification

The inverter leg current sensing is done by monitoring the V_{DS} of the low-side MOSFETs. 図 37 shows the test results at a 100% duty cycle. As shown in 図 17, at a 100% duty cycle the low-side FET conducts for a 120-degree electrical period and that corresponds to the negative half cycle of the corresponding phase current waveform as shown in 図 37. The waveform is captured at the test conditions given in 表 13.

表 13. Test Condition for Inverter Current Sensing by V_{DS} Monitoring Using DRV8323

PARAMETER	VALUE
Measured MOSFET R_{DS_ON} at 25°C	1.83 mΩ
DRV8323 current sense amplifier gain	20 V/V
DRV8323 current sense amplifier reference voltage	V_{REF}/2 = 1.64 V (measured on the board)
DRV8323 – t_{DRIVE}	1 µs

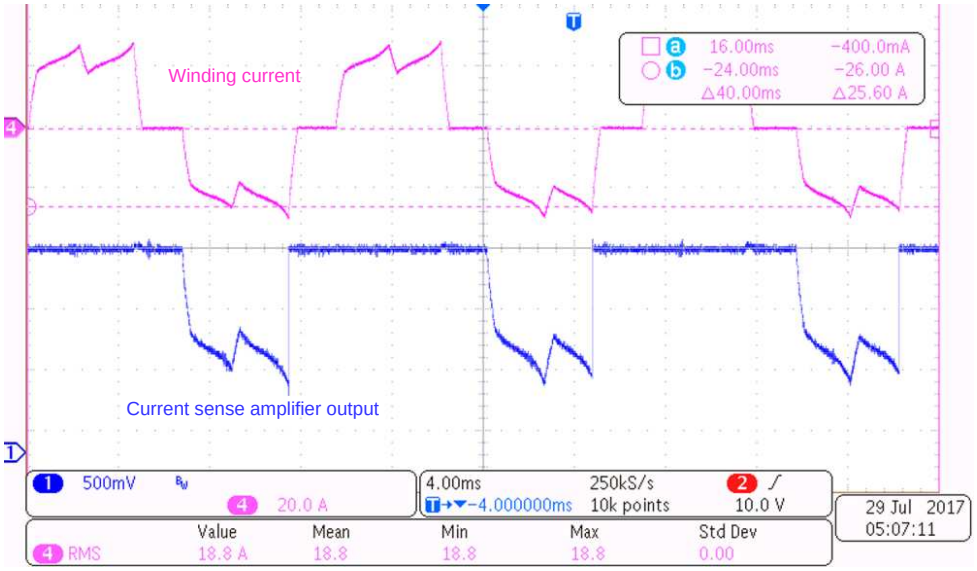

図 37. DRV8323 Current Sense Amplifier Output at 100% Duty Cycle

図 38 shows the test results at a 52% duty cycle. As shown in 図 17, at a 52% duty cycle the low-side FET conducts for a 120-degree electrical period and conducts complimentary to the top-side PWM during the positive winding current. The waveforms are captured at same conditions as given in 表 13.

図 39 shows the PWM zoomed view with these conditions and shows that the sense amplifier output is pretty clean with minimum switching noise, allowing a fast and accurate current sample.

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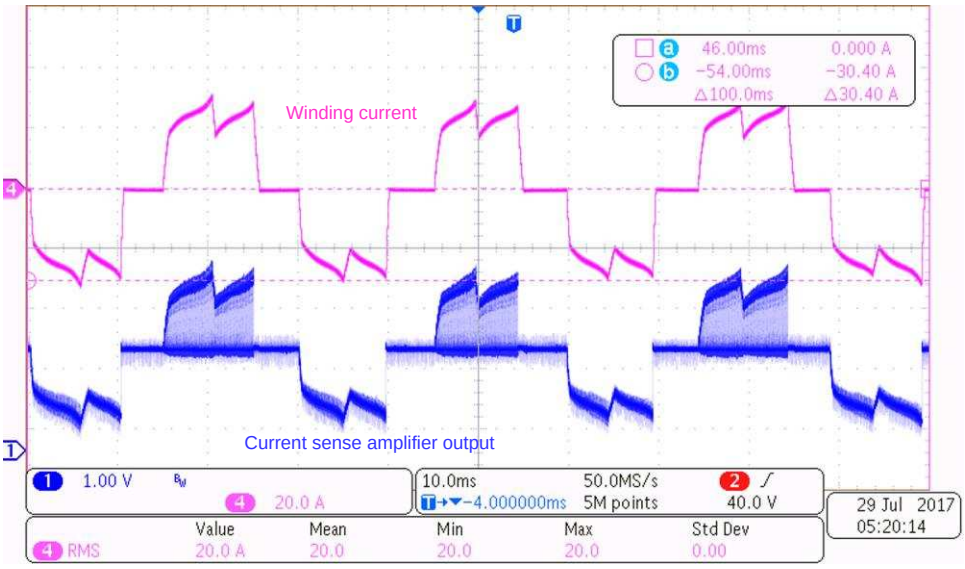

図 38. DRV8323 Current Sense Amplifier Output at 52% Duty Cycle

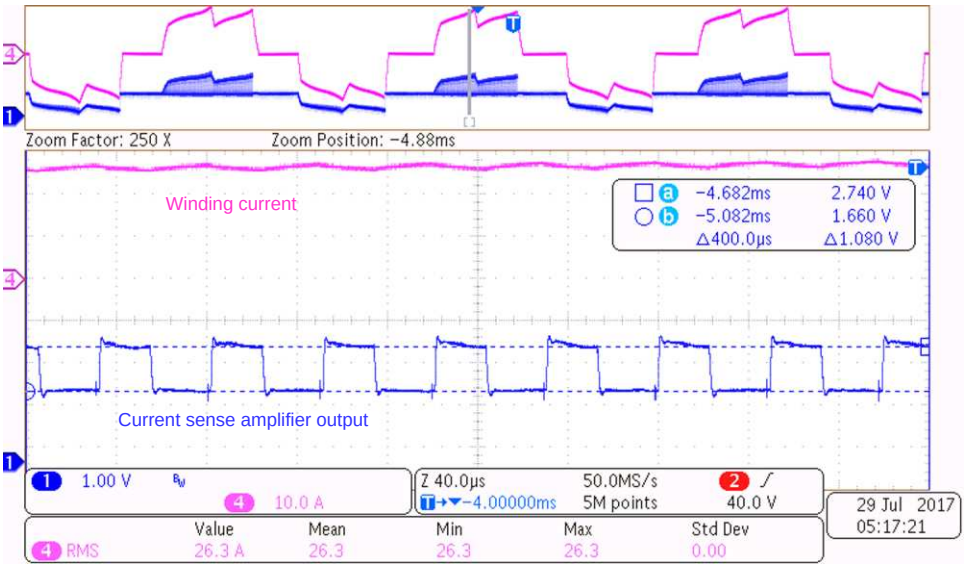

図 39. PWM Cycle View of DRV8323 Current Sense Amplifier Output at 52% Duty Cycle

3.2.6 Overcurrent and Short-Circuit Protection Test

3.2.6.1 Cycle-by-Cycle Overcurrent Protection by V_{DS} Monitoring

図 40 shows the cycle-by-cycle peak current limit by the DRV8323 when the motor is loaded more than the set current limit. The test conditions are specified in 表 14.

表 14. Test Condition for Cycle-by-Cycle Overcurrent Protection by DRV8323

PARAMETER	VALUE
Measured MOSFET R_{DS_ON} at 25°C	1.83 mΩ
V_{DS} threshold	0.06 V
DRV8323 – t_{DRIVE}	1 µs

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表 14. Test Condition for Cycle-by-Cycle Overcurrent Protection by DRV8323 (continued)

PARAMETER	VALUE
Duty cycle deglitch time (OCP_DEG)	2 µs
DRV8323 – TDRIVE overcurrent protection mode (OCP_MODE)	Overcurrent causes an automatic retrying fault

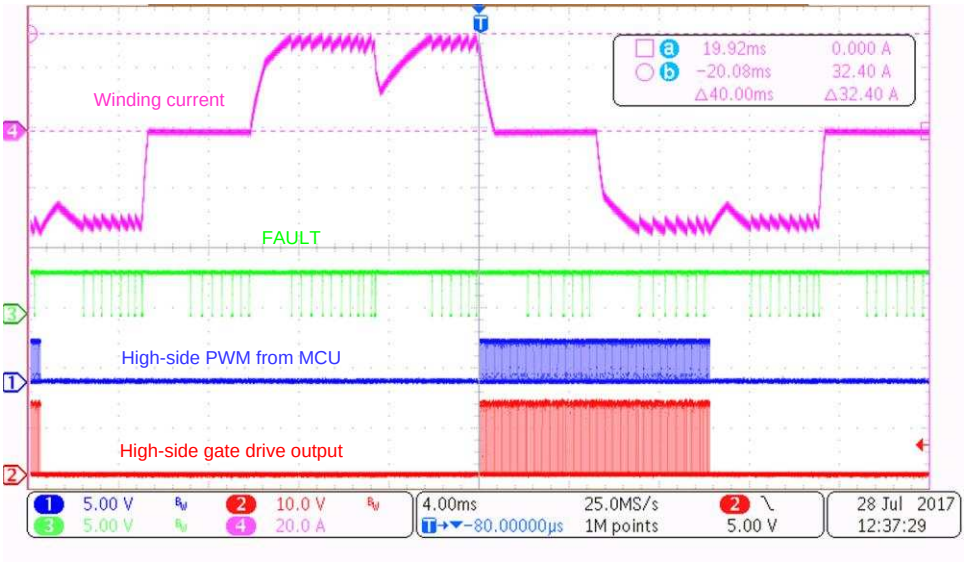

図 40. Cycle-by-Cycle Overcurrent Limit by DRV8323

Assuming the junction temperature of 75°C, the R_{DS_ON} at 75°C ≈ 2.379 mΩ (approximately 1.3 times the R_{DS_ON} at 25°C, from the CSD88599Q5DC datasheet).

Current limit threshold = V_{DS} threshold / R_{DS_ON} = 25.22 A

図 40 shows that the current is limited at 32.4 A. 図 41 shows the zoomed view where the PWM shuts off when the current hits 32.4 A and the fault is created. The fault reset at the next PWM rising edge.

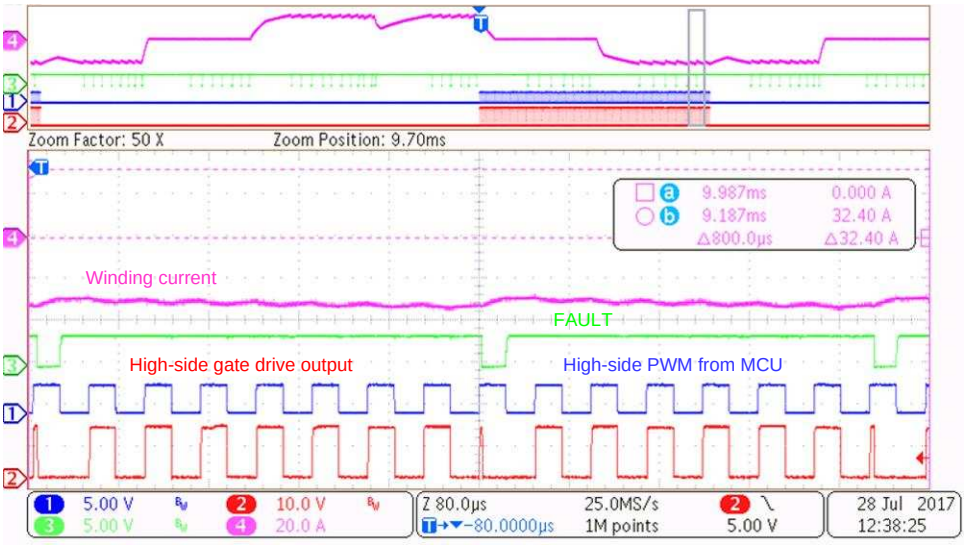

図 41. Cycle-by-Cycle Overcurrent Limit Showing PWM Shutoff

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3.2.6.2 Cycle-by-Cycle Short-Circuit Protection by V_{DS} Monitoring

The test conditions as per 表 15 are used for all the test results in this section and 3.2.6.3.

表 15. Test Conditions for Short-Circuit Protection by V_{DS} Monitoring

PARAMETER	VALUE
Measured MOSFET R_{DS_ON} at 25°C	1.83 mΩ
V_{DS} threshold	0.06 V
DRV8323 – t_{DRIVE}	1 µs
Deglitch time (OCP_DEG)	2 µs
Supply voltage	36 V

Current limit threshold = V_{DS} threshold / R_{DS_ON} = 32.7 A

This means once the current of 32.7 A reaches the V_{DS} comparator in the gate driver trips and wait for a delay deglitch period set by OCP_DEG, before turning off the MOSFET, to ensure that the overcurrent trip is caused by actual overcurrent event and not by any noise signal. But the circuit current increases from 32.7 A to a higher value within the deglitch time. The increase in current is determined by OCP_DEG, short circuit resistance, inductance, and applied DC bus voltage.

For example, assuming:

- Short circuit inductance, L_{SC} = 2 µH
- Driving voltage during short circuit = 36 V (VDC)
- Short circuit resistance, R_{SC} = 0 Ω (for simplicity of analysis)

The increase in current in OCP_DEG can be calculated as in 式 8.

$$\Delta I = \frac{V_{SC}}{L_{SC}} \times \Delta t = 36 \text{ A} \tag{8}$$

The inverter is shorted with a copper wire at the output of the three-phase inverter of this reference design. The expected peak current setting ≈ 32.7 + 36 = 68.7 A

図 42 shows the test setup to simulate a short circuit at the inverter output.

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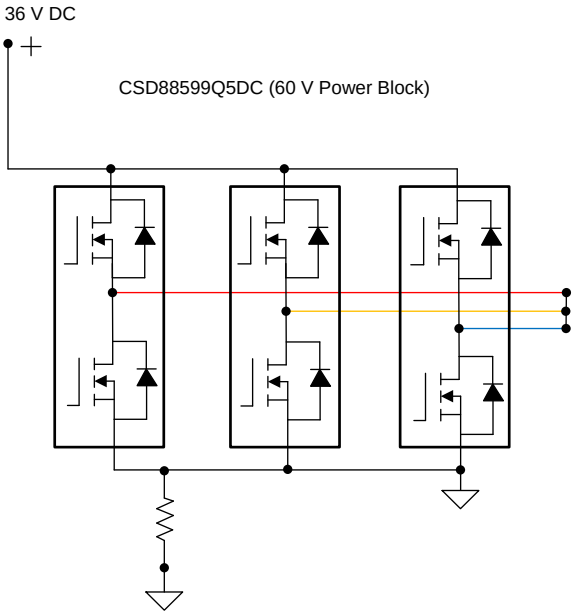

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図 42. Test Setup to Simulate Inverter Short Circuit

図 43 shows the overcurrent protection acted at around 65 A. Once the current hits 65 A, the PWM shuts off immediately and the response time is less than 1 µs.

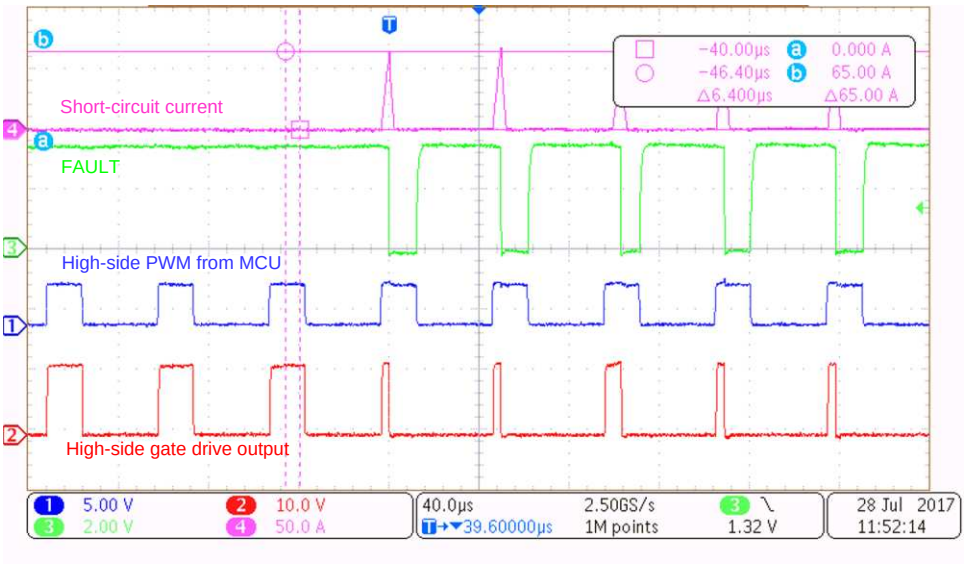

図 43. Cycle-by-Cycle Overcurrent Protection With Inverter Output Shorted

図 44 shows the test setup to simulate a stall current when the motor is rotating. SW is a single-throw, double-pole switch connect between the motor terminals. This switch is used to create a motor winding to a winding short.

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Before SW is closed, the motor was rotating at a steady speed. 図 45 shows the waveforms obtained when the switch SW is closed. When SW is closed, SW carries the short-circuit current. During this condition the motor stops, which causes the Hall state to continue at the current commutation state; therefore, the controller continues to generate the PWM corresponding to this commutation state. The overcurrent protection acted at around 70 A and the PWM shuts off immediately with response time less than 1 µs. 図 45 shows the test results with motor stall condition.

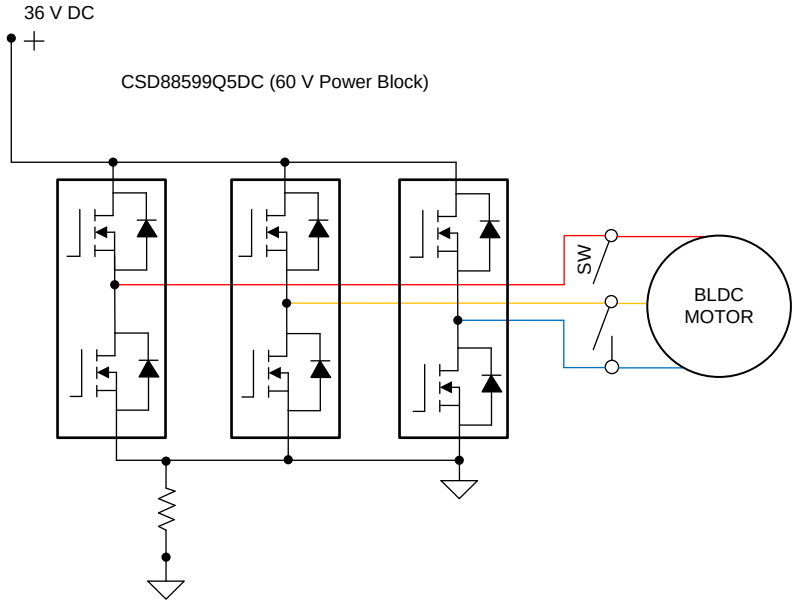

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図 44. Test Setup to Simulate Stall Current When Motor is Running

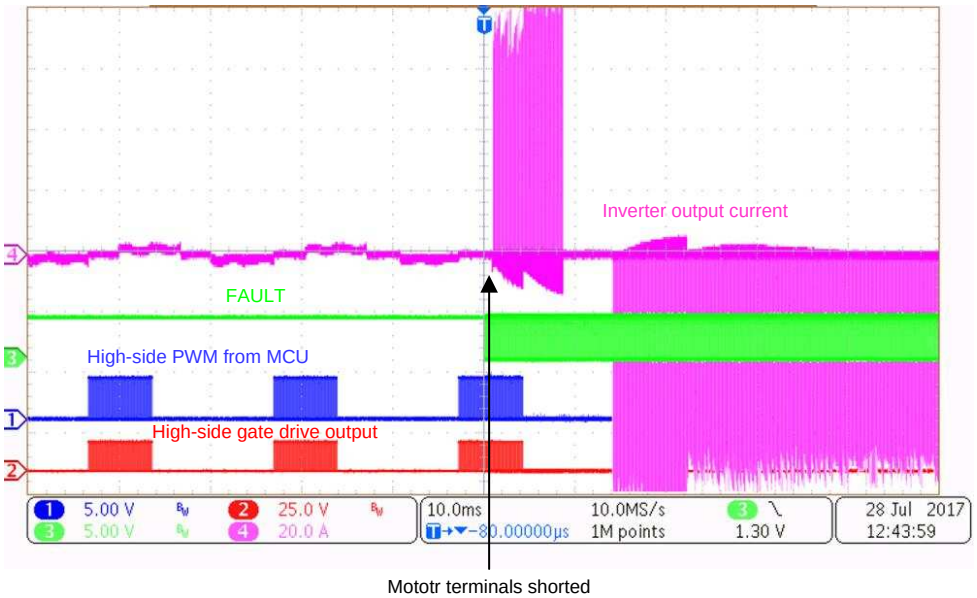

図 45. Cycle-by-Cycle Overcurrent Protection With Motor Stall

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3.2.6.3 Stall Current Latch Protection by DRV8323 V_{DS} Monitoring

The same test setup in 図 44 is used for the stall current protection. 図 46 shows the test results with latch protection by V_{DS} sensing. When a V_{DS} overcurrent event occurs, the device pulls all gate drive outputs low to put all six external MOSFETs into high-impedance mode. The fault is reported on the nFAULT pin with the specific MOSFET in which the overcurrent event detected is reported through the SPI status registers. 図 47 shows a zoomed view of 図 46. The response time from overcurrent detection to the turnoff of the gate drive output is less than 1 µs and the peak current observed is 72 A.

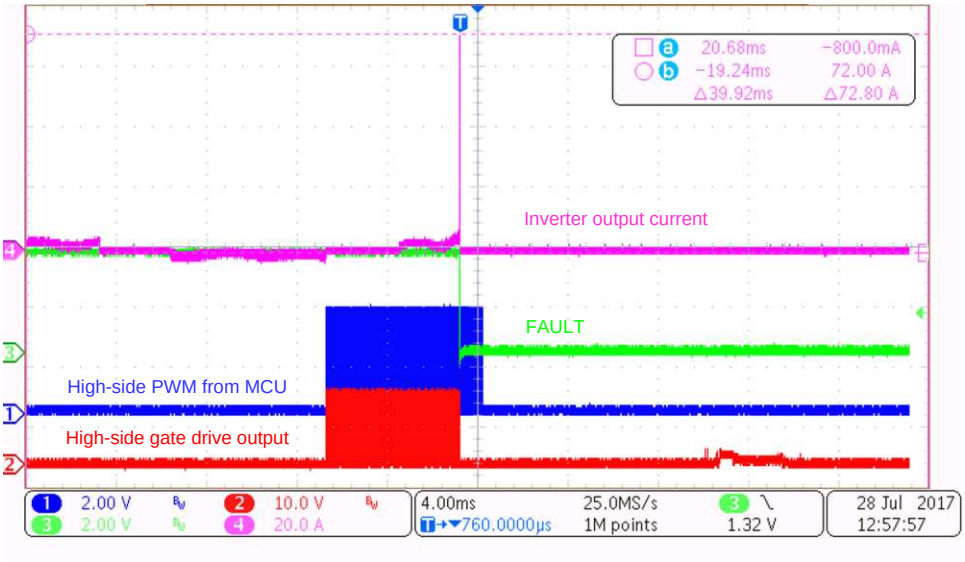

図 46. Overcurrent Latch Protection With Motor Stall by V_{DS} Monitoring

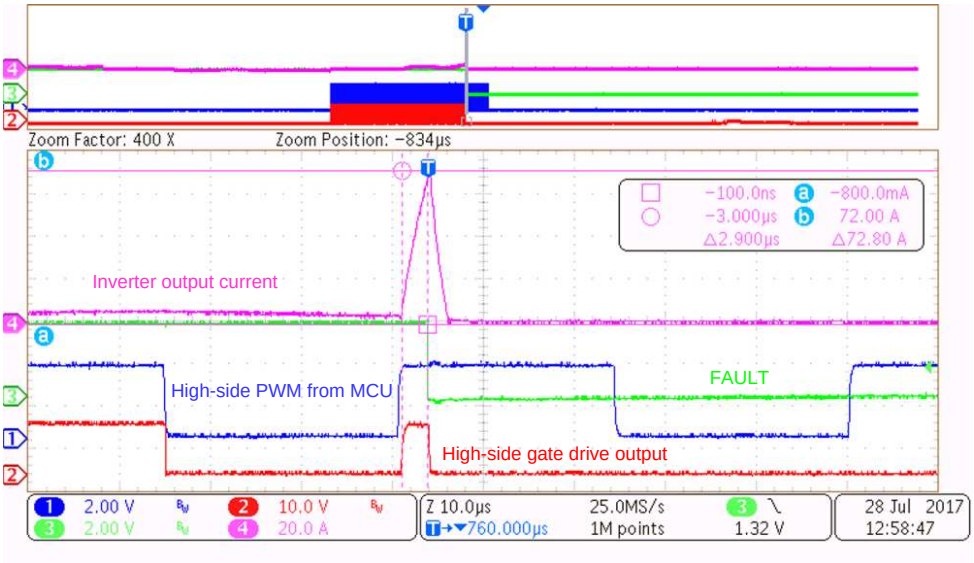

図 47. Zoomed View of Overcurrent Latch Protection With Motor Stall by V_{DS} Monitoring

図 48 shows the test results of latch protection when the inverter output is shorted. The same test setup in 図 42 is used for the short-circuit simulation. The latch protection acted at 65 A with V_{DS} reference of 0.06 V.

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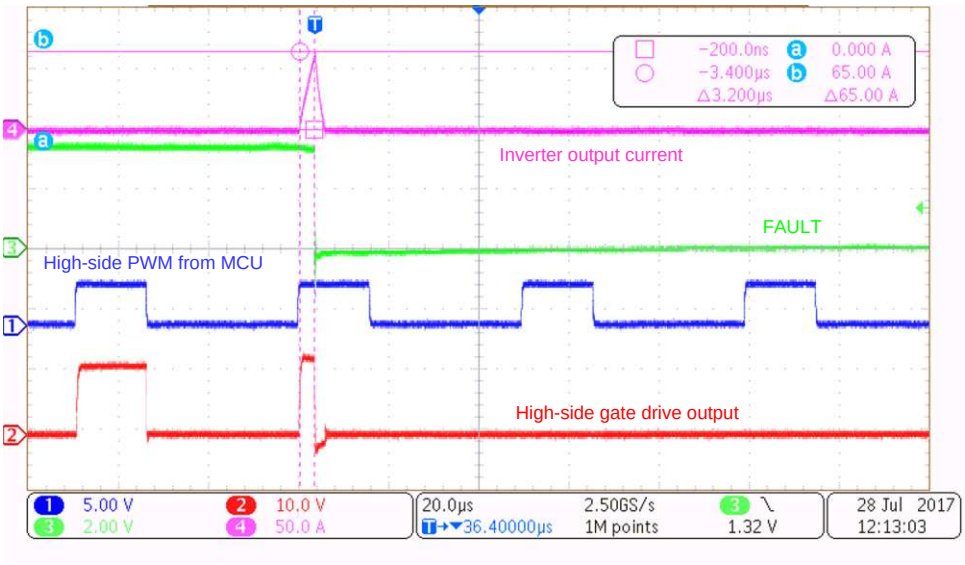

図 48. Overcurrent Latch Protection With Inverter Output Shorted

3.2.7 Testing for Peak Current Capability

図 49 shows the winding current of 60 A when the motor is stalled for 2 seconds. 図 50 shows the thermal image of the board after 2 seconds.

図 51 shows the winding current of 100 A when the motor is stalled for 400 ms. 図 52 shows the thermal image of the board after 400 ms.

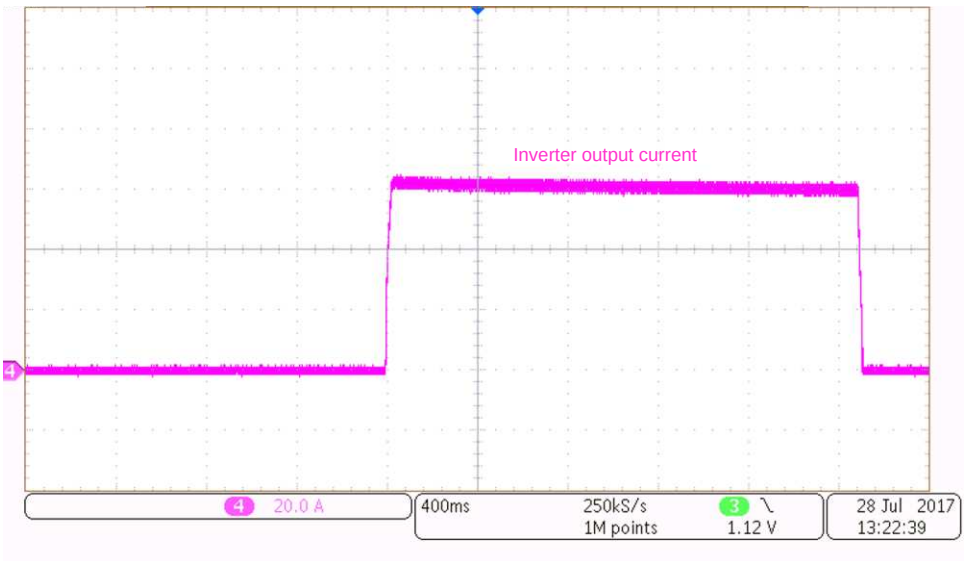

図 49. Peak Current of 60-A Peak Current in Motor Winding During Motor Stall

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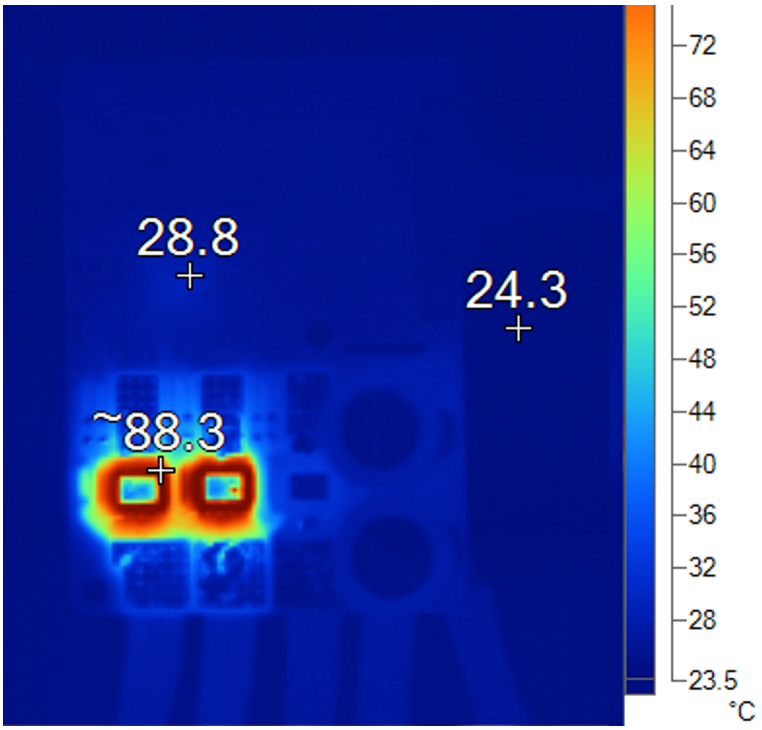

図 50. Thermal Image of Board After 2 Seconds With 60-A Peak Current in Motor Winding

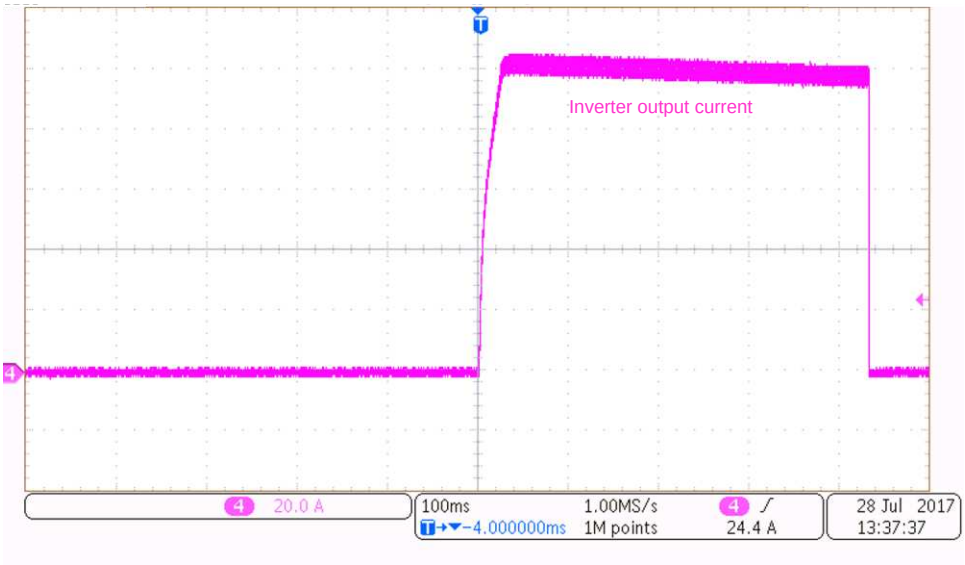

図 51. Peak Current of 100-A Peak Current in Motor Winding During Motor Stall

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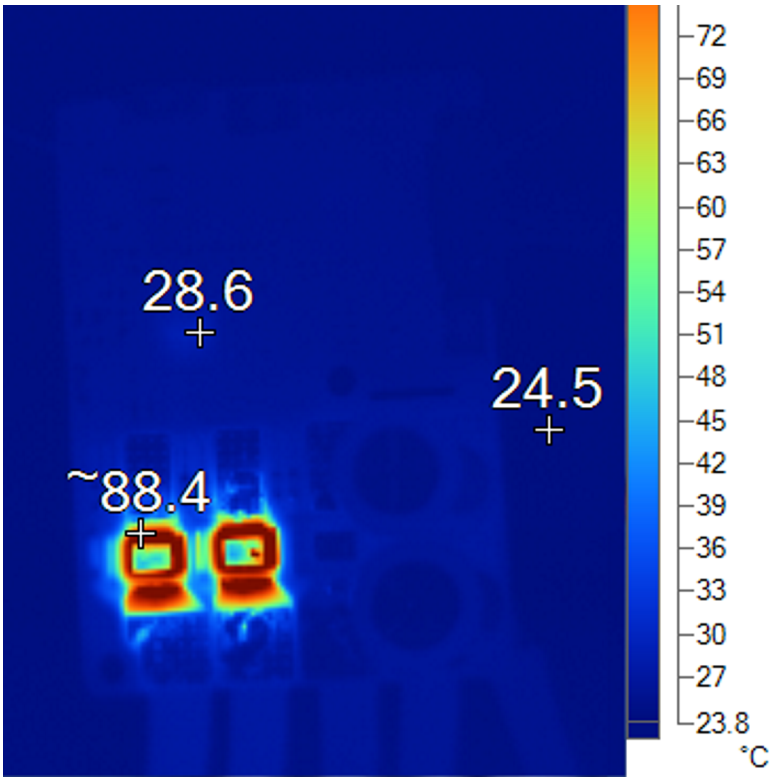

図 52. Thermal Image of Board After 400 ms With 100-A Peak Current in Motor Winding

The board is also tested at single-pulse peak currents of 200 A for 100 ms and 400 A for 10 ms. The testing is done multiple times and MOSFET power blocks operated without failure, showing the reliability of the solution. 図 53 and 図 54 shows the MOSFET current, V_{DS} voltage, and V_{GS} voltage with this testing. The MOSFET is also tested with multiple-pulse peak currents of 200 A with a 100-ms on-time and a 1% duty cycle. The testing is also done at 400 A with a 10-ms on-time and a 1% duty cycle. The results are shown in 図 55 and 図 56.

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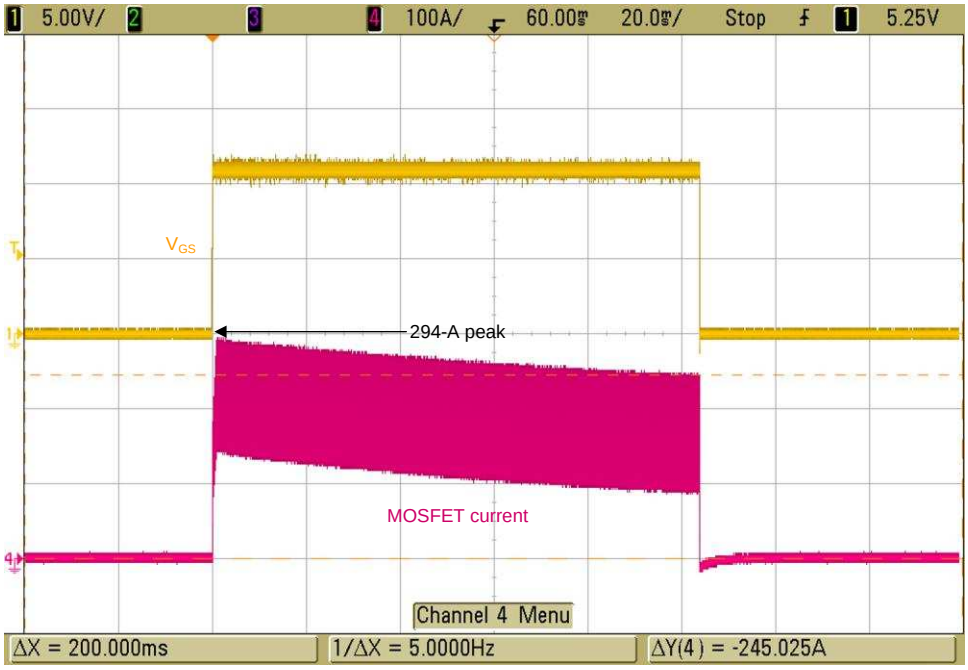

図 53. Single-Pulse Peak Current Testing With 200 A for 100 ms

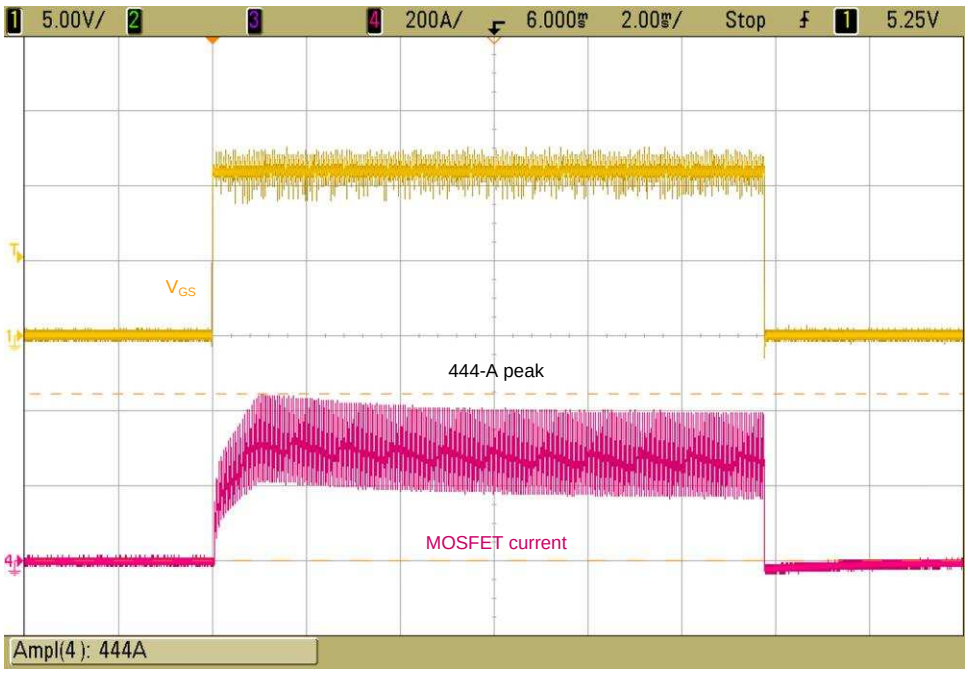

図 54. Single-Pulse Peak Current Testing With 400 A for 10 ms

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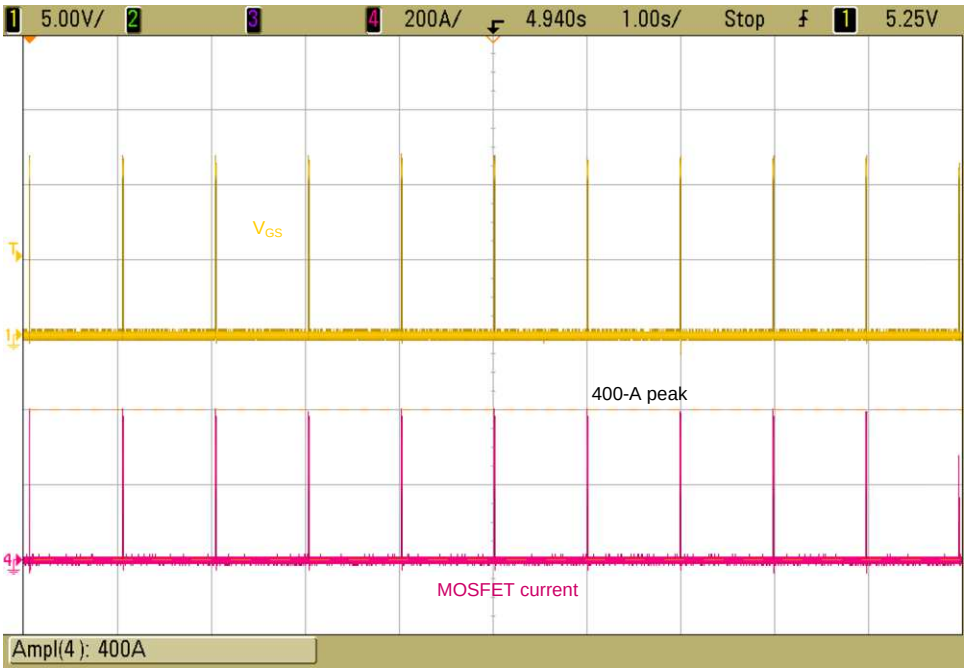

図 55. Multiple-Pulse Peak Current Testing With 400 A for 10 ms With 1% Duty Cycle (990 ms off)

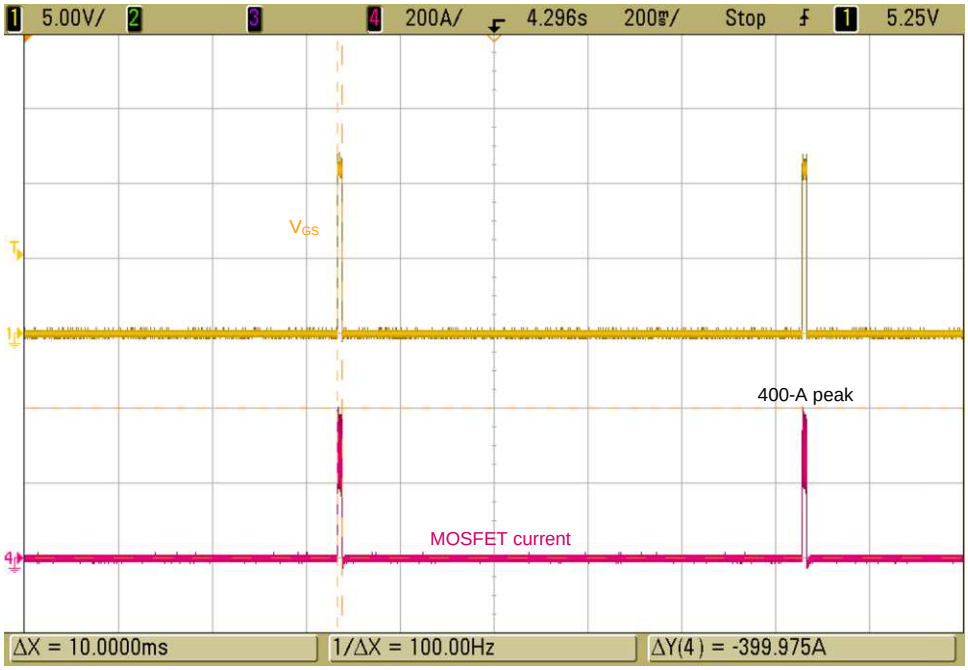

図 56. Multiple-Pulse Peak Current Testing With 400 A for 10 ms With 1% Duty Cycle (Zoomed)

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3.2.8 Effectiveness of Power Block Top-Side Cooling

The MOSFET power block CSD88599Q5DC comes with a thermally enhanced DualCool package. With an exposed metal top, this power block device allows for a simple heat sink application to draw out heat through the top of the package and away from the PCB for superior thermal performance at higher currents. From the CSD88599Q5DC datasheet:

- Junction-to-case thermal resistance (top of package) ($R_{\theta JC\_TOP}$) = 2.1°C/W
- Junction-to-case thermal resistance (bottom of package) ($R_{\theta JC\_BOT}$) = 1.1°C/W

To understand the effectiveness of the top-side heat sink, the board is tested at the conditions specified in 表 16.

表 16. Load Test With Heat Sink to Evaluate Top-Side Cooling

VDC (V)	IDC (A)	WINDING CURRENT (RMS) (A)	DUTY CYCLE	INPUT POWER (W)
36	23.6	22.5	95%	850

This reference design uses a single heat sink for all the three power blocks. The design also uses an electrically insulated thermal interface between the heat sink and the power block top case, having a very low thermal impedance (R_{θ} < 0.5°C/W).

Total thermal impedance to top-side heat sink from the FET junction = ($R_{\theta JC\_TOP}$/3) + R_{θ} (thermal interface).

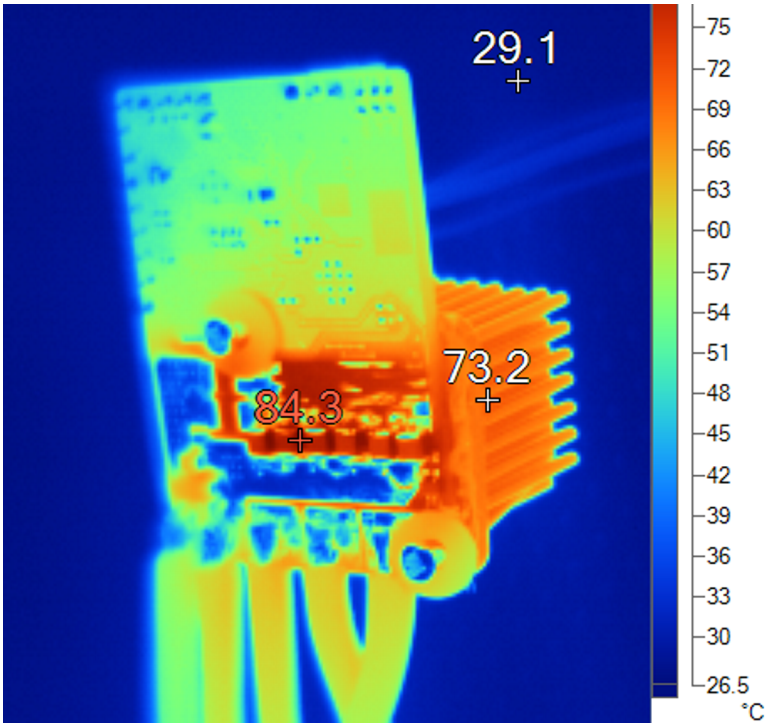

図 57. Thermal Image of Board at 850 W, Showing Effective Top-Side Cooling

From 図 57, the difference between the heat sink temperature and maximum temperature observed on the board is 11°C.

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01485.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01485.

4.3 PCB Layout Recommendations

Use the following layout recommendations when designing the PCB:

- Connect the DRV8323 DVDD 1-µF bypass capacitors directly to the adjacent GND pin to minimize loop impedance for the bypass capacitor.
- Place the PVDD capacitor and charge pump capacitor directly next to the DRV8323.
- Minimize the loop length for the high-side and low-side gate drivers. The high-side loop is from the DRV8323 GH_X to the power MOSFET and returns through SH_X. The low-side loop is from the DRV8323 GL_X to the power MOSFET and returns through GND.
- In this reference design, the PCB is a four-layer layout with a 2-oz (70-micron) copper thickness in every layer. The power tracks are made wide to carry a high current. The tracks are repeated in different layers and are connected by arrays of stitching vias.
- A GND star point is defined in the PCB from where the GND path for the DRV8323 and other signal circuits in the board is tapped.
- For better thermal dissipation from the MOSFET to the PCB, increase the copper area around the MOSFET pad as much as possible. Use arrays of vias under the drain pad of the MOSFET, which will spread heat better to the bottom surface copper area.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01485.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01485.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01485.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01485.

5 Software Files

To download the software files, see the design files at TIDA-01485.

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6 Related Documentation

1. Texas Instruments, *Understanding IDRIVE and TDRIVE in TI Motor Gate Drivers*, Application Report (SLVA714)
2. Texas Instruments, *Sensored 3-Phase BLDC Motor Control Using MSP430*, Application Report (SLAA503)
3. Texas Instruments, *18-V/1-kW, 160-A_{PEAK}, >98% Efficient, High Power Density Brushless Motor Drive Reference Design*, TIDA-00774 Design Guide (TIDUCL0)

6.1 商標

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7 Terminology

SPI— Serial peripheral interface

PWM— Pulse width modulation

BLDC— Brushless DC

MCU— Microcontroller unit

FETs, MOSFETs—Metal-oxide-semiconductor field-effect transistor

ESD— Electrostatic discharge

RPM— Rotation per minute

RMS— Root mean square

8 About the Author

MANU BALAKRISHNAN is a systems engineer at Texas Instruments, where he is responsible for developing subsystem design solutions for the Industrial Motor Drive segment. Manu brings to this role his experience in power electronics and analog and mixed signal designs. He has experience in system-level product design of permanent magnet motor drives. Manu earned his bachelor of technology in electrical and electronics engineering from the University of Kerala and his master of technology in power electronics from National Institute of Technology Calicut, India.

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