参考資料

TI Designs: TIDA-01232
大電流、低ノイズのパラレルLDOのリファレンス・デザイン

概要

このパラレルLDOのリファレンス・デザインでは、TPS7A85低ノイズ、低ドロップアウト・リニア・レギュレータ(LDO)のパラレル構成を紹介します。この構成では、LDOごとに3.5A、または基板ごとに7Aを供給できます。アプリケーションの電流要件を満たすため、このデザインをスタックできるので、さらに柔軟な設計を行えます。

リソース

TIDA-01232	デザイン・フォルダ
TPS7A85	プロダクト・フォルダ

TI E2E™ Community

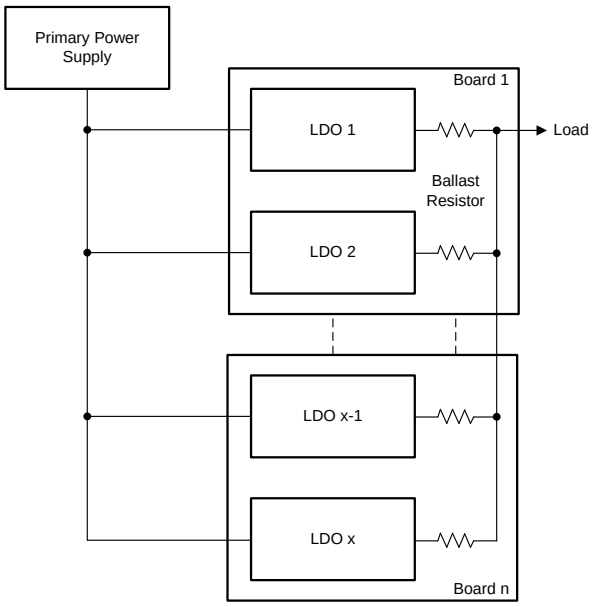
E2Eエキスパートに質問

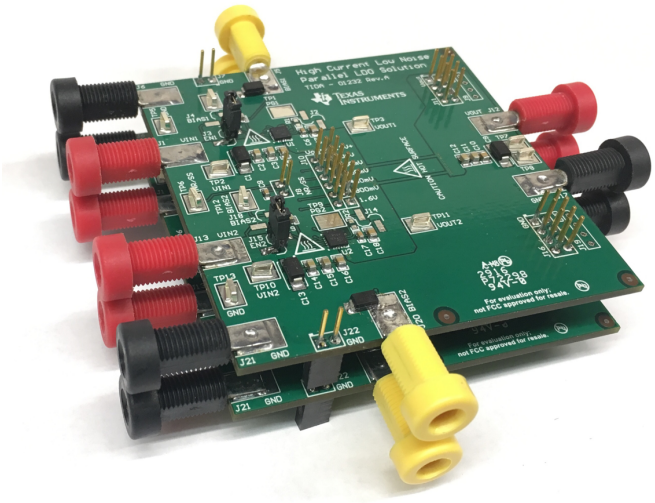
特長

- 出力電流: 基板ごとに最大7A (基板ごとに2つのTPS7A85 LDO)
- 低いドロップアウト電圧: 200mV (標準値)
- 低いノイズ出力: 8つのLDOをパラレル接続時に3.33μV_{RMS} (1つのLDOについて、10Hz～100kHz)
- 高い出力精度: 1% (ライン、負荷、温度の全範囲にわたって)

アプリケーション

- FPGAおよびDSPの電源供給
- DC-DC後の電力フィルタリング
- サーバー





1 System Description

Low-noise low-dropout regulators (LDO) are required in many applications to ensure that power supply noise does not couple into the signal chain. The requirements for current continue to increase as new high-speed analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and clocking circuitry increase data speed and bandwidth. Using a single LDO for the supply is not always possible due to device availability and power dissipation limitations. The TIDA-01232 reference design solves this issue by using multiple LDOs configured to share current in parallel. The current sharing is achieved by using a single low-value ballast resistor, which can be designed as a copper trace on the resistor of a printed-circuit board (PCB).

This circuit uses the high-current LDO, TPS7A85, which is a 4-A device. Every board is populated with two TPS7A85 devices and can provide up to 7 A of current. The boards are designed so that multiple boards can be stacked on top of each other. For example, if a second board is stacked on top of the first board, the solution can provide up to 14 A.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input power rail, V_{IN}	V_{OUT} + 200 mV (typical)
Bias power rail(1), V_{BIAS}	3.0 V to 6.5 V
Maximum output current, I_{OUT}	3.5 A multiplied by the number of LDOs (7 A per board)
Output voltage range, V_{OUT}	0.8 V to 3.95 V (using ANY-OUT™)
Optimized for output Voltage, V_{OUT}	0.8 V
Ballast resistor, $R_{BALLAST}$	5 mΩ
Maximum voltage drop across ballast resistor(2), $V_{BALLAST}$	20 mV

(1) Required for V_{IN} < 1.4 V, recommended for V_{IN} < 2.2 V for best dropout.
(2) The delta between $V_{NOMINAL}$ to V_{OUT} is greater due to the resistance from the connectors in between the boards.

2 System Overview

2.1 Block Diagram

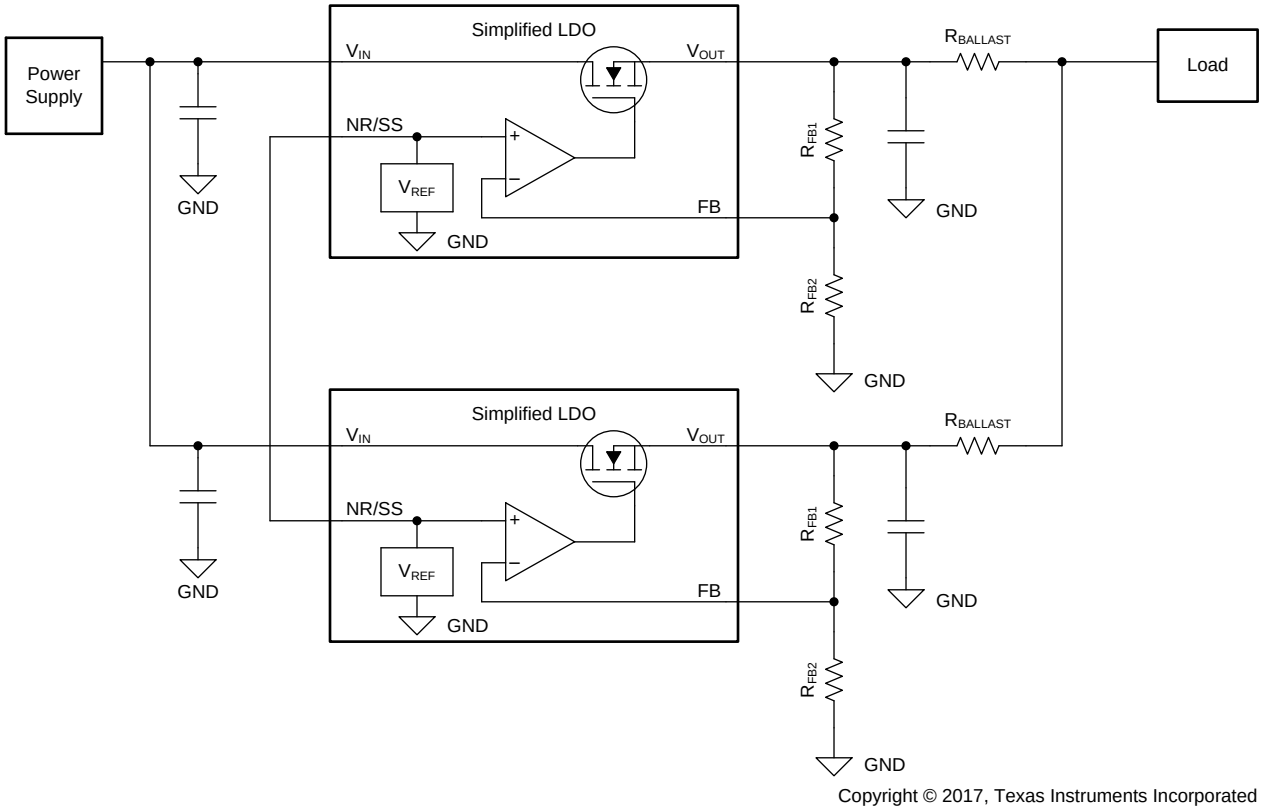


図 1. Two LDOs With Ballast Resistors

2.2 Design Considerations

2.2.1 Theory of Operation

2.2.1.1 Ballast Resistor

This solution uses ballast resistors. Ballast resistors provide an easy way to connect multiple voltage sources together to supply power to a common load. Critical for this method is to minimize the voltage difference at the output of each individual LDO. As LDO accuracy improves, the designer can reduce the size of the ballast resistor.

Every LDO has its own voltage reference and each independent reference is slightly different from every other independent reference; therefore, to achieve the smallest possible error, this solution connects these voltages together through the NR/SS pin. The remaining error sources are the feedback resistor network, the ballast resistor, the internal output field-effect transistor (FET), and the amplifier. 2.2.2 and 3.1.1 provide further detail on how this solution minimizes sources of error.

The following formulas in 式 1 and 式 2 are used to size the ballast resistor:

$$E_{Vout} = E_{Vref} + 2 \times \left(1 - \frac{V_{ref}}{V_{outNom}}\right) \times E_{Rfb} \quad (1)$$

where,

- E_{Vout} is the maximum expected error of the LDO output,
- E_{Vref} is the maximum expected error of the LDO internal reference,
- V_{ref} [(1)] is the reference voltage of the LDO,
- E_{Rfb} is the maximum expected error of the feedback resistors.

$$R_{Ballast} = \frac{V_{outNom} \times (2 \times E_{Vout})}{2 \times I_{outMax\,Single} - I_{outMaxTotal}} \quad (2)$$

where,

- $R_{Ballast}$ is the ballast resistor,
- V_{outNom} is the nominal LDO output,
- E_{Vout} is the maximum expected error of the LDO output,
- $I_{outMaxSingle}$ is the current limit of a single LDO,
- $I_{outMaxTotal}$ is the maximum current of the system.

Minimize the error and the ballast resistor by using the same LDO (TPS7A85) for each of the LDOs paralleled. To further reduce the error, chose an LDO that has the NR/SS voltage (reference voltage) routed to a pin.

Use the following formula in 式 3 to determine if the output of this solution delivers a high enough voltage:

$$V_{outTotMin} = V_{outNom} \times (1 - E_{Vout}) - \frac{I_{outMaxTotal}}{n} \times R_{Ballast} \times (1 + E_{Rballast}) \quad (3)$$

where,

- $V_{outTotMin}$ is the minimum output of the solution (voltage at load) [(2)],
- V_{outNom} is the nominal LDO output,

(1) V_{ref} is equal to V_{FB}

(2) This formula applies to an ideal solution meaning that there are no other resistance elements on the current path, such as a via.

- E_{Vout} is the maximum expected error of the LDO output,
- $I_{outMaxTotal}$ is the maximum current of the system,
- $R_{Ballast}$ is the ballast resistor,
- $E_{Rballast}$ is the maximum expected error due to the ballast resistor tolerance,
- n is the number of parallel LDOs.

Designers may be tempted to move the point where the feedback is connected to the output after the ballast resistor and let the LDO regulate this voltage. The issue here is that the effect of the ballast the resistor would be eliminated and the LDOs would no longer share the load current.

When the resistor is defined for two LDOs, the same resistor must be used to add additional LDOs. As long as the LDOs are the same, the biggest output difference does not change; therefore, the ballast resistor remains the same.

2.2.2 Component Selection

2.2.2.1 LDO Selection

The criteria for the LDO is as follows:

- High accuracy output
- ANY-OUT™ feedback resistors
- High current
- NR/SS pin

ANY-OUT™ feedback resistors provide an advantage in accuracy over traditional adjustable LDOs with external resistor networks. Traditionally, external resistor dividers are not included in the accuracy specification of an LDO. ANY-OUT™ feedback resistors are internal to the LDO and are matched so that the ratio of the resistor divider is accurate. This matching allows the ANY-OUT™ feedback resistors to be included in the overall accuracy specification of the LDO, which makes a 1% LDO with ANY-OUT™ more accurate than a traditional 1% adjustable LDO with external feedback resistors.

The NR/SS pin allows for minimizing the error of the voltage reference, which narrows down the range of the outputs between the LDOs. 3.1.1 provides additional information.

The 4-A, high-precision LDO TPS7A85 meets the criteria, which is the reason it has been chosen for this design.

2.2.3 Connector Selection

The PCB was designed to be stacked upon itself, which is achieved by using 100-mil connectors.

The parts listed in 表 2 are used for this reference design:

表 2. Connector Part Number by Function

FUNCTION	PART NUMBER
Output	SSQ-104-03-G-D
ANY-OUT™	SSQ-106-03-G-D
GND, NR/SS	SSQ-102-03-G-S

2.2.4 Capacitor Selection

This reference design uses local capacitors for the input (C1 through C4, C13 through C16) (1), local output capacitors (C7, C18), feed forward capacitors (C6, C17), as well as global output capacitors (C9 through C12) (2). TI advises to follow the recommendations of the data sheet for capacitor selection. Designers can typically find this information in the “Application and Implementation” sections of data sheets.

(1) Capacitor designators refer to the *Schematics*.
(2) Capacitors C1, C9, and C13 were not populated.

2.3 Highlighted Products

2.3.1 TPS7A85

The TPS7A85 is a low-noise (4.4 μV_{RMS}), low-dropout linear regulator (LDO) capable of sourcing 4 A with only 240 mV of maximum dropout. The device output voltage is pin-programmable from 0.8 V to 3.95 V and adjustable from 0.8 V to 5.0 V using an external resistor divider.

The combination of low-noise (4.4 μV_{RMS}), high power supply rejection ratio (PSRR), and high output current capability makes the TPS7A85 ideal to power noise-sensitive components such as those used in high-speed communications, video, medical, or test and measurement applications. The high performance of the TPS7A85 limits power-supply-generated phase noise and clock jitter, which make this device ideal for powering high-performance serializer and deserializer (SerDes), ADCs, DACs, and RF components. RF amplifiers specifically benefit from the high performance and 5.0-V output capability of the device.

The exceptional accuracy (1% over line, load, and temperature), remote sensing, excellent transient performance, and soft-start capabilities of the TPS7A85 ensure optimal system performance for digital loads that require low-input voltage, low-output (LILO) voltage operation, such as application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs), and digital signal processors (DSPs) .

The versatility of the TPS7A85 makes it a popular choice for many demanding applications.

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

3.1.1 Ballast Resistor Implementation

This subsection serves as a guideline for designing a PCB ballast resistor. 2.2.1.1 describes the formulas used.

Because no target V_{outMin} has been established for this design, the iterative part to reach a target voltage can be skipped.

For this calculation V_{outNom} = 0.8 V, which results in the following E_{Vout} in 式 4:

$$E_{Vout} = E_{Vref} + 2 \times (1 - \frac{V_{ref}}{V_{outNom}}) \times E_{Rfb} = (V_{outNom} \times 1\%) + 2 \times (1 - \frac{0.8\ V}{0.8\ V}) \times E_{Rfb} = (V_{outNom} \times 1\%) + 2 \times (1 - 1) \times E_{Rfb} = V_{outNom} \times 1\% = 0.8\ V \times 0.01 = 8\ mV \quad (4)$$

The error of 8 mV is specified for a single LDO over the full temperature range including the tolerance of the voltage reference as well as the tolerance of the internal feedback resistors, amplifier, and FET. For this reference design, the NR/SS pins are shorted together; therefore, the voltage references of each individual LDO are also shorted to each other. As such, the accuracy of the output remains 1% but the voltage difference between the individual LDOs will be closer to each other.

Measurements prove that the V_{OUT} of the LDOs with the same V_{REF} are closer to each other than the calculated 8 mV. 図 2 shows such a measurement. For example, if the $V_{NR/SS}$ is in the *blue* range, V_{OUT} is most likely to fall within the *blue* marked range of the upper histogram. The same principle applies to the range marked in *red*. By connecting these two reference voltages together, the V_{REF} at the error amplifier input will be somewhere in between these two voltages. The movement of V_{REF} also influences the output and moves the range in between the two marked ranges.

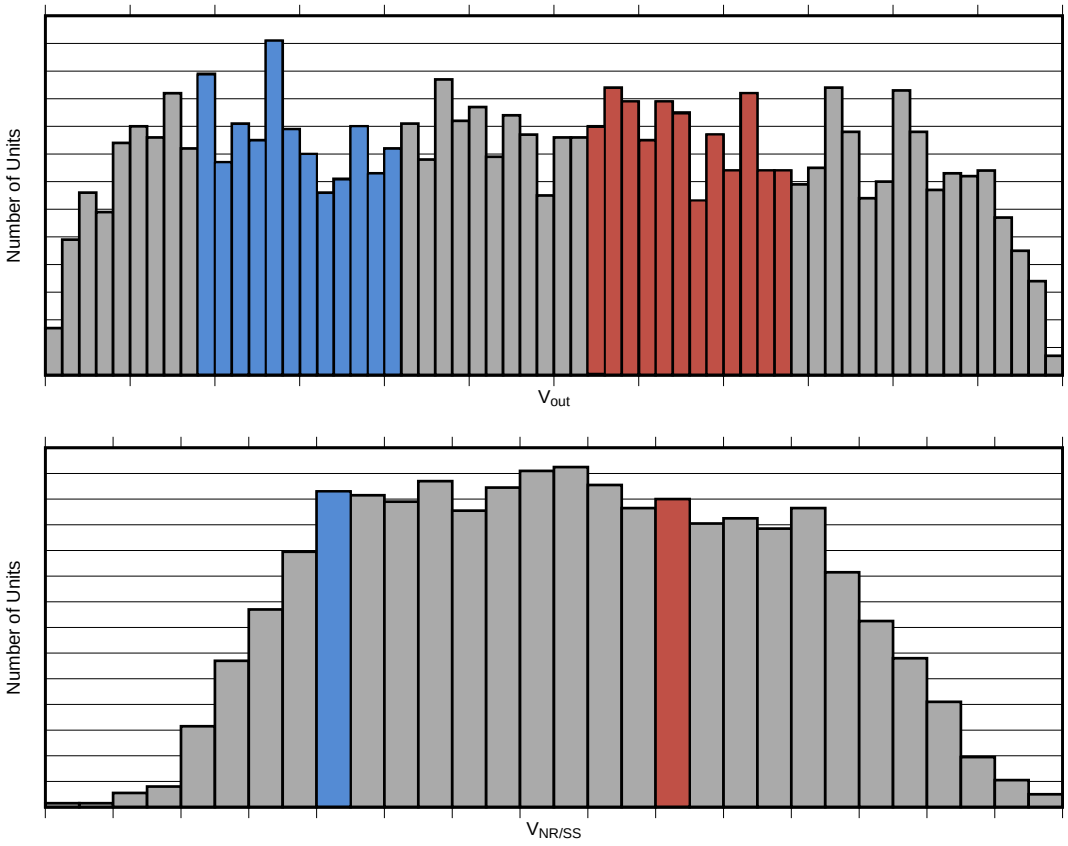


図 2. Histogram of $V_{NR/SS}$ Compared to V_{OUT}

After testing various NR/SS voltages at V_{outNom} = 0.8 V, the typical range of V_{OUT} for each $V_{NR/SS}$ pin did not surpass 1.5 mV, which would otherwise result in an E_{Vout} of ±0.75 mV.

Using this output range means that the following ballast resistor would be required:

$$R_{Ballast} = \frac{V_{outNom} \times (2 \times E_{Vout})}{2 \times I_{outMaxSingle} - I_{outMaxTotal}} = \frac{0.8\ V \times 2 \times 0.75\ mV}{2 \times 4A - 7.5\ A} = 2.4\ m\Omega \quad (5)$$

For some additional margin and to be able to change the V_{outNom} up to 1.6 V, this value is set to 5 mΩ. Choosing $I_{outMaxTotal}$ = 7.5 A is an iterative procedure for evaluating the size and length of the PCB resistor.

After defining the value for the ballast resistor, the next step is to design the PCB trace dimensions to match this resistive value. 式 6 shows how to calculate the resistance of a PCB trace:

$$R = \frac{l \times \rho}{A \times (1 + \alpha \times (T_A - T_0))} \quad (6)$$

where,

- R is the trace resistor of the PCB in Ω,
- l is the length of the trace in meters,
- ρ is the resistivity in Ω meters $\rho_{copper} = 16.8 \times 10^{-9}$ Ωm,
- A is the vertical area of trace in square meters,
- α is the temperature coefficient in $°C^{-1}$ $\alpha_{copper} = 3.9 \times 10^{-3} °C^{-1}$,
- T is the ambient temperature T_0 = 25°C.

図 3 shows the PCB trace dimensions.

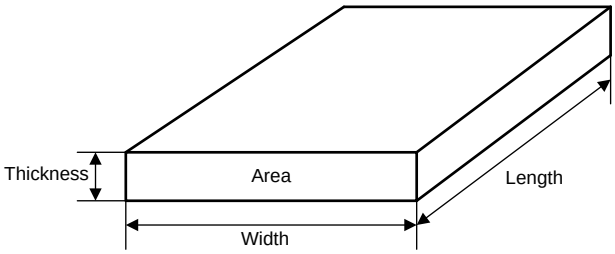


図 3. PCB Trace Dimensions

Use the diagrams of the trace resistance as a function of the trace width to find a reasonable length verse width ratio. The temperature is considered as well and added to the individual plots to avoid burning the trace (see 図 4).

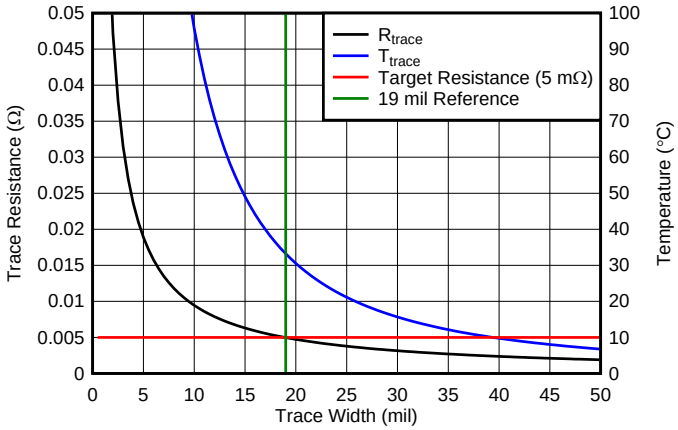


図 4. 400-mil Length PCB Trace Width versus Trace Resistance (Ω)

式 7 shows the formula for the temperature per IPC-2221:

$$\Delta T = \left(\frac{I}{k \times A^{c}} \right)^{\frac{1}{b}} \tag{7}$$

where,

- ΔT is the temperature difference,
- I is the current through the trace,
- A is the vertical area of trace in square mil,
- b is 0.44,
- c is 0.725,
- k is 0.024 for an internal PCB layer and 0.048 for an external PCB layer.

図 4 shows that with a trace width of 19 mil, a length of 400 mil and a thickness of 2 oz should match the desired 5 mΩ. The following calculations of the trace and temperature reinforce the findings of this plot:

$$R = \frac{I \times \rho}{A \times (1 + \alpha \times (T_A - T_0))} = \frac{(400\ \text{mil} \times 2.54 \times 10^{-5}\ (\text{m/mil})) \times (1.68 \times 10^{-8})\ \Omega\text{m}}{((2.8 \times 19)\ \text{mil}^2 \times 6.45 \times 10^{-10}\ (\text{m}^2/\text{mil}^2)) \times (1 + \frac{3.9 \times 10^{-3}}{°\text{C}} \times (25 - 25)\ °\text{C})} \tag{8}$$

$$\Delta T_{4A} = \left(\frac{I}{k \times A^{C}} \right)^{\frac{1}{b}} = \left(\frac{4\ \text{A}}{0.048 \times (2.8\ \text{mil} \times 19\ \text{mil})^{0.725}} \right)^{\frac{1}{0.44}} = 33.2°\text{C} \tag{9}$$

$$\Delta T_{4A} = \left(\frac{I}{k \times A^{C}} \right)^{\frac{1}{b}} = \left(\frac{3.5\,\text{A}}{0.048 \times (2.8\ \text{mil} \times 19\ \text{mil})^{0.725}} \right)^{\frac{1}{0.44}} = 24.5°\text{C} \tag{10}$$

Per the calculations, with a 2-oz (2.8-mil) thick copper trace at ambient temperature (25°C), the trace should have a 19-mil width and 400-mil length to reach the desired 5-mΩ ballast resistor.

3.2 Testing and Results

3.2.1 Test Setup

The scope shots in this section show the typical values. The boards are powered by V_{IN} = 1.1 V, V_{BIAS} = 4.5 V unless otherwise noted. The power supply used for V_{IN} was the Chroma 62006P-100-25. The scope shots were taken with the LeCroy WaveSurfer 454. Each board has two LDOs in parallel. Multiples of two LDOs are added by stacking boards: four LDOs is two boards stacked, six LDOs is three boards stacked, and so forth.

3.2.2 Test Results

3.2.2.1 Start-Up

For the following scope shots *blue* is V_{IN}, *green* is V_{OUT}, *red* is I_{IN}, and *magenta* is V_{EN}.

The following scope shots are for two LDOs (one board).

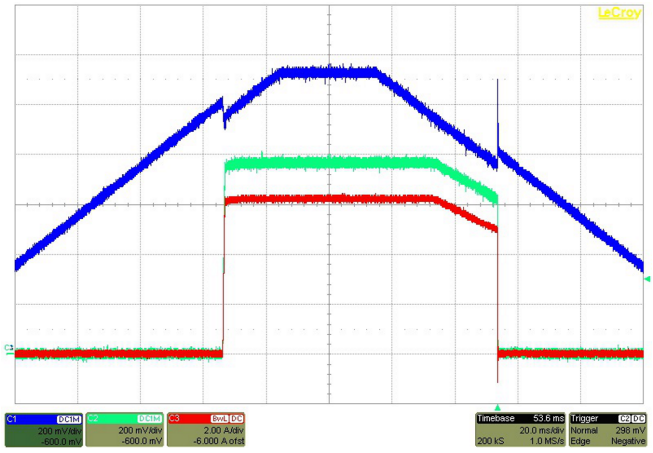


図 5. Start-up—Two LDOs, 6 A

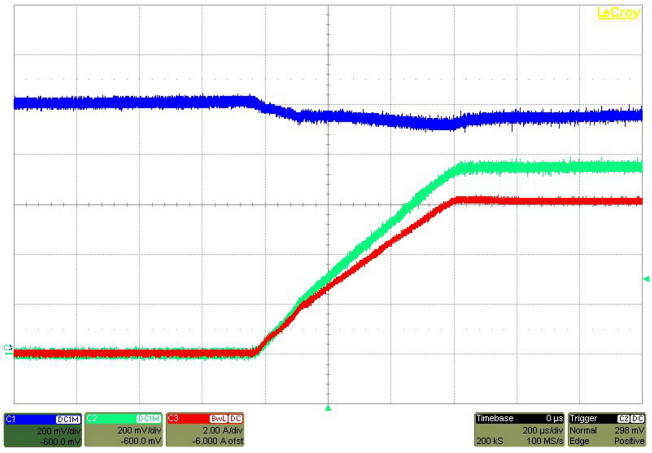


図 6. Start-up—Two LDOs, 6 A (Zoomed in)

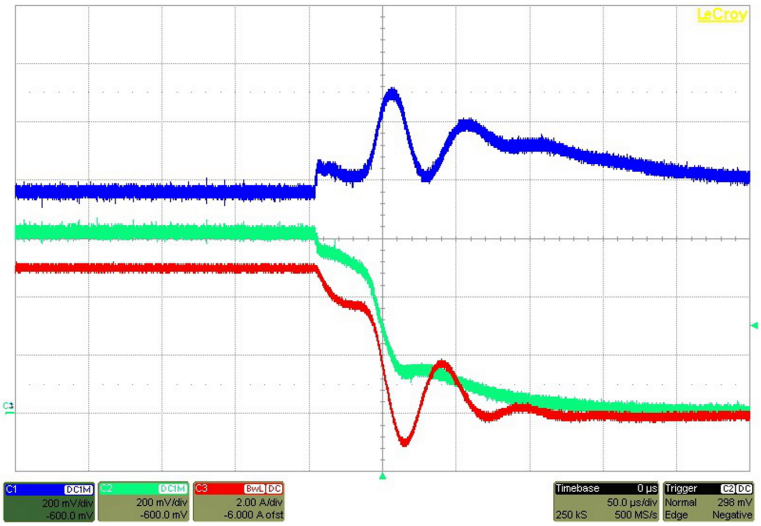


図 7. Shutdown—Two LDOs, 6 A

The following scope shots are for six LDOs (three boards).

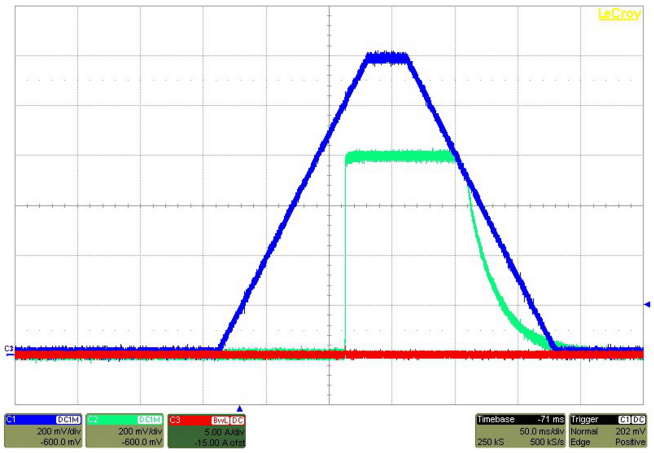


図 8. Start-up—Six LDOs, No Load

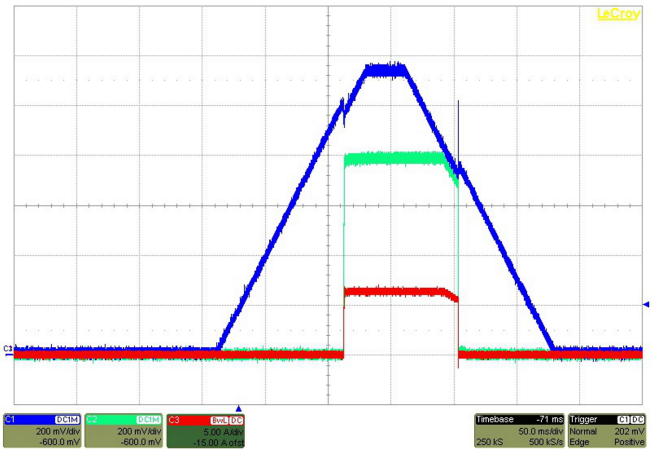


図 9. Start-up—Six LDOs, 6 A

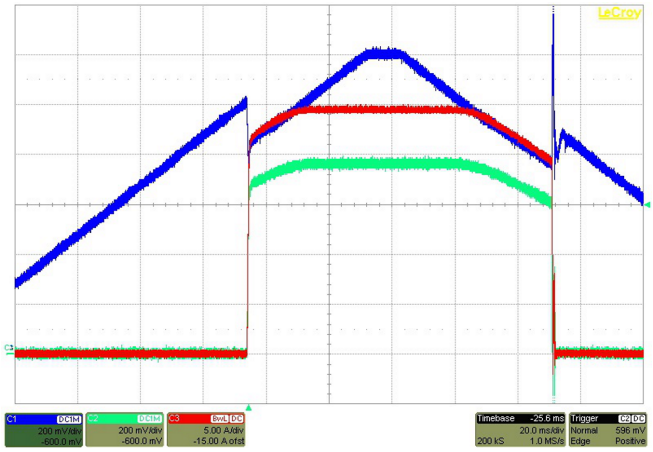


図 10. Start-up—Six LDOs, 24 A

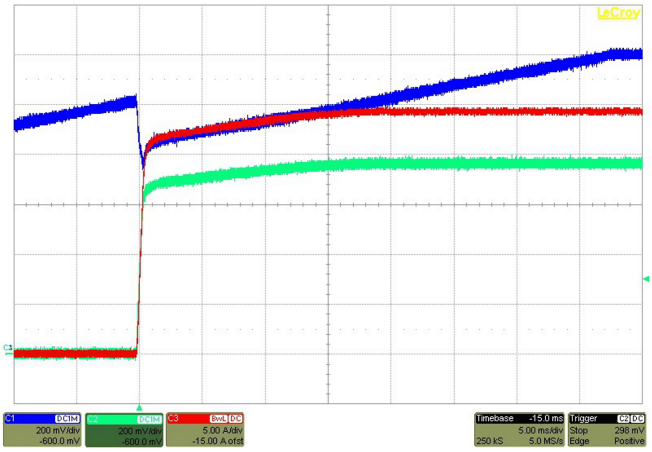


図 11. Start-up—Six LDOs, 24 A (Zoomed in)

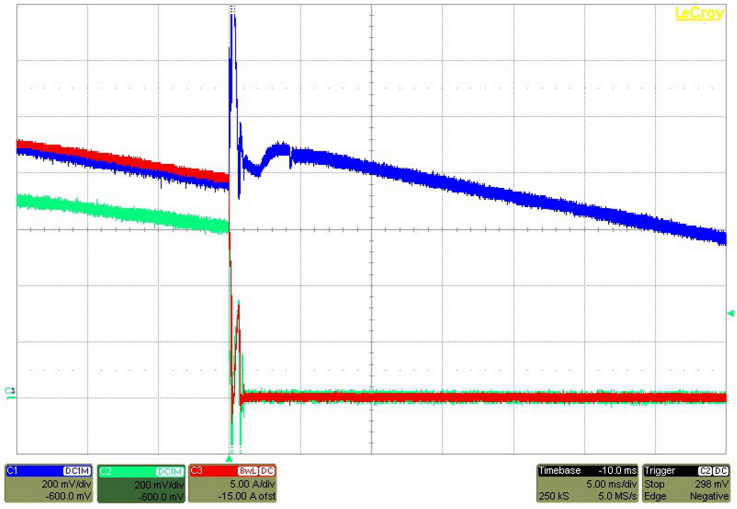


図 12. Shutdown—Six LDOs, 24 A

If the system is started into a full load, TI recommends to first establish V_{BIAS} and V_{IN} and then turn the devices ON using the enable pin. Use a supervisor or a microcontroller to perform this action. The reason for these steps is to relieve the supply and avoid the high load drop V_{IN} under $V_{UVLO} – V_{HYS}$, which causes the LDOs to shut down again. The ringing at the falling edges is caused by the inductance of the load (in this case a 1-m long cable) and the inductance of the cable connecting the boards to the power supply. If V_{IN} spikes higher than V_{UVLO} while shutting down, the LDOs may try to power up again.

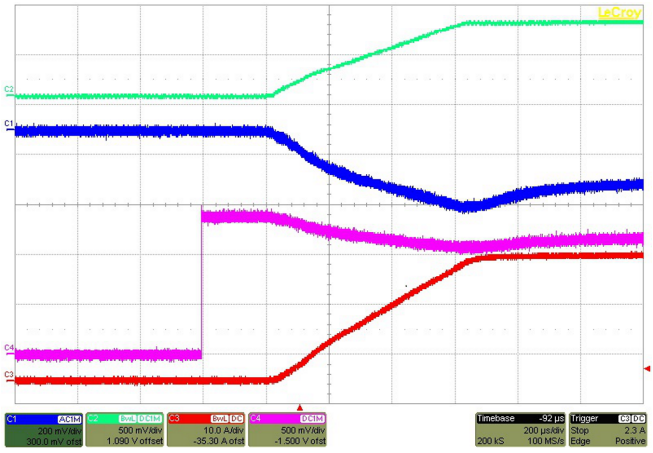


図 13. Enable Start-up—Six LDOs, 24 A

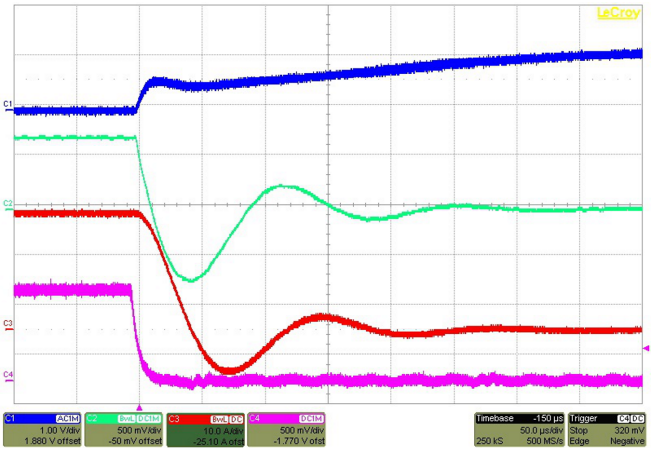


図 14. Enable Shutdown—Six LDOs, 24 A

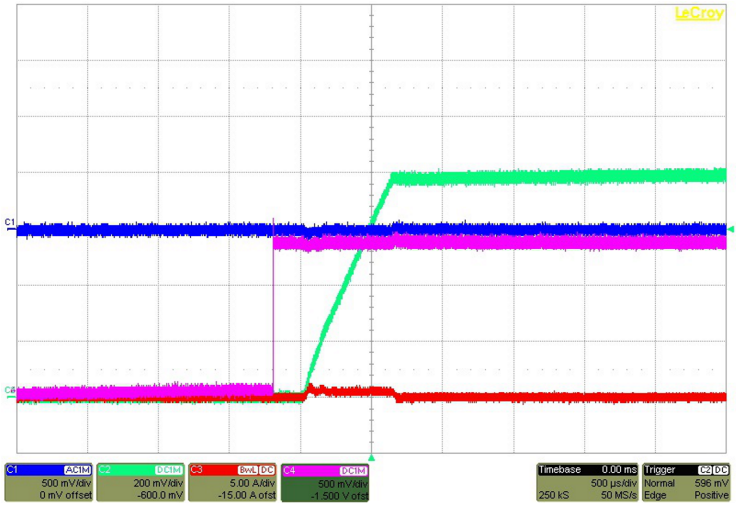


図 15. Enable Start-up—No Load

3.2.2.2 Noise

The following graphs show the noise performance of two, four, and eight parallel LDOs. A resistive load of 0.123 Ω is used for all three examples, which results in a total current load of approximately 6.5 A when the output is set to 0.8 V.

The two main considerations for these graphs are as follows: First, the peaks on the upper end of the frequency are a result of the internal charge pump of the LDO. See the subsection regarding charge pump noise in *TPS7A85 High-Current (4 A), High-Accuracy (1%), Low-Noise (4.4 μV_{RMS}), LDO Voltage Regulator* for further details[3]. Second, the noise keeps decreasing for each LDO added in parallel, which is similar to when amplifiers are set in parallel. By paralleling amplifiers, the noise can be improved by the ratio of sqrt(2) for each time the number of amplifiers is doubled.

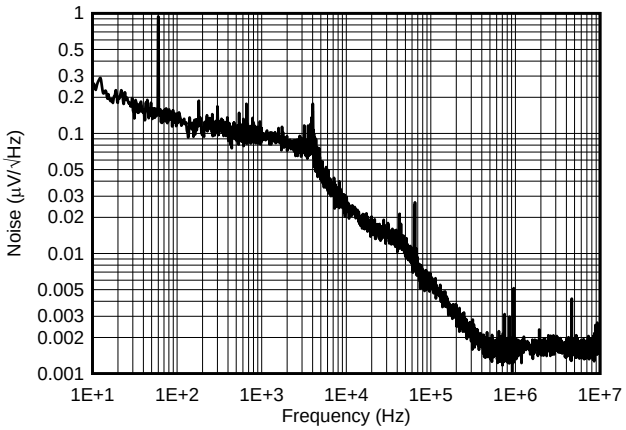


図 16. Output Noise—One LDO (Noise$_{10\ Hz\ –\ 100\ kHz}$ = 7.69 μV_{RMS})

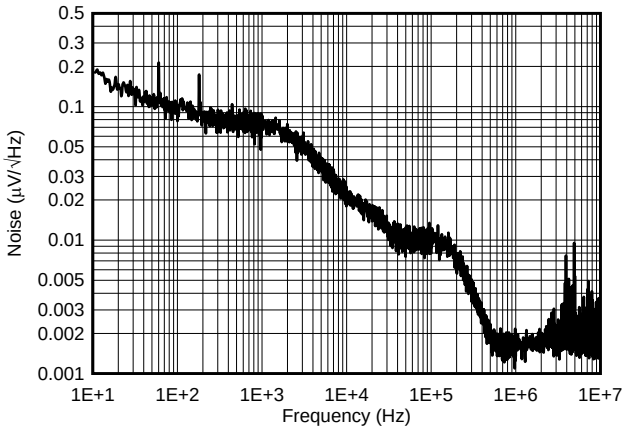


図 17. Output Noise—Two Parallel LDOs (Noise$_{10\ Hz\ –\ 100\ kHz}$ = 5.98 μV_{RMS})

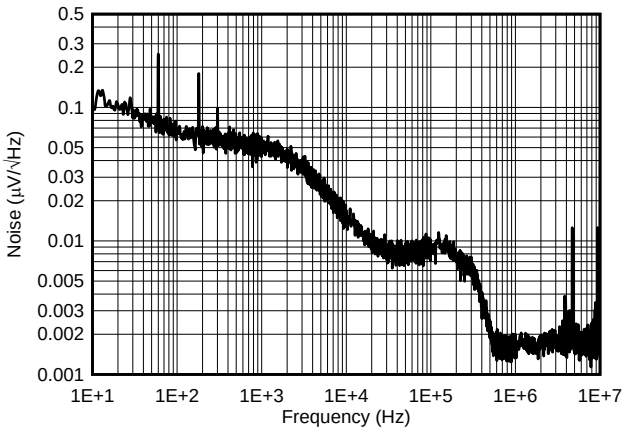


図 18. Output Noise—Four Parallel LDOs (Noise$_{10\ Hz\ –\ 100\ kHz}$ = 4.32 μV_{RMS})

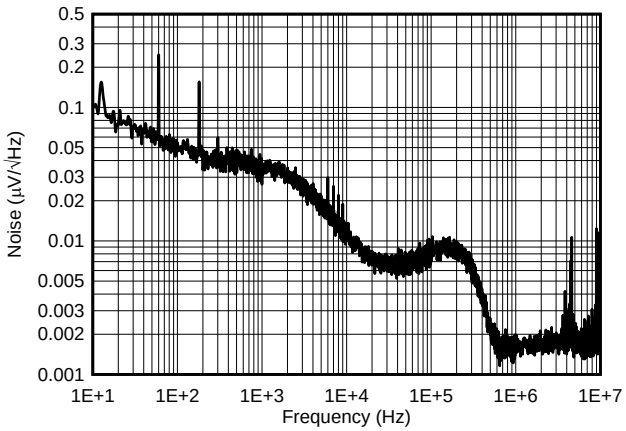


図 19. Output Noise—Eight Parallel LDOs (Noise$_{10\ Hz\ –\ 100\ kHz}$ = 3.33 μV_{RMS})

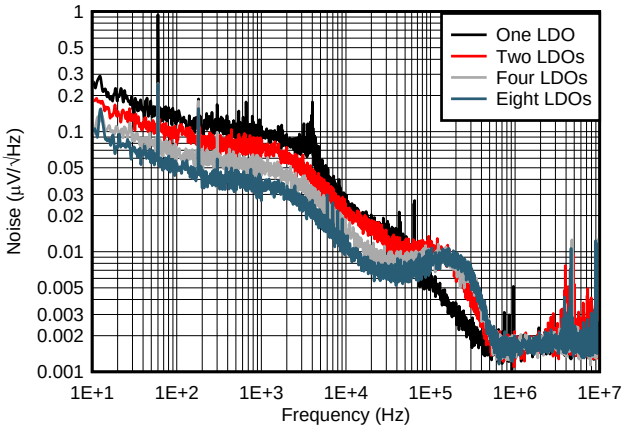


図 20. Output Noise

3.2.2.3 Sharing Performance

For the error plot, the board (or boards) with the worst sharing performance were selected to show the worst case.

The following graphs have two LDOs (one board).

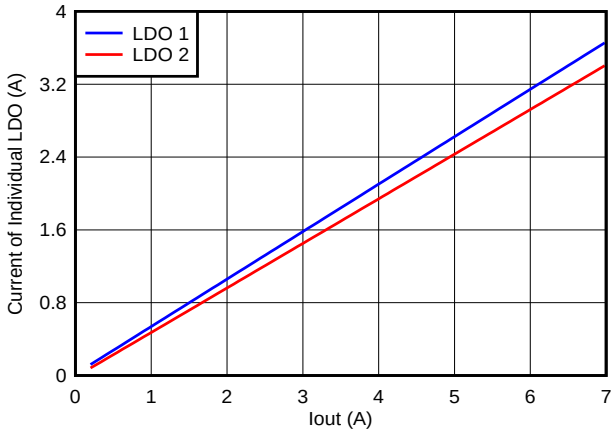


図 21. Sharing Board 1

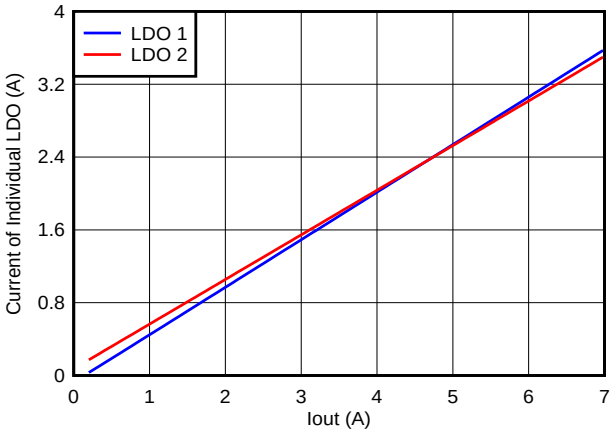


図 22. Sharing Board 2

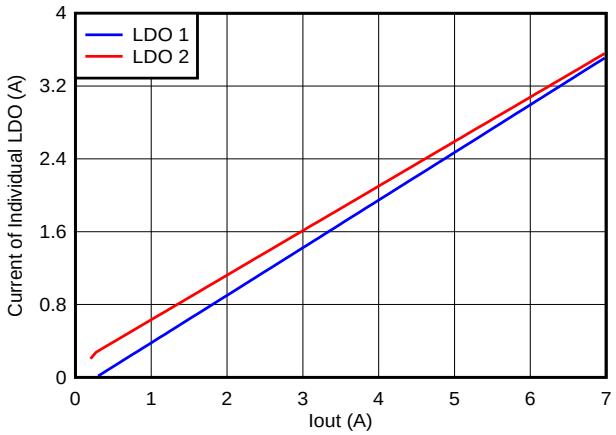


図 23. Sharing Board 3

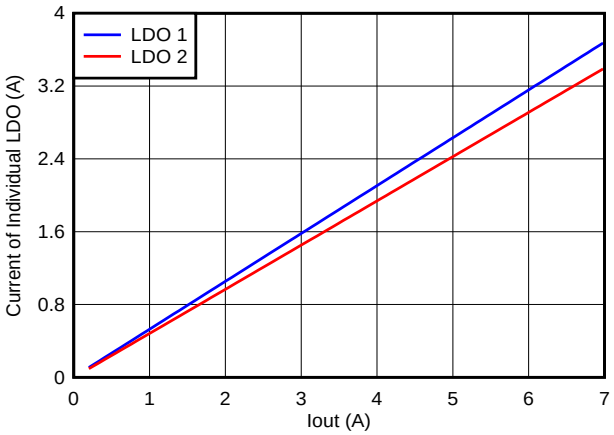


図 24. Sharing Board 4

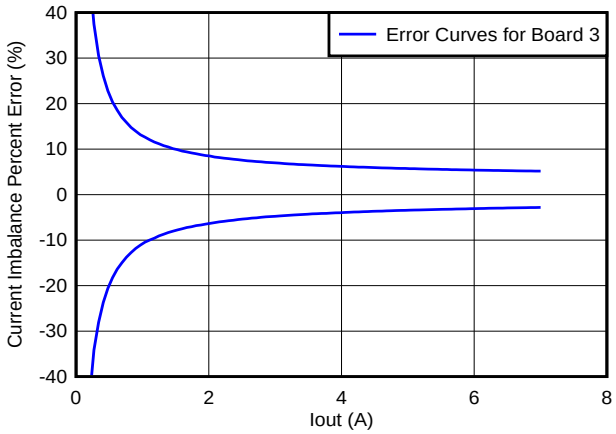


図 25. Sharing Error Board 3

The following error plots have four LDOs (two boards in parallel).

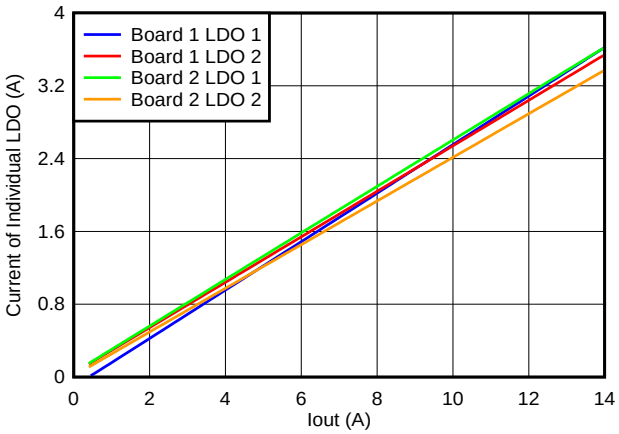


図 **26. Sharing Boards 1 and 2**

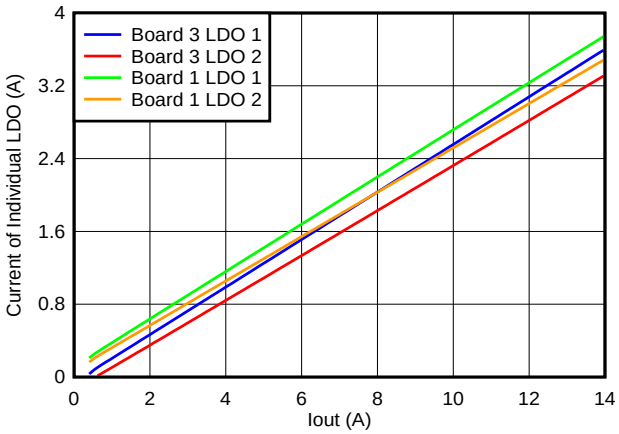


図 **27. Sharing Boards 1 and 3**

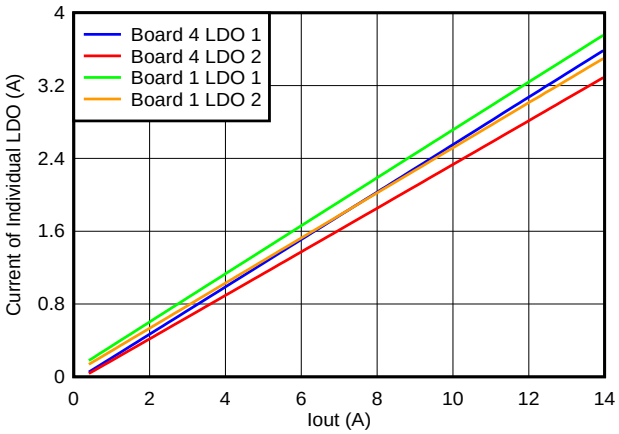


図 **28. Sharing Boards 1 and 4**

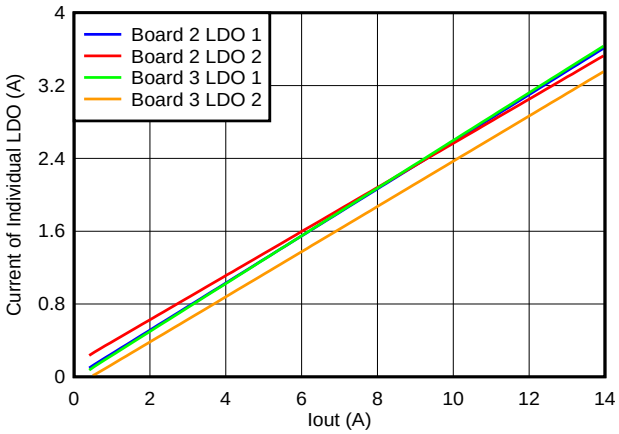


図 **29. Sharing Boards 2 and 3**

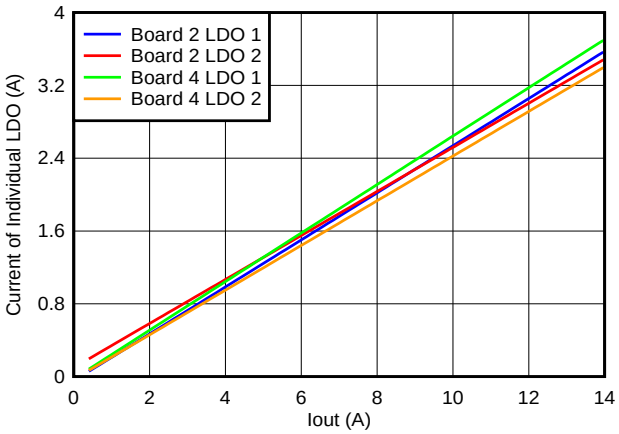


図 **30. Sharing Boards 2 and 4**

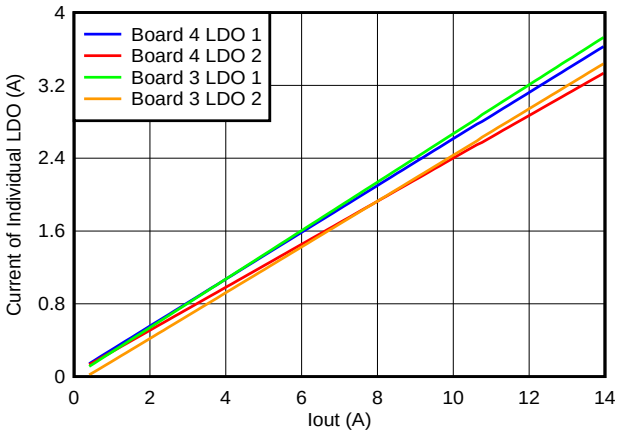


図 **31. Sharing Boards 3 and 4**

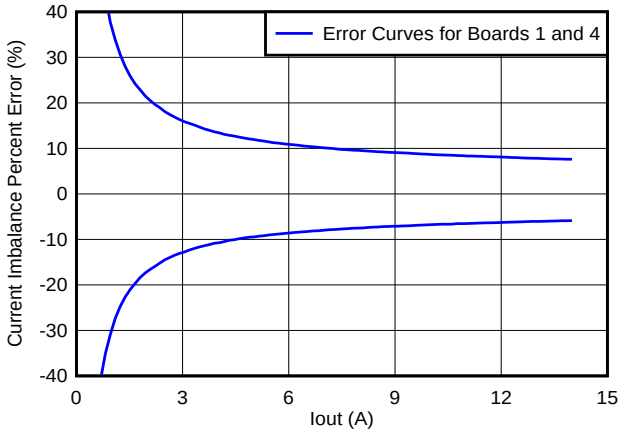


図 32. Sharing Error Boards 1 and 4

The following error plots have six LDOs (three boards in parallel).

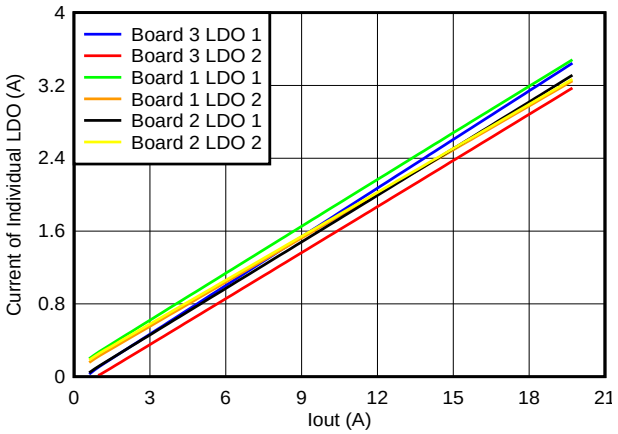


図 33. Sharing Boards 1, 2, and 3

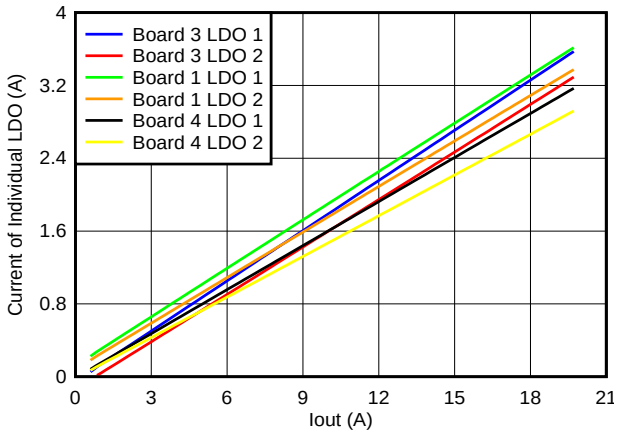


図 34. Sharing Boards 1, 3, and 4

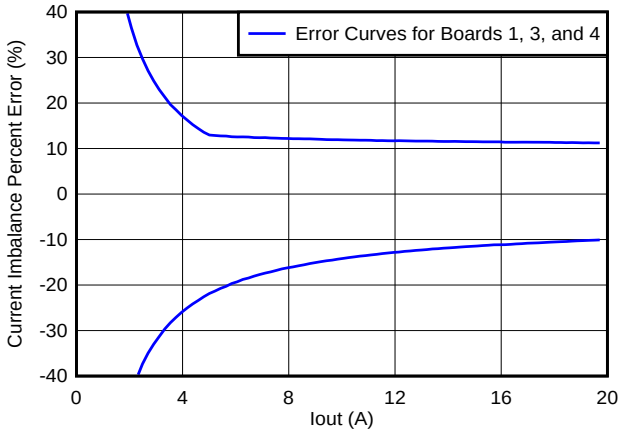


図 35. Sharing Error Boards 1, 3, and 4

3.2.2.4 Load Transients

The following scope shots show the load transient with I_{OUT_MAX} = 23 A in *red* and V_{OUT} in *blue*. The difference between input GND and output GND was subtracted from V_{OUT} to reduce the GND bounce at the output of the system. Note that three boards in parallel = six LDOs.

The ringing on 図 37 results from the inductance in the cables. Expect this ringing to be much flatter or even disappear if the load is on the same PCB as the LDOs.

図 36. Load Transient 0 A to 23 A

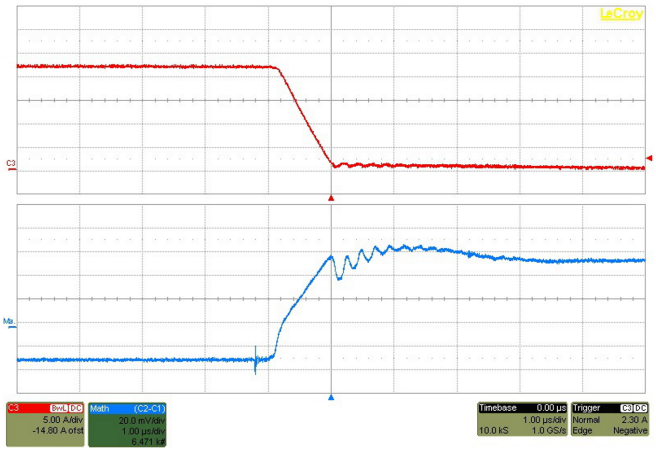


図 37. Load Transient 23 A to 0 A

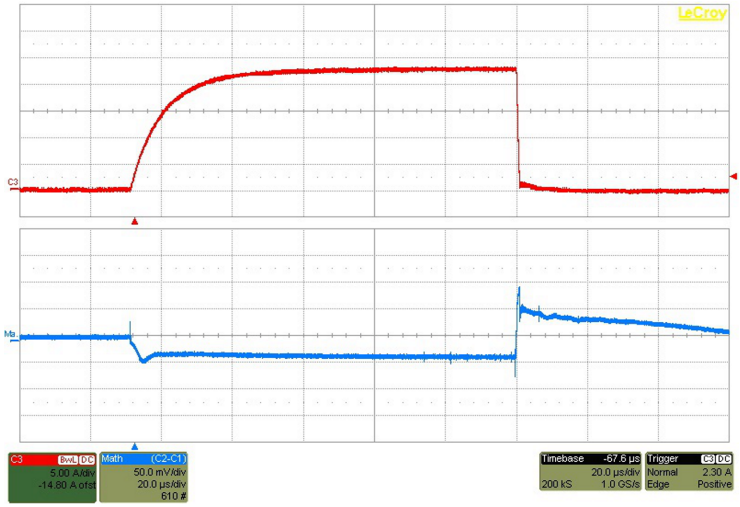


図 38. Load Transient 23 A

3.2.3 Comparison to TIDU421

表 3 shows a quick overview comparing two reference designs: TIDA-01232 and TIDU421. In summary, TI recommends the TIDA-01232 reference design if a very-high-current, low-noise voltage source is required and the TIDU421 reference design if high accuracy at the output is required.

表 3. Comparison Table

PARAMETER	TIDA-01232	TIDU421
LDOs parallel	Tested up to eight	Designed for two LDOs
Load regulations	Voltage drop over ballast resistor	Direct load regulation

表 **3. Comparison Table (continued)**

PARAMETER	TIDA-01232	TIDU421
Additional components	PCB resistance	Amplifier and shunt
Maximum tested current	23 A (six LDOs)	6 A (two LDOs)

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01232.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01232.

4.3 PCB Layout Recommendations

The available PCB design files correspond to “Rev B” of the schematics and layout. The changes to “Rev A” are as follows:

- The PCB ballast resistor has been changed from a longer, multi-layer design to a shorter single-layer design. The resistance of the PCB trace has not been changed and remains at 5 mΩ.
- The BIAS, V_{IN}, and GND test points have been moved to the edge of the board for easier access when boards are stacked together.
- Zener diodes have been added to clamp input as well as output voltages to prevent damaging the device due to voltage peaks generated by the high currents and the inductance of the cables. Zener diodes have also been used and populated in “Rev A”.
- Minor changes have been made on the silkscreen

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01232.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01232.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01232.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01232.

5 Related Documentation

1. Texas Instruments, *Ballast Resistors Allow Load Sharing Between Two Paralleled DC/DC Converters*, Application Report (SLVA250)
2. Texas Instruments, *TI Precision Designs: Verified Design 6A Current-Sharing Dual LDO*, TI Precision Design (TIDU421)
3. Texas Instruments, *TPS7A85 High-Current (4 A), High-Accuracy (1%), Low-Noise (4.4 µVRMS), LDO Voltage Regulator*, TPS7A85 Data Sheet (SBVS267)

5.1 商標

ANY-OUT is a trademark of Texas Instruments.

6 About the Author

NICOLÁS ROMÁN is an application engineer who did a rotation in a rotation in the Linear Power business unit. His final deployment will be as a field application engineer in the TI office in Zürich Switzerland. Nicolás graduated with a BSc FHO in Electrical Engineering at the HSR in Rapperswil, Switzerland (a University of applied science).

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