参考資料

TI Designs: TIDA-01160
UPSおよびインバータ用の小型のシングル・チャネル、絶縁ゲート・ドライバのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

TIDA-01160デザインでは、UPS、インバータ、充電パイル・アプリケーションの電力段の駆動に使用される、ハイサイドまたはローサイドの絶縁ゲート・ドライバ用のリファレンス・ソリューションを紹介します。

このTI Designは、UCC5320S 3kV$_{RMS}$基本絶縁ゲート・ドライバを基礎として、IGBTおよびSiC MOSFETを駆動します。
このリファレンス・デザインには、小型の1.5W絶縁 Fly-Buck™ゲート・ドライバ電源が内蔵されており、絶縁ゲート・ドライバの入力と出力に電力を供給します。

絶縁ゲート・ドライバと絶縁ゲート・ドライバの電源を、外形33mm×23mmの小型の基板に集積することで、このリファレンス・デザインは、完全にテスト済みの、堅牢で、独立し、検証が容易な、シングル・チャネルのドライバ・ソリューションを実現し、100kV/µsを超えるCMTIに耐えられます。

リソース

TIDA-01160	デザイン・フォルダ
UCC5320S	プロダクト・フォルダ
LM25017	プロダクト・フォルダ

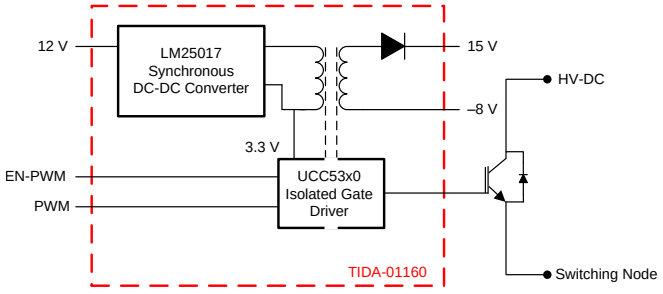
TI E2E™ Community　E2Eエキスパートに質問

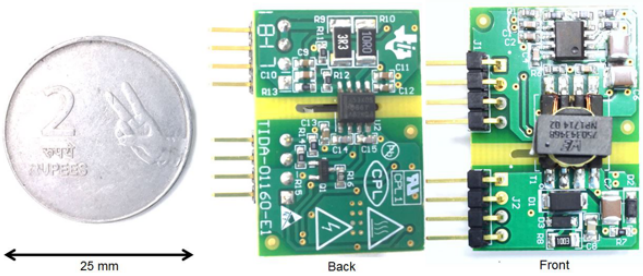
特長

- 単相および三相インバータや、中および高電圧電力コンバータ(100～230V AC)に最適
- 0.5A、2A、6A、10Aのソースおよびシンク電流から、MOSFET、IGBT、SiC-FETの駆動に適しており、最大100Aの電流と最高500kHzの動作周波数に対応
- 電源オンおよび電源オフのシーケンスにおける、IGBTやFETのスプリアスなターンオンおよびターンオフに対する保護
- 4000V$_{PK}$および2500V$_{RMS}$の絶縁バリア
- ドライバ・ソリューションは100kV/µsを超える高い同相過渡耐性を満たし、検証済み
- 低コストで部品数の少ない、小型の絶縁ゲート・ドライバ電源を内蔵して高電圧側の回路へ電力を供給し、負のバイアスによってノイズ耐性を実現
- 小型の外形(33mm×23mm)を持つゲート・ドライバ・ソリューション
- デジタルとアナログ両方のコントローラと簡単に接続
- オプトカプラをベースとするIGBTゲート・ドライバ・ソリューションの性能向上版として代替可能で、より低い伝搬遅延と高いCMTIを実現

アプリケーション

- 単相および三相UPS
- DCおよび家庭用インバータ
- DC充電パイル
- バッテリ充電器
- エネルギー・ストレージ・システム





1 System Description

Any uninterruptible power system (UPS) or DC charge pile system makes use of many gate drivers supporting the main power conversion circuits. Many of the circuits use an interleaved full-bridge LLC, three-level LLC stage in DC charge piles, single- or three-phase PFC, and single- or three-phase inverter in UPS systems. As the controlling MCU is referenced to the battery GND, these power stages require isolation to meet safety requirements, avoid ground loops, and voltage level translation.

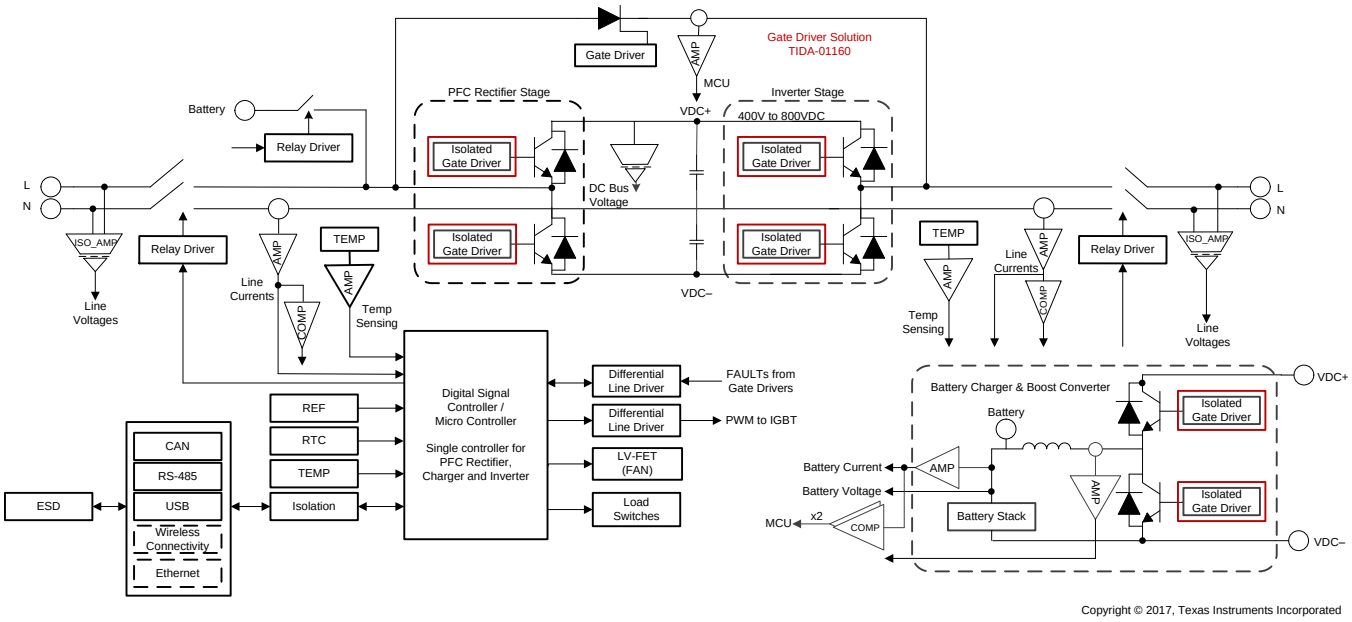


図 1. Reference Diagram for Online UPS

図 1 shows the reference diagram of an online UPS. For a single-phase UPS, the typical requirements for gate drivers are as follows:

表 1. Gate Driver Requirements

MARKET	REQUIREMENT
Isolation needed	≤ 2.5 kV_{RMS}
Driver power supply ratings	V_{IN}: 10 to 16 V (12- or 15-V bus are common); V_{OUT}: 15 V, –8 V; P_{OUT}: 1 to 2 W
Isolation transformer for power supply	≤ 2.5 kV_{RMS}

Considering the system requirements indicated in 表 1, an isolated gate driver solution is a key element in such systems performing high power (few kW) conversion.

The TIDA-01160 design is an attempt to provide protected gate driver solutions for MOSFET and IGBT/SiC-MOSFETs gate drives addressing different topologies.

The benefits of this reference design in these applications include:

- Compact form factor gate drive solution

- Built-in isolated gate driver power supply allows flexibility in routing
- Excellent common-mode transient immunity (CMTI) performance ensuring reliable switching
- Reliability further enhanced by independent undervoltage lockout (UVLO) on the gate drive supplies
- Low propagation delay makes control easier especially at higher switching frequencies

1.1 Key System Specifications

表 2. Key System Specifications

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input supply voltage (V_{IN})	—	10	12	17	V
Enable PWM	—	—	2.31	3.3	V
PWM threshold (L to H)	—	—	2.31	3.3	V
PWM threshold (H to L)	—	0	—	0.99	V
OUTPUT CONDITIONS					
Gate driver supply voltage input side (V_{CCI})	—	3	3.3	—	V
Gate driver positive supply voltage output side (V_{CC2})	This output is configurable	14	15	16	V
Gate driver negative supply voltage output side (V_{EE2})	This output is configurable	–9	–8	–7	V
Source current	C_{LOAD} = 100 nF, f = 20 kHz, Gate resistors: 1.1 Ω	—	10	—	A
Sink current		—	10	—	A
Propagation delay	—	—	125	130	ns
Gate driver power supply efficiency	V_{IN} = 12 V, load = 70 mA	—	75	—	%
SYSTEM CHARACTERISTICS					
Common-mode transient immunity (CMTI)	—	100	—	—	kV/µs
Operating ambient	—	–10	25	55	°C
Board size	Length × Breadth × Height	33 × 23 × 10			mm

2 System Overview

2.1 Block Diagram

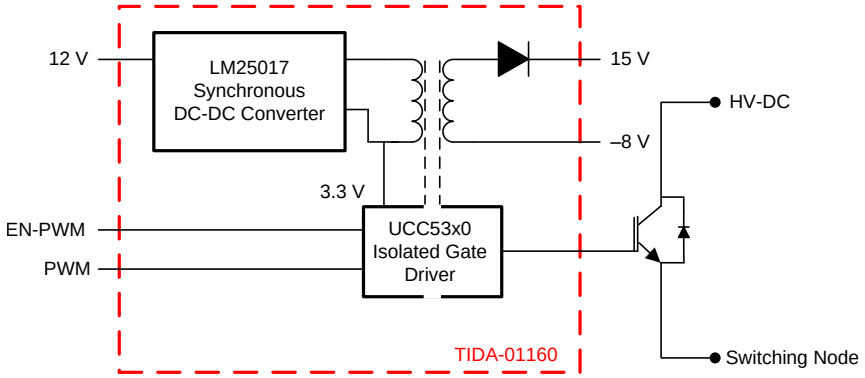


図 2. Block Diagram of TIDA-01160

図 2 shows the high-level block diagram of circuit. The main parts of this design are synchronous step-down converter (LM25017) and isolated gate driver (UCC5320S).

The TIDA-01160 board consists of two main circuit blocks: the isolated gate driver (UCC5320S) and the isolated gate driver power supply (LM25017 and transformer) for the gate drive. The primary side of the driver is powered from the 3.3-V power supply and the secondary side is powered from a 23-V isolated power supply. These voltages are derived from isolated Fly-Buck design with synchronous step-down (buck) converter (LM25017). The 23-V high-side supply voltage is configurable using external Zener diode network. Currently the outputs are set to 15 V and –8 V through a Zener network.

2.2 Highlighted Products

This TIDA-01160 reference design features the following devices, which were selected based on their specifications and appropriateness for this TI Design. The key features of the highlighted products are mentioned as follows. For more information on each of these devices, see their respective product folders at www.TI.com or click on the links for the product folders on the リソース on the first page of this design guide.

2.2.1 UCC5320S

The UCC53x0 is a family of compact, single-channel, isolated IGBT, SiC, and MOSFET gate drivers with superior isolation ratings and variants for pinout configuration and drive strength.

The UCC53x0 is available in an 8-pin SOIC (D) package. This package has a creepage and clearance of 4 mm and can support isolation voltage up to 3 kV_{RMS}, which is good for applications where basic isolation is needed.

The UCC53x0S option provides a split output that can be used to control the rise and fall times of the driver. The UCC53x0M option connects the gate of the transistor to an internal clamp to prevent false turnon caused by Miller current. The UCC53x0E option has its UVLO2 referenced to GND2, which facilitates bipolar supplies. The input side operates from a single 3- to 15-V supply. The output side allows for a supply range from 13.2- to 33-V supply

Unlike an optocoupler, the UCC53x0 family has lower part-to-part skew, lower propagation delay, higher operating temperature, and higher CMTI. Device operation is specified over an ambient temperature range from –55°C to 125°C ambient.

2.2.2 LM25017

For a buck converter to operate in Fly-Buck configuration, the converter has to meet certain criteria. For the Fly-Buck, the primary current flows reversely from output to input during Off time. This negative current will be blocked by the diode in the non-sync buck, which chokes the energy delivery to the secondary. As a result, the isolated output voltage will collapse. Therefore, a non-synchronous buck cannot be used. For some sync-buck converter ICs, the low-side FET is turned off, if negative current is detected in order to have light-load efficiency. In such cases the FET emulates the diode behavior, making such buck converters not suitable for the Fly-Buck configuration.

Also, not all control schemes are fit for the Fly-Buck. As the primary side current in off-time is different from a normal buck, a current-mode control relying on low-side FET current or valley current sensing will not work for the Fly-Buck.

Finally, to incorporate overcurrent and short-circuit protection, a synchronous buck IC that has a current limit on the high-side switch is a good choice because the current waveform in Fly-Buck converter during on-time is similar to a normal buck converter. For ICs that have a valley detect control circuit where the switch current is monitored during the OFF state, the overcurrent may not be detected because the primary current might never hit the overcurrent limit.

Based on this criteria, the LM25017 is used in this TI Design as it operates in continuous conduction mode (CCM) regardless of the output loading. It has constant on-time (COT) control, which is not affected by the current waveform, and the switching stability is easy to manage in converter design. The COT control is an easy-to-design control method; it has the duty on-time fixed and the duty off-time adjusted according to the compared signal between the output feedback ripple and a reference voltage. The advantage of the COT is that it does not require a loop compensation network, which keeps the circuit simple and has fast transient response.

The LM25017 device is a 48-V, 650-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The COT control scheme employed in the LM25017 device requires no loop compensation, provides excellent transient response, and enables very high step-down ratios. A peak current limit circuit protects against overload conditions. The UVLO circuit allows the input undervoltage threshold and hysteresis to be independently programmed.

2.3 System Design Theory

The TIDA-01160 board consists of two main circuit blocks: the isolated gate driver (UCC5320S) and the isolated gate driver power supply (LM25017 and transformer) for the gate drive. The primary side of the driver is powered from the 3.3-V power supply and the secondary side is powered from a 23-V isolated power supply. These voltages are derived from isolated Fly-Buck design with synchronous step-down (buck) converter (LM25017). The 23-V high-side supply voltage is split into 15 V and –8 V through a Zener network.

2.3.1 Fly-Buck versus Conventional Isolated Power Supply Schemes

Traditionally, designers have used different topologies to generate isolated rails, such as flyback converters, push-pull drivers with transformers, and so on. The Fly-Buck converter (or isolated buck converter) is gaining popularity as a low-power isolated bias solution because of its simplicity, ease-of-use, low BOM cost, and the availability of wide-V_{IN} integrated regulators.

The device results in a simpler solution than a flyback converter at lower power levels because of the integrated FETs and absence of isolated feedback loop. The most compelling solutions have been < 5 W, where tight regulation on the secondary voltage is not required, such as the power supply for gate drivers.

The Fly-Buck converter offers the primary non-isolated buck output at no additional cost. Therefore, it results in a simpler design for applications where both isolated and non-isolated outputs are required.

The design of the gate driver and Fly-Buck converter are described in the following subsections.

2.3.2 Isolated Gate Driver Design

図 3 shows the circuit for the UCC5320S and associated components.

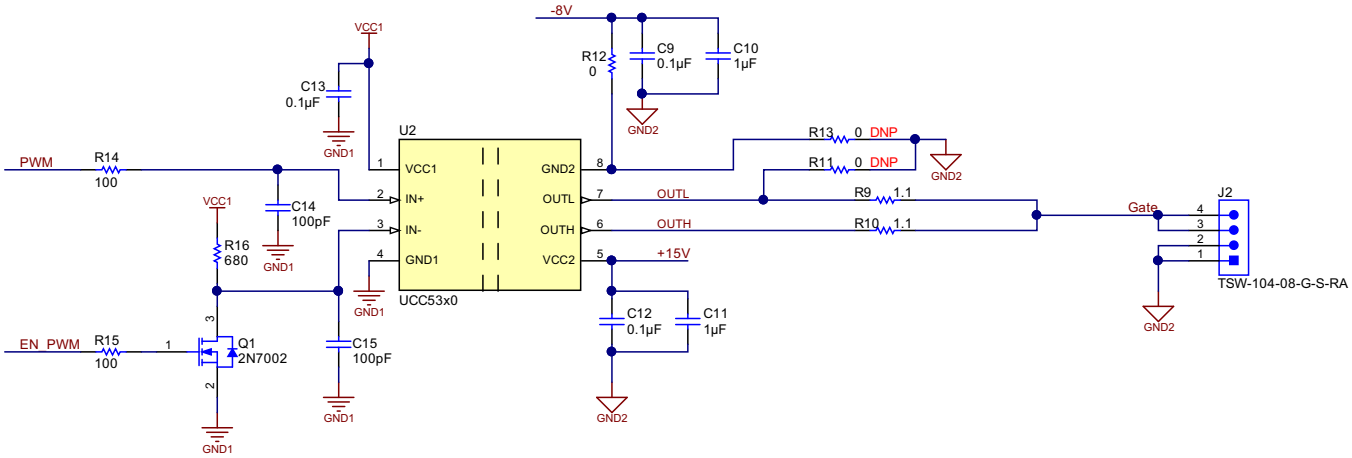


図 3. Isolated Gate Driver Design

This section goes into the details of the gate driver components dimensioning and power requirements. To calculate the required gate drive power, the C2M0040120D-Silicon Carbide Power MOSFET 1200 V 60 A is taken as an example.

2.3.2.1 Requirements for Gate Driver Power

The power consumed by the gate driver is the sum of the quiescent power consumption of the gate driver and the power required to supply the required gate charge to the load.

The quiescent power consumption of the gate driver is given using 式 1:

$$P_{QUIESCENT} = V_{VCCI} \times I_{VCCI} + V_{VCC2} \times I_{VCC2} \quad (1)$$

Substituting the values from the UCC5320 datasheet in 式 1:

$P_{QUIESCENT}$ = (3.3 V × 1.67 mA) + (23 V × 1.1 mA) = 30.811 mW.

The power required to charge and discharge the load (P_{DRV}) during each switching cycle is approximately given by 式 2:

$$P_{DRV} = Q_{GTOT} \times V_{CC2} \times f_{SW} \times \left(\frac{r_{on}}{r_{on} + R_{GON}} + \frac{r_{off}}{r_{off} + R_{GOFF}} \right) \quad (2)$$

Where:

- Q_{GTOT} represents the total gate charge of the power transistor switching. For the C2M0040120D-Silicon Carbide Power MOSFET 1200 V 60 A, Q_{GTOT} = 115 nC
- If a split rail is used to turn on and off, then V_{CC2} is going to be equal to difference between the positive rail to the negative rail. Here V_{CC2} is 15 – (–8) = 23 V.
- f_{SW} is the switching frequency at the control input IN+ (for SiC, use f_{SW} = 60 kHz)
- r_{on} represents the gate driver output resistance in on state
- r_{off} represents the gate driver output resistance in off state
- R_{GON} represents the gate resistor in on state

- R_{GOFF} represents the gate resistor in off state

To see the calculations used to determine R_{GON} and R_{GOFF},see 2.3.2.5.

Substituting these values in 式 2, P_{DRV} comes out to be 78.7 mW.

Therefore, the total power consumed by gate driver is given using 式 3:

$$P_{TOTAL} = P_{QUIESCENT} + P_{DRV} \quad (3)$$

P_{TOTAL}= 30.811 mW + 78.7 mW ≈ 109.511 mW

2.3.2.2 Primary-Side Gate Driver Voltage

VCC1 and GND1 are the supply pins for the input side of the UCC5320S. This voltage (V_{CC1} = 3.3 V) is generated from Fly-Buck converter (2.3.3) . A 0.1-µF capacitor C13 is placed close to the IC power supply to provide stable and clean power supply to the primary side of the gate driver.

2.3.2.3 Secondary-Side Gate Driver Voltage

VCC2 and GND2 are the supply pins for the output side of the UCC5320S. A positive V_{GE} of typically 15 V is required to switch the IGBT well into saturation. In this TI Design, V_{CC2} is fed with 15 V and GND2 with –8 V to ensure that IGBT is in full saturation. The secondary-side gate driver voltage is generated from Fly-Buck converter (2.3.3) and then split using a 15-V Zener and a 10-kΩ resistor to generate 15 V and –8 V. See 2.3.3.6 for more details. Capacitors (C9, C12 = 0.1 µF and C10, C11 = 1 µF) are placed close to the IC power supply to provide stable and clean power supply to the secondary side of the gate driver.

2.3.2.4 PWM Inputs

The device also features a dual-input configuration with two input pins (IN+ and IN–) available to control the state of the output. The user has the flexibility to drive the device using either a non-inverting input pin (IN+) or an inverting input pin (IN–). The state of the output pin is dependent on the bias of both the IN+ and IN– pins.

Once an input pin has been chosen for the PWM drive, the other input pin (the unused input pin) must be properly biased in order to enable the output. The unused input pin can effectively be used to implement an enable and disable function.

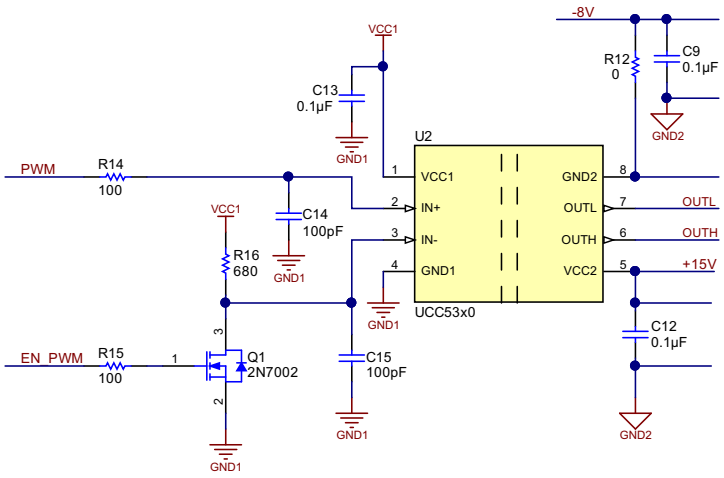


図 4. Using Device in Non-Inverting Configuration

To drive the device in a non-inverting configuration, the PWM control input signal is given to the IN+ pin. In this case, the unused input pin, IN–, must be biased low (for example, tied to GND) in order to enable the output. To implement the enable/disable function, the "EN_PWM" signal is given to the IN– pin through a transistor.

注: To ensure that output is enabled only when EN_PWM is high and is disabled otherwise, a transistor is connected to the IN– pin (see 図 4).

表 3 lists the output states and their inputs:

表 3. Device Logic Table

PWM (GIVEN TO IN+)	EN_PWM (GIVEN TO IN– THROUGH A TRANSISTOR)	GATE (PIN 3 AND 4 OF CONNECTOR J2)
High	High	High
Low	High	Low
High	Low	Low
Low	Low	Low

2.3.2.5 Source and Sink Currents and Gate Resistor Selection (R9, R10)

The gate current can be controlled using an external gate resistor between the driver output and the gate of the IGBT. The value of the gate resistor determines the peak charge and discharge currents. The UCC5320S device features a split-output configuration where the gate drive current is sourced through the OUTH pin and sunk through the OUTL pin. This pin arrangement provides flexibility to apply independent turnon and turnoff resistors to the OUTH and OUTL pins, respectively without the need for diode. The value of the gate resistor influences different aspects of the switching process:

- IGBT turnon and turnoff times
- Switching losses
- dv/dt across the IGBT collector to emitter
- di/dt of the IGBT current

Increasing the value of the gate resistor increases the turnon and turnoff times of the IGBT, which in turn reduces the dv/dt and di/dt, causing reduced EMI. Higher gate resistance also increases switching losses. Decreasing the gate resistance reduces switching losses but increases EMI.

The source and sink currents play a major role in determining turnon and turnoff delays of the power transistors. Ideally, the maximum current that can be sourced and sunk into the switching device can be found as follows:

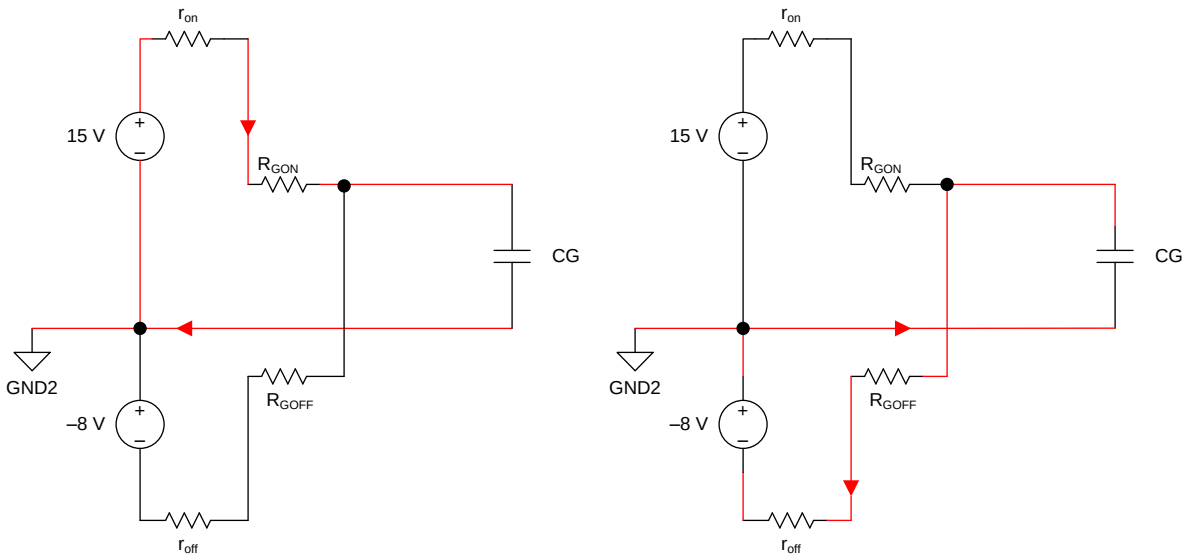


図 5. Simplified Model to Calculate Gate Resistors

2.3.2.5.1 Off to On Transition

In the off-state, the upper plate of the gate capacitance, CG, assumes a steady-state potential of –8 with respect to GND2. When turning on the power device, OUTH is applied to VOUT that results in a charge current of I_{SOURCE} = (15 V – (–8 V)) / (R_{GON} + r_{on}) (see 図 5). Using I_{SOURCE} = 10 A (for 10-A version gate driver) and solving for R_{GON} provides the necessary resistor value for a desired on-current using 式 4:

$$R_{GON} = \frac{\text{Voltage across IGBT gate}}{I_{SOURCE}} - r_{on} \quad (4)$$

In this TI Design, R_{GON}= R10 = 1.1 Ω.

2.3.2.5.2 On to Off Transition

In the on-state, the upper plate of the gate capacitance, CG, assumes a steady-state potential of 15 V with respect to GND2. When turning off the power device, OUTL is applied to VOUT that results in a charge current of I_{SINK} = (15 V – (–8 V)) / (R_{GOFF}+r_{off}). See 図 5. Using I_{SINK} = 10 A (for 10-A version gate driver) and solving for R_{GOFF} provides the necessary resistor value for a desired off-current using 式 5:

$$R_{GOFF} = \frac{\text{Voltage across IGBT gate}}{I_{SOURCE}} - r_{off} \quad (5)$$

In this TI Design, R_{GOFF}= R9 = 1.1 Ω.

Once the value of the gate resistors are determined, use 2.3.2.1 to calculate the gate driver power to make sure that it does not exceed the power dissipation rating of the gate driver.

2.3.3 Gate Driver Power Supply (Fly-Buck Converter) Design Using LM25107

An isolated buck converter, also known as a Fly-Buck converter, is created by replacing the output filter inductor (L1) in a synchronous buck converter with a coupled inductor (X1) or flyback-type transformer, and rectifying the secondary winding voltage using a diode (D1) and a capacitor (COUT2) as shown in 図 6 and 図 7.

For a buck converter to operate in Fly-Buck configuration, it has to meet certain criteria. For the Fly-Buck, the primary current flows reversely from output to input during off-time. This negative current is blocked by the diode in the non-sync buck, which chokes the energy delivery to the secondary. As a result, the isolated output voltage will collapse. Therefore, a non-synchronous buck cannot be used. For some sync-buck converter ICs, the low-side FET is turned off if negative current is detected in order to save light-load efficiency. In such cases, the FET emulates the diode behavior, making such buck converters not suitable for the Fly-Buck configuration.

Also, not all control schemes are fit for the Fly-Buck. As the primary side current in off-time is different from a normal buck, a current-mode control relying on low-side FET current or valley current sensing will not work for the Fly-Buck.

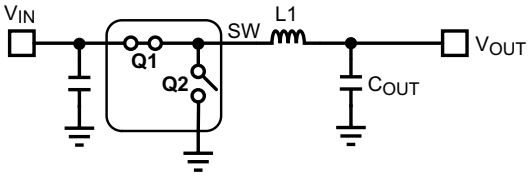


図 6. Synchronous Buck Converter

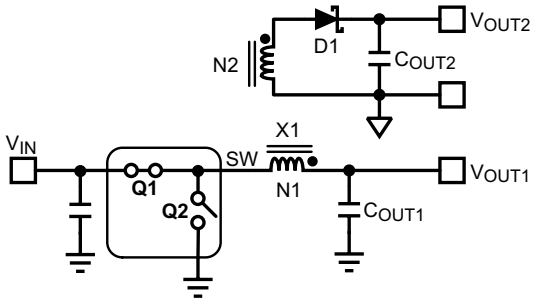
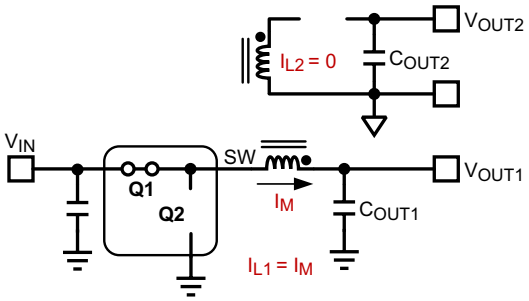


図 7. Isolated Buck Converter (Fly-Buck)

図 8 and 図 9 show the operating modes in an isolated configuration during TON, when the high-side buck switch is on, and TOFF, when the low-side switch is on, respectively.

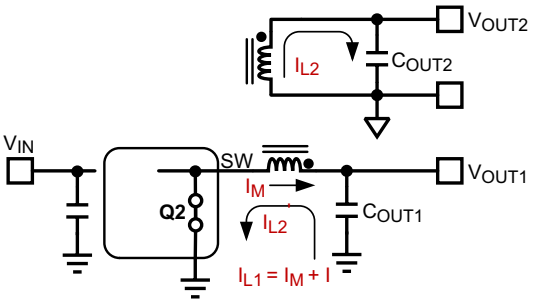
During TON, the current in the secondary winding is zero as the secondary diode is reverse biased. The current in the primary winding is the same as the magnetizing current (similar to a buck converter inductor).



2a) TON (Q1: ON, Q2: OFF)

図 8. Operation During TON (Q1 ON, Q2 OFF)

During TOFF, the current in the secondary winding is decided by the resonant tank formed by C_{OUT1}, the leakage inductance of the coupled inductor, and C_{OUT2}. The current in the primary winding is the sum of the magnetizing current (similar to a buck converter inductor current), and the reflected current from the secondary winding.



2b) TOFF (Q1: OFF, Q2: ON)

図 9. Operation During TOFF (Q1 OFF, Q2 ON)

表 4 presents design specifications for TIDA-01160.

表 4. Design Specification for Fly-Buck Converter

PARAMETER	VALUE
Input voltage range (V_{IN})	10 to 17 V
Primary output voltage (V_{OUT1}/V_{CC1})	3.3 V
Secondary output voltage (V_{OUT2})	23 V
Secondary output maximum power	1.5 W
Switching frequency (f_{SW})	500 kHz

Based on the criteria for Fly-Buck and the design requirements in 表 4, the LM25017 is chosen as the step-down converter.

The LM25017 device is a 48-V, 650-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs that employs COT control scheme. 図 10 depicts the implementation of the Fly-Buck converter with the LM25017.

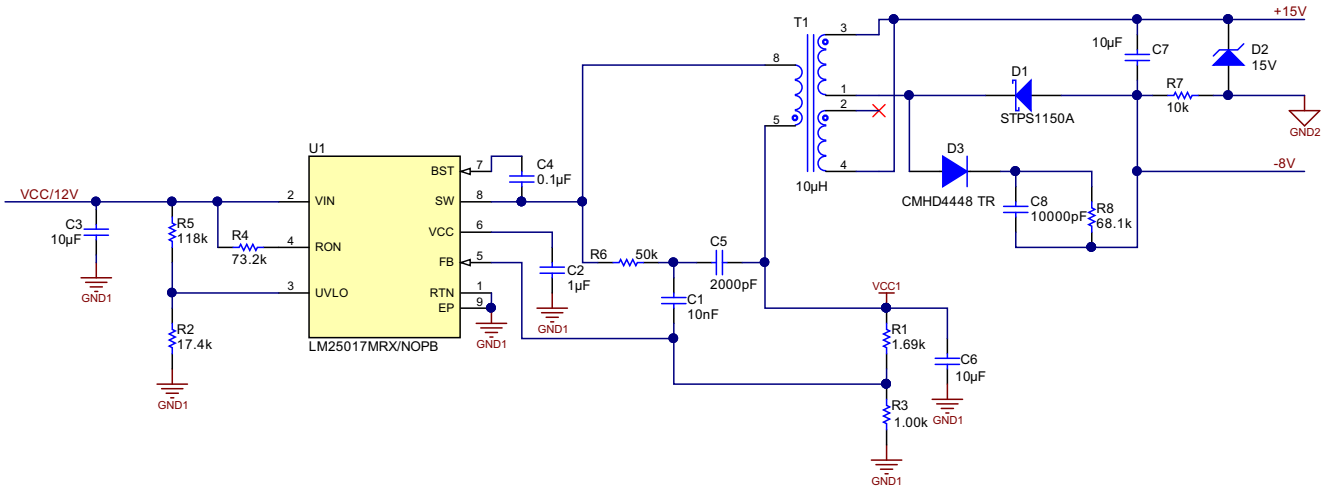


図 10. Implementation of Fly-Buck Converter With LM25017

2.3.3.1 Duty Cycle Calculations and Frequency Selection

The primary output voltage equation is identical to a buck converter and is given by 式 6:

$$V_{OUT1} = \frac{T_{ON}}{T_{ON} + T_{OFF}} \times V_{IN} = D \times V_{IN} \tag{6}$$

Where D is the duty cycle. With the minimum input voltage $V_{IN(MIN)}$ = 10 V, the maximum duty cycle is D_{MAX} = 0.33. Similarly, with the maximum input voltage $V_{IN(MAX)}$ = 17 V, the minimum duty cycle is D_{MIN} = 0.194.

It is recommended to keep the duty cycle below 40 percent during normal operation. As the isolated output only has the off-time window to get the transferred energy, it is important to have a healthy balanced duty cycle.

At maximum input voltage, the maximum switching frequency of LM25017 is restricted by the minimum T_{ON} as shown in 式 7:

$$f_{SW(MAX)} = \frac{D_{MIN}}{T_{ON(MIN)}} = \frac{0.194}{100\ ns} = 1.94\ MHz \tag{7}$$

Resistor R_{ON} sets the nominal switching frequency based on 式 8.

$$f_{SW} = \frac{V_{OUT1}}{K \times R_{ON}} \tag{8}$$

Where $K = 9 \times 10^{-11}$.

Operation at a high switching frequency results in lower efficiency while providing the smallest solution. For this TI Design with V_{OUT1} = 3.3 V, 500 kHz was selected, resulting in R_{ON} = 73.3 kΩ. Selecting a standard value for R_{ON} = R4 = 73.2 kΩ.

2.3.3.2 Turns Ratio Calculations

The secondary output voltage is given by 式 9:

$$V_{OUT2} = \frac{N2}{N1} \times V_{OUT1} - V_F \quad (9)$$

Where:

- V_F is the forward voltage drop of the secondary rectifier diode D1
- N1 and N2 are the number of turns in the primary and secondary windings, respectively

Using the values of V_{OUT1} and V_{OUT2} from 表 4 and V_F = 0.7 V, N2/N1 is almost equal to 7.

The transformer turns ratio (N1/N2) is taken as 1:7.

2.3.3.3 Primary Inductance Calculations (L1)

A coupled inductor or a flyback-type transformer is required for this topology. Energy is transferred from primary to secondary when the synchronous switch of the buck is on.

The primary inductance must be greater than $L_{PRI(MIN)}$ to avoid the peak switch current from exceeding the high-side power switch current limit (I_{HSCL}) . This value is calculated using 式 10:

$$L_{PRI(MIN)} = \frac{V_{OUT1} \times \left(1 - \frac{V_{OUT1}}{V_{IN}}\right)}{2 \times f_{SW} \times \left(I_{HSCL} - I_{OUT1} - I_{OUT2} \times \frac{N2}{N1}\right)} \quad (10)$$

The minimum high-side current limit (I_{HSCL}) for the LM25017 is peak limited to 0.7 A. If the current in the buck switch exceeds this limit, the present cycle is immediately terminated, and a non-resettable off-timer is initiated. Using I_{HSCL} = 0.7 A , $V_{IN(MAX)}$ = 17 V, I_{OUT1} = 10 mA (primary output current, accounting the gate driver consumption and other losses), I_{OUT2} = 45 mA (secondary output current) and using other parameters from 表 4, $L_{PRI(MIN)}$= 7.1 µH.

A higher value such as 10 µH is chosen to keep the high-side switch current below the minimum peak current limit.

Based on L1 = 10 µH, the ripple current (ΔI) is calculated using 式 11:

$$\Delta I_L = \frac{V_{OUT1} \times \left(1 - \frac{V_{OUT1}}{V_{IN}}\right)}{L \times f_{SW}} \quad (11)$$

The ripple current (ΔI) for $V_{IN(MAX)}$ = 17 V comes out to be 0.532 A.

A transformer from Wurth (750343468Rev02) with 1:7 turns ratio is chosen for this TI Design.

2.3.3.4 Peak Current and RMS Current Calculations

The primary positive peak current ($I_{L\_PRI\_POSPK}$) and primary negative peak current ($I_{L\_PRI\_NEGPK}$) are calculated using 式 12 and 式 13, respectively.

$$I_{LPRI\_POSPEAK} = I_{OUT1} + I_{OUT2} \times \frac{N2}{N1} + \frac{V_{OUT1} \times \left(1 - \frac{V_{OUT1}}{V_{IN}}\right)}{2 \times f_{SW} \times L} \quad (12)$$

$$I_{LPRI\_NEGPEAK} = -I_{OUT1} - I_{OUT2} \times \frac{N2}{N1} \times \frac{(1+D)}{(1-D)} - \frac{V_{OUT1} \times \left(1 - \frac{V_{OUT1}}{V_{IN}}\right)}{2 \times f_{SW} \times L} \quad (13)$$

- $I_{L\_PRI\_POSPK}$ = 0.591 A
- $I_{L\_PRI\_NEGPK}$ = – 0.74 A

It is important to make sure that $I_{L\_PRI\_POSPK}$ is less than 0.7 A (minimum high-side current limit for LM25017).

The high-side FET and low-side FET RMS currents are calculated as 0.154 A and 0.240 A, respectively using 式 14 and 式 15.

$$I_{HS\_RMS} = \sqrt{D \times \left(I_{OUT2} \times \frac{N2}{N1}\right)^2 + \frac{D}{12} \times \Delta I_L^2} \quad (14)$$

$$I_{LS\_RMS} = \sqrt{\frac{3D-1}{3 \times (1-D)} \times \left(I_{OUT2} \times \frac{N2}{N1}\right)^2 + \frac{\Delta I_L \times I_{OUT2} \times N_2}{3 \times N_1} + \frac{1-D}{12} \times \Delta I_L^2} \quad (15)$$

The sum of these currents I_{L_RMS}, meaning 0.395 A is the primary-side RMS current for the magnetic, which is calculated using 式 16:

$$I_{L\_RMS} = I_{HS\_RMS} + I_{LS\_RMS} \quad (16)$$

The inductor saturation current rating must be greater than the calculated peak current. This leaves margin for transient conditions if the peak inductor current increases above the steady state value. The RMS or heating current rating must be greater than the calculated RMS current.

2.3.3.5 Secondary Rectifier Diode

During TON, the current in the secondary winding is zero as the secondary diode is reverse biased by a voltage V_{D1} given by 式 17:

$$V_{D1} = V_{OUT2} + \left(V_{IN} - V_{OUT1}\right) \times \frac{N2}{N1} \quad (17)$$

For a $V_{IN(MAX)}$ = 17 V, a Schottky diode of 150 V, 1 A is selected.

2.3.3.6 Split Scheme of Secondary Output Voltage

The secondary-side output voltage (23 V) is split using a 15-V Zener (D2) and a 10-kΩ resistor (R7) as shown in 図 11 to generate 15 V and –8 V. With the Zener diode, the 15-V rail can have a stable output with a tight regulation tolerance, which is important for the turnon speed of high-power IGBTs. For –8 V, using the resistor provides a larger variation margin, but the negative bias is less critical in terms of the level of accuracy. The purpose of the negative bias is to prevent a high dv/dt induced false turnon of the IGBT. As long as the negative bias has low enough potential, it can maintain the secure turnoff of an IGBT.

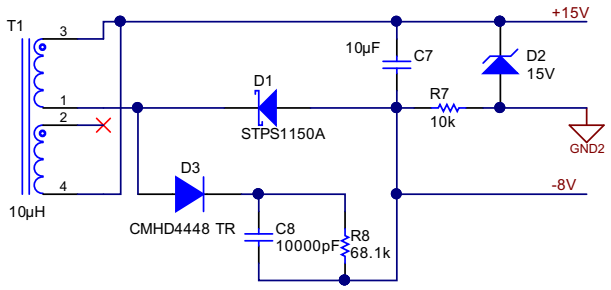


図 11. Split Scheme of Secondary Output Voltage

For a practical Fly-Buck design, preload may be needed on the isolated outputs, depending on the load profile. If running at no load, a voltage spike appears at the switching end of the transformer and pumps some current through the diode to the output capacitor. Without a load current to discharge the output capacitor in time, the output voltage could build up much higher than the designated value. Therefore, some minimum base load current is always needed.

Therefore, the split scheme not only provides the flexibility of setting the positive and negative voltage levels, but also acts as a preload for isolated output.

The current flowing in resistor R7 can be calculated using 式 18:

$$I_{R7} = \frac{0 - (-8)}{10\ k\Omega} = 0.8\ mA \tag{18}$$

The power dissipation across R7 = 0.8 mA × 0.8 mA × 10 kΩ = 6.4 mW. The amount of current flowing through the Zener is also approximately equal to the current flowing in the resistor R7. The peak currents required for driving IGBT gate will be supplied from the decoupling capacitors. The power dissipation of the Zener = 15 V × 0.8 mA = 12 mW. The power dissipation capacity of the diode used is 370 mW at 25°C.

2.3.3.7 Feedback Resistors (R1, R3) Selection

The output voltage is set with a resistor divider from the output node, VCCI (see 図 10), to the FB pin of the LM25017. TI recommends using 1% tolerance or better divider resistors. Use 式 19 to calculate the value of resistors:

$$V_{OUT1} = 1.225 \times \left(\frac{R_{FB2}}{R_{FB1}} + 1 \right) \tag{19}$$

Standard values are chosen with R_{FB2} = R1 = 1.69 kΩ and R_{FB1} = R3 = 1.00 kΩ.

2.3.3.8 Capacitors C3, C6, and C7 Selection

The total input capacitance should be large enough to limit the input voltage ripple to a desired amplitude. For the input ripple voltage ΔV_{IN}, C_{IN} can be calculated using 式 20 where $I_{OUT(MAX)}$ is calculated using 式 21:

$$C_{IN} \geq \frac{I_{OUT(MAX)}}{4 \times f_{SW} \times \Delta V_{IN}} \tag{20}$$

$$I_{OUT\,(MAX)} = I_{OUT1} + \frac{N2}{N1} \times I_{OUT2} \tag{21}$$

Choosing a ΔV_{IN} of 50 mV gives a minimum C_{IN} of 3.25 µF. A standard value of 10 µF is selected for C_{IN}= C3 in this TI Design. The voltage ratings of the capacitor should be greater than the maximum input voltage under all conditions.

A simplified waveform for secondary output current (I_{OUT2}) and the current in the secondary winding is shown in 図 12.

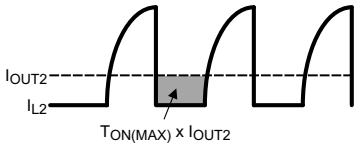


図 12. Secondary Output Current

The secondary output current (I_{OUT2}) is sourced by C_{OUT2} during one time TON. Ignoring the current transitions time in the secondary winding, the secondary output capacitor ripple voltage can be calculated using 式 22:

$$\Delta V_{OUT2} = \frac{I_{OUT2} \times T_{ON(MAX)}}{C_{OUT2}} \quad (22)$$

Setting C_{OUT2} to be 10 µF and using $T_{ON(MAX)}$ from 式 6, the ripple voltage comes out to be 2.97 mV. A capacitor with a 10-µF, 50-V rating is chosen for C7.

図 13 shows the primary winding current waveform (I_{L1}). The reflected secondary winding current adds to the primary winding current. Because of this, the output voltage ripple is not the same as in a non-isolated buck converter. Because the majority of the load current is drawn from the secondary isolated output, the primary output voltage ripple is given by 式 23.

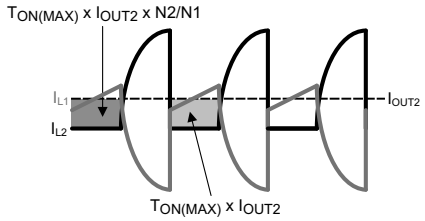


図 13. Primary-Side Current

$$\Delta V_{OUT1} = \frac{\left(I_{OUT2} \times \frac{N2}{N1}\right) \times T_{ON(MAX)}}{C_{OUT1}} \tag{23}$$

Setting a target of ΔV_{OUT1} = 50 mV, C_{OUT1} comes out to be 4.158 µF.

A capacitor with a 10-µF, 25-V rating is chosen for C_{OUT1} = C6.

2.3.3.9 Ripple Circuit (C1, C5, R6)

The LM25017 device uses COT control in which the on-time is terminated by an on timer and the off-time is terminated by the feedback voltage (V_{FB}) falling below the reference voltage (V_{REF}; see 図 14). Therefore, for stable operation, the feedback voltage must decrease monotonically, in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage (V_{FB}) during off-time must be larger than any noise component present at the feedback node. Therefore, the ripple is needed on the feedback pin.

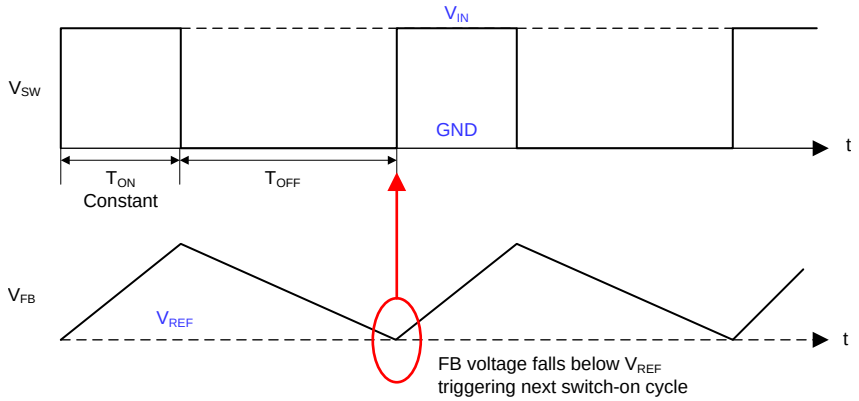


図 14. COT Control Regulation

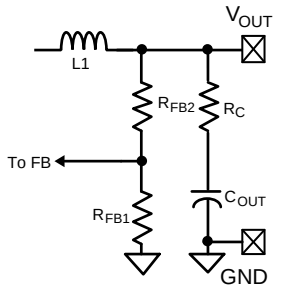
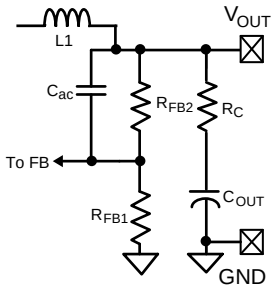
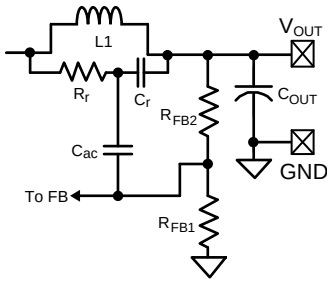
There are many ways to generate ripple as shown in 表 5.

The Type-1 circuit is implemented by adding a resistor in series with the output capacitor. This circuit adds the ripple that is needed for the regulation. This is a low-cost solution, but it has the undesirable effect of having some quantity of ripple on the output voltage. The feedback pin voltage is compared to the band gap voltage of 1.225 V. With a 3.3-V output, there is a 2.7:1 ratio with the resistor divider. The result is three times the amount of ripple on the actual voltage. Therefore, if the amount of ripple in the feedback pin is large, then the ripple on the output voltage will be even larger, which may not be desirable.

The Type-2 circuit is implemented by adding a capacitor across the upper feedback resistor. This circuit has the effect of producing same ripple on the feedback voltage and output voltage. Therefore, the output ripple is reduced. The capacitive ripple is not in phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output node for stable operation. If this condition is not satisfied unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time.

The Type-3 circuit artificially generates the desired ripple information and feeds it to the controller. The capacitor Cr integrates the current through Rr, which is proportional to the voltage across it. This is the same voltage that appears across the inductor. The coupling capacitor Cac couples the ramping voltage into the feedback pin. This approach does not require a resistor for the ripple on the output voltage, and result in a very low output ripple.

表 5. Ripple Configuration

TYPE 1 LOWEST COST CONFIGURATION	TYPE 2 REDUCED RIPPLE CONFIGURATION	TYPE 3 MINIMUM RIPPLE CONFIGURATION
		

The Type-3 ripple circuit is required for the Fly-Buck topology. Type-1 and Type-2 ripple circuits use series resistance and the triangular inductor ripple current to generate ripple at V_{OUT1} and the FB pin. The primary ripple current of a Fly-Buck is the combination or primary and reflected secondary currents as shown in 図 13. In the Fly-Buck topology, Type-1 and Type-2 ripple circuits suffer from large jitter as the reflected load current affects the feedback ripple.

The ripple circuit uses R_r (R6), C_r (C5), and the switch node (SW) voltage to generate a triangular ramp (図 15). The ripple current does this by integrating the voltage across the inductor and coupling the resulting AC signal to the FB pin through capacitor Cac (C1).

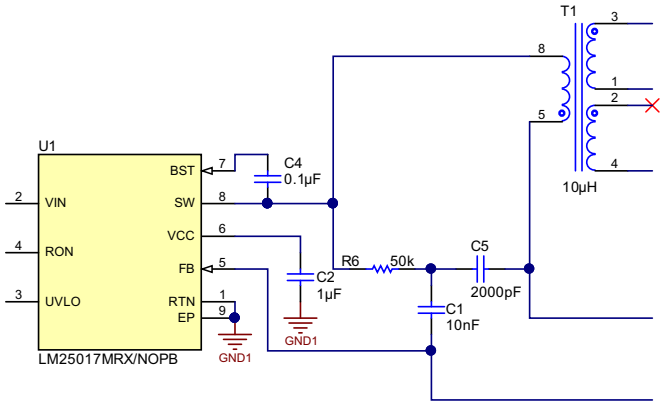


図 15. Ripple Circuit

For a COT converter to be stable, the injected in-phase ripple must be larger than the capacitive ripple on C_{OUT1}. The feedback ripple component values are calculated as follows:

- C_r (C5): The impedance of the integrator capacitor should be small compared to the feedback divider impedance at the desired switching frequency. The impedance of the feedback network is the parallel combination of $R_1||R_3$ (see 式 24). A value of C5 = 2200 pF is chosen.

$$C_r > \left(\frac{R_1 + R_3}{R_1 \times R_3}\right) \times \frac{1}{2 \times \pi \times f_{SW}} \tag{24}$$

- R_r (R6): Because $V_{IN} - V_{OUT1}$ is very large compared to the ripple voltage being produced, consider R6 as being a current source. The current is simply $(V_{IN} - V_{OUT1}) / R_r$.

  A charging capacitor obeys the following: I/C = dv/dt. For V_{IN}, based on the operation frequency and duty cycle, the on-time can be calculated, this is the dt. The dv term is the minimum required ripple, and C_r is as calculated previously. A minimum of 25-mV ripple voltage at the feedback pin (FB) is required for the LM25017 device. Therefore, Rr is calculated using 式 25:

$$R_r = \frac{\left(V_{IN} - V_{OUT1}\right) \times T_{ON}}{C_r \times V_{ripple}} \tag{25}$$

  The calculated value for R_r should be < 106 kΩ. This value provides the minimum ripple for stable operation. A smaller resistance should be selected to allow for variations in T_{ON}, C_{OUT1}, and other components. For this TI Design, R6 = 49.9 kΩ is selected.

- Cac (C1): The AC coupling capacitor should be at least three to four times larger than the integrator capacitor (C_r). A value of C1 = 10 nF.

2.3.3.10 V_{cc} and Bootstrap Capacitor

A 1-µF capacitor of 16 V or higher rating is recommended for the V_{CC} regulator bypass capacitor (C2).

A good value for the BST pin bootstrap capacitor (C4) is 0.1-µF with a 16-V or higher rating.

2.3.3.11 UVLO Resistors (R2, R5)

UVLO resistors set the UVLO threshold and hysteresis according to 式 26 and 式 27:

$$V_{IN}\left(\text{UVLO, rising}\right) = 1.225 \times \left(\frac{R_{UV2}}{R_{UV1}} + 1\right) \tag{26}$$

$$V_{IN\,(HYS)} = I_{HYS} \times R_{UV2} \tag{27}$$

Where:

- I_{HYS} = 20 µA, typical

For a UVLO hysteresis of about 2.5 V and UVLO rising threshold around 10 V, R_{UV1} (R2) of 17.4 kΩ and R_{UV2} (R5) of 118 kΩ are selected for this TI Design.

2.3.3.12 RCD Snubber Design (R8, C8, D3)

An RCD snubber is placed across the secondary side diode (D1) to reduce the ringing when the diode is off.

3 Hardware, Testing Requirements, and Test Results

This section explains the top and bottom views of the PCB for the TIDA-01160, showing all the different sections. This section also explains the power supply requirement and connectors used to connect the external world.

3.1 Required Hardware

3.1.1 TIDA-01160 PCB Overview

図 16 and 図 17 show the top and bottom view of the TIDA-01160 PCB, respectively.

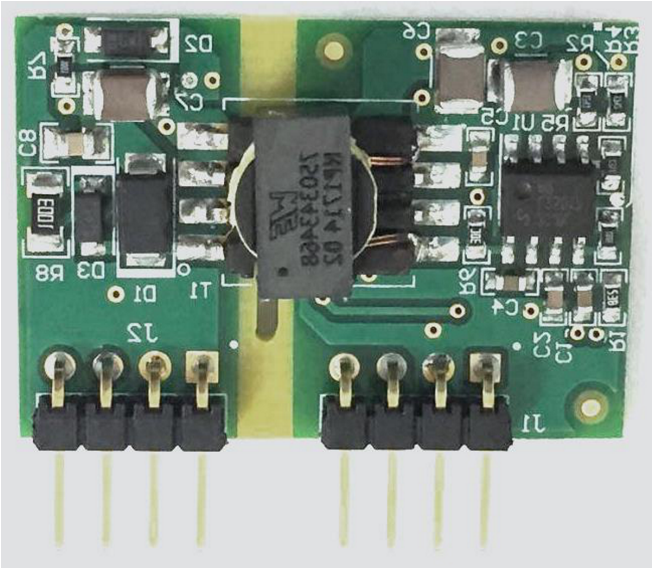


図 16. Top View of TIDA-01160

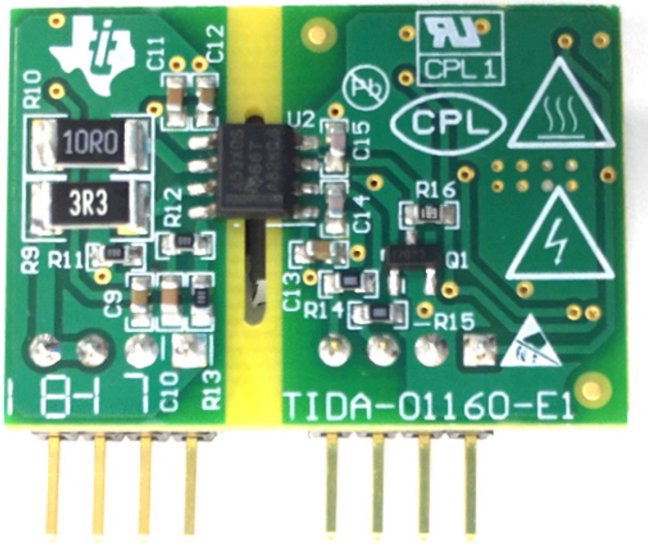


図 17. Bottom View of TIDA-01160

3.1.2 Connectors

表 6 shows the connectors used on the TIDA-01160 PCB and their purposes.

表 6. Connectors

CONNECTOR	PIN NO	PIN NAME	PURPOSE
J1	1	VCC/12 V	Input pin to LM25017
	2	GND1	Input ground
	3	EN_PWM	Enable PWM
	4	PWM	PWM input
J2	1	GND2	Secondary-side ground
	2	GND2	Secondary-side ground
	3	Gate	Input to gate terminal of power switch
	4	Gate	Input to gate terminal of power switch

3.2 Testing and Results

3.2.1 Test Setup

To test the TIDA-01160 board, a half-bridge power stage is used. A top-level representation of the test setup for the half-bridge is shown in 図 18.

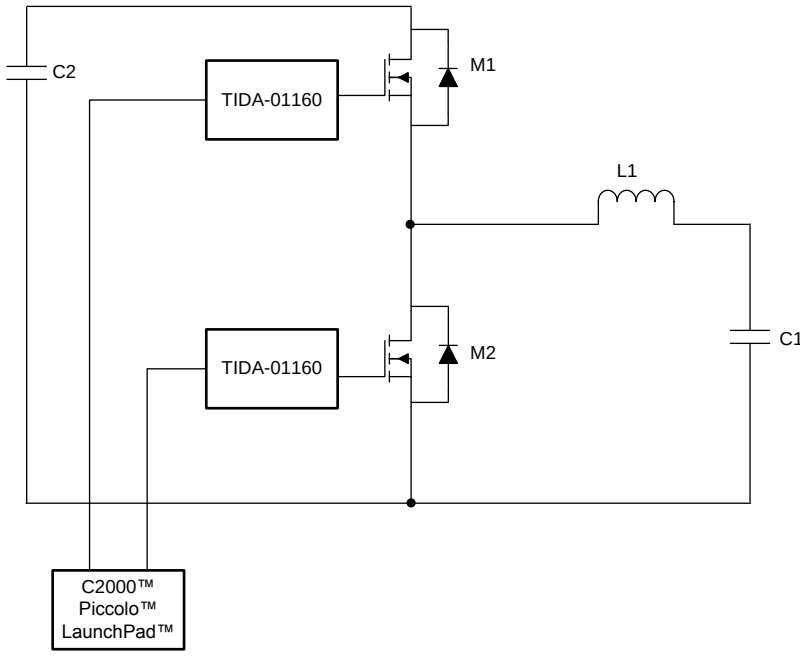


図 18. Test Setup (Half-Bridge) for TIDA-01160

The TIDA-01160 design is connected to the half-bridge power stage, comprising of SiC FET M1, M2, the inductor L1 and capacitors C1 and C2. One TIDA-01160 board is used as a high-side gate driver and connected to M1, while the other TIDA-01160 board is used as a low-side gate driver and connected to M2. The C2000™ Piccolo™ LaunchPad™ is used to generate PWM and EN_PWM signals for driving the half-bridge power stage.

3.2.2 Test Equipment

To validate the board, gather the following equipment:

- DC source: 0- to 400-V DC, 2.5 A rated
- DC source: 0 to 30 V, 500 mA
- Four-channel digital oscilloscope
- Current probe: 0 to 30 A, 50 MHz
- Electronic or resistive load capable of working up to 400 V, 2.5 A
- C2000 LaunchPad or other source for generating PWM and EN_PWM signals

3.2.3 Test Conditions

- Input: The half-bridge power stage needs to be powered from the 0- to 400-V DC power stage. The 0- to 30-V power source is used as the auxiliary power supply to power the TIDA-01160 board.
- Output: The output of the half-bridge power stage is connected to the electronic or resistive load. The load must be capable of varying from 0 to 2.5 A.
- Signal: For the half-bridge stage, set the appropriate dead time between the PWM signals of the high side and low side. Connect EN_PWM to the pin 3 of J1.

3.2.4 Test Procedure

1. Set the 0- to 30-V auxiliary supply to 12 V with a current limit of 500 mA and connect it to J1 pin 1 (VCC/12 V) and pin 2 (GND1) of the TIDA-01160 board.
2. Connect the PWM generated from the C2000 LaunchPad or any other source to J1 pin 4 (PWM) of the TIDA-01160 board.
3. Connect 3.3 V from the C2000 LaunchPad or any other source to J1 pin 3 (EN_PWM) of the TIDA-01160 board.
4. Connect the 0- to 400-V DC power supply to the half-bridge converter input.
5. Connect the electronic or resistive load to the half-bridge converter output.
6. Power up the 0- to 400-V DC power supply to 100 V.
7. Slowly increase the electronic or resistive load to about 100 mA.
8. Increase the 0- to 400-V DC power supply to 400 V.
9. Increase the electronic or resistive load to about 1 A.
10. Capture the switching waveforms in the oscilloscope.

3.3 Test Results

This section shows the test results for the TIDA-01160 design. To see the test conditions and procedure, see 3.2.4.

3.3.1 CMTI Waveforms

This section shows the CMTI test results. The CMTI test is important to characterize the immunity of the gate driver when it experiences high dv/dt transients. In a half-bridge gate driver, the switching node experiences high dv/dt, which can then couple to the gate driver's input pins and distort the PWM signal. Hence, it is important to have a high dv/dt immunity.

For this test, the PWM and EN_PWM inputs (Pin 3 and Pin 4 of J1) were tied to VCC, and a transient pulse was applied across the two grounds with the test port. During the test, the slew rate of the transient was increased and change in the output state was observed.

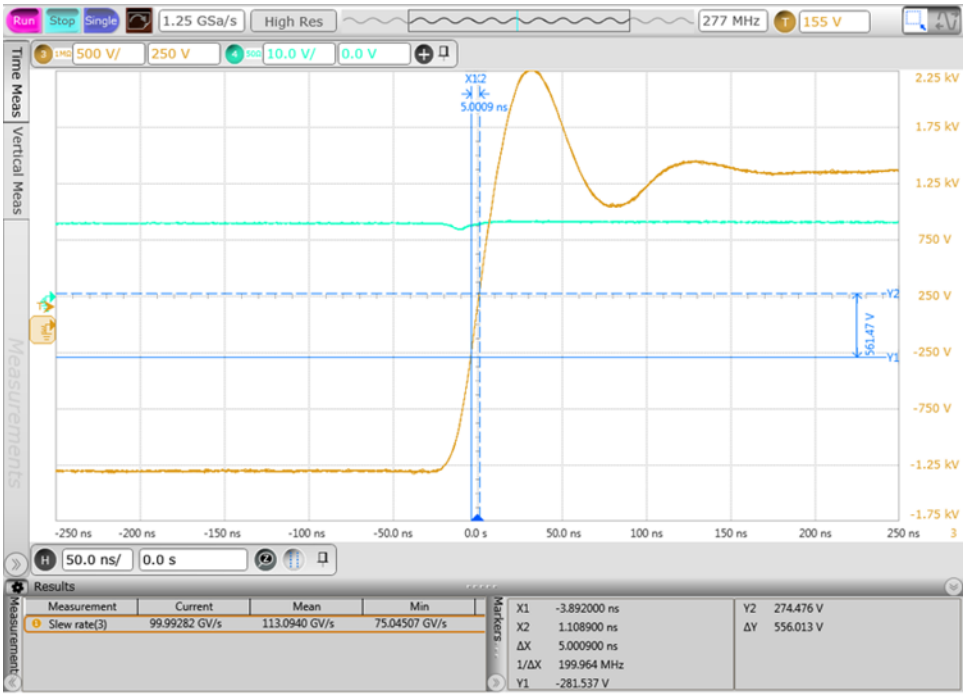


図 19. CMTI 100-kV/µs Pass

In 図 19, the yellow trace is the CMTI pulse applied and the green trace is the gate drive output. The output does not go low even when a CMTI pulse of > 100 kV/µs is applied.

3.3.2 Propagation Delay Waveforms

図 20 and 図 21 show the turnon and turnoff propagation delays measured for the gate driver. A propagation delay of 125 ns is seen. This propagation delay also takes into account the RC filter connected at the input PWM pin.

注: Green trace: PWM input 2 V/div; Blue trace: Gate driver output 10 V/div

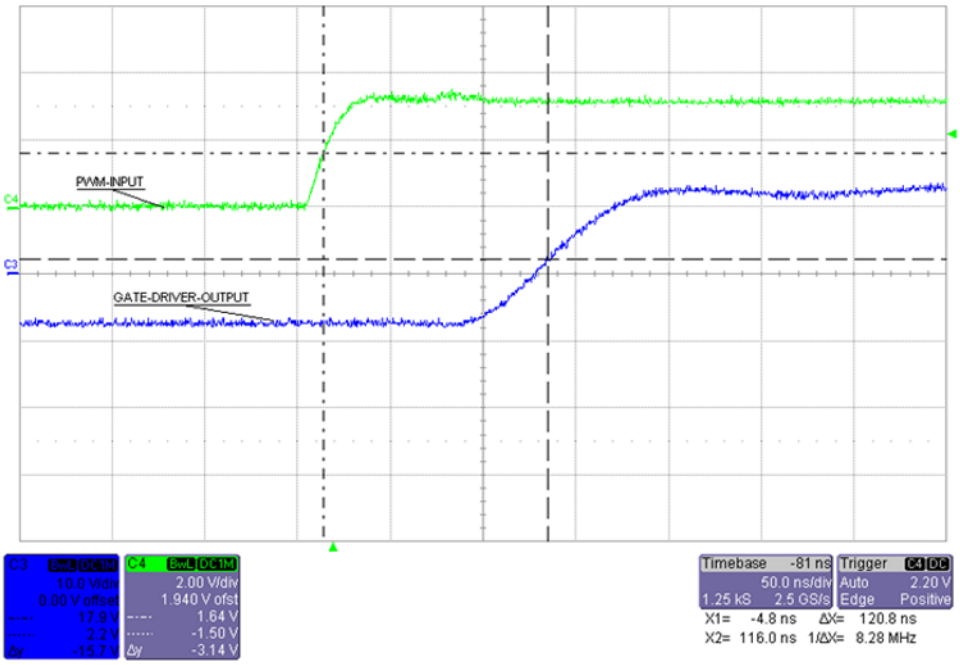


図 20. Gate Driver Propagation Delay (Rising)

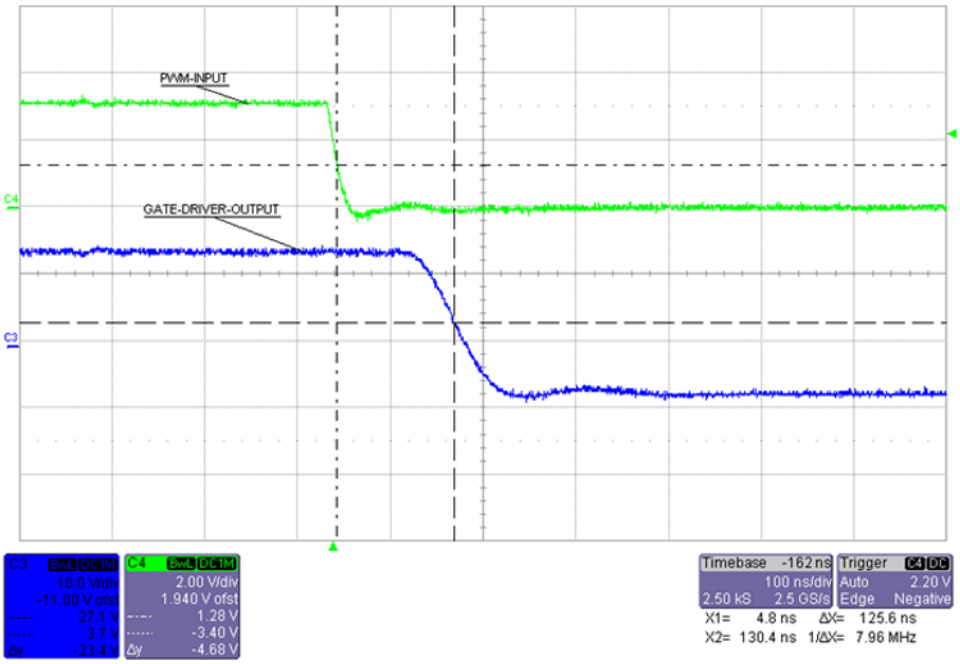


図 21. Gate Driver Propagation Delay (Falling)

3.3.3 Source and Sink Current

図 22 through 図 24 show the source and sink currents delivered directly by the UCC53xx (10-A version). The test was conducted for a 100-nF load at 20-kHz switching frequency and 1.1-Ω gate resistors for both turnon and turnoff. The gate drive source current reaches 10 A and sink current is 10 A.

注: Blue trace: Gate driver output 10 V/div; Pink trace: Gate current 5 A/div

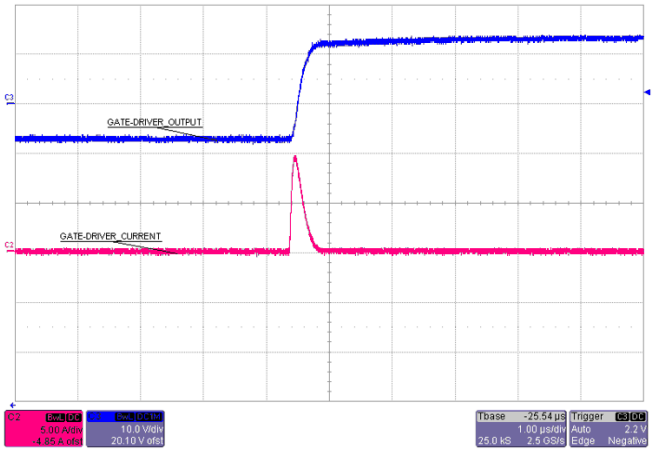


図 22. Gate Driver Output—Source Current

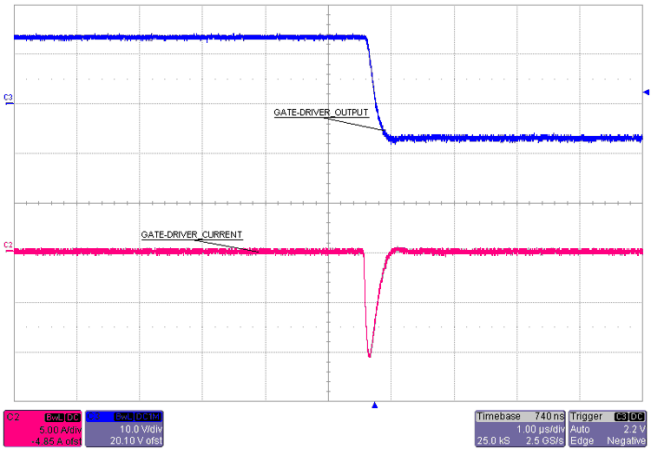


図 23. Gate Driver Output—Sink Current

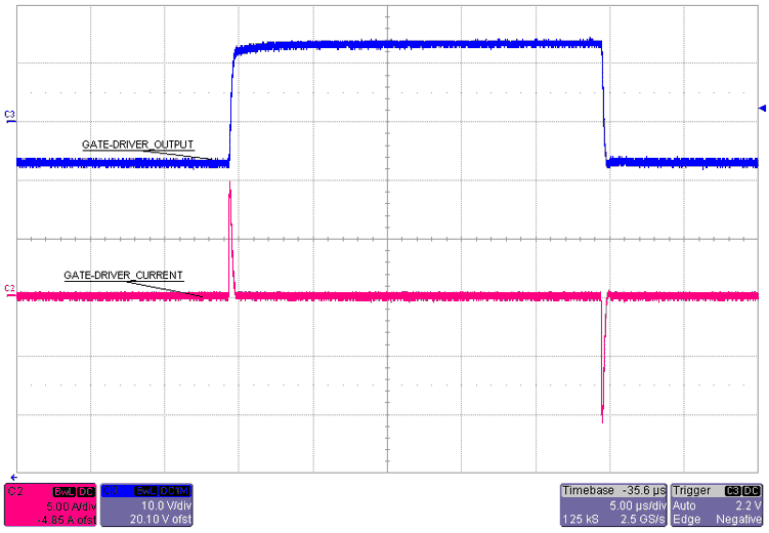


図 24. Source and Sink Current

3.3.4 Gate Driver Switching Waveforms

The gate driver was connected to a half-bridge power stage and the switching waveforms were observed. For a detailed test setup, see 3.2.1.

The test conditions include:

- N-channel SiC power MOSFET: Cree/Wolfspeed C2M0040120D-ND
- $R_{G(ON)}$: 1.1 Ω
- $R_{G(OFF)}$: 1.1 Ω
- Internal resistance: 1.8 Ω
- Gate charge (Q_G): 115 nC
- Input capacitance C_{ISS}: 1893 pF

図 25, 図 26, and 図 27 show the switching node waveforms of the high-side gate driver. For these figures, the red waveform is the gate to source voltage, the blue waveform is the drain-to-source voltage for the high-side driven MOSFET, and the pink waveform is the half-bridge inductor current.

図 25. High-Side Switching Waveform

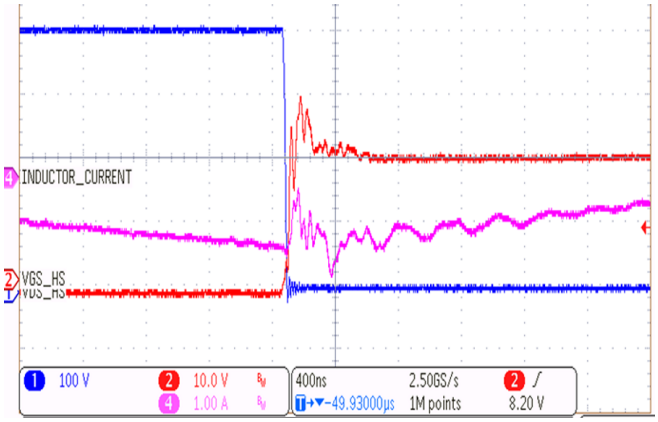


図 26. High-Side Switching Waveform (Zoomed, Turnon)

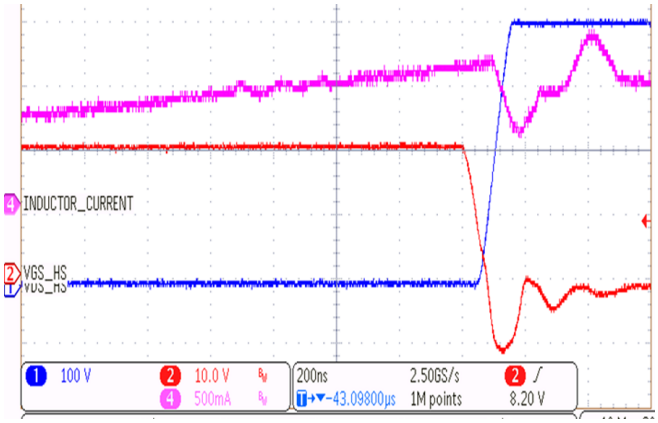


図 27. High-Side Switching Waveform (Zoomed, Turnoff)

3.3.5 UVLO Protection Test

図 28 and 図 29 show the undervoltage lockout for the input power supply of the gate driver. The output PWM starts only when the input power supply of the gate driver reaches a threshold as defined in the UCC5320 datasheet. There is no spurious behavior at startup

注: Yellow trace: 3.3-V rail 5 V/div ; Blue trace: Gate driver output 10 V/div; Green trace: PWM from controller 5 V/div.

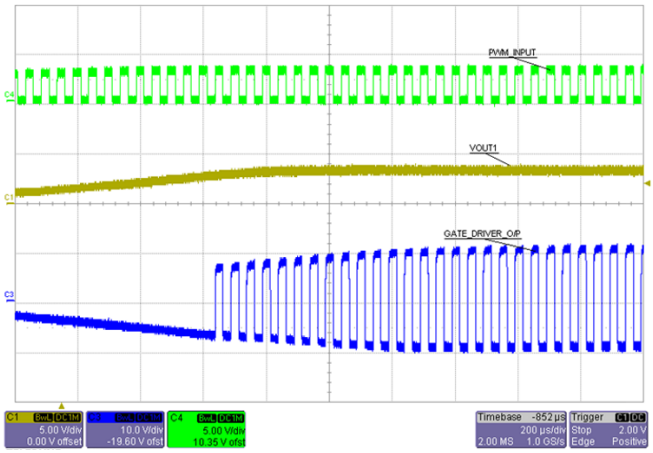


図 28. Gate Driver Input-Side UVLO During Power ON

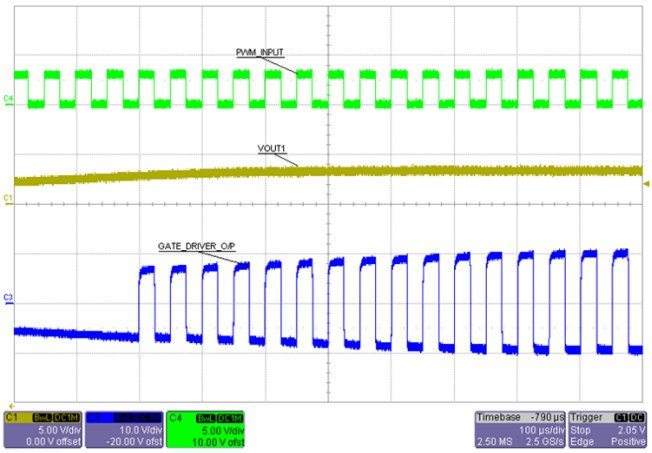


図 29. Gate Driver Input-Side UVLO (Zoomed) During Power ON

図 30 and 図 31 show the undervoltage lockout for output power supply of the gate driver. The output PWM starts only when the power supply of the gate driver reaches a threshold as defined in the UCC5320 datasheet. There is no spurious behavior at startup.

注: CH1: 15-V rail; CH2: Gate driver output; CH3: PWM from controller; CH4: –8-V rail

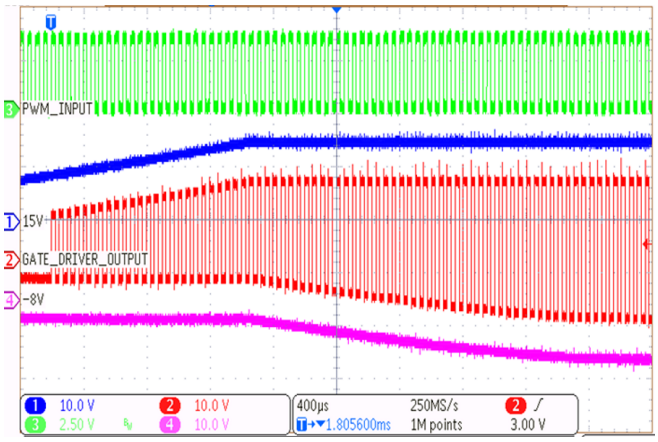


図 30. Gate Driver Output-Side UVLO During Power ON

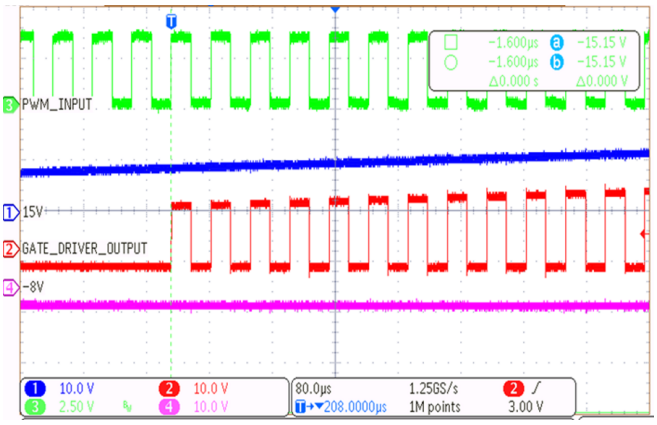


図 31. Gate Driver Output-Side UVLO During Power ON (Zoomed)

3.3.6 Fly-Buck Switching Node and Primary Current Waveforms

図 32 shows the switch node (SW) waveform and primary side inductor current for the 12-V input at full load.

注: Green trace: Switch node voltage, 5 V/div; Pink trace: Primary current, 500 mA/div

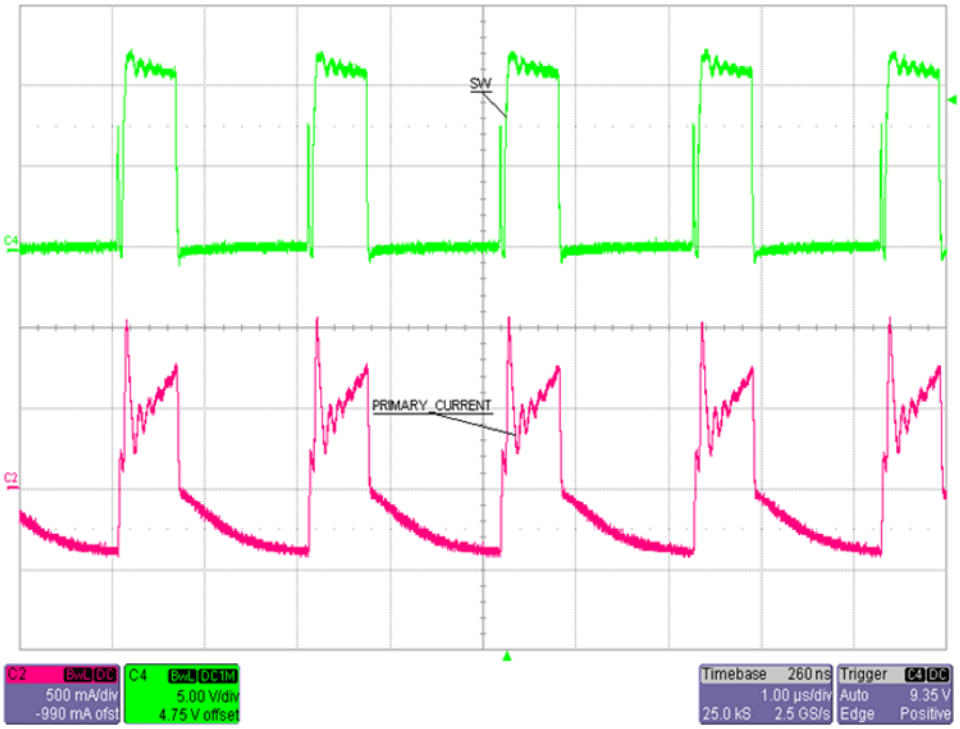


図 32. SW Node and Primary Current Waveform at V_{IN} = 12 V at Full Load

3.3.7 Rectifier and Secondary Current Waveforms

図 33 shows the voltage across diode D1 (V-D1) and secondary current for the 12-V input at full load.

注: Blue trace: Diode (D1) voltage, 50 V/div; Pink trace: Secondary current, 100 mA/div

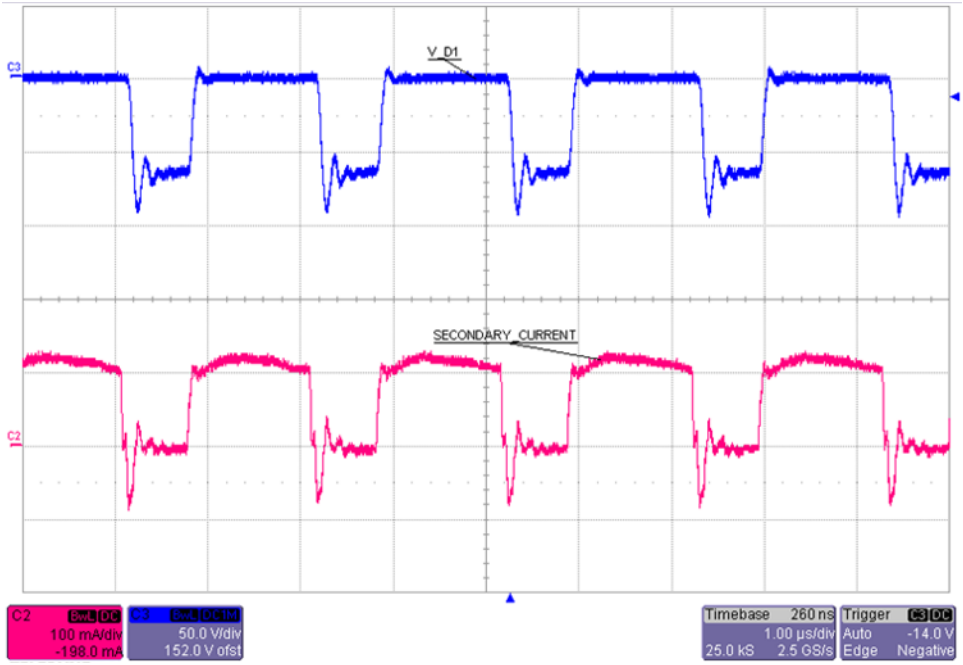


図 33. Voltage Across Diode D1 and Secondary Current at 12-V Input at Full Load

3.3.8 Start-Up and Shutdown (Relative to V_{IN})

図 34 shows the start-up waveforms relative to input of the step-down converter. The output is observed only when the input signal crosses the set UVLO threshold. 図 35 shows the shutdown waveforms relative to input. The output decays down when the input signal falls below the set UVLO threshold.

注: Red trace: Input voltage, VCC/12 V; Blue trace: Non-isolated voltage, 3.3 V, 1 V/div

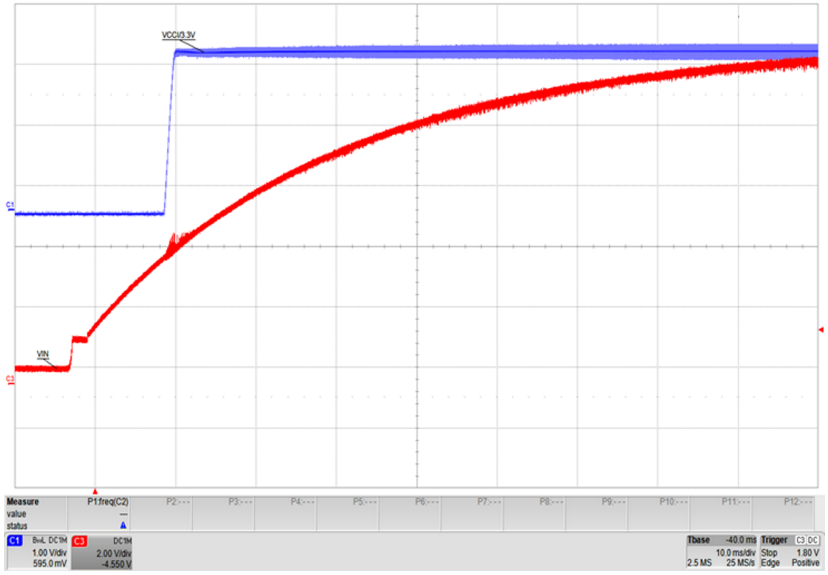


図 34. Start-up Relative to V_{IN}

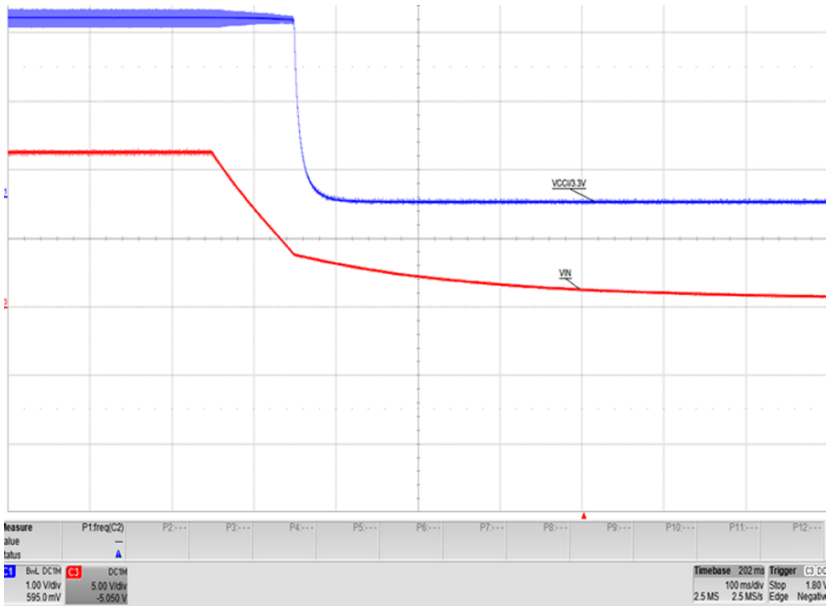


図 35. Shutdown Relative to V_{IN}

3.3.9 Output Ripple

図 36 shows the ripple on the 3.3-V non-isolated output at a 12-V input at full load. A ripple voltage of 70 mVpk-pk is seen.

図 37 shows the ripple on the 23-V isolated output at a 12-V input at full load. A ripple voltage of 118 mVpk-pk is seen

注: Yellow trace: Output ripple, 100 mV/div; Green trace: Switching node, 10 V/div; Blue trace: Diode (D1) voltage, 100 V/div

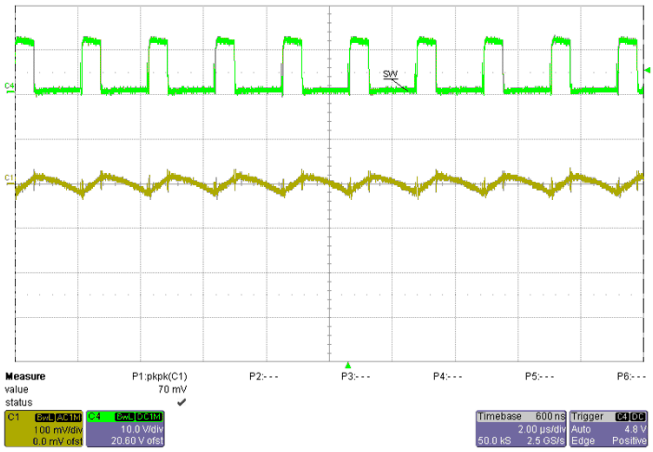


図 36. Non-Isolated Output 3.3 V (Ripple)

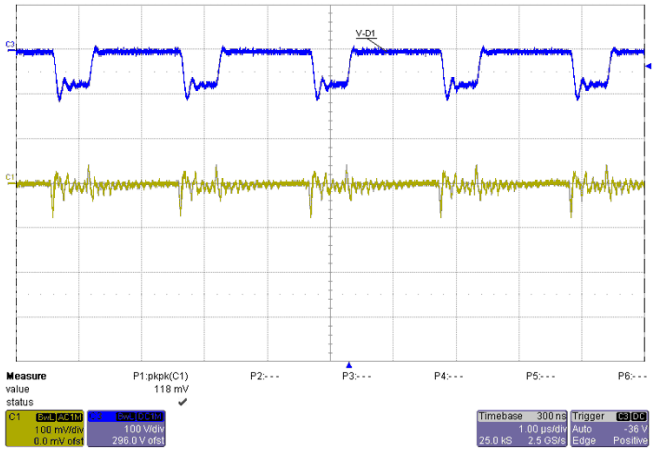


図 37. Isolated Output 23 V (Ripple)

3.3.10 Overcurrent and Short-Circuit Protection Test

The LM25017 device contains an intelligent current limit off-timer. If the current in the buck switch exceeds the current limit threshold, the present cycle is immediately terminated, and a non-resetable off-timer is initiated.

図 38 and 図 39 show the waveforms under short-circuit condition.

注: Yellow trace: 3.3-V non-isolated rail, 5 V/div; Blue trace: 23-V isolated rail, 20 V/div; Pink trace: Output current, 200 mA/div; Green trace: Switching node, 5 V/div.

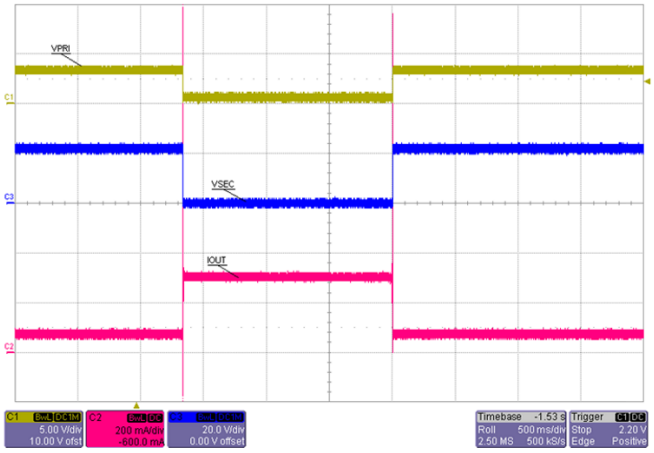


図 38. Short-Circuit Application and Recovery at 12 V_{IN} (Applied From Full Load, Recovered Into Full Load)

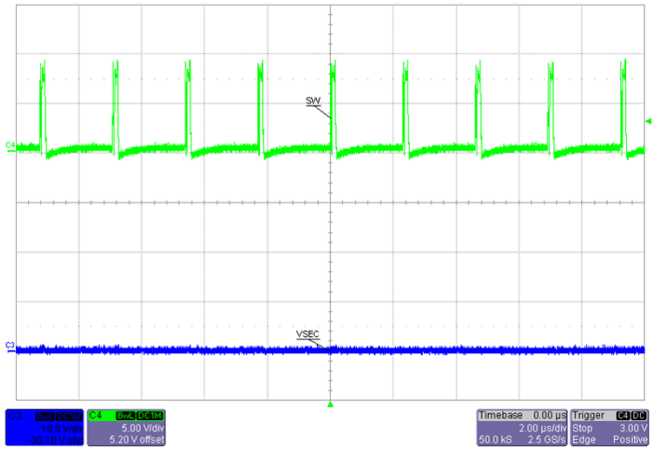


図 39. Switching Node Waveform During Short-Circuit Condition

図 40 shows the waveforms under overcurrent conditions.

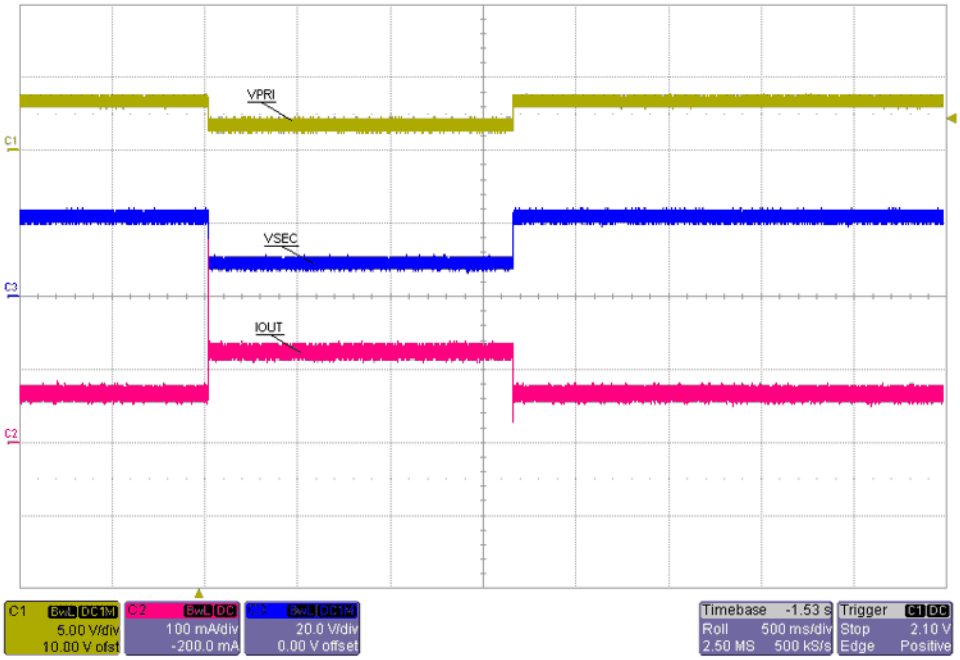


図 40. Overcurrent Application and Recovery at 12 V_{IN} (Applied From Full Load, Recovered Into Full Load)

3.3.11 Performance Data

3.3.11.1 Efficiency and Regulation at 12-V Input

表 7 shows the efficiency and regulation performance data at a 12-V input.

表 7. Efficiency and Regulation at 12-V Input

LOAD (%)	I_{IN} (mA)	V_{OUT1} (V)	V_{OUT2} (V)	I_{OUT2} (mA)	P_{IN} (W)	P_{OUT} (W)	EFFICIENCY (%)	REGULATION V_{OUT1} (%)	REGULATION V_{OUT2} (%)
0	18.452	3.3497	24.630	0.0268	0.2214	0.0007	0.3162	–0.5256	11.2818
10	29.356	3.3473	23.367	5.8950	0.3523	0.1377	39.0860	–0.5969	5.5754
20	43.659	3.3479	22.924	12.8330	0.5239	0.2942	56.1558	–0.5791	3.5739
30	61.349	3.3527	22.638	20.7700	0.7362	0.4702	63.8685	–0.4365	2.2817
40	78.984	3.3591	22.462	28.2500	0.9478	0.6346	66.9551	–0.2465	1.4865
50	92.365	3.3620	22.329	34.0530	1.1084	0.7604	68.6034	–0.1604	0.8856
60	107.967	3.3656	22.184	40.6520	1.2956	0.9018	69.6048	–0.0535	0.2304
70	121.610	3.3698	22.063	48.3580	1.4593	1.0669	73.1104	0.0713	–0.3163
80	136.610	3.3732	21.937	55.3210	1.6393	1.2136	74.0316	0.1722	–0.8856
90	152.960	3.3765	21.811	62.9180	1.8355	1.3723	74.7644	0.2702	–1.4548
100	169.360	3.3803	21.640	70.5300	2.0323	1.5263	75.1021	0.3831	–2.2274
105	173.880	3.3816	21.580	72.6240	2.0866	1.5672	75.1078	0.4217	–2.4986
140	240.750	3.4042	20.502	103.5120	2.8890	2.1222	73.4579	1.0928	–7.3691

3.3.11.2 Efficiency and Regulation at 10-V Input

表 8 shows the efficiency and regulation performance data at a 10-V input.

表 8. Efficiency and Regulation at 10-V Input

LOAD (%)	I_{IN} (mA)	V_{OUT1} (V)	V_{OUT2} (V)	I_{OUT2} (mA)	P_{IN} (W)	P_{OUT} (W)	EFFICIENCY (%)	REGULATION V_{OUT1} (%)	REGULATION V_{OUT2} (%)
0	17.247	3.3433	24.221	0.02640	0.1725	0.0064	3.7075	–0.7382	10.6607
10	30.278	3.3424	23.171	5.8458	0.3028	0.1355	44.7365	–0.7649	5.8635
20	47.594	3.3448	22.781	12.7550	0.4759	0.2906	61.0522	–0.6936	4.0816
30	68.935	3.3511	22.506	20.6510	0.6894	0.4648	67.4217	–0.5066	2.8252
40	89.568	3.3568	22.309	28.0640	0.8957	0.6261	69.8999	–0.3374	1.9252
50	110.088	3.3617	22.089	35.3010	1.1009	0.7798	70.8310	–0.1919	0.9200
60	119.920	3.3659	22.028	40.8030	1.1992	0.8988	74.9507	–0.0672	0.6413
70	138.900	3.3701	21.866	47.9380	1.3890	1.0482	75.4652	0.0575	–0.0988
80	156.540	3.3742	21.702	54.7330	1.5654	1.1878	75.8794	0.1793	–0.8481
90	175.390	3.3790	21.483	61.9730	1.7175	1.3314	77.5159	0.3218	–1.8486
100	198.690	3.3865	21.118	71.0830	1.9869	1.5011	75.5514	0.5444	–3.5163
130	274.750	3.4118	19.864	100.2750	2.7475	1.9919	72.4973	1.2956	–9.2455
146	312.170	3.4234	19.205	114.1790	3.1217	2.1928	70.2440	1.6400	–12.2564

3.3.11.3 Efficiency and Regulation at 17-V Input

表 9 shows the efficiency and regulation performance data at a 17-V input.

表 9. Efficiency and Regulation at 17-V Input

LOAD (%)	I_{IN} (mA)	V_{OUT1} (V)	V_{OUT2} (V)	I_{OUT2} (mA)	P_{IN} (W)	P_{OUT} (W)	EFFICIENCY (%)	REGULATION V_{OUT1} (%)	REGULATION V_{OUT2} (%)
0	21.926	3.3603	25.621	0.0278	0.3727	0.0007	0.1911	–0.2749	14.6238
10	29.744	3.3549	23.821	6.0091	0.5056	0.1431	28.3088	–0.4351	6.5709
20	39.968	3.3538	23.249	13.0150	0.6795	0.3026	44.5335	–0.4678	4.0119
30	52.804	3.3554	22.906	21.0150	0.8977	0.4814	53.6245	–0.4203	2.4774
40	65.182	3.3598	22.671	28.5130	1.1081	0.6464	58.3360	–0.2897	1.4260
50	75.137	3.3665	22.538	34.3700	1.2773	0.7746	60.6446	–0.0909	0.8310
60	87.247	3.3699	22.368	41.7520	1.4832	0.9339	62.9658	0.0100	0.0705
70	98.930	3.3726	22.242	48.7500	1.6818	1.0843	64.4721	0.0901	–0.4932
80	110.459	3.3751	22.132	55.8100	1.8778	1.2352	65.7783	0.1643	–0.9854
90	119.830	3.3775	22.036	63.5690	2.0371	1.4008	68.7644	0.2356	–1.4148
100	131.590	3.3797	21.925	71.4650	2.2370	1.5669	70.0424	0.3009	–1.9114
107	134.890	3.3805	21.890	73.7200	2.2931	1.6137	70.3724	0.3246	–2.0680
130	167.050	3.3581	21.021	92.4610	2.8399	1.9436	68.4410	–0.3402	–5.9558

3.3.12 Performance Curves

3.3.12.1 Efficiency With Output Power

図 41 shows the efficiency curve of the Fly-Buck converter with output power variation.

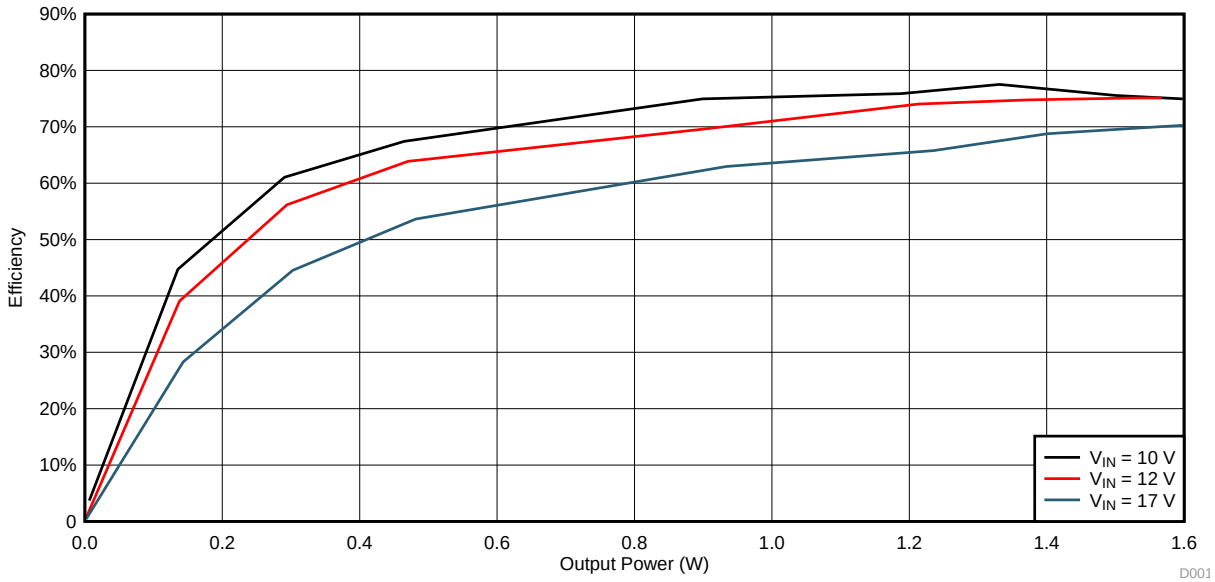


図 41. Efficiency versus Output Power

3.3.12.2 Regulation With Output Power

図 42 shows the regulation of the 3.3-V non-isolated output with output power variation.

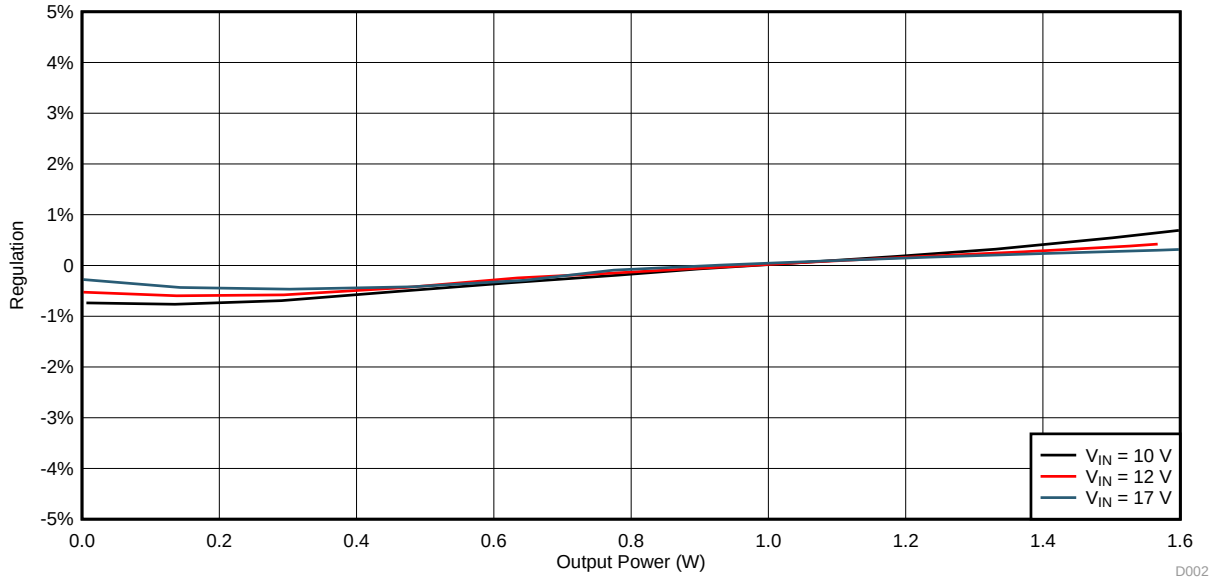


図 42. Non-Isolated Output 3.3-V Regulation With Output Power

図 43 shows the regulation of the 23-V isolated output with output power variation.

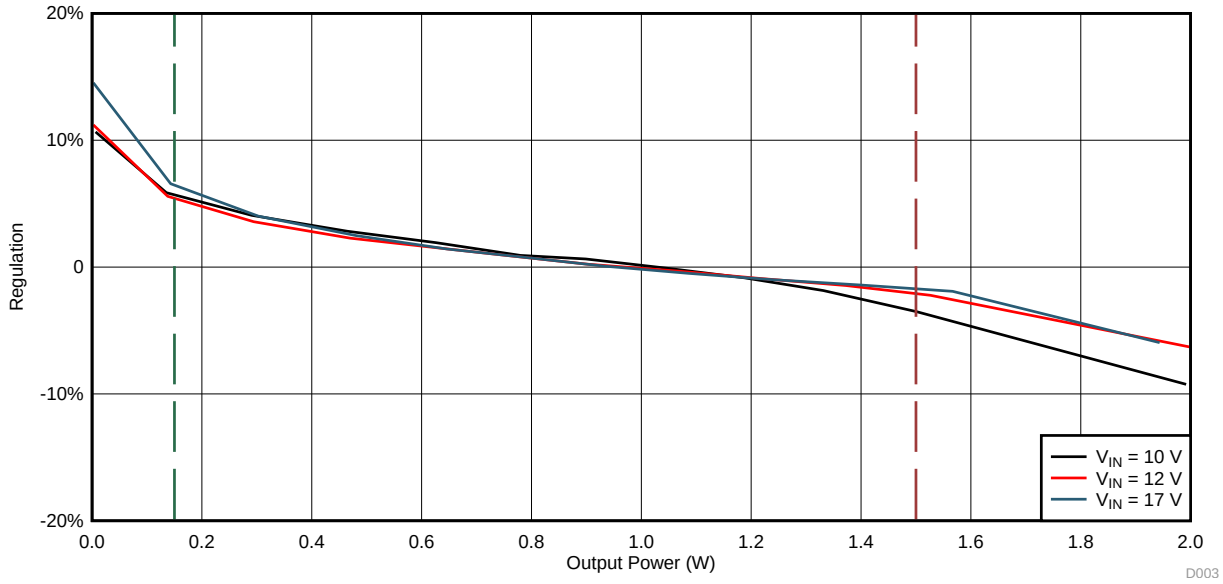


図 43. Isolated Output 23-V Regulation With Output Power

3.3.13 Thermal Measurements

図 44 and 図 45 show the thermal measurements taken at ambient temperature (23.1°C) with a 12-V input voltage, 56-nF load, and 20-kHz switching frequency after letting the board run for half an hour.

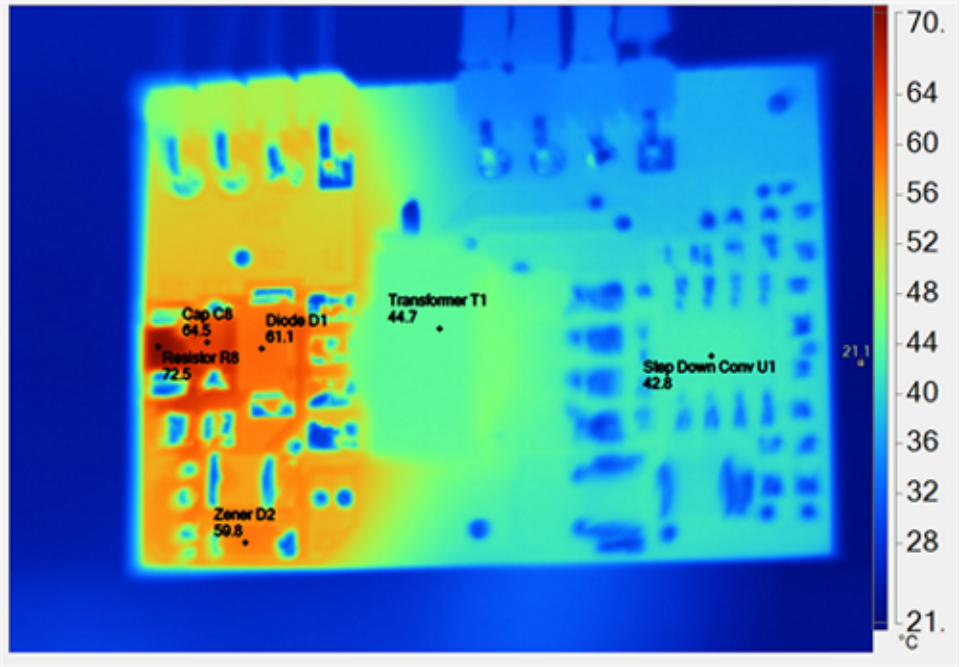


図 44. Thermal Measurements—Top View

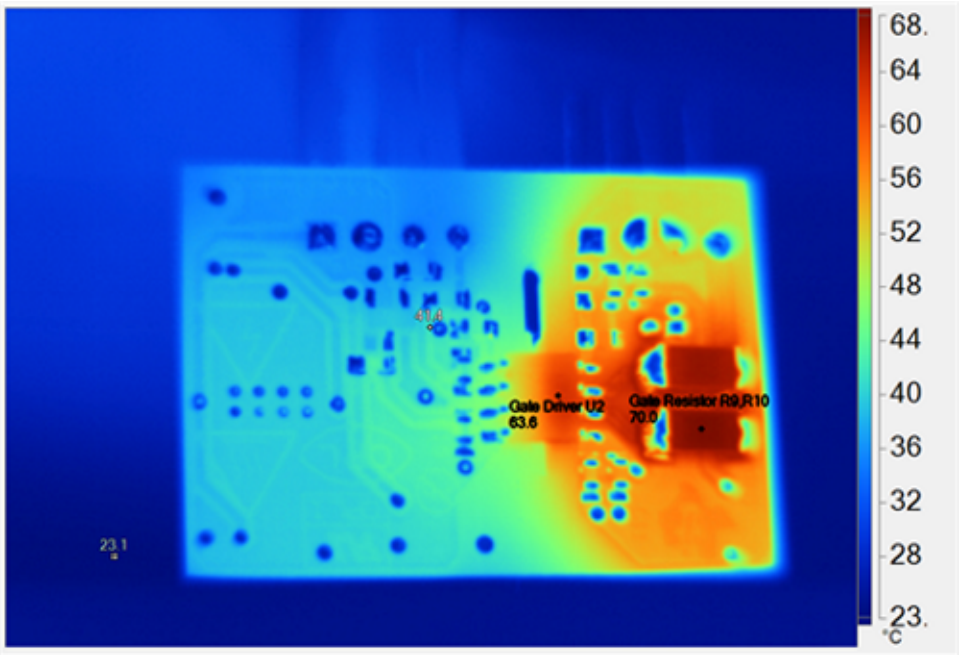


図 45. Thermal Measurements—Bottom View

表 10. Highlighted Image Markers for 図 44

NAME	TEMPERATURE
Gate driver	63.6°C
Transformer	44.7°C
Gate resistors	70.0°C
Zener diode	59.8°C
Snubber resistor	72.5°C
Buck converter IC	42.8°C

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01160.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01160.

4.3 PCB Layout Recommendations

Note that the design contains high voltages. The layout must be done with extreme care.

4.3.1 Fly-Buck Converter Stage Specific Guidelines

- The loop consisting of the input capacitor (C3), VIN pin, and GND pin carries switching currents. Therefore, the input capacitor should be placed close to the IC, directly across VIN and GND pins, and the connections to these two pins should be direct to minimize the loop area.
- Provide sufficient vias for the input capacitor and output capacitor.
- The SW node switches rapidly between VIN and GND every cycle and is therefore a possible source of noise. Minimize the SW node area. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Place the voltage feedback loop away from the high-voltage switching trace, and preferably have a ground shield.
- The trace of the VFB node should be as small as possible to avoid noise coupling.
- Place the bootstrap capacitor as close to the IC as possible, and minimize the connecting trace length and loop area.

4.3.2 Gate Driver Specific Guidelines

- Connect the low-ESR and low-ESL capacitors close to the UCC5320S between the VCC1 and GND1 pins and between the VCC2 and VEE2 pins to support high peak currents when turning on the external power transistor.
- A PCB cutout is recommended to ensure good isolation performance between the primary and secondary side of the UCC5320S. To do this, avoid placing any PCB traces or copper below the device.
- Confine the high peak currents that charge and discharge the transistor gates to a minimal physical area as this will decrease the loop inductance and minimize noise on the gate terminals of the transistors. To ensure this, connect the TIDA-01160 board with very short leads to the transistors.

A proper PCB layout can help dissipate heat from the devices to the PCB and minimize junction to board thermal impedance. See the placement and routing guidelines and layout example in the LM25017 and UCC5320 datasheets.

4.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-01160.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01160.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01160.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01160.

5 Related Documentation

1. Texas Instruments, *AN-2292 Designing an Isolated Buck (Fly-Buck) Converter*, Application Report (SNVA674)
2. Texas Instruments, *Pick the right turns ratio for a Fly-Buck converter*, Editorial Reprint (SLPY004)
3. Xiang Fang, Wei Liu, and Anoop Chadaga, *Product How-to: Fly-Buck adds well-regulated isolated outputs to a buck without optocouplers*, EDN Network (http://www.edn.com/design/power-management/4429791/2/Product-How-to--Fly-Buck-adds-well-regulated-isolated-outputs-to-a-buck-without-optocouplers-)
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5.1 商標

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