参考資料

TI Designs

広いAC/DC入力に対応したEMC準拠、絶縁、2チャネルのバイナリまたはデジタル入力モジュールのリファレンス・デザイン

TEXAS INSTRUMENTS

概要

このTI Designでは、ACまたはDCバイナリ入力モジュールの分解能を向上させる、コスト最適化されたアーキテクチャを紹介します。チャネルごとのコストを最適化するため、マイクロコントローラ・ユニット(MCU)は2つの入力チャネル間で共有されます(グループ絶縁)。ゲイン付きアンプにより広い入力範囲がカバーされ、MCUに統合された10ビットのアナログ/デジタル・コンバータ(ADC)により±3%以内の精度で測定が行われます。このアーキテクチャにより、たとえばオプトカプラをベースとするトポロジなどのように、入力電圧範囲に合わせて複数のバージョンのハードウェアを用意する必要はなくなります。デジタル・アイソレータを使用して、ADCコードや、入力の実効値をホスト・プロセッサへ通知します。このデザインは、IEC61000-4 Level 4に従いESD、EFT、サージのテスト済みです。

リソース

TIDA-00809	デザイン・フォルダ
MSP430G2332	プロダクト・フォルダ
SN6501	プロダクト・フォルダ
LM4041	プロダクト・フォルダ
LMV614	プロダクト・フォルダ
LMV551	プロダクト・フォルダ
ISO1541D	プロダクト・フォルダ
ISO7320C	プロダクト・フォルダ
ISO7820	プロダクト・フォルダ

TI E2E™ Community

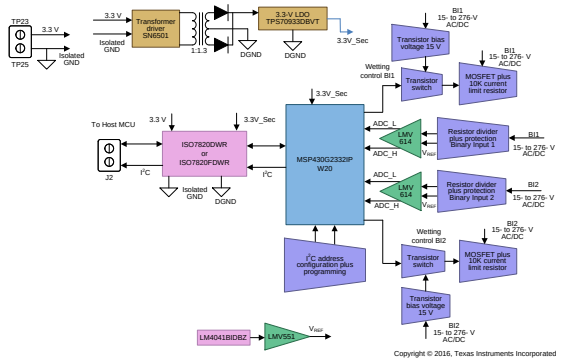
E2Eエキスパートに質問

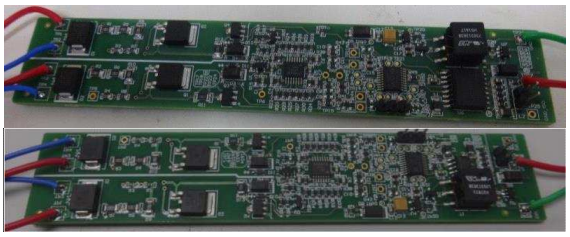
特長

- MSP430™ファミリのMCUをベースとした2チャネル低消費電力AC/DC電圧測定モジュール
- バイナリ・モジュールとホストMCUとの絶縁インターフェイス
- バイナリ・モジュールの設計は基本または強化型のデジタル・アイソレータを使用し、HIGHまたはLOWをデフォルト出力
- LMV614オペアンプをベースとしたゲイン段により測定精度が向上(x1およびx3.5)
- DCレベル・シフト入力用の安定した基準電圧をLM4041で生成し、LMV551でバッファリング
- 測定値±1V(プログラミング可能な分解能またはステップ・サイズ)の精度±3%以下
- 広い温度範囲にわたって入力電圧を正確に測定
- 1V未満の測定分解能
- 最大300V AC/DCの入力定格
- 300kΩ超のバイナリ入力インピーダンス
- 276V入力において消費電流1mA未満
- 事前コンプライアンス用に、IEC61000-4規格の要件に準拠しESD、EFT、サージをテスト済み
- PCBの幅1インチ以下

アプリケーション

- マルチファンクションの保護リレー
- サブステーション・ベイ・コントローラとバッテリ監視
- RTU/FTU/DTU/FRTU
- マージング・ユニット
- PLCデジタル入力モジュール





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1 System Overview

1.1 System Description

1.1.1 Introduction to IED and Subsystems in Grid Applications

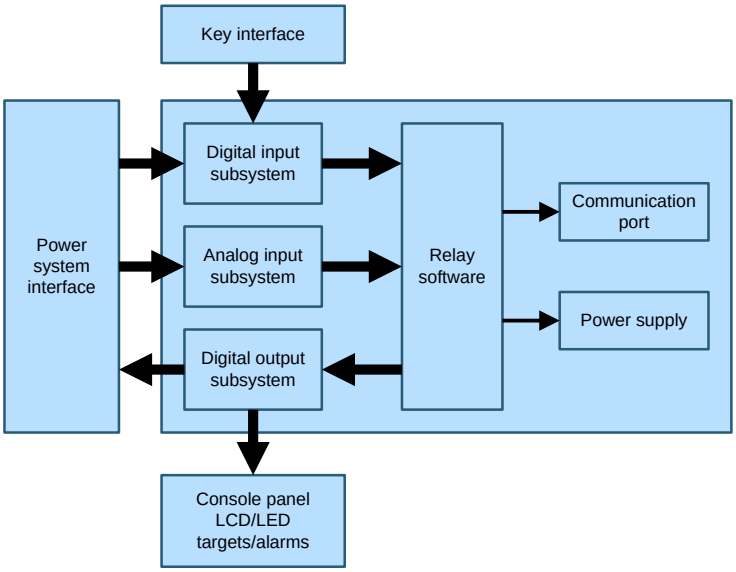


図 1. Generic Block Diagram of a Protection Relay

The protection relay, intelligent electronic device (IED), or substation controllers used in grid applications have the following generic subsystems. The subsystems are based on the functionality and are as follows:

- CPU or DSP module
  - This module handles all protection functions and logic. Additionally, the HMI and communication functions are also handled by this module.
- Power supply
  - Nominal auxiliary voltage: 24-V DC, 48- to 60-V DC, 110- to 125-V DC, 220-V DC, and 230-V AC,

50 or 60 Hz, ± 20%, and 40-W max. admissible consumption

  - Stored energy for up to 50 ms power supply interruption
- AC measurement inputs
  - Nominal frequency (FNOM): 50 or 60 Hz
- CT measurements inputs
  - Nominal current: 1 or 5 A (IN)
- VT measurement inputs
  - Nominal voltage: 57.7 to 500 V
  - Maximum measurable voltage: 577 V_{RMS}

- DC analog input range (independently configurable):
  - ±1.25, ±2.5, ±5, and ±10 V
  - ±1, ±5, ±10, and ±20 mA
  - 0 to 1, 0 to 5, 0 to 10, 0 to 20, and 4 to 20 mA
- DC analog output range (independently configurable):
  - ±5, ±10, ±20 mA, and 4 to 20 mA
- Digital inputs
  - Nominal voltage: 24-V DC, 48- to 60-V DC, 110- to 125-V DC/AC and 220-V DC/AC, ±20% or multi-voltage (24 to 250-V DC/AC)
  - Power consumption per input: 2 to 6 mA, maximum power dissipation is 0.45 W ±20% per input or short peak-current (> 25 mA)
  - Groups of 4, 8, 12, 16, or 32
- Digital output relays
  - Continuous current: 5 A
- Control output relays
  - Continuous current: 5 A
- Time synchronization
  - by an IRIG–B GPS clock (through the IRIG-B input)
  - by an Ethernet SNTP server
  - by a time telegram message issued by remote Scada (DNP3.0, IEC 60870-5-101 or IEC 60870-5-104)
- Communication capabilities
  - Ethernet communication
    - 10/100BASE-TX, auto-crossing or 100BASE-FX
    - Embedded Ethernet switch module with up to six ports (permitting a compact connection of various devices or I/O extensions)
  - Serial communication
    - Up to two SCADA or four IED links per device
    - SCADA protocol can be switched between DNP3.0, IEC 60870-5-101 and MODBUS
    - IED Protocol can be switched between DNP3.0, IEC 60870-5-103, MODBUS and IEC 60870-5-101

This TI Design focuses on designing a digital input module to measure a wide AC/DC input with programmable threshold with digital isolators.

1.1.2 Binary or Digital Inputs

The inputs to the protection relay or substation controllers are called under different names:

- Binary input
- Digital input
- Control input

- Indication input

These names are based on the function performed. This design guide will refer to these inputs as binary inputs. Binary inputs have wide applications. The binary input module specifications differ with OEMs. The binary inputs are designed as modules and, based on the application, one or more modules are used. The following subsections detail some of these applications, functionalities, and specifications. These inputs have galvanic isolation from internal circuits; generally, optocouplers are used for isolation. The number of binary inputs per module can vary as 4, 8, 16, or 32. *The binary inputs are organized in groups (depending upon application) with a common wire. In some of the applications, the inputs are channel isolated.*

1.1.2.1 Binary Input Applications

Some grid applications use binary inputs for the following functionalities:

- Substation battery monitoring
- Bay or substation interlocking
- Breaker status indication
- General interrogations
- LED test
- Diagnostics (self-test)
- Fault indication (alarm)
- Configuration change (operated with new settings to perform different functionality)

1.1.2.2 Binary Input Specifications

Key specifications include:

- Input voltage range
- Threshold for guaranteed operation
- Response or reset time (software provides de-bounce time)
- Power consumption, energized

General specifications include:

- Inputs are jumper selectable for low range (nominal system voltages of up to 100 V) or high range (from 100 to 300 V)
- Tolerance: ±10%
- Common input voltage ranges:
  - 24-V DC
  - 48-V DC
  - 110-V AC/DC
  - 230-V AC/DC
- Frequency: 50 or 60 Hz
- Contacts per common return: Four or more
- Recognition (processing of the inputs) time: ≥ 20 ms
- Inputs protected against continuous overload up to 300-V AC/DC

- All I/O terminals protected with internal transient limiting devices
- Continuous current draw: < 5 mA
- Auto-burnish impulse current: 20 to 50 mA
- Duration of auto-burnish impulse: 25 to 50 ms

1.1.2.3 Wetting or Auto Burnishing

The binary inputs sense a change of the state of the external device. When these external devices are in harsh industrial environments (either outdoor or indoor), their contacts can be exposed to various types of contamination. Normally, there is a thin film of insulating sulfidation, oxidation, or contaminates on the surface of the contacts, sometimes making it difficult or impossible to detect a change of the state. This film must be removed to establish circuit continuity; an impulse of higher than normal current can accomplish this.

The contact inputs with auto-burnish create a high current impulse when the threshold is reached to burn off this oxidation layer as maintenance to the contacts. Afterwards, the contact input current is reduced to a steady-state current. Contact inputs with auto burnishing allow currents up to 50 mA at the first instance when the change of state was sensed. Then, within 25 to 50 ms, this current is slowly reduced to 5 mA. The 50-mA peak current burns any film on the contacts, allowing for proper sensing of state changes.

1.1.2.4 Miscellaneous Features

Filters prevent the input signal from being detected erroneously. The following types of input filters can be used:

- The hardware input filter is used to suppress contact bounce (1 to 64 ms).
- Change-of-state delay is used to suppress short signal interruptions.
- Chatter blocking is used to suppress huge bursts of indications in case of defective battery or intermediate relays.

1.1.3 Isolation

表 1. Key Methods of Isolation

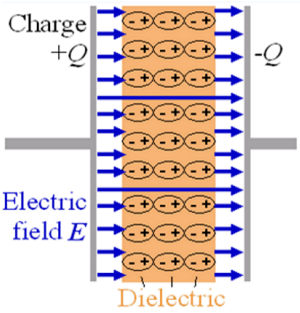
	SiO2: ISO72x; Typical BV is V_{PEAK}/µm • Inorganic • Highly stable (over temperature, moisture, time), high quality • Used extensively and for a long time as dielectric in semiconductor (low defunct rates) • Deposited in a controlled semiconductor process

表 1. Key Methods of Isolation (continued)

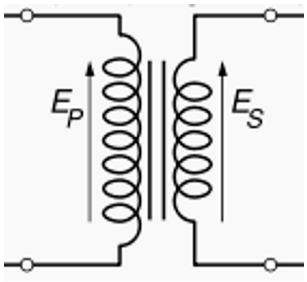
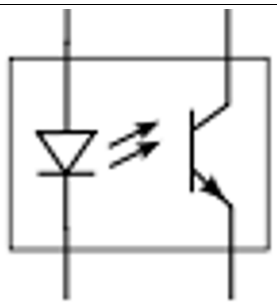
	Polymide: ADI transformer core; Typical BV is 250 V_{PEAK}/µm • Organic • Retains moisture — affects lifetime especially at high voltages • Used in semiconductor mainly for stress relief and now as isolation barrier
	Epoxy: Optocouplers; Typical BV is 50 V_{PEAK}/µm • Uses filler materials • Leaky (higher partial discharge) • Applied at packaging as mold compound • Voids and anomalies are common

表 2. Isolation Solutions Reliability

PARAMETER	OPTO	MAGNETIC	CAPACITIVE
Signaling rate (Mbps)	50	150	150
Propagation delay time (ns)	20	32	12
Pulse width distortion (ns)	2	2	1.5
Channel-to-channel skew (ns)	16	2	1.6
Part-to-part skew (ns)	20	10	2
ESD on all pins (kV)	±2	±2	±4
CM transient immunity (kV/µs)	20	25	25
Temperature (°C)	–45 to 125	–40 to 125	–55 to 125
MTTF at 125°C, 90% confidence (years)	8	1746	2255
FIT at 125°C, 90% confidence	14391	65	50
Magnetic immunity at 1 kHz (Wb/m^2)	—	10^2	10^8
Radiated electromagnetic-field immunity IEC61000-4-3 (80 to 1000 MHz) MIL-STD 461E RS103 (30 to 1000 MHz)	 — —	 Fails Fails	 Compiles Compiles
High-voltage lifetime expectancy (years)	< 5	< 10	> 28

1.1.4 EMC—Transient Overvoltage Stress

In industrial applications, lightning strikes, power source fluctuations, inductive switching, and electrostatic discharge (ESD) can cause damage to binary inputs by generating large transient voltages. The following ESD and surge protection specifications are relevant to binary input applications:

- IEC 61000-4-2 ESD
- IEC 61000-4-4 EFT
- IEC 61000-4-5 Surge

The level of protection can be further enhanced when using external clamping devices such as TVS diodes. The transients are clamped instantaneously (< 1 ns), and the damaging current is diverted away from the protected device.

1.1.5 TI Design Advantages

Some of the advantage of the AC/DC binary input module is as follows:

- Provides isolation using digital isolator with basic or reinforced isolation and increased reliability
- Costs optimized solution with option for expansion up to four digital inputs
- Allows for measurement of wide AC/DC input voltage
- Uses MCU to allow flexibility in terms of input voltage processing, measurement accuracy and control of wetting current
- Reduces measurement error caused due to bridge rectifier at the input (no bridge rectifier used)
- Improves voltage input measurement accuracy by using multiple gain stages
- Provides provision for programmable threshold on the host side

1.2 Key System Specifications

The AC/DC binary module measures the input voltage in terms of ADC counts. To ensure wide input AC/DC voltages are measured within the required accuracy, two gain stages have been used for each input: high gain and low gain. ADC counts after subtracting the DC offset is averaged for 10 or 30 ms. ADC counts for each channel (high and low) are communicated to the host. The host converts the ADC count into voltage for further processing. The conversion factor changes for DC and AC voltages. The conversion factor also changes for high gain and low gain.

表 3. AC/DC Binary Input—Electrical Specifications

SERIAL NUMBER	PARAMETERS	DESCRIPTION	COMMENTS
1	Number of binary inputs	2	Both inputs share common ground
2	Binary input voltage range	15-V to 264-V AC/DC	Maximum permissible voltage input is ≤ 300-V AC/DC
3	Signal frequency	DC or AC (50 and 60 Hz)	
4	Measurement resolution	<1-V steps for values between 24-V to 264-V AC/DC	Binary module communicates measured voltage in terms of ADC counts to the host
5	Gain amplifier	Two gains , ×1 , ×3.5	
6	Measurement accuracy	±3% of measured value ±1 V	
7	Input impedance	≥ 300 kΩ	
8	Current drain	< 1 mA	
9	Response time	≥ 10 ms for DC	Measurement averaged for 10 ms
10	Binary input wetting resistance	≥ 2.5 kΩ	Default: Wetting is off Wetting control PWM is based on Nominal voltage (24 V, 110 V, 230 V)
11	Isolator type	1. I^2C interface with basic isolation 2. Digital isolators with basic isolation 3. Digital isolation with reinforced isolation	Isolated voltage of 3.3-V generated on board 3.3-V input from the host is applied
12	Reference temperature	25°C	Reference temperature
13	Isolation	Group isolated	Isolation
14	Electrical isolation level	5700-V_{RMS} isolation for 1 minute per UL 1577 for reinforced isolation	Electrical isolation level
15	Protection against surge, ESD, EFT (EMC requirements)	ESD: 8 kV , contact Surge: 4 kV , 42-Ω differential mode EFT: 2 kV	Protection against surge, ESD, EFT (EMC requirements)

1.3 Block Diagram

This TI Design provides an innovative and cost optimized method to measure the digital input accurately over wide temperature and input using the MSP430 family of MCUs and high reliability digital isolators. Digital isolators are used to provide the required isolation between the digital input processing circuit and the host MCU. The design provides the following options:

1. Interface to the host interface using digital isolators with basic isolation (BI)
2. Interface to the host interface using digital isolators with reinforced isolation (RI)

The DC or AC inputs are applied across potential divider and the divider output is amplified by ×1 or ×3.5 gain, and the MCU converts the analog input to 10-bit digital value that is used for computing the RMS voltage. The AC input is DC level shifted by VCC/2 for the SAR ADC internal to the MCU using an external reference and buffer. The outputs are communicated to the host through digital isolator. The isolated power supply required for the binary module operation is generated onboard using the SN6501 transformer driver. The transformer used in this design is a larger footprint transformer with isolation rating up to 6 kV_{RMS}.

This TI Design has the following functional blocks:

- Potential divider: Divides the input voltage to within the ADC range for measurement including the gain stage
- Operational amplifier (op amp) gain: Covers the wide AC/DC input over wide range, two gain stages are used. A higher gain amplifier stage is used to measure lower input voltages, and for higher input voltage, a lower gain amplifier is used.
- Wetting current control: MOSFET-based wetting current control circuit with 2.5K impedance is used. The wetting circuit makes use of the resistors short time over voltage with stand capability for testing.
- MCU: Measures the binary input, controls the wetting current, and communicates the measured input value to the host processor
- Digital isolator: Provides the required isolation between the binary module and the host processor
- Power supply: Binary module is powered by 3.3 V from the host side. Isolated power for the binary module is generated

The TI Design has two boards:

- One board has the footprint to mount the smaller package basic isolation digital isolators, named as BI (board with basic insulation isolator option)
- The other board has footprint provision to mount reinforced isolation digital isolators, named as RI (board with reinforced insulation isolator option)

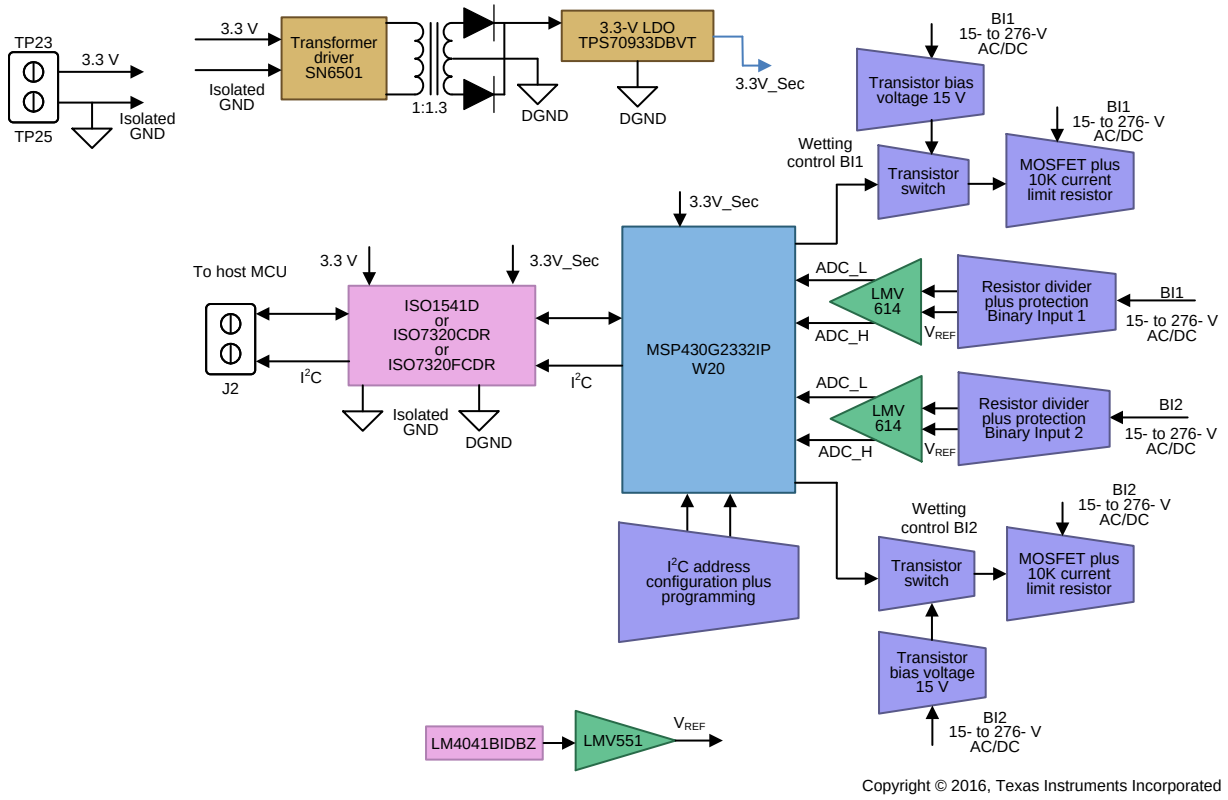


図 2. Binary Module With Digital Isolator (BI)

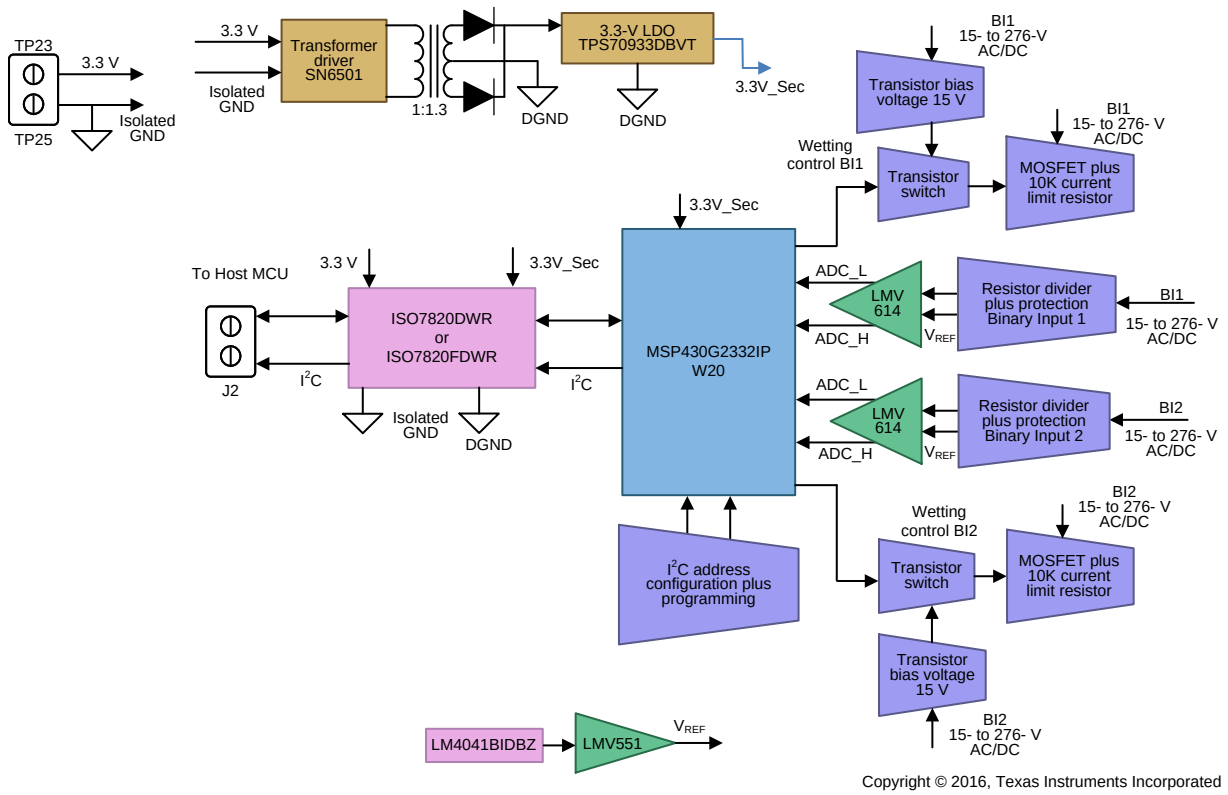


図 3. Binary Module With Digital Isolator (RI)

1.4 Highlighted Products

1.4.1 MCU With Internal 10-Bit SAR ADC

The MSP430G2332IPW2MSP430 ultra-low-power microcontroller has been considered in this TI Design. The MCU has an internal 10-bit ADC.

Other features include:

- Low supply voltage range: 1.8 to 3.6 V
- Ultra-low-power consumption
  - Active mode: 220 μA at 1 MHz, 2.2 V
- Internal very-low-power low-frequency (LF) oscillator
- One 16-bit Timer_A with three capture/compare registers

1.4.2 Digital Isolator

Digital isolators are used to provide the required isolation between the binary module and the host MCU. Digital isolators with different isolation options (basic or reinforced) have been tested on the binary module.

The ISO1541D provides basic isolation. The ISO1541 has a bidirectional data and a unidirectional clock channel. The ISO1541 is useful in applications that have a single master. The ISO7320 has two channels in the same direction and provides basic isolation. The ISO7320FC default output is "low" and the ISO7320C default output is "high".

The ISO7820 has two channels in the same direction and provides reinforced isolation. The default output is high for the ISO7820 and low for the ISO7820F and can be selected based on the application.

Select the isolator depending on the isolation requirements and the EMC levels.

1.4.3 Isolated Power Supply

The isolated power for the MCU, digital isolator, and the signal conditioning circuit used for sensing the binary inputs are generated using a push-pull driver for isolated power supplies, the SN6501DBV. The transformer used for this application is the 750313638. The transformer package is selected to have an isolation voltage of > 5 kV. Choosing a bigger transformer package facilitates easy migration to reinforced isolators. Zener diode PTZTE253.9B is used for protecting the power supply against overvoltage and ESD. The isolated power supply operates with a single 3.3-V input. The host interface provides the required power supply for the binary module operation. An LDO TPS70933DBVT is used to improve the ADC dynamic range and accuracy of the output supply voltage.

1.4.4 Input Voltage Divider, Signal Conditioning, and Protection

- Input protection: TVS SMCJ400CA is used for protecting binary input module against overvoltage and transients. Package selection is critical to ensure low leakage with temperature variation.
- Resistor divider: The AC/DC binary input voltage applied is divided by a resistor divider, which presents a constant resistance to the binary input. Multiple resistors are used to ensure the resistors withstand the maximum input voltage reliably. The output of the resistor divider is measured by the ADC, and the output voltage range is within the ADC measurement range at maximum input. A Zener diode PTZTE255.1B is used to protect the electronic circuit from overvoltage.
- Reference: For measuring AC/DC inputs with internal ADC, the input is level shifted by

ADC_reference/2. The 1.65-V DC reference is generated using the LM4041. The LMV551 low-power op amp is used as a buffer for the reference output.

- Gain: To measure wide input AC/DC voltage accurately, an amplifier gain stage is provided. The gain stages are ×1 and ×3.5. These gains are chosen to cover input range of 15 to 276 V. The LMV614 amplifier stage is used.

1.4.5 Wetting Current Control

1.4.5.1 Transistor Drive for MOSFET Gate Driver

A transistor is used to drive the MOSFET that controls the wetting current. The bias voltage of 15 V max for the MOSFET operation is generated from the binary input using a Zener regulator. The bias current for the Zener must be in μA and take care when selecting the Zener. Voltage Vz versus Iz characteristics is critical.

1.4.5.2 Wetting Current Limiting Resistor and MOSFET

Four resistors, 10 kΩ each connected in parallel, are used as current limit for wetting current. A D-PAK MOSFET with a 600-V rating AOD2N60A is used that ensures reliability of the MOSFET. The short time overload capability of the resistor is being used and take care to not test the wetting current for tests > 100 ms (typically 50 ms).

2 System Design and Component Selection

2.1 MCU With Internal ADC

The binary input modules are cost sensitive, and to ensure the overall solution cost is optimal, an MCU with an internal ADC has been selected. The internal ADC is a 10-bit SAR ADC.

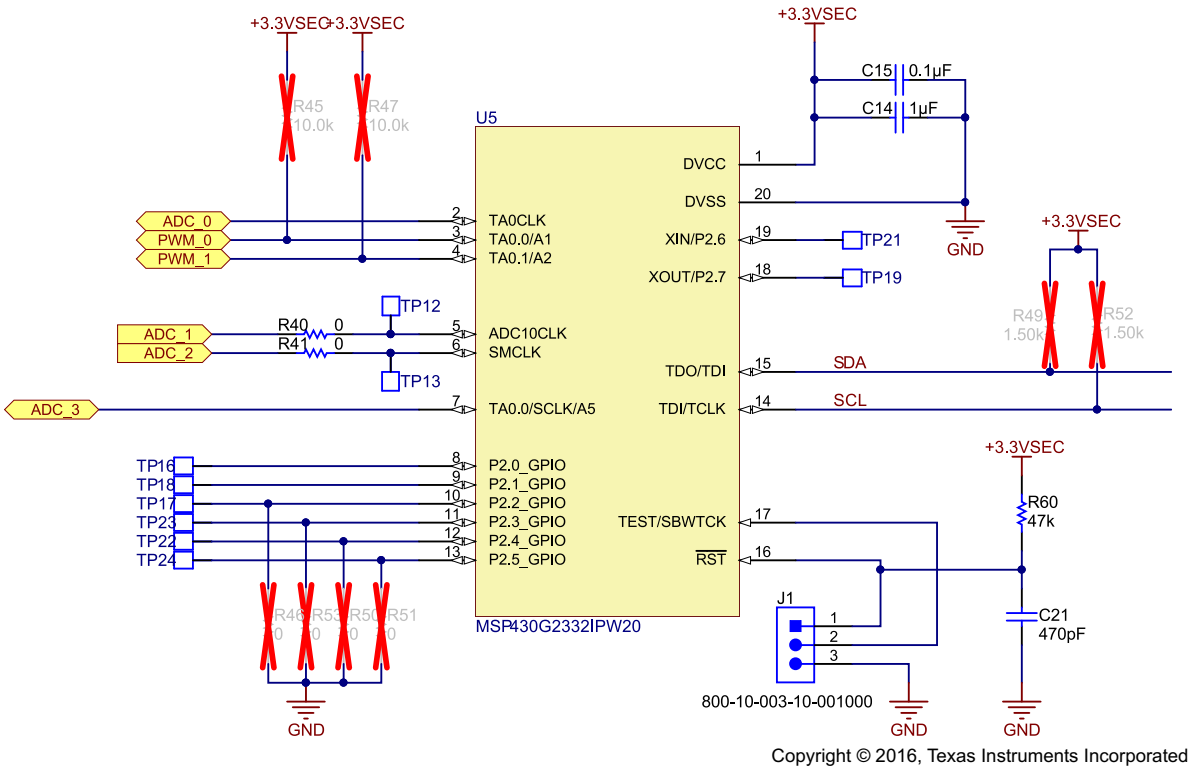


図 4. MCU Functionality Configuration

Texas Instruments' MSP430 family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. Combined with five low-power modes, the architecture is optimized to achieve an extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 µs.

The MCU considered is the MSP430G2332IPW20. The MSP430G2332IPW20 is an ultra-low-power mixed signal microcontroller with a built-in 16-bit timer. The device has up to 16 I/O capacitive-touch enabled pins and built-in communication capability using the universal serial communication interface. The MSP430G2332IPW20 has a 10-bit ADC.

Features:

- Low supply voltage range: 1.8 to 3.6 V
- Ultra-low power consumption
  - Active mode: 220 µA at 1 MHz, 2.2 V
  - Standby mode: 0.5 µA
  - Off mode (RAM retention): 0.1 µA

- Five power-saving modes
- Ultra-fast wake-up from standby mode in less than 1 μs
- 16-bit RISC architecture, 62.5-ns instruction cycle time

- Basic clock module configurations
  - Internal frequencies up to 16 MHz with four calibrated frequencies
  - Internal very-low-power LF oscillator
  - 32-kHz crystal
  - External digital clock source
- One 16-bit Timer_A with three capture/compare registers
- Universal serial interface (USI) supporting SPI and I2C
- 10-bit 200-ksps ADC with internal reference, sample-and-hold, and Autoscan (MSP430G2x32 only)
- Brownout detector
- Serial onboard programming, no external programming voltage needed, programmable code protection by security fuse
- On-chip emulation logic with Spy-Bi-Wire interface
- Package TSSOP: 20-pin

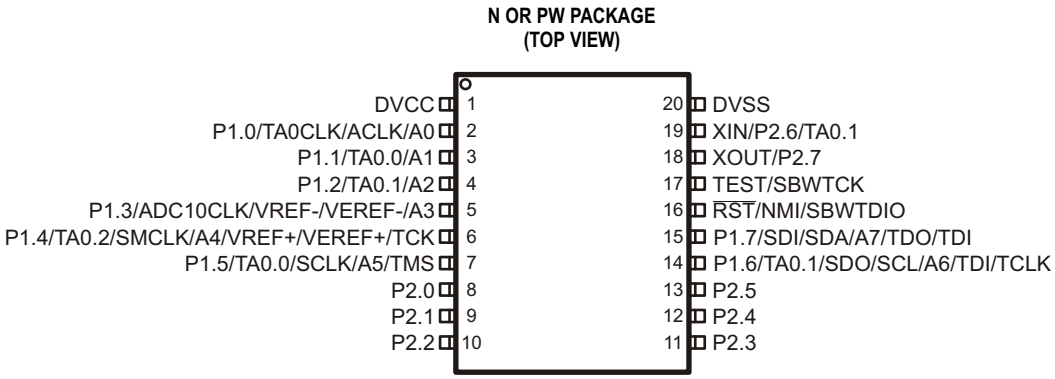


図 5. MCU Pinout Description

2.1.1 MCU Resources

表 4. MCU RAM and Flash Size

PIN NUMBER	DESCRIPTION	SIZE
1	Flash	4 KB
2	RAM	256 bytes
3	ADC10	8 channels
4	Package and pin count	20-TSSOP

2.1.2 MCU Configuration

表 5. MCU Pin Configuration for the AC/DC Binary Module

PIN NUMBER	PIN FUNCTION	CONFIGURATION
1	DVCC	3.3 V_{SEC}
2	A0	ADC_0 (Binary Input1—low gain)
3	TA0.0	PWM_0 (Control of Binary Input1 wetting current)
4	TA0.1	PWM_1 (Control of Binary Input2 wetting current)
5	A3	ADC_1 (Binary Input1—high gain)
6	A4	ADC_2 (Binary Input2—high gain)
7	A5	ADC_3 (Binary Input2—low gain)
8	P2.0	Not used—configured as output
9	P2.1	Not used—configured as output
10	P2.2	Can be used to set I^2C address—configured as output
11	P2.3	Can be used to set I^2C address—configured as output
12	P2.4	Can be used to set I^2C address—configured as output
13	P2.5	Can be used to set I^2C address—configured as output
14	SCL	I^2C clock
15	SDA	I^2C data
16	/RST	Programming
17	SBWTCK	Programming
18	P2.7	Not used—configured as output
19	P2.6	Not used—configured as output
20	DVSS	GND

2.1.3 ADC Features

The ADC used is a 10-bit, 8-channel ADC with Autoscan and DMA capabilities.

表 6. 10-Bit ADC, Timing Parameters (MSP430G2x32 Only)(1)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$	ADC input clock frequency	For specified performance of ADC10 linearity parameters	ADC10SR = 0	3 V	0.45		6.3	MHz
			ADC10SR = 1		0.45		1.5	
$f_{ADC10OSC}$	ADC10 built-in oscillator frequency	ADC10DIVx = 0, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	ADC10 built-in oscillator, ADC10SSELx = 0, $f_{ADC10CLK} = f_{ADC10OSC}$		3 V	2.06		3.51	µs
		$f_{ADC10CLK}$ from ACLK, MCLK, or SMCLK: ADC10SSELx ≠ 0			13 × ADC10DIV × $1/f_{ADC10CLK}$			
$t_{ADC10ON}$	Turn-on setting time of the ADC	(2)					100	ns

(1) Over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(2) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.

表 7. 10-Bit ADC, Linearity Parameters (MSP430G2x32 Only)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error		3 V			±1	LSB
E_D	Differential linearity error		3 V			±1	LSB
E_O	Offset error	Source impedance R_S < 100 Ω	3 V			±1	LSB
E_G	Gain error		3 V		±1.1	±2	LSB
E_T	Total unadjusted error		3 V		±2	±5	LSB

2.2 Digital Isolator

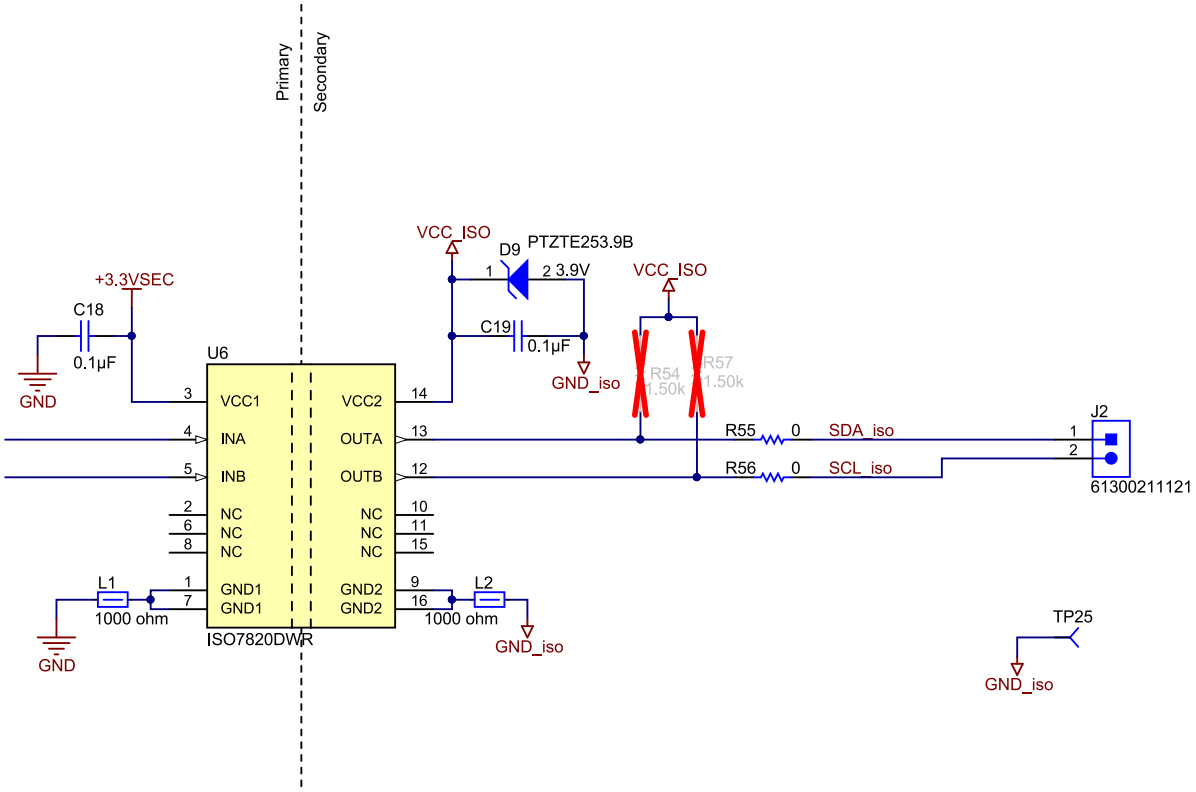


図 6. Digital Isolator With RI

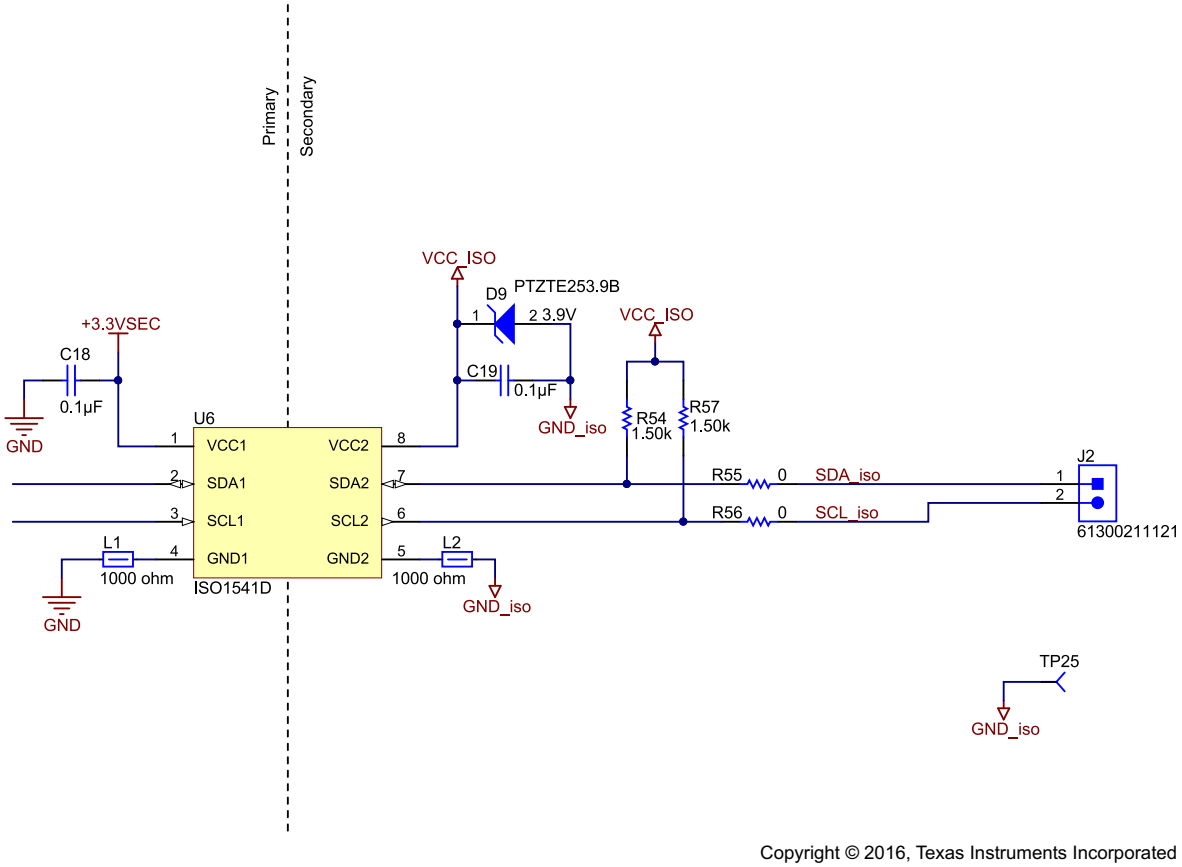


図 7. Digital Isolator With BI

2.2.1 ISO1541D

The ISO1541 devices are low-power, bidirectional isolators that are compatible with I^2C interfaces. The ISO1541 has a bidirectional data and a unidirectional clock channel. The ISO1541 is useful in applications that have a single master while the ISO1540 is ideally fit for multi-master applications (http://www.ti.com/product/ISO1541).

Features:

- Isolated bidirectional, I^2C compatible, communication
- Supports up to 1-MHz operation
- 3- to 5.5-V supply range
- Open-drain outputs with 3.5-mA side 1 and 35-mA side 2 sink current capability
- –40°C to 125°C operating temperature
- ±50-kV/µs transient immunity (typical)
- HBM ESD protection of 4 kV on all pins; 8 kV on bus pins

2.2.2 ISO7320CDR or ISO7320FDR

The ISO732x provides galvanic isolation up to 3000 V_{RMS} for 1 minute per UL and 4242 V_{PK} per VDE. These devices have two isolated channels comprised of logic input and output buffers separated by silicon dioxide (SiO_2) insulation barriers. The ISO7320 has two channels in the same direction. In case of input power or signal loss, the default output is low for devices with the suffix 'F' and high for devices without the suffix 'F'. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. The ISO732x have integrated noise filters for harsh industrial environments where short noise pulses may be present at the device input pins. The ISO732x have TTL input thresholds and operate from 3- to 5.5-V supply levels (http://www.ti.com/product/ISO7320C).

Features:

- Signaling rate: 25 Mbps
- Integrated noise filter on the inputs
- Default output high and low options
- Low power consumption: Typical ICC per channel at 1 Mbps:
  - ISO7320: 1.2 mA (5-V supplies), 0.9 mA (3.3-V supplies)
  - ISO7321: 1.7 mA (5-V supplies), 1.2 mA (3.3-V supplies)
- Low propagation delay: 33 ns typical (5-V supplies)
- 3.3-V and 5-V level translation
- Wide temperature range: –40°C to 125°C
- 65 kV/μs transient immunity, typical (5-V supplies)
- Robust electromagnetic compatibility (EMC)
  - System-level ESD, EFT, and Surge immunity
  - Low emissions
- Isolation barrier life: > 25 years
- Operates from 3.3-V and 5-V supplies

表 8. ISO7320FCD Specifications

PARAMETER	VALUE
Manufacturer part number	ISO7320FCD
Technology	Capacitive coupling
Number of channels	2
Inputs: Side 1/Side 2	2/0
Channel type	Unidirectional
Voltage: Isolation voltage	3000 V_{RMS}
Common-mode transient immunity (min)	25 kV/μs
Data rate	25 Mbps
Propagation delay tpLH / tpHL (max)	57 ns, 57 ns
Pulse width distortion (max)	4 ns
Rise / fall time (typ)	2.4 ns, 2.1 ns
Supply voltage	3 to 5.5 V
Operating temperature	–40°C to 125°C

2.2.3 ISO7820DWR of ISO7820FDWR

The ISO7820 is a high-performance, dual-channel digital isolator with 8000-V_{PK} isolation voltage The isolator provides high electromagnetic immunity and low emissions at low power consumption, while isolating CMOS or LVCMOS digital I/Os. The ISO7820 has two forward channels and no reverse-direction channel. If the input power or signal is lost, the default output is high for the ISO7820 and low for the ISO7820F. Used in conjunction with isolated power supplies, this device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry (http://www.ti.com/product/iso7820/description/).

Features:

- Signaling rate: Up to 100 Mbps
- Wide supply range: 2.25 to 5.5 V
- 2.25- to 5.5-V level translation
- Wide temperature range: –55°C to 125°C
- Low power consumption, Typical 1.7 mA per channel at 1 Mbps
- Low propagation delay: 11 ns typical (5-V supplies)
- Industry leading CMTI (Min): ±100 kV/μs
- Robust EMC
- System-level ESD, EFT, and Surge immunity
- Low emissions
- Isolation barrier life: > 25 years

表 9. ISO7820DW Specifications

PARAMETER	VALUE
Manufacturer part number	ISO7820DW
Technology	Capacitive coupling
Number of channels	2
Inputs: Side 1/Side 2	2/0
Channel type	Unidirectional
Isolation voltage	5700 V_{RMS}
Common-mode transient immunity (min)	70 kV/μs
Data rate	100 Mbps
Propagation delay tpLH / tpHL (max)	16 ns, 16 ns
Pulse width distortion (max)	4.6 ns
Rise / fall time (typ)	2.4 ns, 2.4 ns
Supply voltage	2.25 to 5.5 V
Operating temperature	–55°C to 125°C
Supplier device package	16-SOIC

2.3 Isolated Power Supply

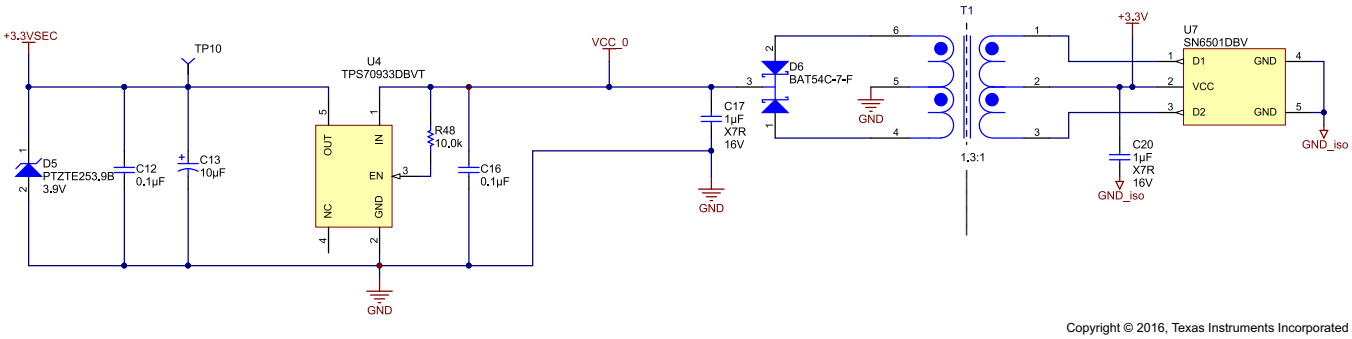


図 8. Isolated Power Supply

2.3.1 Push-Pull Driver for Isolated Power Supplies (SN6501DBV)

The SN6501 is a monolithic oscillator and power-driver, specifically designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3-V or 5-V DC power supply. The secondary can be wound to provide any isolated voltage based on the transformer turns ratio.

The SN6501 consists of an oscillator followed by a gate drive circuit that provides the complementary output signals to drive the ground referenced N-channel power switches. The internal logic ensures break before-make action between the two switches. The SN6501 is available in a small SOT-23 (5) package and is specified for operation at temperatures from –40°C to 125°C.

Features:

- Push-pull driver for small transformers
- Single 3.3- or 5-V supply
- High primary-side current drive:
  - 5-V supply: 350 mA (max)
  - 3.3-V supply: 150 mA (max)
- Low ripple on rectified output permits small output capacitors
- Small 5-pin SOT-23 package

2.3.2 Isolation Transformer

表 10. Isolation Transformer 750313638 Specifications

PARAMETER	SPECIFICATION
Type	DC/DC converter
Applications	Forward, push-pull converters
Intended chipset	SN6501
Voltage—Primary	—
Voltage—Auxiliary	—
Voltage—Isolation	5000 V_{RMS}
Frequency	—
Operating temperature	–40°C to 125°C
Mounting type	Surface mount

表 10. Isolation Transformer 750313638 Specifications (continued)

PARAMETER	SPECIFICATION
Size and dimension	9.14 × 8.00 mm (L × W)
Height—Seated (max)	7.62 mm
Chipset manufacturer	Texas Instruments

2.3.3 Power Supply Overvoltage and ESD Protection Zener (PTZTE253.9B)

表 11. 3.9-V Power Supply Protection Zener Diode Specification

PARAMETER	SPECIFICATION
Voltage—Zener (Nom; Vz)	4.1 V
Tolerance	±6%
Power—Max	1 W
Impedance (Max; Zzt)	15 Ω
Current—Reverse leakage at Vr	40 µA at 1 V
Mounting type	Surface mount
Package or case	DO-214AC, SMA
Supplier device package	PMDS

2.3.4 LDO

The TPS70933DBVT linear regulator is an ultra-low, quiescent current device designed for power sensitive applications. A precision band-gap and error amplifier provides 2% accuracy over temperature. A quiescent current of only 1 µA makes these devices ideal solutions for battery-powered, always-on systems that require very little idle-state power dissipation. These devices have thermal-shutdown, current-limit, and reverse-current protections for added safety.

表 12. 3.3-V LDO Specifications

PARAMETER	SPECIFICATION
Regulator topology	Positive fixed
Voltage—Output	3.3 V
Current—Output	150 mA
Voltage—Dropout (Typical)	0.96 V at 150 mA
Number of regulators	1
Voltage—Input	Up to 30 V
Current—Limit (Min)	200 mA
Operating temperature	–40°C to 125°C
Package	SOT23-5

2.4 Input Voltage Divider, Signal Conditioning, and Protection

Note on Resistor Dividers

The 300-kΩ resistance was increased to 500 kΩ and 1 MΩ, and voltage measurement accuracy was tested. No variation in accuracy was observed with increase in resistance. The 300-kΩ impedance has been finalized assuming that the binary inputs would be specified with minimum resistance. The division ratio has to be maintained even with an increase in total resistance.

Note on Gain Resistors

Because these modules are expected to measured AC/DC inputs, the resistance value is critical for accuracy. Do not increase the resistance above the values used as shown in 図 9. In case values are increased, there may be change in accuracy, and these need to be verified.

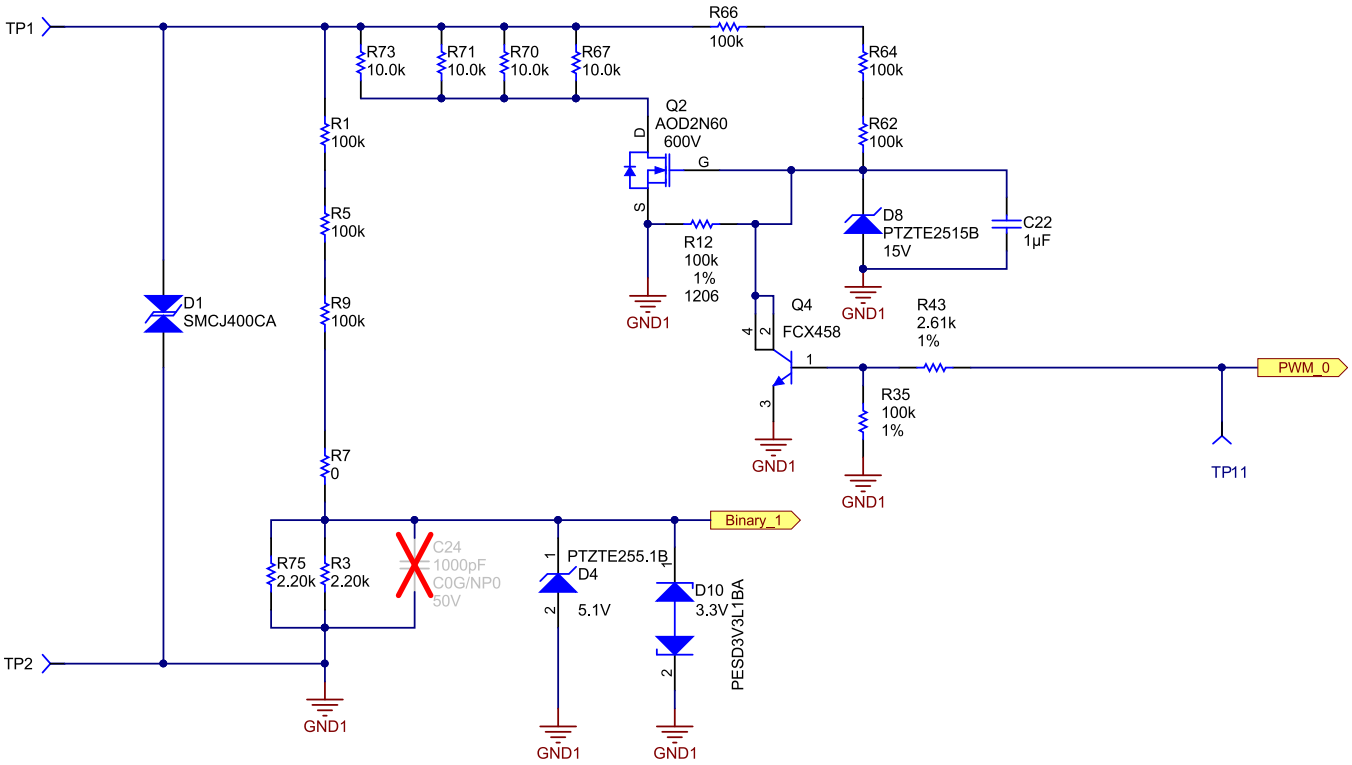


図 9. Channel 1 Input Potential Divider

注: Populate D4 for DC input type only.

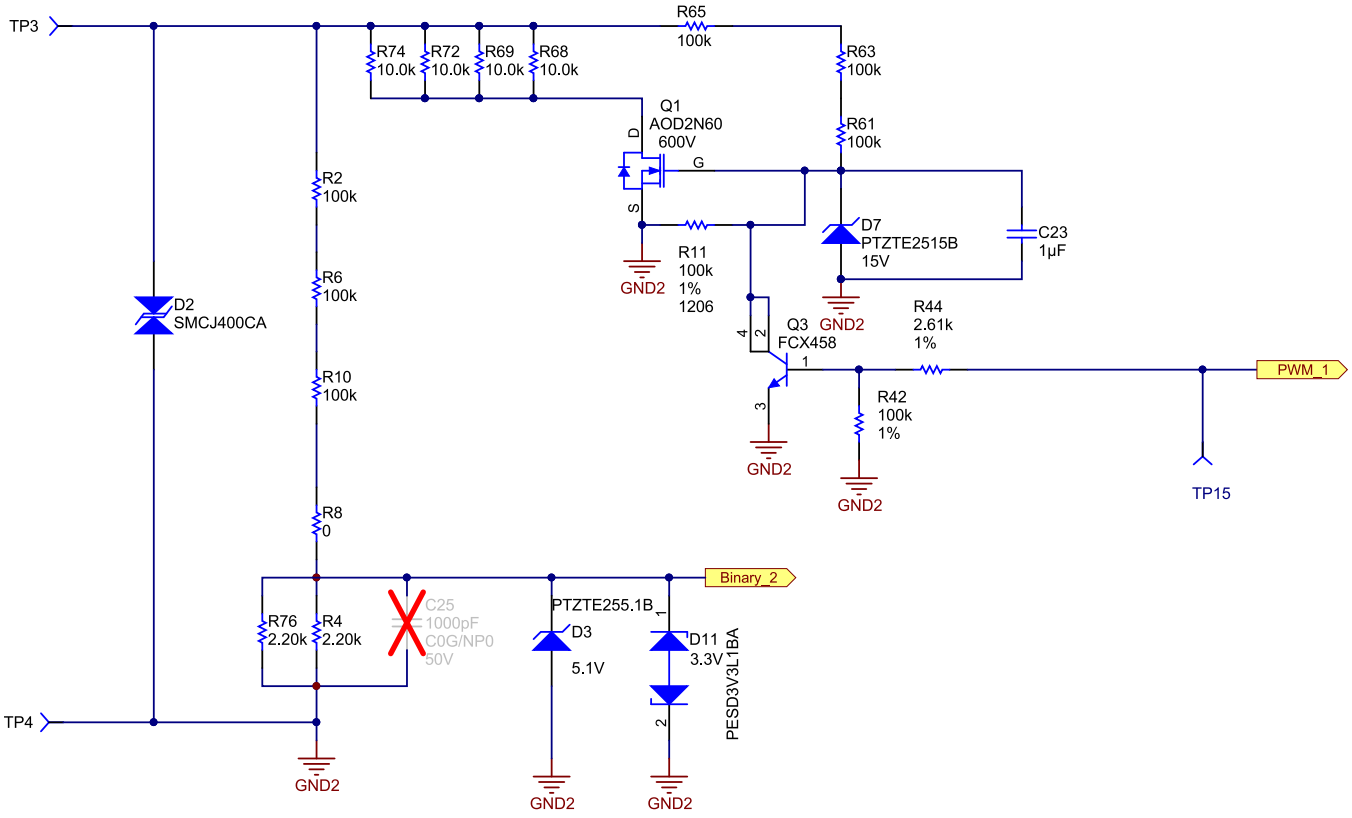


図 10. Channel 2 Input Potential Divider

注: Populate D3 for DC input type only.

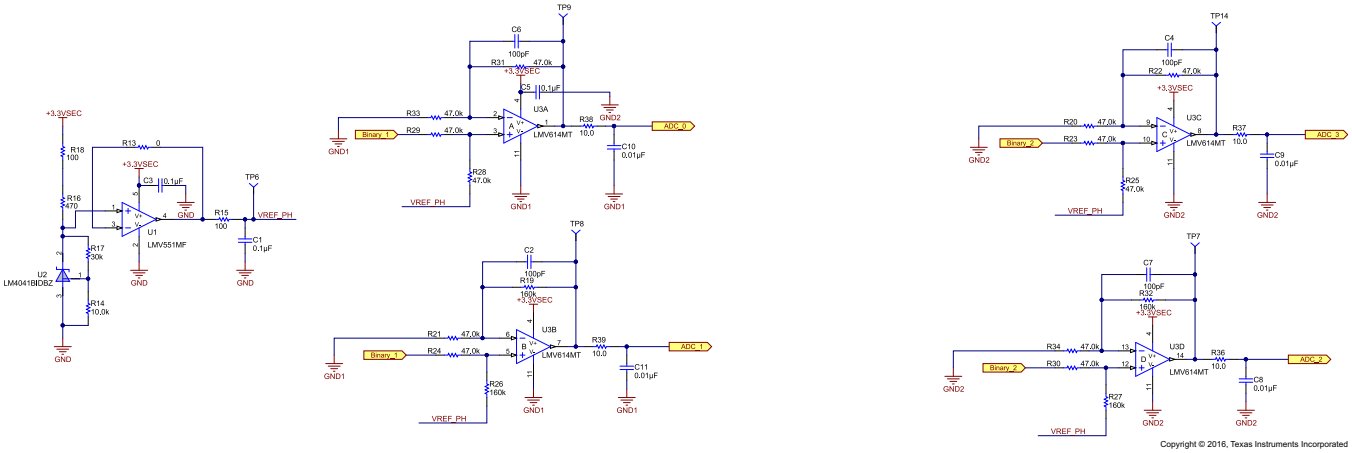


図 11. Binary Input 1 and 2 Gain and Reference Including Buffer

2.4.1 Input Protection

The binary input module is protected against overvoltage and transients. The SMCJ400CA and PESD3V3L1BA are used to achieve the required protection. These devices are optional and can be used based on the application.

表 13. SMCJ400 Specifications

PARAMETER	SPECIFICATION
Type	Zener
Bidirectional channels	1
Voltage—Reverse standoff (Typ)	400 V
Voltage—Breakdown (Min)	447 V
Voltage—Clamping (Max) at I_{PP}	648 V
Current—Peak pulse (10/1000 µs)	2.3 A
Power—Peak pulse	1500 W (1.5 kW)
Power line protection	No
Applications	General Purpose
Capacitance at frequency	—
Operating temperature	–55°C to 150°C (T_J)
Mounting type	Surface mount
Package or case	DO-214AB, SMC

表 14. PESD3V3L1BA TVS Diode Specifications

PARAMETER	SPECIFICATION
Manufacturer part number	ISO7820DW
Technology	Capacitive coupling
Number of channels	2
Inputs: Side 1/Side 2	2/0
Channel type	Unidirectional
Voltage—Isolation	5700 V_{RMS}
Common-mode transient immunity (min)	70 kV/µs
Data rate	100 Mbps
Propagation delay tpLH / tpHL (max)	16 ns, 16 ns
Pulse width distortion (max)	4.6 ns
Rise / fall time (typ)	2.4 ns, 2.4 ns
Voltage—Supply	2.25 to 5.5 V
Operating temperature	–55°C to 125°C
Supplier device package	SOD-323

2.4.2 Resistor Divider

A 100-kΩ 1206 package resistor, which can withstand a maximum voltage of 200 V, is selected for this application. The

2.4.3 ADC Input Overvoltage Protection (PTZTE255.1B)

A Zener diode is used to protect the electronic circuit from overvoltage and ESD.

表 15. 5.1-V Analog Input to ADC Protection Diode Specifications

PARAMETER	SPECIFICATION
Voltage—Zener (Nom; Vz)	5.4 V
Tolerance	±6%
Power—Max	1 W
Impedance (Max; Zzt)	8 Ω
Current—Reverse leakage at Vr	20 µA at 1 V
Mounting type	Surface mount
Package or case	DO-214AC, SMA

2.4.4 Amplifier Gain Stage Using LMV614

The LMV614 is a quad low-voltage, low-power op amp. The device is designed specifically for low-voltage general purpose applications. Other important product characteristics are its rail to-rail I/O, low supply voltage of 1.8 V, and wide temperature range. The LMV614 input common mode extends 200 mV beyond the supplies and the output can swing rail-to-rail unloaded and within 30 mV with 2-kΩ load at a 1.8-V supply. The LMV614 achieves a gain bandwidth of 1.4 MHz while drawing 100 µA (typ) quiescent current.

The industrial-plus temperature range of −40°C to 125°C allows the LMV614 to accommodate a broad range of extended environment applications.

The LMV614 is offered in 14-pin TSSOP and SOIC. These small package amplifiers offer an ideal solution for applications requiring minimum PCB footprint. Applications with area constrained PC board requirements include portable and battery operated electronics (http://www.ti.com/product/LMV614).

Features:

- (Typical 1.8-V supply values; unless otherwise noted)
- Ensured 1.8-V, 2.7-V, and 5-V specifications
- Output swing
  - with 600-Ω load 80 mV from rail
  - with 2-kΩ load 30 mV from rail
- V_{CM} 200 mV beyond rails
- Supply current (per channel) 100 µA
- Gain bandwidth product 1.4 MHz
- Maximum V_{OS} 4.0 mV

2.4.5 Reference

The DC reference for level-shifting is generated using the LM4041.

2.4.5.1 Adjustable Precision Shunt Voltage Reference

The LM4041 series of shunt voltage references are versatile, easy-to-use references suitable for a wide array of applications. The reference is used for level shifting the AC voltage input by AVDD/2. The input voltage is shifted to 1.65 V. This series requires no external capacitors for operation and is stable with all capacitive loads. Additionally, the reference offers low-dynamic impedance, low noise, and a low-temperature coefficient to ensure a stable output voltage over a wide range of operating currents and temperatures. The LM4041 uses fuse and Zener-zap reverse breakdown voltage trim during wafer sort to offer four output voltage tolerances, ranging from 0.1% (max) for the A grade to 1% (max) for the D grade. As a result, a great deal of flexibility is offered to designers in choosing the best cost-to-performance ratio for their applications. The LM4041 is available in a fixed (1.225 V nominal) or an adjustable version, which requires an external resistor divider to set the output to a value between 1.225 and 10 V.

Features:

- Small packages: SOT23, SC70-5
- No output capacitor required
- Output voltage tolerance
- LM4041D: ±1% at 25°C
- Low output noise: 20 μV_{RMS} (10 Hz to 10 kHz)
- Wide operating current range: 60 μA to 12 mA
- Extended temperature range: –40°C to 125°C
- Low temperature coefficient: 100 ppm/°C (max)

2.4.5.2 Buffer for Reference

The LMV551 are high-performance, low-power op amps implemented with TI's advanced VIP50 process. They feature 3 MHz of bandwidth while consuming only 37 μA of current per amplifier, which is an exceptional bandwidth to power ratio in this op amp class. These amplifiers are unity gain stable and provide an excellent solution for low power applications requiring a wide bandwidth.

表 16. Reference Buffer Amplifier Specifications

PARAMETER	SPECIFICATION
Amplifier type	General purpose
Number of circuits	1
Output type	Rail-to-rail
Slew rate	1 V/μs
Gain bandwidth product	3 MHz
–3-db bandwidth	—
Current—Input bias	20 nA
Voltage—Input offset	1 mV
Current—Supply	37 μA
Current—Output per channel	25 mA
Voltage—Supply, single or dual (±)	2.7 to 5.5 V
Operating temperature	–40°C to 125°C

表 16. Reference Buffer Amplifier Specifications (continued)

PARAMETER	SPECIFICATION
Mounting type	Surface mount

2.5 Wetting Current Control (Used for DC Inputs Only)

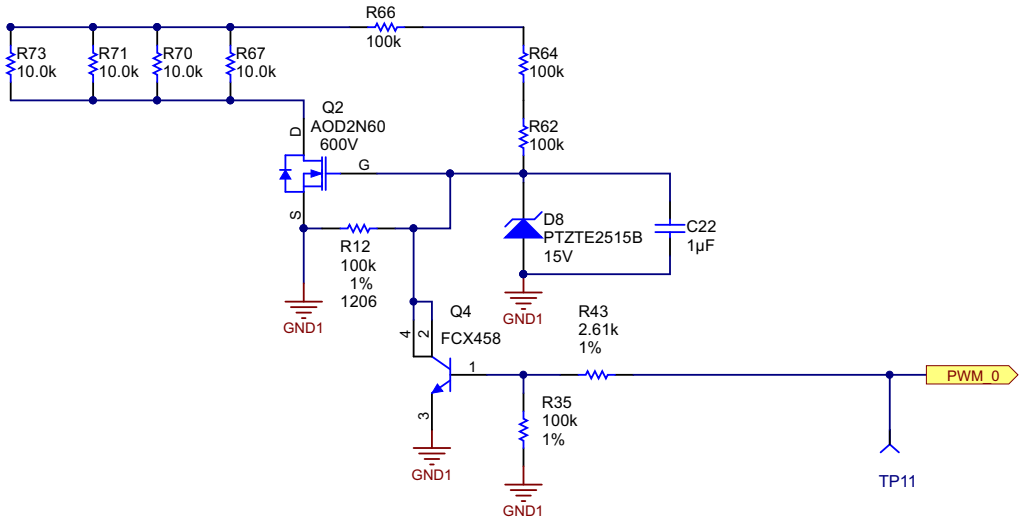


図 12. Wetting Current Control Circuit

2.5.1 Transistor Drive for MOSFET Gate Drive

A transistor is used to drive the MOSFET that controls the wetting current. The bias voltage of 15 V max is generated from the binary input using a Zener PTZTE2515BCT regulator.

表 17. 15-V Transistor Bias Voltage Regulation Zener Specification

PARAMETER	SPECIFICATION
Voltage—Zener (Nom; Vz)	15.4 V
Tolerance	±6%
Power—Max	1 W
Impedance (Max; Zzt)	10 Ω
Current—Reverse leakage at Vr	10 µA at 11 V
Mounting type	Surface mount
Package or case	DO-214AC, SMA

表 18. FCX458 Transistor Specifications

PARAMETER	SPECIFICATION
Transistor type	NPN
Current—Collector (Ic; Max)	225 mA
Voltage—Collector emitter breakdown (Max)	400 V
Vce saturation (Max) at Ib, Ic	500 mV at 6 mA, 50 mA
Current—Collector cutoff (Max)	100 nA
DC current gain (hFE) (Min) at Ic, Vce	100 at 50 mA, 10 V
Power (Max)	1 W
Frequency—Transition	50 MHz
Mounting type	Surface mount
Package or case	TO-243AA

2.5.2 Current Limiting Resistors and MOSFET (AOD2N60A)

表 19. Wetting Current Control MOSFET Specifications

PARAMETER	SPECIFICATION
FET type	MOSFET N-channel, metal oxide
FET feature	Standard
Drain-to-source Voltage (V_{DS})	600 V
Current—Continuous drain (Id) at 25°C	2 A (Tc)
Rds On (Max) at Id, Vgs	4.7 Ω at 1 A, 10 V
$V_{GS(th)}$ (Max) at Id	4.5 V at 250 µA
Gate charge (Qg) at Vgs	11 nC at 10 V
Input capacitance (Ciss) at V_{DS}	295 pF at 25 V
Power (Max)	57 W
Mounting type	Surface mount
Package or case	TO-252-3, DPak (two leads + tab), SC-63
Supplier device package	TO-252 (D-Pak)

Four resistors, 1206 package 10-kΩ each in parallel, are used as current limit for wetting current. A D-PAK MOSFET with a 600-V rating is used for enhanced reliability.

2.6 Host Interface

The host interface can be simulated using an I^2C interface. The following steps are for the binary module and the host interface:

- The binary module is configured to be the master.
- The binary module computes the required RMS value.
- The measured value can be communicated to the host.

The I^2C interface is available in the ISO1541D family. When using the ISO7320 or ISO7820 family of digital isolators, one-way communication is simulated to send out the data to the host. The bit banging method can be followed with the binary module as the master generating DATA and clock.

For an alternate interface approach, the thresholds can be set using jumpers, and a digital isolator can be used as a digital output to indicate the DC input status.

2.7 Hardware Design Guidelines

- Input voltage divider selection: Ensure the resistors are de-rated by 30% for the maximum withstand The voltage rating.
- Wetting current control resistor selection: The short time overload capability must be greater than 2.5 times the normal voltage withstand capability for one second.
- 15-V Zener selection for MOSFET switching: Vz must be constant for wide bias currents. The Zener current must be as low as possible to reduce power loss.
- Zener selection for ADC input overvoltage protection: At lower biasing, current Vz reduces and this will clip the input voltage affecting accuracy. The Vz at low bias current must be selected such that at the lowest input voltage, the voltage would be sufficient to bias the MOSFET.

2.8 Enhancements

A different solution is discussed in this design guide. The TI digital isolator portfolio is listed at the Products for Digital Isolators page (http://www.ti.com/lsds/ti/isolation/digital-isolators-products.page#). TI has roadmap of products including high-speed, robust EMC digital isolators (http://www.ti.com/product/ISO7741).

3 Getting Started Hardware and Software

3.1 Hardware

3.1.1 Power Connection

The binary input module is powered by a 3.3-V DC input from the host side. The isolated power is generated on board. The 3.3-V DC input is connected as shown in 表 20:

表 20. Power Supply Connection to Binary Module

PINS	SIGNAL NAME
TP27	3.3 V
TP28	Ground

3.1.2 Input Voltage (Digital Input) Connection

表 21. Binary Input Connection

INPUT	PINS	SIGNAL NAME
BI 1	TP1	DC input +ve
	TP2	DC input –ve
BI 2	TP3	DC input +ve
	TP4	DC input –ve

3.1.3 Host Interface

表 22. Binary Module Digital Output to Host Interface

PINS	SIGNAL NAME
J2-Pin1	Data out
J2-Pin2	Clock out
TP25	Ground

3.2 Software

3.2.1 Initialization

表 23. MCU Peripherals Initialization for AC/DC Binary Module Functionality

FUNCTIONALITY	DESCRIPTION
MCU clock	SMCLK and DCO are initialized to 1 MHz
Timer	1. Configure the timer capture control register (TA0CCTL0) to select no capture CMx as 0, compare/capture input selected as CCIxA, output mode OUTMODx as 0 and enable compare interrupt CCIE. 2. Timer A programmed to provide interrupt every 200 µs (or any other sampling interval desired). Set the sampling interval (TA0CCR0) 3. Configure the Timer A control register (TA0CTL) to choose SMCLK, divider as 1 and up/down mode.
ADC – Four channels	1. Disable conversion. 2. Configure the following options for the ADC control register0 (ADC10CTL0): (a) Enable ADC interrupt. (b) Switch ON ADC. (c) Set the sample and hold time to 16× ADC10CLKs. (d) Set the reference voltages for ADC: VR+ = V_{CC} and VR– = VSS ADC10CTL0, once configured, does not need to be changed to switch between different channels. 3. Configure the following options for the ADC control register0 (ADC10CTL1): (a) Set the mode to single channel single conversion. (b) Set the ADC clock to ADC1OSC. (c) Set the divider to 1. (d) Set the sampling trigger to ADC10SC bit. (e) Set the channel to be sampled (A0). 4. Enable ADC channels ADC10AE0. 5. Enable conversion. 6. Once the sampling interval timer issues a trigger, the first ADC channel (A0) is sampled. (a) Once the sample value for channel A0 is read from ADC10MEM, clear the ADC10SC bit. (b) Reinitialize ADC10CTL1 and ADC10AE0 with the other desired ADC channel (A3, A4, or A5). (c) Conversion can be started by making the ADC10SC bit high. (d) Repeat the same process for the other channels (every sampling interval) until all channels have been sampled.
Ports	1. Configure the direction of the ports (P1DIR); 0 as inputs and 1 as outputs. 2. Set the default values for outputs (0 as low, 1 as high).
I^2C	1. Set the output pins for I^2C (P1.6 and P1.7) to high. 2. Enable the pull up resistors for P1.6 and P1.7 (P1REN). 3. Enable the USI function by setting the USIPE6 and USIPE7 bits in USICTL0 register. 4. Disable the USI peripheral using software reset (USISWRST bit). 5. Enable I^2C mode and USI interrupt enable. 6. Set clock polarity. 7. Disable automatic clear control (USIIFGCC bit). 8. Enable USI peripheral by clearing the (USISWRST bit).

3.2.2 Functionality

表 24. AC/DC Binary Module Functional Description

FUNCTIONALITY	DESCRIPTION
Power ON	1. Stop the watchdog timer. 2. Initialize the clocks to set SMCLK to 1 MHz. 3. Disable all interrupts. 4. Set the direction of port pins to default values. 5. Initialize I^2C in master mode 6. Configure Timer A to provide an interval based interrupt using compare register. The timer interrupt can be used to periodically trigger ADC sampling. 7. Initialize ADC to sample one ADC channel. Re-initialize ADC10CTL1 and ADC10AE0 to sample a different ADC channel. 8. Enable all interrupts.
ADC sample capturing for all four channels	• Samples are triggered by setting ADC10SC bit. (From the timer interrupt for the first channel, meaning A0). • When conversion is complete, it triggers an interrupt. The result is obtained by reading the register ADC10MEM. • Reinitialize the ADC to read the other ADC channels and issue ADC10SC trigger. Repeat this step to read the other ADC channels.
ADC samples integration	• After the value is read from ADC10MEM, the offset has to be corrected. • For each ADC channel, the sample values are added over a timer period (1 ms) and then averaged by dividing with the number of sample counts.
30- and 60-ms ADC count calculation	Calculation of 1-ms average (for each channel): • The 1-ms average for each channel can be stored for three iterations (that is, three such 1-ms average values).
	Calculation of 3-ms average (for each channel): • 3-ms average can be calculated using the three counts of 1-ms averages and is stored for 10 or 20 counts.
	Calculation of 30- or 60-ms average (for each channel): • 10 or 20 counts of 3-ms average is stored and can be averaged to provide 30 or 60 ms average.
I^2C interface for communicating ADC count to host	• The 30-ms average values for all four channels can be transmitted over I^2C to the host processor. • A pre-requisite for this is to have a host processor (for example, LaunchPad) that runs as an I^2C slave. • The master sends 30-ms averages for each channel on I^2C.

3.2.3 Calculations

表 25. Maximum DC Input Allowed

PARAMETER	SPECIFICATION
DC offset in ADC counts	511
ADC range in counts	1023 – 511 = 512
Resistor divider ratio	301.1 kΩ / 1.1 kΩ = 273.72
DC input ADC reference span	ADCref = 1.65 V
Maximum input voltage	ADCref × Resistor divider ratio ≥ 300 V

表 26. Maximum AC Input Allowed

PARAMETER	SPECIFICATION
DC offset in ADC counts	511
Peak ADC range in counts	1023 – 511 = 512
RMS ADC range in counts	512 / (1.414) = 362
Resistor divider ratio	301.1 kΩ / 1.1 kΩ = 273.72
AC RMS ADC reference span	AvgRef = 1.65 V / (1.414) = 1.1668
Maximum input voltage	AvgRef × Resistor divider ratio ≥ 300 V

表 27. Converting ADC Count to Voltage — DC Input Low Gain

PARAMETER	SPECIFICATION
ADCref	1.65 V
Maximum input	450 V
Gain factor	1
Max ADC count for DC input	512
DC voltage equivalent for one ADC count	Maximum input / (ADC count × Gain factor) = 0.878 V

The minimum ADC resolution of 1 count equals approximately 1 V. To improve the resolution, a gain stage of 3.4 is used.

表 28. Converting ADC Count to Voltage — DC Input High Gain

PARAMETER	SPECIFICATION
ADCref	1.65 V
Maximum input	450 V
Gain factor	3.4
Max ADC count for DC input	512
DC voltage equivalent for one ADC count	Maximum input / (ADC count × Gain factor) = 0.2582

表 29. Converting ADC Count to Voltage — AC Input Low Gain

PARAMETER	SPECIFICATION
ADCref — peak	1.65 V
Maximum input	315 V
Gain factor	1
Max ADC count for RMS input	512 / 1.414 = 362
RMS voltage equivalent for one ADC count	Maximum input / (ADC count × Gain factor) = 0.870

The minimum ADC resolution of 1 count equals approximately 1 V. To overcome this issue, a gain stage of 3.4 is used.

表 30. Converting ADC Count to Voltage — AC Input High Gain

PARAMETER	SPECIFICATION
ADCref — peak	1.65 V
Maximum input	315 V
Gain factor	3.4
Max ADC count for RMS input	512 / 1.414 = 362
RMS voltage equivalent for one ADC count	Maximum input / (ADC count × Gain factor) = 0.260

3.2.4 Programming

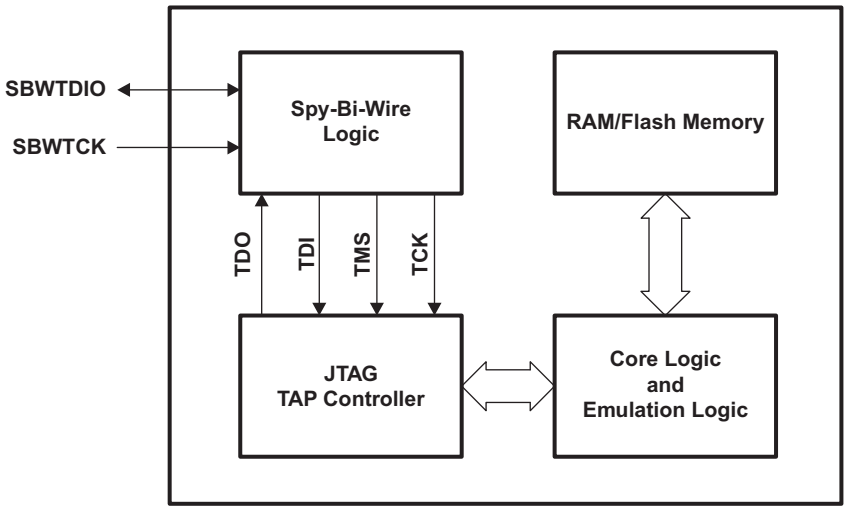


図 13. Spy-Bi-Wire Basic Concept

The 2-wire interface is made up of the SBWTCK (Spy-Bi-Wire test clock) and SBWTDIO (Spy-Bi-Wire test data I/O) pins. The SBWTCK signal is the clock signal and is a dedicated pin. In normal operation, this pin is internally pulled to ground. The SBWTDIO signal represents the data and is a bidirectional connection. To reduce the overhead of the 2-wire interface, the SBWTDIO line is shared with the $\overline{\text{RST}}$/NMI pin of the device.

4 Testing and Results

4.1 Test Setup

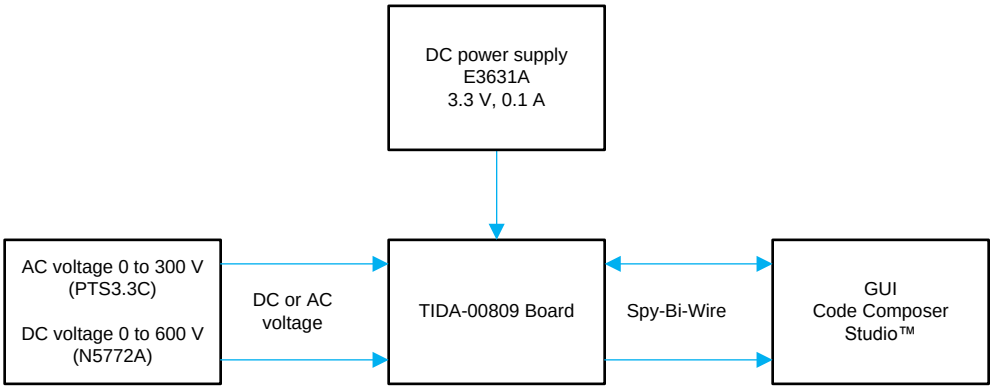


図 14. Test Setup for Binary Module Performance

The test setup for testing the binary module consists of

- DC power supply (3.3 V)
- AC or DC input voltage (20 to 270 V)
- TIDA-00809 board with BI or RI digital isolators
- GUI for firmware upgrade and data capture

Ensure the inputs do not exceed the range specified above for proper operation.

4.2 Test Data

4.2.1 Functional Testing

表 31. Functional Testing

PARAMETER	SPECIFICATION	MEASUREMENT
Isolated supply	3.3 V	3.31
Reference output	1.65 V	1.645
Op amp gain	×1 , ×3.7	OK
MCU programming	Spy-Bi-Wire	OK

4.2.2 Voltage Measurement Accuracy Testing

注: The readings in the following subsections are measurements taken without any calibration. The errors include component tolerances and ADC errors. The accuracy can be improved by introducing software calibration.

The errors observed can be further improved by calibrating gain. To ensure that the results are less than ±3.0% of the ±1-V measured value (programmable step size), applying gain calibration is recommended. The gain calibration can be applied on the host side or binary module side. For initial testing, averaging was done for 10, 30, and 60 ms. The measurement was repeatable at 30 and 60 ms for AC input, and there was no difference observed in the measured values. In case measurements are expected to be done faster than 30 ms, characterize accuracy before implementing.

4.2.2.1 Testing With 30-ms Averaging

表 32. AC Input Voltage versus Measured Voltage Difference

INPUT PARAMETERS			A0 AND A3		A4 AND A5	
APPLIED VOLTAGE AT 50 Hz	ALLOWED VOLTAGE LIMIT (±V)	GAIN	MEASURED VOLTAGE	DIFF	MEASURED VOLTAGE	DIFF
15	1.45	High	14.764	–0.236	15.042	0.042
23	1.69		22.285	–0.715	22.842	–0.158
24	1.72		23.399	–0.601	23.677	–0.323
48	2.44		46.519	–1.481	46.798	–1.202
108	4.24	Low	107.705	–0.295	107.705	–0.295
109	4.27		106.735	–2.265	108.675	–0.325
110	4.3		107.705	–2.295	109.646	–0.354
111	4.33		110.616	–0.384	110.616	–0.384
112	4.36		110.616	–1.384	111.586	–0.414
228	7.84		224.143	–3.857	225.113	–2.887
229	7.87		224.143	–4.857	225.113	–3.887
230	7.9		224.143	–5.857	227.054	–2.946
231	7.93		225.113	–5.887	228.024	–2.976
232	7.96		227.054	–4.946	227.054	–4.946
264	8.92		256.163	–7.837	258.104	–5.896
276	9.28		269.748	–6.252	268.778	–7.222

表 33. DC Input Voltage versus Measured Voltage Difference

INPUT PARAMETERS			A0 AND A3		A4 AND A5	
APPLIED VOLTAGE	ALLOWED VOLTAGE LIMIT (±V)	GAIN	MEASURED VOLTAGE	DIFF	MEASURED VOLTAGE	DIFF
10	1.3	High	9.876	–0.124	9.876	–0.124
15	1.45		14.941	–0.059	14.941	–0.059
23	1.69		22.791	–0.209	22.791	–0.209
24	1.72		23.804	–0.196	23.804	–0.196
25	1.75		24.564	–0.436	24.817	–0.183
48	2.44		47.355	–0.645	47.355	–0.645
108	4.24	Low	106.735	–1.265	107.617	–0.383
109	4.27		108.499	–0.501	108.499	–0.501
110	4.3		109.381	–0.619	109.381	–0.619
111	4.33		110.263	–0.737	110.263	–0.737
112	4.36		111.145	–0.855	111.145	–0.855
228	7.84		225.819	–2.181	225.819	–2.181
229	7.87		226.701	–2.299	226.701	–2.299
230	7.9		228.465	–1.535	228.465	–1.535
231	7.93		229.347	–1.653	229.347	–1.653
232	7.96		230.23	–1.77	231.112	–0.888
264	8.92		260.221	–3.779	260.221	–3.779
320	10.6		316.676	–3.324	315.794	–4.206

4.2.2.2 Error in % of the Measured Value

表 34. AC Input Voltage versus Measured Voltage Error (% of the Reading)

INPUT PARAMETERS		A0 AND A3	A4 AND A5
APPLIED VOLTAGE AT 50 Hz	GAIN	ERROR (%)	ERROR (%)
15	High	–1.58	0.28
23		–3.11	–0.69
24		–2.51	–1.34
48		–3.09	–2.51
108	Low	–0.27	–0.27
109		–2.08	–0.30
110		–2.09	–0.32
111		–0.35	–0.35
112		–1.24	–0.37
228		–1.69	–1.27
229		–2.12	–1.70
230		–2.55	–1.28
231		–2.55	–1.29
232		–2.13	–2.13
264		–2.97	–2.23
276		–2.27	–2.62

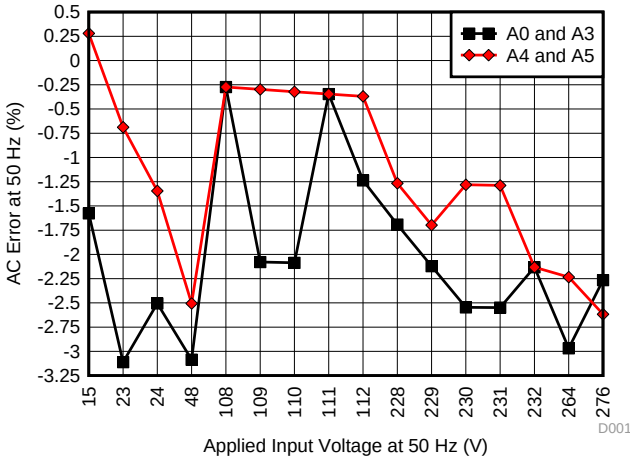


図 15. Input Voltage versus Measured Voltage Error (% of the Reading)

表 35. Input Voltage versus Measured Voltage Error (% of the Reading)

INPUT PARAMETERS		A0 AND A3	A4 AND A5
APPLIED VOLTAGE DC INPUT	GAIN	ERROR (%)	ERROR (%)
10	High	–1.24	–1.24
15		–0.39	–0.39
23		–0.91	–0.91
24		–0.82	–0.82
25		–1.75	–0.73
48		–1.34	–1.34
108	Low	–1.17	–0.35
109		–0.46	–0.46
110		–0.56	–0.56
111		–0.66	–0.66
112		–0.76	–0.76
228		–0.96	–0.96
229		–1.00	–1.00
230		–0.67	–0.67
231		–0.72	–0.72
232		–0.76	–0.38
264		–1.43	–1.43
320		–1.04	–1.31

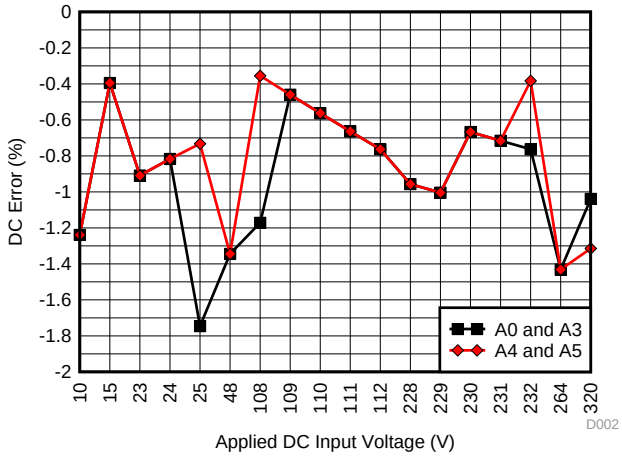


図 16. DC Input Voltage versus Measured Voltage Error (% of the Reading)

4.2.2.3 Frequency Variation

表 36. Voltage Measurement Error With Frequency

GAIN	INPUT VOLTAGE	MEASURED VOLTAGE AT 50 Hz	ERROR (%)	MEASURED VOLTAGE AT 60 Hz	ERROR (%)
High	48	46.79758	–2.50505	47.07613	–1.92472
Low	240	231.9055	–3.3727	231.9055	–3.3727

注: Variation between reading at 50 and 60 Hz was observed to be within 1%.

4.2.2.4 Wetting Current Measurement

表 37. Wetting Current Measurement at Different Voltage Inputs (DC Only)

DC VOLTAGE INPUT SWITCHED ON FOR 50 ms	IMPEDANCE	INPUT 1 CURRENT (mA)	DUTY CYCLE	INPUT 2 CURRENT (mA)	DUTY CYCLE
24 V	2.5 K	~9	N/A	~9	N/A
110 V	2.5 K	~44	N/A	~44	N/A
230 V	2.5 K	~44	50%	~44	50%

4.2.2.5 Drift Due to Temperature Variation of Signal Conditioning Circuit

The signal conditioning circuit consisting of the resistor divider, the 400-V input TVS, 5.1-V ADC input protection Zener, was tested for temperature variation. The leakage current for the 400-V TVS is < 1 µA at rated voltage for SMCJ package. The following results indicate that the effect of leakage current does not significantly influence the voltage input to ADC.

表 38. Voltage Drift With Temperature at 300-V Input

TEMPERATURE (°C)	MEASURED VOLTAGE (V)	DIFFERENCE (–V)
–10	298.92	–1.082
12	299.01	–0.986
40	299.01	–0.986
70	299.11	–0.890

表 39. Voltage Drift With Temperature at 110-V Input

TEMPERATURE (°C)	MEASURED VOLTAGE (V)	DIFFERENCE (–V)
–10	109.84	–0.160
10	109.74	–0.256
40	109.84	–0.160
70	109.84	–0.160

表 40. Voltage Drift With Temperature at 24-V Input

TEMPERATURE (°C)	MEASURED VOLTAGE (V)	DIFFERENCE (–V)
–10	23.98	–0.018
10	23.89	–0.113
40	23.98	–0.018
70	23.98	–0.018

4.2.2.6 Binary Input Testing With Digital Output (ISO7320)

The binary module uses an I^2C isolator to communicate the voltage reading to the host MCU. Alternatively, digital isolator can be used with the module to sense fixed voltages.

表 41. Test Results for ISO7320

DC INPUT V_{IN}	APPLIED VOLTAGE	TOLERANCE	BINARY INPUT 1 OBSERVATION	BINARY INPUT 2 OBSERVATION
24	22	±3% of V_{IN} ±1 V	Low	Low
24	26	±3% of V_{IN} ±1 V	High	High
110	106	±3% of V_{IN} ±1 V	Low	Low
110	114	±3% of V_{IN} ±1 V	High	High
240	230	±3% of V_{IN} ±1 V	Low	Low
240	250	±3% of V_{IN} ±1 V	High	High

4.2.2.7 Binary Input Testing With Digital Output (ISO7820)

The digital isolator can be used with the module to sense fixed voltages.

表 42. Test Results for ISO7820

DC INPUT V_{IN}	APPLIED VOLTAGE	TOLERANCE	BINARY INPUT 1 OBSERVATION	BINARY INPUT 2 OBSERVATION
24	22	±3% of V_{IN} ±1 V	Low	Low
24	26	±3% of V_{IN} ±1 V	High	High
110	106	±3% of V_{IN} ±1 V	Low	Low
110	114	±3% of V_{IN} ±1 V	High	High
240	230	±3% of V_{IN} ±1 V	Low	Low
240	250	±3% of V_{IN} ±1 V	High	High

4.2.3 IEC Pre-Compliance Testing—Digital Isolator ISO1541D With BI

The following EMC tests have been performed.

表 43. EMC Tests

TEST	STANDARD
ESD	IEC61000-4-2
EFT	IEC61000-4-4
Surge	IEC61000-4-5

表 44. Performance Criteria

CRITERIA	ACCEPTANCE (PASS) CRITERIA
A	The binary input module must continue to operate as intended. No loss of function or performance occur even during the test.
B	Temporary degradation of performance is accepted. After the test, the binary input module must continue to operate as intended without manual intervention.
C	During the test, a loss of functions accepted, but no destruction of hardware or software. After the test, the binary input module must continue to operate as intended automatically after manual restart or power off/power on.

4.2.3.1 IEC61000-4-2 ESD Test

The IEC610004-2 ESD test simulates the electrostatic discharge of an operator directly onto an adjacent electronic component. An electrostatic charge usually develops in low relative humidity, and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the binary input module, which can happen through direct contact with the binary input module (contact discharge), or through an air-gap (air-discharge). This was applied across signal inputs only. A series of 10 negative and positive pulses were applied directly on the binary inputs during the test (contact discharge). After the test, the binary input module module was verified for functionality. The test results show the binary input module was able to withstand the required discharge. The binary input module was not permanently damaged.

表 45. ESD Test Steps

TEST NO	TEST MODE	OBSERVATION
1	Contact 2 kV	Pass
2	Contact –2 kV	Pass
3	Contact 4 kV	Pass
4	Contact –4 kV	Pass
5	Contact 5 kV	Pass
6	Contact –5 kV	Pass

表 46. ESD Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
ESD	IEC 61000-4-2, contact	Binary input	±4 kV	Pass , Criteria B (After the test, the module continued to operate as intended)

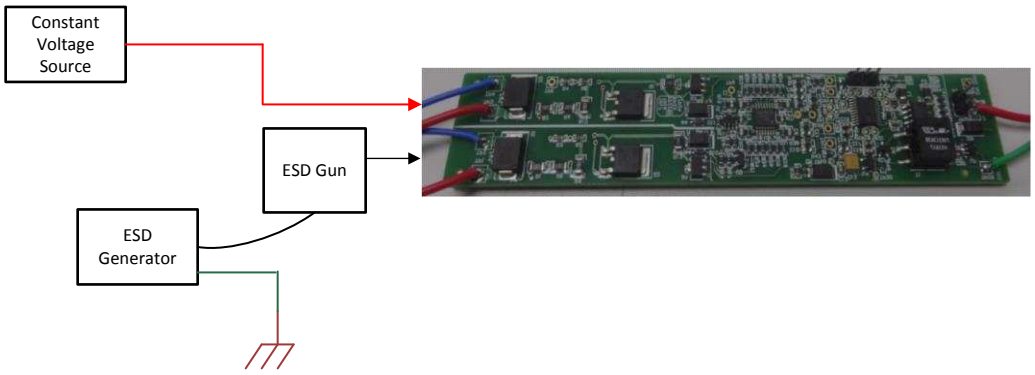


図 17. ESD Setup for Binary Input Module With BI Digital Isolator

注: The ISO1541 can be used with ESD requirements up to 4 kV although these tests confirm that the device performs without failure for a higher ESD level.

4.2.3.2 IEC61000-4-4 EFT Test

The burst signal is injected on the voltage inputs. The test is carried out with the binary input module placed 10 cm above the reference plate. After the test, the binary input module was verified for functionality. The test results show the binary input module was able to withstand up to ±2 kV. The binary input module was able to perform normally after each test. Because functionality could not be verified during the test, the result was noted as passing Class B.

The EFT burst at I/O connectors and the performance criteria expected are as follows:

表 47. EFT Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
EFT	IEC61000-4-4, ±2 kV on binary input	Input lines	± 2 kV	Pass, Criteria B (After the test, the module continued to operate as intended)

表 48. Test Results Steps and Observations for EFT Testing

TEST NO	TEST MODE	OBSERVATION
1	0.5 kV, 5 kHz	Pass
2	–0.5 kV, 5 kHz	Pass
3	1 kV, 5 kHz	Pass
4	–1 kV, 5 kHz	Pass
7	2 kV, 5 kHz	Pass
8	–2 kV, 5 kHz	Pass

図 18. EFT Setup for Binary Input Module With BI Digital Isolator

4.2.3.3 IEC61000-4-5 Surge Test

The IEC61000-4-5 surge test simulates switching transients caused by lightning strikes or the switching of power systems including load changes and short circuits. The test requires five positive and five negative surge pulses with a time interval between successive pulses of 1 minute or less. The unshielded symmetrical data line setup as defined by the IEC61000-4-5 specification was used for this test. The test generator was configured for 1.2/50-µs surges and diode clamps were used for line-to-ground coupling. A series of five negative and positive pulses, with 10 seconds spacing between each pulse, were applied during the test.

After the test, the binary module was verified for functionality. The test results show the binary input module was able to withstand up to ±4 kV surge. The binary input module was able to perform normally after each test. Because functionality could not be verified during the test, the result was noted as passing with Class B.

表 49. Surge Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
Surge, DM	IEC 61000-4-5: (1.2 / 50 µs–8 / 20 µs), 42 Ω–0.5 µF	Binary input signal line	± 4 kV	Pass , Criteria B (After the test the Module continued to operate as intended)

表 50. Surge Test Steps

TEST NO	TEST MODE	OBSERVATION
1	1.0 kV	Pass
2	–1.0 kV	Pass
3	2.0 kV	Pass
4	–2.0 kV	Pass
5	4.0 kV	Pass
6	–4.0 kV	Pass

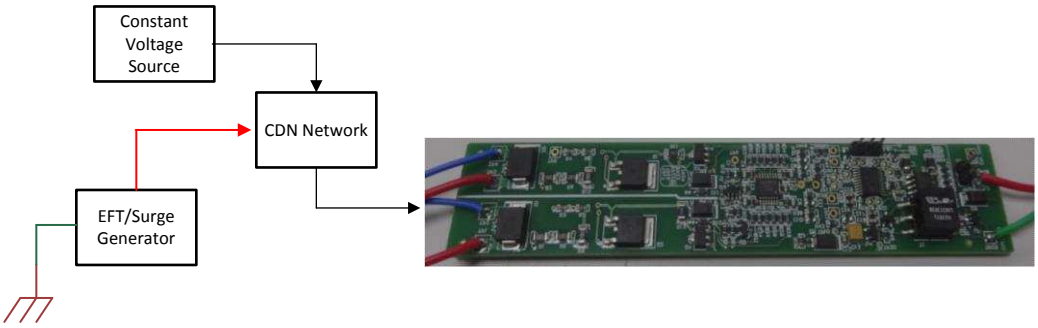


図 19. Surge Setup for Binary Input Module With BI Digital Isolator

4.2.4 IEC Pre-Compliance Testing—Digital Isolator ISO7320 With BI

The following tests were done for the ISO7320C and ISO7320FC devices.

4.2.4.1 IEC61000-4-2 ESD Test

The IEC610004-2 ESD test simulates the electrostatic discharge of an operator directly onto an adjacent electronic component. An electrostatic charge usually develops in low relative humidity, and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the binary input module, which can happen through direct contact with the binary input module (contact discharge), or through an air-gap (air-discharge). This was applied across signal inputs only. A series of 10 negative and positive pulses were applied directly on the binary inputs during the test (contact discharge). After the test, the binary module was verified for functionality. The test results show the binary input module was able to withstand the required discharge. The binary input module was not permanently damaged.

表 51. ESD Test Steps

TEST NO	TEST MODE	OBSERVATION
1	Contact 2 kV	Pass
2	Contact –2 kV	Pass
3	Contact 4 kV	Pass
4	Contact –4 kV	Pass
5	Contact 6 kV	Pass
6	Contact –6 kV	Pass
7	Contact 8 kV	Pass
8	Contact –8 kV	Pass

表 52. ESD Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
ESD	IEC 61000-4-2, contact	Binary input	±4 kV	Pass, Criteria B (After the test, the module continued to operate as intended.)

注: The ISO7320 can be used with ESD requirements up to 6 kV although these tests confirm that the device performs without failure for a higher ESD level.

4.2.4.2 IEC61000-4-4 EFT Test

The burst signal is injected on the voltage inputs. The test is carried out with the binary input module placed 10 cm above the reference plate. After the test, the binary module was verified for functionality. The test results show the binary input module was able to withstand up to ±2 kV. The binary input module was able to perform normally after each test. Because functionality could not be verified during the test, the result was noted as passing Class B.

The EFT burst at I/O connectors and the performance criteria expected are as follows:

表 53. EFT Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
EFT	IEC61000-4-4, ±2 kV on binary input	Input lines	± 2 kV	Pass, Criteria B (After the test, the module continued to operate as intended.)

表 54. Test Results Steps and Observations for EFT Testing

TEST NO	TEST MODE	OBSERVATION
1	0.5 kV, 5 kHz	Pass
2	–0.5 kV, 5 kHz	Pass
3	1 kV, 5 kHz	Pass
4	–1 kV, 5 kHz	Pass
7	2 kV, 5 kHz	Pass
8	–2 kV, 5 kHz	Pass

4.2.4.3 IEC61000-4-5 Surge Test

The IEC61000-4-5 surge test simulates switching transients caused by lightning strikes or the switching of power systems including load changes and short circuits. The test requires five positive and five negative surge pulses with a time interval between successive pulses of 1 minute or less. The unshielded symmetrical data line setup as defined by the IEC61000-4-5 specification was used for this test. The test generator was configured for 1.2/50-µs surges and diode clamps were used for line-to-ground coupling. A series of five negative and positive pulses, with 10 seconds spacing between each pulse, were applied during the test.

After the test, the binary module was verified for functionality. The test results show the binary input module was able to withstand up to ±4 kV surge. The binary input module was able to perform normally after each test. Because functionality could not be verified during the test, the result was noted as passing with Class B.

表 55. Surge Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
Surge, DM	IEC 61000-4-5: (1.2/50 µs to 8/20 µs), 42 Ω–0.5 µF	Binary input signal line	± 4 kV	Pass, Criteria B (After the test, the module continued to operate as intended.)

表 56. Surge Test Steps

TEST NO	TEST MODE	OBSERVATION
1	1.0 kV	Pass
2	–1.0 kV	Pass
3	2.0 kV	Pass
4	–2.0 kV	Pass
5	4.0 kV	Pass
6	–4.0 kV	Pass

4.2.5 IEC Pre-Compliance Testing—Digital Isolator ISO7820 With RI

The following tests were done for the ISO7520CDW, ISO7820, and ISO7820F devices.

4.2.5.1 IEC61000-4-2 ESD Test

The IEC610004-2 ESD test simulates the electrostatic discharge of an operator directly onto an adjacent electronic component. An electrostatic charge usually develops in low relative humidity, and on low-conductivity carpets, or vinyl garments. To simulate a discharge event, an ESD generator applies ESD pulses to the binary input module, which can happen through direct contact with the binary input module (contact discharge), or through an air-gap (air-discharge). This was applied across signal inputs only. A series of 10 negative and positive pulses were applied directly on the binary inputs during the test (contact discharge). After the test, the binary module was verified for functionality. The test results show the binary input module was able to withstand the required discharge. The binary input module was not permanently damaged.

表 57. ESD Test Steps

TEST NO	TEST MODE	OBSERVATION
1	Contact 2 kV	Pass
2	Contact –2 kV	Pass
3	Contact 4 kV	Pass
4	Contact –4 kV	Pass
5	Contact 8 kV	Pass
6	Contact –8 kV	Pass

表 58. ESD Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
ESD	IEC 61000-4-2, contact	Signal lines	±8 kV	Pass, Criteria B (After the test, the module continued to operate as intended.)

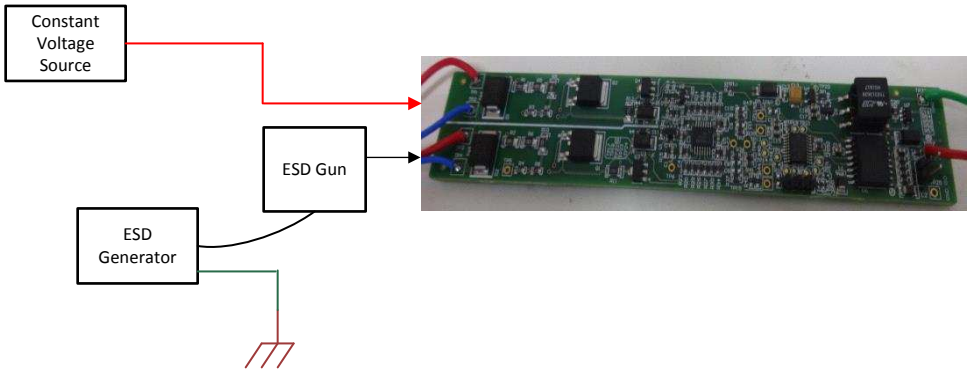


図 20. ESD Setup for Binary Input Module With RI

4.2.5.2 IEC61000-4-4 EFT Test

The EFT burst at I/O connectors and the performance criteria expected are as follows:

表 59. EFT Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
EFT	IEC61000-4-4, ±2 KV on binary input	Input lines	± 2 kV	Pass, Criteria B (After the test, the module continued to operate as intended.)

表 60. Test Results Steps and Observations for EFT Testing

TEST NO	TEST MODE	OBSERVATION
1	0.5 kV , 5 kHz	Pass
2	–0.5 kV , 5 kHz	Pass
3	1 kV , 5 kHz	Pass
4	–1 kV , 5 kHz	Pass
7	2 kV , 5 kHz	Pass
8	–2 kV , 5 kHz	Pass

The burst signal is injected on the voltage inputs. The test is carried out with the binary input module placed 10 cm above the reference plate. After the test, the binary module was verified for functionality. The test results show the binary input module was able to withstand up to ±2 kV. The binary input module was able to perform normally after each test. Because functionality could not be verified during the test, the result was noted as passing Class B.

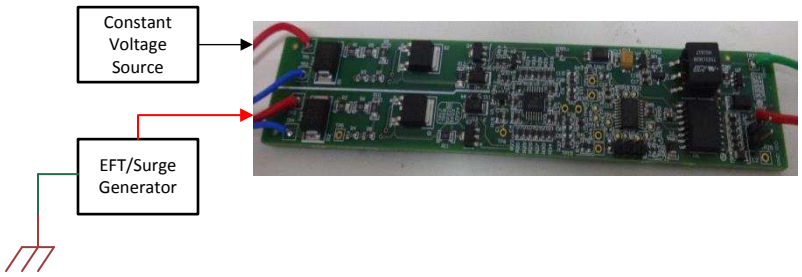


図 21. EFT Setup for Binary Input Module With RI

4.2.5.3 IEC61000-4-5 Surge Test

The IEC61000-4-5 surge test simulates switching transients caused by lightning strikes or the switching of power systems including load changes and short circuits. The test requires five positive and five negative surge pulses with a time interval between successive pulses of 1 minute or less. The unshielded symmetrical data line setup as defined by the IEC61000-4-5 specification was used for this test. The test generator was configured for 1.2/50-µs surges and diode clamps were used for line-to-ground coupling. A series of five negative and positive pulses, with 10 seconds spacing between each pulse, were applied during the test.

After the test, the binary module was verified for functionality. The test results show the binary input module was able to withstand up to ±4 kV surge. The binary input module was able to perform normally after each test. Because functionality could not be verified during the test, the result was noted as passing with Class B.

表 61. Surge Test Observations

IMMUNITY TEST	STANDARD	PORT	TARGET VOLTAGE	RESULT
Surge, DM	IEC 61000-4-5: (1.2/50 µs to 8/20 µs), 42 Ω to 0.5 µF	Binary input signal line	±4 kV	Pass, Criteria B (After the test, the module continued to operate as intended.)

表 62. Surge Test Steps

TEST NO	TEST MODE	OBSERVATION
1	1.0 kV	Pass
2	–1.0 kV	Pass
3	2.0 kV	Pass
4	–2.0 kV	Pass
5	4.0 kV	Pass
6	–4.0 kV	Pass

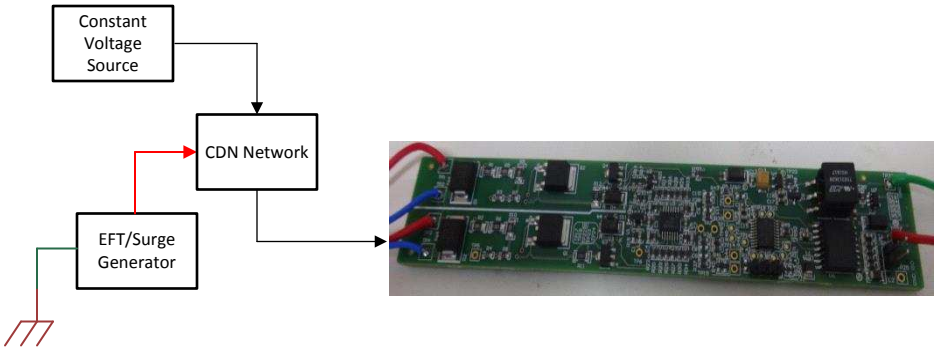


図 22. Surge Setup for Binary Input Module With RI

4.2.6 Summary

表 63. Test Results Summary for AC/DC Binary Input Module—BI and RI

TEST	OBSERVATION
Power supply: Binary module with BI and RI	OK
Measurement of AC/DC voltage input with BI and RI digital isolators	OK
AC/DC input voltage measurement accuracy	< ±3% ± 1 V
EMC pre-compliance (ESD, EFT, Surge) testing for the binary input module with BI	OK
EMC pre-compliance (ESD, EFT, Surge) testing for the binary input module with RI	OK

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00809.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00809.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00809.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00809.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00809.

6 References

1. Texas Instruments, *MSP430™ Programming With the JTAG Interface*, User's Guide (SLAU320)
2. Texas Instruments, *Digitally Isolated 2-Channel, Wide AC/DC Binary Input Module*, TIDA-00490 Design Guide (TIDU857)

6.1 商標

7 Terminology

BI— Basic insulation

RI— Reinforced insulation

8 About the Author

KALLIKUPPA MUNIYAPPA SREENIVASA is a systems architect at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Sreenivasa brings to this role his experience in high-speed digital and analog systems design. Sreenivasa earned his bachelor of electronics (BE) in electronics and communication engineering (BE-E&C) from VTU, Mysore, India.

リビジョンAの改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年7月発行のものから更新 **Page**

- プレビュー・ページから 変更 1
- タイトルを「広いAC/DC入力に対応したEMC準拠、グループ絶縁、2チャネルのバイナリ入力モジュールのリファレンス・デザイン」から 変更 1
- 「特長」の「1Vより良好な測定分解能」を 削除 1
- 「アプリケーション」に「PLCデジタル入力モジュール」を 追加 1
- measurement resolution range limit from 270-V AC/DC to 264-V AC/DC 変更 9
- electrical isolation level from >2 kV_{RMS} to 5700 V_{RMS} 変更 9
- note under 図 9 追加 24
- note under 図 10 追加 25
- target voltage in ESD test from ±8 kV to ±4 kV 変更 44
- target voltage in ESD test from ±8 kV to ±6 kV 変更 47

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