

# TXB0304 自動方向検出機能搭載 4 ビット双方向レベル・シフタ/電圧トランスレータ

## 1 特長

- 完全に対称な電源電圧：A ポートで 0.9V~3.6V、B ポートで 0.9V~3.6V
- $V_{CC}$  絶縁機能：どちらかの  $V_{CC}$  入力が GND レベルになると、すべての出力が高インピーダンス状態になる
- $V_{CCA}$  を基準とする出カインエーブル (OE) 入力回路
- 低消費電力：5 $\mu$ A 以下 ( $I_{CCA}$ 、 $I_{CCB}$ )
- $I_{off}$ により部分的パワーダウン・モードをサポート
- JESD 78、Class II準拠で100mA超のラッチアップ性能
- JESD 22を超えるESD保護
  - 8000V、人体モデル (A114-B)
  - 1000V、荷電デバイス・モデル (C101)

## 2 アプリケーション

- パーソナル・エレクトロニクス
- 産業用
- エンタープライズ
- 通信機器

## 3 概要

この4ビット非反転トランスレータは、設定可能な2つの独立した電源レールを採用しています。Aポートは $V_{CCA}$ に追従する設計で、 $V_{CCA}$ は0.9V~3.6Vの電源電圧に対応します。Bポートは $V_{CCB}$ に追従する設計で、 $V_{CCB}$ は0.9V~3.6Vの電源電圧に対応します。このため、1V、1.2V、1.5V、1.8V、2.5V、3.3Vの任意の電圧ノード間での低電圧双方向変換が可能です。

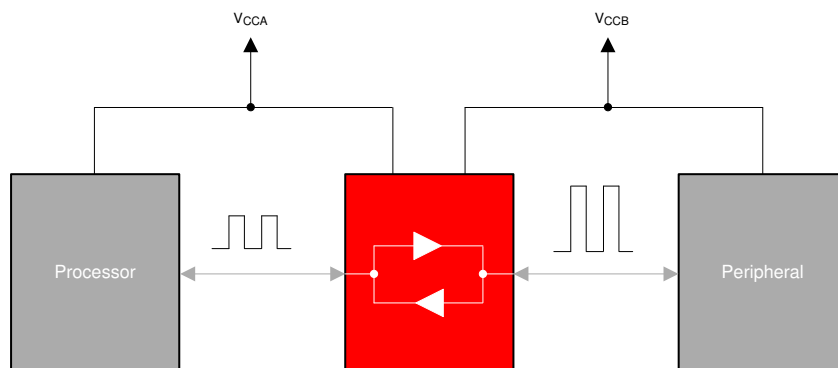
TXB0304の場合、出カインエーブル (OE) 入力が Low のとき、全出力が高インピーダンス状態になります。電源オンまたは電源オフ時に確実に高インピーダンス状態になるように、プルダウン抵抗を介して OE を GND に接続する必要があります。この抵抗の最小値は、ドライバの電流ソース能力によって決定します。OE デバイス制御ピンの入力回路は、 $V_{CCA}$  から電力供給されます。このデバイスは、 $I_{off}$ を使用する部分的パワーダウン・アプリケーション用に完全に動作が規定されています。 $I_{off}$ 回路が出力をディセーブルにするため、電源切断時にデバイスに電流が逆流して損傷に至ることを回避できます。TXB0304 と TXBN0304 の唯一の違いは、前者は OE 信号がアクティブ High であり、後者は OE 信号がアクティブ Low であることです。

### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ (公称)
TXB0304	RUT UQFN (12)	2.00mm x 1.70mm
	RSV UQFN (16)	2.60mm x 1.80mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

### TXB0304 の代表的なアプリケーション・ブロック図



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## 目次

1	特長 .....	1	8.2	Functional Block Diagram .....	10
2	アプリケーション .....	1	8.3	Feature Description .....	11
3	概要 .....	1	8.4	Device Functional Modes .....	11
4	改訂履歴 .....	2	<b>9</b>	<b>Application and Implementation</b> .....	<b>12</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	9.1	Application Information .....	12
<b>6</b>	<b>Specifications</b> .....	<b>4</b>	9.2	Typical Application .....	12
6.1	Absolute Maximum Ratings .....	4	<b>10</b>	<b>Power Supply Recommendations</b> .....	<b>13</b>
6.2	ESD Ratings .....	4	<b>11</b>	<b>Layout</b> .....	<b>13</b>
6.3	Recommended Operating Conditions .....	4	11.1	Layout Guidelines .....	13
6.4	Thermal Information .....	5	11.2	Layout Example .....	14
6.5	Electrical Characteristics .....	5	<b>12</b>	<b>デバイスおよびドキュメントのサポート</b> .....	<b>15</b>
6.6	Timing Requirements .....	6	12.1	デバイス・サポート .....	15
6.7	Switching Characteristics .....	6	12.2	ドキュメントのサポート .....	15
6.8	Operating Characteristics .....	7	12.3	コミュニティ・リソース .....	15
6.9	Typical Characteristics .....	7	12.4	商標 .....	15
<b>7</b>	<b>Parameter Measurement Information</b> .....	<b>8</b>	12.5	静電気放電に関する注意事項 .....	15
<b>8</b>	<b>Detailed Description</b> .....	<b>10</b>	12.6	Glossary .....	15
8.1	Overview .....	10	<b>13</b>	<b>メカニカル、パッケージ、および注文情報</b> .....	<b>15</b>

## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (May 2016) から Revision G に変更	Page
• Changed text in <a href="#">Power Supply Recommendations</a> section. ....	13

Revision E (August 2014) から Revision F に変更	Page
• 「 <a href="#">概要</a> 」セクションを変更 .....	1
• 「 <a href="#">Absolute Maximum Ratings</a> 」、「 <a href="#">Recommended Operating Conditions<sup>(1)(2)</sup></a> 」、「 <a href="#">Switching Characteristics</a> 」、「 <a href="#">Electrical Characteristics</a> 」の各表を変更。 .....	1

Revision D (October 2012) から Revision E に変更	Page
• 「 <a href="#">ESD 定格</a> 」表、「 <a href="#">機能説明</a> 」セクション、「 <a href="#">デバイスの機能モード</a> 」セクション、「 <a href="#">アプリケーションと実装</a> 」セクション、「 <a href="#">電源に関する推奨事項</a> 」セクション、「 <a href="#">レイアウト</a> 」セクション、「 <a href="#">デバイスおよびドキュメントのサポート</a> 」セクション、「 <a href="#">メカニカル、パッケージ、および注文情報</a> 」セクション 追加 .....	1
• Changed VCCA and VCCB in the ABS MAX table to V <sub>CCA</sub> and V <sub>CCB</sub> in 3 places .....	4
• Changed in ELEC CHARAC table the 0.9 x V <sub>CCA</sub> and 0.9 x V <sub>CCB</sub> from MAX column into the MIN column .....	5
• Changed in ELEC CHARAC table 0.2 (2 places) in the MIN column to the MAX .....	5

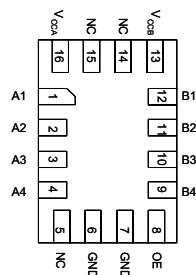
Revision C (May 2012) から Revision D に変更	Page
• Added <a href="#">Application Information</a> section .....	12

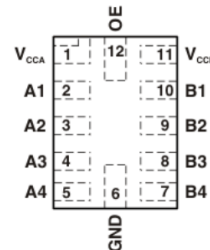
Revision B (September 2011) から Revision C に変更	Page
• Added package pin out diagram notes. ....	3

## 5 Pin Configuration and Functions

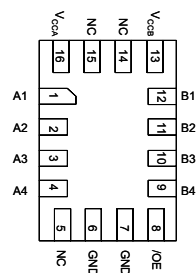
**RSV Package  
16-Pin UQFN  
TXB0304 Top View**



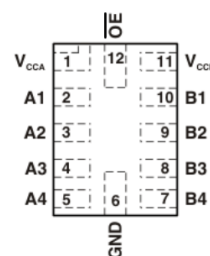
**RUT Package  
12-Pin UQFN  
TXB0304 Top View**



**RSV Package  
16-Pin UQFN  
TXBN0304 Top View**



**RUT Package  
12-Pin UQFN  
TXBN0304 Top View**



A. See [Layout Guidelines](#) for notes about package pin out diagrams.

### Pin Functions

NAME	PIN		TYPE	DESCRIPTION			
	TXB0304	TXBN0304					
	RSV	RUT	RSV	RUT			
A1	1	2	1	2	I/O	Input/output 1	Referenced to $V_{CCA}$
A2	2	3	2	3	I/O	Input/output 2	
A3	3	4	3	4	I/O	Input/output 3	
A4	4	5	4	5	I/O	Input/output 4	
B1	12	10	12	10	I/O	Input/output 4	Referenced to $V_{CCB}$
B2	11	9	11	9	I/O	Input/output 3	
B3	10	8	10	8	I/O	Input/output 2	
B4	9	7	9	7	I/O	Input/output 1	
GND	6, 7	6	6,7	6	GND	Ground	
NC	5, 14, 15	—	5, 14, 15	—	—	No connection; not internally connected	
OE	8	12	—	—	I	3-state output-mode enable. Pull OE (TXB0304) low to place all outputs in 3-state mode. Referenced to $V_{CCA}$ .	
$\overline{OE}$	—	—	8	12	I	3-state output-mode enable. Pull $\overline{OE}$ (TXBN0304) high to place all outputs in 3-state mode. Referenced to $V_{CCA}$ .	
$V_{CCA}$	16	1	16	1	—	A-port supply voltage $0.9\text{ V} \leq V_{CCA} \leq 3.6\text{ V}$	
$V_{CCB}$	13	11	13	11	—	B-port supply voltage $0.9\text{ V} \leq V_{CCB} \leq 3.6\text{ V}$	

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

			MIN	MAX	UNIT
$V_{CCA}$	Supply voltage		-0.5	4.6	V
$V_{CCB}$			-0.5	4.6	
$V_I$	Input voltage	A port	-0.5	4.6	V
		B port	-0.5	4.6	
$V_O$	Voltage applied to any output in the high-impedance or power-off state	A port	-0.5	4.6	V
		B port	-0.5	4.6	
$V_O$	Voltage applied to any output in the high or low state <sup>(2)</sup>	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current	$V_I < 0$		-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50	mA
$I_O$	Continuous output current			±50	mA
	Continuous current through $V_{CCA}$ , $V_{CCB}$ , or GND			±100	mA
$T_{stg}$	Storage temperature		-65	150	°C
$T_J$	Junction temperature		-40	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The value of  $V_{CCA}$  and  $V_{CCB}$  are provided in the recommended operating conditions table.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions <sup>(1)(2)</sup>

			$V_{CCA}$	$V_{CCB}$	MIN	MAX	UNIT
$V_{CCA}$	Supply voltage				0.9	3.6	V
$V_{CCB}$							
$V_{IH}$	High-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	$V_{CCI} \times 0.65$	$V_{CCI}$	V
		OE/ $\overline{OE}$	0.9 V to 3.6 V	0.9 V to 3.6 V	$V_{CCA} \times 0.65$	3.6	
$V_{IL}$	Low-level input voltage	Data inputs	0.9 V to 3.6 V	0.9 V to 3.6 V	0	$V_{CCI} \times 0.35$	V
		OE/ $\overline{OE}$	0.9 V to 1.2 V	0.9 V to 3.6 V	0	$V_{CCA} \times 0.3$	
			1.2 V to 3.6 V	0.9 V to 3.6 V	0	$V_{CCA} \times 0.35$	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state	A-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	V
		B-port	0.9 V to 3.6 V	0.9 V to 3.6 V	0	3.6	
$\Delta t/\Delta v$	Input transition rise or fall rate	A-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	ns/V
		B-port inputs	0.9 V to 3.6 V	0.9 V to 3.6 V		40	
$T_A$	Operating free-air temperature				-40	85	°C

- (1) The A and B sides of an unused data I/O pair must be held in the same state, such as, both at  $V_{CCI}$  or both at GND.
- (2)  $V_{CCI}$  is the supply voltage associated with the input port.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TXB0304		UNIT
		RUT (UQFN)	RSV (UQFN)	
		12 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.4	131.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	55.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.9	55.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.6	1.4	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	46.9	55.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		$V_{CCA}$	$V_{CCB}$	MIN	TYP	MAX	UNIT
$V_{OHA}$	High-level output voltage	$I_{OH} = -20 \mu A$	$T_A = 25^\circ C$	0.9 V to 3.6 V		$0.9 \times V_{CCA}$			V
$V_{OLA}$	Low-level output voltage	$I_{OL} = 20 \mu A$	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V				0.2	V
$V_{OHB}$	High-level output voltage	$I_{OH} = -20 \mu A$	$T_A = 25^\circ C$		0.9 V to 3.6 V	$0.9 \times V_{CCB}$			V
$V_{OLB}$	Low-level output voltage	$I_{OL} = 20 \mu A$	$-40^\circ C$ to $85^\circ C$		0.9 V to 3.6 V			0.2	V
$I_I$	OE	$V_I = V_{CCI}$ or GND	$T_A = 25^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			$\pm 1$	$\mu A$
			$-40^\circ C$ to $85^\circ C$					$\pm 2$	
$I_{off}$	A port	$V_I$ or $V_O = 0$ to 3.6 V	$T_A = 25^\circ C$	0 V	0 V to 3.6 V			$\pm 1$	$\mu A$
	B port		$-40^\circ C$ to $85^\circ C$					$\pm 2$	
$I_{OZ}$		A or B port	OE = GND	$T_A = 25^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			
	$-40^\circ C$ to $85^\circ C$			$\pm 2$					
$I_{CCA}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			5	$\mu A$
$I_{CCB}$		$V_I = V_{CCB}$ or GND, $I_O = 0$	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			5	$\mu A$
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			10	$\mu A$
$I_{CCZA}$	High-Z state supply current	$V_I = V_{CCI}$ or GND, $I_O = 0$ , OE = GND	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			5	$\mu A$
$I_{CCZB}$	High-Z state supply current	$V_I = V_{CCB}$ or GND, $I_O = 0$ , OE = GND	$-40^\circ C$ to $85^\circ C$	0.9 V to 3.6 V	0.9 V to 3.6 V			5	$\mu A$
$C_i$	OE	$T_A = 25^\circ C$		0.9 V to 3.6 V	0.9 V to 3.6 V			3	pF
$C_{io}$	A port	$T_A = 25^\circ C$ , OE = GND		0.9 V to 3.6 V	0.9 V to 3.6 V			6.7	pF
	B port					6.7			

## 6.6 Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	LOAD	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	MAX	UNIT
Data rate	C <sub>L</sub> = 15 pF	0.9 to 3.6 V	0.9 to 3.6 V		50	Mbps
	C <sub>L</sub> = 15 pF	1.2 to 3.6 V	1.2 to 3.6 V		100	Mbps
	C <sub>L</sub> = 15 pF	1.8 to 3.6 V	1.8 to 3.6 V		140	Mbps
	C <sub>L</sub> = 30 pF	0.9 to 3.6 V	0.9 to 3.6 V		40	Mbps
	C <sub>L</sub> = 30 pF	1.2 to 3.6 V	1.2 to 3.6 V		90	Mbps
	C <sub>L</sub> = 30 pF	1.8 to 3.6 V	1.8 to 3.6 V		130	Mbps
	C <sub>L</sub> = 50 pF	1.2 to 3.6 V	1.2 to 3.6 V		80	Mbps
	C <sub>L</sub> = 50 pF	1.8 to 3.6 V	1.8 to 3.6 V		120	Mbps
	C <sub>L</sub> = 100 pF	1.2 to 3.6 V	1.2 to 3.6 V		70	Mbps
C <sub>L</sub> = 100 pF	1.8 to 3.6 V	1.8 to 3.6 V		100	Mbps	

## 6.7 Switching Characteristics

 over operating free-air temperature range (unless otherwise noted). (For parameter descriptions, see [Figure 2](#) and [Figure 3](#).)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD	V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>pd</sub>	A	B	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	A	B	C <sub>L</sub> = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	A	B	C <sub>L</sub> = 15	1.8-3.6	1.8-3.6		3.7	4.8	
	A	B	C <sub>L</sub> = 30	0.9-3.6	0.9-3.6		19.5	34	
	A	B	C <sub>L</sub> = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	A	B	C <sub>L</sub> = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	A	B	C <sub>L</sub> = 50	1.2-3.6	1.2-3.6		8	12.3	
	A	B	C <sub>L</sub> = 50	1.8-3.6	1.8-3.6		4	5.4	
	A	B	C <sub>L</sub> = 100	1.2-3.6	1.2-3.6		8.6	13.5	
	B	A	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		18.9	30	ns
	B	A	C <sub>L</sub> = 15	1.2-3.6	1.2-3.6		7.5	11.5	
	B	A	C <sub>L</sub> = 15	1.8-3.6	1.8-3.6		3.7	5	
	B	A	C <sub>L</sub> = 30	0.9-3.6	0.9-3.6		19.5	34	
	B	A	C <sub>L</sub> = 30	1.2-3.6	1.2-3.6		7.8	11.9	
	B	A	C <sub>L</sub> = 30	1.8-3.6	1.8-3.6		3.8	5.2	
	B	A	C <sub>L</sub> = 50	1.2-3.6	1.2-3.6		8	12.3	
	B	A	C <sub>L</sub> = 50	1.8-3.6	1.8-3.6		4	5.4	
	B	A	C <sub>L</sub> = 100	1.2-3.6	1.2-3.6		8.6	13.5	
t <sub>en</sub>	OE	A	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6			262	ns
				1.2-3.6	1.2-3.6			64	
				1.8-3.6	1.8-3.6			37	
		B	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6			332	
				1.2-3.6	1.2-3.6			76	
				1.8-3.6	1.8-3.6			41	
t <sub>dis</sub>	OE	A	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6			172	ns
		B	C <sub>L</sub> = 15	0.9-3.6	0.9-3.6			169	ns
t <sub>FB</sub> , t <sub>FB</sub>	B-port rise and fall times		C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		2.95		ns
t <sub>SA</sub> , t <sub>SA</sub>	A-port rise and fall times		C <sub>L</sub> = 15	0.9-3.6	0.9-3.6		3.1		ns
t <sub>SK(O)</sub>	Channel-to-channel skew		C <sub>L</sub> = 15	0.9-3.6	0.9-3.6			0.15	ns

 (1) T<sub>A</sub> = 25°C

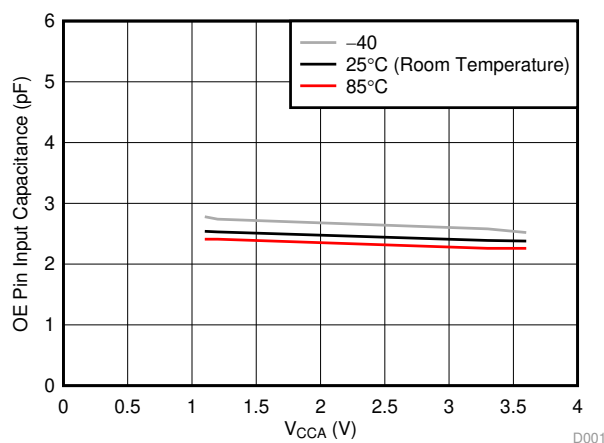
### 6.8 Operating Characteristics

$C_{pd}$  - power dissipation capacitance measured at  $T_A = 25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	TYP <sup>(1)</sup>	UNIT	
$C_{pdA}$	A-port input, B-port output	$C_L = 0$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$ , $OE = V_{CCA}$ (outputs enabled)	34	pF	
	B-port input, A-port output		34		
$C_{pdB}$	A-port input, B-port output		34	pF	
	B-port input, A-port output		34		
$C_{pdA}$	A-port input, B-port output		$C_L = 0$ , $f = 10\text{ MHz}$ , $t_r = t_f = 1\text{ ns}$ , $OE = \text{GND}$ (outputs disabled)	0.01	pF
	B-port input, A-port output			0.01	
$C_{pdB}$	A-port input, B-port output	0.01		pF	
	B-port input, A-port output	0.01			

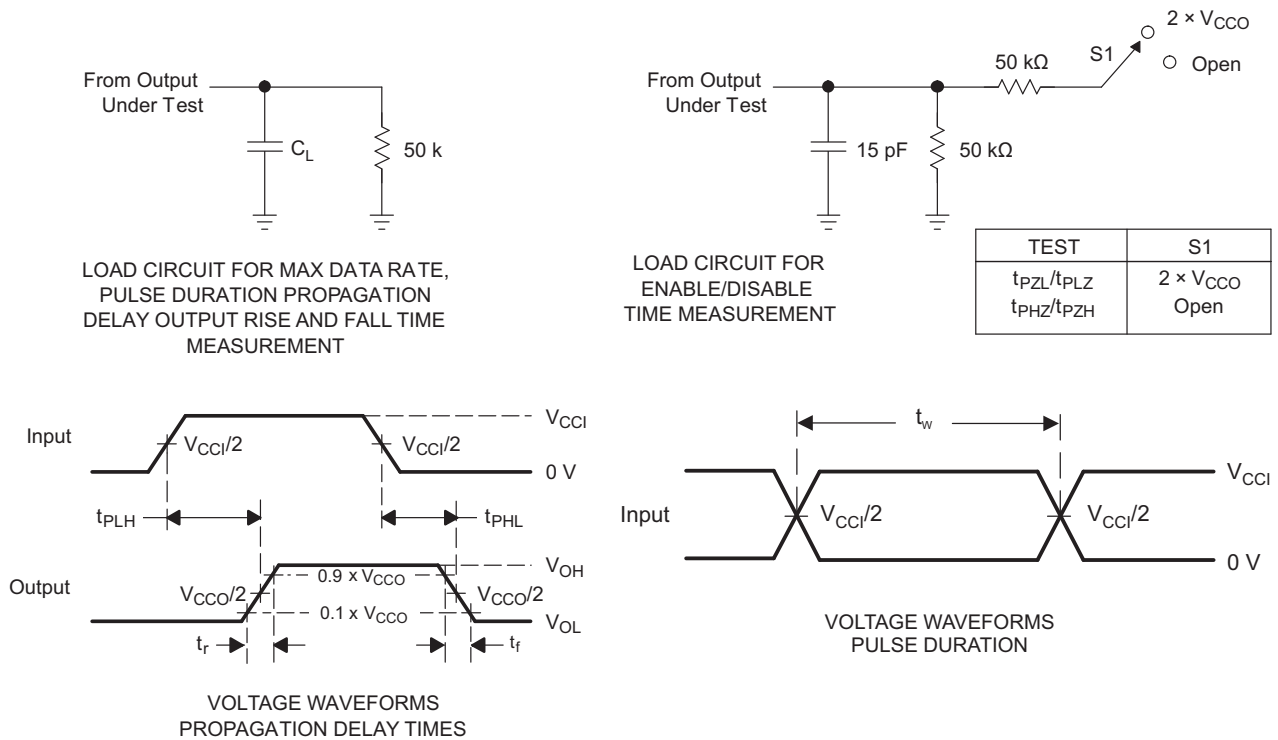
(1)  $V_{CCA}$ ,  $V_{CCB}$  0.9 V to 3.6 V

### 6.9 Typical Characteristics



**Figure 1. Input Capacitors for OE Pin ( $C_i$ ) vs Power Supply ( $V_{CCA}$ )**

## 7 Parameter Measurement Information

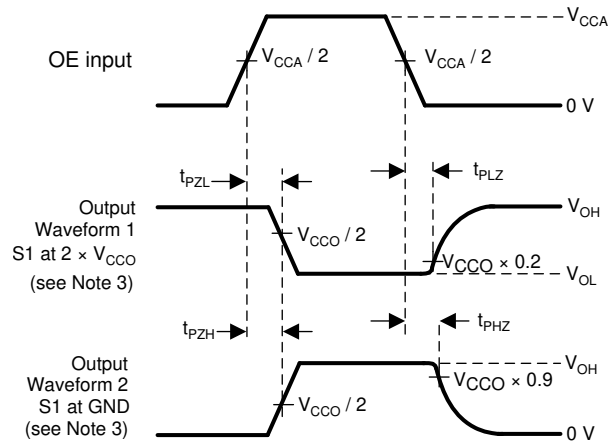


- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR 10 MHz,  $Z_0 = 50 \Omega$ ,  $dv/dt \geq 1$  V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- E.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
- F.  $V_{CCO}$  is the  $V_{CC}$  associated with output port.
- G. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuits and Voltage Waveforms**



**Parameter Measurement Information (continued)**



- (1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- (2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- (3) Waveform 1 is for an output with internal such that the output is high, except when OE is high. Waveform 2 is for an output with conditions such that the output is low, except when OE is high.

**Figure 3. Enable and Disable Times**

## 8 Detailed Description

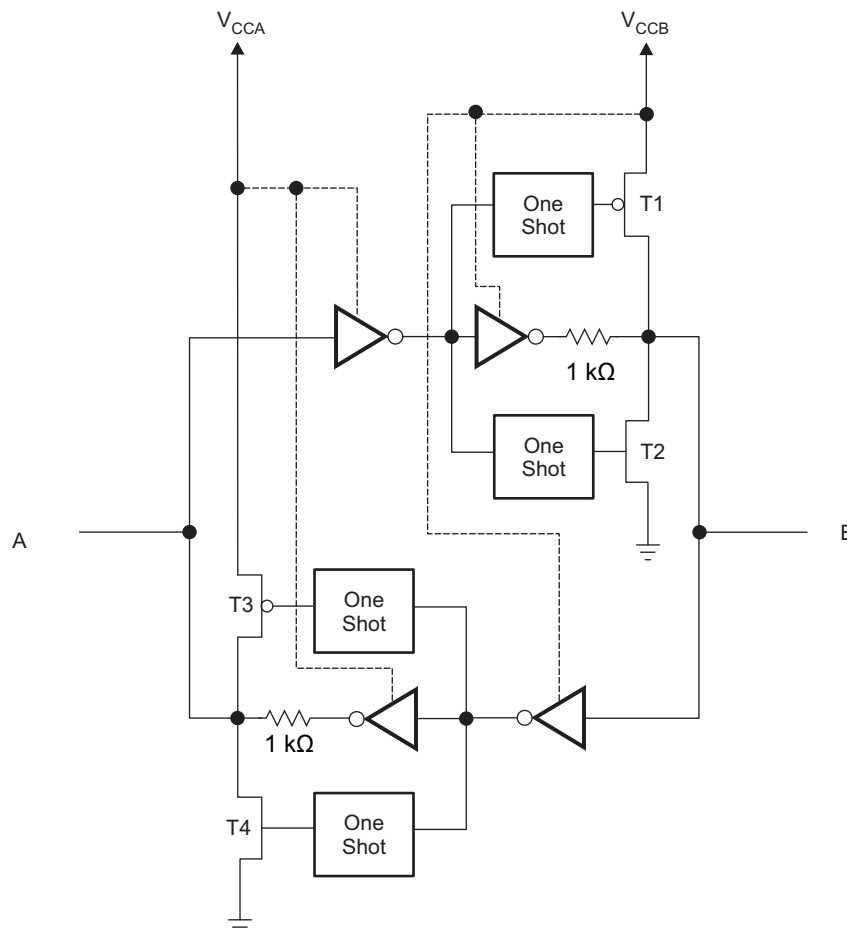
### 8.1 Overview

The TXB0304 and TXBN0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another.

#### 8.1.1 Architecture

The TXB0304 and TXBN0304 architecture (see [Figure 4](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a dc state, the output drivers of the TXB0304 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction. The output one shots detect rising or falling edges on the A or B ports. During a rising edge, the one shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is  $30\ \Omega$  at  $V_{CCO} = 0.9\ \text{V}$  to  $1\ \text{V}$ ,  $10\ \Omega$  at  $V_{CCO} = 1.1\ \text{V}$  to  $1.7\ \text{V}$ , and  $5\ \Omega$  at  $V_{CCO} = 1.8\ \text{V}$  to  $3.3\ \text{V}$ .

### 8.2 Functional Block Diagram



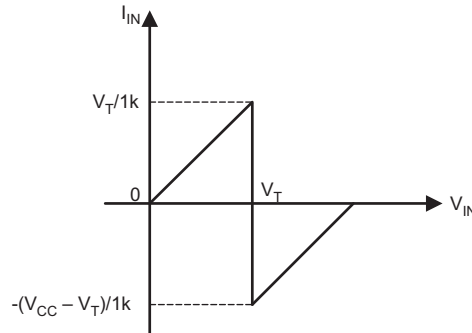
Copyright © 2016, Texas Instruments Incorporated

**Figure 4. Architecture of TXB0304 I/O Cell**

### 8.3 Feature Description

#### 8.3.1 Input Driver Requirements

Typical  $I_{IN}$  vs  $V_{IN}$  characteristics of the TXB0304/TXBN0304 are shown in Figure 5. For proper operation, the device driving the data I/Os of the TXB0304 must have drive strength of at least  $\pm 3$  mA.



- (1)  $V_{CC}$  is power supply of TXB0304.
- (2)  $V_T$  is the input threshold voltage of TXB0304 (typically it is  $V_{CC}/2$ ).

**Figure 5. Typical  $I_{IN}$  vs  $V_{IN}$  Curve**

### 8.4 Device Functional Modes

#### 8.4.1 Enable and Disable

The TXB0304 has an OE input that is used to disable the device by setting OE = low ( $\overline{OE}$  = high for TXBN0304), which places all I/Os in the high-impedance (Hi-Z) state. The disable time ( $t_{dis}$ ) indicates the delay between when OE goes low and when the outputs actually get disabled (Hi-Z). The enable time ( $t_{en}$ ) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is high.

#### 8.4.2 Pullup or Pulldown Resistor on I/O Lines

The TXB0304/TXBN0304 is designed to drive capacitive loads of up to 100 pF. The output drivers of the TXB0304 have low dc drive strength. If pull-up or pull-down resistors are connected externally to the data I/Os, their values must be kept higher than 20 k $\Omega$  to ensure that they do not contend with the output drivers of the TXB0304. but if the receiver is integrated with the smaller pull down or pull up resistor, below formula can be used for estimation to evaluate the  $V_{OH}$  and  $V_{OL}$ .

$$V_{ol} = V_{CCout} \times \frac{1.5k\Omega}{1.5k\Omega + R_{pu}} \tag{1}$$

$$V_{oh} = V_{CCout} \times \frac{R_{pd}}{1.5k\Omega + R_{pd}}$$

where

- $V_{CCOUT}$  is the output port supply voltage on either  $V_{CCA}$  or  $V_{CCB}$
- $R_{PD}$  is the value of the external pull down resistor
- $R_{PU}$  is the value of the external pull up resistor
- 1.5 k $\Omega$  is the counting the variation of the serial resistor 1k $\Omega$  in the I/O line. (2)

Because of this restriction on external resistors, the TXB0304 should not be used in applications such as I<sup>2</sup>C or 1-Wire where an open-drain driver is connected on the bidirectional data I/O. For these applications, use a device from the TI [TXS010X](#) series of level translators.

## 9 Application and Implementation

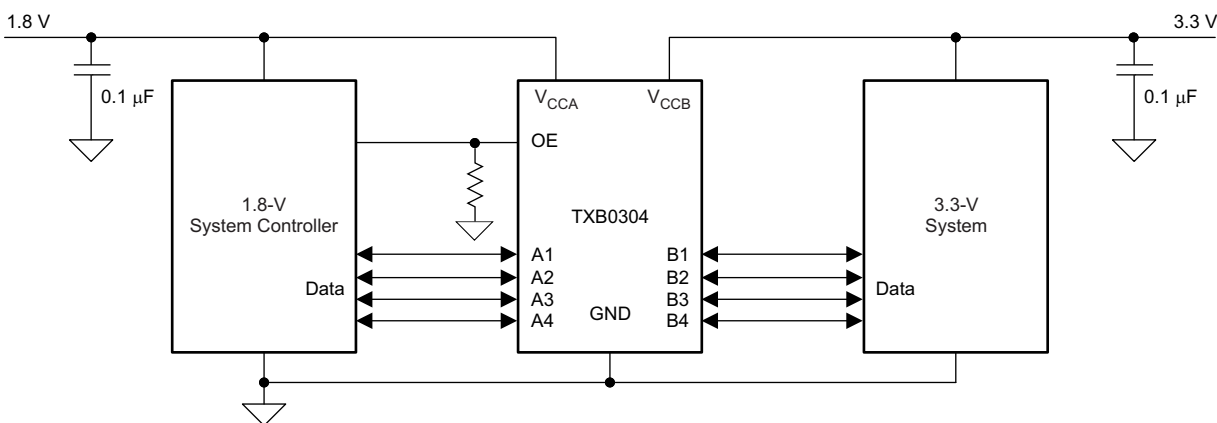
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TXB0304 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, please refer to TI [TXS010X](#) products. Any external pull-down or pull-up resistors are recommended larger than 20 k $\Omega$ .

### 9.2 Typical Application



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**Figure 6. Typical Application Schematic**

#### 9.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#).

**Table 1. Design Parameters**

DESIGN PARAMETERS	EXAMPLE VALUE
Input voltage range	0.9 V to 3.6 V
Output voltage range	0.9 V to 3.6 V

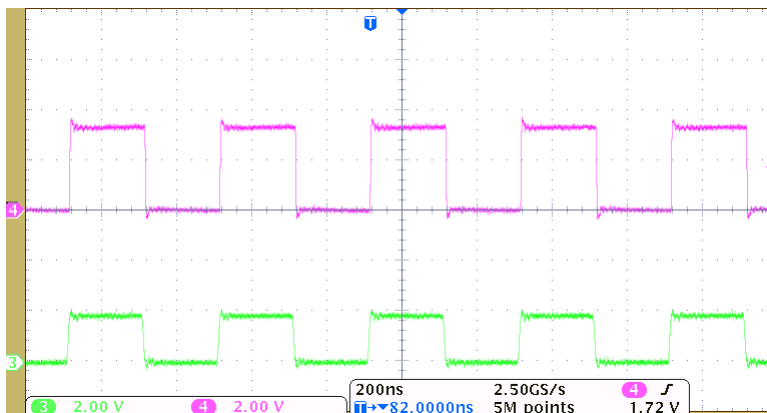
#### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0304 device to determine the input voltage range. For a valid logic high the value must exceed the  $V_{IH}$  of the input port. For a valid logic low the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXB0304 device is driving to determine the output voltage range.
  - Don't recommend to have the external pull-up or pull-down resistors. If mandatory, it is recommended the value should be larger than 20 k $\Omega$ .

- An external pull-down or pull-up resistor decreases the output  $V_{OH}$  and  $V_{OL}$ . Use the below equations in section 8.5.2 to draft estimate the  $V_{OH}$  and  $V_{OL}$  as a result of an external pull-down and pull-up resistor.

### 9.2.3 Application Curve



**Figure 7. Level-Translation of a 2.5-MHz Signal**

## 10 Power Supply Recommendations

During operation, TXB0304 can work at both  $V_{CCA} \leq V_{CCB}$  and  $V_{CCA} \geq V_{CCB}$ . During power-up sequencing, any power supply can be ramped up first. Both the supplies are recommended to be powered down together. The TXB0304 has circuitry that disables all input/output ports when either VCC is switched off ( $V_{CCA/B} = 0$  V).

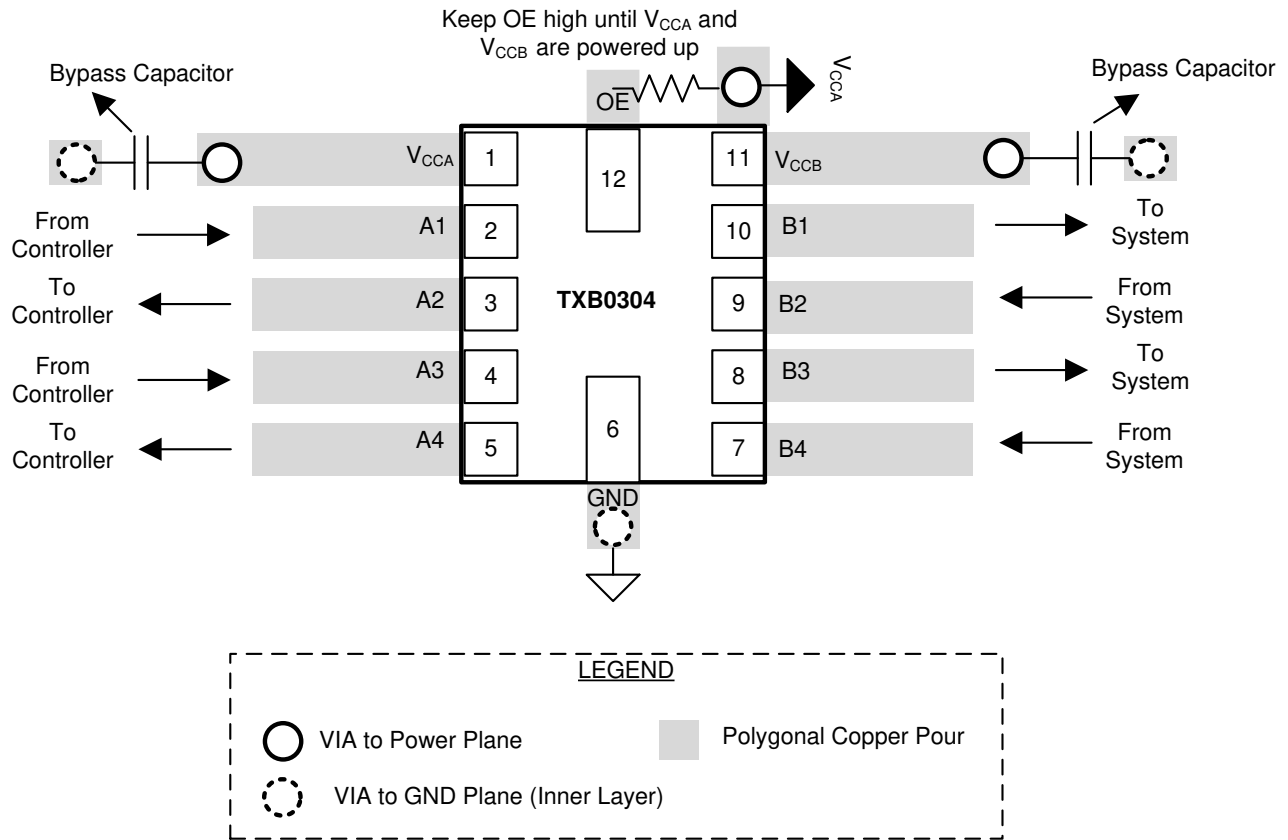
## 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. And should be placed as close as possible to the  $V_{CCA}$ ,  $V_{CCB}$  pin and GND pin
- Short trace-lengths should be used to avoid excessive loading.
- For long transmission lines, place a series resistor equivalent to the impedance of the transmission lines to avoid signal integrity issues
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.
- Pullup resistors are not required on both sides for Logic I/O.
- If pullup or pulldown resistors are needed, the resistor value must be over 20 k $\Omega$ .
- 20 k $\Omega$  is a safe recommended value, if the customer can accept higher  $V_{ol}$  or lower  $V_{oh}$ , smaller pull up or pull down resistor is allowed, the draft estimation is  $V_{ol} = V_{ccout} \times 1.5k / (1.5k + R_{pu})$  and  $V_{oh} = V_{ccout} \times R_{pd} / (1.5k + R_{pd})$ .
- If pullup resistors are needed, please refer to the TXS0104 or contact TI.
- For detailed information, refer to application note [SCEA043](#).

### 11.2 Layout Example



**Figure 8. TXB0304 PCB Layout**

## 12 デバイスおよびドキュメントのサポート

### 12.1 デバイス・サポート

#### 12.1.1 開発サポート

TI TXS010X 製品については、[www.ti.com/product/txs0101](http://www.ti.com/product/txs0101) を参照してください。

TXB0304 IBIS モデルについては、[SCEM544](#) を参照してください。

### 12.2 ドキュメントのサポート

#### 12.2.1 関連資料

関連資料については、以下を参照してください。

- アプリケーション・レポート、『*A Guide to Voltage Translation With TXB-Type Translators*』(英語)、[SCEA043](#)
- ユーザー・ガイド、『*TXB0304 Evaluation Module*』(英語)、[SCEU003](#)

### 12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0304RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTJ	<a href="#">Samples</a>
TXB0304RUTR	ACTIVE	UQFN	RUT	12	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(737, 73R, 73V)	<a href="#">Samples</a>
TXBN0304RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	ZTK	<a href="#">Samples</a>
TXBN0304RUTR	ACTIVE	UQFN	RUT	12	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	74R	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

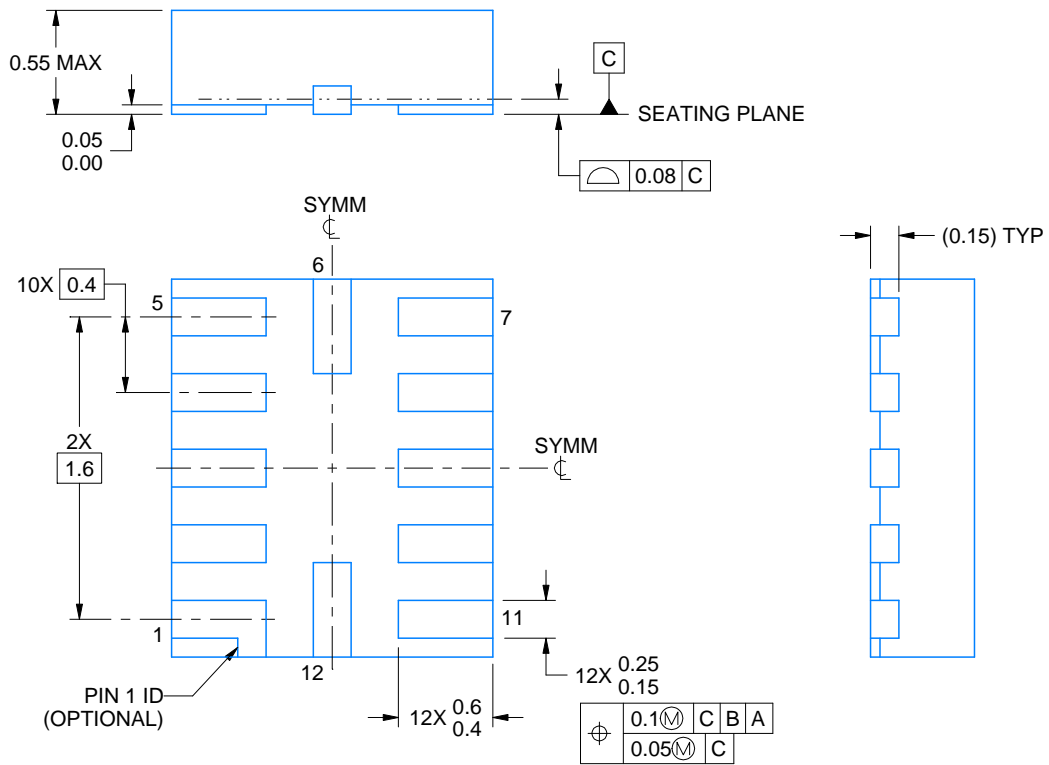
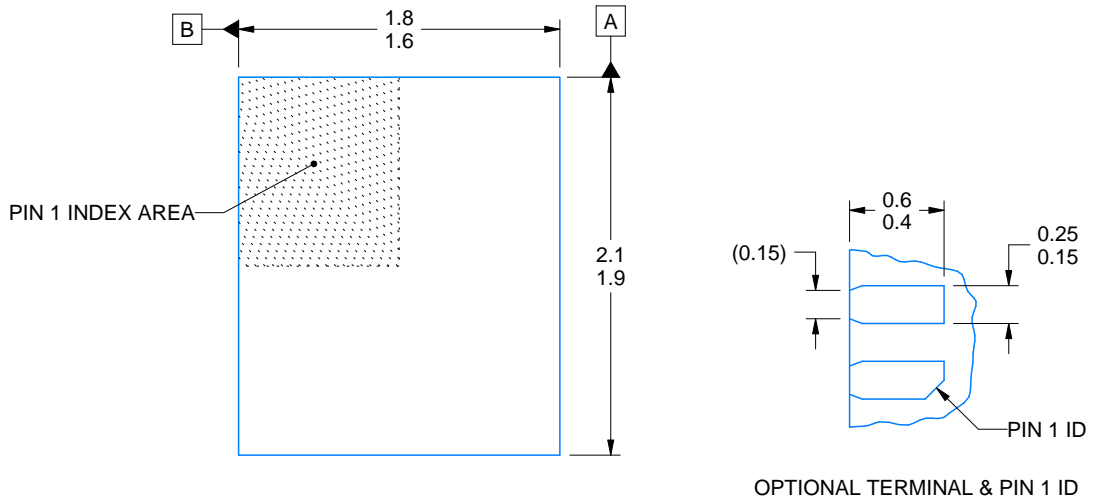
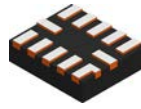

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXB0304RUTR	UQFN	RUT	12	3000	180.0	9.5	1.9	2.3	0.75	4.0	8.0	Q1
TXB0304RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	177.8	12.4	2.0	2.8	0.7	4.0	12.0	Q1
TXBN0304RSVR	UQFN	RSV	16	3000	330.0	12.4	2.1	2.9	0.75	4.0	12.0	Q1
TXBN0304RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXB0304RUTR	UQFN	RUT	12	3000	184.0	184.0	19.0
TXB0304RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0
TXBN0304RSVR	UQFN	RSV	16	3000	202.0	201.0	28.0
TXBN0304RSVR	UQFN	RSV	16	3000	184.0	184.0	19.0
TXBN0304RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0



4220310/A 11/2016

NOTES:

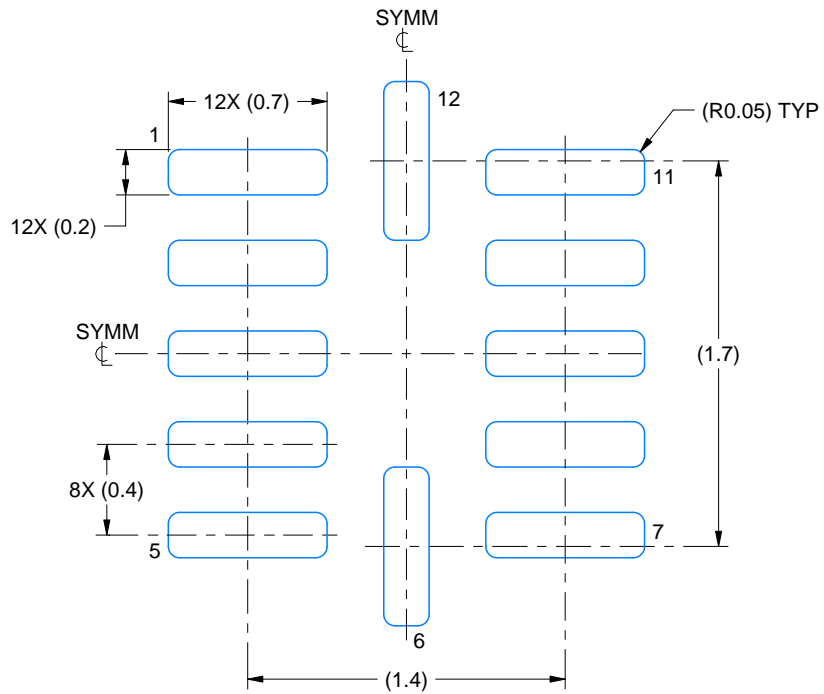
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

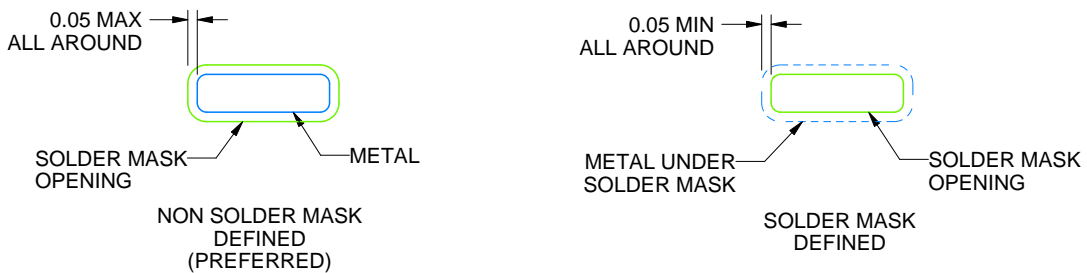
RUT0012A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

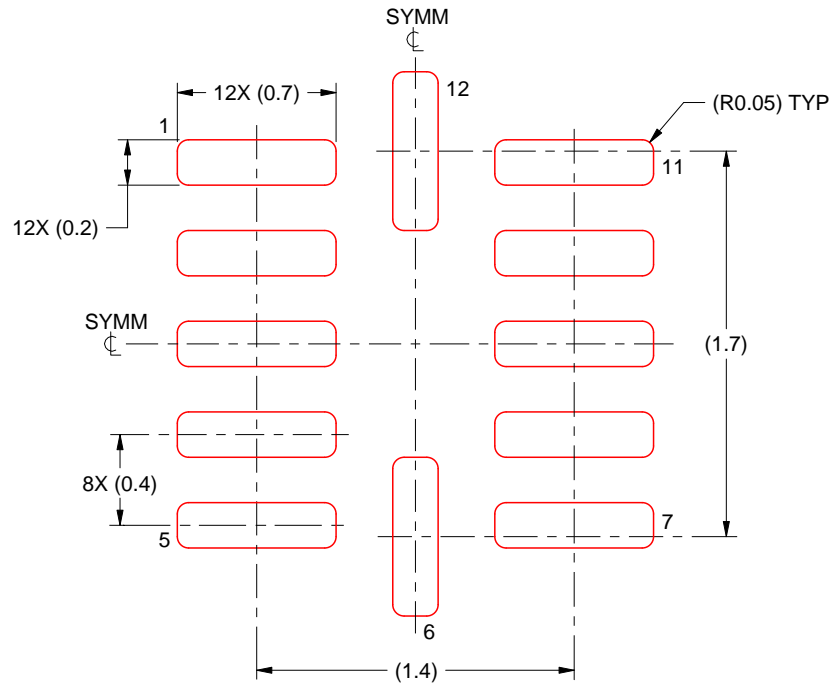
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

RUT0012A

UQFN - 0.55 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## GENERIC PACKAGE VIEW

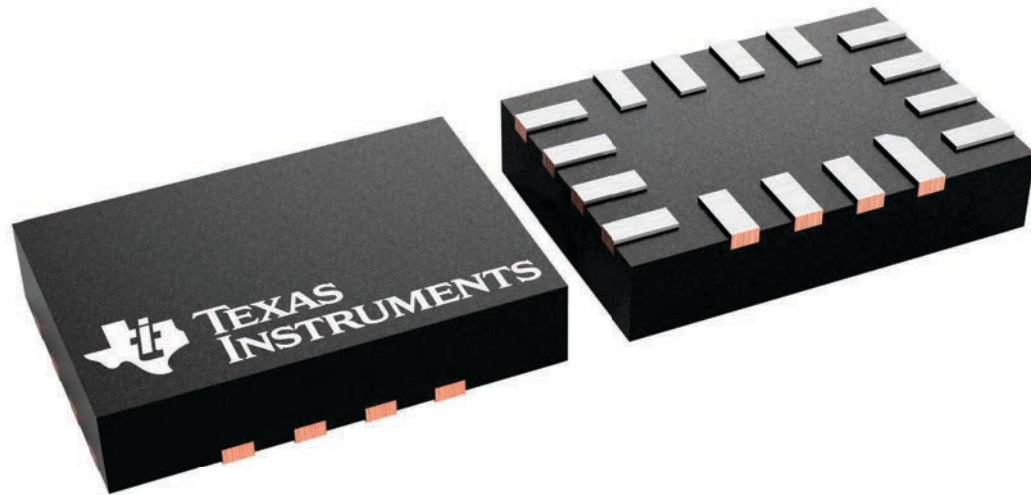
**RSV 16**

**UQFN - 0.55 mm max height**

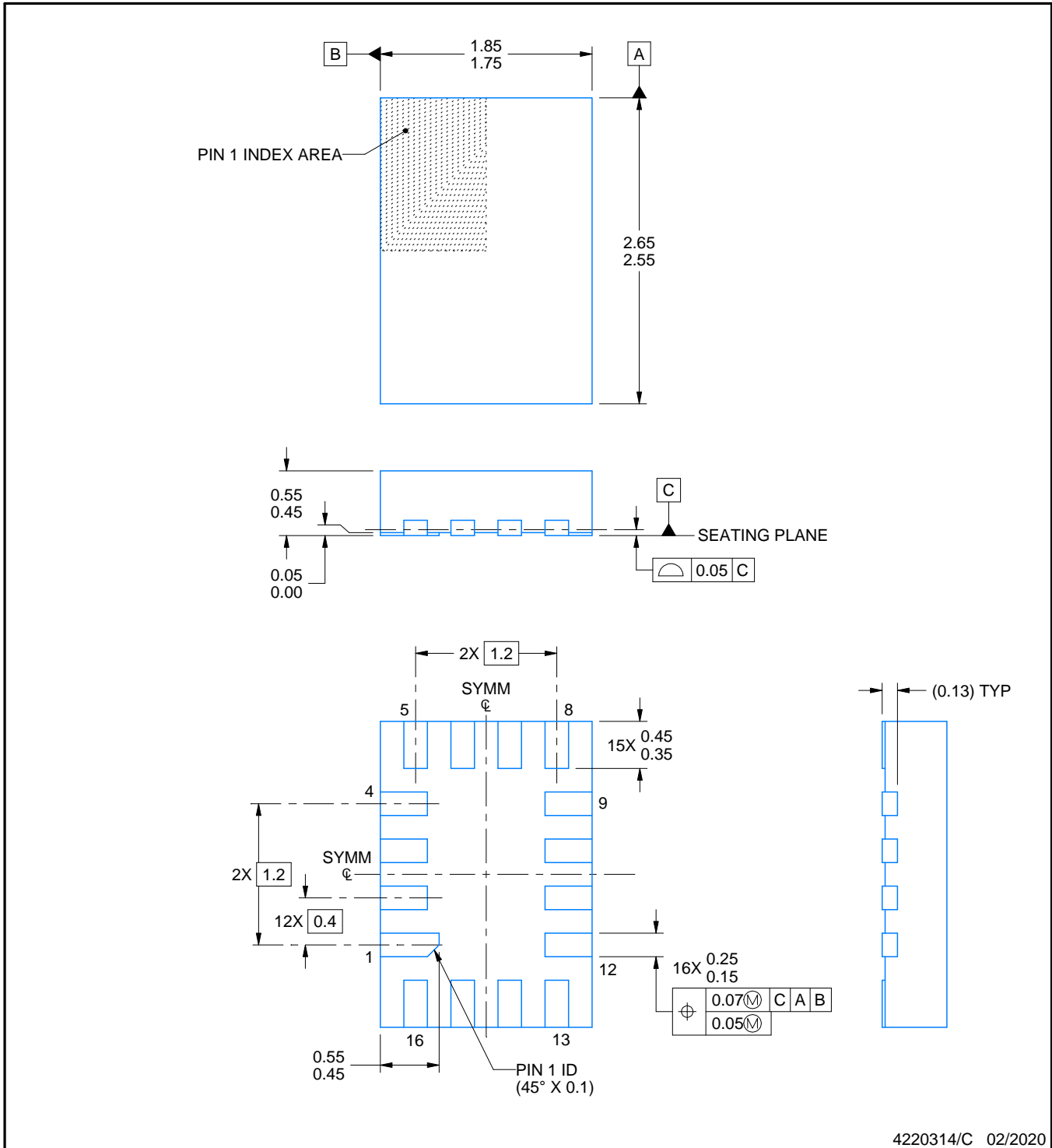
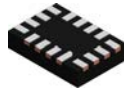
1.8 x 2.6, 0.4 mm pitch

ULTRA THIN QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4231225/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

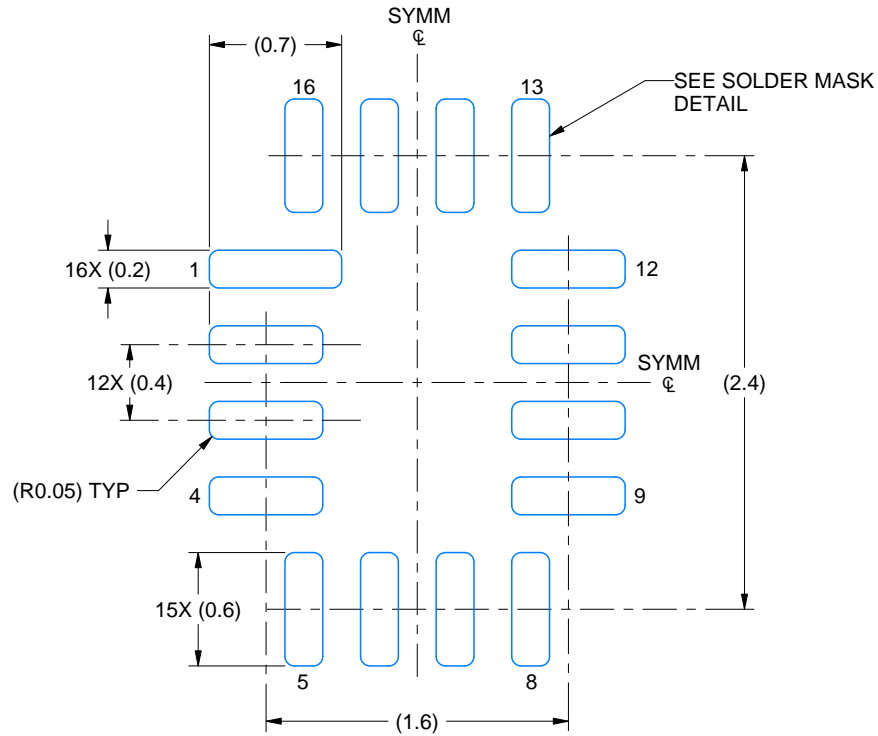


# EXAMPLE BOARD LAYOUT

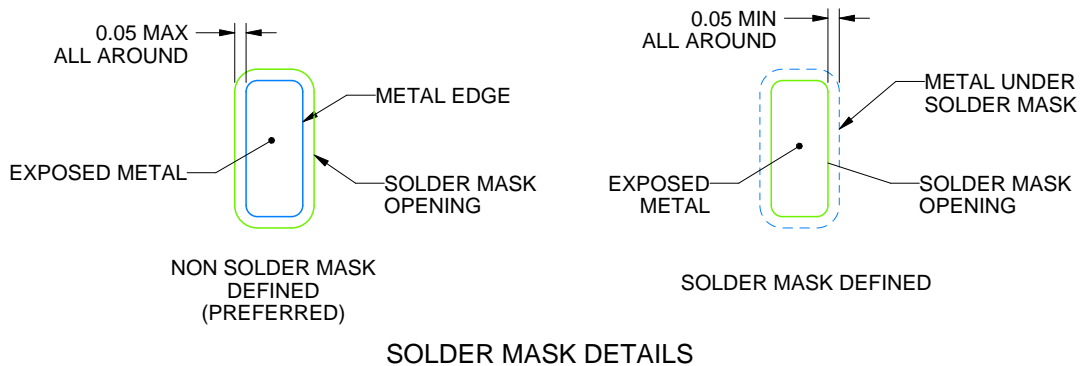
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4220314/C 02/2020

NOTES: (continued)

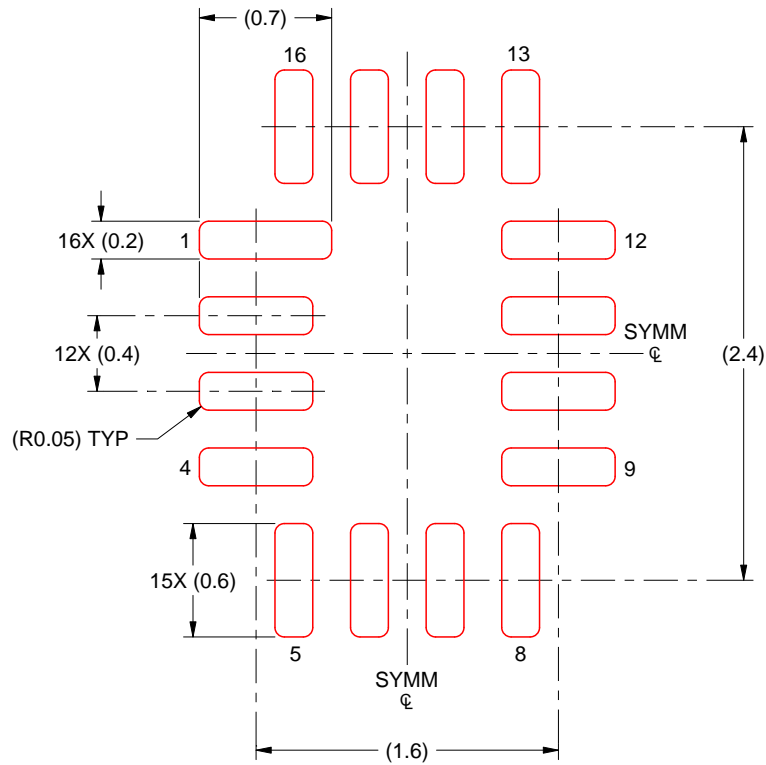
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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