TEXAS INSTRUMENTS
ADC12DJ3200QML-SP
JAJSGI4B – NOVEMBER 2018 – REVISED MARCH 2021

ADC12DJ3200QML-SP 6.4GSPS シングル・チャネルまたは 3.2GSPS デュアル・チャネル、" />12 ビット、RF サンプリング A/D コンバータ (ADC)

1 特長

- ADC コア:
  - 12 ビット分解能
  - シングル・チャネル・モードで最大 6.4GSPS
  - デュアル・チャネル・モードで最大 3.2GSPS
- ノイズ・フロア (信号なし、V_{FS} = $1V_{PP-DIFF}$):
  - デュアル・チャネルモード:-149.5dBFS/Hz
  - シングル・チャネルモード:-152.4dBFS/Hz
- ピーク・ノイズ・パワー比 (NPR):45.4dB
- バッファ付きアナログ入力、V_{CMI} = 0V:
  - アナログ入力帯域幅 (-3dB):7GHz
  - 使用可能な入力周波数範囲:> 10GHz
  - フルスケール入力電圧 (V_{FS}、デフォルト):$0.8V_{pp}$
- ノイズなしのアパーチャ遅延 (t_{AD}) 調整:
  - 高精度サンプリング制御:19fs ステップ
  - 遅延は温度および電圧に対して不変
- 使いやすい同期機能
  - SYSREF タイミングの自動較正
  - サンプル・マーキング用のタイムスタンプ
- JESD204B サブクラス-1 準拠のインターフェイス:
  - 最大レーン速度:12.8Gbps
  - 最大 16 レーンを使用してレーン速度を低減可能
- デュアル・チャネル・モードのデジタル・ダウン・コンバータ
  - 実数出力:DDC バイパスまたは 2x 間引き
  - 複素数出力:4x、8x、または 16x 間引き
- 耐放射線性能:
  - 吸収線量 (TID):300krad (Si)
  - シングル・イベント・ラッチアップ (SEL):120MeV-cm^2/mg
  - シングル・イベント・アップセット (SEU) 耐性レジスタ
- 消費電力:3W

2 アプリケーション

- 衛星通信 (SATCOM)
- 位相アレイ・レーダー、SIGINT、ELINT
- 合成開口レーダー (SAR)
- タイム・オブ・フライト (ToF) および LIDAR 距離測定
- RF サンプリングのソフトウェア無線 (SDR)
- 分光測定

3 概要

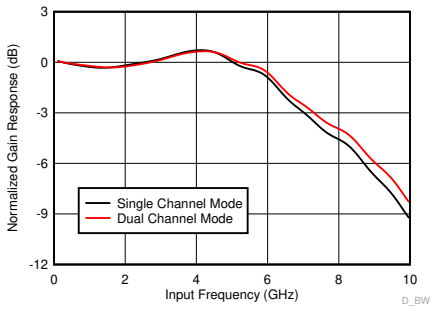
ADC12DJ3200QML-SP デバイスは、RF サンプリング、ギガ・サンプルの A/D コンバータ (ADC) で、DC から 10GHz 超までの入力周波数を直接サンプリングできます。デュアル・チャネル・モードでは、ADC12DJ3200QML-SP は最大 3200MSPS をサンプリングできます。シングル・チャネル・モードでは、最大 6400MSPS をサンプリングできます。チャネル数 (デュアル・チャネル・モード) とナイキスト帯域幅 (シングル・チャネル・モード) のトレードオフをプログラム可能なので、多くのチャネル数を必要とするアプリケーション、または瞬間的に広い信号帯域幅を必要とするアプリケーションのどちらの要求にも対応できる、柔軟なハードウェアを開発できます。フルパワー入力帯域幅 (-3dB) は 7GHz で、使用可能な周波数はデュアル・チャネルでもシングル・チャネル・モードでも -3dB ポイントを超えて拡大されるため、L バンド、S バンド、C バンド、X バンドを直接 RF サンプリングでき、周波数の機動性が高いシステムを実現できます。

ADC12DJ3200QML-SP は、高速の JESD204B 出力インターフェイスを使用し、最大 16 の直列化されたレーンを持ち、決定論的レイテンシとマルチデバイス同期についてサブクラス-1 に準拠しています。シリアル出力レーンは、最大 12.8Gbps をサポートし、ビット・レートとレーン数のトレードオフを設定可能です。革新的な同期機能として、ノイズなしのアパーチャ遅延 (t_{AD}) 調整、SYSREF のウィンドウ処理などがあり、合成開口レーダー (SAR) や位相アレイ MIMO 通信のシステム設計を簡素化できます。デュアル・チャネル・モードではオプションのデジタル・ダウン・コンバータ (DDC) により、インターフェイス速度の低減 (実数および複素数間引きモード) と、信号のデジタル・ミキシング (複素数間引きモードのみ) が可能です。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
ADC12DJ3200QML-SP	CLGA (196) CCGA (196) フリップ・チップ	15.00mm×15.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



ADC12DJ3200QML-SP で測定された入力帯域幅

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- 「*特長*」に NPR を追加 ... 1
- Updated the Specifications with production data ... 9
- Added the *Typical Characteristics* section ... 26
- Added requirement for at least 3 SYSREF rising edges at SYSREF± pins to receive a valid SYSREF windowing output (see *SYSREF Windowing* section) ... 46
- Updated *Application Information* section. ... 134
- Added NPR measurement data to *Typical Application* section ... 137
- Updated list of related content in the *Development Support* section and the *Related Documentation* section ... 149

5 Pin Configuration and Functions

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	AGND	BG	AGND	INA+	INA-	AGND	NCOA0	ORA0	CALTRIG	DA3+	DA3-	DA2+	DA2-	DGND
B	AGND	$\overline{\text{SYNCSE}}$	AGND	AGND	AGND	AGND	NCOA1	ORA1	CALSTAT	DA7+	DA7-	DA6+	DA6-	DGND
C	TMSTP+	VA19	VA19	VA19	VA19	AGND	AGND	DGND	DGND	VD11	VD11	VD11	DA5+	DA1+
D	TMSTP-	VA19	VA11	AGND	AGND	AGND	AGND	DGND	DGND	DGND	DGND	VD11	DA5-	DA1-
E	VA19	VA19	VA11	AGND	AGND	AGND	AGND	DGND	DGND	DGND	DGND	VD11	DA4+	DA0+
F	AGND	VA11	VA11	AGND	AGND	AGND	AGND	DGND	DGND	DGND	DGND	VD11	DA4-	DA0-
G	CLK+	AGND	VA11	AGND	AGND	AGND	AGND	DGND	DGND	DGND	DGND	VD11	$\overline{\text{SCS}}$	SCLK
H	CLK-	AGND	VA11	AGND	AGND	AGND	AGND	DGND	DGND	DGND	DGND	VD11	SDI	SDO
J	AGND	VA11	VA11	AGND	AGND	AGND	AGND	DGND	DGND	DGND	DGND	VD11	DB4-	DB0-
K	VA19	VA19	VA11	AGND	AGND	AGND	AGND	DGND	DGND	DGND	DGND	VD11	DB4+	DB0+
L	SYSREF+	VA19	VA11	AGND	AGND	AGND	AGND	DGND	DGND	DGND	DGND	VD11	DB5-	DB1-
M	SYSREF-	VA19	VA19	VA19	VA19	AGND	AGND	DGND	DGND	VD11	VD11	VD11	DB5+	DB1+
N	AGND	TDIODE+	AGND	AGND	AGND	AGND	NCOB1	ORB1	DGND	DB7+	DB7-	DB6+	DB6-	DGND
P	AGND	TDIODE-	AGND	INB+	INB-	AGND	NCOB0	ORB0	PD	DB3+	DB3-	DB2+	DB2-	DGND

図 5-1. ZMX (CGLA) and NWE (CCGA)Package, 196-Pad Flip Chip Ceramic LGA, Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	A1, A3, A6, B1, B3, B4, B6, B6, C6, C7, D4, D5, D6, D7, E4, E5, E6, E7, F1, F4, F5, F6, F7, G2, G4, G5, G6, G7, H2, H4, H5, H6, H7, J1, J4, J5, J6, J7, K4, K5, K6, K7, L4, L5, L6, L7, M6, M7, N1, N3, N4, N5, N6, P1, P3, P6	—	Analog supply ground. AGND and DGND should be directly connected on circuit board.
BG	A2	O	Bandgap voltage output. This pin is capable of sourcing 100 µA and can drive a load up to 80 pF. See the *Analog Reference Voltage* section for more details. This pin can be left disconnected if not used.
CALSTAT	B9	O	Foreground calibration status output or device alarm output. Functionality is programmed through CAL_STATUS_SEL. This pin can be left disconnected if not used.
CALTRIG	A9	I	Foreground calibration trigger input. This pin is only used if hardware calibration triggering is selected in CAL_TRIG_EN, otherwise software triggering is performed using CAL_SOFT_TRIG. This pin should be tied to GND if not used.
CLK+	G1	I	Device (sampling) clock positive input. The clock signal must be AC coupled to this input. In single-channel mode, the analog input signal is sampled on both rising and falling edges. In dual-channel mode, the analog signal is sampled on the rising edge. This differential input has an internal 100-Ω differential termination and is self-biased to the optimal input common mode voltage.
CLK–	H1	I	Device (sampling) clock negative input. Must be AC coupled.
DA0+	E14	O	High-speed serialized-data output for channel A, lane 0, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA0–	F14	O	High-speed serialized-data output for channel A, lane 0, negative connection. This pin can be left disconnected if not used.
DA1+	C14	O	High-speed serialized-data output for channel A, lane 1, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA1–	D14	O	High-speed serialized-data output for channel A, lane 1, negative connection. This pin can be left disconnected if not used.
DA2+	A12	O	High-speed serialized-data output for channel A, lane 2, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA2–	A13	O	High-speed serialized-data output for channel A, lane 2, negative connection. This pin can be left disconnected if not used.
DA3+	A10	O	High-speed serialized-data output for channel A, lane 3, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA3–	A11	O	High-speed serialized-data output for channel A, lane 3, negative connection. This pin can be left disconnected if not used.
DA4+	E13	O	High-speed serialized-data output for channel A, lane 4, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DA4–	F13	O	High-speed serialized-data output for channel A, lane 4, negative connection. This pin can be left disconnected if not used.
DA5+	C13	O	High-speed serialized-data output for channel A, lane 5, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA5–	D13	O	High-speed serialized-data output for channel A, lane 5, negative connection. This pin can be left disconnected if not used.
DA6+	B12	O	High-speed serialized-data output for channel A, lane 6, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA6–	B13	O	High-speed serialized-data output for channel A, lane 6, negative connection. This pin can be left disconnected if not used.
DA7+	B10	O	High-speed serialized-data output for channel A, lane 7, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DA7–	B11	O	High-speed serialized-data output for channel A, lane 7, negative connection. This pin can be left disconnected if not used.
DB0+	K14	O	High-speed serialized-data output for channel B, lane 0, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB0–	J14	O	High-speed serialized-data output for channel B, lane 0, negative connection. This pin can be left disconnected if not used.
DB1+	M14	O	High-speed serialized-data output for channel B, lane 1, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB1–	L14	O	High-speed serialized-data output for channel B, lane 1, negative connection. This pin can be left disconnected if not used.
DB2+	P12	O	High-speed serialized-data output for channel B, lane 2, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB2–	P13	O	High-speed serialized-data output for channel B, lane 2, negative connection. This pin can be left disconnected if not used.
DB3+	P10	O	High-speed serialized-data output for channel B, lane 3, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB3–	P11	O	High-speed serialized-data output for channel B, lane 3, negative connection. This pin can be left disconnected if not used.
DB4+	K13	O	High-speed serialized-data output for channel B, lane 4, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB4–	J13	O	High-speed serialized-data output for channel B, lane 4, negative connection. This pin can be left disconnected if not used.
DB5+	M13	O	High-speed serialized-data output for channel B, lane 5, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB5–	L13	O	High-speed serialized-data output for channel B, lane 5, negative connection. This pin can be left disconnected if not used.
DB6+	N12	O	High-speed serialized-data output for channel B, lane 6, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.
DB6–	N13	O	High-speed serialized-data output for channel B, lane 6, negative connection. This pin can be left disconnected if not used.
DB7+	N10	O	High-speed serialized-data output for channel B, lane 7, positive connection. This differential output must be AC-coupled and must always be terminated with a 100-Ω differential termination at the receiver. This pin can be left disconnected if not used.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
DB7–	N11	O	High-speed serialized-data output for channel B, lane 7, negative connection. This pin can be left disconnected if not used.
DGND	A14, B14, C8, C9, D8, D9, D10, D11, E8, E9, E10, E11, F8, F9, F10, F11, G8, G9, G10, G11, H8, H9, H10, H11, J8, J9, J10, J11, K8, K9, K10, K11, L8, L9, L10, L11, M8, M9, N9, N14, P14	—	Digital supply ground. AGND and DGND should be directly connected on circuit board.
INA+	A4	I	Channel A analog input positive connection. The differential full-scale input range is determined by the full-scale voltage adjust register. The input common mode voltage should be set to AGND. This input is terminated to ground through a 50-Ω termination resistor. Use of INA is recommended for single-channel mode due to optimized performance. This pin can be left disconnected if not used.
INA–	A5	I	Channel A analog input negative connection. This input is terminated to ground through a 50-Ω termination resistor. Use of INA is recommended for single-channel mode due to optimized performance. This pin can be left disconnected if not used.
INB+	P4	I	Channel B analog input positive connection. The differential full-scale input range is determined by the full-scale voltage adjust register. The input common mode voltage should be set to AGND. This input is terminated to ground through a 50-Ω termination resistor. This pin can be left disconnected if not used.
INB–	P5	I	Channel B analog input negative connection. This input is terminated to ground through a 50-Ω termination resistor. This pin can be left disconnected if not used.
NCOA0	A7	I	NCO accumulator selection control LSB for DDC A. NCOA0 and NCOA1 select which NCO, of a possible four NCOs, is used for digital mixing. The remaining unselected NCOs continue to run to maintain phase coherency and can be swapped in by changing the values of NCOA0 and NCOA1. This is an asynchronous input. This pin should be tied to GND if not used.
NCOA1	B7	I	NCO accumulator selection control MSB for DDC A. This pin should be tied to GND if not used.
NCOB0	P7	I	NCO accumulator selection control LSB for DDC B. NCOB0 and NCOB1 select which NCO, of a possible four NCOs, is used for digital mixing. The remaining unselected NCOs continue to run to maintain phase coherency and can be swapped in by changing the values of NCOB0 and NCOB1. This is an asynchronous input. This pin should be tied to GND if not used.
NCOB1	N7	I	NCO accumulator selection control MSB for DDC B. This pin should be tied to GND if not used.
ORA0	A8	O	Fast overrange detection status for channel A for T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status will go high. The minimum pulse duration is set by OVR_N. This pin can be left disconnected if not used.
ORA1	B8	O	Fast overrange detection status for channel A for T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status will go high. The minimum pulse duration is set by OVR_N. This pin can be left disconnected if not used.
ORB0	P8	O	Fast overrange detection status for channel B for T0 threshold. When the analog input exceeds the threshold programmed into OVR_T0, this status will go high. The minimum pulse duration is set by OVR_N. This pin can be left disconnected if not used.
ORB1	N8	O	Fast overrange detection status for channel B for T1 threshold. When the analog input exceeds the threshold programmed into OVR_T1, this status will go high. The minimum pulse duration is set by OVR_N. This pin can be left disconnected if not used.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PD	P9	I	This pin disables all analog circuits and serializer outputs when set high for temperature diode calibration only. Do not use this pin to power down the device for power savings. Tie this pin to GND during normal operation. For information regarding reliable serializer operation, see the *Power down Modes* section.
SCLK	G14	I	Serial interface clock. This pin functions as the serial-interface clock input which clocks the serial programming data in and out. *Using the Serial Inrterface* describes the serial interface in more detail. This pin supports 1.1 V to 1.9 V CMOS levels.
$\overline{SCS}$	G13	I	Serial interface chip select active low input. *Using the Serial Inrterface* describes the serial interface in more detail. This pin supports 1.1 V to 1.9 V CMOS levels. This pin has a 82-kΩ pull-up resistor to VD11.
SDI	H13	I	Serial interface data input. *Using the Serial Inrterface* describes the serial interface in more detail. This pin supports 1.1 V to 1.9 V CMOS levels.
SDO	H14	O	Serial interface data output. *Using the Serial Inrterface* describes the serial interface in more detail. This pin is high impedance during normal device operation. This pin outputs 1.9-V CMOS levels during serial interface read operations. This pin can be left disconnected if not used.
$\overline{SYNCSE}$	B2	I	JESD204B SYNC signal single-ended active low input. This pin provides the JESD204B-required synchronization request input. A logic low applied to this input initiates code group synchronization and the initial lane alignment sequence. The choice of single-ended or differential $\overline{SYNC}$ (using TMSTP+ and TMSTP- pins) is selected by programming SYNC_SEL. This pin should be tied to GND if differential $\overline{SYNC}$ (TMSTP±) is used as the JESD204B SYNC signal.
SYSREF+	L1	I	SYSREF positive input used to achieve synchronization and deterministic latency across the JESD204B interface. This differential input (SYSREF+ to SYSREF–) has an internal 100-Ω differential termination. It is self-biased when AC coupled (SYSREF_LVPECL_EN must be set to 0), but can be DC coupled by setting SYSREF_LVPECL_EN to 1, which changes the internal termination to 50-Ω single-ended termination to ground on each SYSREF+ and SYSREF- input. The common mode voltage must be within the recommended range when DC coupled.
SYSREF–	M1	I	SYSREF negative input.
TDIODE+	N2	I	Temperature diode positive (anode) connection. An external temperature sensor can be connected to TDIODE+ and TDIODE– to monitor the junction temperature of the device. This pin can be left disconnected if not used.
TDIODE–	P2	I	Temperature diode negative (cathode) connection. This pin can be left disconnected if not used.
TMSTP+	C1	I	Timestamp input positive connection or differential JESD204B $\overline{SYNC}$ positive connection. This input is used as the timestamp input when SYNC_SEL is set to use $\overline{SYNCSE}$ as the JESD204B SYNC signal. This input is used as the JESD204B SYNC signal when SYNC_SEL is set to use TMSTP+ and TMSTP– as the JESD204B SYNC signal. For additional usage information as timestamp input, see the *Timestamp* section. This pin can be left disconnected if $\overline{SYNCSE}$ is used and timestamp is not required.
TMSTP–	D1	I	Timestamp input positive connection or differential JESD204B $\overline{SYNC}$ negative connection. This pin can be left disconnected if $\overline{SYNCSE}$ is used and timestamp is not required.
VA11	D3, E3, F2, F3, G3, H3, J2, J3, K3, L3	I	1.1-V analog supply.
VA19	C2, C3, C4, C5, D2, E1, E2, K1, K2, L2, M2, M3, M4, M5	I	1.9-V analog supply.

表 5-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VD11	C10, C11, C12, D12, E12, F12, G12, H12, J12, K12, L12, M10, M11, M12	I	1.1-V digital supply.

6 Specifications

6.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range	VA19(2)	–0.3	2.35	V
		VA11(2)	–0.3	1.32	
		VD11(3)	–0.3	1.32	
		Voltage between VD11 and VA11	–1.32	1.32	
V_{GND}	Voltage between AGND and DGND		–0.1	0.1	V
V_{PIN}	Pin voltage range	DA[7:0]+, DA[7:0]–, DB[7:0]+, DB[7:0]–, TMSTP+, TMSTP–(3)	–0.5	VD11 + 0.5(5)	V
		CLK+, CLK–, SYSREF+, SYSREF–(2)	–0.5	VA11 + 0.5(4)	
		BG, TDIODE+, TDIODE–(2)	–0.5	VA19 + 0.5(6)	
		INA+, INA–, INB+, INB–(2)	–1	1	
		CALSTAT, CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, ORA0, ORA1, ORB0, ORB1, PD, SCLK, $\overline{SCS}$, SDI, SDO, $\overline{SYNCSE}$ (2)	–0.5	VA19 + 0.5(6)	
$I_{MAX(ANY)}$	Peak input current (any input except INA+, INA–, INB+, INB–)		–25	25	mA
$I_{MAX(INx)}$	Peak input current (INA+, INA–, INB+, INB–)		–50	50	mA
$P_{MAX(INx)}$	Peak RF input power (INA+, INA–, INB+, INB–)	Single-ended with Z_{S-SE} = 50 Ω		16.4	dBm
$I_{MAX(ALL)}$	Peak total input current (sum of absolute value of all currents forced in or out, not including power-supply current)			100	mA
T_j	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured to AGND.
(3) Measured to DGND.
(4) Maximum voltage not to exceed VA11 absolute maximum rating.
(5) Maximum voltage not to exceed VD11 absolute maximum rating.
(6) Maximum voltage not to exceed VA19 absolute maximum rating.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range	VA19, analog 1.9-V supply(2)	1.8	1.9	2	V
		VA11, analog 1.1-V supply(2)	1.05	1.1	1.15	
		VD11, digital 1.1-V supply(3)	1.05	1.1	1.15	
V_{CMI}	Input common-mode voltage	INA+, INA–, INB+, INB–(2)	–50	0	100	mV
		CLK+, CLK–, SYSREF+, SYSREF–(2) (4)	0	0.3	0.55	V
		TMSTP+, TMSTP–(3) (5)	0	0.3	0.55	
V_{ID}	Input voltage, peak-to-peak differential	CLK+ to CLK–, SYSREF+ to SYSREF–, TMSTP+ to TMSTP–	0.4	1.0	2.0	$V_{PP-DIFF}$
		INA+ to INA–, INB+ to INB–			1(6)	
V_{IH}	High-level input voltage	CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, PD, SCLK, $\overline{SCS}$, SDI, $\overline{SYNCSE}$ (2)	0.7			V
V_{IL}	Low-level input voltage	CALTRIG, NCOA0, NCOA1, NCOB0, NCOB1, PD, SCLK, $\overline{SCS}$, SDI, $\overline{SYNCSE}$ (2)			0.45	V
I_{C_TD}	Temperature diode input current	TDIODE+ to TDIODE–		100		µA
C_L	BG maximum load capacitance				100	pF
I_O	BG maximum output current				100	µA
DC	Input clock duty cycle		30%	50%	70%	
T_A	Operating free-air temperature		–55			°C
T_j	Operating junction temperature				125(1)	°C

(1) Prolonged use above a junction temperature of 105°C may increase the device failure-in-time (FIT) rate.
(2) Measured to AGND.
(3) Measured to DGND.
(4) TI strongly recommends that CLK± be AC-coupled with DEVCLK_LVPECL_EN set to 0 to allow CLK± to self bias to the optimal input common-mode voltage for best performance. TI recommends AC-coupling for SYSREF± unless DC-coupling is required, in which case LVPECL input mode must be used (SYSREF_LVPECL_EN = 1).
(5) TMSTP± does not have internal biasing, which requires TMSTP± to be biased externally whether AC-coupled with TMSTP_LVPECL_EN = 0 or DC-coupled with TMSTP_LVPECL_EN = 1.
(6) ADC output code saturates when V_{ID} for INA± or INB± exceeds the programmed full-scale voltage (V_{FS}) set by FS_RANGE_A for INA± or FS_RANGE_B for INB±.

6.4 Thermal Information

THERMAL METRIC(1)		ADC12DJ3200QML-SP ZMX (CLGA) NWE (CCGA) 196 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	24.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.5(2)	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) The case bottom temperature was taken at the bottom of the solder columns on a fixed temperature PCB. This parameter only applies when solder columns are attached to the device.

6.5 Electrical Characteristics: DC Specifications

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
DC ACCURACY							
	Resolution	Resolution with no missing codes			12		Bits
DNL	Differential nonlinearity	Maximum positive excursion from ideal step size			0.4		LSB
		Maximum negative excursion from ideal step size			–0.3		LSB
INL	Integral nonlinearity	Maximum positive excursion from ideal transfer function			3		LSB
		Maximum negative excursion from ideal transfer function			–2		LSB
ANALOG INPUTS (INA+, INA–, INB+, INB–)							
V_{OFF}	Offset error	CAL_OS = 0			±2.0		mV
		CAL_OS = 1			±0.5		mV
V_{OFF_ADJ}	Input offset voltage adjustment range	Available offset correction range (see CAL_OS bit in the CAL_CFG0 register or the OADJ_A_FG0_VINA register)			±55		mV
V_{OFF_DRIFT}	Offset drift	Foreground calibration at nominal temperature only			23		µV/°C
		Foreground calibration at each temperature			0		
V_{IN_FSR}	Analog differential input full-scale range	Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000)	[1, 2, 3]	750	810	850	mV_{PP}
		Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF)			1050		
		Minimum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0x2000)			490		
$V_{IN\_FSR\_DRIFT}$	Analog differential input full-scale range drift	Default FS_RANGE_A and FS_RANGE_B setting, foreground calibration at nominal temperature only, inputs driven by 50-Ω source, includes effect of R_{IN} drift			–0.01		%/°C
		Default FS_RANGE_A and FS_RANGE_B setting, foreground calibration at each temperature, inputs driven by 50-Ω source, includes effect of R_{IN} drift			–0.022		
$V_{IN\_FSR\_MATCH}$	Analog differential input full-scale range matching	Matching between INA± and INB±, default setting, dual-channel mode			1%		
R_{IN}	Single-ended input resistance to AGND	Each input pin is terminated to AGND, measured at T_A = 25°C	[1]	48	50	52	Ω
R_{IN_TEMPCO}	Input termination linear temperature coefficient				14.7		mΩ/°C
C_{IN}	Single-ended input capacitance	Single-channel mode at DC			0.4		pF
		Dual-channel mode at DC			0.4		

6.5 Electrical Characteristics: DC Specifications (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
TEMPERATURE DIODE CHARACTERISTICS (TDIODE+, TDIODE–)							
ΔV_{BE}	Temperature diode voltage slope	Forced forward current of 100 µA; offset voltage (approximately 0.792 V at 0°C) varies with process and must be measured for each device; perform offset measurement with the device unpowered or with the PD pin asserted to minimize device self-heating; only assert the PD pin long enough to take the offset measurement			–1.6		mV/°C
BAND-GAP VOLTAGE OUTPUT (BG)							
V_{BG}	Reference output voltage	I_L ≤ 100 µA			1.1		V
V_{BG_DRIFT}	Reference output temperature drift	I_L ≤ 100 µA			–102		µV/°C
CLOCK INPUTS (CLK+, CLK–, SYSREF+, SYSREF–, TMSTP+, TMSTP–)							
Z_T	Internal termination	Differential termination with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0, and TMSTP_LVPECL_EN = 0			100		Ω
		Single-ended termination to GND (per pin) with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0, and TMSTP_LVPECL_EN = 0			50		
V_{CM}	Input common-mode voltage, self-biased	Self-biasing common-mode voltage for CLK± when AC-coupled (DEVCLK_LVPECL_EN must be set to 0)			0.3		V
		Self-biasing common-mode voltage for SYSREF± when AC-coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver enabled (SYSREF_RECV_EN = 1)			0.3		
		Self-biasing common-mode voltage for SYSREF± when AC-coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver disabled (SYSREF_RECV_EN = 0)			VA11		
C_{L_DIFF}	Differential input capacitance	Between positive and negative differential input pins			0.1		pF
C_{L_SE}	Single-ended input capacitance	Each input to ground			0.5		pF
SERDES OUTPUTS (DA[7:0]+, DA[7:0]–, DB[7:0]+, DB[7:0]–)							
V_{OD}	Differential output voltage, peak-to-peak	100-Ω load	[1, 2, 3]	550	600	650	$mV_{PP-DIFF}$
V_{CM}	Output common-mode voltage	AC-coupled			VD11 / 2		V
Z_{DIFF}	Differential output impedance				100		Ω

6.5 Electrical Characteristics: DC Specifications (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
CMOS INTERFACE (SCLK, SDI, SDO, $\overline{SCS}$, PD, NCOA0, NCOA1, NCOB0, NCOB1, CALSTAT, CALTRIG, ORA0, ORA1, ORB0, ORB1, $\overline{SYNCSE}$)							
I_{IH}	High-level input current		[1, 2, 3]			40	µA
I_{IL}	Low-level input current		[1, 2, 3]	–40			µA
C_I	Input capacitance				2		pF
V_{OH}	High-level output voltage	I_{LOAD} = –400 µA	[1, 2, 3]	1.65			V
V_{OL}	Low-level output voltage	I_{LOAD} = 400 µA	[1, 2, 3]			150	mV

(1) For subgroup definitions, please see 表 6-1.

6.6 Electrical Characteristics: Power Consumption

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
I_{VA19}	1.9-V analog supply current	Power mode 1: single-channel mode, JMODE 1 (16 lanes, DDC bypassed), foreground calibration			890		mA
I_{VA11}	1.1-V analog supply current				500		mA
I_{VD11}	1.1-V digital supply current				542		mA
P_{DIS}	Power dissipation				2.8		W
I_{VA19}	1.9-V analog supply current	Power mode 2: single-channel mode, JMODE 0 (8 lanes, DDC bypassed), foreground calibration	[1, 2, 3]		890	1000	mA
I_{VA11}	1.1-V analog supply current		[1, 2, 3]		500	650	mA
I_{VD11}	1.1-V digital supply current		[1, 2, 3]		595	850	mA
P_{DIS}	Power dissipation		[1, 2, 3]		2.9	3.5	W
I_{VA19}	1.9-V analog supply current	Power mode 3: single-channel mode, JMODE 1 (16 lanes, DDC bypassed), background calibration			1172		mA
I_{VA11}	1.1-V analog supply current				600		mA
I_{VD11}	1.1-V digital supply current				561		mA
P_{DIS}	Power dissipation				3.5		W
I_{VA19}	1.9-V analog supply current	Power mode 4: dual-channel mode, JMODE 3 (16 lanes, DDC bypassed), background calibration			1254		mA
I_{VA11}	1.1-V analog supply current				600		mA
I_{VD11}	1.1-V digital supply current				573		mA
P_{DIS}	Power dissipation				3.7		W
I_{VA19}	1.9-V analog supply current	Power mode 5: dual-channel mode, JMODE 11 (8 lanes, 4x decimation), foreground calibration			971		mA
I_{VA11}	1.1-V analog supply current				500		mA
I_{VD11}	1.1-V digital supply current				1033		mA
P_{DIS}	Power dissipation				3.6		W

(1) For subgroup definitions, please see 表 6-1.

6.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN}= 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
FPBW	Full-power input bandwidth (–3 dB)(2)	Foreground calibration			7.3		GHz
		Background calibration			7.3		
XTALK	Channel-to-channel crosstalk	Dual-channel mode, aggressor = 400 MHz, –1 dBFS			–88		dB
		Dual-channel mode, aggressor = 3 GHz, –1 dBFS			–56		
		Dual-channel mode, aggressor = 6 GHz, –1 dBFS			–57		
CER	Code error rate	Does not include SerDes bit-error rate (BER)			10^{-18}		Errors / Sample
$NOISE_{DC}$	DC input noise standard deviation	No input, foreground calibration, excludes DC offset, includes fixed interleaving spur (f_S / 2 spur)			2.5		LSB
NSD	Noise spectral density, no input signal, excludes fixed interleaving spur (f_S / 2 spur)	Maximum full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xFFFF) setting, foreground calibration			–149.5		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000) setting, foreground calibration			–147.5		
NF	Noise figure, no input, Z_S = 100 Ω	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting, foreground calibration			23.5		dB
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting, foreground calibration			25.5		
SNR	Signal-to-noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			55.7		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration			57.2		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			55.5		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]	51.0	55.0		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration			56.0		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			53.0		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			51.8		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			50.4		
SNR	Signal-to-noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 347 MHz, A_{IN} = –16 dBFS			56.4		dBFS
		f_{IN} = 997 MHz, A_{IN} = –16 dBFS			56.6		
		f_{IN} = 2482 MHz, A_{IN} = –16 dBFS			56.5		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS			56.3		
		f_{IN} = 6397 MHz, A_{IN} = –16 dBFS			56.5		
		f_{IN} = 8197 MHz, A_{IN} = –16 dBFS			56.0		
SINAD	Signal-to-noise and distortion ratio, large signal, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			55.3		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			54.9		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]	50.0	54.4		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			51.3		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			49.9		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			48.1		

6.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN}= 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
ENOB	Effective number of bits, large signal, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			8.9		Bits
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			8.8		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]	8.0	8.7		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			8.2		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			8.0		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			7.7		
SFDR	Spurious-free dynamic range, large signal, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			69		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration			70		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			68		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]	58	67		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration			62		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			59		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			56		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			53		
SFDR	Spurious-free dynamic range, small signal, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –16 dBFS			74		dBFS
		f_{IN} = 997 MHz, A_{IN} = –16 dBFS			75		
		f_{IN} = 2482 MHz, A_{IN} = –16 dBFS			74		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS			75		
		f_{IN} = 6397 MHz, A_{IN} = –16 dBFS			74		
		f_{IN} = 8197 MHz, A_{IN} = –16 dBFS			76		
f_S / 2	f_S / 2 fixed interleaving spur, independent of input signal	No input	[4, 5, 6]		–77	–50	dBFS
HD2	2nd-order harmonic distortion	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			–75		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration			–75		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			–74		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]		–75	–58	
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration			–74		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			–61		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			–61		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			–64		

6.7 Electrical Characteristics: AC Specifications (Dual-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), f_{IN}= 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
HD3	3rd-order harmonic distortion	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			–72		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration			–70		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			–74		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]		–67	–58	
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A and FS_RANGE_B setting, foreground calibration			–62		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			–59		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			–56		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			–53		
f_S / 2-f_{IN}	f_S / 2 – f_{IN} interleaving spur, signal dependent	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			–76		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			–72		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]		–73	–58	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			–71		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			–68		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			–66		
SPUR	Worst-harmonic, 4th-order distortion or higher	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			–76		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			–74		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]		–74	–60	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			–72		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			–69		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			–68		
IMD3	3rd-order intermodulation distortion	f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–86		dBFS
		f_{IN} = 997 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–82		
		f_{IN} = 2482 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–73		
		f_{IN} = 4997 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–65		
		f_{IN} = 6397 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–60		
		f_{IN} = 8197 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–52		

(1) For subgroup definitions, please see 表 6-1.
(2) Full-power input bandwidth (FPBW) is defined as the input frequency where the reconstructed output of the ADC has dropped 3 dB below the power of a full-scale input signal at a low input frequency. Useable bandwidth may exceed the –3-dB full-power input bandwidth.

6.8 Electrical Characteristics: AC Specifications (Single-Channel Mode)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA±, f_{IN} = 347 MHz, A_{IN} = –1 dBFS,f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
FPBW	Full-power input bandwidth (–3 dB)(2)	Foreground calibration			7.1		GHz
		Background calibration			7.1		
CER	Code error rate	Does not include SerDes bit-error rate (BER)			10^{-18}		Errors / Sample
$NOISE_{DC}$	DC input noise standard deviation	No input, foreground calibration, excludes DC offset, includes fixed interleaving spurs (f_S / 2 and f_S / 4 spurs)			2.8		LSB
NSD	Noise spectral density, no input signal, excludes fixed interleaving spurs (f_S / 2 and f_S / 4 spur)	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting, foreground calibration			–152.4		dBFS/Hz
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting, foreground calibration			–150.0		
NF	Noise figure, no input, Z_S = 100 Ω	Maximum full-scale voltage (FS_RANGE_A = 0xFFFF) setting, foreground calibration			20.6		dB
		Default full-scale voltage (FS_RANGE_A = 0xA000) setting, foreground calibration			23.1		
SNR	Signal-to-noise ratio, large signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			55.8		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration			57.1		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			55.5		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]	51.0	54.9		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration			56.1		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			53.1		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			51.9		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			50.6		
SNR	Signal-to-noise ratio, small signal, excluding DC, HD2 to HD9 and interleaving spurs	f_{IN} = 347 MHz, A_{IN} = –16 dBFS			56.5		dBFS
		f_{IN} = 997 MHz, A_{IN} = –16 dBFS			56.6		
		f_{IN} = 2482 MHz, A_{IN} = –16 dBFS			56.5		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS			56.5		
		f_{IN} = 6397 MHz, A_{IN} = –16 dBFS			56.5		
		f_{IN} = 8197 MHz, A_{IN} = –16 dBFS			56.2		
SINAD	Signal-to-noise and distortion ratio, large signal, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			54.6		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			53.6		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]	43.9	51.3		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			50.8		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			49.6		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			47.2		
ENOB	Effective number of bits, large signal, excluding DC and f_S / 2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			8.8		Bits
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			8.6		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]	7.0	8.2		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			8.1		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			7.9		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			7.5		

6.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA±, f_{IN} = 347 MHz, A_{IN} = –1 dBFS,f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range, large signal, excluding DC, f_S / 4 and f_S / 2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			66		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration			67		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			60		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]	45	56		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration			52		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			58		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			57		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			52		
SFDR	Spurious-free dynamic range, small signal, excluding DC, f_S / 4 and f_S / 2 fixed spurs	f_{IN} = 347 MHz, A_{IN} = –16 dBFS			70		dBFS
		f_{IN} = 997 MHz, A_{IN} = –16 dBFS			66		
		f_{IN} = 2482 MHz, A_{IN} = –16 dBFS			66		
		f_{IN} = 4997 MHz, A_{IN} = –16 dBFS			67		
		f_{IN} = 6397 MHz, A_{IN} = –16 dBFS			68		
		f_{IN} = 8197 MHz, A_{IN} = –16 dBFS			65		
f_S / 2	f_S / 2 fixed interleaving spur, independent of input signal	No input, OS_CAL disabled, spur can be improved by running OS_CAL			–64		dBFS
f_S / 4	f_S / 4 fixed interleaving spur, independent of input signal	No input	[4, 5, 6]		–70	–50	dBFS
HD2	2nd-order harmonic distortion	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			–72		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration			–69		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			–70		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]		–71	–58	
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration			–73		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			–66		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			–65		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			–67		
HD3	3rd-order harmonic distortion	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			–71		dBFS
		f_{IN} = 347 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration			–67		
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			–70		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]		–67	–58	
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS, maximum FS_RANGE_A setting, foreground calibration			–62		
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			–61		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			–59		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			–56		

6.8 Electrical Characteristics: AC Specifications (Single-Channel Mode) (continued)

typical values at T_A = 25°C, VA19 = 1.9 V, VA11 = 1.1 V, VD11= 1.1 V, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA±, f_{IN} = 347 MHz, A_{IN} = –1 dBFS,f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
f_S / 2-f_{IN}	f_S / 2 – f_{IN} interleaving spur, signal dependent	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			–68		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			–63		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]		–56	–45	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			–58		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			–57		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			–56		
f_S / 4±f_{IN}	f_S / 4 ± f_{IN} interleaving spurs, signal dependent	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			–76		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			–74		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]		–75	–58	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			–73		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			–69		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			–70		
SPUR	Worst harmonic 4th-order distortion or higher	f_{IN} = 347 MHz, A_{IN} = –1 dBFS			–74		dBFS
		f_{IN} = 997 MHz, A_{IN} = –1 dBFS			–75		
		f_{IN} = 2482 MHz, A_{IN} = –1 dBFS	[4, 5, 6]		–74	–60	
		f_{IN} = 4997 MHz, A_{IN} = –1 dBFS			–70		
		f_{IN} = 6397 MHz, A_{IN} = –1 dBFS			–70		
		f_{IN} = 8197 MHz, A_{IN} = –1 dBFS			–66		
IMD3	3rd-order intermodulation distortion	f_{IN} = 347 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–89		dBFS
		f_{IN} = 997 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–79		
		f_{IN} = 2482 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–73		
		f_{IN} = 4997 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–65		
		f_{IN} = 6397 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–61		
		f_{IN} = 8197 MHz ± 5 MHz, A_{IN} = –7 dBFS per tone			–54		

(1) For subgroup definitions, please see 表 6-1.
(2) Full-power input bandwidth (FPBW) is defined as the input frequency where the reconstructed output of the ADC has dropped 3 dB below the power of a full-scale input signal at a low input frequency. Useable bandwidth may exceed the –3-dB full-power input bandwidth.

6.9 Timing Requirements

			SUBGROUP(1)	MIN	NOM	MAX	UNIT
DEVICE (Sampling) CLOCK (CLK+, CLK–)							
f_{CLK}	Input clock frequency (CLK+, CLK–), both single-channel and dual-channel modes(2)	Maximum input clock frequency	[4, 5, 6]	3200			MHz
		Minimum input clock frequency			800		MHz
SYSREF (SYSREF+, SYSREF–)							
t_{CLK}	Input clock period (CLK+, CLK–), both single-channel and dual-channel modes(2)	Maximum input clock frequency	[4, 5, 6]	312.5			ps
		Minimum input clock frequency			1250		ps
$t_{INV(SYSREF)}$	Duration of invalid SYSREF capture region of CLK± period, indicating setup or hold time violation, as measured by the SYSREF_POS status register(3)				48		ps
$t_{INV(TEMP)}$	Drift of invalid SYSREF capture region over temperature, a positive number indicates a shift toward the MSB of the SYSREF_POS register				0		ps/°C
$t_{INV(VA11)}$	Drift of invalid SYSREF capture region over the VA11 supply voltage, a positive number indicates a shift toward the MSB of the SYSREF_POS register				0.36		ps/mV
$t_{STEP(SP)}$	Delay of the SYSREF_POS LSB	SYSREF_ZOOM = 0			77		ps
		SYSREF_ZOOM = 1			24		
$t_{(PH\_SYS)}$	Minimum SYSREF± assertion duration after a SYSREF± rising edge event				4		ns
$t_{(PL\_SYS)}$	Minimum SYSREF± de-assertion duration after a SYSREF± falling edge event				4		ns
JESD204B SYNC TIMING ($\overline{SYNCSE}$ OR TMSTP±)							
$t_{H(\overline{SYNCSE})}$	Minimum hold time from multiframe boundary (SYSREF rising edge captured high) to de-assertion of JESD204B SYNC signal ($\overline{SYNCSE}$ if SYNC_SEL = 0 or TMSTP± if SYNC_SEL = 1) for NCO synchronization (NCO_SYNC_ILA = 1)	JMODE = 0, 2, 4, 6, 10, 13 or 15			21		t_{CLK} cycles
		JMODE = 1, 3, 5, 7, 9, 11, 14 or 16			17		
		JMODE = 12, 17 or 18			9		
$t_{SU(\overline{SYNCSE})}$	Minimum setup time from de-assertion of JESD204B SYNC signal ($\overline{SYNCSE}$ if SYNC_SEL = 0 or TMSTP± if SYNC_SEL = 1) to multiframe boundary (SYSREF rising edge captured high) for NCO synchronization (NCO_SYNC_ILA = 1)	JMODE = 0, 2, 4, 6, 10, 13 or 15			–2		t_{CLK} cycles
		JMODE = 1, 3, 5, 7, 9, 11, 14 or 16			2		
		JMODE = 12, 17 or 18			10		
$t_{(\overline{SYNCSE})}$	$\overline{SYNCSE}$ minimum assertion time to trigger link resynchronization				4		Frames
SERIAL PROGRAMMING INTERFACE (SCLK, SDI, $\overline{SCS}$)							
$f_{CLK(SCLK)}$	Serial clock frequency		[4, 5, 6]	0.0		15.625	MHz
$t_{(PH)}$	Serial clock high value pulse duration		[4, 5, 6]	32			ns
$t_{(PL)}$	Serial clock low value pulse duration		[4, 5, 6]	32			ns
$t_{SU(\overline{SCS})}$	Setup time from $\overline{SCS}$ to rising edge of SCLK		[4, 5, 6]	25			ns
$t_{H(\overline{SCS})}$	Hold time from rising edge of SCLK to $\overline{SCS}$		[4, 5, 6]	3			ns
$t_{SU(SDI)}$	Setup time from SDI to rising edge of SCLK		[4, 5, 6]	25			ns
$t_{H(SDI)}$	Hold time from rising edge of SCLK to SDI		[4, 5, 6]	3			ns

(1) For subgroup definitions, please see 表 6-1.
(2) Unless functionally limited to a smaller range in 表 7-18 based on the programmed JMODE.
(3) Use SYSREF_POS to select an optimal SYSREF_SEL value for SYSREF capture, see SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) for more information on SYSREF windowing. The invalid region, specified by $t_{INV(SYSREF)}$, indicates the portion of the CLK± period (t_{CLK}), as measured by SYSREF_SEL, that may result in a setup and hold violation. Verify that the timing skew between SYSREF± and CLK± over system operating conditions from the nominal conditions (that used to find optimal SYSREF_SEL) does not result in the invalid region occurring at the selected SYSREF_SEL position in SYSREF_POS, otherwise a temperature dependent SYSREF_SEL selection may be needed to track the skew between CLK± and SYSREF±.

6.10 Switching Characteristics

typical values at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
DEVICE (SAMPLING) CLOCK (CLK+, CLK–)							
t_{AD}	Sampling (aperture) delay from CLK± rising edge (dual-channel mode) or rising and falling edge (single-channel mode) to sampling instant	TAD_COARSE = 0x00, TAD_FINE = 0x00 and TAD_INV = 0			350		ps
$t_{AD(MAX)}$	Maximum t_{AD} Adjust programmable delay, not including clock inversion (TAD_INV = 0)	Coarse adjustment (TAD_COARSE = 0xFF)			289		ps
		Fine adjustment (TAD_FINE = 0xFF)			4.9		
$t_{AD(STEP)}$	t_{AD} Adjust programmable delay step size	Coarse adjustment (TAD_COARSE)			1.13		ps
		Fine adjustment (TAD_FINE)			19		
t_{AJ}	Aperture jitter, rms	Minimum t_{AD} adjust coarse setting (TAD_COARSE = 0x00, TAD_INV = 0)			56		fs
		Maximum t_{AD} adjust coarse setting (TAD_COARSE = 0xFF) excluding TAD_INV (TAD_INV = 0)			68(4)		
SERIAL DATA OUTPUTS (DA[7:0]+, DA[7:0]–, DB[7:0]+, DB[7:0]–)							
f_{SERDES}	Serialized output bit rate	Maximum output bit rate	[9, 10, 11]	12.8			Gbps
		Minimum output bit rate			1		Gbps
UI	Serialized output unit interval	Minimum output unit interval	[9, 10, 11]			78.125	ps
		Maximum output unit interval			1000		ps
t_{TLH}	Low-to-high transition time (differential)	20% to 80%, PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04			27		ps
t_{THL}	High-to-low transition time (differential)	20% to 80%, PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04			27		ps
DDJ	Data dependent jitter, peak-to-peak	PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04, JMODE = 2			11.7		ps
RJ	Random jitter, RMS	PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04, JMODE = 2			0.8		ps

6.10 Switching Characteristics (continued)

typical values at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
TJ	Total jitter, peak-to-peak, with gaussian portion defined with respect to a BER=1e-15 (Q = 7.94)	PRBS-7 test pattern, 12.8 Gbps, SER_PE = 0x04, JMODE = 0, 2			24		ps
		PRBS-7 test pattern, 6.4 Gbps, SER_PE = 0x04, JMODE = 1, 3			20		
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 4, 5, 6, 7			31		
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 9			32		
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 10, 11			35		
		PRBS-7 test pattern, 3.2 Gbps, SER_PE = 0x04, JMODE = 12			24		
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 13, 14			35		
		PRBS-7 test pattern, 8 Gbps, SER_PE = 0x04, JMODE = 15, 16			31		
ADC CORE LATENCY							
t_{ADC}	Deterministic delay from the CLK± edge that samples the reference sample to the CLK± edge that samples SYSREF going high(2)	JMODE = 0			–8.5		t_{CLK} cycles
		JMODE = 1			–20.5		
		JMODE = 2			–9		
		JMODE = 3			–21		
		JMODE = 4			–4.5		
		JMODE = 5			–24.5		
		JMODE = 6			–5		
		JMODE = 7			–25		
		JMODE = 9			60		
		JMODE = 10			140		
		JMODE = 11			136		
		JMODE = 12			120		
		JMODE = 13			232		
		JMODE = 14			232		
		JMODE = 15			446		
		JMODE = 16			430		
		JMODE = 17			–48.5		
		JMODE = 18			–49		

6.10 Switching Characteristics (continued)

typical values at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating temperature range provided in the *Recommended Operating Conditions* table

PARAMETER		TEST CONDITIONS	SUBGROUP(1)	MIN	TYP	MAX	UNIT
JESD204B AND SERIALIZER LATENCY							
t_{TX}	Delay from the CLK± rising edge that samples SYSREF high to the first bit of the multiframe on the JESD204B serial output lane corresponding to the reference sample of t_{ADC} (3)	JMODE = 0		72(5)		84(5)	t_{CLK} cycles
		JMODE = 1		119(5)		132(5)	
		JMODE = 2		72(5)		84(5)	
		JMODE = 3		119(5)		132(5)	
		JMODE = 4		67(5)		80(5)	
		JMODE = 5		106(5)		119(5)	
		JMODE = 6		67(5)		80(5)	
		JMODE = 7		106(5)		119(5)	
		JMODE = 9		106(5)		119(5)	
		JMODE = 10		67(5)		80(5)	
		JMODE = 11		106(5)		119(5)	
		JMODE = 12		213(5)		225(5)	
		JMODE = 13		67(5)		80(5)	
		JMODE = 14		106(5)		119(5)	
		JMODE = 15		67(5)		80(5)	
		JMODE = 16		106(5)		119(5)	
		JMODE = 17		195(5)		208(5)	
		JMODE = 18		195(5)		208(5)	
SERIAL PROGRAMMING INTERFACE (SDO)							
$t_{(OZD)}$	Delay from falling edge of 16th SCLK cycle during read operation for SDO transition from tri-state to valid data			1(5)			ns
$t_{(ODZ)}$	Delay from $\overline{SCS}$ rising edge for SDO transition from valid data to tri-state					10(5)	ns
$t_{(OD)}$	Delay from falling edge of SCLK during read operation to SDO valid		[4, 5, 6]	1		10	ns

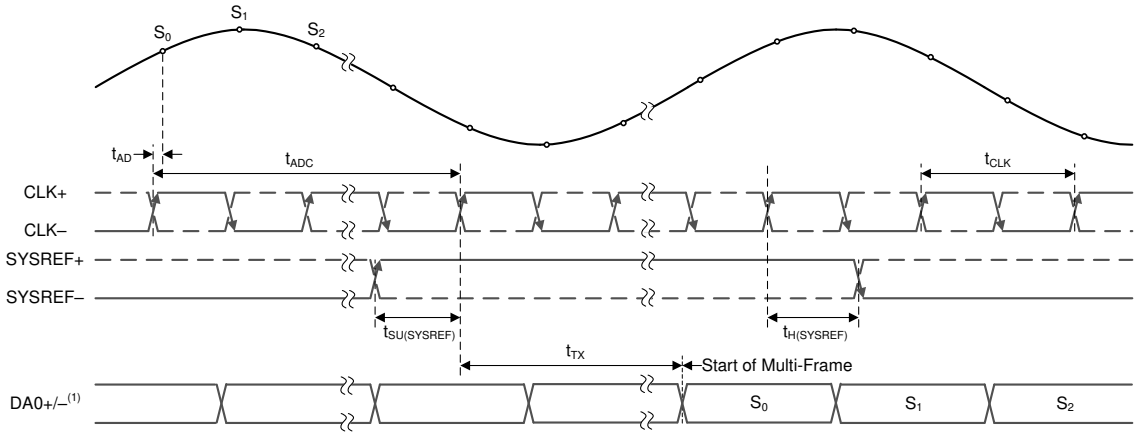
(1) For subgroup definitions, please see 表 6-1.
(2) t_{ADC} is an exact, unrounded, deterministic delay. The delay can be negative if the reference sample is sampled after the SYSREF high capture point, in which case the total latency is smaller than the delay given by t_{TX}.
(3) The values given for t_{TX} include deterministic and non-deterministic delays. The delay varies over process, temperature, and voltage. JESD204B accounts for these variations when operating in subclass-1 mode in order to achieve deterministic latency. Proper receiver RBD values must be chosen such that the elastic buffer release point does not occur within the invalid region of the local multiframe clock (LMFC) cycle.
(4) t_{AJ} increases because of additional attenuation on the internal clock path.
(5) This parameter is specified by design and is not tested in production.

6.11 Timing Diagrams

表 6-1. Quality Conformance Inspection(1)

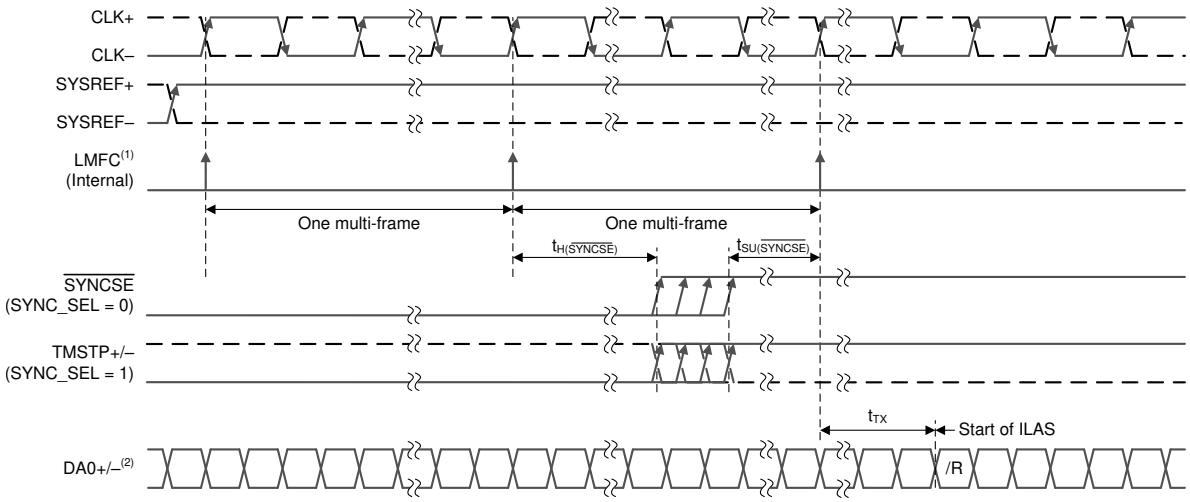
SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	–55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	–55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	–55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	–55

(1) MIL-STD-883, Method 5005 - Group A



A. Only the SerDes lane DA0± is shown, but DA0± is representative of all lanes. The number of output lanes used and bit-packing format is dependent on the programmed JMODE value.

図 6-1. ADC Timing Diagram



A. It is assumed that the internal LMFC is aligned with the rising edge of CLK± that captures the SYSREF± high value.

B. Only SerDes lane DA0± is shown, but DA0± is representative of all lanes. All lanes output /R at approximately the same point in time. The number of lanes is dependent on the programmed JMODE value.

図 6-2. $\overline{\text{SYNCSE}}$ and TMSTP± Timing Diagram for NCO Synchronization

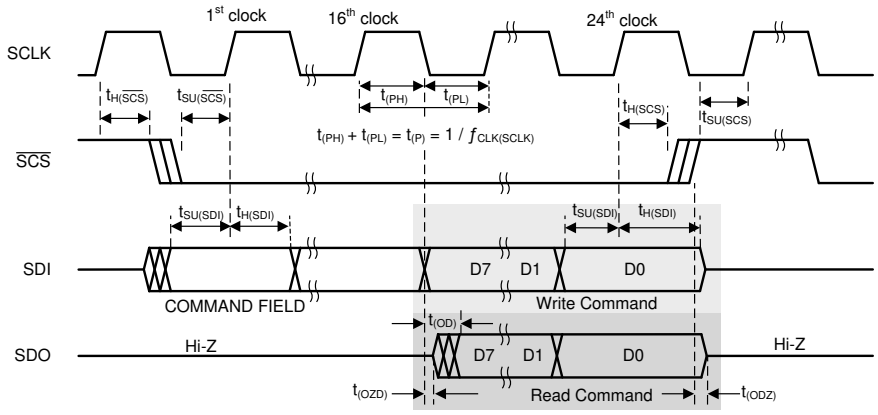
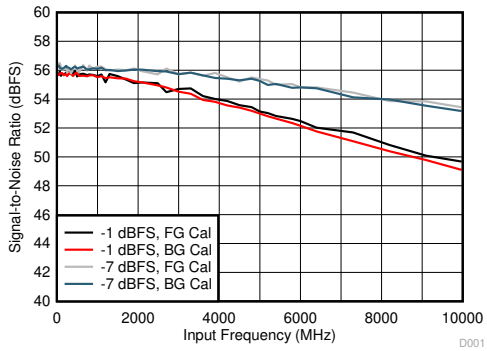


図 6-3. Serial Interface Timing

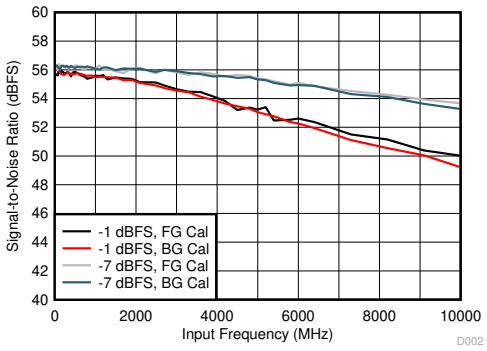
6.12 Typical Characteristics

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



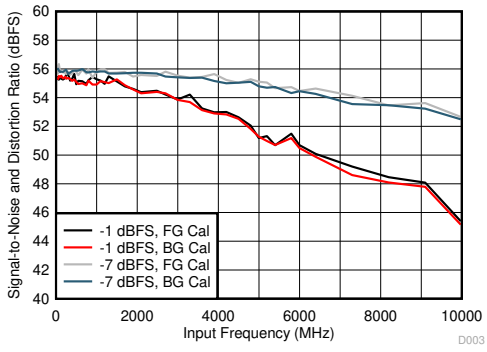
JMODE 3, f_S = 3200 MHz, foreground (FG) and background (BG) calibration

図 6-4. SNR vs Input Frequency



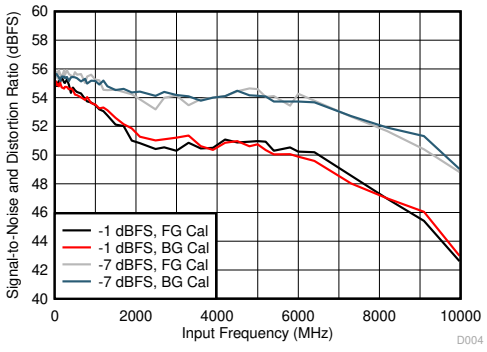
JMODE 1, f_S = 6400 MHz, FG and BG calibration

図 6-5. SNR vs Input Frequency



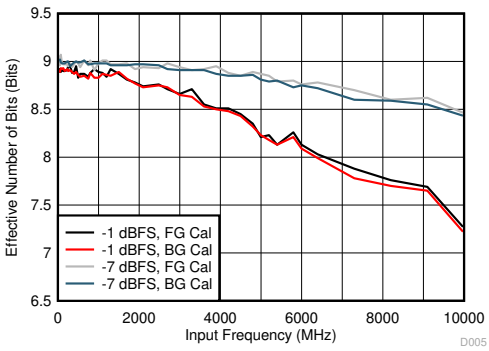
JMODE 3, f_S = 3200 MHz, FG and BG calibration

図 6-6. SINAD vs Input Frequency



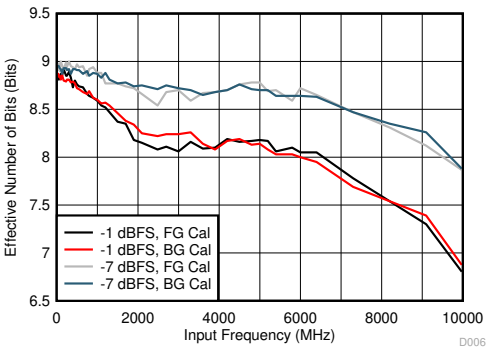
JMODE 1, f_S = 6400 MHz, FG and BG calibration

図 6-7. SINAD vs Input Frequency



JMODE 3, f_S = 3200 MHz, FG and BG calibration

図 6-8. ENOB vs Input Frequency

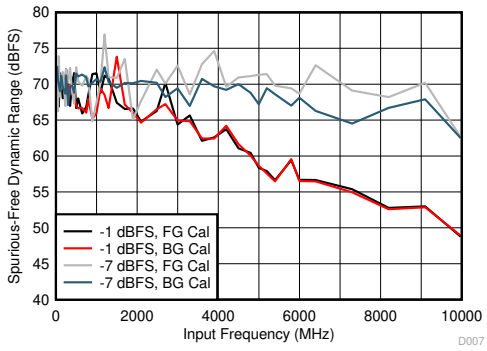


JMODE 1, f_S = 6400 MHz, FG and BG calibration

図 6-9. ENOB vs Input Frequency

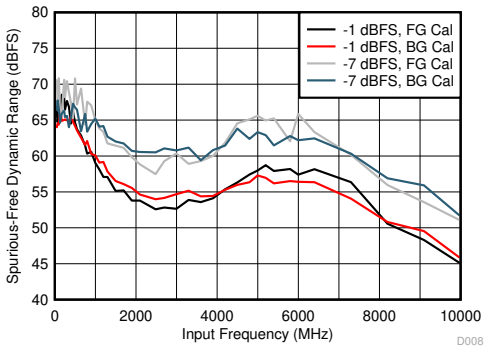
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



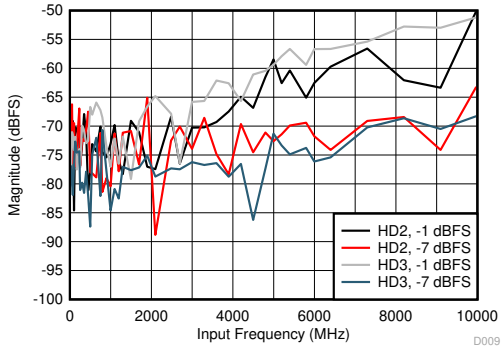
JMODE 3, f_S = 3200 MHz, FG and BG calibration

図 6-10. SFDR vs Input Frequency



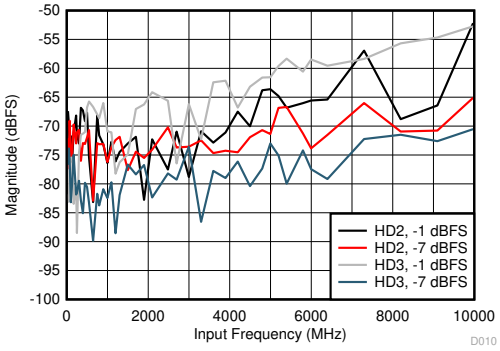
JMODE 1, f_S = 6400 MHz, FG and BG calibration

図 6-11. SFDR vs Input Frequency



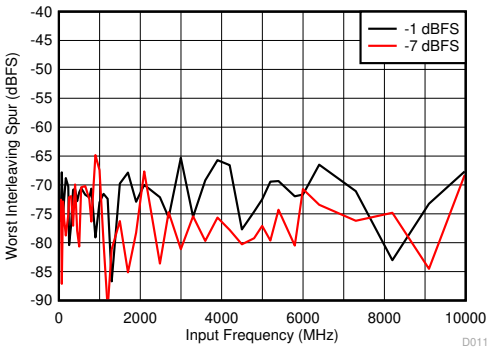
JMODE 3, f_S = 3200 MHz, FG calibration

図 6-12. HD2 and HD3 vs Input Frequency



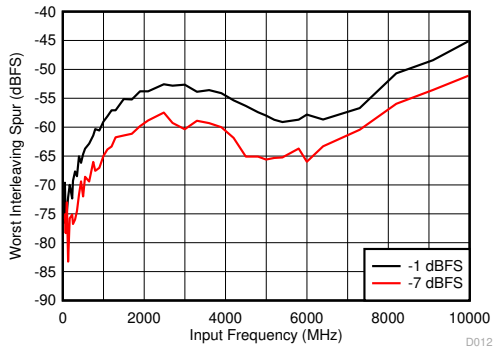
JMODE 1, f_S = 6400 MHz, FG calibration

図 6-13. HD2 and HD3 vs Input Frequency



JMODE 3, f_S = 3200 MHz, FG calibration, includes f_S / 2 – f_{IN} spur only

図 6-14. Worst Interleaving Spur vs Input Frequency

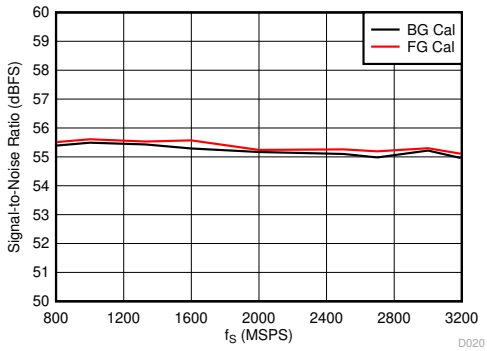


JMODE 1, f_S = 6400 MHz, FG calibration, includes f_S / 2 – f_{IN} and f_S /4 ± f_{IN} spurs only

図 6-15. Worst Interleaving Spur vs Input Frequency

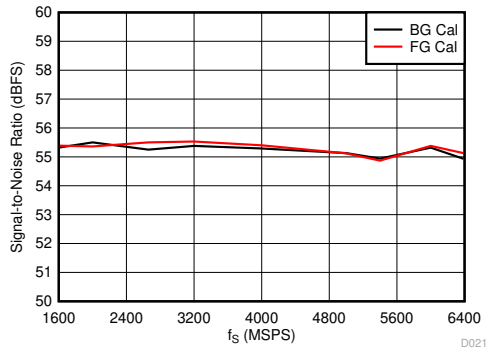
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



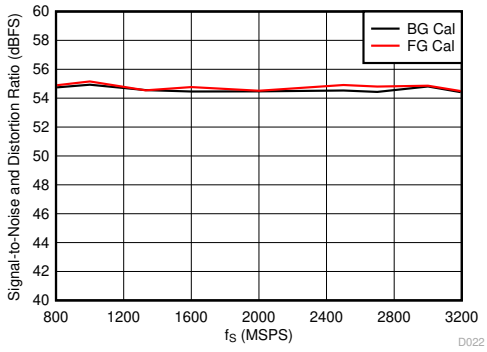
JMODE 3, FG and BG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-16. SNR vs Sampling Rate



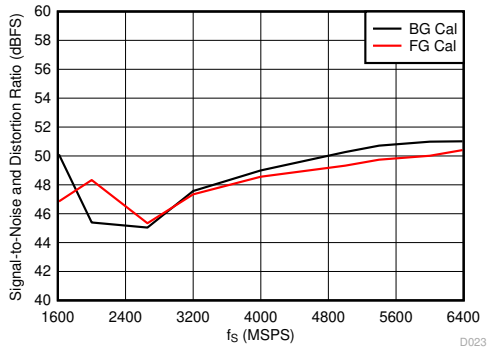
JMODE 1, FG and BG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-17. SNR vs Sampling Rate



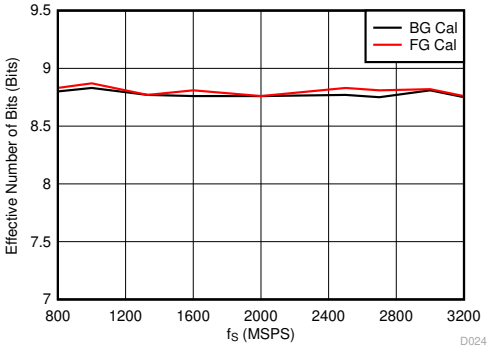
JMODE 3, FG and BG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-18. SINAD vs Sampling Rate



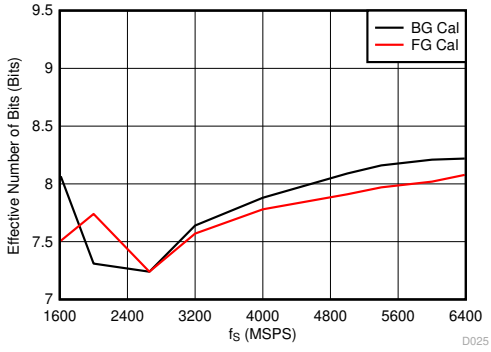
JMODE 1, FG and BG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-19. SINAD vs Sampling Rate



JMODE 3, FG and BG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-20. ENOB vs Sampling Rate

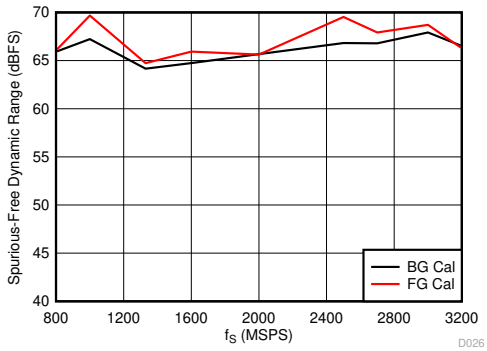


JMODE 1, FG and BG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-21. ENOB vs Sampling Rate

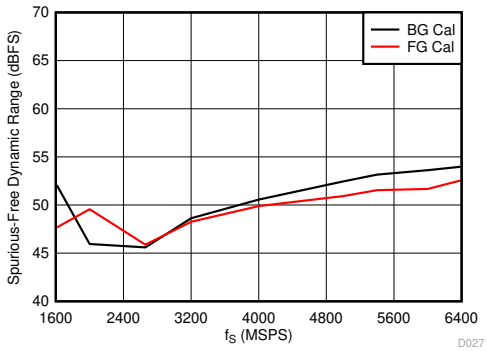
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



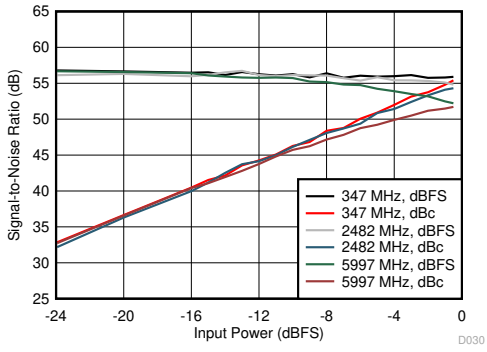
JMODE 3, FG and BG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-22. SFDR vs Sampling Rate



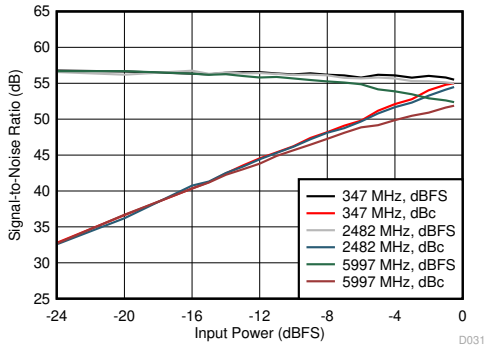
JMODE 1, FG and BG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-23. SFDR vs Sampling Rate



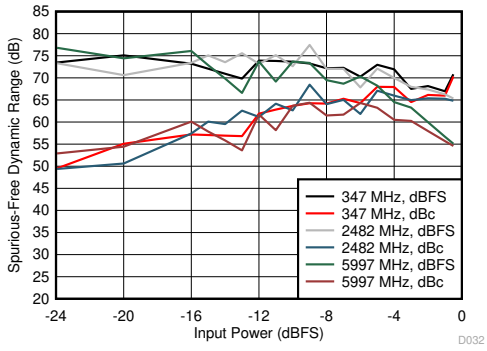
JMODE 3, FG calibration, f_S = 3200 MSPS

図 6-24. SNR vs Input Power



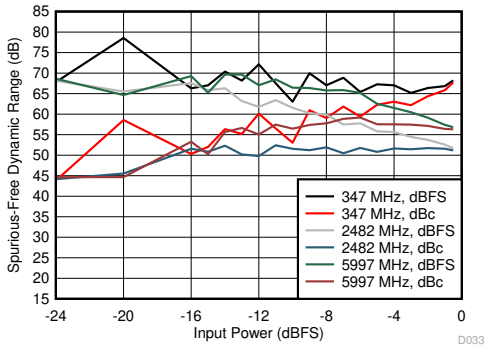
JMODE 1, FG calibration, f_S = 6400 MSPS

図 6-25. SNR vs Input Power



JMODE 3, FG calibration, f_S = 3200 MSPS

図 6-26. SFDR vs Input Power

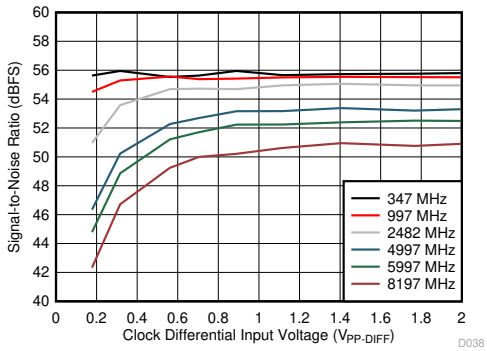


JMODE 1, FG calibration, f_S = 6400 MSPS

図 6-27. SFDR vs Input Power

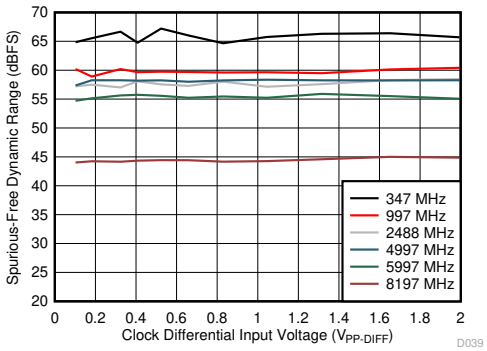
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



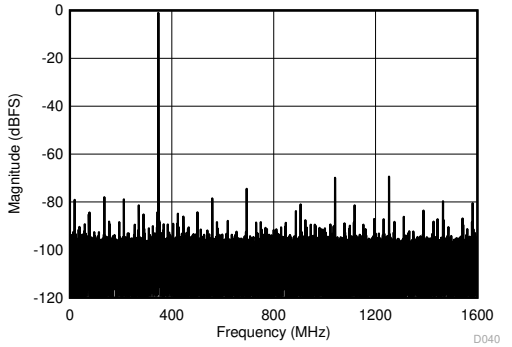
JMODE 1, FG calibration, f_S = 6400 MSPS, A_{IN} = –1 dBFS

図 6-28. SNR vs Clock Amplitude



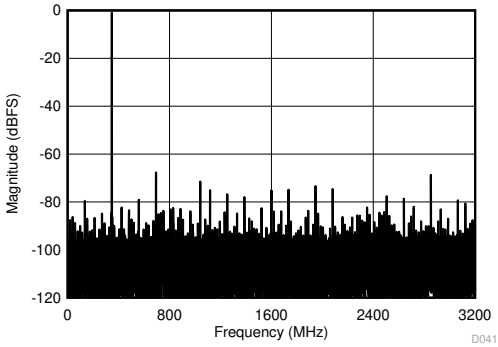
JMODE 1, FG calibration, f_S = 6400 MSPS, A_{IN} = –1 dBFS

図 6-29. SFDR vs Clock Amplitude



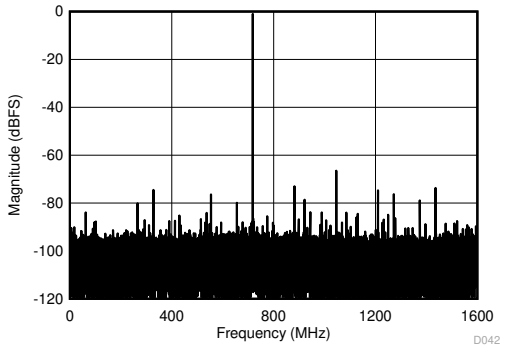
JMODE 3, FG calibration, f_S = 3200 MSPS, SNR = 56.3 dBFS, SFDR = 69 dBFS, ENOB = 9.0 bits

図 6-30. Single-Tone FFT at f_{IN} = 347 MHz, A_{IN} = –1 dBFS



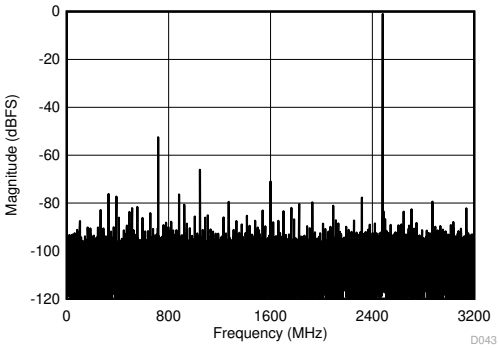
JMODE 1, FG calibration, f_S = 6400 MSPS, SNR = 55.9 dBFS, SFDR = 68 dBFS, ENOB = 8.9 bits

図 6-31. Single-Tone FFT at f_{IN} = 347 MHz, A_{IN} = –1 dBFS



JMODE 3, FG calibration, f_S = 3200 MSPS, SNR = 55.3 dBFS, SFDR = 66 dBFS, ENOB = 8.8 bits

図 6-32. Single-Tone FFT at f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

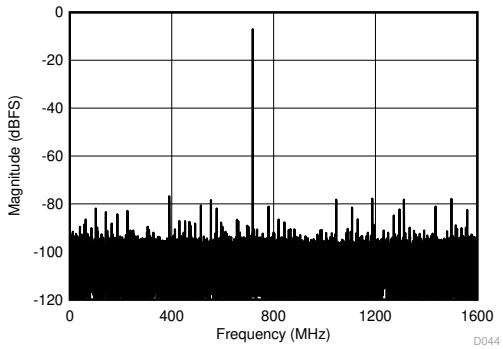


JMODE 1, FG calibration, f_S = 6400 MSPS, SNR = 55.5 dBFS, SFDR = 52 dBFS, ENOB = 8.1 bits

図 6-33. Single-Tone FFT at f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

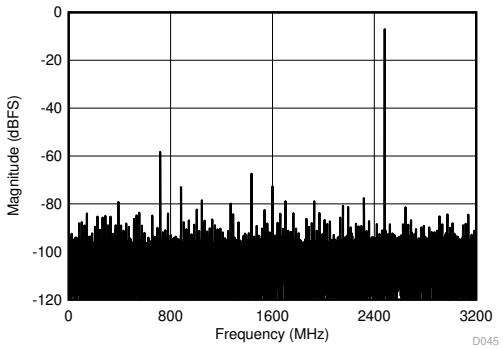
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



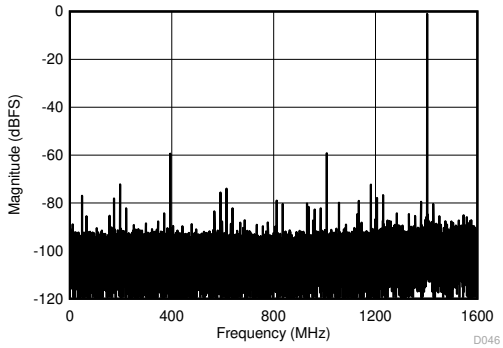
JMODE 3, FG calibration, f_S = 3200 MSPS, SNR = 56.2 dBFS, SFDR = 77 dBFS, ENOB = 9.0 bits

図 6-34. Single-Tone FFT at f_{IN} = 2482 MHz, A_{IN} = –7 dBFS



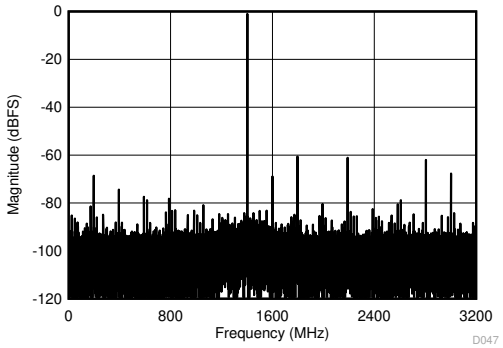
JMODE 1, FG calibration, f_S = 6400 MSPS, SNR = 56.1 dBFS, SFDR = 58 dBFS, ENOB = 8.6 bits

図 6-35. Single-Tone FFT at f_{IN} = 2482 MHz, A_{IN} = –7 dBFS



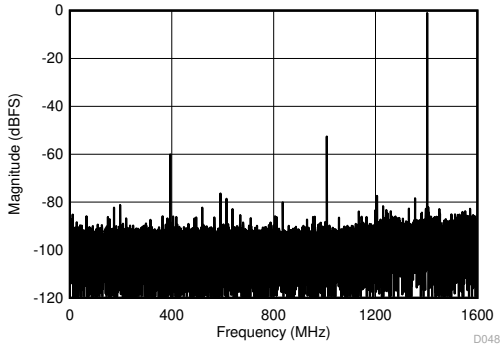
JMODE 3, FG calibration, f_S = 3200 MSPS, SNR = 53.0 dBFS, SFDR = 59 dBFS, ENOB = 8.2 bits

図 6-36. Single-Tone FFT at f_{IN} = 4997 MHz, A_{IN} = –1 dBFS



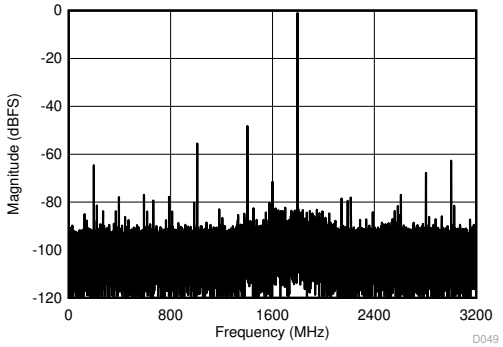
JMODE 1, FG calibration, f_S = 6400 MSPS, SNR = 53.5 dBFS, SFDR = 61 dBFS, ENOB = 8.2 bits

図 6-37. Single-Tone FFT at f_{IN} = 4997 MHz, A_{IN} = –1 dBFS



JMODE 3, FG calibration, f_S = 3200 MSPS, SNR = 51.1 dBFS, SFDR = 53 dBFS, ENOB = 7.8 bits

図 6-38. Single-Tone FFT at f_{IN} = 8197 MHz, A_{IN} = –1 dBFS

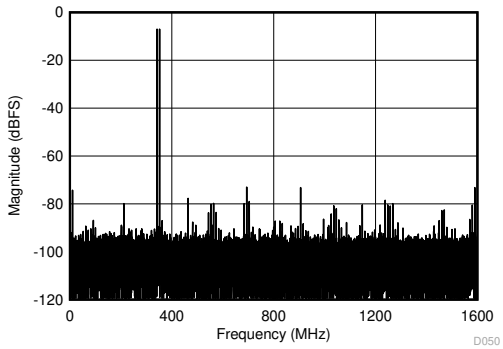


JMODE 1, FG calibration, f_S = 6400 MSPS, SNR = 51.4 dBFS, SFDR = 48 dBFS, ENOB = 7.3 bits

図 6-39. Single-Tone FFT at f_{IN} = 8197 MHz, A_{IN} = –1 dBFS

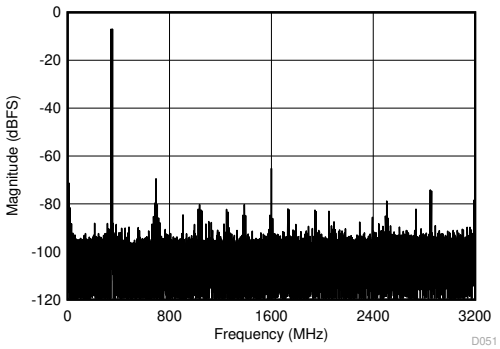
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



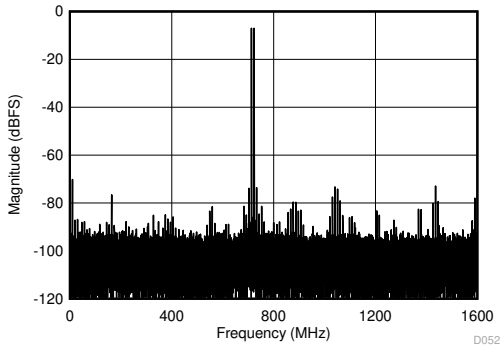
JMODE 3, FG calibration, f_S = 3200 MSPS, f_1 = 342 MHz, f_2 = 352 MHz, A_{IN} = –7 dBFS per tone, SFDR = –73 dBFS, IMD3 = –87 dBFS, IMD2 = –74 dBFS

図 6-40. Two-Tone FFT at f_{IN} = 347 MHz, A_{IN} = –1 dBFS



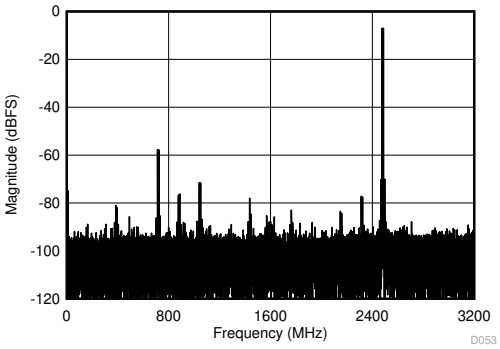
JMODE 1, FG calibration, f_S = 6400 MSPS, f_1 = 342 MHz, f_2 = 352 MHz, A_{IN} = –7 dBFS per tone, SFDR = –70 dBFS, IMD3 = –91 dBFS, IMD2 = –71 dBFS

図 6-41. Two-Tone FFT at f_{IN} = 347 MHz, A_{IN} = –1 dBFS



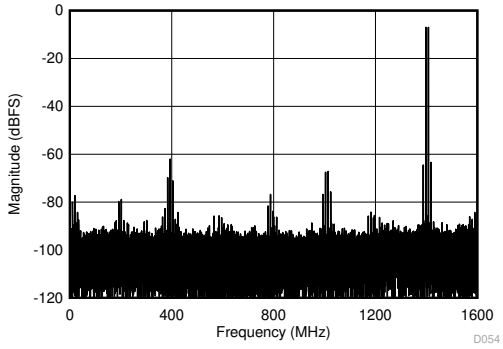
JMODE 3, FG calibration, f_S = 3200 MSPS, f_1 = 2477 MHz, f_2 = 2487 MHz, A_{IN} = –7 dBFS per tone, SFDR = –70 dBFS, IMD3 = –74 dBFS, IMD2 = –70 dBFS

図 6-42. Two-Tone FFT at f_{IN} = 2482 MHz, A_{IN} = –1 dBFS



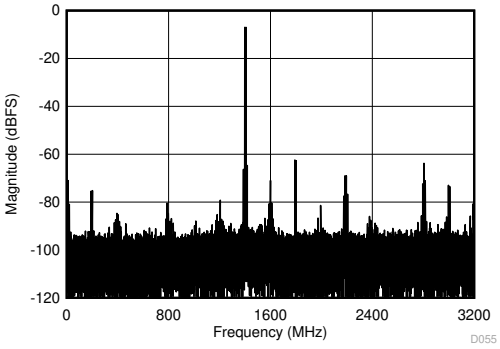
JMODE 1, FG calibration, f_S = 6400 MSPS, f_1 = 2477 MHz, f_2 = 2487 MHz, A_{IN} = –7 dBFS per tone, SFDR = –58 dBFS, IMD3 = –70 dBFS, IMD2 = –75 dBFS

図 6-43. Two-Tone FFT at f_{IN} = 2482 MHz, A_{IN} = –1 dBFS



JMODE 3, FG calibration, f_S = 3200 MSPS, f_1 = 4992 MHz, f_2 = 5002 MHz, A_{IN} = –7 dBFS per tone, SFDR = –62 dBFS, IMD3 = –63 dBFS, IMD2 = –80 dBFS

図 6-44. Two-Tone FFT at f_{IN} = 4997 MHz, A_{IN} = –1 dBFS

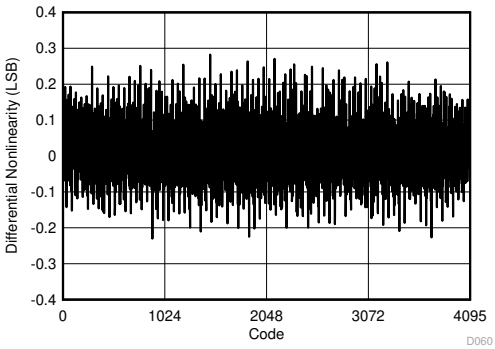


JMODE 1, FG calibration, f_S = 6400 MSPS, f_1 = 4992 MHz, f_2 = 5002 MHz, A_{IN} = –7 dBFS per tone, SFDR = –62 dBFS, IMD3 = –65 dBFS, IMD2 = –71 dBFS

図 6-45. Two-Tone FFT at f_{IN} = 4997 MHz, A_{IN} = –1 dBFS

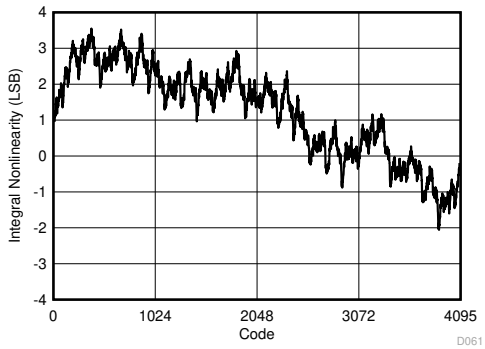
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



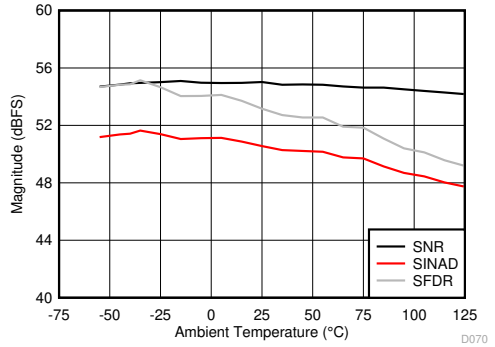
JMODE 1, FG calibration, f_S = 6400 MSPS, f_{IN} = 99.97 MHz

図 6-46. DNL vs Code



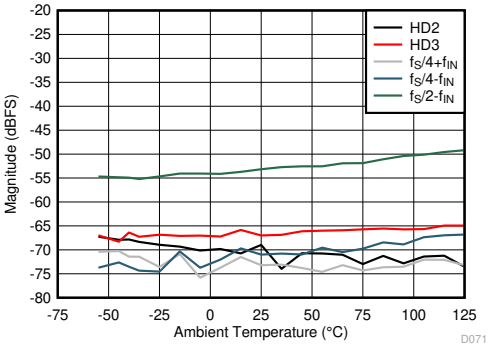
JMODE 1, FG calibration, f_S = 6400 MSPS, f_{IN} = 99.97 MHz

図 6-47. INL vs Code



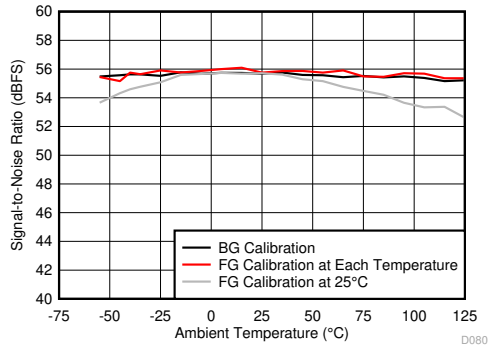
JMODE 1, BG calibration, f_S = 6400 MSPS, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-48. Performance vs Temperature



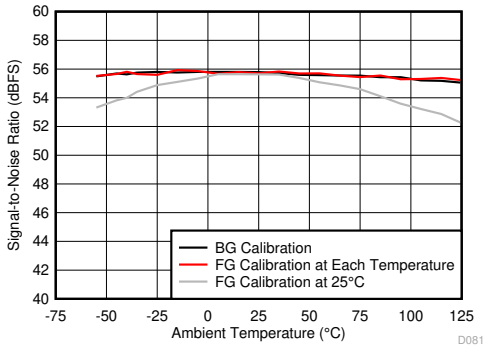
JMODE 1, FG calibration, f_S = 6400 MSPS, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-49. Performance vs Temperature



JMODE 3, f_S = 3200 MSPS, f_{IN} = 347 MHz, A_{IN} = –1 dBFS

図 6-50. SNR vs Temperature and Calibration Mode

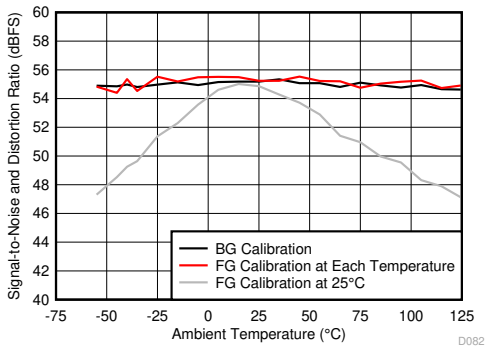


JMODE 1, f_S = 6400 MSPS, f_{IN} = 347 MHz, A_{IN} = –1 dBFS

図 6-51. SNR vs Temperature and Calibration Mode

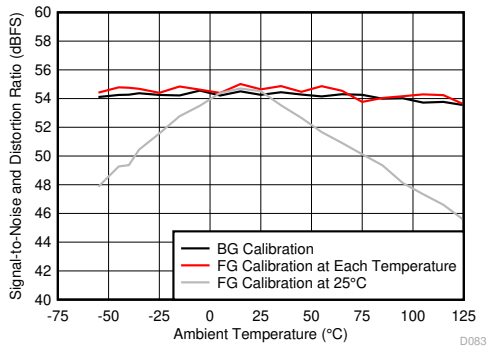
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



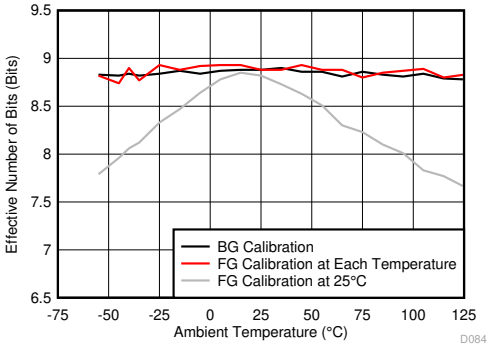
JMODE 3, f_S = 3200 MSPS, f_{IN} = 347 MHz, A_{IN} = –1 dBFS

図 6-52. SINAD vs Temperature and Calibration Mode



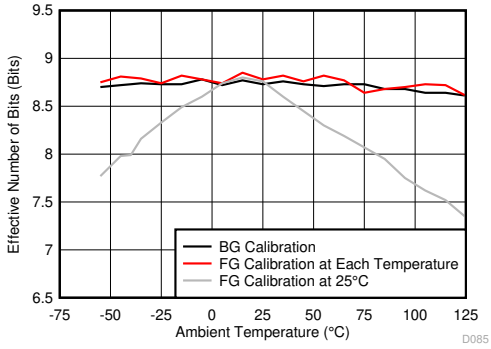
JMODE 1, f_S = 6400 MSPS, f_{IN} = 347 MHz, A_{IN} = –1 dBFS

図 6-53. SINAD vs Temperature and Calibration Mode



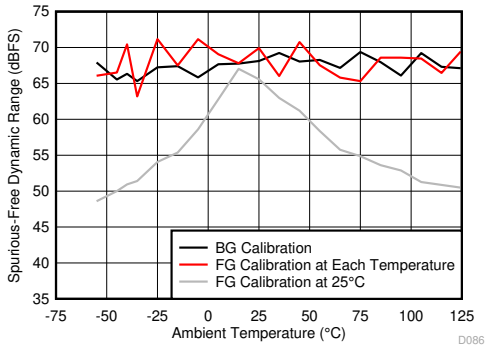
JMODE 3, f_S = 3200 MSPS, f_{IN} = 347 MHz, A_{IN} = –1 dBFS

図 6-54. ENOB vs Temperature and Calibration Mode



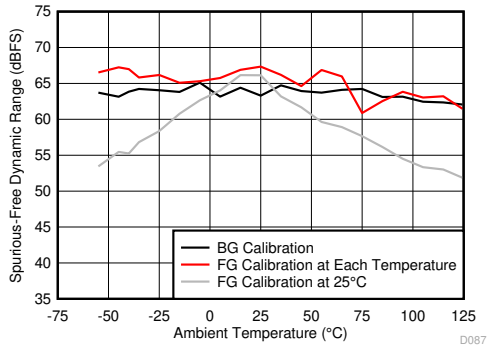
JMODE 1, f_S = 6400 MSPS, f_{IN} = 347 MHz, A_{IN} = –1 dBFS

図 6-55. ENOB vs Temperature and Calibration Mode



JMODE 3, f_S = 3200 MSPS, f_{IN} = 347 MHz, A_{IN} = –1 dBFS

図 6-56. SFDR vs Temperature and Calibration Mode

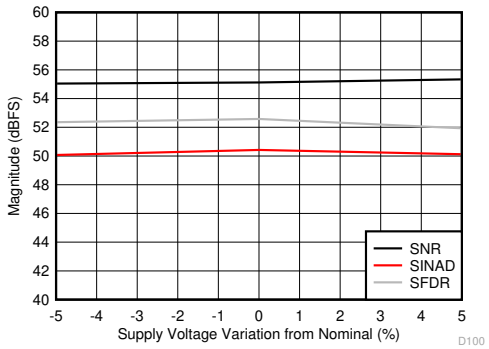


JMODE 1, f_S = 6400 MSPS, f_{IN} = 347 MHz, A_{IN} = –1 dBFS

図 6-57. SFDR vs Temperature and Calibration Mode

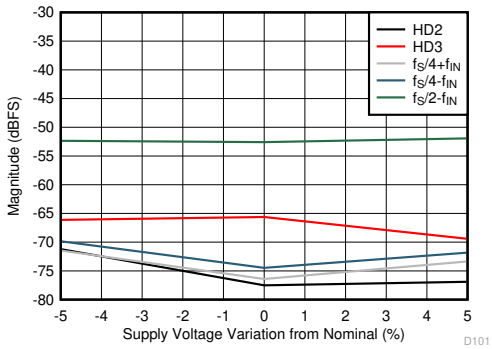
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



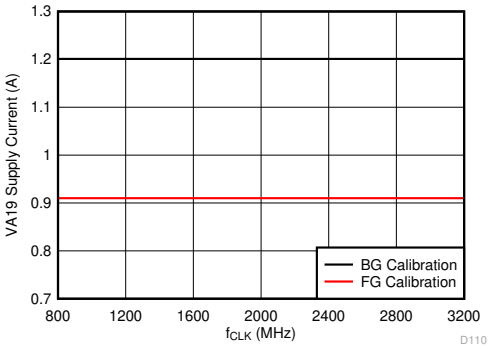
JMODE 1, FG calibration, f_S = 6400 MSPS, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-58. Performance vs Supply Voltage



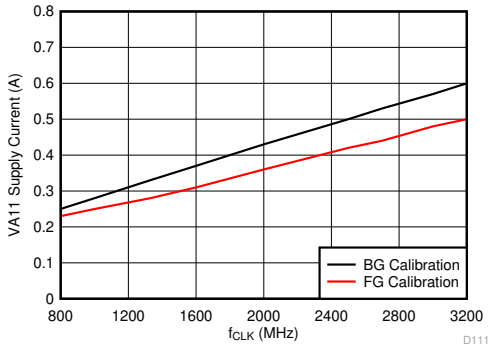
JMODE 1, FG calibration, f_S = 6400 MSPS, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-59. Performance vs Supply Voltage



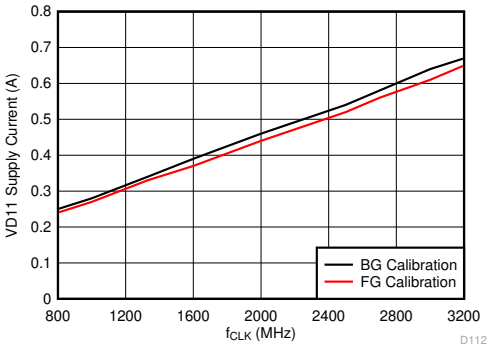
JMODE 1, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-60. VA19 Supply Current vs Clock Rate



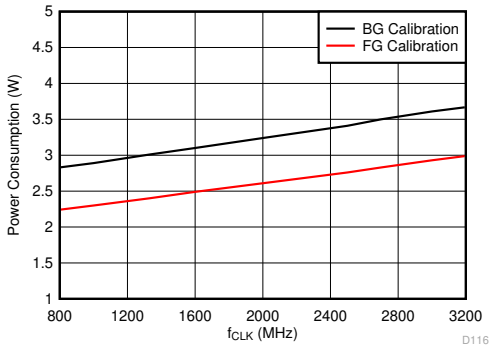
JMODE 1, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-61. VA11 Supply Current vs Clock Rate



JMODE 1, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-62. VD11 Supply Current vs Clock Rate

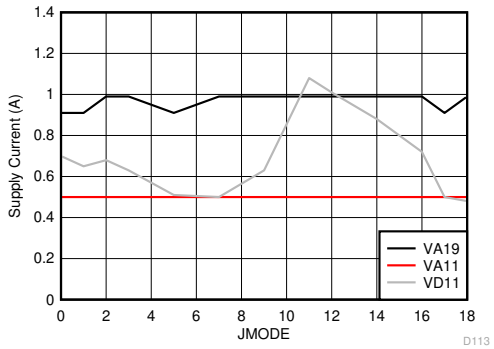


JMODE 1, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-63. Power Consumption vs Clock Rate

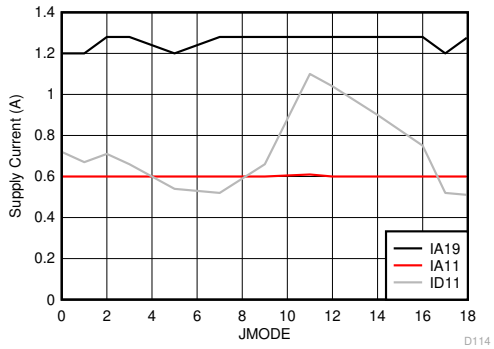
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



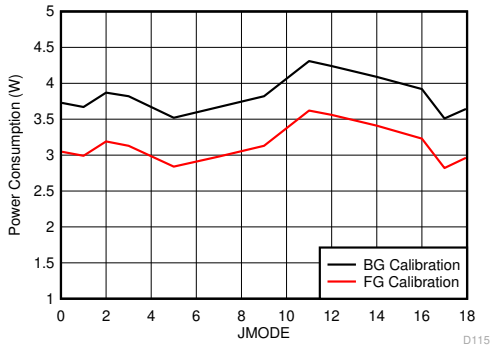
f_{CLK} = 3200 MHz, FG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-64. Supply Current vs JMODE



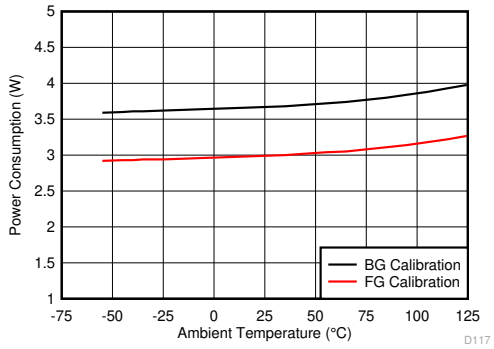
f_{CLK} = 3200 MHz, BG calibration, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-65. Supply Current vs JMODE



f_{CLK} = 3200 MHz, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-66. Power Consumption vs JMODE



JMODE 1, f_S = 6400 MSPS, f_{IN} = 2482 MHz, A_{IN} = –1 dBFS

図 6-67. Power Consumption vs Temperature

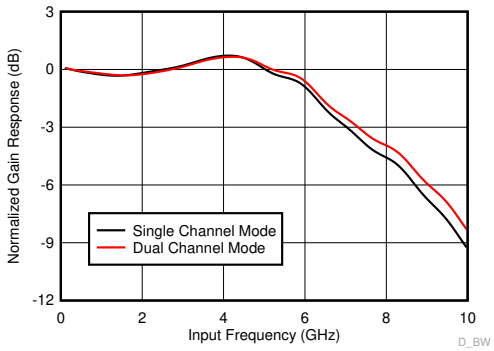
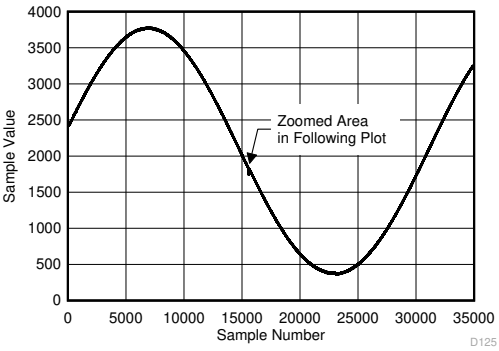


図 6-68. Gain Response vs Input Frequency

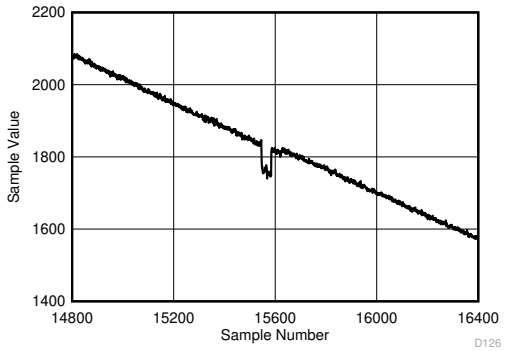


JMODE 1, f_S = 6400 MSPS, f_{IN} = 3199.9 MHz

図 6-69. Background Calibration Core Transition (AC Signal)

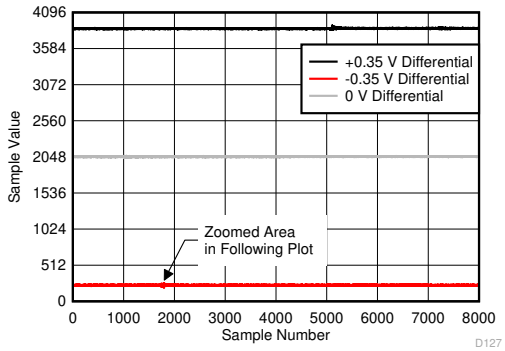
6.12 Typical Characteristics (continued)

typical values are at T_A = 25°C, nominal supply voltages, default full-scale voltage (FS_RANGE_A = FS_RANGE_B = 0xA000), input signal applied to INA± in single-channel modes, f_{IN} = 347 MHz, A_{IN} = –1 dBFS, f_{CLK} = maximum-rated clock frequency, filtered 1-V_{PP} sine-wave clock, JMODE = 1, and background calibration (unless otherwise noted); SNR results exclude DC, HD2 to HD9 and interleaving spurs; SINAD and ENOB exclude DC and f_S / 2 fixed spurs; SFDR results exclude DC and signal-independent interleaving spurs (f_S / 4 and f_S / 2 spurs)



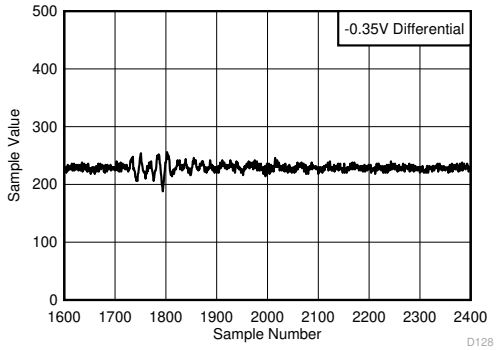
JMODE 1, f_S = 6400 MSPS, f_{IN} = 3199.9 MHz

図 6-70. Background Calibration Core Transition (AC Signal Zoomed)



JMODE 1, f_S = 6400 MSPS, DC input

図 6-71. Background Calibration Core Transition (DC Signal)



JMODE 1, f_S = 6400 MSPS, DC input

図 6-72. Background Calibration Core Transition (DC Signal Zoomed)

7 Detailed Description

7.1 Overview

The ADC12DJ3200QML-SP device is an RF-sampling, giga-sample, analog-to-digital converter (ADC) that can directly sample input frequencies from DC to above 10 GHz. In dual-channel mode, the ADC12DJ3200QML-SP can sample up to 3200 MSPS and up to 6400 MSPS in single-channel mode. Programmable tradeoffs in channel count (dual-channel mode) and Nyquist bandwidth (single-channel mode) allow development of flexible hardware that meets the needs of both high channel count or wide instantaneous signal bandwidth applications. Full-power input bandwidth (–3 dB) of 7.0 GHz, with usable frequencies exceeding the –3-dB point in both dual- and single-channel modes, allows direct RF sampling of L-band, S-band, C-band, and X-band for frequency agile systems.

ADC12DJ3200QML-SP uses a high-speed JESD204B output interface with up to 16 serialized lanes. The serial output lanes support up to 12.8 Gbps and can be configured to trade-off bit rate and number of lanes. The JESD204B block supports the subclass-1 method for deterministic latency and multi-device synchronization using SYSREF. A number of innovative synchronization features, including noiseless aperture delay (t_{AD}) adjustment and SYSREF windowing, simplify system design for multi-channel systems. Aperture delay adjustment can be used to simplify SYSREF capture, to align the sampling instance between multiple ADCs or to sample an ideal location of a front-end track and hold (T&H) amplifier output. SYSREF windowing offers a simplistic way to measure invalid timing regions of SYSREF relative to the device clock and then choose an optimal sampling location. Dual-edge sampling (DES) is implemented in single-channel mode to reduce the maximum clock rate applied to the ADC to support a wide range of clock sources and relax setup and hold timing for SYSREF capture.

Optional digital down converters (DDC) are available in dual-channel mode. The DDC block provides a range of decimation settings that allow the device to work in ultra-wideband, wideband, and more-narrow-band receive systems. Decimation reduces the interface rate or the number of lanes required to transfer the data to the logic device. Additionally, data from a single ADC channel (in dual-channel mode) can be sent to separate DDC blocks for multi-band receive applications or to support redundant logic devices.

ADC12DJ3200QML-SP provides foreground and background calibration options for gain, offset and static linearity errors. Foreground calibration is run at system startup or at specified times during which the ADC is offline and not sending data to the logic device. Background calibration allows the ADC to run continually while the cores are calibrated in the background so that the system does not experience downtime. The calibration routine is also used to match the gain and offset between sub-ADC cores to minimize spurious artifacts from time interleaving.

The ADC12DJ3200QML-SP has a single event latch-up tolerance to 120 MeV-cm^2/mg and a total ionizing dose to 300 krad (Si) for radiation-sensitive applications. Serial programming interface and programming registers are protected against radiation upsets while other key circuitry is monitored by alarms for quick detection of upsets.

7.2 Functional Block Diagram

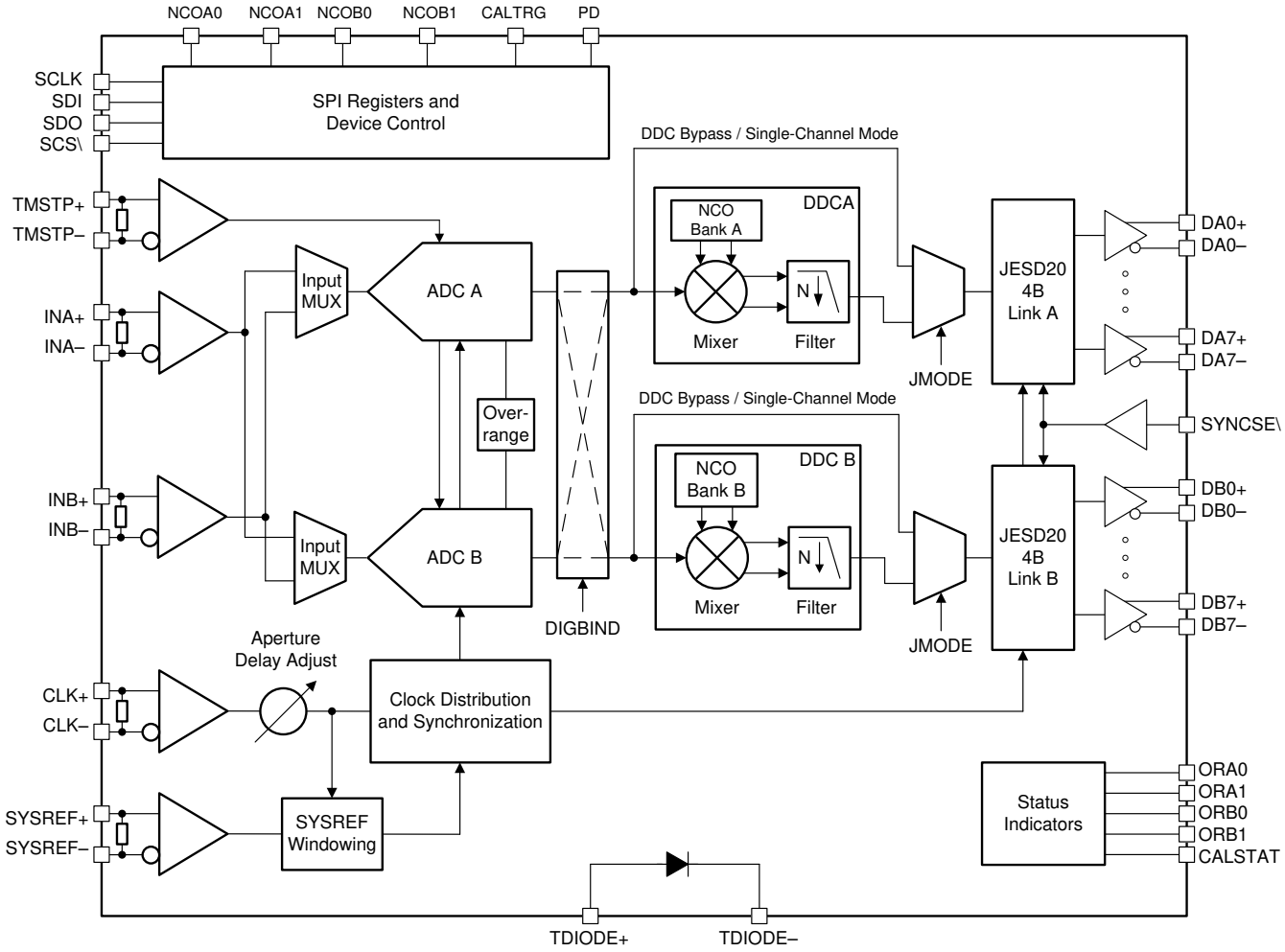


図 7-1. Functional Block Diagram

7.3 Feature Description

7.3.1 Analog Inputs

The analog inputs of the ADC12DJ3200QML-SP have internal buffers to enable high input bandwidth and to isolate sampling capacitor glitch noise from the input circuit. Analog inputs must be driven differentially because operation with a single-ended signal results in degraded performance. Both AC-coupling and DC-coupling of the analog inputs is supported. The analog inputs are designed for an input common-mode voltage (V_{CMI}) of 0 V, which is terminated internally through single-ended, 50-Ω resistors to ground (GND) on each input pin. DC-coupled input signals must have a common-mode voltage that meets the device input common-mode requirements specified as V_{CMI} in the *Recommended Operating Conditions* table. The 0-V input common-mode voltage simplifies the interface to split-supply, fully-differential amplifiers and to a variety of transformers and baluns. The ADC12DJ3200QML-SP includes internal analog input protection to protect the ADC inputs during overranged input conditions; see the *Analog Input Protection* section. 図 7-2 shows a simplified analog input model.

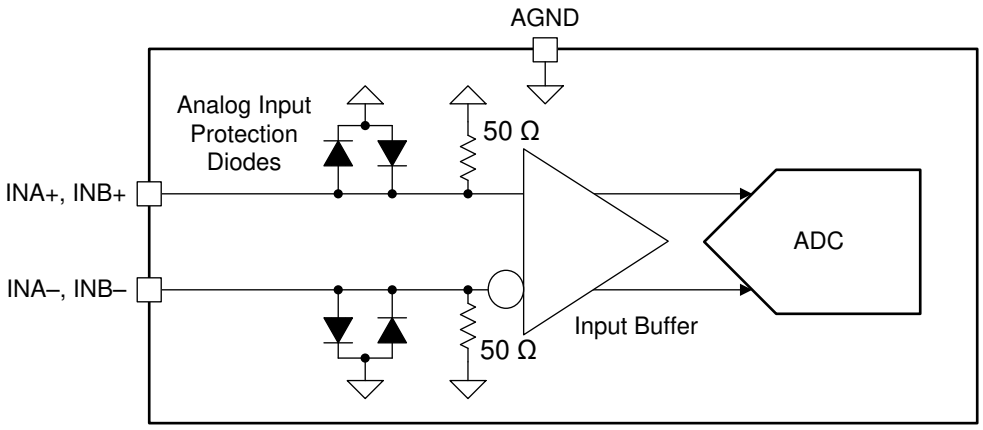


図 7-2. ADC12DJ3200QML-SP Analog Input Internal Termination and Protection Diagram

There is minimal degradation in analog input bandwidth when using single-channel mode versus dual-channel mode. In single-channel mode, INA± is strongly recommended to be used as the input to the ADC because ADC performance is optimized for INA±. However, either analog input (INA+ and INA– or INB+ and INB–) can be used. Using INB± results in degraded performance unless custom trim routines are used to optimize performance for INB± in each device. The desired input can be chosen using SINGLE_INPUT in the input mux control register.

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INA± is strongly recommended to be used as the input to the ADC in single-channel mode for optimized performance.

7.3.1.1 Analog Input Protection

The analog inputs are protected against overdrive conditions by internal clamping diodes that are capable of sourcing or sinking input currents during overrange conditions, see the voltage and current limits in the *Absolute Maximum Ratings* table. The overrange protection is also defined for a peak RF input power in the *Absolute Maximum Ratings* table, which is frequency independent. Operation above the maximum conditions listed in the *Recommended Operating Conditions* table results in an increase in failure-in-time (FIT) rate, so the system must correct the overdrive condition as quickly as possible. 図 7-2 shows the analog input protection diodes.

7.3.1.2 Full-Scale Voltage (V_{FS}) Adjustment

Input full-scale voltage (V_{FS}) adjustment is available, in fine increments, for each analog input through the FS_RANGE_A register setting (see the INA full-scale range adjust register) and FS_RANGE_B register setting (see the INB full-scale range adjust register) for INA± and INB±, respectively. The available adjustment range is

specified in the *Electrical Characteristics: DC Specifications* table. Larger full-scale voltages improve SNR and noise floor (in dBFS/Hz) performance, but can degrade harmonic distortion. The full-scale voltage adjustment is useful for matching the full-scale range of multiple ADCs when developing a multi-converter system or for external interleaving of multiple ADC12DJ3200QML-SPs to achieve higher sampling rates.

7.3.1.3 Analog Input Offset Adjust

The input offset voltage for each input can be adjusted through the OADJ_x_INy registers (registers 0x08A and 0x095), where x represents the ADC core (A, B, or C) and y represents the analog input (INA± or INB±). The adjustment range is approximately 28 mV to –28 mV differential. See the *Calibration Modes and Trimming* section for more information.

7.3.2 ADC Core

The ADC12DJ3200QML-SP consists of a total of six ADC cores. The cores are interleaved for higher sampling rates and swapped on-the-fly for calibration as required by the operating mode. This section highlights the theory and key features of the ADC cores.

7.3.2.1 ADC Theory of Operation

The differential voltages at the analog inputs are captured by the rising edge of CLK± in dual-channel mode or by the rising and falling edges of CLK± in single-channel mode. After capturing the input signal, the ADC converts the analog voltage to a digital value by comparing the voltage to the internal reference voltage. If the voltage on INA– or INB– is higher than the voltage on INA+ or INB+, respectively, then the digital output is a negative 2's complement value. If the voltage on INA+ or INB+ is higher than the voltage on INA– or INB–, respectively, then the digital output is a positive 2's complement value. 式 1 can calculate the differential voltage at the input pins from the digital output.

$$V_{IN} = \frac{Code}{2^N} V_{FS} \quad (1)$$

where

- Code is the signed decimation output code (for example, –2048 to +2047)
- N is the ADC resolution
- and V_{FS} is the full-scale input voltage of the ADC as specified in the *セクション 6.3* table, including any adjustment performed by programming FS_RANGE_A or FS_RANGE_B

7.3.2.2 ADC Core Calibration

ADC core calibration is required to optimize the analog performance of the ADC cores. Calibration must be repeated when operating conditions change significantly, namely temperature, in order to maintain optimal performance. The ADC12DJ3200QML-SP has a built-in calibration routine that can be run as a foreground operation or a background operation. Foreground operation requires ADC downtime, where the ADC is no longer sampling the input signal, to complete the process. Background calibration can be used to overcome this limitation and allow constant operation of the ADC. See the *Calibration Modes and Trimming* section for detailed information on each mode.

7.3.2.3 ADC Overrange Detection

To make sure that system gain management has the quickest possible response time, a low-latency configurable overrange function is included. The overrange function works by monitoring the converted 12-bit samples at the ADC to quickly detect if the ADC is near saturation or already in an overrange condition. The absolute value of the upper 8 bits of the ADC data are checked against two programmable thresholds, OVR_T0 and OVR_T1. These thresholds apply to both channel A and channel B in dual-channel mode. 表 7-1 lists how an ADC sample is converted to an absolute value for a comparison of the thresholds.

表 7-1. Conversion of ADC Sample for Overrange Comparison

ADC SAMPLE (Offset Binary)	ADC SAMPLE (2's Complement)	ABSOLUTE VALUE	UPPER 8 BITS USED FOR COMPARISON
1111 1111 1111 (4095)	0111 1111 1111 (+2047)	111 1111 1111 (2047)	1111 1111 (255)
1111 1111 0000 (4080)	0111 1111 0000 (+2032)	111 1111 0000 (2032)	1111 1110 (254)
1000 0000 0000 (2048)	0000 0000 0000 (0)	000 0000 0000 (0)	0000 0000 (0)
0000 0001 0000 (16)	1000 0001 0000 (–2032)	111 1111 0000 (2032)	1111 1110 (254)
0000 0000 0000 (0)	1000 0000 0000 (–2048)	111 1111 1111 (2047)	1111 1111 (255)

If the upper 8 bits of the absolute value equal or exceed the OVR_T0 or OVR_T1 thresholds during the monitoring period, then the overrange bit associated with the threshold is set to 1, otherwise the overrange bit is 0. In dual-channel mode, the overrange status can be monitored on the ORA0 and ORA1 pins for channel A and the ORB0 and ORB1 pins for channel B, where ORx0 corresponds to the OVR_T0 threshold and ORx1 corresponds to the OVR_T1 threshold. In single-channel mode, the overrange status for the OVR_T0 threshold is determined by monitoring both the ORA0 and ORB0 outputs and the OVR_T1 threshold is determined by monitoring both ORA1 and ORB1 outputs. In single-channel mode, the two outputs for each threshold must be OR'd together to determine whether an overrange condition occurred. OVR_N can be used to set the output pulse duration from the last overrange event. 表 7-2 lists the overrange pulse lengths for the various OVR_N settings (see the overrange configuration register). In decimation modes (only in the JMODEs where $\overline{CS}$ = 1 in 表 7-18), the overrange status is also embedded into the output data samples. For complex decimation modes, the OVR_T0 threshold status is embedded as the LSB along with the upper 15 bits of every complex I sample and the OVR_T1 threshold status is embedded as the LSB along with the upper 15 bits of every complex Q sample. For real decimation modes, the OVR_T0 threshold status is embedded as the LSB of every even-numbered sample and the OVR_T1 threshold status is embedded as the LSB of every odd-numbered sample. 表 7-3 lists the outputs, related data samples, threshold settings, and the monitoring period equation. The embedded overrange bit goes high if the associated channel exceeds the associated overrange threshold within the monitoring period set by OVR_N. Use 表 7-3 to calculate the monitoring period.

表 7-2. Overrange Monitoring Period for the ORA0, ORA1, ORB0, and ORB1 Outputs

OVR_N	OVERRANGE PULSE LENGTH SINCE LAST OVERRANGE EVENT (DEVCLK Cycles)
0	8
1	16
2	32
3	64
4	128
5	256
6	512
7	1024

表 7-3. Threshold and Monitoring Period for Embedded Overrange Indicators in Dual-Channel Decimation Modes

OVERRANGE INDICATOR	ASSOCIATED THRESHOLD	DECIMATION TYPE	OVERRANGE STATUS EMBEDDED IN	MONITORING PERIOD (ADC Samples)
ORA0	OVR_T0	Real decimation (JMODE 9)	Channel A even-numbered samples	2^{OVR_N+1} (1)
		Complex down-conversion (JMODE 10-16, except JMODE 12)	Channel A in-phase (I) samples	2^{OVR_N} (1)
ORA1	OVR_T1	Real decimation (JMODE 9)	Channel A odd-numbered samples	2^{OVR_N+1} (1)
		Complex down-conversion (JMODE 10-16, except JMODE 12)	Channel A quadrature (Q) samples	2^{OVR_N} (1)
ORB0	OVR_T0	Real decimation (JMODE 9)	Channel B even-numbered samples	2^{OVR_N+1} (1)
		Complex down-conversion (JMODE 10-16, except JMODE 12)	Channel B in-phase (I) samples	2^{OVR_N} (1)
ORB1	OVR_T1	Real decimation (JMODE 9)	Channel B odd-numbered samples	2^{OVR_N+1} (1)
		Complex down-conversion (JMODE 10-16, except JMODE 12)	Channel B quadrature (Q) samples	2^{OVR_N} (1)

(1) OVR_N is the monitoring period register setting.

Typically, the OVR_T0 threshold can be set near the full-scale value (228 for example). When the threshold is triggered, a typical system can turn down the system gain to avoid clipping. The OVR_T1 threshold can be set much lower. For example, the OVR_T1 threshold can be set to 64 (peak input voltage of −12 dBFS). If the input signal is strong, the OVR_T1 threshold is tripped occasionally. If the input is quite weak, the threshold is never tripped. The downstream logic device monitors the OVR_T1 bit. If OVR_T1 stays low for an extended period of time, then the system gain can be increased until the threshold is occasionally tripped (meaning the peak level of the signal is above −12 dBFS).

7.3.2.4 Code Error Rate (CER)

ADC cores can generate bit errors within a sample, often called *code errors (CER)* or referred to as *sparkle codes*, resulting from metastability caused by non-ideal comparator limitations. The ADC12DJ3200QML-SP uses a unique ADC architecture that inherently allows significant code error rate improvements from traditional pipelined flash or successive approximation register (SAR) ADCs. The code error rate of the ADC12DJ3200QML-SP is multiple orders of magnitude better than what can be achieved in alternative architectures at equivalent sampling rates providing significant signal reliability improvements.

7.3.3 Timestamp

The TMSTP+ and TMSTP– differential input can be used as a time-stamp input to mark a specific sample based on the timing of an external trigger event relative to the sampled signal. TIMESTAMP_EN (see the LSB control bit output register) must be set in order to use the timestamp feature and output the timestamp data. When enabled, the LSB of the 12-bit ADC digital output reports the status of the TMSTP± input. In effect, the 12-bit output sample consists of the upper 11-bits of the 12-bit converter and the LSB of the 12-bit output sample is the output of a parallel 1-bit converter (TMSTP±) with the same latency as the ADC core. In the 8-bit operating modes, the LSB of the 8-bit output sample is used to output the timestamp status. The trigger must be applied to the differential TMSTP+ and TMSTP– inputs. The trigger can be asynchronous to the ADC sampling clock and is sampled at approximately the same time as the analog input. Timestamp cannot be used when a JMODE with decimation is selected and instead SYSREF must be used to achieve synchronization through the JESD204B subclass-1 method for achieving deterministic latency.

7.3.4 Clocking

The clocking subsystem of the ADC12DJ3200QML-SP has two input signals, device clock (CLK+, CLK–) and SYSREF (SYSREF+, SYSREF–). Within the clocking subsystem there is a noiseless aperture delay adjustment (t_{AD} adjust), a clock duty cycle corrector, and a SYSREF capture block. 図 7-3 shows the clocking subsystem.

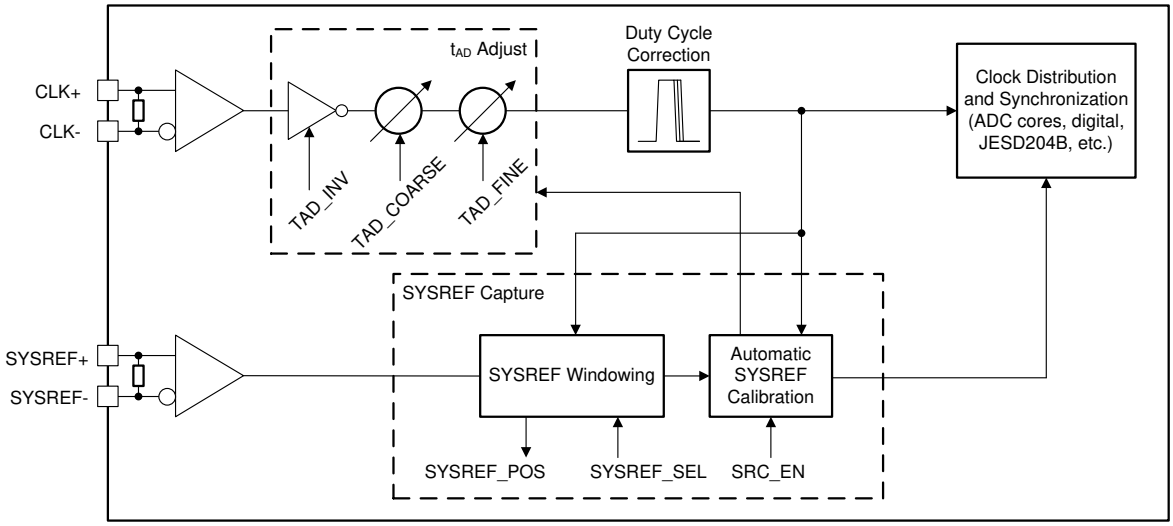

図 7-3. ADC12DJ3200QML-SP Clocking Subsystem

The device clock is used as the sampling clock for the ADC core as well as the clocking for the digital processing and serializer outputs. Use a low-noise (low jitter) device clock to maintain high signal-to-noise ratio (SNR) within the ADC. In dual-channel mode, the analog input signal for each input is sampled on the rising edge of the device clock. In single-channel mode, both the rising and falling edges of the device clock are used to capture the analog signal to reduce the maximum clock rate required by the ADC. A noiseless aperture delay adjustment (t_{AD} adjust) allows the user to shift the sampling instance of the ADC in fine steps in order to synchronize multiple ADC12DJ3200QML-SPs or to fine-tune system latency. Duty cycle correction is implemented in the ADC12DJ3200QML-SP to ease the requirements on the external device clock while maintaining high performance. 表 7-4 summarizes the device clock interface in dual-channel mode and single-channel mode.

表 7-4. Device Clock vs Mode of Operation

MODE OF OPERATION	SAMPLING RATE VS f_{CLK}	SAMPLING INSTANT
Dual-channel mode	1 × f_{CLK}	Rising edge
Single-channel mode	2 × f_{CLK}	Rising and falling edge

SYSREF is a system timing reference used for JESD204B subclass-1 implementations of deterministic latency. SYSREF is used to achieve deterministic latency and for multi-device synchronization. SYSREF must be captured by the correct device clock edge in order to achieve repeatable latency and synchronization. The ADC12DJ3200QML-SP includes SYSREF windowing and automatic SYSREF calibration to ease the requirements on the external clocking circuits and to simplify the synchronization process. SYSREF can be implemented as a single pulse or as a periodic clock. In periodic implementations, SYSREF must be equal to, or an integer division of, the local multiframe clock frequency. 式 2 is used to calculate valid SYSREF frequencies.

$$f_{SYSREF} = \frac{R \times f_{CLK}}{10 \times F \times K \times n} \quad (2)$$

where

- R and F are set by the JMODE setting (see 表 7-18)
- f_{CLK} is the device clock frequency (CLK±)
- K is the programmed multiframe length (see 表 7-18 for valid K settings)

- and n is any positive integer

7.3.4.1 Noiseless Aperture Delay Adjustment (t_{AD} Adjust)

The ADC12DJ3200QML-SP contains a delay adjustment on the device clock (sampling clock) input path, called t_{AD} adjust, that can be used to shift the sampling instance within the device in order to align sampling instances among multiple devices or for external interleaving of multiple ADC12DJ3200QML-SPs. Further, t_{AD} adjust can be used for automatic SYSREF calibration to simplify synchronization; see the *Automatic SYSREF Calibration* section. Aperture delay adjustment is implemented in a way that adds no additional noise to the clock path, however a slight degradation in aperture jitter (t_{AJ}) is possible at large values of TAD_COARSE because of internal clock path attenuation. The degradation in aperture jitter results in minor SNR degradations at high input frequencies (see t_{AJ} in the *Switching Characteristics* table). This feature is programmed using TAD_INV, TAD_COARSE, and TAD_FINE in the DEVCLK timing adjust ramp control register.. Setting TAD_INV inverts the input clock resulting in a delay equal to half the clock period. 表 7-5 summarizes the step sizes and ranges of the TAD_COARSE and TAD_FINE variable analog delays. All three delay options are independent and can be used in conjunction. All clocks within the device are shifted by the programmed t_{AD} adjust amount, which results in a shift of the timing of the JESD204B serialized outputs and affects the capture of SYSREF.

表 7-5. t_{AD} Adjust Adjustment Ranges

ADJUSTMENT PARAMETER	ADJUSTMENT STEP	DELAY SETTINGS	MAXIMUM DELAY
TAD_INV	1 / (f_{CLK} × 2)	1	1 / (f_{CLK} × 2)
TAD_COARSE	See $t_{TAD(STEP)}$ in the *Switching Characteristics* table	256	See $t_{TAD(MAX)}$ in the *Switching Characteristics* table
TAD_FINE	See $t_{TAD(STEP)}$ in the *Switching Characteristics* table	256	See $t_{TAD(MAX)}$ in the *Switching Characteristics* table

In order to maintain timing alignment between converters, stable and matched power-supply voltages and device temperatures must be provided.

Aperture delay adjustment can be changed on-the-fly during normal operation but may result in brief upsets to the JESD204B data link. Use TAD_RAMP to reduce the probability of the JESD204B link losing synchronization; see the *Aperture Delay Ramp Control (TAD_RAMP)* section.

7.3.4.2 Aperture Delay Ramp Control (TAD_RAMP)

The ADC12DJ3200QML-SP contains a function to gradually adjust the t_{AD} adjust setting towards the newly written TAD_COARSE value. This functionality allows the t_{AD} adjust setting to be adjusted with minimal internal clock circuitry glitches. The TAD_RAMP_RATE parameter allows either a slower (one TAD_COARSE LSB per 256 t_{CLK} cycles) or faster ramp (four TAD_COARSE LSBs per 256 t_{CLK} cycles) to be selected. The TAD_RAMP_EN parameter enables the ramp feature and any subsequent writes to TAD_COARSE initiate a new cramp.

7.3.4.3 SYSREF Capture for Multi-Device Synchronization and Deterministic Latency

The clocking subsystem is largely responsible for achieving multi-device synchronization and deterministic latency. The ADC12DJ3200QML-SP uses the JESD204B subclass-1 method to achieve deterministic latency and synchronization. Subclass 1 requires that the SYSREF signal be captured by a deterministic device clock (CLK±) edge at each system power-on and at each device in the system. This requirement imposes setup and hold constraints on SYSREF relative to CLK±, which can be difficult to meet at giga-sample clock rates over all system operating conditions. The ADC12DJ3200QML-SP includes a number of features to simplify this synchronization process and to relax system timing constraints:

- The ADC12DJ3200QML-SP uses dual-edge sampling (DES) in single-channel mode to reduce the CLK± input frequency by half and double the timing window for SYSREF (see 表 7-4)
- A SYSREF position detector (relative to CLK±) and selectable SYSREF sampling position aid the user in meeting setup and hold times over all conditions; see the *SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing)* section

- Easy-to-use automatic SYSREF calibration uses the aperture timing adjust block (t_{AD} adjust) to shift the ADC sampling instance based on the phase of SYSREF (rather than adjusting SYSREF based on the phase of the ADC sampling instance); see the *Automatic SYSREF Calibration* section

7.3.4.3.1 SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing)

The SYSREF windowing block is used to first detect the position of SYSREF relative to the CLK± rising edge and then to select a desired SYSREF sampling instance, which is a delay version of CLK±, to maximize setup and hold timing margins. In many cases a single SYSREF sampling position (SYSREF_SEL) is sufficient to meet timing for all systems (device-to-device variation) and conditions (temperature and voltage variations). However, this feature can also be used by the system to expand the timing window by tracking the movement of SYSREF as operating conditions change or to remove system-to-system variation at production test by finding a unique optimal value at nominal conditions for each system.

This section describes proper usage of the SYSREF windowing block. First, apply the device clock and SYSREF to the device. The location of SYSREF relative to the device clock cycle is determined and stored in the SYSREF_POS bits of the SYSREF capture position register. At least three rising edges must be applied to the SYSREF± input before SYSREF_POS is valid. Each bit of SYSREF_POS represents a potential SYSREF sampling position. If a bit in SYSREF_POS is set to 1, then the corresponding SYSREF sampling position has a potential setup or hold violation. Upon determining the valid SYSREF sampling positions (the positions of SYSREF_POS that are set to 0) the desired sampling position can be chosen by setting SYSREF_SEL in the clock control register 0 to the value corresponding to that SYSREF_POS position. In general, the middle sampling position between two setup and hold instances is chosen. Ideally, SYSREF_POS and SYSREF_SEL are performed at the nominal operating conditions of the system (temperature and supply voltage) to provide maximum margin for operating condition variations. This process can be performed at final test and the optimal SYSREF_SEL setting can be stored for use at every system power up. Further, SYSREF_POS can be used to characterize the skew between CLK± and SYSREF± over operating conditions for a system by sweeping the system temperature and supply voltages. For systems that have large variations in CLK± to SYSREF± skew, this characterization can be used to track the optimal SYSREF sampling position as system operating conditions change. In general, a single value can be found that meets timing over all conditions for well-matched systems, such as those where CLK± and SYSREF± come from a single clocking device.

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SYSREF_SEL must be set to 0 when using automatic SYSREF calibration; see the *Automatic SYSREF Calibration* section.

The step size between each SYSREF_POS sampling position can be adjusted using SYSREF_ZOOM. When SYSREF_ZOOM is set to 0, the delay steps are coarser. When SYSREF_ZOOM is set to 1, the delay steps are finer. See the *Switching Characteristics* table for delay step sizes when SYSREF_ZOOM is enabled and disabled. In general, SYSREF_ZOOM is recommended to always be used (SYSREF_ZOOM = 1) unless a transition region (defined by 1's in SYSREF_POS) is not observed, which can be the case for low clock rates. Bits 0 and 23 of SYSREF_POS are always be set to 1 because there is insufficient information to determine if these settings are close to a timing violation, although the actual valid window can extend beyond these sampling positions. The value programmed into SYSREF_SEL is the decimal number representing the desired bit location in SYSREF_POS. 表 7-6 lists some example SYSREF_POS readings and the optimal SYSREF_SEL settings. Although 24 sampling positions are provided by the SYSREF_POS status register, SYSREF_SEL only allows selection of the first 16 sampling positions, corresponding to SYSREF_POS bits 0 to 15. The additional SYSREF_POS status bits are intended only to provide additional knowledge of the SYSREF valid window. In general, lower values of SYSREF_SEL are selected because of delay variation over supply voltage, however in the fourth example a value of 15 provides additional margin and can be selected instead.

表 7-6. Examples of SYSREF_POS Readings and SYSREF_SEL Selections

SYSREF_POS[23:0]			OPTIMAL SYSREF_SEL SETTING
0x02E[7:0] (Largest Delay)	0x02D[7:0](1)	0x02C[7:0](1) (Smallest Delay)	
b10000000	b0110000 0	b00011001	8 or 9

表 7-6. Examples of SYSREF_POS Readings and SYSREF_SEL Selections (continued)

SYSREF_POS[23:0]			OPTIMAL SYSREF_SEL SETTING
0x02E[7:0] (Largest Delay)	0x02D[7:0](1)	0x02C[7:0](1) (Smallest Delay)	
b10011000	b00000000	b00110001	12
b10000000	b01100000	b0 0000001	6 or 7
b10000000	b00000011	b00000001	4 or 15
b10001100	b01100011	b00011001	6

(1) Red coloration indicates the bits that are selected, as given in the last column of this table.

7.3.4.3.2 Automatic SYSREF Calibration

The ADC12DJ3200QML-SP has an automatic SYSREF calibration feature to alleviate the often challenging setup and hold times associated with capturing SYSREF for giga-sample data converters. Automatic SYSREF calibration uses the t_{AD} adjust feature to shift the device clock to maximize the SYSREF setup and hold times or to align the sampling instance based on the SYSREF rising edge.

The ADC12DJ3200QML-SP must have a proper device clock applied and be programmed for normal operation before starting the automatic SYSREF calibration. When ready to initiate automatic SYSREF calibration, a continuous SYSREF signal must be applied. SYSREF must be a continuous (periodic) signal when using the automatic SYSREF calibration. Start the calibration process by setting SRC_EN high in the SYSREF calibration enable register after configuring the automatic SYSREF calibration using the SRC_CFG register. Upon setting SRC_EN high, the ADC12DJ3200QML-SP searches for the optimal t_{AD} adjust setting until the device clock falling edge is internally aligned to the SYSREF rising edge. TAD_DONE in the SYSREF calibration status register can be monitored to make sure that the SYSREF calibration has finished. By aligning the device clock falling edge with the SYSREF rising edge, automatic SYSREF calibration maximizes the internal SYSREF setup and hold times relative to the device clock and also sets the sampling instant based on the SYSREF rising edge. After the automatic SYSREF calibration finishes, the rest of the startup procedure can be performed to finish bringing up the system.

For multi-device synchronization, the SYSREF rising edge timing must be matched at all devices and therefore trace lengths must be matched from a common SYSREF source to each ADC12DJ3200QML-SP. Any skew between the SYSREF rising edge at each device results in additional error in the sampling instance between devices, however repeatable deterministic latency from system startup to startup through each device must still be achieved. No other design requirements are needed in order to achieve multi-device synchronization as long as a proper elastic buffer release point is chosen in the JESD2048 receiver.

図 7-4 shows a timing diagram of the SYSREF calibration procedure. The optimized setup and hold times are shown as $t_{SU(OPT)}$ and $t_{H(OPT)}$, respectively. Device clock and SYSREF are referred to as *internal* in this diagram because the phase of the internal signals are aligned within the device and not to the external (applied) phase of the device clock or SYSREF.

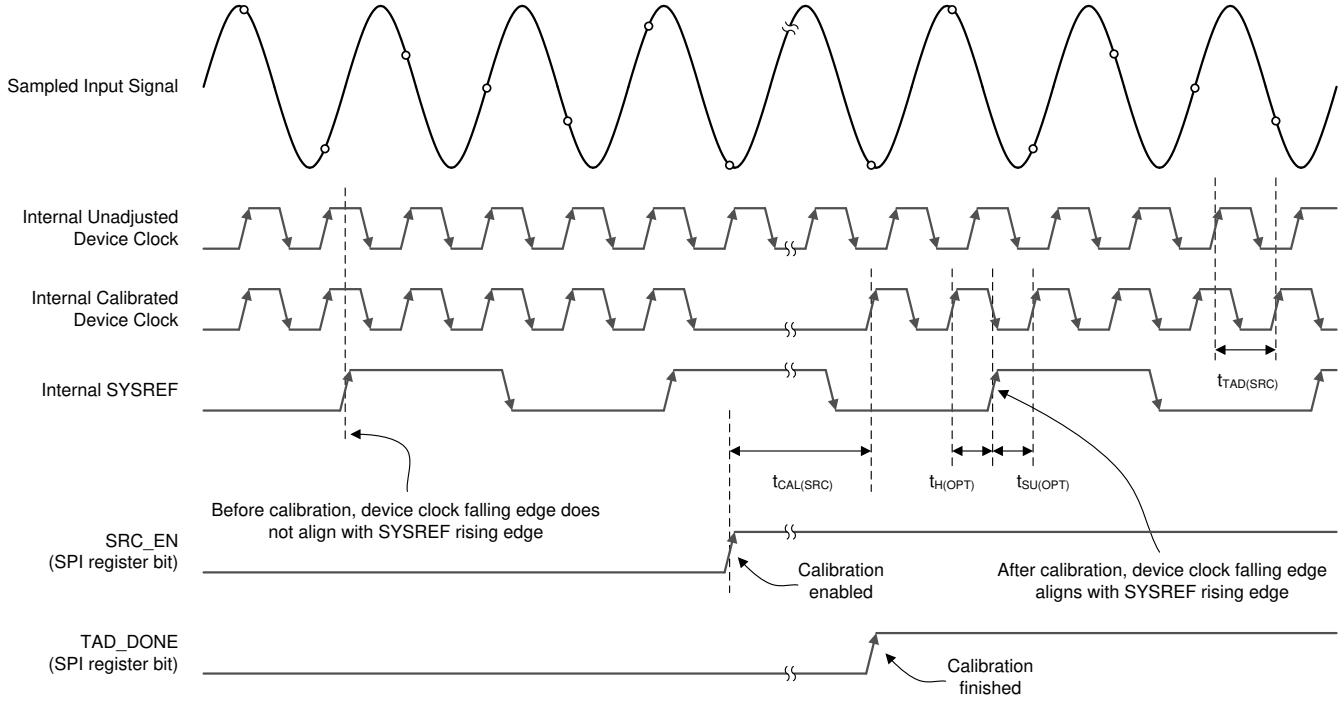

図 7-4. SYSREF Calibration Timing Diagram

When finished, the t_{AD} adjust setting found by the automatic SYSREF calibration can be read from SRC_TAD in the SYSREF calibration status register. After calibration, the system continues to use the calibrated t_{AD} adjust setting for operation until the system is powered down. However, if desired, the user can then disable the SYSREF calibration and fine-tune the t_{AD} adjust setting according to the systems needs. Alternatively, the use of the automatic SYSREF calibration can be done at product test (or periodic recalibration) of the optimal t_{AD} adjust setting for each system. This value can be stored and written to the TAD register (TAD_INV, TAD_COARSE, and TAD_FINE) upon system startup.

Do not run the SYSREF calibration when the ADC calibration (foreground or background) is running. If background calibration is the desired use case, disable the background calibration when the SYSREF calibration is used, then reenable the background calibration after TAD_DONE goes high. SYSREF_SEL in the clock control register 0 must be set to 0 when using SYSREF calibration.

SYSREF calibration searches the TAD_COARSE delays using both noninverted (TAD_INV = 0) and inverted clock polarity (TAD_INV = 1) to minimize the required TAD_COARSE setting in order to minimize loss on the clock path to reduce aperture jitter (t_{AJ}).

7.3.5 Digital Down Converters (Dual-Channel Mode Only)

After converting the analog voltage to a digital value, the digitized sample can either be sent directly to the JESD204B interface block (DDC bypass) or sent to the digital down conversion (DDC) block for frequency conversion and decimation (in dual-channel mode only). Frequency conversion and decimation allow a specific frequency band to be selected and output in the digital data stream while reducing the effective data rate and interface speed or width. The DDC is designed such that the digital processing does not degrade the noise spectral density (NSD) performance of the ADC. 図 7-5 illustrates the digital down converter for channel A of the ADC12DJ3200QML-SP. Channel B has the same structure with the input data selected by DIG_BIND_B and the NCO selection mux controlled by pins NCOB[1:0] or through CSELB[1:0].

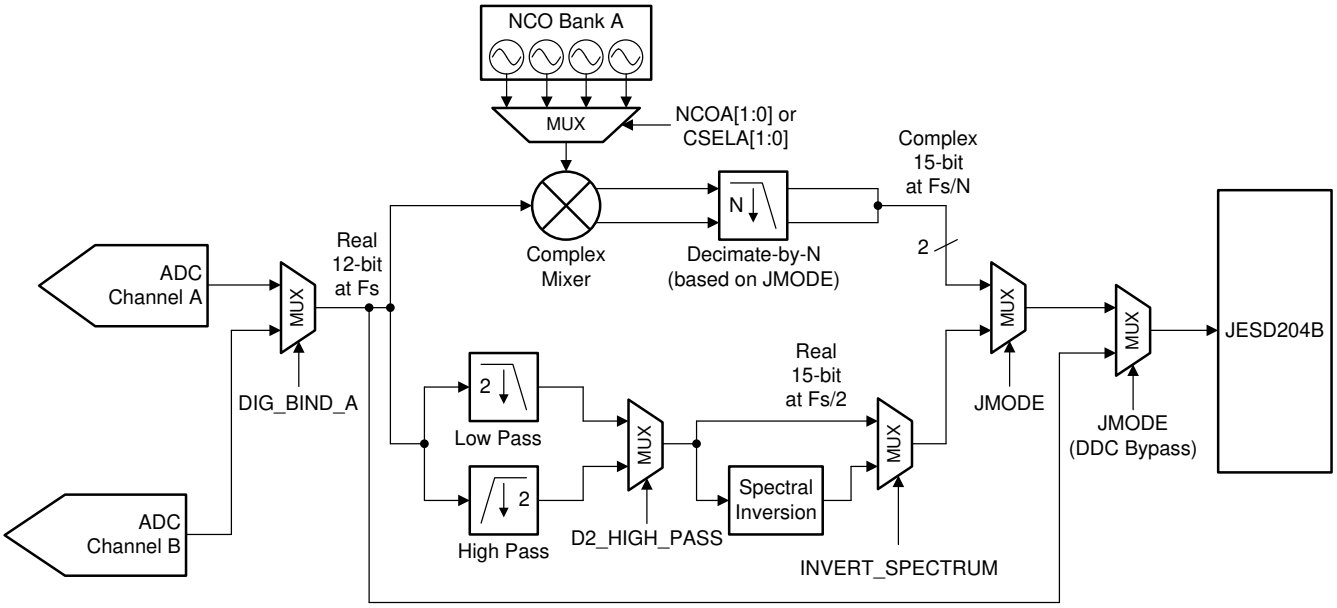

図 7-5. Channel A Digital Down Conversion Block (Dual-Channel Mode Only)

7.3.5.1 Numerically-Controlled Oscillator and Complex Mixer

The DDC contains a complex numerically-controlled oscillator (NCO) and a complex mixer. 式 3 shows the complex exponential sequence generated by the oscillator.

$$x[n] = e^{j\omega n} \quad (3)$$

The frequency (ω) is specified by a 32-bit register setting. The complex exponential sequence is multiplied by the real input from the ADC to mix the desired carrier to a frequency equal to $f_{IN} + f_{NCO}$, where f_{IN} is the analog input frequency after aliasing (in undersampling systems) and f_{NCO} is the programmed NCO frequency.

7.3.5.1.1 NCO Fast Frequency Hopping (FFH)

Fast frequency hopping (FFH) is made possible by each DDC having four independent NCOs that can be controlled by the NCOA0 and NCOA1 pins for DDC A and the NCOB0 and NCOB1 pins for DDC B. Each NCO has independent frequency settings (see the *Basic NCO Frequency Setting Mode* section) and initial phase settings (see the *NCO Phase Offset Setting* section) that can be set independently. Further, all NCOs have independent phase accumulators that continue to run when the specific NCO is not selected, allowing the NCOs to maintain their phase between selection so that downstream processing does not need to perform carrier recovery after each hop, for instance.

NCO hopping occurs when the NCO GPIO pins change state. The pins are controlled asynchronously and therefore synchronous switching is not possible. Associated latencies are demonstrated in 図 7-6, where t_{TX} and t_{ADC} are provided in the *Switching Characteristics* table. All latencies in 表 7-7 are approximations only.

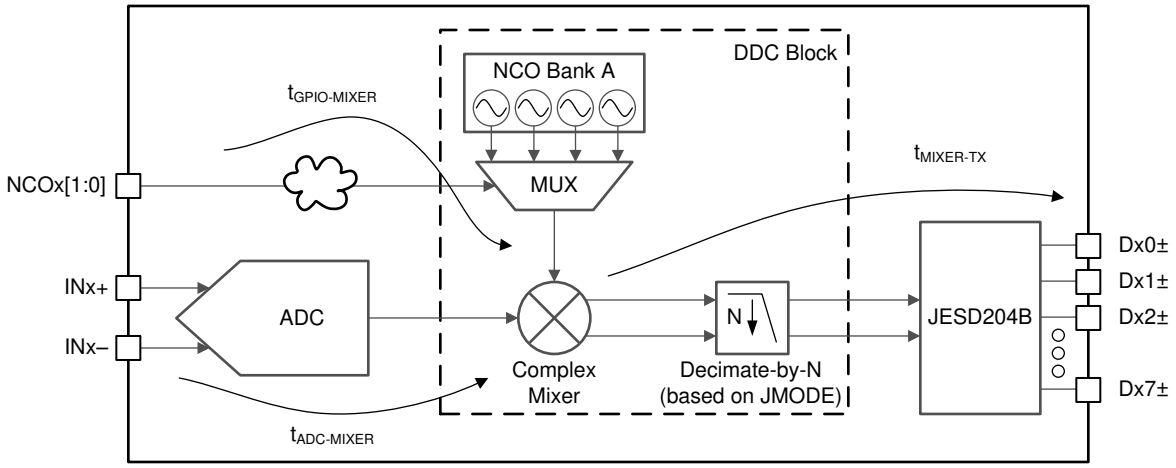

図 7-6. NCO Fast Frequency Hopping Latency Diagram

表 7-7. NCO Fast Frequency Hopping Latency Definitions

LATENCY PARAMETER	VALUE OR CALCULATION	UNITS
$t_{GPIO-MIXER}$	~36 to ~40	t_{CLK} cycles
$t_{ADC-MIXER}$	~36	t_{CLK} cycles
$t_{MIXER-TX}$	$(t_{TX} + t_{ADC}) - t_{ADC-MIXER}$	t_{CLK} cycles

7.3.5.1.2 NCO Selection

Within each channel DDC, four different frequency and phase settings are available for use. Each of the four settings use a different phase accumulator within the NCO. Because all four phase accumulators are independent and continuously running, rapid switching between different NCO frequencies is possible allowing for phase coherent frequency hopping.

The specific frequency-phase pair used for each channel is selected through the NCOA[1:0] or NCOB[1:0] input pins when CMODE is set to 1. Alternatively, the selected NCO can be chosen through SPI by CSELA for DDC A and CSELB for DDC B by setting CMODE to 0 (default). The logic table for NCO selection is provided in 表 7-8 for both the GPIO and SPI selection options.

表 7-8. Logic Table for NCO Selection Using GPIO or SPI

NCO SELECTION	CMODE	NCOx1	NCOx0	CSELx[1]	CSELx[0]
NCO 0 using GPIO	1	0	0	X	X
NCO 1 using GPIO	1	0	1	X	X
NCO 2 using GPIO	1	1	0	X	X
NCO 3 using GPIO	1	1	1	X	X
NCO 0 using SPI	0	X	X	0	0
NCO 1 using SPI	0	X	X	0	1
NCO 2 using SPI	0	X	X	1	0
NCO 3 using SPI	0	X	X	1	1

The frequency for each phase accumulator is programmed independently through the FREQAx, FREQBx (x = 0 to 3) and, optionally, NCO_RDIV register settings. The phase offset for each accumulator is programmed independently through the PHASEAx and PHASEBx (x = 0 to 3) register settings.

7.3.5.1.3 Basic NCO Frequency Setting Mode

In basic NCO frequency-setting mode (NCO_RDIV = 0x0000), the NCO frequency setting is set by the 32-bit register value, FREQAx and FREQBx (x = 0 to 3). The NCO frequency for DDC A can be calculated using 式 4, where FREQAx can be replaced by FREQBx to calculate the NCO frequency for DDC B.

$$f_{(NCO)} = \text{FREQAx} \times 2^{-32} \times f_{(DEVCLK)} \text{ (x = 0 – 3)} \quad (4)$$

注

Changing the FREQAx and FREQBx register settings during operation results in a non-deterministic NCO phase. If deterministic phase is required, the NCOs must be resynchronized; see the *NCO Phase Synchronization* section.

7.3.5.1.4 Rational NCO Frequency Setting Mode

In basic NCO frequency mode, the frequency step size is very small and many frequencies can be synthesized, but sometimes an application requires very specific frequencies that fall between two frequency steps. For example with f_S equal to 2457.6 MHz and a desired $f_{(NCO)}$ equal to 5.02 MHz, the value for FREQAx is 8773085.867. Truncating the fractional portion results in an $f_{(NCO)}$ equal to 5.0199995 MHz, which is not the desired frequency.

To produce the desired frequency, the NCO_RDIV parameter is used to force the phase accumulator to arrive at specific frequencies without error. First, select a frequency step size ($f_{(STEP)}$) that is appropriate for the NCO frequency steps required. The typical value of $f_{(STEP)}$ is 10 kHz. Next, use 式 5 to program the NCO_RDIV value.

$$\text{NCO\_RDIV} = \frac{\left(f_{DEVCLK} / f_{STEP}\right)}{64} \quad (5)$$

The result of 式 5 must be an integer value. If the value is not an integer, adjust either of the parameters until the result is an integer value.

For example, select a value of 1920 for NCO_RDIV.

注

NCO_RDIV values larger than 8192 can degrade the NCO SFDR performance and are not recommended.

Now use 式 6 to calculate the FREQAx register value.

$$FREQAx = round\left(2^{32} \times f_{NCO} / f_{DEVCLK}\right) \quad (6)$$

Alternatively, the following equations can be used:

$$N = \frac{f_{(NCO)}}{f_{(STEP)}} \quad (7)$$

$$FREQAx = round\left(2^{26} \times N / NCO\_RDIV\right) \quad (8)$$

表 7-9 lists common values for NCO_RDIV in 10-kHz frequency steps.

表 7-9. Common NCO_RDIV Values (For 10-kHz Frequency Steps)

f_{CLK} (MHz)	NCO_RDIV
3200	5000
3072	4800
2949.12	4608
2457.6	3840
1966.08	3072
1600	2500
1474.56	2304
1228.8	1920

7.3.5.1.5 NCO Phase Offset Setting

The NCO phase-offset setting for each NCO is set by the 16-bit register value PHASEAx and PHASEBx (where x = 0 to 3). The value is left-justified into a 32-bit field and then added to the phase accumulator.

Use 式 9 to calculate the phase offset in radians.

$$\Phi(rad) = PHASEA/Bx \times 2^{-16} \times 2 \times \pi \ (x=0 \text{ to } 3) \quad (9)$$

7.3.5.1.6 NCO Phase Synchronization

The NCOs must be synchronized after setting or changing the value of FREQAx or FREQBx. NCO synchronization is performed when the JESD204B link is initialized or by SYSREF, based on the settings of NCO_SYNC_ILA and NCO_SYNC_NEXT. The procedures are as follows for the JESD204B initialization procedure and the SYSREF procedure for both DC-coupled and AC-coupled SYSREF signals.

NCO synchronization using the JESD204B SYNC signal ($\overline{SYNCSE}$ or TMSTP±):

1. The device must be programmed for normal operation
2. Set NCO_SYNC_ILA to 1
3. Set JESD_EN to 0
4. Program FREQAx, FREQBx, PHASEAx, and PHASEBx to the desired settings

5. In the JESD204B receiver (logic device), deassert the $\overline{\text{SYNC}}$ signal by setting $\overline{\text{SYNC}}$ high
6. Set JESD_EN to 1
7. Assert the $\overline{\text{SYNC}}$ signal by setting $\overline{\text{SYNC}}$ low in the JESD204B receiver to start the code group synchronization (CGS) process
8. After achieving CGS, deassert the $\overline{\text{SYNC}}$ signal by setting $\overline{\text{SYNC}}$ high at the same time for all ADCs to be synchronized and verify that the SYNC setup and hold times are met (as specified in the *セクション 6.9* table)

NCO synchronization using SYSREF (DC-coupled):

1. The device must be programmed for normal operation
2. Set JESD_EN to 1 to start the JESD204B link (the SYNC signal can respond as normal during the CGS process)
3. Program FREQAx, FREQBx, PHASEAx, and PHASEBx to the desired settings
4. Verify that SYSREF is disabled (held low)
5. Arm NCO synchronization by setting NCO_SYNC_NEXT to 1
6. Issue a single SYSREF pulse to all ADCs to synchronize NCOs within all devices

NCO synchronization using SYSREF (AC-coupled):

1. The device must be programmed for normal operation
2. Set JESD_EN to 1 to start the JESD204B link (the SYNC signal can respond as normal during the CGS process)
3. Program FREQAx, FREQBx, PHASEAx, and PHASEBx to the desired settings
4. Run SYSREF continuously
5. Arm NCO synchronization by setting NCO_SYNC_NEXT to 1 at the same time at all ADCs by timing the rising edge of SCLK for the last data bit (LSB) at the end of the SPI write so that the SCLK rising edge occurs after a SYSREF rising edge and early enough before the next SYSREF rising edge so that the trigger is armed before the next SYSREF rising edge (a long SYSREF period is recommended)
6. NCOs in all ADCs are synchronized by the next SYSREF rising edge

7.3.5.2 Decimation Filters

The decimation filters are arranged to provide a programmable overall decimation of 2, 4, 8, or 16. All filter outputs have a resolution of 15 bits. The decimate-by-2 filter has a real output and the decimate-by-4, decimate-by-8, and decimate-by-16 filters have complex outputs. 表 7-10 lists the effective output sample rates, available signal bandwidths, output formats, and stop-band attenuation for each decimation mode. The available bandwidths of the complex output modes are twice that of equivalent real decimation modes because of the nature of the I/Q data and complex signaling. This higher bandwidth results in the decimate-by-2 real and decimate-by-4 complex modes having approximately the same useful output bandwidth.

表 7-10. Output Sample Rates and Signal Bandwidths

DECIMATION SETTING	$f_{(DEVCLK)}$				OUTPUT FORMAT
	OUTPUT RATE (MSPS)	MAX ALIAS PROTECTED SIGNAL BANDWIDTH (MHz)	STOP-BAND ATTENUATION	PASS-BAND RIPPLE	
No decimation	$f_{(DEVCLK)}$	$f_{(DEVCLK)}$ / 2	—	< ±0.001 dB	Real signal, 12-bit data
Decimate-by-2	$f_{(DEVCLK)}$ / 2	0.4 × $f_{(DEVCLK)}$ / 2	> 89 dB	< ±0.001 dB	Real signal, 15-bit data
Decimate-by-4 (D4_AP87 = 0)	$f_{(DEVCLK)}$ / 4	0.8 × $f_{(DEVCLK)}$ / 4	> 90 dB	< ±0.001 dB	Complex signal, 15-bit data
Decimate-by-4 (D4_AP87 = 1)	$f_{(DEVCLK)}$ / 4	0.875 × $f_{(DEVCLK)}$ / 4	> 66 dB	< ±0.005 dB	Complex signal, 15-bit data
Decimate-by-8	$f_{(DEVCLK)}$ / 8	0.8 × $f_{(DEVCLK)}$ / 8	> 90 dB	< ±0.001 dB	Complex signal, 15-bit data
Decimate-by-16	$f_{(DEVCLK)}$ / 16	0.8 × $f_{(DEVCLK)}$ / 16	> 90 dB	< ±0.001 dB	Complex signal, 15-bit data

図 7-7 to 図 7-18 provide the composite decimation filter responses. The pass-band section (black trace) shows the alias-protected region of the response. The transition band (red trace) shows the transition region of the response, or the regions that alias into the transition region, which is not alias protected and therefore desired signals must not be within this band. The aliasing band (blue trace) shows the attenuation applied to the bands that alias back into the pass band after decimation and are sufficiently low to prevent undesired signals from showing up in the pass band. Use analog input filtering for additional attenuation of the aliasing band or to prevent harmonics, interleaving spurs, or other undesired spurious signals from folding into the desired signal band before the decimation filter.

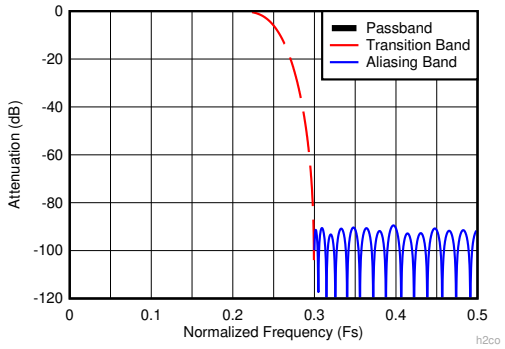

図 7-7. Decimate-by-2 Composite Response (D2_HIGH_PASS = 0)

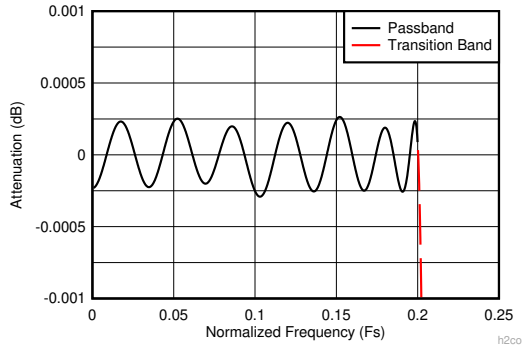

図 7-8. Decimate-by-2 Composite Zoomed Pass-Band Response (D2_HIGH_PASS = 0)

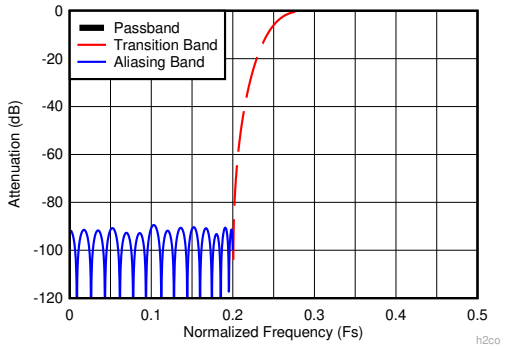

図 7-9. Decimate-by-2 Composite Response (D2_HIGH_PASS = 1)

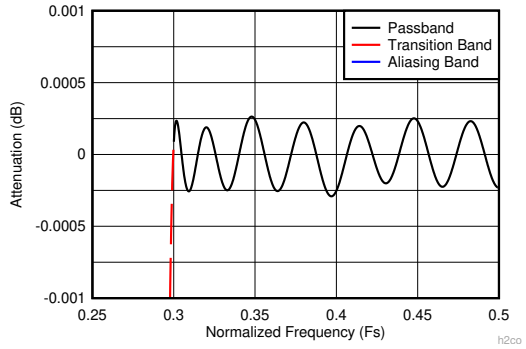

図 7-10. Decimate-by-2 Composite Zoomed Pass-Band Response (D2_HIGH_PASS = 1)

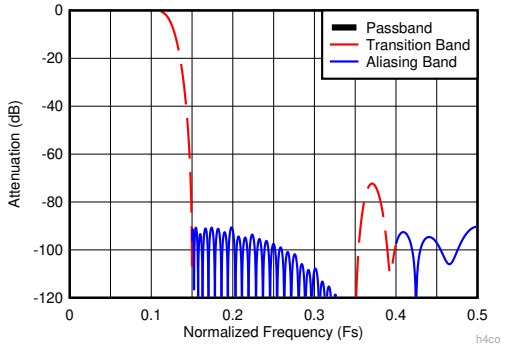

図 7-11. Decimate-by-4 Composite Response (D4_AP87 = 0)

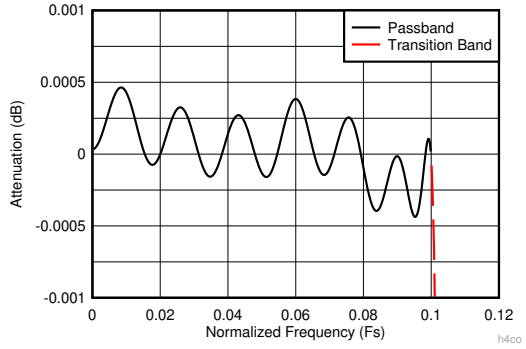

図 7-12. Decimate-by-4 Composite Zoomed Pass-Band Response (D4_AP87 = 0)

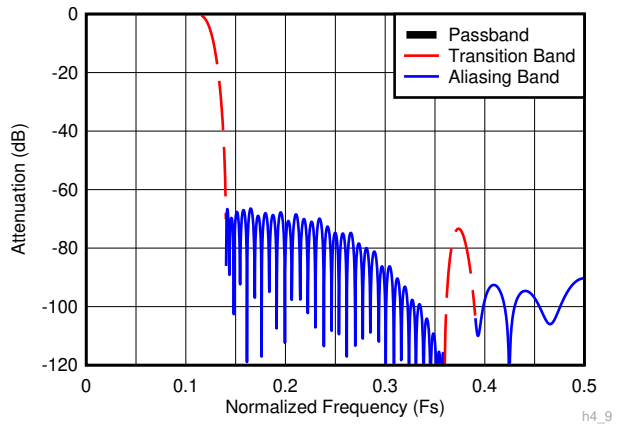

図 7-13. Decimate-by-4 Composite Response (D4_AP87 = 1)

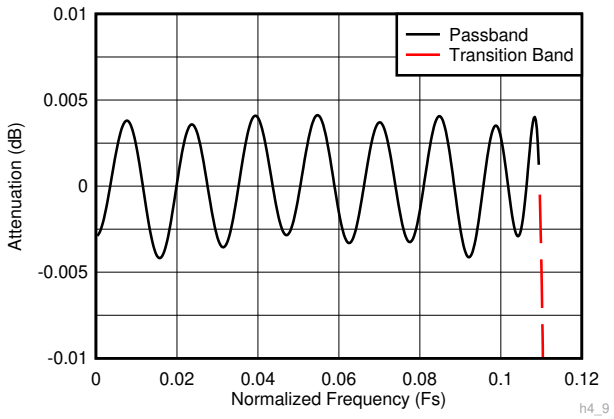

図 7-14. Decimate-by-4 Composite Zoomed Pass-Band Response (D4_AP87 = 1)

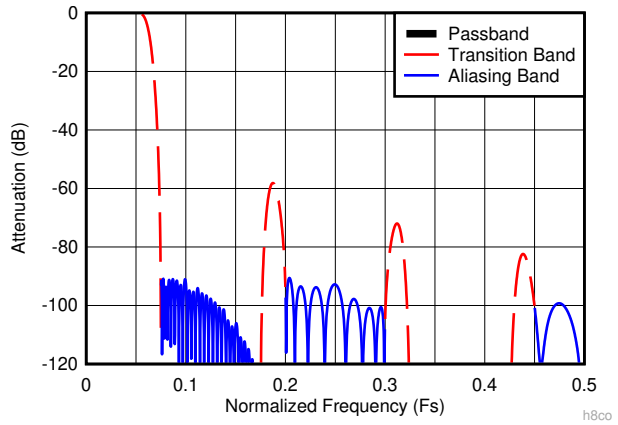

図 7-15. Decimate-by-8 Composite Response

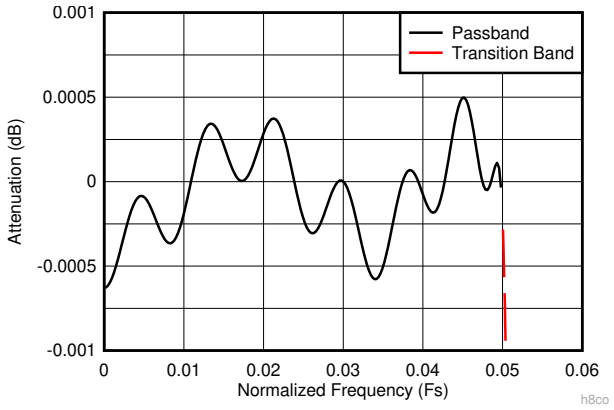

図 7-16. Decimate-by-8 Composite Zoomed Pass-Band Response

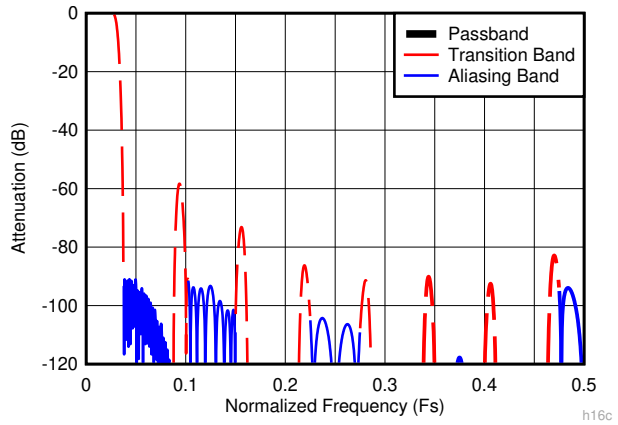

図 7-17. Decimate-by-16 Composite Response

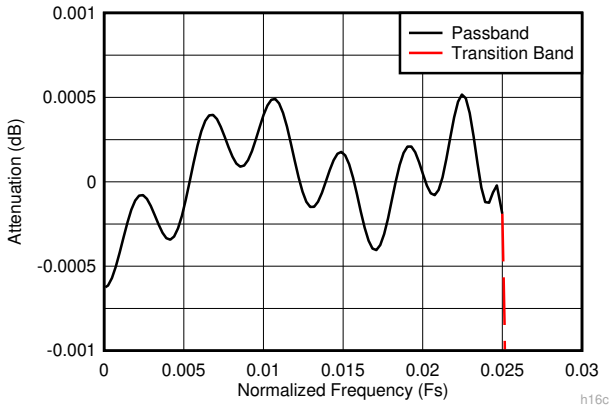

図 7-18. Decimate-by-16 Composite Zoomed Pass-Band Response

For maximum efficiency, a group of high-speed filter blocks are implemented with specific blocks used for each decimation setting to achieve the composite responses illustrated in 図 7-7 to 図 7-18. 表 7-11 describes the combination of filter blocks used for each decimation setting and 表 7-12 lists the coefficient details and decimation factor of each filter block. The coefficients are symmetric with the center tap indicated by bold text.

表 7-11. Decimation Mode Filter Usage

DECIMATION SETTING	FILTER BLOCKS USED
2	CS80
4 (D4_AP87 = 0)	CS45, CS80
4 (D4_AP87 = 1)	CS45, CS87
8	CS20, CS40, CS80
16	CS10, CS20, CS40, CS80

表 7-12. Filter Coefficient Details

FILTER COEFFICIENT SET (Decimation Factor of Filter)											
CS10 (2)		CS20 (2)		CS40 (2)		CS45 (2)		CS80 (2)		CS87 (2)	
–65	–65	109	109	–327	–327	56	56	–37	–37	–15	–15
0	0	0	0	0	0	0	0	0	0	0	0
577	577	–837	–837	2231	2231	–401	–401	118	118	23	23
1024		0	0	0	0	0	0	0	0	0	0
		4824	4824	–8881	–8881	1596	1596	–291	–291	–40	–40
		8192		0	0	0	0	0	0	0	0
				39742	39742	–4979	–4979	612	612	64	64
				65536		0	0	0	0	0	0
						20113	20113	–1159	–1159	–97	–97
						32768		0	0	0	0
								2031	2031	142	142
								0	0	0	0
								–3356	–3356	–201	–201
								0	0	0	0
								5308	5308	279	279
								0	0	0	0
								–8140	–8140	–380	–380
								0	0	0	0
								12284	12284	513	513
								0	0	0	0
								–18628	–18628	–690	–690
								0	0	0	0
								29455	29455	939	939
								0	0	0	0
								–53191	–53191	–1313	–1313
								0	0	0	0
								166059	166059	1956	1956
								262144		0	0
										–3398	–3398
										0	0
										10404	10404
										16384	

7.3.5.3 Output Data Format

The DDC output data varies depending on the selected JMODE. Real decimate-by-2 mode (JMODE 9) consists of 15-bit real output data. Complex decimation modes (JMODE 10 to 16), except for JMODE 12, consist of 15-bit complex data plus the two overrange threshold-detection control bits. JMODE 12 output data consists of 12-bit complex data, but does not include the two overrange threshold-detection control bits that must instead be monitored using the ORA0, ORA1 and ORB0, ORB1 output pins. 表 7-13 lists the data format for JMODE 9 and 表 7-14 lists the data format for all JMODEs except JMODE 12.

表 7-13. Real Decimation (JMODE 9) Output Sample Format

DDC CHANNEL	ODD, EVEN SAMPLE	16-BIT OUTPUT WORD															
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
A	Even	DDC A even-numbered sample, 15-bit output data															OVR_T0
A	Odd	DDC A odd-numbered sample, 15-bit output data															OVR_T1
B	Even	DDC B even-numbered sample, 15-bit output data															OVR_T0
B	Odd	DDC B odd-numbered sample, 15-bit output data															OVR_T1

表 7-14. Complex Decimation Output Sample Format (Except JMODE 12)

I/Q SAMPLE	16-BIT OUTPUT WORD															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
I	DDC in-phase (I) 15-bit output data															OVR_T0
Q	DDC quadrature (Q) 15-bit output data															OVR_T1

7.3.5.4 Decimation Settings

7.3.5.4.1 Decimation Factor

The decimation setting is adjustable over the following settings and is set by the JMODE parameter. See 表 7-18 for the available JMODE values and the corresponding decimation settings.

- DDC Bypass: No decimation, real output
- Decimate-by-2: Real output (JMODE 9)
- Decimate-by-4: Complex output (JMODE 10 to 12)
- Decimate-by-8: Complex output (JMODE 13 to 14)
- Decimate-by-16: Complex output (JMODE 15 to 16)

7.3.5.4.2 DDC Gain Boost

The DDC gain boost (see the DDC configuration register) provides additional gain through the DDC block. Setting BOOST to 1 sets the total decimation filter chain gain to 6.02 dB. With a setting of 0, the total decimation filter chain has a 0-dB gain. Only use this setting when the negative image of the input signal is filtered out by the decimation filters, otherwise clipping may occur. There is no reduction in analog performance when gain boost is enabled or disabled, but care must be taken to understand the reference output power for proper performance calculations.

7.3.6 JESD204B Interface

The ADC12DJ3200QML-SP uses the JESD204B high-speed serial interface for data converters to transfer data from the ADC to the receiving logic device. The ADC12DJ3200QML-SP serialized lanes are capable of operating up to 12.8 Gbps, slightly above the JESD204B maximum lane rate. A maximum of 16 lanes can be used to allow lower lane rates for interfacing with speed-limited logic devices. 図 7-19 shows a simplified block diagram of the JESD204B interface protocol.

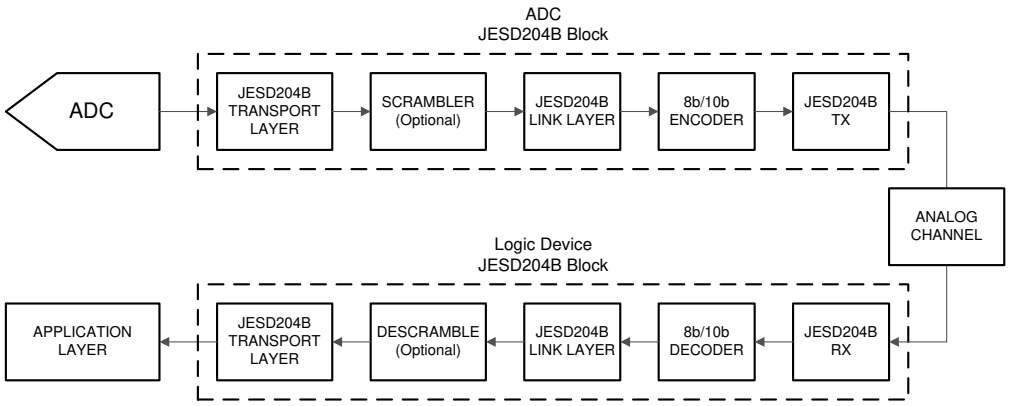

図 7-19. Simplified JESD204B Interface Diagram

The various signals used in the JESD204B interface and the associated ADC12DJ3200QML-SP pin names are summarized briefly in 表 7-15 for reference.

表 7-15. Summary of JESD204B Signals

SIGNAL NAME	ADC12DJ3200QML-SP PIN NAMES	DESCRIPTION
Data	DA0+...DA7+, DA0–...DA7–, DB0+...DB7+, DB0–...DB7–	High-speed serialized data after 8b, 10b encoding
$\overline{\text{SYNC}}$	$\overline{\text{SYNCSE}}$, TMSTP+, TMSTP–	Link initialization signal (handshake), toggles low to start code group synchronization (CGS) process
Device clock	CLK+, CLK–	ADC sampling clock, also used for clocking digital logic and output serializers
SYSREF	SYSREF+, SYSREF–	System timing reference used to deterministically reset the internal local multiframe counters in each JESD204B device

7.3.6.1 Transport Layer

The transport layer takes samples from the ADC output (in decimation bypass mode) or from the DDC output and maps the samples into octets, frames, multiframes, and lanes. Sample mapping is defined by the JESD204B mode that is used, defined by parameters such as L, M, F, S, N, N', CF, and so forth. There are a number of predefined transport layer modes in the ADC12DJ3200QML-SP that are defined in 表 7-18. The high level configuration parameters for the transport layer in the ADC12DJ3200QML-SP are described in 表 7-16. For simplicity, the transport layer mode is chosen by simply setting the JMODE parameter and the desired K value. For reference, the various configuration parameters for JESD204B are defined in 表 7-17.

7.3.6.2 Scrambler

An optional data scrambler can be used to scramble the octets before transmission across the channel. Scrambling is recommended in order to remove the possibility of spectral peaks in the transmitted data. The JESD204B receiver automatically synchronizes its descrambler to the incoming scrambled data stream. The initial lane alignment sequence (ILA) is never scrambled. Scrambling can be enabled by setting SCR (in the JESD204B Control register).

7.3.6.3 Link Layer

The link layer serves multiple purposes in JESD204B, including establishing the code boundaries (see the *Code Group Synchronization (CGS)* section), initializing the link (see the *Initial Lane Alignment Sequence (ILAS)* section), encoding the data (see the *8b, 10b Encoding* section), and monitoring the health of the link (see the *Frame and Multiframe Monitoring* section).

7.3.6.3.1 Code Group Synchronization (CGS)

The first step in initializing the JESD204B link, after SYSREF is processed, is to achieve code group synchronization. The receiver first asserts the SYNC signal when ready to initialize the link. The transmitter responds to the request by sending a stream of K28.5 characters. The receiver then aligns its character clock to the K28.5 character sequence. Code group synchronization is achieved after receiving four K28.5 characters successfully. The receiver deasserts SYNC on the next local multiframe clock (LMFC) edge after CGS is achieved and waits for the transmitter to start the initial lane alignment sequence.

7.3.6.3.2 Initial Lane Alignment Sequence (ILAS)

After the transmitter detects the SYNC signal deassert, the transmitter waits until its next LMFC edge to start sending the initial lane alignment sequence. The ILAS consists of four multiframes each containing a predetermined sequence. The receiver searches for the start of the ILAS to determine the frame and multiframe boundaries. As the ILAS reaches the receiver for each lane, the lane starts to buffer its data until all receivers have received the ILAS and subsequently release the ILAS from all lanes at the same time in order to align the lanes. The second multiframe of the ILAS contains configuration parameters for the JESD204B that can be used by the receiver to verify that the transmitter and receiver configurations match.

7.3.6.3.3 8b, 10b Encoding

The data link layer converts the 8-bit octets from the transport layer into 10-bit characters for transmission across the link using 8b, 10b encoding. 8b, 10b encoding provides DC balance for AC-coupling of the SerDes links and a sufficient number of edge transitions for the receiver to reliably recover the data clock. 8b, 10b also provides some amount of error detection where a single bit error in a character likely results in either not being able to find the 10-bit character in the 8b, 10b decoder lookup table or incorrect character disparity.

7.3.6.3.4 Frame and Multiframe Monitoring

The ADC12DJ3200QML-SP supports frame and multiframe monitoring for verifying the health of the JESD204B link. If the last octet of a frame matches the last octet of the previous frame, then the last octet in the second frame is replaced with an /F/ (/K28.7/) character. If the second frame is the last frame of a multiframe, then an /A/ (/K28.3/) character is used instead. When scrambling is enabled, if the last octet of a frame is 0xFC then the transmitter replaces the octet with an /F/ (/K28.7/) character. With scrambling, if the last octet of a multiframe is 0x7C then the transmitter replaces the octet with an /A/ (/K28.3/) character. When the receiver detects an /F/ or /A/ character, the receiver checks if the character occurs at the end of a frame or multiframe, and replaces that octet with the appropriate data character. The receiver can report an error if the alignment characters occur in the incorrect place and trigger a link realignment.

7.3.6.4 Physical Layer

The JESD204B physical layer consists of a current mode logic (CML) output driver and receiver. The receiver consists of a clock detection and recovery (CDR) unit to extract the data clock from the serialized data stream and can contain an equalizer to correct for the low-pass response of the physical transmission channel. Likewise, the transmitter can contain pre-equalization to account for frequency dependent losses across the channel. The total reach of the SerDes links depends on the data rate, board material, connectors, equalization, noise and jitter, and required bit-error performance. The SerDes lanes do not have to be matched in length because the receiver aligns the lanes during the initial lane alignment sequence.

7.3.6.4.1 SerDes Pre-Emphasis

The ADC12DJ3200QML-SP high-speed output drivers can pre-equalize the transmitted data stream by using pre-emphasis in order to compensate for the low-pass response of the transmission channel. Configurable pre-emphasis settings allow the output drive waveform to be optimized for different PCB materials and signal transmission distances. The pre-emphasis setting is adjusted through the serializer pre-emphasis setting

SER_PE (in the serializer pre-emphasis control register). Higher values increase the pre-emphasis to compensate for more lossy PCB materials. This adjustment is best used in conjunction with an eye-diagram analysis capability in the receiver. Adjust the pre-emphasis setting to optimize the eye-opening for the specific hardware configuration and line rates needed.

7.3.6.5 JESD204B Enable

The JESD204B interface must be disabled through JESD_EN (in the JESD204B enable register) while any of the other JESD204B parameters are being changed. When JESD_EN is set to 0 the block is held in reset and the serializers are powered down. The clocks for this section are also gated off to further save power. When the parameters are set as desired, the JESD204B block can be enabled (JESD_EN is set to 1).

7.3.6.6 Multi-Device Synchronization and Deterministic Latency

JESD204B subclass 1 outlines a method to achieve deterministic latency across the serial link. If two devices achieve the same deterministic latency then they can be considered synchronized. This latency must be achieved from system startup to startup to be deterministic. There are two key requirements to achieve deterministic latency. The first is proper capture of SYSREF for which the ADC12DJ3200QML-SP provides a number of features to simplify this requirement at giga-sample clock rates (see the *SYSREF Capture for Multi-Device Synchronization and Deterministic Latency* section for more information).

The second requirement is to choose a proper elastic buffer release point in the receiver. Because the ADC12DJ3200QML-SP is an ADC, the ADC12DJ3200QML-SP is the transmitter (TX) in the JESD204B link and the logic device is the receiver (RX). The elastic buffer is the key block for achieving deterministic latency, and does so by absorbing variations in the propagation delays of the serialized data as the data travels from the transmitter to the receiver. A proper release point is one that provides sufficient margin against delay variations. An incorrect release point results in a latency variation of one LMFC period. Choosing a proper release point requires knowing the average arrival time of data at the elastic buffer, referenced to an LMFC edge, and the total expected delay variation for all devices. With this information the region of invalid release points within the LMFC period can be defined, which stretches from the minimum to maximum delay for all lanes. Essentially, the designer must make certain that the data for all lanes arrives at all devices before the release point occurs.

図 7-20 illustrates a timing diagram that demonstrates this requirement. In this figure, the data for two ADCs is shown. The second ADC has a longer routing distance (t_{PCB}) and results in a longer link delay. First, the invalid region of the LMFC period is marked off as determined by the data arrival times for all devices. Then, the release point is set by using the release buffer delay (RBD) parameter to shift the release point an appropriate number of frame clocks from the LMFC edge so that the release point occurs within the valid region of the LMFC cycle. In the case of 図 7-20, the LMFC edge (RBD = 0) is a good choice for the release point because there is sufficient margin on each side of the valid region.

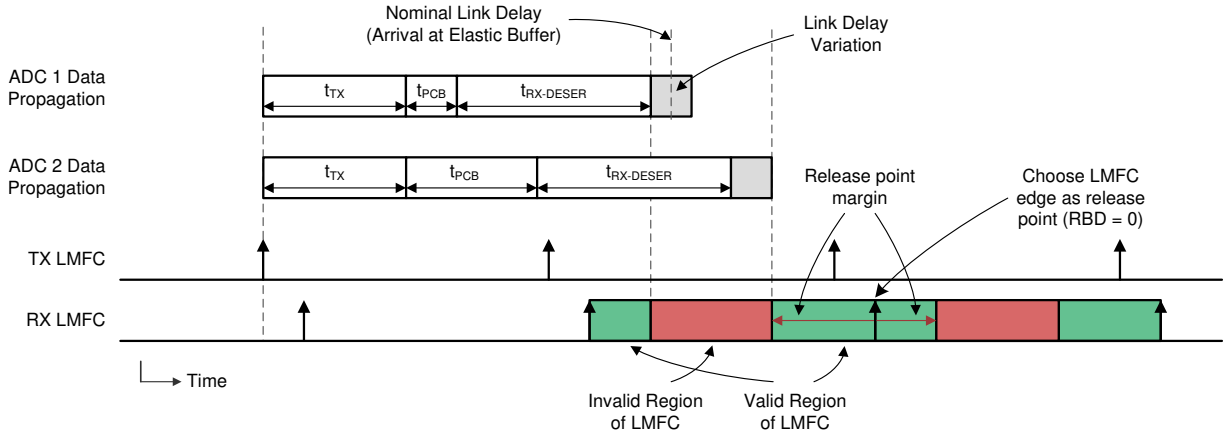

図 7-20. LMFC Valid Region Definition for Elastic Buffer Release Point Selection

The TX and RX LMFCs do not necessarily need to be phase aligned, but knowledge of their phase is important for proper elastic buffer release point selection. Also, the elastic buffer release point occurs within every LMFC

cycle, but the buffers only release when all lanes have arrived. Therefore, the total link delay can exceed a single LMFC period; see the *JESD204B multi-device synchronization: Breaking down the requirements techincal brief* for more information.

7.3.6.7 Operation in Subclass 0 Systems

The ADC12DJ3200QML-SP can operate with subclass 0 compatibility provided that multi-ADC synchronization and deterministic latency are not required. With these limitations, the device can operate without the application of SYSREF. The internal local multiframe clock is automatically self-generated with unknown timing. SYNC is used as normal to initiate the CGS and ILA.

7.3.7 Alarm Monitoring

A number of built-in alarms are available to monitor internal events. Several types of alarms and upsets are detected by this feature:

1. Serializer PLL is not locked
2. JESD204B link is not transmitting data (not in the data transmission state)
3. SYSREF causes internal clocks to be realigned
4. An upset that impacts the internal clocks

When an alarm occurs, a bit for each specific alarm is set in ALM_STATUS. Each alarm bit remains set until the host system writes a 1 to clear the alarm. If the alarm type is not masked (see the alarm mask register), then the alarm is also indicated by the ALARM register. The CALSTAT output pin can be configured as an alarm output that goes high when an alarm occurs; see the CAL_STATUS_SEL bit in the calibration pin configuration register.

7.3.7.1 NCO Upset Detection

The NCO_ALM register bit indicates if the NCO in channel A or B has been upset. The NCO phase accumulators in channel A are continuously compared to channel B. If the accumulators differ for even one clock cycle, the NCO_ALM register bit is set and remains set until cleared by the host system by writing a 1. This feature requires the phase and frequency words for each NCO accumulator in DDC A (PHASEAx, FREQAx) to be set to the same values as the NCO accumulators in DDC B (PHASEBx, FREQBx). For example, PHASEA0 must be the same as PHASEB0 and FREQA0 must be the same as FREQB0, however, PHASEA1 can be set to a different value than PHASEA0. This requirement ultimately reduces the number of NCO frequencies available for phase coherent frequency hopping from four to two for each DDC. DDC B can use a different NCO frequency than DDC A by setting the NCOB[1:0] pins to a different value than NCOA[1:0]. This detection is only valid after the NCOs are synchronized by either SYSREF or the start of the ILA sequence (as determined by the NCO synchronization register). For the NCO upset detection to work properly, follow these steps:

1. Program JESD_EN = 0
2. Make sure the device is configured to use both channels (PD_ACH = 0, PD_BCH = 0)
3. Select a JMODE that uses the NCO
4. Program all NCO frequencies and phases to be the same for channel A and B (for example, FREQA0 = FREQB0, FREQA1 = FREQB1, FREQA2 = FREQB2, and FREQA3 = FREQB3)
5. If desired, use the CMODE and CSEL registers or the NCOA[1:0] and NCOB[1:0] pins to choose a unique frequency for channel A and channel B
6. Program JESD_EN = 1
7. Synchronize the NCOs (using the ILA or using SYSREF); see NCO Phase Synchronization
8. Write a 1 to the NCO_ALM register bit to clear it
9. Monitor the NCO_ALM status bit or the CALSTAT output pin if CAL_STATUS_SEL is properly configured
10. If the frequency or phase registers are changed while the NCO is enabled, the NCOs can get out of synchronization
11. Repeat steps 7-9
12. If the device enters and exits global power down, repeat steps 7-9

7.3.7.2 Clock Upset Detection

The CLK_ALM register bit indicates if the internal clocks have been upset. The clocks in channel A are continuously compared to channel B. If the clocks differ for even one DEVCLK / 2 cycle, the CLK_ALM register bit is set and remains set until cleared by the host system by writing a 1. For the CLK_ALM register bit to function properly, follow these steps:

1. Program JESD_EN = 0
2. Make sure the part is configured to use both channels (PD_ACH = 0, PD_BCH = 0)
3. Program JESD_EN = 1
4. Write CLK_ALM = 1 to clear CLK_ALM
5. Monitor the CLK_ALM status bit or the CALSTAT output pin if CAL_STATUS_SEL is properly configured
6. When exiting global power-down (via MODE or the PD pin), the CLK_ALM status bit may be set and must be cleared by writing a 1 to CLK_ALM

7.3.8 Temperature Monitoring Diode

A built-in thermal monitoring diode is made available on the TDIODE+ and TDIODE– pins. This diode facilitates temperature monitoring and characterization of the device in higher ambient temperature environments. Although the on-chip diode is not highly characterized, the diode can be used effectively by performing a baseline measurement (offset) at a known ambient or board temperature and creating a linear equation with the diode voltage slope provided in the *Electrical Characteristics: DC Specifications* table. Perform offset measurement with the device unpowered or with the PD pin asserted to minimize device self-heating. Only assert the PD pin long enough to take the offset measurement. Recommended monitoring devices include the LM95233 device and similar remote-diode temperature monitoring products from Texas Instruments.

7.3.9 Analog Reference Voltage

The reference voltage for the ADC12DJ3200QML-SP is derived from an internal band-gap reference. A buffered version of the reference voltage is available at the BG pin for user convenience. This output has an output-current capability of ±100 µA. The BG output must be buffered if more current is required. No provision exists for the use of an external reference voltage, but the full-scale input voltage can be adjusted through the full-scale-range register settings. In unique cases, the VA11 supply voltage can act as the reference voltage by setting BG_BYPASS (see the internal reference bypass register).

7.4 Device Functional Modes

The ADC12DJ3200QML-SP can be configured to operate in a number of functional modes. These modes are described in this section.

7.4.1 Dual-Channel Mode

The ADC12DJ3200QML-SP can be used as a dual-channel ADC where the sampling rate is equal to the clock frequency ($f_S = f_{CLK}$) provided at the CLK+ and CLK– pins. The two inputs, AIN± and BIN±, serve as the respective inputs for each channel in this mode. This mode is chosen simply by setting JMODE to the appropriate setting for the desired configuration as described in 表 7-18. The analog inputs can be swapped by setting DUAL_INPUT (see the input mux control register)

7.4.2 Single-Channel Mode (DES Mode)

The ADC12DJ3200QML-SP can also be used as a single-channel ADC where the sampling rate is equal to two times the clock frequency ($f_S = 2 \times f_{CLK}$) provided at the CLK+ and CLK– pins. This mode effectively interleaves the two ADC channels together to form a single-channel ADC at twice the sampling rate. This mode is chosen simply by setting JMODE to the appropriate setting for the desired configuration as described in 表 7-18. Either analog input, INA± or INB±, can serve as the input to the ADC, however INA± is recommended for best performance. The analog input can be selected using SINGLE_INPUT (see the input mux control register). The digital down-converters cannot be used in single-channel mode.

注

For optimized performance in single-channel mode, use INA± as the input to the ADC.

7.4.3 JESD204B Modes

The ADC12DJ3200QML-SP can be programmed as a single-channel or dual-channel ADC, with or without decimation, and a number JESD204B output formats. 表 7-16 summarizes the basic operating mode configuration parameters and whether they are user configured or derived.

注意

Powering down high-speed data outputs (DA0± ... DA7±, DB0± ... DB7±) for extended times can damage the output serializers, especially at high data rates. For information regarding reliable serializer operation, see the *Power-Down Modes* section.

表 7-16. ADC12DJ3200QML-SP Operating Mode Configuration Parameters

PARAMETER	DESCRIPTION	USER CONFIGURED OR DERIVED	VALUE
JMODE	JESD204B operating mode, automatically derives the rest of the JESD204B parameters, single-channel or dual-channel mode and the decimation factor	User configured	Set by JMODE (see the JESD204B mode register)
D	Decimation factor	Derived	See 表 7-18
DES	1 = single-channel mode, 0 = dual-channel mode	Derived	See 表 7-18
R	Number of bits transmitted per lane per DEVCLK cycle. The JESD204B line rate is the DEVCLK frequency times R. This parameter sets the SerDes PLL multiplication factor or controls bypassing of the SerDes PLL.	Derived	See 表 7-18
Links	Number of JESD204B links used	Derived	See 表 7-18
K	Number of frames per multiframe	User configured	Set by KM1 (see the JESD204B K parameter register), see the allowed values in 表 7-18

There are a number of parameters required to define the JESD204B format, all of which are sent across the link during the initial lane alignment sequence. In the ADC12DJ3200QML-SP, most parameters are automatically derived based on the selected JMODE; however, a few are configured by the user. 表 7-17 describes these parameters.

表 7-17. JESD204B Initial Lane Alignment Sequence Parameters

PARAMETER	DESCRIPTION	USER CONFIGURED OR DERIVED	VALUE
ADJCNT	LMFC adjustment amount (not applicable)	Derived	Always 0
ADJDIR	LMFC adjustment direction (not applicable)	Derived	Always 0
BID	Bank ID	Derived	Always 0
CF	Number of control words per frame	Derived	Always 0
CS	Control bits per sample	Derived	Always set to 0 in ILAS, see 表 7-18 for actual usage
DID	Device identifier, used to identify the link	User configured	Set by DID (see the JESD204B DID parameter register), see 表 7-19
F	Number of octets (bytes) per frame (per lane)	Derived	See 表 7-18
HD	High-density format (samples split between lanes)	Derived	Always 0
JESDV	JESD204 standard revision	Derived	Always 1
K	Number of frames per multiframe	User configured	Set by the KM1 register, see the JESD204B K parameter register
L	Number of serial output lanes per link	Derived	See 表 7-18
LID	Lane identifier for each lane	Derived	See 表 7-19
M	Number of converters used to determine lane bit packing; may not match number of ADC channels in the device	Derived	See 表 7-18
N	Sample resolution (before adding control and tail bits)	Derived	See 表 7-18
N'	Bits per sample after adding control and tail bits	Derived	See 表 7-18
S	Number of samples per converter (M) per frame	Derived	See 表 7-18
SCR	Scrambler enabled	User configured	Set by the JESD204B control register
SUBCLASSV	Device subclass version	Derived	Always 1
RES1	Reserved field 1	Derived	Always 0
RES2	Reserved field 2	Derived	Always 0
CHKSUM	Checksum for ILAS checking (sum of all above parameters modulo 256)	Derived	Computed based on parameters in this table

Configuring the ADC12DJ3200QML-SP is made easy by using a single configuration parameter called JMODE (see the JESD204B mode register). Using 表 7-18, the correct JMODE value can be found for the desired operating mode. The modes listed in 表 7-18 are the only available operating modes. This table also gives a range and allowable step size for the K parameter (set by KM1, see the JESD204B K parameter register), which sets the multiframe length in number of frames.

表 7-18. ADC12DJ3200QML-SP Operating Modes

ADC12DJ3200QML-SP OPERATING MODE	USER-SPECIFIED PARAMETER		DERIVED PARAMETERS											INPUT CLOCK RANGE (MHz)
	JMODE	K [Min:Step:Max]	D	DES	Links	N	CS	N'	L (Per Link)	M (Per Link)	F	S	R (Fbit / Fclk)	
12-bit, single-channel, 8 lanes	0	3:1:32	1	1	2	12	0	12	4	4(1)	8	5	4	800-3200
12-bit, single-channel, 16 lanes	1	3:1:32	1	1	2	12	0	12	8	8(1)	8	5	2	800-3200

表 7-18. ADC12DJ3200QML-SP Operating Modes (continued)

ADC12DJ3200QML-SP OPERATING MODE	USER-SPECIFIED PARAMETER		DERIVED PARAMETERS											INPUT CLOCK RANGE (MHz)
	JMODE	K [Min:Step:Max]	D	DES	Links	N	CS	N'	L (Per Link)	M (Per Link)	F	S	R (Fbit / Fclk)	
12-bit, dual-channel, 8 lanes	2	3:1:32	1	0	2	12	0	12	4	4(1)	8	5	4	800-3200
12-bit, dual-channel, 16 lanes	3	3:1:32	1	0	2	12	0	12	8	8(1)	8	5	2	800-3200
8-bit, single-channel, 4 lanes	4	18:2:32	1	1	2	8	0	8	2	1	1	2	5	800-2560
8-bit, single-channel, 8 lanes	5	18:2:32	1	1	2	8	0	8	4	1	1	4	2.5	800-3200
8-bit, dual-channel, 4 lanes	6	18:2:32	1	0	2	8	0	8	2	1	1	2	5	800-2560
8-bit, dual-channel, 8 lanes	7	18:2:32	1	0	2	8	0	8	4	1	1	4	2.5	800-3200
Reserved	8	—	—	—	—	—	—	—	—	—	—	—	—	—
15-bit, real data, decimate-by-2, 8 lanes	9	9:1:32	2	0	2	15	1(2)	16	4	1	2	4	2.5	800-3200
15-bit, decimate-by-4, 4 lanes	10	9:1:32	4	0	2	15	1(2)	16	2	2	2	1	5	800-2560
15-bit, decimate-by-4, 8 lanes	11	9:1:32	4	0	2	15	1(2)	16	4	2	2	2	2.5	800-3200
12-bit, decimate-by-4, 16 lanes	12	3:1:32	4	0	2	12	0	12	8	8(1)	8	5	1	1000-3200
15-bit, decimate-by-8, 2 lanes	13	5:1:32	8	0	2	15	1(2)	16	1	2	4	1	5	800-2560
15-bit, decimate-by-8, 4 lanes	14	9:1:32	8	0	2	15	1(2)	16	2	2	2	1	2.5	800-3200
15-bit, decimate-by-16, 1 lane	15	3:1:32	16	0	1	15	1(2)	16	1	4	8	1	5	800-2560
15-bit, decimate-by-16, 2 lanes	16	5:1:32	16	0	2	15	1(2)	16	1	2	4	1	2.5	800-3200
8-bit, single-channel, 16 lanes	17	18:2:32	1	1	2	8	0	8	8	1	1	8	1.25	800-3200
8-bit, dual-channel, 16 lanes	18	18:2:32	1	0	2	8	0	8	8	1	1	8	1.25	800-3200

(1) M equals L in these modes to allow the samples to be sent in time-order over L lanes. The M parameter does not represent the actual number of converters. Interleave the M sample streams from each link in the receiver to produce the correct sample data; see 表 7-20 to 表 7-37 for more details.

(2) $\overline{CS}$ is always reported as 0 in the initial lane alignment sequence (ILAS) for the ADC12DJ3200QML-SP.

The ADC12DJ3200QML-SP has a total of 16 high-speed output drivers that are grouped into two 8-lane JESD204B links. Most operating modes use two links with up to eight lanes per link. The lanes and their derived configuration parameters are described in 表 7-19. For a specified JMODE, the lowest indexed lanes for each link are used and the higher indexed lanes for each link are automatically powered down. Always route the lowest indexed lanes to the logic device.

表 7-19. ADC12DJ3200QML-SP Lane Assignment and Parameters

DEVICE PIN DESIGNATION	LINK	DID (User Configured)	LID (Derived)
DA0±	A	Set by DID (see theJESD204B DID parameter register), the effective DID is equal to the DID register setting (DID)	0
DA1±			1
DA2±			2
DA3±			3
DA4±			4
DA5±			5
DA6±			6
DA7±			7
DB0±	B	Set by DID (see theJESD204B DID parameter register), the effective DID is equal to the DID register setting plus 1 (DID+1)	0
DB1±			1
DB2±			2
DB3±			3
DB4±			4
DB5±			5
DB6±			6
DB7±			7

7.4.3.1 JESD204B Output Data Formats

Output data are formatted in a specific optimized fashion for each JMODE setting. When the DDC is not used (decimation = 1) the 12-bit offset binary values are mapped into octets. For the DDC mode, the 16-bit values (15-bit complex data plus 1 overrange bit) are mapped into octets. The following tables show the specific mapping formats for a single frame. In all mappings the tail bits (T) are 0 (zero). In 表 7-20 to 表 7-37, the single-channel format samples are defined as Sn, where n is the sample number within the frame. In the dual-channel real output formats (DDC bypass and decimate-by-2), the samples are defined as An and Bn, where An are samples from channel A and Bn are samples from channel B. In the complex output formats (decimate-by-4, decimate-by-8, decimate-by-16), the samples are defined as AIn, AQn, BIn and BQn, where AIn and AQn are the in-phase and quadrature-phase samples of channel A and BIn and BQn are the in-phase and quadrature-phase samples of channel B. All samples are formatted as MSB first, LSB last.

表 7-20. JMODE 0 (12-bit, Decimate-by-1, Single-Channel, 8 Lanes)

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	S0		S8		S16		S24		S32							T
DA1	S2		S10		S18		S26		S34							T
DA2	S4		S12		S20		S28		S36							T
DA3	S6		S14		S22		S30		S38							T
DB0	S1		S9		S17		S25		S33							T
DB1	S3		S11		S19		S27		S35							T
DB2	S5		S13		S21		S29		S37							T
DB3	S7		S15		S23		S31		S39							T

表 7-21. JMODE 1 (12-Bit, Decimate-by-1, Single-Channel, 16 Lanes)

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	S0		S16		S32		S48		S64							T
DA1	S2		S18		S34		S50		S66							T
DA2	S4		S20		S36		S52		S68							T
DA3	S6		S22		S38		S54		S70							T
DA4	S8		S24		S40		S56		S72							T
DA5	S10		S26		S42		S58		S74							T
DA6	S12		S28		S44		S60		S76							T
DA7	S14		S30		S46		S62		S78							T
DB0	S1		S17		S33		S49		S65							T
DB1	S3		S19		S35		S51		S67							T
DB2	S5		S21		S37		S53		S69							T
DB3	S7		S23		S39		S55		S71							T
DB4	S9		S25		S41		S57		S73							T
DB5	S11		S27		S43		S59		S75							T
DB6	S13		S29		S45		S61		S77							T
DB7	S15		S31		S47		S63		S79							T

表 7-22. JMODE 2 (12-Bit, Decimate-by-1, Dual-Channel, 8 Lanes)

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	A0		A4		A8		A12		A16							T
DA1	A1		A5		A9		A13		A17							T
DA2	A2		A6		A10		A14		A18							T
DA3	A3		A7		A11		A15		A19							T
DB0	B0		B4		B8		B12		B16							T
DB1	B1		B5		B9		B13		B17							T
DB2	B2		B6		B10		B14		B18							T
DB3	B3		B7		B11		B15		B19							T

表 7-23. JMODE 3 (12-Bit, Decimate-by-1, Dual-Channel, 16 Lanes)

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	A0		A8		A16		A24		A32		T					
DA1	A1		A9		A17		A25		A33		T					
DA2	A2		A10		A18		A26		A34		T					
DA3	A3		A11		A19		A27		A35		T					
DA4	A4		A12		A20		A28		A36		T					
DA5	A5		A13		A21		A29		A37		T					
DA6	A6		A14		A22		A30		A38		T					
DA7	A7		A15		A23		A31		A39		T					
DB0	B0		B8		B16		B24		B32		T					
DB1	B1		B9		B17		B25		B33		T					
DB2	B2		B10		B18		B26		B34		T					
DB3	B3		B11		B19		B27		B35		T					
DB4	B4		B12		B20		B28		B36		T					
DB5	B5		B13		B21		B29		B37		T					
DB6	B6		B14		B22		B30		B38		T					
DB7	B7		B15		B23		B31		B39		T					

表 7-24. JMODE 4 (8-Bit, Decimate-by-1, Single-Channel, 4 Lanes)

OCTET	0	
NIBBLE	0	1
DA0	S0	
DA1	S2	
DB0	S1	
DB1	S3	

表 7-25. JMODE 5 (8-Bit, Decimate-by-1, Single-Channel, 8 Lanes)

OCTET	0	
NIBBLE	0	1
DA0	S0	
DA1	S2	
DA2	S4	
DA3	S6	
DB0	S1	
DB1	S3	
DB2	S5	
DB3	S7	

表 7-26. JMODE 6 (8-Bit, Decimate-by-1, Dual-Channel, 4 Lanes)

OCTET	0	
NIBBLE	0	1
DA0	A0	
DA1	A1	
DB0	B0	
DB1	B1	

表 7-27. JMODE 7 (8-Bit, Decimate-by-1, Dual-Channel, 8 Lanes)

OCTET	0	
NIBBLE	0	1
DA0	A0	
DA1	A1	
DA2	A2	
DA3	A3	
DB0	B0	
DB1	B1	
DB2	B2	
DB3	B3	

表 7-28. JMODE 9 (15-Bit, Decimate-by-2, Dual-Channel, 8 Lanes)

OCTET	0		1	
NIBBLE	0	1	2	3
DA0	A0			
DA1	A1			
DA2	A2			
DA3	A3			
DB0	B0			
DB1	B1			
DB2	B2			
DB3	B3			

表 7-29. JMODE 10 (15-Bit, Decimate-by-4, Dual-Channel, 4 Lanes)

OCTET	0		1	
NIBBLE	0	1	2	3
DA0	AI0			
DA1	AQ0			
DB0	BI0			
DB1	BQ0			

表 7-30. JMODE 11 (15-Bit, Decimate-by-4, Dual-Channel, 8 Lanes)

OCTET	0		1	
NIBBLE	0	1	2	3
DA0	AI0			
DA1	AI1			
DA2	AQ0			
DA3	AQ1			
DB0	BI0			
DB1	BI1			
DB2	BQ0			
DB3	BQ1			

表 7-31. JMODE 12 (12-Bit, Decimate-by-4, Dual-Channel, 16 Lanes)

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	AI0		AI4		AI8		AI12		AI16							T
DA1	AQ0		AQ4		AQ8		AQ12		AQ16							T
DA2	AI1		AI5		AI9		AI13		AI17							T
DA3	AQ1		AQ5		AQ9		AQ13		AQ17							T
DA4	AI2		AI6		AI10		AI14		AI18							T
DA5	AQ2		AQ6		AQ10		AQ14		AQ218							T
DA6	AI3		AI7		AI11		AI15		AI19							T
DA7	AQ3		AQ7		AQ11		AQ15		AQ19							T
DB0	BI0		BI4		BI8		BI12		BI16							T
DB1	BQ0		BQ4		BQ8		BQ12		BQ16							T
DB2	BI1		BI5		BI9		BI13		BI17							T
DB3	BQ1		BQ5		BQ9		BQ13		BQ17							T
DB4	BI2		BI6		BI10		BI14		BI18							T
DB5	BQ2		BQ6		BQ10		BQ14		BQ218							T
DB6	BI3		BI7		BI11		BI15		BI19							T
DB7	BQ3		BQ7		BQ11		BQ15		BQ19							T

表 7-32. JMODE 13 (15-Bit, Decimate-by-8, Dual-Channel, 2 Lanes)

OCTET	0		1		2		3	
NIBBLE	0	1	2	3	4	5	6	7
DA0	AI0				AQ0			
DB0	BI0				BQ0			

表 7-33. JMODE 14 (15-Bit, Decimate-by-8, Dual-Channel, 4 Lanes)

OCTET	0		1	
NIBBLE	0	1	2	3
DA0	AI0			
DA1	AQ0			
DB0	BI0			
DB1	BQ0			

表 7-34. JMODE 15 (15-Bit, Decimate-by-16, Dual-Channel, 1 Lane)

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	AI0				AQ0				BI0				BQ0			

表 7-35. JMODE 16 (15-Bit, Decimate-by-16, Dual-Channel, 2 Lanes)

OCTET	0		1		2		3	
NIBBLE	0	1	2	3	4	5	6	7
DA0	AI0				AQ0			
DB0	BI0				BQ0			

表 7-36. JMODE 17 (8-bit, Decimate-by-1, Single-Channel, 16 lanes)

OCTET	0	
NIBBLE	0	1
DA0	S0	
DA1	S2	
DA2	S4	
DA3	S6	
DA4	S8	
DA5	S10	
DA6	S12	
DA7	S14	
DB0	S1	
DB1	S3	
DB2	S5	
DB3	S7	
DB4	S9	
DB5	S11	
DB6	S13	
DB7	S15	

表 7-37. JMODE 18 (8-Bit, Decimate-by-1, Dual-Channel, 16 Lanes)

OCTET	0	
NIBBLE	0	1
DA0	A0	
DA1	A1	
DA2	A2	
DA3	A3	
DA4	A4	
DA5	A5	
DA6	A6	
DA7	A7	
DB0	B0	
DB1	B1	
DB2	B2	
DB3	B3	
DB4	B4	
DB5	B5	
DB6	B6	
DB7	B7	

7.4.3.2 Dual DDC and Redundant Data Mode

When operating in dual-channel mode, the data from one channel can be routed to both digital down-converter blocks by using DIG_BIND_A or DIG_BIND_B (see the digital channel binding register). This feature enables down-conversion of two separate captured bands from a single ADC channel. The second ADC can be powered down in this mode by setting PD_ACH or PD_BCH (see the device configuration register).

Additionally, DIG_BIND_A or DIG_BIND_B can be used to provide redundant data to separate digital processors by routing data from one ADC channel to both JESD204B links. Redundant data mode is available for all JMODE modes except for the single-channel modes. Both dual DDC mode and redundant data mode are demonstrated in 図 7-21 where the data for ADC channel A is routed to both DDCs and then transmitted to a single processor or two processors (for redundancy).

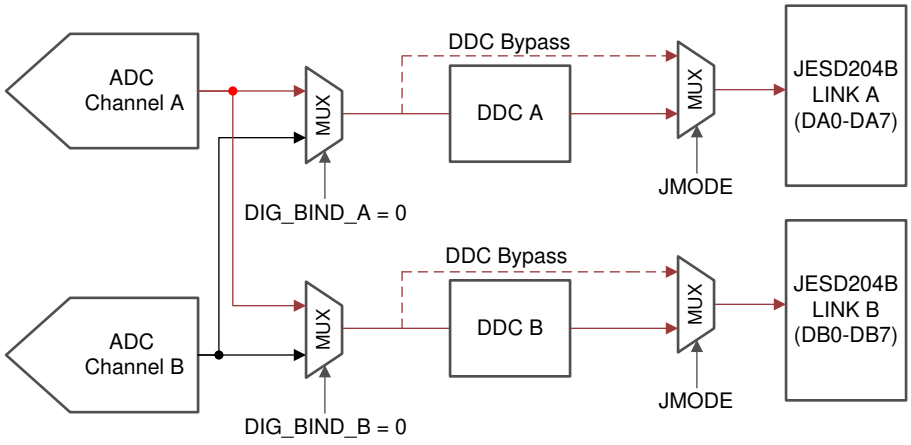

図 7-21. Dual DDC Mode or Redundant Data Mode for Channel A

7.4.4 Power-Down Modes

The PD input pin allows the ADC12DJ3200QML-SP devices to be entirely powered down. Power-down can also be controlled by MODE (see the Device Configuration register). The serial data output drivers are disabled when PD is high. When the device returns to normal operation, the JESD204 link must be re-established, and the ADC pipeline and decimation filters contain meaningless information so the system must wait a sufficient time for the data to be flushed. If power-down for power savings is desired, the system must power down the supply voltages regulators for VA19, VA11, and VD11 rather than make use of the PD input or MODE settings.

注意

Powering down the high-speed data outputs (DA0± ... DA7±, DB0± ... DB7±) for extended times may damage the output serializers, especially at high data rates. Powering down the serializers occurs when the PD pin is held high, the MODE register is programmed to a value other than 0x00 or 0x01, the PD_ACH or PD_BCH registers settings are programmed to 1, or when the JMODE register setting is programmed to a mode that uses less than the 16 total lanes that the device allows. For instance, JMODE 0 uses eight total lanes and therefore the four highest-indexed lanes for each JESD204B link (DA4± ... DA7±, DB4± ... DB7±) are powered down in this mode. When the PD pin is held high or the MODE register is programmed to a value other than 0x00 or 0x01, all output serializers are powered down. When the PD_ACH or PD_BCH register settings are programmed to 1, the associated ADC channel and lanes are powered down. To prevent unreliable operation, the PD pin and MODE register must only be used for brief periods of time to measure temperature diode offsets and not used for long-term power savings. Furthermore, using a JMODE that uses fewer than 16 lanes results in unreliable operation of the unused lanes. If the system will never use the unused lanes during the lifetime of the device, then the unused lanes do not cause issues and can be powered down. If the system may make use of the unused lanes at a later time, the reliable operation of the serializer outputs can be maintained by enabling JEXTRA_A and JEXTRA_B, which results in the VD11 power consumption to increase and the output serializers to toggle.

7.4.5 Test Modes

A number of device test modes are available. These modes insert known patterns of information into the device data path for assistance with system debug, development, or characterization.

7.4.5.1 Serializer Test-Mode Details

Test modes are enabled by setting JTEST (see the JESD204B test pattern control register) to the desired test mode. Each test mode is described in detail in the following sections. Regardless of the test mode, the serializer outputs are powered up based on JMODE. Only enable the test modes when the JESD204B link is disabled. 図 7-22 provides a diagram showing the various test mode insertion points.

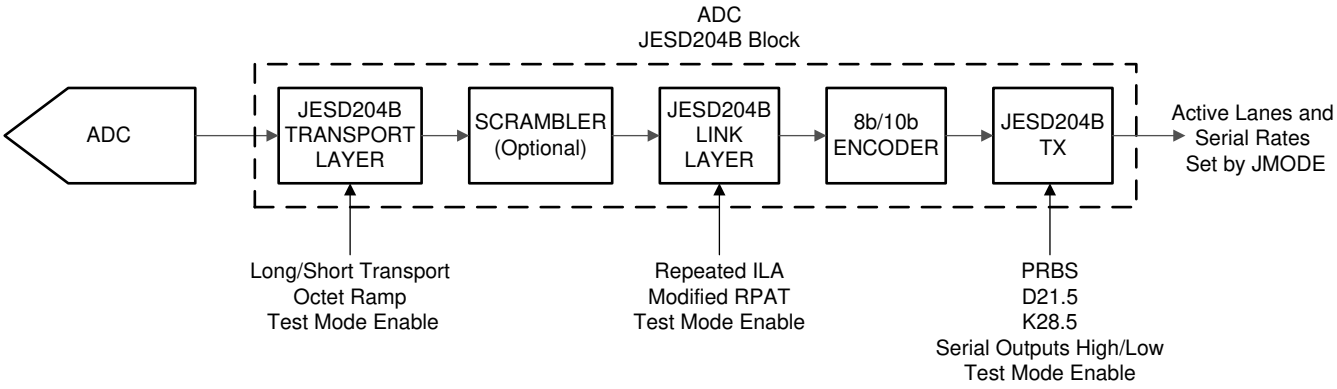

図 7-22. Test Mode Insertion Points

7.4.5.2 PRBS Test Modes

The PRBS test modes bypass the 8b, 10b encoder. These test modes produce pseudo-random bit streams that comply with the ITU-T O.150 specification. These bit streams are used with lab test equipment that can self-synchronize to the bit pattern and, therefore, the initial phase of the pattern is not defined.

The sequences are defined by a recursive equation. For example, 式 10 defines the PRBS7 sequence.

$$y[n] = y[n - 6] \oplus y[n - 7] \quad (10)$$

where

- bit n is the XOR of bit [n – 6] and bit [n – 7], which are previously transmitted bits

表 7-38 lists equations and sequence lengths for the available PRBS test modes. The initial phase of the pattern is unique for each lane.

表 7-38. PBRS Mode Equations

PRBS TEST MODE	SEQUENCE	SEQUENCE LENGTH (bits)
PRBS7	y[n] = y[n – 6]⊕y[n – 7]	127
PRBS15	y[n] = y[n – 14]⊕y[n – 15]	32767
PRBS23	y[n] = y[n – 18]⊕y[n – 23]	8388607

7.4.5.3 Ramp Test Mode

In the ramp test mode, the JESD204B link layer operates normally, but the transport layer is disabled and the input from the formatter is ignored. After the ILA sequence, each lane transmits an identical octet stream that increments from 0x00 to 0xFF and repeats.

7.4.5.4 Short and Long Transport Test Mode

JESD204B defines both short and long transport test modes to verify that the transport layers in the transmitter and receiver are operating correctly. The ADC12DJ3200QML-SP has three different transport layer test patterns depending on the N' value of the specified JMODE (see 表 7-18).

7.4.5.4.1 Short Transport Test Pattern

Short transport test patterns send a predefined octet format that repeats every frame. In the ADC12DJ3200QML-SP, all JMODE configurations that have an N' value of 8 or 12 use the short transport test pattern. 表 7-39 and 表 7-40 define the short transport test patterns for N' values of 8 and 12. All applicable lanes are shown, however only the enabled lanes (lowest indexed) for the configured JMODE are used.

表 7-39. Short Transport Test Pattern for N' = 8 Modes (Length = 2 Frames)

FRAME	0	1
DA0	0x00	0xFF
DA1	0x01	0xFE
DA2	0x02	0xFD
DA3	0x03	0xFC
DB0	0x00	0xFF
DB1	0x01	0xFE
DB2	0x02	0xFD
DB3	0x03	0xFC

表 7-40. Short Transport Test Pattern for N' = 12 Modes (Length = 1 Frame)

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DA0	0xF01		0xF02		0xF03		0xF04		0xF05							T
DA1	0xE11		0xE12		0xE13		0xE14		0xE15							T
DA2	0xD21		0xD22		0xD23		0xD24		0xD25							T
DA3	0xC31		0xC32		0xC33		0xC34		0xC35							T
DA4	0xB41		0xB42		0xB43		0xB44		0xB45							T
DA5	0xA51		0xA52		0xA53		0xA54		0xA55							T
DA6	0x961		0x962		0x963		0x964		0x965							T
DA7	0x871		0x872		0x873		0x874		0x875							T
DB0	0xF01		0xF02		0xF03		0xF04		0xF05							T
DB1	0xE11		0xE12		0xE13		0xE14		0xE15							T
DB2	0xD21		0xD22		0xD23		0xD24		0xD25							T
DB3	0xC31		0xC32		0xC33		0xC34		0xC35							T
DB4	0xB41		0xB42		0xB43		0xB44		0xB45							T
DB5	0xA51		0xA52		0xA53		0xA54		0xA55							T
DB6	0x961		0x962		0x963		0x964		0x965							T
DB7	0x871		0x872		0x873		0x874		0x875							T

7.4.5.4.2 Long Transport Test Pattern

The long-transport test mode is used in all of the JMODE modes where N' equals 16. Patterns are generated in accordance with the JESD204B standard and are different for each output format as defined in 表 7-18. The rules for the pattern are defined below. 式 11 gives the length of the test pattern. The long transport test pattern is the same for link A and link B, where DAx lanes belong to link A and DBx lanes belong to link B.

$$\text{Long Test Pattern Length (Frames)} = K \times \text{ceil}[(M \times S + 2) / K] \quad (11)$$

- Sample Data:
  - Frame 0: Each sample contains N bits, with all samples set to the converter ID (CID) plus 1 (CID + 1). The CID is defined based on the converter number within the link; two links are used in all modes except JMODE 15. Within a link, the converters are numbered by channel (A or B) and in-phase (I) and quadrature-phase (Q) and reset between links. For instance, in JMODE 10, two links are used so channel A and B data are separated into separate links and the in-phase component for each channel has CID = 0 and the quadrature-phase component has CID = 1. In JMODE 15, one link is used, so channel A and B are within the same link and AI has CID = 0, AQ has CID = 1, BI has CID = 2, and BQ has CID = 3.
  - Frame 1: Each sample contains N bits, with each sample (for each converter) set as its individual sample ID (SID) within the frame plus 1 (SID + 1)
  - Frame 2 +: Each sample contains N bits, with the data set to 2^{N-1} for all samples (for example, if N is 15 then 2^{N-1} = 16384)
- Control Bits (if $\overline{CS}$ > 0):
  - Frame 0 to M × S – 1: The control bit belonging to the sample mod (i, S) of the converter floor (i, S) is set to 1 and all others are set to 0, where i is the frame index (i = 0 is the first frame of the pattern). Essentially, the control bit *walks* from the lowest indexed sample to the highest indexed sample and from the lowest indexed converter to the highest indexed converter, changing position every frame.
  - Frame M × S +: All control bits are set to 0

表 7-41 describes an example long transport test pattern for when JMODE = 10, K = 10.

表 7-41. Example Long Transport Test Pattern (JMODE = 10, K = 10)

TIME →																				PATTERN REPEATS →
OCTET NUM	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
DA0	0x0003		0x0002		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x0003	
DA1	0x0004		0x0003		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x0004	
DB0	0x0003		0x0002		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x0003	
DB1	0x0004		0x0003		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x8000		0x0004	
	Frame n		Frame n + 1		Frame n + 2		Frame n + 3		Frame n + 4		Frame n + 5		Frame n + 6		Frame n + 7		Frame n + 8		Frame n + 9		Frame n + 10	

The pattern starts at the end of the initial lane alignment sequence (ILAS) and repeats indefinitely as long as the link remains running. For more details see the JESD204B specification, section 5.1.6.3.

7.4.5.5 D21.5 Test Mode

In this test mode, the controller transmits a continuous stream of D21.5 characters (alternating 0s and 1s).

7.4.5.6 K28.5 Test Mode

In this test mode, the controller transmits a continuous stream of K28.5 characters.

7.4.5.7 Repeated ILA Test Mode

In this test mode, the JESD204B link layer operates normally, except that the ILA sequence (ILAS) repeats indefinitely instead of starting the data phase. Whenever the receiver issues a synchronization request, the transmitter initiates code group synchronization. Upon completion of code group synchronization, the transmitter repeatedly transmits the ILA sequence.

7.4.5.8 Modified RPAT Test Mode

A 12-octet repeating pattern is defined in INCITS TR-35-2004. The purpose of this pattern is to generate white spectral content for JESD204B compliance and jitter testing. 表 7-42 lists the pattern before and after 8b, 10b encoding.

表 7-42. Modified RPAT Pattern Values

OCTET NUMBER	Dx.y NOTATION	8-BIT INPUT TO 8b, 10b ENCODER	20b OUTPUT OF 8b, 10b ENCODER (Two Characters)
0	D30.5	0xBE	0x86BA6
1	D23.6	0xD7	
2	D3.1	0x23	0xC6475
3	D7.2	0x47	
4	D11.3	0x6B	0xD0E8D
5	D15.4	0x8F	
6	D19.5	0xB3	0xCA8B4
7	D20.0	0x14	
8	D30.2	0x5E	0x7949E
9	D27.7	0xFB	
10	D21.1	0x35	0xAA665
11	D25.2	0x59	

7.4.6 Calibration Modes and Trimming

The ADC12DJ3200QML-SP has two calibration modes available: foreground calibration and background calibration. When foreground calibration is initiated the ADCs are automatically taken offline and the output data becomes mid-code (0x000 in 2's complement) while a calibration is occurring. Background calibration allows the ADC to continue normal operation while the ADC cores are calibrated in the background by swapping in a different ADC core to take its place. Additional offset calibration features are available in both foreground and background calibration modes. Further, a number of ADC parameters can be trimmed to optimize performance in a user system.

The ADC12DJ3200QML-SP consists of a total of six sub-ADCs, each referred to as a *bank*, with two banks forming an ADC core. The banks sample out-of-phase so that each ADC core is two-way interleaved. The six banks form three ADC cores, referred to as ADC A, ADC B, and ADC C. In foreground calibration mode, ADC A samples INA± and ADC B samples INB± in dual-channel mode and both ADC A and ADC B sample INA± (or INB±) in single-channel mode. In the background calibration modes, the third ADC core, ADC C, is swapped in periodically for ADC A and ADC B so that they can be calibrated without disrupting operation. 図 7-23 illustrates a diagram of the calibration system including labeling of the banks that make up each ADC core. When calibration is performed the linearity, gain, and offset voltage for each bank are calibrated to an internally generated calibration signal. The analog inputs can be driven during calibration, both foreground and background, except that when offset calibration (OS_CAL or BGOS_CAL) is used there must be no signals (or aliased signals) near DC for proper estimation of the offset (see the *Offset Calibration* section).

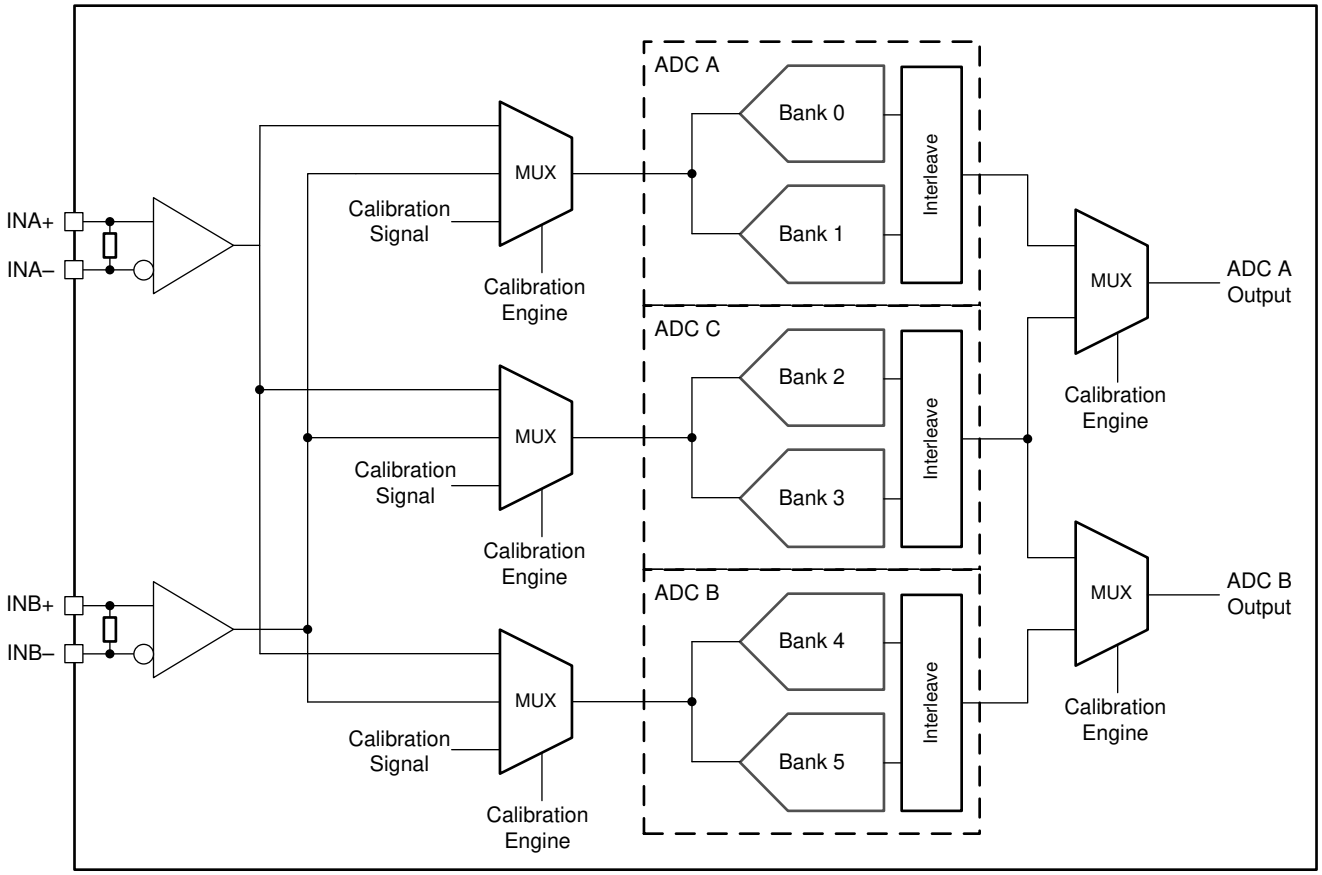

図 7-23. ADC12DJ3200QML-SP Calibration System Block Diagram

In addition to calibration, a number of ADC parameters are user controllable to provide trimming for optimal performance. These parameters include input offset voltage, ADC gain, interleaving timing, and input termination resistance. The default trim values are programmed at the factory to unique values for each device that are determined to be optimal at the test system operating conditions. The user can read the factory-programmed

values from the trim registers and adjust as desired. The register fields that control the trimming are labeled according to the input that is being sampled (INA± or INB±), the bank that is being trimmed, or the ADC core that is being trimmed. The user is not expected to change the trim values as operating conditions change, however optimal performance can be obtained by doing so. Any custom trimming must be done on a per device basis because of process variations, meaning that there is no global optimal setting for all parts. See the *Trimming* section for information about the available trim parameters and associated registers.

7.4.6.1 Foreground Calibration Mode

Foreground calibration requires the ADC to stop converting the analog input signals during the procedure. Foreground calibration always runs on power-up and the user must wait a sufficient time before programming the device to make sure that the calibration is finished. Foreground calibration can be initiated by triggering the calibration engine. The trigger source can be either the CAL_TRIG pin or CAL_SOFT_TRIG (see the calibration software trigger register) and is chosen by setting CAL_TRIG_EN (see the calibration pin configuration register).

7.4.6.2 Background Calibration Mode

Background calibration mode allows the ADC to continuously operate, with no interruption of data. This continuous operation is accomplished by activating an extra ADC core that is calibrated and then takes over operation for one of the other previously active ADC cores. When that ADC core is taken offline, that ADC is calibrated and can in turn take over to allow the next ADC to be calibrated. This process operates continuously, making sure that the ADC cores always provide the optimum performance regardless of system operating condition changes. Because of the additional active ADC core, background calibration mode has increased power consumption in comparison to foreground calibration mode. The low-power background calibration (LPBG) mode discussed in the *Low-Power Background Calibration (LPBG) Mode* section provides reduced average power consumption in comparison with the standard background calibration mode. Background calibration can be enabled by setting CAL_BG (see the calibration configuration 0 register). CAL_TRIG_EN must be set to 0 and CAL_SOFT_TRIG must be set to 1.

Great care has been taken to minimize effects on converted data as the core switching process occurs; however, small brief glitches may still occur on the converter data as the cores are swapped.

7.4.6.3 Low-Power Background Calibration (LPBG) Mode

Low-power background calibration (LPBG) mode reduces the power-overhead of enabling additional ADC cores. Off-line cores are powered down until ready to be calibrated and put on-line. Set LP_EN = 1 to enable the low-power background calibration feature. LP_SLEEP_DLY is used to adjust the amount of time an ADC sleeps before waking up for calibration (if LP_EN = 1 and LP_TRIG = 0). LP_WAKE_DLY sets how long the core is allowed to stabilize before calibration and being put on-line. LP_TRIG is used to select between an automatic switching process or one that is controlled by the user via CAL_SOFT_TRIG or CAL_TRIG. In this mode there is an increase in power consumption during the ADC core calibration. The power consumption roughly alternates between the power consumption in foreground calibration when the spare ADC core is sleeping to the power consumption in background calibration when the spare ADC is being calibrated. Design the power-supply network to handle the transient power requirements for this mode.

7.4.7 Offset Calibration

Foreground calibration and background calibration modes inherently calibrate the offsets of the ADC cores; however, the input buffers sit outside of the calibration loop and therefore their offsets are not calibrated by the standard calibration process. In both dual-channel mode and single-channel mode, uncalibrated input buffer offsets result in a shift in the mid-code output (dc offset) with no input. Further, in single-channel mode uncalibrated input buffer offsets can result in a fixed spur at f_S / 2. A separate calibration is provided to correct the input buffer offsets.

There must be no signals at or near dc, or aliased signals that fall at or near dc, in order to properly calibrate the offsets. These input signals must not exist during normal operation, or the system must be designed to mute the input signal during calibration. Foreground offset calibration is enabled using CAL_OS and only performs the calibration one time as part of the foreground calibration procedure. Background offset calibration is enabled via CAL_BGOS and continues to correct the offset as part of the background calibration routine to account for operating condition changes. When CAL_BGOS is set, the system must make sure that there are no dc or near-dc signals or aliased signals that fall at or near dc during normal operation. Offset calibration can be performed as a foreground operation when using background calibration by setting CAL_OS to 1 before setting CAL_EN, but does not correct for variations as operating conditions change.

The offset calibration correction uses the input offset voltage trim registers (see 表 7-43) to correct the offset and therefore must not be written by the user when offset calibration is used. The user can read the calibrated values by reading the OADJ_x_VINy registers, where x is the ADC core and y is the input (INA± or INB±), after calibration is completed. Only read the values when FG_DONE is read as 1 when using foreground offset calibration (CAL_OS = 1) and do not read the values when using background offset calibration (CAL_BGOS = 1).

7.4.8 Trimming

表 7-43 lists the parameters that can be trimmed and the associated registers.

表 7-43. Trim Register Descriptions

TRIM PARAMETER	TRIM REGISTER	NOTES
Band-gap reference	BG_TRIM	Measurement on BG output pin.
Input termination resistance	RTRIM_x, where x = A for INA± or B for INB±)	The device must be powered on with a clock applied.
Input offset voltage	OADJ_x_VINy, where x = ADC core (A, B or C) and y = A for INA± or B for INB±)	A different trim value is allowed for each ADC core (A, B, or C) to allow more consistent offset performance in background calibration mode.
INA± and INB± gain	GAIN_TRIM_x, where x = A for INA± or B for INB±)	Set FS_RANGE_A and FS_RANGE_B to default values before trimming the input. Use FS_RANGE_A and FS_RANGE_B to adjust the full-scale input voltage.
INA± and INB± full-scale input voltage	FS_RANGE_x, where x = A for INA± or B for INB±)	Full-scale input voltage adjustment for each input. The default value is effected by GAIN_TRIM_x (x = A or B). Trim GAIN_TRIM_x with FS_RANGE_x set to the default value. FS_RANGE_x can then be used to trim the full-scale input voltage.
Intra-ADC core timing (bank timing)	Bx_TIME_y, where x = bank number (0–5) and y = 0° or –90° clock phase	Trims the timing between the two banks of an ADC core (ADC A, B, or C) for two clock phases, either 0° or –90°. The –90° clock phase is used in single-channel mode only.
Inter-ADC core timing (dual-channel mode)	TADJ_A, TADJ_B, TADJ_CA, TADJ_CB	The suffix letter (A, B, CA, or CB) indicates the ADC core that is being trimmed. CA indicates the timing trim in background calibration mode for ADC C when standing in for ADC A, whereas CB is the timing trim for ADC C when standing in for ADC B.
Inter-ADC core timing (single-channel mode)	TADJ_A_FG90, TADJ_B_FG0, TADJ_A_BG90, TADJ_C_BG0, TADJ_C_BG90, TADJ_B_BG0	The middle letter (A, B, or C) indicates the ADC core that is being trimmed. FG indicates a trim for foreground calibration while BG indicates background calibration. The suffix of 0 or 90 indicates the clock phase applied to the ADC core. 0 indicates a 0° clock and is sampling in-phase with the clock input. 90 indicates a 90° clock and therefore is sampling out-of-phase with the clock input. These timings must be trimmed for optimal performance if the user prefers to use INB± in single-channel mode. These timings are trimmed for INA± at the factory.

7.4.9 Offset Filtering

The ADC12DJ3200QML-SP has an additional feature that can be enabled to reduce offset-related interleaving spurs at f_S / 2 and f_S / 4 (single input mode only). Offset filtering is enabled via CAL_OSFILT. The OSFILT_BW and OSFILT_SOAK parameters can be adjusted to tradeoff offset spur reduction with potential impact on information in the mission mode signal being processed. Set these two parameters to the same value under most situations. The DC_RESTORE setting is used to either retain or filter out all DC-related content in the signal.

7.5 Programming

7.5.1 Using the Serial Interface

The serial interface is accessed using the following four pins: serial clock (SCLK), serial data in (SDI), serial data out (SDO), and serial interface chip-select ($\overline{SCS}$). Register access is enabled through the $\overline{SCS}$ pin.

7.5.1.1 $\overline{SCS}$

This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

7.5.1.2 SCLK

Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.

7.5.1.3 SDI

Each register access requires a specific 24-bit pattern at this input. This pattern consists of a read-and-write (R/W) bit, register address, and register value. The data are shifted in MSB first and multi-byte registers are always in little-endian format (least significant byte stored at the lowest address). Setup and hold times with respect to the SCLK must be observed (see the *Timing requirements* table).

7.5.1.4 SDO

The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the read bit and register address portion of read bus cycles.

As shown in 図 7-24, each register access consists of 24 bits. The first bit is high for a read and low for a write.

The next 15 bits are the address of the register that is to be written to. During write operations, the last eight bits are the data written to the addressed register. During read operations, the last eight bits on SDI are ignored and, during this time, the SDO outputs the data from the addressed register. 図 7-24 shows the serial protocol details.

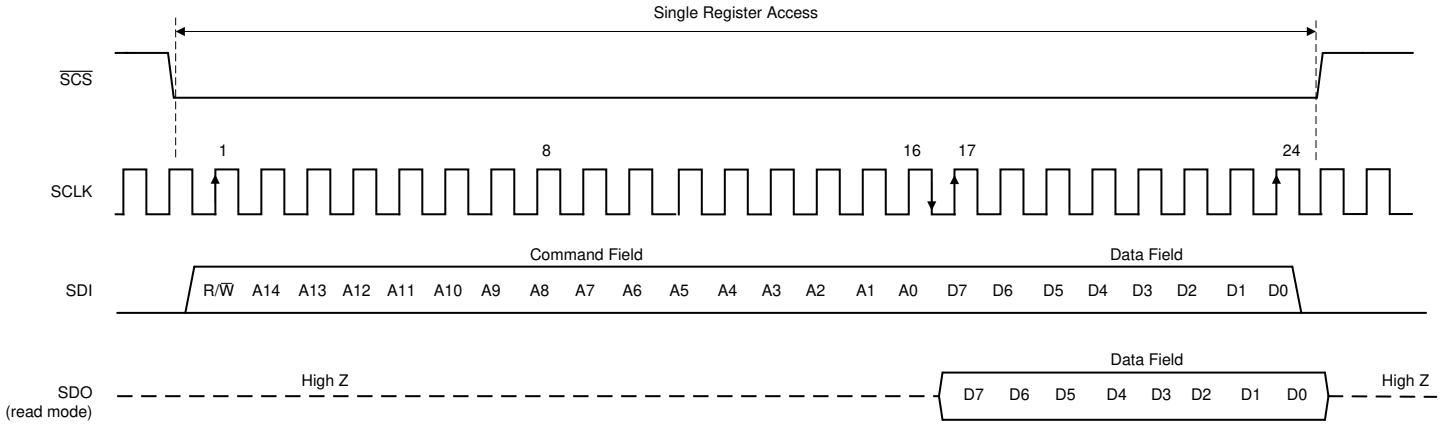

図 7-24. Serial Interface Protocol: Single Read/Write

7.5.1.5 Streaming Mode

The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifics the access type, register address, and data value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the $\overline{SCS}$ input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8-bit transfer of the streaming transaction. The ADDR_ASC bit (register 000h, bits 5 and 2) controls whether the address value ascends (increments) or descends (decrements). Streaming mode can be disabled by setting the ADDR_HOLD bit (see the user SPI configuration register). 図 7-25 shows the streaming mode transaction details.

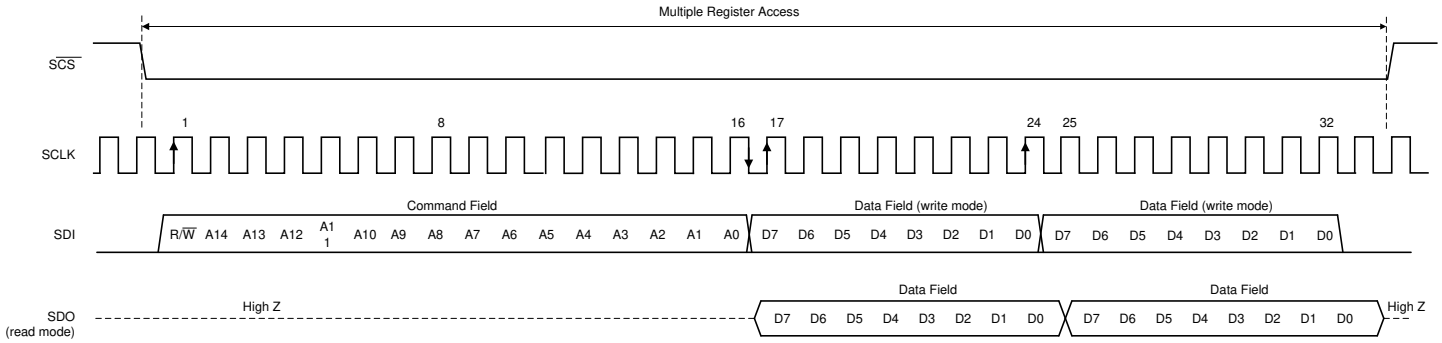

図 7-25. Serial Interface Protocol: Streaming Read and Write

See the セクション 7.6 section for detailed information regarding the registers.

注

The serial interface must not be accessed during ADC calibration. Accessing the serial interface during this time impairs the performance of the device until the device is calibrated correctly. Writing or reading the serial registers also reduces dynamic ADC performance for the duration of the register access time.

7.6 Register Maps

Memory Map lists all the ADC12DJ3200QML-SP registers.

表 7-44.

ADDRESS	RESET	ACRONYM	TYPE	REGISTER NAME
STANDARD SPI-3.0 (0x000 to 0x00F)				
0x000	0x30	CONFIG_A	R/W	Configuration A Register
0x001	Undefined	RESERVED	R	RESERVED
0x002	0x00	DEVICE_CONFIG	R/W	Device Configuration Register
0x003	0x03	CHIP_TYPE	R	Chip Type Register
0x004-0x005	0x0020	CHIP_ID	R	Chip ID Registers
0x006	0x0A	CHIP_VERSION	R	Chip Version Register
0x007-0x00B	Undefined	RESERVED	R	RESERVED
0x00C-0x00D	0x0451	VENDOR_ID	R	Vendor Identification Register
0x00E-0x00F	Undefined	RESERVED	R	RESERVED
USER SPI CONFIGURATION (0x010 to 0x01F)				
0x010	0x00	USR0	R/W	User SPI Configuration Register
0x011-0x01F	Undefined	RESERVED	R	RESERVED
MISCELLANEOUS ANALOG REGISTERS (0x020 to 0x047)				
0x020-0x028	Undefined	RESERVED	R	RESERVED
0x029	0x00	CLK_CTRL0	R/W	Clock Control Register 0
0x02A	0x20	CLK_CTRL1	R/W	Clock Control Register 1
0x02B	Undefined	RESERVED	R	RESERVED
0x02C-0x02E	Undefined	SYSREF_POS	R	SYSREF Capture Position Register
0x02F	Undefined	RESERVED	R	RESERVED
0x030-0x031	0xA000	FS_RANGE_A	R/W	INA Full-Scale Range Adjust Register
0x032-0x033	0xA000	FS_RANGE_B	R/W	INB Full-Scale Range Adjust Register
0x034-0x037	Undefined	RESERVED	R	RESERVED
0x038	0x00	BG_BYPASS	R/W	Internal Reference Bypass Register
0x039-0x03A	Undefined	RESERVED	R	RESERVED
0x03B	0x00	TMSTP_CTRL	R/W	TMSTP± Control Register
0x03C-0x047	Undefined	RESERVED	R	RESERVED
SERIALIZER REGISTERS (0x048 to 0x05F)				
0x048	0x00	SER_PE	R/W	Serializer Pre-Emphasis Control Register
0x049-0x05F	Undefined	RESERVED	R	RESERVED
CALIBRATION REGISTERS (0x060 to 0x0FF)				
0x060	0x01	INPUT_MUX	R/W	Input Mux Control Register
0x061	0x01	CAL_EN	R/W	Calibration Enable Register
0x062	0x01	CAL_CFG0	R/W	Calibration Configuration 0 Register
0x063-0x069	Undefined	RESERVED	R	RESERVED
0x06A	Undefined	CAL_STATUS	R	Calibration Status Register
0x06B	0x00	CAL_PIN_CFG	R/W	Calibration Pin Configuration Register
0x06C	0x01	CAL_SOFT_TRIG	R/W	Calibration Software Trigger Register
0x06D	Undefined	RESERVED	R	RESERVED
0x06E	0x88	CAL_LP	R/W	Low-Power Background Calibration Register
0x06F	Undefined	RESERVED	R	RESERVED
0x070	0x00	CAL_DATA_EN	R/W	Calibration Data Enable Register

表 7-44. (continued)

ADDRESS	RESET	ACRONYM	TYPE	REGISTER NAME
0x071	Undefined	CAL_DATA	R/W	Calibration Data Register
0x072-0x079	Undefined	RESERVED	R	RESERVED
0x07A	Undefined	GAIN_TRIM_A	R/W	Channel A Gain Trim Register
0x07B	Undefined	GAIN_TRIM_B	R/W	Channel B Gain Trim Register
0x07C	Undefined	BG_TRIM	R/W	Band-Gap Reference Trim Register
0x07D	Undefined	RESERVED	R	RESERVED
0x07E	Undefined	RTRIM_A	R/W	VINA Input Resistor Trim Register
0x07F	Undefined	RTRIM_B	R/W	VINB Input Resistor Trim Register
0x080	Undefined	TADJ_A_FG90	R/W	Timing Adjustment for A-ADC, Single-Channel Mode, Foreground Calibration Register
0x081	Undefined	TADJ_B_FG0	R/W	Timing Adjustment for B-ADC, Single-Channel Mode, Foreground Calibration Register
0x082	Undefined	TADJ_A_BG90	R/W	Timing Adjustment for A-ADC, Single-Channel Mode, Background Calibration Register
0x083	Undefined	TADJ_C_BG0	R/W	Timing Adjustment for C-ADC, Single-Channel Mode, Background Calibration Register
0x084	Undefined	TADJ_C_BG90	R/W	Timing Adjustment for C-ADC, Single-Channel Mode, Background Calibration Register
0x085	Undefined	TADJ_B_BG0	R/W	Timing Adjustment for B-ADC, Single-Channel Mode, Background Calibration Register
0x086	Undefined	TADJ_A	R/W	Timing Adjustment for A-ADC, Dual-Channel Mode Register
0x087	Undefined	TADJ_CA	R/W	Timing Adjustment for C-ADC Acting for A-ADC, Dual-Channel Mode Register
0x088	Undefined	TADJ_CB	R/W	Timing Adjustment for C-ADC Acting for B-ADC, Dual-Channel Mode Register
0x089	Undefined	TADJ_B	R/W	Timing Adjustment for B-ADC, Dual-Channel Mode Register
0x08A-0x08B	Undefined	OADJ_A_INA	R/W	Offset Adjustment for A-ADC and INA Register
0x08C-0x08D	Undefined	OADJ_A_INB	R/W	Offset Adjustment for A-ADC and INB Register
0x08E-0x08F	Undefined	OADJ_C_INA	R/W	Offset Adjustment for C-ADC and INA Register
0x090-0x091	Undefined	OADJ_C_INB	R/W	Offset Adjustment for C-ADC and INB Register
0x092-0x093	Undefined	OADJ_B_INA	R/W	Offset Adjustment for B-ADC and INA Register
0x094-0x095	Undefined	OADJ_B_INB	R/W	Offset Adjustment for B-ADC and INB Register
0x096	Undefined	RESERVED	R	RESERVED
0x097	0x00	OSFILT0	R/W	Offset Filtering Control 0
0x098	0x33	OSFILT1	R/W	Offset Filtering Control 1
0x099-0x0FF	Undefined	RESERVED	R	RESERVED
ADC BANK REGISTERS (0x100 to 0x15F)				
0x100-0x101	Undefined	RESERVED	R	RESERVED
0x102	Undefined	B0_TIME_0	R/W	Timing Adjustment for Bank 0 (0° Clock) Register
0x103	Undefined	B0_TIME_90	R/W	Timing Adjustment for Bank 0 (–90° Clock) Register
0x104-0x111	Undefined	RESERVED	R	RESERVED
0x112	Undefined	B1_TIME_0	R/W	Timing Adjustment for Bank 1 (0° Clock) Register
0x113	Undefined	B1_TIME_90	R/W	Timing Adjustment for Bank 1 (–90° Clock) Register
0x114-0x121	Undefined	RESERVED	R	RESERVED
0x122	Undefined	B2_TIME_0	R/W	Timing Adjustment for Bank 2 (0° Clock) Register
0x123	Undefined	B2_TIME_90	R/W	Timing Adjustment for Bank 2 (–90° Clock) Register
0x124-0x131	Undefined	RESERVED	R	RESERVED
0x132	Undefined	B3_TIME_0	R/W	Timing Adjustment for Bank 3 (0° Clock) Register

表 7-44. (continued)

ADDRESS	RESET	ACRONYM	TYPE	REGISTER NAME
0x133	Undefined	B3_TIME_90	R/W	Timing Adjustment for Bank 3 (–90° Clock) Register
0x134-0x141	Undefined	RESERVED	R	RESERVED
0x142	Undefined	B4_TIME_0	R/W	Timing Adjustment for Bank 4 (0° Clock) Register
0x143	Undefined	B4_TIME_90	R/W	Timing Adjustment for Bank 4 (–90° Clock) Register
0x144-0x151	Undefined	RESERVED	R	RESERVED
0x152	Undefined	B5_TIME_0	R/W	Timing Adjustment for Bank 5 (0° Clock) Register
0x153	Undefined	B5_TIME_90	R/W	Timing Adjustment for Bank 5 (–90° Clock) Register
0x154-0x15F	Undefined	RESERVED	R	RESERVED
LSB CONTROL REGISTERS (0x160 to 0x1FF)				
0x160	0x00	ENC_LSB	R/W	LSB Control Bit Output Register
0x161-0x1FF	Undefined	RESERVED	R	RESERVED
JESD204B REGISTERS (0x200 to 0x20F)				
0x200	0x01	JESD_EN	R/W	JESD204B Enable Register
0x201	0x02	JMODE	R/W	JESD204B Mode (JMODE) Register
0x202	0x1F	KM1	R/W	JESD204B K Parameter Register
0x203	0x01	JSYNC_N	R/W	JESD204B Manual SYNC Request Register
0x204	0x02	JCTRL	R/W	JESD204B Control Register
0x205	0x00	JTEST	R/W	JESD204B Test Pattern Control Register
0x206	0x00	DID	R/W	JESD204B DID Parameter Register
0x207	0x00	FCHAR	R/W	JESD204B Frame Character Register
0x208	Undefined	JESD_STATUS	R/W	JESD204B, System Status Register
0x209	0x00	PD_CH	R/W	JESD204B Channel Power-Down
0x20A	0x00	JEXTRA_A	R/W	JESD204B Extra Lane Enable (Link A)
0x20B	0x00	JEXTRA_B	R/W	JESD204B Extra Lane Enable (Link B)
0x20C-0x20F	Undefined	RESERVED	R	RESERVED
DIGITAL DOWN CONVERTER REGISTERS (0x210-0x2AF)				
0x210	0x00	DDC_CFG	R/W	DDC Configuration Register
0x211	0xF2	OVR_T0	R/W	Overrange Threshold 0 Register
0x212	0xAB	OVR_T1	R/W	Overrange Threshold 1 Register
0x213	0x07	OVR_CFG	R/W	Overrange Configuration Register
0x214	0x00	CMODE	R/W	DDC Configuration Preset Mode Register
0x215	0x00	CSEL	R/W	DDC Configuration Preset Select Register
0x216	0x02	DIG_BIND	R/W	Digital Channel Binding Register
0x217-0x218	0x0000	NCO_RDIV	R/W	Rational NCO Reference Divisor Register
0x219	0x02	NCO_SYNC	R/W	NCO Synchronization Register
0x21A-0x21F	Undefined	RESERVED	R	RESERVED
0x220-0x223	0xC0000000	FREQA0	R/W	NCO Frequency (DDC A Preset 0)
0x224-0x225	0x0000	PHASEA0	R/W	NCO Phase (DDC A Preset 0)
0x226-0x227	Undefined	RESERVED	R	RESERVED
0x228-0x22B	0xC0000000	FREQA1	R/W	NCO Frequency (DDC A Preset 1)
0x22C-0x22D	0x0000	PHASEA1	R/W	NCO Phase (DDC A Preset 1)
0x22E-0x22F	Undefined	RESERVED	R	RESERVED
0x230-0x233	0xC0000000	FREQA2	R/W	NCO Frequency (DDC A Preset 2)
0x234-0x235	0x0000	PHASEA2	R/W	NCO Phase (DDC A Preset 2)
0x236-0x237	Undefined	RESERVED	R	RESERVED

表 7-44. (continued)

ADDRESS	RESET	ACRONYM	TYPE	REGISTER NAME
0x238-0x23B	0xC0000000	FREQA3	R/W	NCO Frequency (DDC A Preset 3)
0x23C-0x23D	0x0000	PHASEA3	R/W	NCO Phase (DDC A Preset 3)
0x23E-0x23F	Undefined	RESERVED	R	RESERVED
0x240-0x243	0xC0000000	FREQB0	R/W	NCO Frequency (DDC B Preset 0)
0x244-0x245	0x0000	PHASEB0	R/W	NCO Phase (DDC B Preset 0)
0x246-0x247	Undefined	RESERVED	R	RESERVED
0x248-0x24B	0xC0000000	FREQB1	R/W	NCO Frequency (DDC B Preset 1)
0x24C-0x24D	0x0000	PHASEB1	R/W	NCO Phase (DDC B Preset 1)
0x24E-0x24F	Undefined	RESERVED	R	RESERVED
0x250-0x253	0xC0000000	FREQB2	R/W	NCO Frequency (DDC B Preset 2)
0x254-0x255	0x0000	PHASEB2	R/W	NCO Phase (DDC B Preset 2)
0x256-0x257	Undefined	RESERVED	R	RESERVED
0x258-0x25B	0xC0000000	FREQB3	R/W	NCO Frequency (DDC B Preset 3)
0x25C-0x25D	0x0000	PHASEB3	R/W	NCO Phase (DDC B Preset 3)
0x25E-0x296	Undefined	RESERVED	R	RESERVED
0x297	Undefined	SPIN_ID	R	Spin Identification Value
0x298-0x2AF	Undefined	RESERVED	R	RESERVED
SYSREF CALIBRATION REGISTERS (0x2B0 to 0x2BF)				
0x2B0	0x00	SRC_EN	R/W	SYSREF Calibration Enable Register
0x2B1	0x05	SRC_CFG	R/W	SYSREF Calibration Configuration Register
0x2B2-0x2B4	Undefined	SRC_STATUS	R	SYSREF Calibration Status
0x2B5-0x2B7	0x00	TAD	R/W	DEVCLK Aperture Delay Adjustment Register
0x2B8	0x00	TAD_RAMP	R/W	DEVCLK Timing Adjust Ramp Control Register
0x2B9-0x2BF	Undefined	RESERVED	R	RESERVED
ALARM REGISTERS (0x2C0 to 0x2C2)				
0x2C0	Undefined	ALARM	R	Alarm Interrupt Status Register
0x2C1	0x1F	ALM_STATUS	R/W	Alarm Status Register
0x2C2	0x1F	ALM_MASK	R/W	Alarm Mask Register

7.6.1 Register Descriptions

7.6.1.1 Standard SPI-3.0 (0x000 to 0x00F)

表 7-45. Standard SPI-3.0 Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x000	0x30	CONFIG_A	Configuration A Register	セクション 7.6.1.2
0x001	Undefined	RESERVED	RESERVED	—
0x002	0x00	DEVICE_CONFIG	Device Configuration Register	セクション 7.6.1.3
0x003	0x03	CHIP_TYPE	Chip Type Register	セクション 7.6.1.4
0x004-0x005	0x0020	CHIP_ID	Chip ID Registers	セクション 7.6.1.5
0x006	0x0A	CHIP_VERSION	Chip Version Register	セクション 7.6.1.6
0x007-0x00B	Undefined	RESERVED	RESERVED	—
0x00C-0x00D	0x0451	VENDOR_ID	Vendor Identification Register	セクション 7.6.1.7
0x00E-0x00F	Undefined	RESERVED	RESERVED	—

7.6.1.2 Configuration A Register (address = 0x000) [reset = 0x30]

図 7-26. Configuration A Register (CONFIG_A)

7	6	5	4	3	2	1	0
SOFT_RESET	RESERVED	ADDR_ASC	SDO_ACTIVE	RESERVED			
R/W-0	R-0	R/W-1	R-1	R-0000			

表 7-46. CONFIG_A Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RESET	R/W	0	Setting this bit results in a full reset of the device. This bit is self-clearing. After writing this bit, the device may take up to 750 ns to reset. During this time, do not perform any SPI transactions.
6	RESERVED	R	0	RESERVED
5	ADDR_ASC	R/W	1	0: Descend – decrement address while streaming reads/writes 1: Ascend – increment address while streaming reads/writes (default)
4	SDO_ACTIVE	R	1	Always returns 1, indicating that the device always uses 4-wire SPI mode.
3-0	RESERVED	R	0000	RESERVED

7.6.1.3 Device Configuration Register (address = 0x002) [reset = 0x00]

図 7-27. Device Configuration Register (DEVICE_CONFIG)

7	6	5	4	3	2	1	0
RESERVED						MODE	
R-0000 00						R/W-00	

表 7-47. DEVICE_CONFIG Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0000 00	RESERVED
1-0	MODE	R/W	00	The SPI 3.0 specification lists 1 as the low-power functional mode, 2 as the low-power fast resume, and 3 as power-down. This device does not support these modes. 0: Normal operation – full power and full performance (default) 1: Normal operation – full power and full performance 2: Power down - everything is powered down. Only use this setting for brief periods of time to calibrate the on-chip temperature diode measurement. See the セクション 6.3 table for more information. 3: Power down - everything is powered down. Only use this setting for brief periods of time to calibrate the on-chip temperature diode measurement. See the セクション 6.3 table for more information.

7.6.1.4 Chip Type Register (address = 0x003) [reset = 0x03]

図 7-28. Chip Type Register (CHIP_TYPE)

7	6	5	4	3	2	1	0
RESERVED				CHIP_TYPE			
R-0000				R-0011			

表 7-48. CHIP_TYPE Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000	RESERVED
3-0	CHIP_TYPE	R	0011	Always returns 0x3, indicating that the device is a high-speed ADC.

7.6.1.5 Chip ID Register (address = 0x004 to 0x005) [reset = 0x0020]

図 7-29. Chip ID Register (CHIP_ID)

15	14	13	12	11	10	9	8
CHIP_ID[15:8]							
R-0x00h							
7	6	5	4	3	2	1	0
CHIP_ID[7:0]							
R-0x20h							

表 7-49. CHIP_ID Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CHIP_ID	R	0x0020h	Always returns 0x0020, indicating that this device is an ADC12DJ3200QML-SP device.

7.6.1.6 Chip Version Register (address = 0x006) [reset = 0x01]

図 7-30. Chip Version Register (CHIP_VERSION)

7	6	5	4	3	2	1	0
CHIP_VERSION							
R-0000 1010							

表 7-50. CHIP_VERSION Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CHIP_VERSION	R	0000 1010	Chip version, returns 0x0A.

7.6.1.7 Vendor Identification Register (address = 0x00C to 0x00D) [reset = 0x0451]

図 7-31. Vendor Identification Register (VENDOR_ID)

15	14	13	12	11	10	9	8
VENDOR_ID[15:8]							
R-0x04h							
7	6	5	4	3	2	1	0
VENDOR_ID[7:0]							
R-0x51h							

表 7-51. VENDOR_ID Field Descriptions

Bit	Field	Type	Reset	Description
15-0	VENDOR_ID	R	0x0451h	Always returns 0x0451 (TI vendor ID).

7.6.1.8 User SPI Configuration (0x010 to 0x01F)

表 7-52. User SPI Configuration Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x010	0x00	USR0	User SPI Configuration Register	セクション 7.6.1.9
0x011-0x01F	Undefined	RESERVED	RESERVED	—

7.6.1.9 User SPI Configuration Register (address = 0x010) [reset = 0x00]

図 7-32. User SPI Configuration Register (USR0)

7	6	5	4	3	2	1	0
RESERVED							ADDR_HOLD
R-0000 000							R/W-0

表 7-53. USR0 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	ADDR_HOLD	R/W	0	0: Use the ADDR_ASC bit to define what happens to the address during streaming (default) 1: Address remains static throughout streaming operation; this setting is useful for reading/writing calibration vector information at the CAL_DATA register

7.6.1.10 Miscellaneous Analog Registers (0x020 to 0x047)

表 7-54. Miscellaneous Analog Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x020-0x028	Undefined	RESERVED	RESERVED	—
0x029	0x00	CLK_CTRL0	Clock Control Register 0	セクション 7.6.1.11
0x02A	0x20	CLK_CTRL1	Clock Control Register 1	セクション 7.6.1.12
0x02B	Undefined	RESERVED	RESERVED	—
0x02C-0x02E	Undefined	SYSREF_POS	SYSREF Capture Position Register	セクション 7.6.1.13
0x02F	Undefined	RESERVED	RESERVED	—
0x030-0x031	0xA000	FS_RANGE_A	INA Full-Scale Range Adjust Register	セクション 7.6.1.14
0x032-0x033	0xA000	FS_RANGE_B	INB Full-Scale Range Adjust Register	セクション 7.6.1.15
0x034-0x037	Undefined	RESERVED	RESERVED	—
0x038	0x00	BG_BYPASS	Internal Reference Bypass Register	セクション 7.6.1.16
0x039-0x03A	Undefined	RESERVED	RESERVED	—
0x03B	0x00	SYNC_CTRL	TMSTP± Control Register	セクション 7.6.1.17
0x03C-0x047	Undefined	RESERVED	RESERVED	—

7.6.1.11 Clock Control Register 0 (address = 0x029) [reset = 0x00]

図 7-33. Clock Control Register 0 (CLK_CTRL0)

7	6	5	4	3	2	1	0
RESERVED	SYSREF_PROC_EN	SYSREF_RECV_EN	SYSREF_ZOOM	SYSREF_SEL			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0000			

表 7-55. CLK_CTRL0 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	RESERVED
6	SYSREF_PROC_EN	R/W	0	This bit enables the SYSREF processor. This bit must be set to allow the device to process SYSREF events. SYSREF_RECV_EN must be set before setting SYSREF_PROC_EN.
5	SYSREF_RECV_EN	R/W	0	Set this bit to enable the SYSREF receiver circuit.
4	SYSREF_ZOOM	R/W	0	Set this bit to *zoom* in the SYSREF strobe status (affects SYSREF_POS).
3-0	SYSREF_SEL	R/W	0000	Set this field to select which SYSREF delay to use. Set this field based on the results returned by SYSREF_POS. Set this field to 0 to use SYSREF calibration.

7.6.1.12 Clock Control Register 1 (address = 0x02A) [reset = 0x00]

図 7-34. Clock Control Register 1 (CLK_CTRL1)

7	6	5	4	3	2	1	0
RESERVED					DEVCLK_LVPECL_EN	SYSREF_LVPECL_EN	SYSREF_INVERTED
R/W-0010 0					R/W-0	R/W-0	R/W-0

表 7-56. CLK_CTRL1 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0010 0	RESERVED
2	DEVCLK_LVPECL_EN	R/W	0	Activate low-voltage PECL mode for DEVCLK.
1	SYSREF_LVPECL_EN	R/W	0	Activate low-voltage PECL mode for SYSREF.
0	SYSREF_INVERTED	R/W	0	Inverts the SYSREF signal used for alignment.

7.6.1.13 SYSREF Capture Position Register (address = 0x02C-0x02E) [reset = Undefined]

図 7-35. SYSREF Capture Position Register (SYSREF_POS)

23	22	21	20	19	18	17	16
SYSREF_POS[23:16]							
R-Undefined							
15	14	13	12	11	10	9	8
SYSREF_POS[15:8]							
R-Undefined							
7	6	5	4	3	2	1	0
SYSREF_POS[7:0]							
R-Undefined							

表 7-57. SYSREF_POS Field Descriptions

Bit	Field	Type	Reset	Description
23-0	SYSREF_POS	R	Undefined	This field returns a 24-bit status value that indicates the position of the SYSREF edge with respect to DEVCLK. Use this field to program SYSREF_SEL.

7.6.1.14 INA Full-Scale Range Adjust Register (address = 0x030-0x031) [reset = 0xA000]

図 7-36. INA Full-Scale Range Adjust Register (FS_RANGE_A)

15	14	13	12	11	10	9	8
FS_RANGE_A[15:8]							
R/W-0xA0h							
7	6	5	4	3	2	1	0
FS_RANGE_A[7:0]							
R/W-0x00h							

表 7-58. FS_RANGE_A Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FS_RANGE_A	R/W	0xA000h	This field enables adjustment of the analog full-scale range for INA. 0x0000: Settings below 0x2000 may result in degraded device performance 0x2000: 500 mV_{PP} - Recommended minimum setting 0xA000: 800 mV_{PP} (default) 0xFFFF: 1000 mV_{PP}

7.6.1.15 INB Full-Scale Range Adjust Register (address = 0x032-0x033) [reset = 0xA000]

図 7-37. INB Full Scale Range Adjust Register (FS_RANGE_B)

15	14	13	12	11	10	9	8
FS_RANGE_B[15:8]							
R/W-0xA0							
7	6	5	4	3	2	1	0
FS_RANGE_B[7:0]							
R/W-0x00							

表 7-59. FS_RANGE_B Field Descriptions

Bit	Field	Type	Reset	Description
15-0	FS_RANGE_B	R/W	0xA000h	This field enables adjustment of the analog full-scale range for INB. 0x0000: Settings below 0x2000 may result in degraded device performance 0x2000: 500 mV_{PP} - Recommended minimum setting 0xA000: 800 mV_{PP} (default) 0xFFFF: 1000 mV_{PP}

7.6.1.16 Internal Reference Bypass Register (address = 0x038) [reset = 0x00]

図 7-38. Internal Reference Bypass Register (BG_BYPASS)

7	6	5	4	3	2	1	0
RESERVED							BG_BYPASS
R/W-0000 000							R/W-0

表 7-60. BG_BYPASS Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	BG_BYPASS	R/W	0	When set, VA11 is used as the voltage reference instead of the internal reference.

7.6.1.17 TMSTP± Control Register (address = 0x03B) [reset = 0x00]

図 7-39. TMSTP± Control Register (TMSTP_CTRL)

7	6	5	4	3	2	1	0
RESERVED						TMSTP_LVPECL_EN	TMSTP_RECV_EN
R/W-0000 00						R/W-0	R/W-0

表 7-61. TMSTP_CTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	TMSTP_LVPECL_EN	R/W	0	When set, this bit activates the low-voltage PECL mode for the differential TMSTP± input.
0	TMSTP_RECV_EN	R/W	0	This bit enables the differential TMSTP± input.

7.6.1.18 Serializer Registers (0x048 to 0x05F)

表 7-62. Serializer Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x048	0x00	SER_PE	Serializer Pre-Emphasis Control Register	セクション 7.6.1.19
0x049-0x05F	Undefined	RESERVED	RESERVED	—

7.6.1.19 Serializer Pre-Emphasis Control Register (address = 0x048) [reset = 0x00]

図 7-40. Serializer Pre-Emphasis Control Register (SER_PE)

7	6	5	4	3	2	1	0
RESERVED				SER_PE			
R/W-0000				R/W-0000			

表 7-63. SER_PE Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-0	SER_PE	R/W	0000	This field sets the pre-emphasis for the serial lanes to compensate for the low-pass response of the PCB trace. This setting is a global setting that affects all 16 lanes.

7.6.1.20 Calibration Registers (0x060 to 0x0FF)

表 7-64. Calibration Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x060	0x01	INPUT_MUX	Input Mux Control Register	セクション 7.6.1.21
0x061	0x01	CAL_EN	Calibration Enable Register	セクション 7.6.1.22
0x062	0x01	CAL_CFG0	Calibration Configuration 0 Register	セクション 7.6.1.23
0x063-0x069	Undefined	RESERVED	RESERVED	—
0x06A	Undefined	CAL_STATUS	Calibration Status Register	セクション 7.6.1.24
0x06B	0x00	CAL_PIN_CFG	Calibration Pin Configuration Register	セクション 7.6.1.25
0x06C	0x01	CAL_SOFT_TRIG	Calibration Software Trigger Register	セクション 7.6.1.26
0x06D	Undefined	RESERVED	RESERVED	—
0x06E	0x88	CAL_LP	Low-Power Background Calibration Register	セクション 7.6.1.27
0x06F	Undefined	RESERVED	RESERVED	—
0x070	0x00	CAL_DATA_EN	Calibration Data Enable Register	セクション 7.6.1.28
0x071	Undefined	CAL_DATA	Calibration Data Register	セクション 7.6.1.29
0x072-0x079	Undefined	RESERVED	RESERVED	—
0x07A	Undefined	GAIN_TRIM_A	Channel A Gain Trim Register	セクション 7.6.1.30
0x07B	Undefined	GAIN_TRIM_B	Channel B Gain Trim Register	セクション 7.6.1.31
0x07C	Undefined	BG_TRIM	Band-Gap Reference Trim Register	セクション 7.6.1.32
0x07D	Undefined	RESERVED	RESERVED	—
0x07E	Undefined	RTRIM_A	VINA Input Resistor Trim Register	セクション 7.6.1.33
0x07F	Undefined	RTRIM_B	VINB Input Resistor Trim Register	セクション 7.6.1.34
0x080	Undefined	TADJ_A_FG90	Timing Adjustment for A-ADC, Single-Channel Mode, Foreground Calibration Register	セクション 7.6.1.35
0x081	Undefined	TADJ_B_FG0	Timing Adjustment for B-ADC, Single-Channel Mode, Foreground Calibration Register	セクション 7.6.1.36
0x082	Undefined	TADJ_A_BG90	Timing Adjustment for A-ADC, Single-Channel Mode, Background Calibration Register	セクション 7.6.1.37
0x083	Undefined	TADJ_C_BG0	Timing Adjustment for C-ADC, Single-Channel Mode, Background Calibration Register	セクション 7.6.1.39
0x084	Undefined	TADJ_C_BG90	Timing Adjustment for C-ADC, Single-Channel Mode, Background Calibration Register	セクション 7.6.1.39
0x085	Undefined	TADJ_B_BG0	Timing Adjustment for B-ADC, Single-Channel Mode, Background Calibration Register	セクション 7.6.1.40
0x086	Undefined	TADJ_A	Timing Adjustment for A-ADC, Dual-Channel Mode Register	セクション 7.6.1.41
0x087	Undefined	TADJ_CA	Timing Adjustment for C-ADC Acting for A-ADC, Dual-Channel Mode Register	セクション 7.6.1.42
0x088	Undefined	TADJ_CB	Timing Adjustment for C-ADC Acting for B-ADC, Dual-Channel Mode Register	セクション 7.6.1.43
0x089	Undefined	TADJ_B	Timing Adjustment for B-ADC, Dual-Channel Mode Register	セクション 7.6.1.44
0x08A-0x08B	Undefined	OADJ_A_INA	Offset Adjustment for A-ADC and INA Register	セクション 7.6.1.45
0x08C-0x08D	Undefined	OADJ_A_INB	Offset Adjustment for A-ADC and INB Register	セクション 7.6.1.46
0x08E-0x08F	Undefined	OADJ_C_INA	Offset Adjustment for C-ADC and INA Register	セクション 7.6.1.47
0x090-0x091	Undefined	OADJ_C_INB	Offset Adjustment for C-ADC and INB Register	セクション 7.6.1.48

表 7-64. Calibration Registers (continued)

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x092-0x093	Undefined	OADJ_B_INA	Offset Adjustment for B-ADC and INA Register	セクション 7.6.1.49
0x094-0x095	Undefined	OADJ_B_INB	Offset Adjustment for B-ADC and INB Register	セクション 7.6.1.50
0x096	Undefined	RESERVED	RESERVED	—
0x097	0x00	0SFILT0	Offset Filtering Control 0	セクション 7.6.1.51
0x098	0x33	OSFILT1	Offset Filtering Control 1	セクション 7.6.1.52
0x099-0x0FF	Undefined	RESERVED	RESERVED	—

7.6.1.21 Input Mux Control Register (address = 0x060) [reset = 0x01]

図 7-41. Input Mux Control Register (INPUT_MUX)

7	6	5	4	3	2	1	0
RESERVED			DUAL_INPUT	RESERVED		SINGLE_INPUT	
R/W-000			R/W-0	R/W-00		R/W-01	

表 7-65. INPUT_MUX Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4	DUAL_INPUT	R/W	0	This bit selects inputs for dual-channel modes. If JMODE is selecting a single-channel mode, this register has no effect. 0: A channel samples INA, B channel samples INB (no swap, default) 1: A channel samples INB, B channel samples INA (swap)
3-2	RESERVED	R/W	00	RESERVED
1-0	SINGLE_INPUT	R/W	01	Thid field defines which input is sampled in single-channel mode. If JMODE is not selecting a single-channel mode, this register has no effect. 0: Reserved 1: INA is used (default) 2: INB is used 3: Reserved

7.6.1.22 Calibration Enable Register (address = 0x061) [reset = 0x01]

図 7-42. Calibration Enable Register (CAL_EN)

7	6	5	4	3	2	1	0
RESERVED							CAL_EN
R/W-0000 000							R/W-1

表 7-66. CAL_EN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	CAL_EN	R/W	1	Calibration enable. Set this bit high to run calibration. Set this bit low to hold the calibration in reset to program new calibration settings. Clearing CAL_EN also resets the clock dividers that clock the digital block and JESD204B interface. Some calibration registers require clearing CAL_EN before making any changes. All registers with this requirement contain a note in their descriptions. After changing the registers, set CAL_EN to re-run calibration with the new settings. Always set CAL_EN before setting JESD_EN. Always clear JESD_EN before clearing CAL_EN.

7.6.1.23 Calibration Configuration 0 Register (address = 0x062) [reset = 0x01]

Only change this register when CAL_EN is 0.

図 7-43. Calibration Configuration 0 Register (CAL_CFG0)

7	6	5	4	3	2	1	0
RESERVED			CAL_OSFILT	CAL_BGOS	CAL_OS	CAL_BG	CAL_FG
R/W-000			R/W-0	R/W-0	R/W-0	R/W-0	R/W-1

表 7-67. CAL_CFG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	0000	RESERVED
4	CAL_OSFILT	R/W	0	Enable offset filtering by setting this bit high.
3	CAL_BGOS	R/W	0	0 : Disables background offset calibration (default) 1: Enables background offset calibration (requires CAL_BG to be set).
2	CAL_OS	R/W	0	0 : Disables foreground offset calibration (default) 1: Enables foreground offset calibration (requires CAL_FG to be set)
1	CAL_BG	R/W	0	0 : Disables background calibration (default) 1: Enables background calibration
0	CAL_FG	R/W	1	0 : Resets calibration values, skips foreground calibration 1: Resets calibration values, then runs foreground calibration (default)

7.6.1.24 Calibration Status Register (address = 0x06A) [reset = Undefined]

図 7-44. Calibration Status Register (CAL_STATUS)

7	6	5	4	3	2	1	0
RESERVED						CAL_STOPPED	FG_DONE
R						R	R

表 7-68. CAL_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R		RESERVED
1	CAL_STOPPED	R		This bit returns a 1 when the background calibration has successfully stopped at the requested phase. This bit returns a 0 when calibration starts operating again. If background calibration is disabled, this bit is set when foreground calibration is completed or skipped.
0	FG_DONE	R		This bit is set high when the foreground calibration completes.

7.6.1.25 Calibration Pin Configuration Register (address = 0x06B) [reset = 0x00]

図 7-45. Calibration Pin Configuration Register (CAL_PIN_CFG)

7	6	5	4	3	2	1	0
RESERVED					CAL_STATUS_SEL		CAL_TRIG_EN
R/W-0000 0					R/W-00		R/W-0

表 7-69. CAL_PIN_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0000 0	RESERVED
2-1	CAL_STATUS_SEL	R/W	00	0: CALSTAT output pin matches FG_DONE 1: RESERVED 2: CALSTAT output pin matches ALARM 3: CALSTAT output pin is always low
0	CAL_TRIG_EN	R/W	0	Choose the hardware or software trigger source with this bit. 0: Use the CAL_SOFT_TRIG register for the calibration trigger; the CAL_TRIG input is disabled (ignored) 1: Use the CAL_TRIG input for the calibration trigger; the CAL_SOFT_TRIG register is ignored

7.6.1.26 Calibration Software Trigger Register (address = 0x06C) [reset = 0x01]

図 7-46. Calibration Software Trigger Register (CAL_SOFT_TRIG)

7	6	5	4	3	2	1	0
RESERVED							CAL_SOFT_TRIG
R/W-0000 000							R/W-1

表 7-70. CAL_SOFT_TRIG Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	CAL_SOFT_TRIG	R/W	1	CAL_SOFT_TRIG is a software bit to provide functionality of the CAL_TRIG input. Program CAL_TRIG_EN = 0 to use CAL_SOFT_TRIG for the calibration trigger. If no calibration trigger is needed, leave CAL_TRIG_EN = 0 and CAL_SOFT_TRIG = 1 (trigger is set high).

7.6.1.27 Low-Power Background Calibration Register (address = 0x06E) [reset = 0x88]

図 7-47. Low-Power Background Calibration Register (CAL_LP)

7	6	5	4	3	2	1	0
LP_SLEEP_DLY			LP_WAKE_DLY		RESERVED	LP_TRIG	LP_EN
R/W-010			R/W-01		R/W-0	R/W-0	R/W-0

表 7-71. CAL_LP Field Descriptions

Bit	Field	Type	Reset	Description
7-5	LP_SLEEP_DLY	R/W	010	Adjust how long an ADC sleeps before waking up for calibration (only applies when LP_EN = 1 and LP_TRIG = 0). Values below 4 are not recommended because of limited overall power reduction benefits. 0: Sleep delay = $(2^3 + 1) \times 256 \times t_{DEVCLK}$ 1: Sleep delay = $(2^{15} + 1) \times 256 \times t_{DEVCLK}$ 2: Sleep delay = $(2^{18} + 1) \times 256 \times t_{DEVCLK}$ 3: Sleep delay = $(2^{21} + 1) \times 256 \times t_{DEVCLK}$ 4: Sleep delay = $(2^{24} + 1) \times 256 \times t_{DEVCLK}$: default is approximately 1338 ms with a 3.2-GHz clock 5: Sleep delay = $(2^{27} + 1) \times 256 \times t_{DEVCLK}$ 6: Sleep delay = $(2^{30} + 1) \times 256 \times t_{DEVCLK}$ 7: Sleep delay = $(2^{33} + 1) \times 256 \times t_{DEVCLK}$
4-3	LP_WAKE_DLY	R/W	01	Adjust how much time is given up for settling before calibrating an ADC after wake-up (only applies when LP_EN = 1). Values lower than 1 are not recommended because there is insufficient time for the core to stabilize before calibration begins. 0:Wake Delay = $(2^3 + 1) \times 256 \times t_{DEVCLK}$ 1: Wake Delay = $(2^{18} + 1) \times 256 \times t_{DEVCLK}$: default is approximately 21 ms with a 3.2-GHz clock 2: Wake Delay = $(2^{21} + 1) \times 256 \times t_{DEVCLK}$ 3: Wake Delay = $(2^{24} + 1) \times 256 \times t_{DEVCLK}$
2	RESERVED	R/W	0	RESERVED
1	LP_TRIG	R/W	0	0: ADC sleep duration is set by LP_SLEEP_DLY (autonomous mode) 1: ADCs sleep until woken by a trigger; an ADC is awoken when the calibration trigger (CAL_SOFT_TRIG bit or CAL_TRIG input) is low
0	LP_EN	R/W	0	0: Disables low-power background calibration (default) 1: Enables low-power background calibration (only applies when CAL_BG = 1)

7.6.1.28 Calibration Data Enable Register (address = 0x070) [reset = 0x00]

図 7-48. Calibration Data Enable Register (CAL_DATA_EN)

7	6	5	4	3	2	1	0
RESERVED							CAL_DATA_EN
R/W-0000 000							R/W-0

表 7-72. CAL_DATA_EN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	CAL_DATA_EN	R/W	0	Set this bit to enable the CAL_DATA register to enable reading and writing of calibration data; see the セクション 7.6.1.29 for more information.

7.6.1.29 Calibration Data Register (address = 0x071) [reset = Undefined]

図 7-49. Calibration Data Register (CAL_DATA)

7	6	5	4	3	2	1	0
CAL_DATA							
R/W							

表 7-73. CAL_DATA Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CAL_DATA	R/W	Undefined	After setting CAL_DATA_EN, repeated reads of this register return all calibration values for the ADCs. Repeated writes of this register input all calibration values for the ADCs. To read the calibration data, read the register 673 times. To write the vector, write the register 673 times with previously stored calibration data. To speed up the read/write operation, set ADDR_HOLD = 1 and use the streaming read or write process. Accessing the CAL_DATA register when CAL_STOPPED = 0 corrupts the calibration. Also, stopping the process before reading or writing 673 times leaved the calibration data in an invalid state.

7.6.1.30 Channel A Gain Trim Register (address = 0x07A) [reset = Undefined]

図 7-50. Channel A Gain Trim Register (GAIN_TRIM_A)

7	6	5	4	3	2	1	0
GAIN_TRIM_A							
R/W							

表 7-74. GAIN_TRIM_A Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GAIN_TRIM_A	R/W	Undefined	This register enables gain trim of channel A. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.31 Channel B Gain Trim Register (address = 0x07B) [reset = Undefined]

図 7-51. Channel B Gain Trim Register (GAIN_TRIM_B)

7	6	5	4	3	2	1	0
GAIN_TRIM_B							
R/W							

表 7-75. GAIN_TRIM_B Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GAIN_TRIM_B	R/W	Undefined	This register enables gain trim of channel B. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.32 Band-Gap Reference Trim Register (address = 0x07C) [reset = Undefined]

図 7-52. Band-Gap Reference Trim Register (BG_TRIM)

7	6	5	4	3	2	1	0
RESERVED				BG_TRIM			
R/W-0000				R/W			

表 7-76. BG_TRIM Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-0	BG_TRIM	R/W	Undefined	This register enables the internal band-gap reference to be trimmed. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.33 VINA Input Resistor Trim Register (address = 0x07E) [reset = Undefined]

図 7-53. VINA Input Resistor Trim Register (RTRIM_A)

7	6	5	4	3	2	1	0
RTRIM							
R/W							

表 7-77. RTRIM_A Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RTRIM_A	R/W	Undefined	This register controls the VINA ADC input termination trim. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.34 VINB Input Resistor Trim Register (address = 0x07F) [reset = Undefined]

図 7-54. VINB Input Resistor Trim Register (RTRIM_B)

7	6	5	4	3	2	1	0
RTRIM							
R/W							

表 7-78. RTRIM_B Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RTRIM_B	R/W	Undefined	This register controls the VINB ADC input termination trim. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.35 Timing Adjust for A-ADC, Single-Channel Mode, Foreground Calibration Register (address = 0x080) [reset = Undefined]

図 7-55. Register (TADJ_A_FG90)

7	6	5	4	3	2	1	0
TADJ_A_FG90							
R/W							

表 7-79. TADJ_A_FG90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_A_FG90	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.36 Timing Adjust for B-ADC, Single-Channel Mode, Foreground Calibration Register (address = 0x081) [reset = Undefined]

図 7-56. Register (TADJ_B_FG0)

7	6	5	4	3	2	1	0
TADJ_B_FG0							
R/W							

表 7-80. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_B_FG0	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.37 Timing Adjust for A-ADC, Single-Channel Mode, Background Calibration Register (address = 0x082) [reset = Undefined]

図 7-57. Register (TADJ_A_BG90)

7	6	5	4	3	2	1	0
TADJ_A_BG90							
R/W							

表 7-81. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_A_BG90	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.38 Timing Adjust for C-ADC, Single-Channel Mode, Background Calibration Register (address = 0x083) [reset = Undefined]

図 7-58. Timing Adjust for C-ADC, Single-Channel Mode, Background Calibration Register (TADJ_C_BG0)

7	6	5	4	3	2	1	0
TADJ_C_BG0							
R/W							

表 7-82. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_C_BG0	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.39 Timing Adjust for C-ADC, Single-Channel Mode, Background Calibration Register (address = 0x084) [reset = Undefined]

図 7-59. Timing Adjust for C-ADC, Single-Channel Mode, Background Calibration Register (TADJ_C_BG90)

7	6	5	4	3	2	1	0
TADJ_C_BG90							
R/W							

表 7-83. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_C_BG90	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.40 Timing Adjust for B-ADC, Single-Channel Mode, Background Calibration Register (address = 0x085) [reset = Undefined]

図 7-60. Timing Adjust for B-ADC, Single-Channel Mode, Background Calibration Register (TADJ_B_BG0)

7	6	5	4	3	2	1	0
TADJ_B_BG0							
R/W							

表 7-84. TADJ_B_FG0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_B_BG0	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.41 Timing Adjust for A-ADC, Dual-Channel Mode Register (address = 0x086) [reset = Undefined]

図 7-61. Timing Adjust for A-ADC, Dual-Channel Mode Register (TADJ_A)

7	6	5	4	3	2	1	0
TADJ_A							
R/W							

表 7-85. TADJ_A Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_A	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.42 Timing Adjust for C-ADC Acting for A-ADC, Dual-Channel Mode Register (address = 0x087) [reset = Undefined]

図 7-62. Timing Adjust for C-ADC Acting for A-ADC, Dual-Channel Mode Register (TADJ_CA)

7	6	5	4	3	2	1	0
TADJ_CA							
R/W							

表 7-86. TADJ_CA Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_CA	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.43 Timing Adjust for C-ADC Acting for B-ADC, Dual-Channel Mode Register (address = 0x088) [reset = Undefined]

図 7-63. Timing Adjust for C-ADC Acting for B-ADC, Dual-Channel Mode Register (TADJ_CB)

7	6	5	4	3	2	1	0
TADJ_CB							
R/W							

表 7-87. TADJ_CB Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_CB	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.44 Timing Adjust for B-ADC, Dual-Channel Mode Register (address = 0x089) [reset = Undefined]

図 7-64. Timing Adjust for B-ADC, Dual-Channel Mode Register (TADJ_B)

7	6	5	4	3	2	1	0
TADJ_B							
R/W							

表 7-88. TADJ_B Field Descriptions

Bit	Field	Type	Reset	Description
7-0	TADJ_B	R/W	Undefined	This register (and other subsequent TADJ* registers) are used to adjust the sampling instant of each ADC core. Different TADJ registers apply to different ADCs under different modes or phases of background calibration. After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.45 Offset Adjustment for A-ADC and INA Register (address = 0x08A-0x08B) [reset = Undefined]

図 7-65. Offset Adjustment for A-ADC and INA Register (OADJ_A_INA)

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_INA[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_A_INA[7:0]							
R/W							

表 7-89. OADJ_A_INA Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_A_INA	R/W	Undefined	Offset adjustment value for ADC0 (A-ADC) applied when ADC0 samples INA. The format is unsigned. After reset, the factory-trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS = 1 and CAL_BGOS = 0, only read OADJ* registers if FG_DONE = 1 • If CAL_BG = 1 and CAL_BGOS = 1, only read OADJ* register if CAL_STOPPED = 1

7.6.1.46 Offset Adjustment for A-ADC and INB Register (address = 0x08C-0x08D) [reset = Undefined]

図 7-66. Offset Adjustment for A-ADC and INB Register (OADJ_A_INB)

15	14	13	12	11	10	9	8
RESERVED				OADJ_A_INB[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_A_INB[7:0]							
R/W							

表 7-90. OADJ_A_INB Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_A_INB	R/W	Undefined	Offset adjustment value for ADC0 (A-ADC) applied when ADC0 samples INB. The format is unsigned. After reset, the factory-trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS = 1 and CAL_BGOS = 0, only read OADJ* registers if FG_DONE = 1 • If CAL_BG = 1 and CAL_BGOS = 1, only read OADJ* register if CAL_STOPPED = 1

7.6.1.47 Offset Adjustment for C-ADC and INA Register (address = 0x08E-0x08F) [reset = Undefined]

図 7-67. Offset Adjustment for C-ADC and INA Register (OADJ_C_INA)

15	14	13	12	11	10	9	8
RESERVED				OADJ_C_INA[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_C_INA[7:0]							
R/W							

表 7-91. OADJ_C_INA Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_C_INA	R/W	Undefined	Offset adjustment value for ADC1 (A-ADC) applied when ADC1 samples INA. The format is unsigned. After reset, the factory-trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS = 1 and CAL_BGOS = 0, only read OADJ* registers if FG_DONE = 1 • If CAL_BG = 1 and CAL_BGOS = 1, only read OADJ* register if CAL_STOPPED = 1

7.6.1.48 Offset Adjustment for C-ADC and INB Register (address = 0x090-0x091) [reset = Undefined]

図 7-68. Offset Adjustment for C-ADC and INB Register (OADJ_C_INB)

15	14	13	12	11	10	9	8
RESERVED				OADJ_C_INB[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_C_INB[7:0]							
R/W							

表 7-92. OADJ_C_INB Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_C_INB	R/W	Undefined	Offset adjustment value for ADC1 (A-ADC) applied when ADC1 samples INB. The format is unsigned. After reset, the factory-trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS = 1 and CAL_BGOS = 0, only read OADJ* registers if FG_DONE = 1 • If CAL_BG = 1 and CAL_BGOS = 1, only read OADJ* register if CAL_STOPPED = 1

7.6.1.49 Offset Adjustment for B-ADC and INA Register (address = 0x092-0x093) [reset = Undefined]

図 7-69. Offset Adjustment for B-ADC and INA Register (OADJ_B_INA)

15	14	13	12	11	10	9	8
RESERVED				OADJ_B_INA[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_B_INA[7:0]							
R/W							

表 7-93. OADJ_B_INA Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_B_INA	R/W	Undefined	Offset adjustment value for ADC2 (B-ADC) applied when ADC2 samples INA. The format is unsigned. After reset, the factory-trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS = 1 and CAL_BGOS = 0, only read OADJ* registers if FG_DONE = 1 • If CAL_BG = 1 and CAL_BGOS = 1, only read OADJ* register if CAL_STOPPED = 1

7.6.1.50 Offset Adjustment for B-ADC and INB Register (address = 0x094-0x095) [reset = Undefined]

図 7-70. Offset Adjustment for B-ADC and INB Register (OADJ_B_INB)

15	14	13	12	11	10	9	8
RESERVED				OADJ_B_INB[11:8]			
R/W-0000				R/W			
7	6	5	4	3	2	1	0
OADJ_B_INB[7:0]							
R/W							

表 7-94. OADJ_B_INB Field Descriptions

Bit	Field	Type	Reset	Description
15-12	RESERVED	R/W	0000	RESERVED
11-0	OADJ_B_INB	R/W	Undefined	Offset adjustment value for ADC2 (B-ADC) applied when ADC2 samples INB. The format is unsigned. After reset, the factory-trimmed value can be read and adjusted as required. Important notes: • Never write OADJ* registers while foreground calibration is underway • Never write OADJ* registers if CAL_BG and CAL_BGOS are set • If CAL_OS = 1 and CAL_BGOS=0, only read OADJ* registers if FG_DONE = 1 • If CAL_BG = 1 and CAL_BGOS=1, only read OADJ* register if CAL_STOPPED = 1

7.6.1.51 Offset Filtering Control 0 Register (address = 0x097) [reset = 0x00]

図 7-71. Offset Filtering Control 0 Register (OSFILT0)

7	6	5	4	3	2	1	0
RESERVED							DC_RESTORE
R/W-0000 000							R/W

表 7-95. OSFILT0 Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	DC_RESTORE	R/W	0	When set, the offset filtering feature (enabled by CAL_OSFILT) filters only the offset mismatch across ADC banks and does not remove the frequency content near DC. When cleared, the feature filters all offsets from all banks, thus filtering all DC content in the signal; see the *セクション 7.4.9* section.

7.6.1.52 Offset Filtering Control 1 Register (address = 0x098) [reset = 0x33]

図 7-72. Offset Filtering Control 1 Register (OSFILT1)

7	6	5	4	3	2	1	0
OSFILT_BW				OSFILT_SOAK			
R/W-0011				R/W-0011			

表 7-96. OSFILT1 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	OSFILT_BW	R/W	0011	This field adjusts the IIR filter bandwidth for the offset filtering feature (enabled by CAL_OSFILT). More bandwidth suppresses more flicker noise from the ADCs and reduces the offset spurs. Less bandwidth minimizes the impact of the filters on the mission mode signal. OSFILT_BW: IIR coefficient: –3-dB bandwidth (single sided) 0: Reserved 1: 2^{-10} : 609e-9 × F_{DEVCLK} 2: 2^{-11} : 305e-9 × F_{DEVCLK} 3: 2^{-12} : 152e-9 × F_{DEVCLK} 4: 2^{-13} : 76e-9 × F_{DEVCLK} 5: 2^{-14} : 38e-9 × F_{DEVCLK} 6-15: Reserved
3-0	OSFILT_SOAK	R/W	0011	This field adjusts the IIR soak time for the offset filtering feature. This field applies when offset filtering and background calibration are both enabled. This field determines how long the IIR filter is allowed to settle when first connected to an ADC after the ADC is calibrated. After the soak time completes, the ADC is placed online using the IIR filter. Set OSFILT_SOAK = OSFILT_BW.

7.6.1.53 ADC Bank Registers (0x100 to 0x15F)

表 7-97. ADC Bank Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x100-0x101	Undefined	RESERVED	RESERVED	—
0x102	Undefined	B0_TIME_0	Timing Adjustment for Bank 0 (0° Clock) Register	セクション 7.6.1.54
0x103	Undefined	B0_TIME_90	Timing Adjustment for Bank 0 (–90° Clock) Register	セクション 7.6.1.55
0x104-0x111	Undefined	RESERVED	RESERVED	—
0x112	Undefined	B1_TIME_0	Timing Adjustment for Bank 1 (0° Clock) Register	セクション 7.6.1.56
0x113	Undefined	B1_TIME_90	Timing Adjustment for Bank 1 (–90° Clock) Register	セクション 7.6.1.57
0x114-0x121	Undefined	RESERVED	RESERVED	—
0x122	Undefined	B2_TIME_0	Timing Adjustment for Bank 2 (0° Clock) Register	セクション 7.6.1.58
0x123	Undefined	B2_TIME_90	Timing Adjustment for Bank 2 (–90° Clock) Register	セクション 7.6.1.59
0x124-0x131	Undefined	RESERVED	RESERVED	—
0x132	Undefined	B3_TIME_0	Timing Adjustment for Bank 3 (0° Clock) Register	セクション 7.6.1.60
0x133	Undefined	B3_TIME_90	Timing Adjustment for Bank 3 (–90° Clock) Register	セクション 7.6.1.61
0x134-0x141	Undefined	RESERVED	RESERVED	—
0x142	Undefined	B4_TIME_0	Timing Adjustment for Bank 4 (0° Clock) Register	セクション 7.6.1.62
0x143	Undefined	B4_TIME_90	Timing Adjustment for Bank 4 (–90° Clock) Register	セクション 7.6.1.63
0x144-0x151	Undefined	RESERVED	RESERVED	—
0x152	Undefined	B5_TIME_0	Timing Adjustment for Bank 5 (0° Clock) Register	セクション 7.6.1.64
0x153	Undefined	B5_TIME_90	Timing Adjustment for Bank 5 (–90° Clock) Register	セクション 7.6.1.65
0x154-0x15F	Undefined	RESERVED	RESERVED	—

7.6.1.54 Timing Adjustment for Bank 0 (0° Clock) Register (address = 0x102) [reset = Undefined]

図 7-73. Timing Adjustment for Bank 0 (0° Clock) Register (B0_TIME_0)

7	6	5	4	3	2	1	0
B0_TIME_0							
R/W							

表 7-98. B0_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B0_TIME_0	R/W	Undefined	Time adjustment for bank 0 (applied when the ADC is configured for 0° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.55 Timing Adjustment for Bank 0 (–90° Clock) Register (address = 0x103) [reset = Undefined]

図 7-74. Timing Adjustment for Bank 0 (–90° Clock) Register (B0_TIME_90)

7	6	5	4	3	2	1	0
B0_TIME_90							
R/W							

表 7-99. B0_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B0_TIME_90	R/W	Undefined	Time adjustment for bank 0 (applied when the ADC is configured for –90° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.56 Timing Adjustment for Bank 1 (0° Clock) Register (address = 0x112) [reset = Undefined]

図 7-75. Timing Adjustment for Bank 1 (0° Clock) Register (B1_TIME_0)

7	6	5	4	3	2	1	0
B1_TIME_0							
R/W							

表 7-100. B1_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B1_TIME_0	R/W	Undefined	Time adjustment for bank 1 (applied when the ADC is configured for 0° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.57 Timing Adjustment for Bank 1 (–90° Clock) Register (address = 0x113) [reset = Undefined]

図 7-76. Timing Adjustment for Bank 1 (–90° Clock) Register (B1_TIME_90)

7	6	5	4	3	2	1	0
B1_TIME_90							
R/W							

表 7-101. B1_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B1_TIME_90	R/W	Undefined	Time adjustment for bank 1 (applied when the ADC is configured for –90° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.58 Timing Adjustment for Bank 2 (0° Clock) Register (address = 0x122) [reset = Undefined]

図 7-77. Timing Adjustment for Bank 2 (0° Clock) Register (B2_TIME_0)

7	6	5	4	3	2	1	0
B2_TIME_0							
R/W							

表 7-102. B2_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B2_TIME_0	R/W	Undefined	Time adjustment for bank 2 (applied when the ADC is configured for 0° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.59 Timing Adjustment for Bank 2 (–90° Clock) Register (address = 0x123) [reset = Undefined]

図 7-78. Timing Adjustment for Bank 2 (–90° Clock) Register (B2_TIME_90)

7	6	5	4	3	2	1	0
B2_TIME_90							
R/W							

表 7-103. B2_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B2_TIME_90	R/W	Undefined	Time adjustment for bank 2 (applied when the ADC is configured for –90° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.60 Timing Adjustment for Bank 3 (0° Clock) Register (address = 0x132) [reset = Undefined]

図 7-79. Timing Adjustment for Bank 3 (0° Clock) Register (B3_TIME_0)

7	6	5	4	3	2	1	0
B3_TIME_0							
R/W							

表 7-104. B3_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B3_TIME_0	R/W	Undefined	Time adjustment for bank 3 (applied when the ADC is configured for 0° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.61 Timing Adjustment for Bank 3 (–90° Clock) Register (address = 0x133) [reset = Undefined]

図 7-80. Timing Adjustment for Bank 3 (–90° Clock) Register (B3_TIME_90)

7	6	5	4	3	2	1	0
B3_TIME_90							
R/W							

表 7-105. B3_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B3_TIME_90	R/W	Undefined	Time adjustment for bank 3 (applied when the ADC is configured for –90° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.62 Timing Adjustment for Bank 4 (0° Clock) Register (address = 0x142) [reset = Undefined]

図 7-81. Timing Adjustment for Bank 4 (0° Clock) Register (B4_TIME_0)

7	6	5	4	3	2	1	0
B4_TIME_0							
R/W							

表 7-106. B4_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B4_TIME_0	R/W	Undefined	Time adjustment for bank 4 (applied when the ADC is configured for 0° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.63 Timing Adjustment for Bank 4 (–90° Clock) Register (address = 0x143) [reset = Undefined]

図 7-82. Timing Adjustment for Bank 4 (–90° Clock) Register (B4_TIME_90)

7	6	5	4	3	2	1	0
B4_TIME_90							
R/W							

表 7-107. B4_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B4_TIME_90	R/W	Undefined	Time adjustment for bank 4 (applied when the ADC is configured for –90° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.64 Timing Adjustment for Bank 5 (0° Clock) Register (address = 0x152) [reset = Undefined]

図 7-83. Timing Adjustment for Bank 5 (0° Clock) Register (B5_TIME_0)

7	6	5	4	3	2	1	0
B5_TIME_0							
R/W							

表 7-108. B5_TIME_0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B5_TIME_0	R/W	Undefined	Time adjustment for bank 5 (applied when the ADC is configured for 0° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.65 Timing Adjustment for Bank 5 (–90° Clock) Register (address = 0x153) [reset = Undefined]

図 7-84. Timing Adjustment for Bank 5 (–90° Clock) Register (B5_TIME_90)

7	6	5	4	3	2	1	0
B5_TIME_90							
R/W							

表 7-109. B5_TIME_90 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	B5_TIME_90	R/W	Undefined	Time adjustment for bank 5 (applied when the ADC is configured for –90° clock phase). After reset, the factory-trimmed value can be read and adjusted as required.

7.6.1.66 LSB Control Registers (0x160 to 0x1FF)

表 7-110. LSB Control Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x160	0x00	ENC_LSB	LSB Control Bit Output Register	図 7-73
0x161-0x1FF	Undefined	RESERVED	RESERVED	—

7.6.1.67 LSB Control Bit Output Register (address = 0x160) [reset = 0x00]

図 7-85. LSB Control Bit Output Register (ENC_LSB)

7	6	5	4	3	2	1	0
RESERVED							TIMESTAMP_EN
R/W-0000 000							R/W-0

表 7-111. ENC_LSB Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	TIMESTAMP_EN	R/W	0	When set, the transport layer transmits the timestamp signal on the LSB of the output samples. Only supported in decimate-by-1 (DDC bypass) modes. TIMESTAMP_EN has priority over CAL_STATE_EN. TMSTP_RECV_EN must also be set high when using timestamp. The latency of the timestamp signal (through the entire device) matches the latency of the analog ADC inputs. In 8-bit modes, the control bit is placed on the LSB of the 8-bit samples (leaving 7 bits of sample data). If the device is configured for 12-bit data, the control bit is placed on the LSB of the 12-bit data (leaving 11 bits of sample data). The control bit enabled by this register is never advertised in the ILA (the $\overline{CS}$ field is 0 in the ILA).

7.6.1.68 JESD204B Registers (0x200 to 0x20F)

表 7-112. JESD204B Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x200	0x01	JESD_EN	JESD204B Enable Register	セクション 7.6.1.69
0x201	0x02	JMODE	JESD204B Mode Register	セクション 7.6.1.70
0x202	0x1F	KM1	JESD204B K Parameter Register	セクション 7.6.1.71
0x203	0x01	JSYNC_N	JESD204B Manual SYNC Request Register	セクション 7.6.1.72
0x204	0x02	JCTRL	JESD204B Control Register	セクション 7.6.1.73
0x205	0x00	JTEST	JESD204B Test Pattern Control Register	セクション 7.6.1.74
0x206	0x00	DID	JESD204B DID Parameter Register	セクション 7.6.1.75
0x207	0x00	FCHAR	JESD204B Frame Character Register	セクション 7.6.1.76
0x208	Undefined	JESD_STATUS	JESD204B, System Status Register	セクション 7.6.1.77
0x209	0x00	PD_CH	JESD204B Channel Power-Down	セクション 7.6.1.78
0x20A	0x00	JEXTRA_A	JESD204B Extra Lane Enable (Link A)	セクション 7.6.1.79
0x20B	0x00	JEXTRA_B	JESD204B Extra Lane Enable (Link B)	セクション 7.6.1.80
0x20C-0x20F	Undefined	RESERVED	RESERVED	—

7.6.1.69 JESD204B Enable Register (address = 0x200) [reset = 0x01]

図 7-86. JESD204B Enable Register (JESD_EN)

7	6	5	4	3	2	1	0
RESERVED							JESD_EN
R/W-0000 000							R/W-1

表 7-113. JESD_EN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	JESD_EN	R/W	1	0 : Disables JESD204B interface 1 : Enables JESD204B interface Before altering other JESD204B registers, JESD_EN must be cleared. When JESD_EN is 0, the block is held in reset and the serializers are powered down. The clocks are gated off to save power. The LMFC counter is also held in reset, so SYSREF does not align the LMFC. Always set CAL_EN before setting JESD_EN. Always clear JESD_EN before clearing CAL_EN.

7.6.1.70 JESD204B Mode Register (address = 0x201) [reset = 0x02]

図 7-87. JESD204B Mode Register (JMODE)

7	6	5	4	3	2	1	0
RESERVED			JMODE				
R/W-000			R/W-0001 0				

表 7-114. JMODE Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4-0	JMODE	R/W	0001 0	Specify the JESD204B output mode (including DDC decimation factor). Only change this register when JESD_EN = 0 and CAL_EN = 0.

7.6.1.71 JESD204B K Parameter Register (address = 0x202) [reset = 0x1F]

図 7-88. JESD204B K Parameter Register (KM1)

7	6	5	4	3	2	1	0
RESERVED			KM1				
R/W-000			R/W-1111 1				

表 7-115. KM1 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4-0	KM1	R/W	1111 1	K is the number of frames per multiframe and this register must be programmed as K-1. Depending on the JMODE setting, there are constraints on the legal values of K. (default: KM1 = 31, K = 32). Only change this register when JESD_EN is 0.

7.6.1.72 JESD204B Manual SYNC Request Register (address = 0x203) [reset = 0x01]

図 7-89. JESD204B Manual SYNC Request Register (JSYNC_N)

7	6	5	4	3	2	1	0
RESERVED							JSYNC_N
R/W-0000 000							R/W-1

表 7-116. JSYNC_N Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	JSYNC_N	R/W	1	Set this bit to 0 to request JESD204B synchronization (equivalent to the $\overline{\text{SYNCSE}}$ pin being asserted). For normal operation, leave this bit set to 1. The JSYNC_N register can always generate a synchronization request, regardless of the SYNC_SEL register. However, if the selected sync pin is stuck low, the synchronization request cannot be de-asserted unless SYNC_SEL = 2 is programmed.

7.6.1.73 JESD204B Control Register (address = 0x204) [reset = 0x02]

図 7-90. JESD204B Control Register (JCTRL)

7	6	5	4	3	2	1	0
RESERVED				SYNC_SEL		SFORMAT	SCR
R/W-0000				R/W-00		R/W-1	R/W-0

表 7-117. JCTRL Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-2	SYNC_SEL	R/W	00	0: Use the $\overline{\text{SYNCSE}}$ input for the SYNC~ function (default) 1: Use the TMSTP± differential input for the SYNC~ function; TMSTP_RECV_EN must also be set 2: Do not use any sync input signal (use software SYNC~ through JSYNC_N)
1	SFORMAT	R/W	1	Output sample format for JESD204B samples. 0: Offset binary 1: Signed 2's complement (default)
0	SCR	R/W	0	0: Scrambler disabled (default) 1: Scrambler enabled Only change this register when JESD_EN is 0.

7.6.1.74 JESD204B Test Pattern Control Register (address = 0x205) [reset = 0x00]

図 7-91. JESD204B Test Pattern Control Register (JTEST)

7	6	5	4	3	2	1	0
RESERVED				JTEST			
R/W-0000				R/W-0000			

表 7-118. JTEST Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-0	JTEST	R/W	0000	0: Test mode disabled; normal operation (default) 1: PRBS7 test mode 2: PRBS15 test mode 3: PRBS23 test mode 4: Ramp test mode 5: Transport layer test mode 6: D21.5 test mode 7: K28.5 test mode 8: Repeated ILA test mode 9: Modified RPAT test mode 10: Serial outputs held low 11: Serial outputs held high 12–15: Reserved Only change this register when JESD_EN is 0.

7.6.1.75 JESD204B DID Parameter Register (address = 0x206) [reset = 0x00]

図 7-92. JESD204B DID Parameter Register (DID)

7	6	5	4	3	2	1	0
DID							
R/W-0000 0000							

表 7-119. DID Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DID	R/W	0000 0000	Specifies the device ID (DID) value that is transmitted during the second multiframe of the JESD204B ILA. Link A transmits DID, and link B transmits DID+1. Bit 0 is ignored and always returns 0 (if an odd number is programmed, that number is decremented to an even number). Only change this register when JESD_EN is 0.

7.6.1.76 JESD204B Frame Character Register (address = 0x207) [reset = 0x00]

図 7-93. JESD204B Frame Character Register (FCHAR)

7	6	5	4	3	2	1	0
RESERVED						FCHAR	
R/W-0000 00						R/W-00	

表 7-120. FCHAR Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1-0	FCHAR	R/W	00	Specify which comma character is used to denote end-of-frame. This character is transmitted opportunistically (see the *セクション 7.3.6.3.4* section). 0: Use K28.7 (default, JESD204B compliant) 1: Use K28.1 (not JESD204B compliant) 2: Use K28.5 (not JESD204B compliant) 3: Reserved When using a JESD204B receiver, always use FCHAR = 0. When using a general-purpose 8b, 10b receiver, the K28.7 character may cause issues. When K28.7 is combined with certain data characters, a false, misaligned comma character can result, and some receivers realign to the false comma. To avoid this condition, program FCHAR to 1 or 2. Only change this register when JESD_EN is 0.

7.6.1.77 JESD204B, System Status Register (address = 0x208) [reset = Undefined]

図 7-94. JESD204B, System Status Register (JESD_STATUS)

7	6	5	4	3	2	1	0
RESERVED	LINK_UP	SYNC_STATUS	REALIGNED	ALIGNED	PLL_LOCKED	RESERVED	
R	R	R	R/W	R/W	R	R	

表 7-121. JESD_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	Undefined	RESERVED
6	LINK_UP	R	Undefined	When set, this bit indicates that the JESD204B link is up.
5	SYNC_STATUS	R	Undefined	Returns the state of the JESD204B SYNC~ signal. 0: SYNC~ asserted 1: SYNC~ de-asserted

表 7-121. JESD_STATUS Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	REALIGNED	R/W	Undefined	When high, this bit indicates that an internal digital clock, frame clock, or multiframe (LMFC) clock phase was realigned by SYSREF. Write a 1 to clear this bit.
3	ALIGNED	R/W	Undefined	When high, this bit indicates that the multiframe (LMFC) clock phase has been established by SYSREF. The first SYSREF event after enabling the JESD204B encoder will set this bit. Write a 1 to clear this bit.
2	PLL_LOCKED	R	Undefined	When high, this bit indicates that the PLL is locked.
1-0	RESERVED	R	Undefined	RESERVED

7.6.1.78 JESD204B Channel Power-Down Register (address = 0x209) [reset = 0x00]

図 7-95. JESD204B Channel Power-Down Register (PD_CH)

7	6	5	4	3	2	1	0
RESERVED						PD_BCH	PD_ACH
R/W-0000 00						R/W-0	R/W-0

表 7-122. PD_CH Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	PD_BCH	R/W	0	When set, the *B* ADC channel is powered down. The digital channels that are bound to the *B* ADC channel are also powered down (see the セクション 7.6.1.88). Important notes: Set JESD_EN = 0 before changing PD_CH. To power-down both ADC channels, use MODE. If both channels are powered down, then the entire JESD204B subsystem (including the PLL and LMFC) are powered down If the selected JESD204B mode transmits A and B data on link A, and the B digital channel is disabled, link A remains operational, but the B-channel samples are undefined.
0	PD_ACH	R/W	0	When set, the *A* ADC channel is powered down. The digital channels that are bound to the *A* ADC channel are also powered down (セクション 7.6.1.88). Important notes: Set JESD_EN = 0 before changing PD_CH. To power-down both ADC channels, use MODE. If both channels are powered down, then the entire JESD204B subsystem (including the PLL and LMFC) are powered down If the selected JESD204B mode transmits A and B data on link A, and the B digital channel is disabled, link A remains operational, but the B-channel samples are undefined.

7.6.1.79 JESD204B Extra Lane Enable (Link A) Register (address = 0x20A) [reset = 0x00]

図 7-96. JESD204B Extra Lane Enable (Link A) Register (JEXTRA_A)

7	6	5	4	3	2	1	0
EXTRA_LANE_A							EXTRA_SER_A
R/W-0000 000							R/W-0

表 7-123. JESD204B Extra Lane Enable (Link A) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	EXTRA_LANE_A	R/W	0000 000	Program these register bits to enable extra lanes (even if the selected JMODE does not require the lanes to be enabled). EXTRA_LANE_A(n) enables An (n = 1 to 7). This register enables the link layer clocks for the affected lanes. To also enable the extra serializes set EXTRA_SER_A = 1.
0	EXTRA_SER_A	R/W	0	0: Only the link layer clocks for extra lanes are enabled. 1: Serializers for extra lanes are also enabled. Use this mode to transmit data from the extra lanes. Important notes: Only change this register when JESD_EN = 0. The bit-rate and mode of the extra lanes are set by the JMODE and JTEST parameters. This register does not override the PD_CH register, so ensure that the link is enabled to use this feature. To enable serializer n, the lower number lanes 0 to n-1 must also be enabled, otherwise serializer n does not receive a clock.

7.6.1.80 JESD204B Extra Lane Enable (Link B) Register (address = 0x20B) [reset = 0x00]

図 7-97. JESD204B Extra Lane Enable (Link B) Register (JEXTRA_B)

7	6	5	4	3	2	1	0
EXTRA_LANE_B							EXTRA_SER_B
R/W-0000 000							R/W-0

表 7-124. JESD204B Extra Lane Enable (Link B) Field Descriptions

Bit	Field	Type	Reset	Description
7-1	EXTRA_LANE_B	R/W	0000 000	Program these register bits to enable extra lanes (even if the selected JMODE does not require the lanes to be enabled). EXTRA_LANE_B(n) enables Bn (n = 1 to 7). This register enables the link layer clocks for the affected lanes. To also enable the extra serializes set EXTRA_SER_B = 1.
0	EXTRA_SER_B	R/W	0	0: Only the link layer clocks for extra lanes are enabled. 1: Serializers for extra lanes are also enabled. Use this mode to transmit data from the extra lanes. Important notes: Only change this register when JESD_EN = 0. The bit-rate and mode of the extra lanes are set by the JMODE and JTEST parameters. This register does not override the PD_CH register, so ensure that the link is enabled to use this feature. To enable serializer n, the lower number lanes 0 to n-1 must also be enabled, otherwise serializer n does not receive a clock.

7.6.1.81 Digital Down Converter Registers (0x210-0x2AF)

表 7-125. Digital Down Converter and Overrange Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x210	0x00	DDC_CFG	DDC Configuration Register	セクション 7.6.1.82
0x211	0xF2	OVR_T0	Overrange Threshold 0 Register	セクション 7.6.1.83
0x212	0xAB	OVR_T1	Overrange Threshold 1 Register	セクション 7.6.1.84
0x213	0x07	OVR_CFG	Overrange Configuration Register	セクション 7.6.1.85
0x214	0x00	CMODE	DDC Configuration Preset Mode Register	セクション 7.6.1.86
0x215	0x00	CSEL	DDC Configuration Preset Select Register	セクション 7.6.1.87
0x216	0x02	DIG_BIND	Digital Channel Binding Register	セクション 7.6.1.88
0x217-0x218	0x0000	NCO_RDIV	Rational NCO Reference Divisor Register	セクション 7.6.1.89
0x219	0x02	NCO_SYNC	NCO Synchronization Register	セクション 7.6.1.90
0x21A-0x21F	Undefined	RESERVED	RESERVED	—
0x220-0x223	0xC0000000	FREQA0	NCO Frequency (DDC A Preset 0)	セクション 7.6.1.91
0x224-0x225	0x0000	PHASEA0	NCO Phase (DDC A Preset 0)	セクション 7.6.1.92
0x226-0x227	Undefined	RESERVED	RESERVED	—
0x228-0x22B	0xC0000000	FREQA1	NCO Frequency (DDC A Preset 1)	セクション 7.6.1.91
0x22C-0x22D	0x0000	PHASEA1	NCO Phase (DDC A Preset 1)	セクション 7.6.1.92
0x22E-0x22F	Undefined	RESERVED	RESERVED	—
0x230-0x233	0xC0000000	FREQA2	NCO Frequency (DDC A Preset 2)	セクション 7.6.1.91
0x234-0x235	0x0000	PHASEA2	NCO Phase (DDC A Preset 2)	セクション 7.6.1.92
0x236-0x237	Undefined	RESERVED	RESERVED	—
0x238-0x23B	0xC0000000	FREQA3	NCO Frequency (DDC A Preset 3)	セクション 7.6.1.91
0x23C-0x23D	0x0000	PHASEA3	NCO Phase (DDC A Preset 3)	セクション 7.6.1.92
0x23E-0x23F	Undefined	RESERVED	RESERVED	—
0x240-0x243	0xC0000000	FREQB0	NCO Frequency (DDC B Preset 0)	セクション 7.6.1.91
0x244-0x245	0x0000	PHASEB0	NCO Phase (DDC B Preset 0)	セクション 7.6.1.92
0x246-0x247	Undefined	RESERVED	RESERVED	—
0x248-0x24B	0xC0000000	FREQB1	NCO Frequency (DDC B Preset 1)	セクション 7.6.1.91
0x24C-0x24D	0x0000	PHASEB1	NCO Phase (DDC B Preset 1)	セクション 7.6.1.92
0x24E-0x24F	Undefined	RESERVED	RESERVED	—
0x250-0x253	0xC0000000	FREQB2	NCO Frequency (DDC B Preset 2)	セクション 7.6.1.91
0x254-0x255	0x0000	PHASEB2	NCO Phase (DDC B Preset 2)	セクション 7.6.1.92
0x256-0x257	Undefined	RESERVED	RESERVED	—
0x258-0x25B	0xC0000000	FREQB3	NCO Frequency (DDC B Preset 3)	セクション 7.6.1.91
0x25C-0x25D	0x0000	PHASEB3	NCO Phase (DDC B Preset 3)	セクション 7.6.1.92
0x25E-0x296	Undefined	RESERVED	RESERVED	—
0x297	Undefined	SPIN_ID	Spin Identification Value	セクション 7.6.1.93
0x298-0x2AF	Undefined	RESERVED	RESERVED	—

7.6.1.82 DDC Configuration Register (address = 0x210) [reset = 0x00]

図 7-98. DDC Configuration Register (DDC_CFG)

7	6	5	4	3	2	1	0
RESERVED				D4_AP87	D2_HIGH_PASS	INVERT_SPECTRUM	BOOST
R/W-0000				R/W-0	R/W-0	R/W-0	R/W-0

表 7-126. DDC_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3	D4_AP87	R/W	0	0: Decimate-by-4 mode uses 80% alias protection, > 80-dB suppression 1: Decimate-by-4 mode uses 87.5% alias protection, > 60-dB suppression
2	D2_HIGH_PASS	R/W	0	0: Decimate-by-2 mode uses a low-pass filter 1: Decimate-by-2 mode uses a high-pass filter. Decimating the high-pass signal causes spectral inversion. This inversion can be undone by setting INVERT_SPECTRUM.
1	INVERT_SPECTRUM	R/W	0	0: No inversion applied to output spectrum 1: Output spectrum is inverted This register only applies when the DDC is enabled and is producing a real output (not complex). The spectrum is inverted by mixing the signal with FSOUT / 2 (for example, invert all odd samples).
0	BOOST	R/W	0	DDC gain control. Only applies to DDC modes with complex decimation. 0: Final filter has 0-dB gain (default) 1: Final filter has 6.02-dB gain. Only use this setting when certain that the negative image of the input signal is filtered out by the DDC, otherwise digital clipping may occur.

7.6.1.83 Overrange Threshold 0 Register (address = 0x211) [reset = 0xF2]

図 7-99. Overrange Threshold 0 Register (OVR_T0)

7	6	5	4	3	2	1	0
OVR_T0							
R/W-1111 0010							

表 7-127. OVR_T0 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OVR_T0	R/W	1111 0010	Overrange threshold 0. This parameter defines the absolute sample level that causes control bit 0 to be set. The detection level in dBFS (peak) is: 20_{log10}(OVR_T0 / 256) Default: 0xF2 = 242 → –0.5 dBFS.

7.6.1.84 Overrange Threshold 1 Register (address = 0x212) [reset = 0xAB]

図 7-100. Overrange Threshold 1 Register (OVR_T1)

7	6	5	4	3	2	1	0
OVR_T1							
R/W-1010 1011							

表 7-128. OVR_T1 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OVR_T1	R/W	1010 1011	Overrange threshold 1. This parameter defines the absolute sample level that causes control bit 1 to be set. The detection level in dBFS (peak) is: 20_{log10}(OVR_T1 / 256) Default: 0xAB = 171 → –3.5 dBFS.

7.6.1.85 Overrange Configuration Register (address = 0x213) [reset = 0x07]

図 7-101. Overrange Configuration Register (OVR_CFG)

7	6	5	4	3	2	1	0
RESERVED				OVR_EN	OVR_N		
R/W-0000				R/W-0	R/W-111		

表 7-129. OVR_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000 0	RESERVED
3	OVR_EN	R/W	0	Enables overrange status output pins when set high. The ORA0, ORA1, ORB0, and ORB1 outputs are held low when OVR_EN is set low. This register only effects the overrange output pins (ORxx) and not the overrange status embedded in the data samples.
2-0	OVR_N(1)	R/W	111	Program this register to adjust the pulse extension for the ORA0, ORA1 and ORB0, ORB1 outputs. The minimum pulse duration of the overrange outputs is 8 × 2^{OVR_N} DEVCLK cycles. Incrementing this field doubles the monitoring period.

(1) Changing the OVR_N setting while JESD_EN=1 may cause the phase of the monitoring period to change.

7.6.1.86 DDC Configuration Preset Mode Register (address = 0x214) [reset = 0x00]

図 7-102. DDC Configuration Preset Mode Register (CMODE)

7	6	5	4	3	2	1	0
RESERVED						CMODE	
R/W-0000 00						R/W-00	

表 7-130. CMODE Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1-0	CMODE	R/W	00	The NCO frequency and phase for DDC A are set by the FREQAx and PHASEAx registers and the NCO frequency and phase for DDC B are set by the FREQBx and PHASEBx registers, where *x* is the configuration preset (0 through 3). 0: Use CSEL register to select the active NCO configuration preset for DDC A and DDC B 1: Use NCOA[1:0] pins to select the active NCO configuration preset for DDC A and use NCOB[1:0] pins to select the active NCO configuration preset for DDC B 2: Use NCOA[1:0] pins to select the active NCO configuration preset for both DDC A and DDC B 3: Reserved

7.6.1.87 DDC Configuration Preset Select Register (address = 0x215) [reset = 0x00]

図 7-103. DDC Configuration Preset Select Register (CSEL)

7	6	5	4	3	2	1	0
RESERVED				CSELB		CSELA	
R/W-0000				R/W-00		R/W-00	

表 7-131. CSEL Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000	RESERVED
3-2	CSELB	R/W	00	When CMODE = 0, this register is used to select the active NCO configuration preset for DDC B.
1-0	CSELA	R/W	00	When CMODE = 0, this register is used to select the active NCO configuration preset for DDC A. Example: If CSELA = 0, then FREQA0 and PHASEA0 are the active settings. If CSELA = 1, then FREQA1 and PHASEA1 are the active settings.

7.6.1.88 Digital Channel Binding Register (address = 0x216) [reset = 0x02]

図 7-104. Digital Channel Binding Register (DIG_BIND)

7	6	5	4	3	2	1	0
RESERVED						DIG_BIND_B	DIG_BIND_A
R/W-0000 00						R/W-1	R/W-0

表 7-132. DIG_BIND Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	DIG_BIND_B	R/W	0	Digital channel B input select: 0: Digital channel B receives data from ADC channel A 1: Digital channel B receives data from ADC channel B (default)
0	DIG_BIND_A	R/W	0	Digital channel A input select: 0: Digital channel A receives data from ADC channel A (default) 1: Digital channel A receives data from ADC channel B When using single-channel mode, always use the default setting for DIG_BIND or the device does not work. Set JESD_EN = 0 and CAL_EN = 0 before changing DIG_BIND. The DIG_BIND setting is combined with PD_ACH, PD_BCH to determine if a digital channel is powered down. Each digital channel (and link) is powered down when the ADC channel it is bound to is powered down (by PD_ACH, PD_BCH).

7.6.1.89 Rational NCO Reference Divisor Register (address = 0x217 to 0x218) [reset = 0x0000]

図 7-105. Rational NCO Reference Divisor Register (NCO_RDIV)

15	14	13	12	11	10	9	8
NCO_RDIV[15:8]							
R/W-0000 0000							
7	6	5	4	3	2	1	0
NCO_RDIV[7:0]							
R/W-0000 0000							

表 7-133. NCO_RDIV Field Descriptions

Bit	Field	Type	Reset	Description
15-0	NCO_RDIV	R/W	0x0000h	Sometimes the 32-bit NCO frequency word does not provide the desired frequency step size and can only approximate the desired frequency. This condition results in a frequency error. Use this register to eliminate the frequency error. This register is used for all configuration presets; see the *セクション 7.3.5.1.4* section.

7.6.1.90 NCO Synchronization Register (address = 0x219) [reset = 0x02]

図 7-106. NCO Synchronization Register (NCO_SYNC)

7	6	5	4	3	2	1	0
RESERVED						NCO_SYNC_ILA	NCO_SYNC_NEXT
R/W-0000 00						R/W-1	R/W-0

表 7-134. NCO_SYNC Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	NCO_SYNC_ILA	R/W	0	When this bit is set, the NCO phase is initialized by the LMFC edge that starts the ILA sequence (default).
0	NCO_SYNC_NEXT	R/W	0	After writing a 0 and then a 1 to this bit, the next SYSREF rising edge initializes the NCO phase. When the NCO phase is initialized by SYSREF, the NCO does not reinitialize on future SYSREF edges unless a 0 and a 1 is written to this bit again. Follow these steps to align the NCO in multiple parts: • Ensure the device is powered up, JESD_EN is set, and the device clock is running. • Ensure that SYSREF is disabled (not toggling). • Program NCO_SYNC_ILA = 0 on all devices. • Write NCO_SYNC_NEXT = 0 on all devices. • Write NCO_SYNC_NEXT = 1 on all devices. NCO sync is armed. • Instruct the SYSREF source to generate 1 or more SYSREF pulses. • All devices initialize their NCO using the first SYSREF rising edge.

7.6.1.91 NCO Frequency (DDC A or DDC B and Preset x) Register (address = see 表 7-125) [reset = see 表 7-125]

図 7-107. NCO Frequency (DDC A or DDC B and Preset x) Register (FREQAx or FREQBx)

31	30	29	28	27	26	25	24
FREQAx[31:24] or FREQBx[31:24]							
R/W-0xC0							
23	22	21	20	19	18	17	16
FREQAx[23:16] or FREQBx[23:16]							
R/W-0x00							
15	14	13	12	11	10	9	8
FREQAx[15:8] or FREQBx[15:8]							
R/W-0x00							
7	6	5	4	3	2	1	0
FREQAx[7:0] or FREQBx[7:0]							
R/W-0x00							

表 7-135. FREQAx or FREQBx Field Descriptions

Bit	Field	Type	Reset	Description
31-0	FREQAx or FREQBx	R/W	See 表 7-125	Changing this register after the JESD204B interface is running results in non-deterministic NCO phase. If deterministic phase is required, the JESD204B interface must be re-initialized after changing this register. This register can be interpreted as signed or unsigned. When interpreted as signed (2's complement) the NCO frequency is between $-f_S$ / 2 to f_S / 2. When interpreted as unsigned the NCO frequency is between 0 and f_S.

7.6.1.92 NCO Phase (DDC A or DDC B and Preset x) Register (address = see 表 7-125) [reset = see 表 7-125]

図 7-108. NCO Phase (DDC A or DDC B and Preset x) Register (PHASEAx or PHASEBx)

15	14	13	12	11	10	9	8
PHASEAx[15:8] or PHASEBx[15:8]							
R/W-0x00							
7	6	5	4	3	2	1	0
PHASEAx[7:0] or PHASEBx[7:0]							
R/W-0x00							

表 7-136. PHASEAx or PHASEBx Field Descriptions

Bit	Field	Type	Reset	Description
15-0	PHASEAx or PHASEBx	R/W	See 表 7-125	This value is MSB-justified into a 32-bit field and then added to the phase accumulator. This register can be interpreted as signed or unsigned; see the *セクション 7.3.5.1.5* section.

7.6.1.93 Spin Identification Register (address = 0x297) [reset = Undefined]

図 7-109. Spin Identification Register (SPIN_ID)

7	6	5	4	3	2	1	0
RESERVED			SPIN_ID				
R-000			R				

表 7-137. SPIN_ID Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	000	RESERVED
4-0	SPIN_ID	R	5	Spin identification value. 5 : ADC12DJ3200QML-SP

7.6.2 SYSREF Calibration Registers (0x2B0 to 0x2BF)

表 7-138. SYSREF Calibration Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x2B0	0x00	SRC_EN	SYSREF Calibration Enable Register	セクション 7.6.2.2
0x2B1	0x05	SRC_CFG	SYSREF Calibration Configuration Register	セクション 7.6.2.3
0x2B2-0x2B4	Undefined	SRC_STATUS	SYSREF Calibration Status	セクション 7.6.2.4
0x2B5-0x2B7	0x00	TAD	DEVCLK Aperture Delay Adjustment Register	セクション 7.6.2.5
0x2B8	0x00	TAD_RAMP	DEVCLK Timing Adjust Ramp Control Register	セクション 7.6.2.6
0x2B9-0x2BF	Undefined	RESERVED	RESERVED	—

7.6.2.1 SYSREF Calibration Enable Register (address = 0x2B0) [reset = 0x00]

図 7-110. SYSREF Calibration Enable Register (SRC_EN)

7	6	5	4	3	2	1	0
RESERVED							SRC_EN
R/W-0000 000							R/W-0

表 7-139. SRC_EN Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R/W	0000 000	RESERVED
0	SRC_EN	R/W	0	0: SYSREF calibration disabled; use the TAD register to manually control the TAD[16:0] output and adjust the DEVCLK delay (default) 1: SYSREF calibration enabled; the DEVCLK delay is automatically calibrated; the TAD register is ignored A 0-to-1 transition on SRC_EN starts the SYSREF calibration sequence. Program SRC_CFG before setting SRC_EN. Ensure that ADC calibration is not currently running before setting SRC_EN.

7.6.2.2 SYSREF Calibration Configuration Register (address = 0x2B1) [reset = 0x05]

図 7-111. SYSREF Calibration Configuration Register (SRC_CFG)

7	6	5	4	3	2	1	0
RESERVED				SRC_AVG		SRC_HDUR	
R/W-0000				R/W-01		R/W-01	

表 7-140. SRC_CFG Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0000 00	RESERVED
3-2	SRC_AVG	R/W	01	Specifies the amount of averaging used for SYSREF calibration. Larger values increase calibration time and reduce the variance of the calibrated value. 0: 4 averages 1: 16 averages 2: 64 averages 3: 256 averages
1-0	SRC_HDUR	R/W	01	Specifies the duration of each high-speed accumulation for SYSREF Calibration. If the SYSREF period exceeds the supported value, the calibration fails. Larger values increase calibration time and support longer SYSREF periods. For a given SYSREF period, larger values also reduce the variance of the calibrated value. 0: 4 cycles per accumulation, max SYSREF period of 85 DEVCLK cycles 1: 16 cycles per accumulation, max SYSREF period of 1100 DEVCLK cycles 2: 64 cycles per accumulation, max SYSREF period of 5200 DEVCLK cycles 3: 256 cycles per accumulation, max SYSREF period of 21580 DEVCLK cycles Max duration of SYSREF calibration is bounded by: $T_{SYSREFCAL}$ (in DEVCLK cycles) = 256 × 19 × $4^{(SRC\_AVG + SRC\_HDUR + 2)}$

7.6.2.3 SYSREF Calibration Status Register (address = 0x2B2 to 0x2B4) [reset = Undefined]

図 7-112. SYSREF Calibration Status Register (SRC_STATUS)

23	22	21	20	19	18	17	16
RESERVED						SRC_DONE	SRC_TAD[16]
R						R	R
15	14	13	12	11	10	9	8
SRC_TAD[15:8]							
R							
7	6	5	4	3	2	1	0
SRC_TAD[7:0]							
R							

表 7-141. SRC_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
23-18	RESERVED	R	Undefined	RESERVED
17	SRC_DONE	R	Undefined	This bit returns a 1 when SRC_EN = 1 and SYSREF calibration is complete.
16-0	SRC_TAD	R	Undefined	This field returns the value for TAD[16:0] computed by the SYSREF calibration. This field is only valid if SRC_DONE = 1.

7.6.2.4 DEVCLK Aperture Delay Adjustment Register (address = 0x2B5 to 0x2B7) [reset = 0x000000]

図 7-113. DEVCLK Aperture Delay Adjustment Register (TAD)

23	22	21	20	19	18	17	16
RESERVED							TAD_INV
R/W-0000 000							R/W-0
15	14	13	12	11	10	9	8
TAD_COARSE							
R/W-0000 0000							
7	6	5	4	3	2	1	0
TAD_FINE							
R/W-0000 0000							

表 7-142. TAD Field Descriptions

Bit	Field	Type	Reset	Description
23-17	RESERVED	R/W	0000 000	RESERVED
16	TAD_INV	R/W	0	Invert DEVCLK by setting this bit equal to 1.
15-8	TAD_COARSE	R/W	0000 0000	This register controls the DEVCLK aperture delay adjustment when SRC_EN = 0. Use this register to manually control the DEVCLK aperture delay when SYSREF calibration is disabled. If ADC calibration or JESD204B is running, TI recommends gradually increasing or decreasing this value (1 code at a time) to avoid clock glitches. See the *セクション 6.10* table for TAD_COARSE resolution.
7-0	TAD_FINE	R/W	0000 0000	See the *セクション 6.10* table for TAD_FINE resolution.

7.6.2.5 DEVCLK Timing Adjust Ramp Control Register (address = 0x2B8) [reset = 0x00]

図 7-114. DEVCLK Timing Adjust Ramp Control Register (TAD_RAMP)

7	6	5	4	3	2	1	0
RESERVED						TAD_RAMP_RATE	TAD_RAMP_EN
R/W-0000 00						R/W-0	R/W-0

表 7-143. TAD_RAMP Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R/W	0000 00	RESERVED
1	TAD_RAMP_RATE	R/W	0	Specifies the ramp rate for the TAD[15:8] output when the TAD[15:8] register is written when TAD_RAMP_EN = 1. 0: TAD[15:8] ramps up or down one code per 256 DEVCLK cycles. 1: TAD[15:8] ramps up or down 4 codes per 256 DEVCLK cycles.
0	TAD_RAMP_EN	R/W	0	TAD ramp enable. Set this bit if coarse TAD adjustments are desired to ramp up or down instead of changing abruptly. 0: After writing the TAD[15:8] register the aperture delay is updated within 1024 DEVCLK cycles 1: After writing the TAD[15:8] register the aperture delay ramps up or down until the aperture delay matches the TAD[15:8] register

7.6.3 Alarm Registers (0x2C0 to 0x2C2)

表 7-144. Alarm Registers

ADDRESS	RESET	ACRONYM	REGISTER NAME	SECTION
0x2C0	Undefined	ALARM	Alarm Interrupt Status Register	セクション 7.6.3.2
0x2C1	0x1F	ALM_STATUS	Alarm Status Register	セクション 7.6.3.3
0x2C2	0x1F	ALM_MASK	Alarm Mask Register	セクション 7.6.3.4

7.6.3.1 Alarm Interrupt Register (address = 0x2C0) [reset = Undefined]

図 7-115. Alarm Interrupt Register (ALARM)

7	6	5	4	3	2	1	0
RESERVED							ALARM
R							R

表 7-145. ALARM Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	Undefined	RESERVED
0	ALARM	R	Undefined	This bit returns a 1 whenever any alarm occurs that is unmasked in the ALM_STATUS register. Use ALM_MASK to mask (disable) individual alarms. CAL_STATUS_SEL can be used to drive the ALARM bit onto the CALSTAT output pin to provide a hardware alarm interrupt signal.

7.6.3.2 Alarm Status Register (address = 0x2C1) [reset = 0x1F]

図 7-116. Alarm Status Register (ALM_STATUS)

7	6	5	4	3	2	1	0
RESERVED			PLL_ALM	LINK_ALM	REALIGNED_ALM	NCO_ALM	CLK_ALM
R/W-000			R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

表 7-146. ALM_STATUS Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4	PLL_ALM	R/W	1	PLL lock lost alarm. This bit is set whenever the PLL is not locked. Write a 1 to clear this bit.
3	LINK_ALM	R/W	1	Link alarm. This bit is set whenever the JESD204B link is enabled, but is not in the DATA_ENC state. Write a 1 to clear this bit.
2	REALIGNED_ALM	R/W	1	Realigned alarm. This bit is set whenever SYSREF causes the internal clocks (including the LMFC) to be realigned. Write a 1 to clear this bit.
1	NCO_ALM	R/W	1	NCO alarm. This bit can be used to detect an upset to the NCO phase. This bit is set when any of the following occur: • The NCOs are disabled (JESD_EN = 0) • The NCOs are synchronized (intentionally or unintentionally) • Any phase accumulators in channel A do not match channel B Write a 1 to clear this bit.
0	CLK_ALM	R/W	1	Clock alarm. This bit can be used to detect an upset to the digital block and JESD204B clocks. This bit is set whenever the internal clock dividers for the A and B channels do not match. Write a 1 to clear this bit.

7.6.3.3 Alarm Mask Register (address = 0x2C2) [reset = 0x1F]

図 7-117. Alarm Mask Register (ALM_MASK)

7	6	5	4	3	2	1	0
RESERVED			MASK_PLL_ALM	MASK_LINK_ALM	MASK_REALIGNED_ALM	MASK_NCO_ALM	MASK_CLK_ALM
R/W-000			R/W-1	R/W-1	R/W-1	R/W-1	R/W-1

表 7-147. ALM_MASK Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R/W	000	RESERVED
4	MASK_PLL_ALM	R/W	1	When set, PLL_ALM is masked and does not impact the ALARM register bit.
3	MASK_LINK_ALM	R/W	1	When set, LINK_ALM is masked and does not impact the ALARM register bit.
2	MASK_REALIGNED_ALM	R/W	1	When set, REALIGNED_ALM is masked and does not impact the ALARM register bit.
1	MASK_NCO_ALM	R/W	1	When set, NCO_ALM is masked and does not impact the ALARM register bit.
0	MASK_CLK_ALM	R/W	1	When set, CLK_ALM is masked and does not impact the ALARM register bit.

8 Application Information Disclaimer

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ADC12DJ3200QML-SP can be used in a wide range of space-based applications including wideband satellite communications (SATCOM) and synthetic aperture radar (SAR). The wide input bandwidth enables direct RF sampling to at least 8 GHz and the high sampling rate allows signal bandwidths of greater than 2 GHz. The *セクション 8.2* section describes one configuration that meets the needs of a number of these applications while the following sections describe generic application information.

8.1.1 Analog Inputs

Most applications can be narrowed down into two categories: those that need DC coupling and those that do not need DC coupling. The needs and interface recommendations for each category are different. In most cases, the driving circuit will need to perform a conversion from single-ended signaling at the signal source to differential signaling for the ADC12DJ3200QML-SP inputs.

Applications that require DC coupling will need to use a DC coupled amplifier to drive the ADC. DC coupling is often more difficult due to the need for matched common-mode voltage (V_{CM}) between the driver amplifier and ADC12DJ3200QML-SP. ADC12DJ3200QML-SP makes this easy for many applications due to the 0-V input common-mode voltage (V_{ICM}). A 0-V V_{ICM} allows a split supply differential amplifier to drive the ADC directly with no V_{CM} shift which in turn allows the amplifier to operate at its optimal operating point, typically with an output common-mode voltage (V_{OCM}) equal to the midpoint of the two supplies. If the differential amplifier has a pin to set its V_{OCM} then that pin can be tied directly to GND. An example amplifier that is capable of driving ADC12DJ3200QML-SP is the LMH5401-SP which is capable of converting from single-ended to differential signaling and has a high gain-bandwidth product to match the ADC12DJ3200QML-SP bandwidth capabilties.

The second category, applications that do not require DC coupling, will often find that best performance can be achieved using transformers or baluns to convert from single-ended to differential signaling. These transformers can also perform impedance conversion such that a 50-Ω, single-ended source is well matched to the 100-Ω, differential termination inside the ADC12DJ3200QML-SP. For instance, a 1:2 impedance ratio transformer can provide both single-ended to differential conversion and proper impedance matching. The transformer outputs can be either AC-coupled, or directly connected to the ADC differential inputs, which are terminated internally to GND on each input pin through a 50-Ω resistor. Baluns must be selected to cover the needed frequency range, have a 1:2 impedance ratio, and have acceptable gain and phase balance over the frequency range of interest. Poor gain and phase balance will result in degraded 2nd-harmonic distortion performance. 表 8-1 lists a number of recommended baluns for different frequency ranges, but is not fully inclusive.

表 8-1. Recommended Baluns

PART NUMBER	MANUFACTURER(1)	MINIMUM FREQUENCY (MHz)	MAXIMUM FREQUENCY (MHz)
BAL-0009SMG	Marki Microwave	0.5	9000
BAL-0208SMG	Marki Microwave	2000	8000
TCM2-43X+	Mini-Circuits	10	4000
TCM2-33WX+	Mini-Circuits	10	3000
B0430J50100AHF	Anaren	400	3000

(1) See the *Third-Party Products Disclaimer* section.

8.1.2 Analog Input Bandwidth

ADC12DJ3200QML-SP has a very high full-power input bandwidth to allow direct sampling of signals up to 10 GHz. In many cases, a transformer or balun is used to convert the front-end signal chain's single-ended signals to the differential signals ADC12DJ3200QML-SP requires. A 2:1 transformer will present a 100-Ω differential source impedance to the ADC from a single-ended 50-Ω source, however baluns or transformers with poor output return loss (not well matched to differential 100 Ω impedance) will result in frequency ripple in the ADC12DJ3200QML-SP frequency response. To improve the frequency ripple, resistive attenuators (Pi- or T-type) can be used to improve the output return loss of the drive component to dampen frequency response ripples at the cost of additional gain and drive strength in the preceding amplifier chain. Typically, 3 dB of attenuation is sufficient to dampen frequency response ripple introduced by poor output return loss. To be more general, achieving maximum frequency response flatness (as shown in 図 6-68) with ADC12DJ3200QML-SP requires the output impedance of the device or passive component preceding the ADC12DJ3200QML-SP to be well matched to a differential, 100-Ω resistance. Additional impedance matching will not typically improve bandwidth.

8.1.3 Clocking

The ADC12DJ3200QML-SP clock inputs must be AC-coupled to the device to provide rated performance. The clock source must have extremely low jitter (integrated phase noise) to achieve rated performance. Recommended clock synthesizers include the LMX2615-SP.

The JESD204B data converter system (ADC plus FPGA) requires additional SYSREF and device clocks. The LMK04832 device is an excellent choice to generate these clocks. Depending on the ADC clock frequency and jitter requirements, this device may also be used as the system clock synthesizer or as a device clock and SYSREF distribution device when multiple ADC12DJ3200QML-SP devices are used in a system.

8.1.4 Radiation Environment Recommendations

Careful consideration should be given to the environmental conditions when using a product in a radiation environment.

8.1.4.1 Single Event Latch-Up (SEL)

One-time single event latch-up (SEL) testing was performed according to EIA/JEDEC Standard, EIA/JEDEC57. The linear energy transfer threshold (LETth) shown in Features is the maximum LET tested.

8.1.4.2 Single Event Functional Interrupt (SEFI)

The register map of ADC12DJ3200QML-SP was designed to hold the programmed values during radiation events up to the maximum LET used for SEL testing.

8.1.4.3 Single Event Upset (SEU)

The high speed digital path of ADC12DJ3200QML-SP, including the DDC block and JESD204B block, is susceptible to radiation events. The following recommendations are provided to allow automatic recovery and to improve the recovery time of the JESD204B interface block of ADC12DJ3200QML-SP after being upset.

- Always use a continuous, periodic SYSREF in order to quickly recover internal clocks and counters. Set the period to be long enough to limit spurious performance degradation caused by coupling, but short enough to recover within the system requirements. SYSREF will help both the transmitter (ADC12DJ3200QML-SP) and receiver (FPGA or ASIC) recover after an SEU. SYSREF sets an upper bound for the time the link takes to discover a frame or multi-frame misalignment. As a minimum requirement, SYSREF must be activated when the receiver asserts the JESD204B $\overline{\text{SYNC}}$ signal.
- The receiver (FPGA or ASIC) must perform frame and multiframe alignment monitoring. Monitoring should include looking for misplaced or missing end-of-frame and end-of-multiframe characters. Misplaced characters are those that occur in the incorrect spot of a frame or multiframe, meaning not the last character of a frame or multiframe. Missing characters are those that the receiver deems should be included at the end of a frame or multiframe based on the character replacement rules of JESD204B. When two or more misplaced or missing characters are found (without receiving any in the correct position), the link should be reestablished by asserting $\overline{\text{SYNC}}$ to restart the CGS and ILAS processes.
- Enable scrambling to make sure the alignment characters are generated with consistent probabilities independent of the ADC data. Not using scrambling could result in long recovery times after a shift in frame or multiframe alignment.
- Make sure that the receiver frame-alignment state machine is implemented according to the JESD204B standard, including support for reinitialization over the data interface. If the transmitter (ADC12DJ3200QML-SP) re-initializes the link (indicated by sending K28.5 characters without the receiver asserting the $\overline{\text{SYNC}}$ signal) the receiver should transition to the initial frame and lane alignment states.
- Additional robustness can be achieved in the 12-bit, DDC bypass JMODEs by monitoring the four tail bits at the end of each frame. Missing or misplaced tail bits can be treated the same as a frame misalignment error.

The accumulators of the numerically-controlled oscillators (NCOs) used by the DDC block are also susceptible to upsets. An upset of the NCO phase can be detected by using the NCO upset alarm feature described in セクション 7.3.7.1. After an upset has been detected, the NCO must be reinitialized if phase synchronization between multiple ADC12DJ3200QML-SP devices is required. A more robust solution can be achieved if the NCO frequency is chosen to be a harmonic of the SYSREF frequency (integer related to the SYSREF frequency) and NCO synchronization using SYSREF (AC coupled) described in NCO Phase Synchronization is used. This allows SYSREF to automatically reset the NCO phase after an upset and automatically recovers the phase synchronization between multiple ADC12DJ3200QML-SP devices without having to resynchronize all ADC12DJ3200QML-SP devices in the system. This condition is met if $f_{NCO} = n \times f_{SYSREF}$.

8.2 Typical Application

A common use-case for ADC12DJ3200QML-SP is as the digitizer in a wideband RF sampling receiver. Many applications, such as wideband satellite communications or synthetic aperture radar (SAR), will fall into this common configuration. In this case, DC coupling is not required and therefore a transformer or balun is used to interface the single-ended amplifier with the differential inputs of ADC12DJ3200QML-SP.

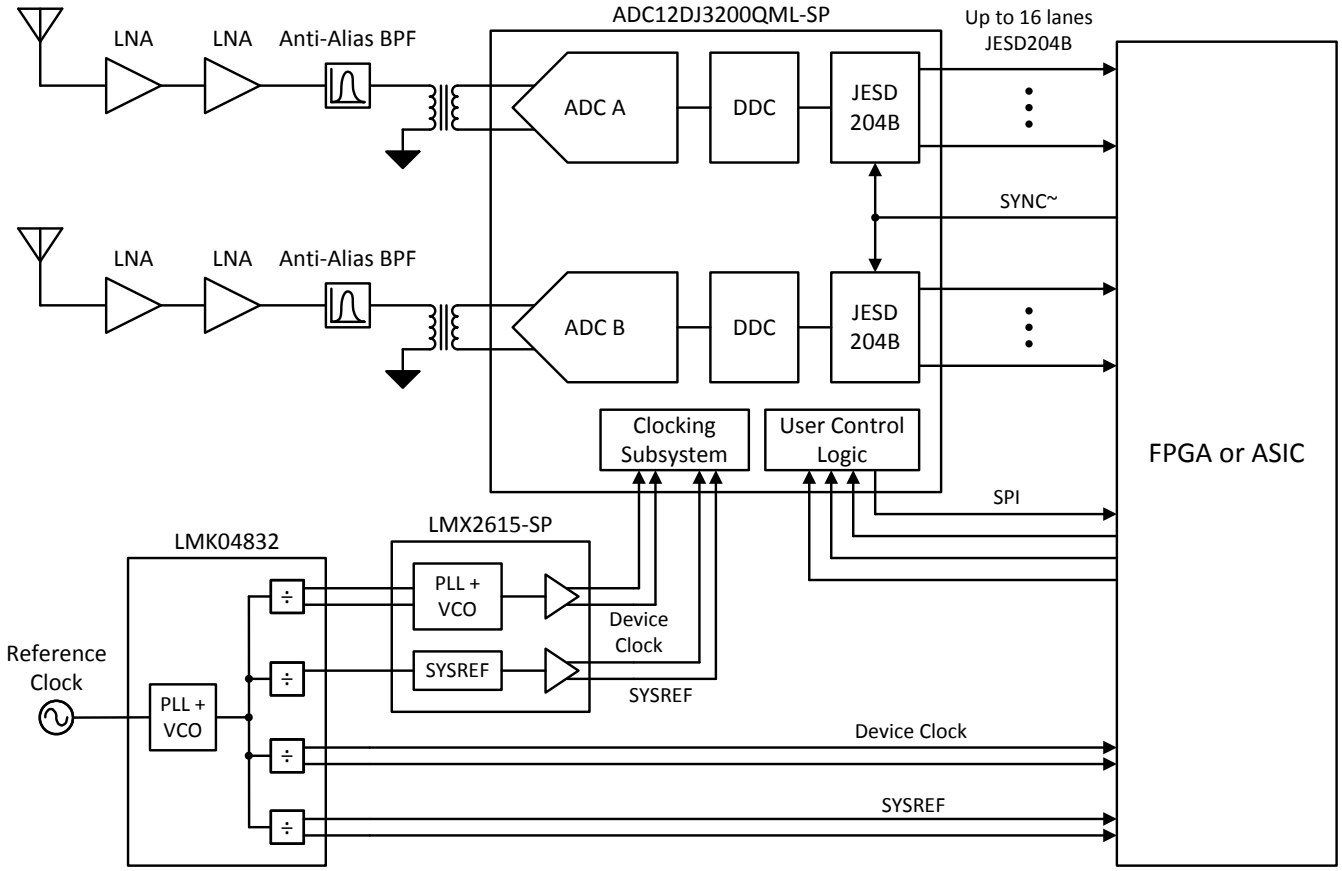


図 8-1. Typical Configuration for Wideband RF Sampling Receiver

8.2.1 Design Requirements

A wideband RF sampling receiver can be configured in a number of different modes. For instance, ADC12DJ3200QML-SP could operate in dual channel mode and sample in either the 1st, 2nd or 3rd Nyquist zone. However, in this example assume that ADC12DJ3200QML-SP operates in single-channel mode at a sampling rate of 6.4 GSPS and the 2nd Nyquist zone is used. The input signals can then be between 3.2 GHz to 6.4 GHz, less anti-alias filtering margin, when running in single-channel mode at 6.4 GSPS. The RF components are not addressed in detail here, but instead is discussed in generalities in the *RF Input Signal Path* section.

表 8-2. Wideband RF Sampling Receiver System Requirements

System Requirement	Specification	Units
Sampling rate	6.4	GSPS
Instantaneous signal bandwidth	2.5	GHz
Input signal center frequency	4.8	GHz
ADC interface	JESD204B	—
Maximum SerDes line rate	6.4	Gbps

8.2.2 Detailed Design Procedure

The component selection and ADC12DJ3200QML-SP configuration for the application described in セクション 8.2.1 is discussed is this section. The components of the wideband RF sampling receiver are given in 表 8-3 along with the reason for the selection.

表 8-3. Wideband RF Sampling Receiver Component Selection

COMPONENT	SELECTION	REASON
ADC	Texas Instruments' ADC12DJ3200QML-SP	Sampling rate requirement (6.4 GSPS) and high input frequency makes ADC12DJ3200QML-SP a natural choice.
Sampling clock generation	Texas Instruments' LMX2615-SP	LMX2615-SP generates a high performing sampling clock due to low jitter (45 fs) and high output swing. The SYSREF features simplify multi-device synchronization.
Clock distribution	Texas Instruments' LMK04832	Support for 7 JESD204 ADCs, DACs or logic devices (FPGA or ASIC) and a number of operating modes such as single PLL mode, dual PLL mode or clock distribution mode.
Transformer/Balun	Marki Microwave's BAL-0208SMG(1)	Small size, wide frequency coverage and good performance within required frequency band.

(1) See the *Third-Party Products Disclaimer* section.

The ADC12DJ3200QML-SP configuration and key parameters are given in 表 8-4. The calculations or sources for the various parameters are provided where applicable.

表 8-4. ADC12DJ3200QML-SP Configuration and Key Parameters

PARAMETER	CALCULATION	SETTING OR VALUE	UNITS
JMODE	—	1	—
DDC mode	From JMODE selection	N/A (dual-channel mode only)	—
ADC channels	From JMODE selection	1	—
Analog input used	INA± provides best performance in single-channel mode	INA±	—
Total SerDes lanes	From JMODE selection	16	Lanes
R (f_{BIT} / f_{CLK})	From JMODE selection	2	Gbps / GHz
SerDes line rate	$f_{LINERATE} = f_{CLK} * R$	6.4	Gbps
Links	From JMODE selection	2	Links
L (per link)	From JMODE selection	8	Lanes / Link
M (per link)	From JMODE selection	8	Converters / Link
F	From JMODE selection	8	Frames / Lane
S	From JMODE selection	5	Samples / Frame
K	ceil(17/F) ≤ K ≤ min(32, floor(1024/F))	8 (others allowed)	Frames / Multiframe
CLK± Frequency	$f_{CLK} = f_S / 2$ (for single-channel mode)	3.2	GHz
SYSREF frequency	$f_{SYSREF} = f_{LINERATE} / (10 * F * K * n)$	10 / n	MHz
Total clock jitter	$\tau_T = \text{sqrt}(\tau_{CLK}^2 + \tau_{AJ}^2)$	83	fs

8.2.2.1 RF Input Signal Path

Most RF sampling receivers will include a number of low-noise amplifiers (LNAs) or gain blocks after the antenna to increase the signal level of the desired signal. The use of appropriate band-limiting filters after the LNAs reduces receiver sensitivity loss due to blocking signals by rejecting unwanted frequencies. The final amplifier, which will drive the ADC12DJ3200QML-SP through the transformer, must be selected to provide high linearity (IMD3, SFDR) at the full-scale input power level of the ADC12DJ3200QML-SP plus the insertion loss of the transformer. The noise figure performance of the final driver amplifier is less important than its linearity as long as sufficient gain is provided by the previous gain stages. The maximum output power must be less than the absolute maximum input power of the ADC12DJ3200QML-SP in case of overdrive conditions. If the amplifier is capable of driving an output power larger than the ADC12DJ3200QML-SP can tolerate then an external clamping or limiting circuit must be implemented to protect the ADC12DJ3200QML-SP input. Overdrive conditions must be corrected quickly to prevent cumulative damage to the ADC12DJ3200QML-SP.

8.2.2.2 Calculating Values of AC-Coupling Capacitors

AC-coupling capacitors are used in the input CLK± and JESD204B output data pairs. The capacitor values must be large enough to address the lowest frequency signals of interest, but not so large as to cause excessively long startup biasing times, or unwanted parasitic inductance.

The minimum capacitor value can be calculated based on the lowest frequency signal that is transferred through the capacitor. Given a 50-Ω single-ended clock or data path impedance, good practice is to set the capacitor impedance to be <1 Ω at the lowest frequency of interest. This setting provides minimal impact on signal level at that frequency. For the CLK± path, the minimum-rated clock frequency is 800 MHz. Therefore, the minimum capacitor value can be calculated from:

$$Z_C = 1/\left(2 \times \pi \times f_{CLK} \times C\right) \tag{12}$$

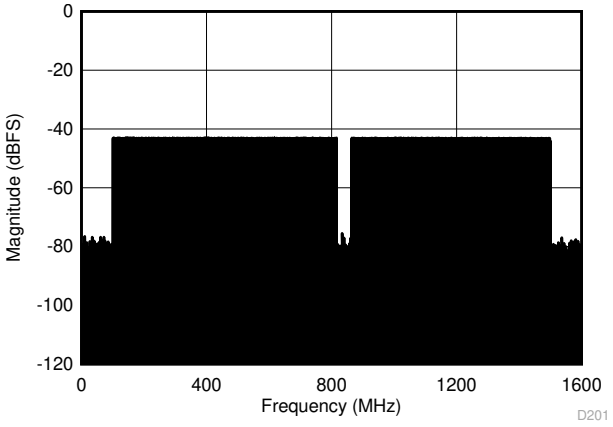
Setting Z_c = 1 Ω and rearranging gives:

$$C = 1/\left(2 \times \pi \times 800\ \text{MHz} \times 1\ \Omega\right) = 199\ \text{pF} \tag{13}$$

Therefore, a capacitance value of at least 199 pF is needed to provide the low-frequency response for the CLK± path. If the minimum clock frequency is higher than 800 MHz, this calculation can be revisited for that frequency. Similar calculations can be done for the JESD204B output data capacitors based on the minimum frequency in that interface. Capacitors must also be selected for good response at high frequencies (low inductance) and with dimensions that match the high-frequency signal traces they are connected to. Capacitors of the 0201 size are frequently well suited to these applications.

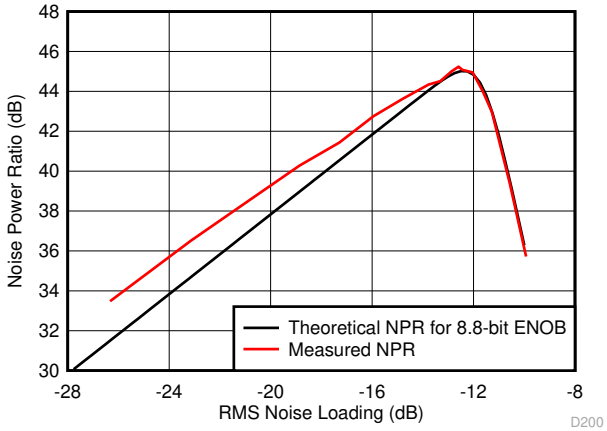
8.2.3 Application Curves

The ADC12DJ3200QML-SP can be used in a number of different operating modes to suit multiple applications. Single-tone and two-tone performance is shown in detail in the セクション 6 section. Noise-power ratio (NPR) is a performance metric that is often used to quantify performance of a wideband multi-channel receiver. These systems receive a large number of closely spaced signals that are uncorrelated. The summation of these uncorrelated signals forms a signal that looks like a normally (Gaussian) distributed noise source and NPR attempts to quantify performance for this type of signal. NPR measures the ratio of noise power in a notched band to the signal power in an equal size band. 図 8-2 shows an example NPR measurement in dual-channel mode. The input signal spans from 100 MHz to 1.5 GHz and the notch is 45 MHz wide centered at a frequency of 839.7 MHz. The input power is swept to find the optimal RMS noise loading which is the input power where the NPR is at a maximum. The peak NPR, occurring at the optimal input power loading, becomes the desired operating point for wideband multi-channel receivers with normally distributed input signals. An input power sweep for dual-channel mode is shown in 図 8-3 which shows the peak NPR of 45.2 dB occurring at the optimal loading of –12.6 dB relative to the peak (saturated) input power of the ADC. This peak NPR roughly corresponds to the performance of an 8.8-bit ADC, so the effective number of bits (ENOB) is 8.8 bits. Example measurements in single-channel mode are shown in 図 8-4 and 図 8-5. The signal generator output was limited to 1.5 GHz in order to achieve sufficient output power to saturate the ADC input for the single-channel mode measurement. The NPR calculation compensates for the limited signal bandwidth.



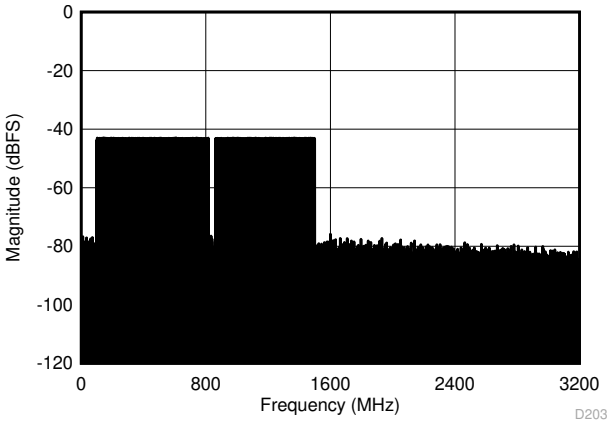
JMODE 3 , f_S = 3200 MSPS, signal band is 100 MHz to 1500 MHz, notch center frequency = 839.7 MHz, notch bandwidth = 45 MHz

図 8-2. Example NPR Measurement at Optimal Loading for ADC12DJ3200QML-SP in Dual-Channel Mode



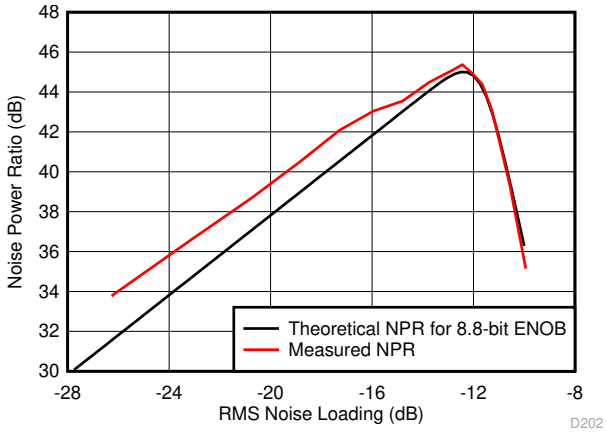
JMODE 3 , f_S = 3200 MSPS, signal band is 100 MHz to 1500 MHz, notch center frequency = 839.7 MHz, notch bandwidth = 45 MHz, peak NPR = 45.2 dB at noise loading of -12.6 dB

図 8-3. NPR vs Input RMS Noise Loading in Dual-Channel Mode



JMODE 1 , f_S = 6400 MSPS, signal band is 100 MHz to 1500 MHz, notch center frequency = 839.7 MHz, notch bandwidth = 45 MHz

図 8-4. Example NPR Measurement at Optimal Loading for ADC12DJ3200QML-SP in Single-Channel Mode



JMODE 1 , f_S = 6400 MSPS, signal band is 100 MHz to 1500 MHz, notch center frequency = 839.7 MHz, notch bandwidth = 45 MHz, peak NPR = 45.4 dB at noise loading of -12.4 dB

図 8-5. NPR vs Input RMS Noise Loading in Single-Channel Mode

8.3 Initialization Set Up

The device and JESD204 interface require a specific startup and alignment sequence. The general order of that sequence is listed in the following steps.

1. Power-up or reset the device.
2. Apply a stable device CLK signal at the desired frequency.
3. Program JESD_EN = 0 to stop the JESD204B state machine and allow setting changes.
4. Program CAL_EN = 0 to stop the calibration state machine and allow setting changes.
5. Program the desired JMODE.
6. Program the desired KM1 value. KM1 = K–1.
7. Program SYNC_SEL as needed. Choose SYNCSE or timestamp differential inputs.
8. Configure device calibration settings as desired. Select foreground or background calibration modes and offset calibration as needed.
9. Program CAL_EN = 1 to enable the calibration state machine.
10. Enable overrange via OVR_EN and adjust settings if desired.
11. Enable continuous SYSREF generation at the SYSREF source.
12. Verify that SYSREF meets setup and hold times relative to CLK± by either running automatic SYSREF calibration or using SYSREF windowing (see the SYSREF Capture for Multi-Device Synchronization and Deterministic Latency section for more information).
13. Program JESD_EN = 1 to re-start the JESD204B state machine and allow the link to restart.
14. The JESD204B interface operates in response to the applied SYNC signal from the receiver.
15. Program CAL_SOFT_TRIG = 0.
16. Program CAL_SOFT_TRIG = 1 to initiate a calibration.

Power Supply Recommendations

The device requires two different power-supply voltages. 1.9 V DC is required for the VA19 power bus and 1.1 V DC is required for the VA11 and VD11 power buses. The power-supply voltages must be low noise and provide the needed current to achieve rated device performance.

There are two recommended power supply architectures:

1. Step down from the system voltage using high-efficiency DC/DC switching converters followed by a second stage of low-noise regulation by a low drop-out linear regulator (LDO). The LDO provides switching noise reduction, reduces passive filtering requirements and improves voltage accuracy if placed locally at the ADC.
2. Directly step down from the system voltage to the final ADC supply voltages using high-efficiency DC/DC switching converters. This approach provides the best efficiency, but care must be taken to make sure switching noise is minimized to prevent degraded ADC performance. Additional passive filtering is required for best performance and any lossy series components may reduce the actual voltage at the ADC.

TI WEBENCH® Power Designer can be used to select and design the individual power supply elements needed: see the WEBENCH® Power Designer.

A recommended DC/DC switching regulator for the first stage is the TPS50601A-SP, but other similar devices can be used as well. Recommended LDOs for the second stage include TPS7H1101A-SP, TPS7A4501-SP and other similar devices.

For the switcher only approach, the ripple filter must be designed to provide sufficient filtering at the switching frequency of the DC-DC converter and it's harmonics. WEBENCH® reports the switching frequency when used to design the supply. Each application will have different tolerances for noise on the supply voltage so strict ripple requirements are not provided. 図 9-1 and 図 9-2 illustrate the two approaches.

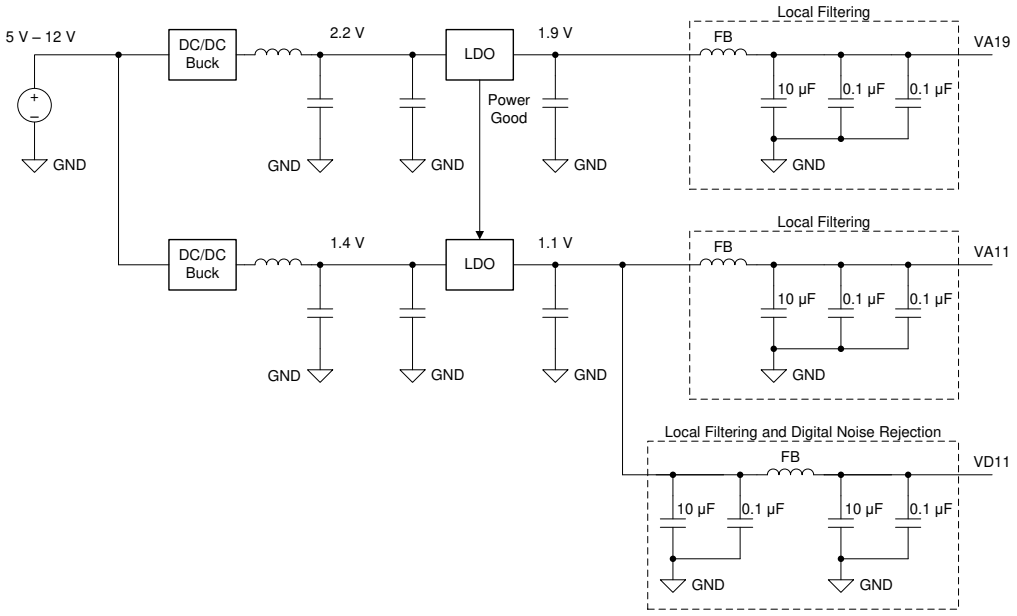


図 9-1. LDO Linear Regulator Example

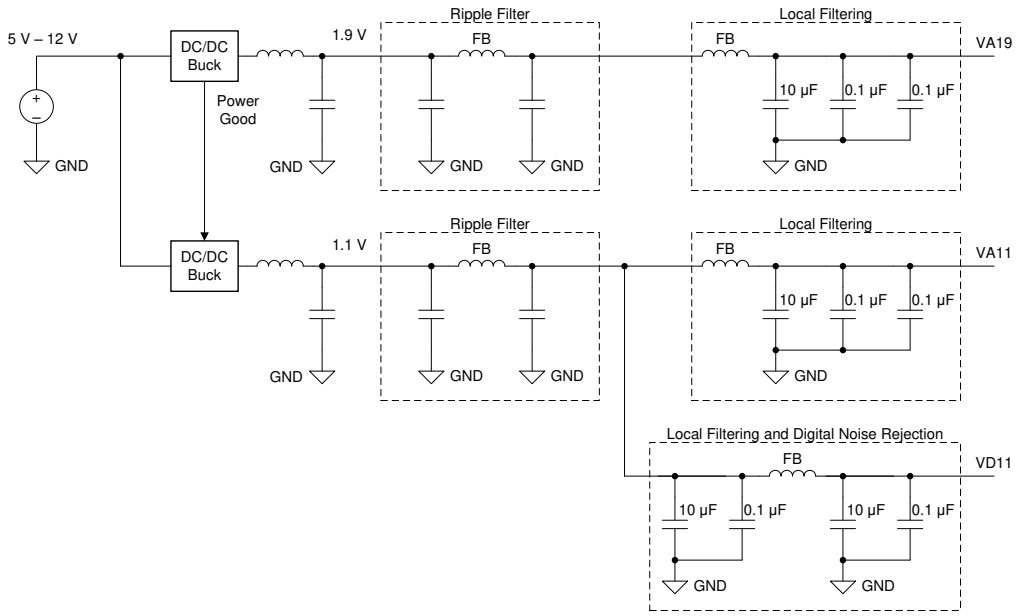


図 9-2. DC/DC Switching Regulator Example

9.1 Power Sequencing

The voltage regulators must be sequenced using the power-good outputs and enable inputs to make sure that the Vx11 regulator is enabled after the VA19 supply is good. Similarly, as soon as the VA19 supply drops out of regulation on power-down, the Vx11 regulator is disabled.

The general requirement for the ADC is that VA19 ≥ Vx11 during power-up, operation, and power-down.

TI also recommends that VA11 and VD11 are derived from a common 1.1-V regulator. This recommendation makes sure that all 1.1-V blocks are at the same voltage, and no sequencing problems exist between these supplies. Also use ferrite bead filters to isolate any noise on the VA11 and VD11 buses from affecting each other.

9 Layout

9.1 Layout Guidelines

There are many critical signals that require specific care during board design:

1. Analog input signals
2. CLK and SYSREF
3. JESD204B data outputs:
   a. DA[0:3] and DB[0:3] operating at up to 12.8 Gbit per second
   b. DA[4:7] and DB[4:7] operating at up to 6.4 Gbit per second
4. Power connections
5. Ground connections

The analog input signals, clock signals and JESD204B data outputs must be routed for excellent signal quality at high frequencies, but should also be routed for maximum isolation from each other. Use the following general practices:

1. Route using loosely coupled 100-Ω differential traces when possible. This routing minimizes impact of corners and length-matching serpentines on pair impedance.
2. Provide adequate pair-to-pair spacing to minimize crosstalk, especially with loosely coupled differential traces. Tightly coupled differential traces may be used to reduce self-radiated noise or to improve neighboring trace noise immunity when adequate spacing cannot be provided.
3. Provide adequate ground plane pour spacing to minimize coupling with the high-speed traces. Any ground plane pour must have sufficient via connections to the main ground plane of the board. Do not use floating or poorly connected ground pours.
4. Use smoothly radiused corners. Avoid 45- or 90-degree bends to reduce impedance mismatches.
5. Incorporate ground plane cutouts at component landing pads to avoid impedance discontinuities at these locations. Cut-out below the landing pads on one or multiple ground planes to achieve a pad size or stackup height that achieves the needed 50-Ω, single-ended impedance.
6. Avoid routing traces near irregularities in the reference ground planes. Irregularities include cuts in the ground plane or ground plane clearances associated with power and signal vias and through-hole component leads.
7. Provide symmetrically located ground tie vias adjacent to any high-speed signal vias at an appropriate spacing as determined by the maximum frequency the trace will transport ($<< \lambda_{MIN}/8$).
8. When high-speed signals must transition to another layer using vias, transition as far through the board as possible (top to bottom is best case) to minimize via stubs on top or bottom of the vias. If layer selection is not flexible, use back-drilled or buried, blind vias to eliminate stubs. Always place ground vias close to the signal vias when transitioning between layers to provide a nearby ground return path.

Pay particular attention to potential coupling between JESD204B data output routing and the analog input routing. Switching noise from the JESD204B outputs can couple into the analog input traces and show up as wideband noise due to the high input bandwidth fo the ADC. Ideally, route the JESD204B data outputs on a separate layer from the ADC input traces to avoid noise coupling (not shown in the *Layout Example* section). Tightly coupled traces can also be used to reduce noise coupling.

Impedance mismatch between the CLK± input pins and the clock source can result in reduced amplitude of the clock signal at the ADC CLK± pins due to signal reflections or standing waves. A reduction in the clock amplitude may degrade ADC noise performance, especially at high input frequencies. To avoid this, keep the clock source close to the ADC (as shown in the *Layout Example* section) or implement impedance matching at the ADC CLK± input pins.

In addition, TI recommends performing signal quality simulations of the critical signal traces before committing to fabrication. Insertion loss, return loss, and time domain reflectometry (TDR) evaluations should be done.

The power and ground connections for the device are also very important. These rules must be followed:

1. Provide low-resistance connection paths to all power and ground pins.
2. Use multiple power layers if necessary to access all pins.
3. Avoid narrow isolated paths that increase connection resistance.
4. Use a signal, ground, or power circuit board stackup to maximum coupling between the ground and power planes.

9.2 Layout Example

図 9-1 to 図 9-3 provide examples of the critical traces routed on the device evaluation module (EVM).

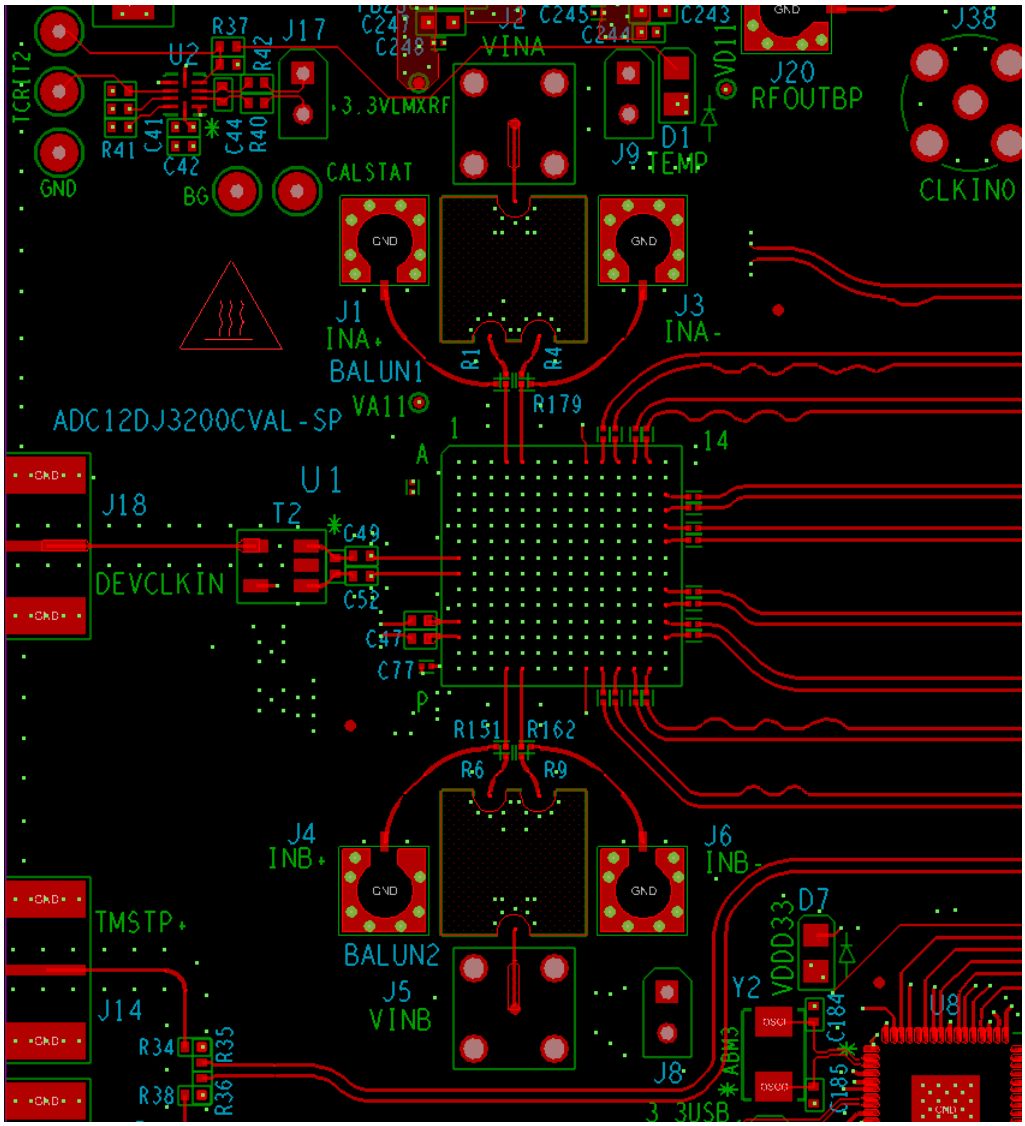


図 9-1. Top Layer Routing: Analog Inputs, CLK and SYSREF, DA0-3, DB0-3

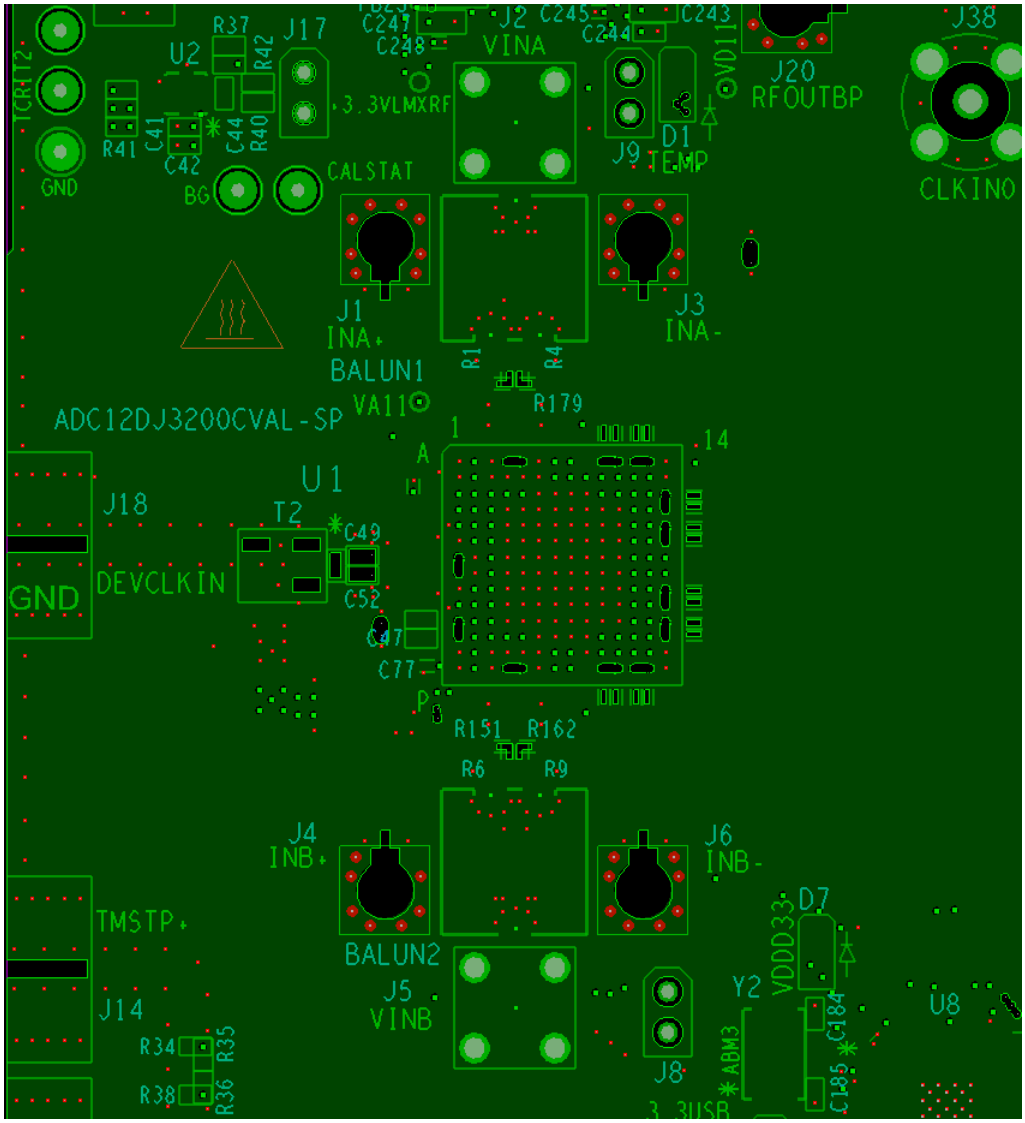


図 9-2. GND1 Cutouts to Optimize Impedance of Component Pads

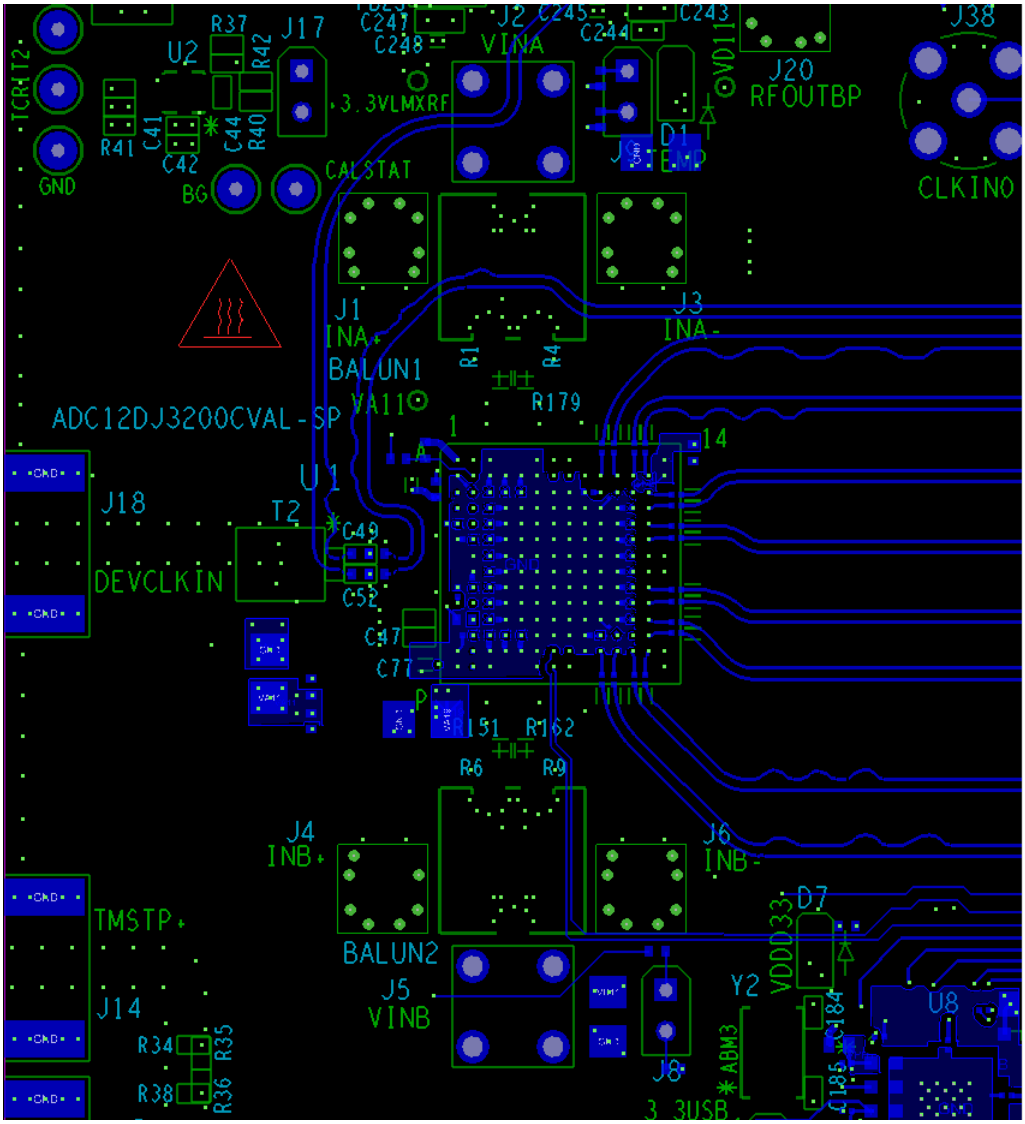


図 9-3. Bottom Layer Routing: Additional CLK Routing, DA4-7, DB4-7

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

- *WEBENCH® Power Designer*
- *Direct RF-Sampling Radar Receiver for L-, S-, C-, and X-Band Using ADC12DJ3200 Reference Design*
- *Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems*
- *Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers*

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

-
- Texas Instruments, *JESD204B multi-device synchronization: Breaking down the requirements Technical Brief*
- Texas Instruments, *LMX2615-SP Space Grade 40-MHz to 15-GHz Wideband Synthesizer With Phase Synchronization and JESD204B Support*
- Texas Instruments, *LMK04832 Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner With Dual Loop PLLs*
- Texas Instruments, *LMH5401-SP radiation hardened 6.5-GHz, low-noise, low-power, gain-configurable fully differential amplifier*
- Texas Instruments, *TMP461-SP Radiation Hardened Remote and Local Digital Temperature Sensor*
- Texas Instruments, *LMT01-SP radiation hardened 2-pin precision digital output temperature sensor*
- Texas Instruments, *MSP430FR5969-SP Radiation Hardened Mixed-Signal Microcontroller*
- Texas Instruments, *TPS50601A-SP Radiation Hardened 3-V to 7-V Input, 6-A Synchronous Buck Converter*
- Texas Instruments, *TPS7H1101A-SP 1.5-V to 7-V Input, 3-A, Radiation-Hardened LDO Regulator*
- Texas Instruments, *TPS7A4501-SP Low-Dropout Voltage Regulator*
- Texas Instruments, *ADC12DJ3200EVMCVAL Evaluation Module User's Guide*

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Community Resources

10.5 Trademarks

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Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962F1820901VXC	ACTIVE	CLGA	ZMX	196	119	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-55 to 125	F1820901VXC ADC12DJ32FM	Samples
5962F1820901VYF	ACTIVE	CCGA	NWE	196	119	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	-55 to 125	F1820901VYF ADC12DJ32FM	Samples
ADC12DJ3200NWE/EM	ACTIVE	CCGA	NWE	196	119	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	25 to 25	ADC12DJ32EM EVAL	Samples
ADC12DJ3200ZMX/EM	ACTIVE	CLGA	ZMX	196	119	RoHS-Exempt & Green	Call TI	N / A for Pkg Type	25 to 25	ADC12DJ32EM EVAL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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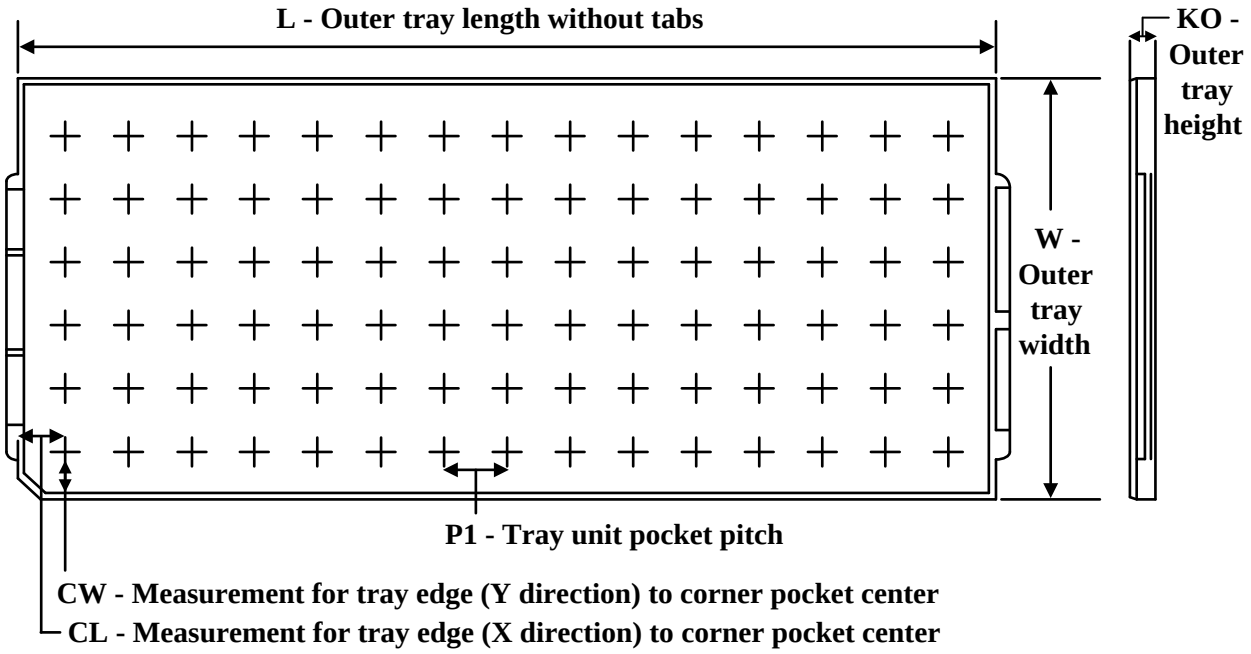
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

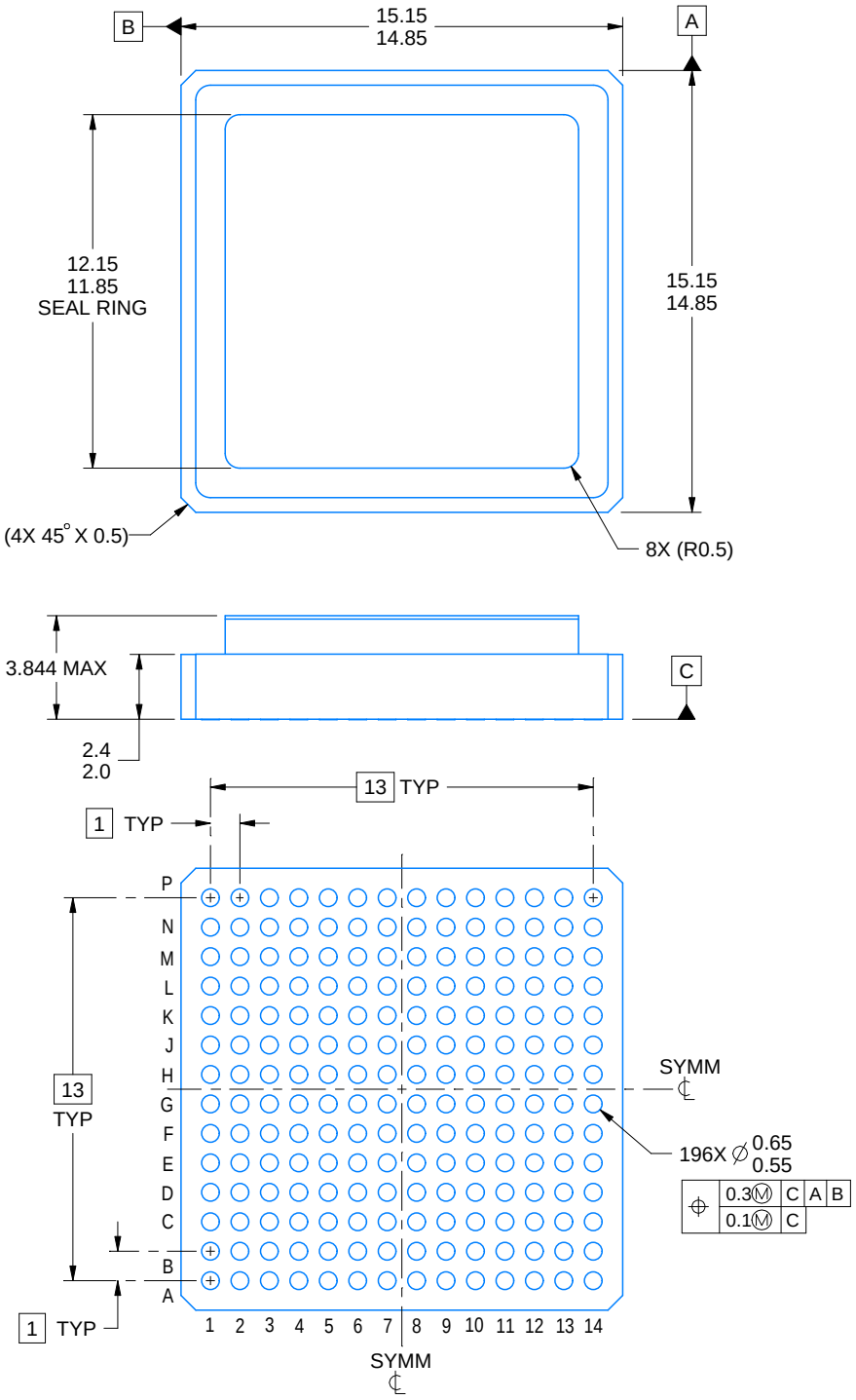
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC12DJ3200ZMX/EM	ZMX	CLGA	196	119	7 X 17	150	315	135.9	12190	18.1	12.7	12.9

PACKAGE OUTLINE

ZMX0196A

CLGA - 3.844 mm max height

Ceramic Land Grid Array



4222071/D 06/2018

NOTES:

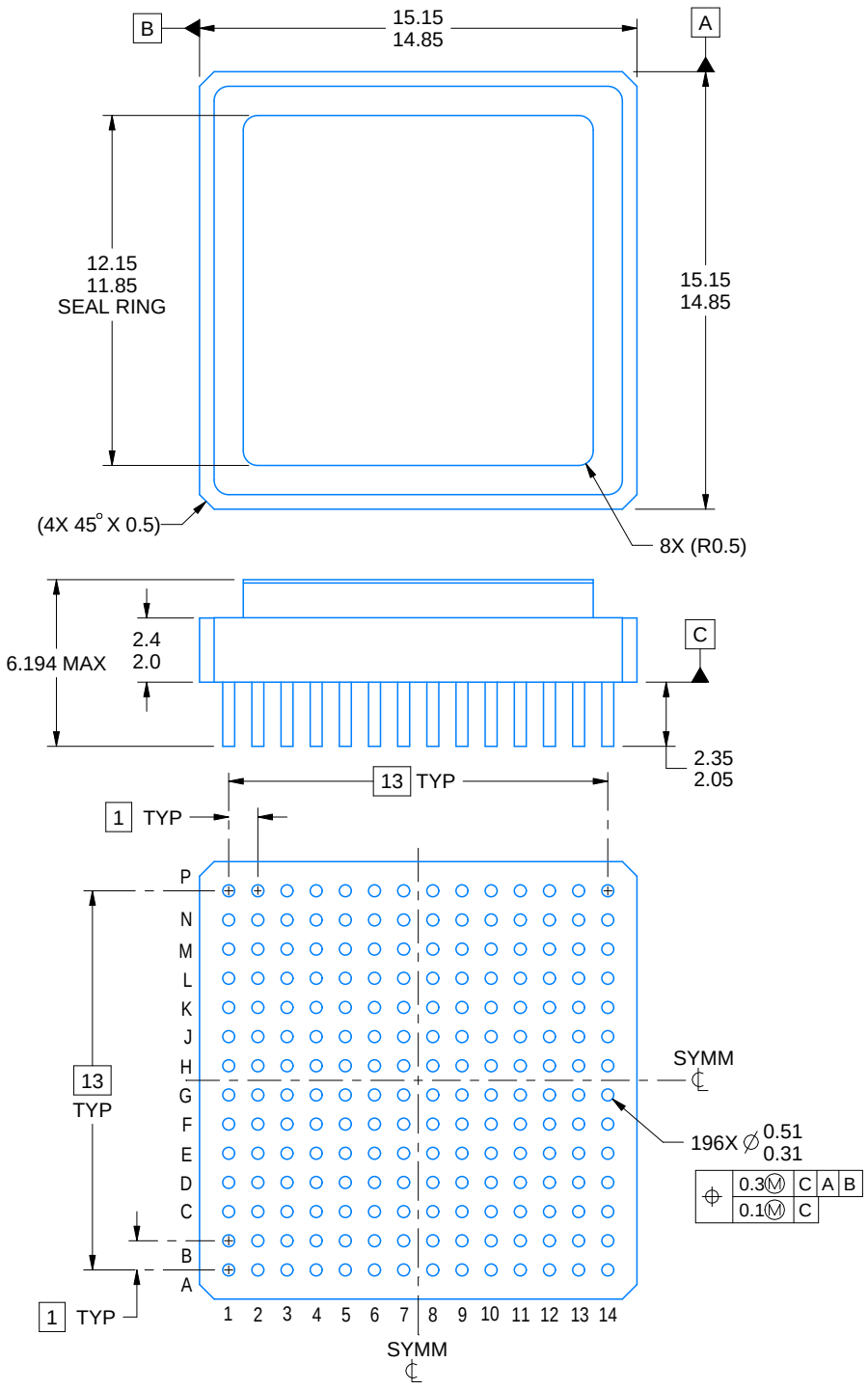
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

PACKAGE OUTLINE

NWE0196A

CCGA - 6.194 mm max height

CERAMIC COLUMN GRID ARRAY



4224655/B 12/2018

NOTES:

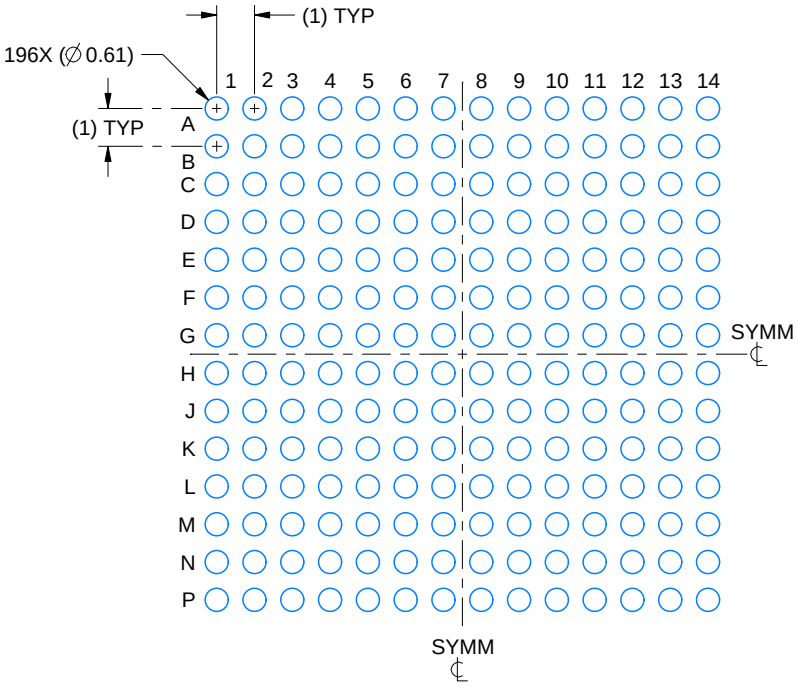
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

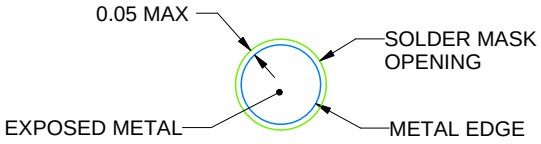
NWE0196A

CCGA - 6.194 mm max height

CERAMIC COLUMN GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 5X



NON-SOLDER MASK DEFINED

SOLDER MASK DETAIL
NOT TO SCALE

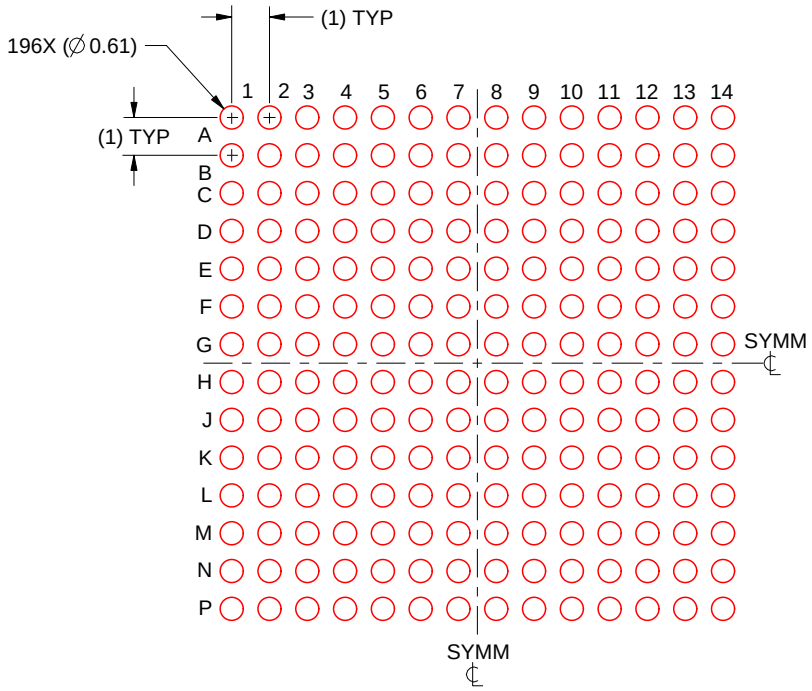
4224655/B 12/2018

EXAMPLE STENCIL DESIGN

NWE0196A

CCGA - 6.194 mm max height

CERAMIC COLUMN GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 5X

4224655/B 12/2018

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