ISO224 ±12Vのシングルエンド入力と ±4Vの差動出力を持つ強化絶縁アンプ

1 特長

- 高グレード(ISO224B)と低グレード(ISO224A)のバージョンで供給
- 工業用アプリケーションでの絶縁電圧測定用に最適化された、±12Vの入力電圧範囲
- 9kV ESDの過電圧入力クランプ
- ±4Vの差動出力電圧範囲(同相電圧VDD2/2)
- 低いDC誤差の動作(ISO224B)
  - 入力オフセット:25°Cで±5mV、最大値±15µV/°C
  - ゲイン誤差:25°Cで±0.3%、最大値±35ppm/°C
  - 非線形性:最大値±0.01%、標準値±0.1ppm/°C
- ハイサイドで4.5V～18Vの単一電源
- ローサイドで4.5V～5.5Vの動作
- 安全関連の認定
  - DIN VDE V 0884-11: 2017-01に準拠した強化絶縁耐圧: 7071V_{PEAK}
  - UL1577に準拠した絶縁耐圧: 5000V_{RMS} (1分間)
- 高いCMTI (ISO224B)：80kV/µs（標準値）

2 アプリケーション

- 次の用途における絶縁式アナログ信号収集
  - グリッド・オートメーション
  - 保護リレー
  - ファクトリ・オートメーション/制御
  - 鉄道輸送
  - モータ駆動
  - 電力分析

3 概要

ISO224は高精度の絶縁アンプで、磁気干渉に対して高い耐性のある絶縁膜により、入力側と出力側の回路が分離されています。この絶縁膜は最高5kV_{RMS}の強化ガルバニック絶縁の認定済みで、寿命が非常に長く、低消費電力です。絶縁電源と組み合わせて使用すると、システムの中で異なる同相電圧レベルで動作する部分が分離され、低電圧デバイスの損傷を防止します。

ISO224の入力は、工業用アプリケーションで広く使用されている±10V信号を正確に検出できるよう最適化されています。このデバイスは、ハイサイドの単一電源で動作します。この独自の機能により絶縁電源の設計が簡素化され、システムのコストを削減できます。内蔵のハイサイド電源電圧検出機能により、システム・レベルの診断が簡単になります。ISO224の出力は±4Vで、低コストのアナログ/デジタル・コンバータ(ADC)を使用できます。出力は差動構造なので、ノイズに高い耐性があります。

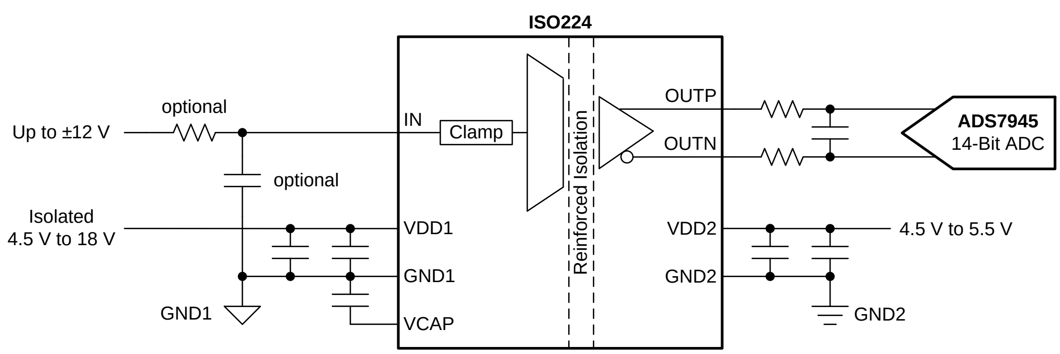
ISO224は拡張工業用温度範囲の-55°C～+125℃で完全に動作が規定されており、幅広の8ピンSOIC (DWV)パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ
ISO224	SOIC (8)	5.85mm×7.5mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



目次

4 改訂履歴

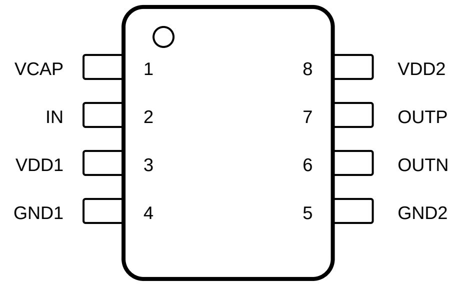
2018年6月発行のものから更新	**Page**
• ドキュメントのステータスを「事前情報」から「量産データ」に 変更	1

5 デバイス比較表

パラメータ	ISO224B	ISO224A
入力オフセット電圧、V_{OS}	±5mV (最大値)	±50mV (最大値)
入力オフセット・ドリフト係数、TCV_{OS}	±15µV/°C(最大値)	±60µV/°C(最大値)
入力換算ノイズ	3µV/√Hz(標準値)	4µV/√Hz(標準値)
ゲイン誤差、E_G	±0.3%(最大値)	±1%(最大値)
ゲイン誤差ドリフト係数、TCE_G	±35ppm/°C(最大値)	±60ppm/°C(最大値)
非線形性	±0.01% (最大値)	±0.02% (最大値)
出力帯域幅、BW	275kHz (標準値)	185kHz(標準値)
同相過渡耐性、CMTI	80kV/µs(標準値)	30kV/µs(標準値)
INからOUTP、OUTNへの信号遅延(50% - 50%)	2.2µs(標準値)	2.8µs (標準値)

6 Pin Configuration and Functions

DWV Package
8-Pin SOIC
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VCAP	—	Supply decoupling capacitor. Connect a 0.22-µF capacitor between this pin and the high-side analog ground.
2	IN	I	Analog input
3	VDD1	—	High-side power supply, 4.5 V to 18 V. See the *Power Supply Recommendations* section for decoupling recommendations.
4	GND1	—	High-side analog ground
5	GND2	—	Low-side analog ground
6	OUTN	O	Inverting analog output
7	OUTP	O	Noninverting analog output
8	VDD2	—	Low-side power supply, 4.5 V to 5.5 V. See the *Power Supply Recommendations* section for decoupling recommendations.

7 Specifications

7.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD1 to GND1	–0.3	26	V
	VDD2 to GND2	–0.3	6.5	
Input voltage	IN to GND1 (2)	–15	15	V
Input current	Continuous, at IN pin (3)	–10	10	mA
Output voltage	OUTP, OUTN	GND2 – 0.3	VDD2 + 0.3	V
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Exposure to absolute-maximum-rated condition for extended periods may increase input leakage current.
(3) Limit the input current at IN pin to prevent permanent damage to the device. The IN pin is internally protected by a voltage clamp. See 図 42 for a typical current versus voltage characteristic curve of the input clamp.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	IN pin only	±9000	V
			All pins except IN	±3000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	High-side power supply	VDD1 to GND1	4.5	5	18	V
	Low-side power supply	VDD2 to GND2	4.5	5	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Input voltage before clipping output (1)	IN to GND1		±13.8		V
V_{FSR}	Specified linear input full-scale voltage (1)	IN to GND1	–12		12	V
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–55	25	125	°C

(1) See the *Analog Input* section for more details.

7.4 Thermal Information

THERMAL METRIC (1)		ISO224x DWV (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	60.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	58.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings(1)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = 18 V, VDD2 = 5.5 V	194.9	mW
		VDD1 = VDD2 = 5.5 V	97.4	
P_{D1}	Maximum power dissipation (high-side supply)	VDD1 = 18 V	140.4	mW
		VDD1 = 5.5 V	42.9	
P_{D2}	Maximum power dissipation (low-side supply)	VDD2 = 5.5 V	54.5	mW

(1) See the *Electrical Characteristics* table for maximum supply current specifications.

7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 0.021	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage (bipolar or unipolar)	2121	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test; see 図 4	1500	V_{RMS}
		At DC voltage	2121	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7071	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8485	
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 12800\ V_{PK}$ (qualification)	8000	V_{PK}
q_{pd}	Apparent charge(4)	Method A, after input/output safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM} = 2545\ V_{PK}$, t_m = 10 s	≤ 5	pC
		Method A, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM} = 3394\ V_{PK}$, t_m = 10 s	≤ 5	
		Method B1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM} = 3977\ V_{PK}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.5\ V_{PP}$ at 1 MHz	~1	pF
R_{IO}	Insulation resistance, input to output(5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$ or 7071 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 6000\ V_{RMS}$, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

7.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
File number: 40040142	File number: E181974

7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 96.3°C/W, T_J = 150°C, T_A = 25°C, VDD1 = 18 V, VDD2 = 5.5 V, see 図 2			55	mA
		$R_{\theta JA}$ = 96.3°C/W, T_J = 150°C, T_A = 25°C, VDD1 = VDD2 = 5.5 V, see 図 2			236	
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 96.3°C/W, T_J = 150°C, T_A = 25°C, see 図 3			1298 (1)	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD1_{max} + I_S \times VDD2_{max}$, where $VDD1_{max}$ is the maximum high-side supply voltage and $VDD2_{max}$ is the maximum low-side supply voltage.

7.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –55°C to +125°C, VDD1 = 4.5 V to 18 V, VDD2 = 4.5 V to 5.5 V, V_{IN} = –12 V to 12 V, and R_{LOAD} = 10 kΩ; typical specifications are at T_A = 25°C, and VDD1 = VDD2 = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{OS}	Input offset voltage (1)	Initial, at T_A = 25°C, IN = GND1, ISO224B	–5	±1	5	mV
		Initial, at T_A = 25°C, IN = GND1, ISO224A	–50	±1	50	
TCV_{OS}	Input offset voltage drift (1)	ISO224B	–15	±3	15	µV/°C
		ISO224A	–60	±12	60	
C_{IN}	Input capacitance	IN to GND1		2		pF
R_{IN}	Input resistance	IN to GND1	1	1.25		MΩ
I_{IB}	Input bias current	IN = GND1		±15		nA
TCI_{IB}	Input bias current drift	IN = GND1		±30		pA/°C
e_n	Input-referred noise density	ISO224B		3		µV/√Hz
		ISO224A		4		

(1) The typical value includes one sigma statistical variation.

Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –55°C to +125°C, VDD1 = 4.5 V to 18 V, VDD2 = 4.5 V to 5.5 V, V_{IN} = –12 V to 12 V, and R_{LOAD} = 10 kΩ; typical specifications are at T_A = 25°C, and VDD1 = VDD2 = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUTS						
	Nominal gain	$(V_{OUTP} – V_{OUTN}) / V_{IN}$		1/3		V/V
E_G	Gain error[1]	Initial, at T_A = 25°C, ISO224B	–0.3%	±0.05%	0.3%	
		Initial, at T_A = 25°C, ISO224A	–1%	0.4%	1%	
TCE_G	Gain error drift[1]	ISO224B	–35	±10	35	ppm/°C
		ISO224A	–60	±20	60	
	Nonlinearity	ISO224B	–0.01%	±0.003%	0.01%	
		ISO224A	–0.02%	±0.003%	0.02%	
	Nonlinearity drift			±0.1		ppm/°C
THD	Total harmonic distortion	f_{IN} = 10 kHz		–84		dB
	Output noise	IN = GND1, f_{IN} = 0 Hz, BW = 10 kHz		300		μV_{RMS}
		IN = GND1, f_{IN} = 0 Hz, BW = 100 kHz		360		
PSRR	Power-supply rejection ratio[2]	vs VDD1, at DC		–107		dB
		vs VDD1, 100-mV and 10-kHz ripple		–101		
		vs VDD2, at DC		–71		
		vs VDD2, 100-mV and 10-kHz ripple		–56		
V_{OUT}	Output voltage	OUTP or OUTN to GND2	GND2 + 0.2		VDD2 – 0.2	V
V_{CMout}	Common-mode output voltage	$(V_{OUTP} + V_{OUTN}) / 2$	0.48 × VDD2	VDD2 / 2	0.52 × VDD2	V
$V_{FAILSAFE}$	Failsafe output voltage	VDD1 missing, OUTP and OUTN forced to GND2			GND2 + 0.1	V
I_{SC}	Output short-circuit current	On OUTP or OUTN to GND2		±18		mA
	Overload recovery time			5		µs
R_{OUT}	Output resistance	On OUTP or OUTN to GND2		< 0.5		Ω
C_{LOAD}	Capacitive load drive[3]	On OUTP or OUTN to GND2			100	pF
		OUTP to OUTN			50	
R_{LOAD}	Resistive load	On OUTP or OUTN		10		kΩ
BW	Small signal output bandwidth	ISO224B	220	275		kHz
		ISO224A	150	185		
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1 kV, ISO224B	55	80		kV/µs
		|GND1 – GND2| = 1 kV, ISO224A	15	30		
POWER SUPPLY						
I_{DD1}	High-side supply current			6.1	7.8	mA
I_{DD2}	Low-side supply current			7.8	9.9	mA

(2) This parameter is output referred.
(3) Use series resistor to decouple higher capacilive load.

7.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r, t_f	Rise time, fall time	ISO224B on OUTP, OUTN		1.5		µs
		ISO224A on OUTP, OUTN		2		µs
	IN to OUTP, OUTN signal delay (50% – 10%)	ISO224B, unfiltered output, see 図 1		1.5	2	µs
		ISO224A, unfiltered output, see 図 1		1.9	2.9	
	IN to OUTP, OUTN signal delay (50% – 50%)	ISO224B, unfiltered output, see 図 1		2.2	2.7	µs
		ISO224A, unfiltered output, see 図 1		2.8	3.8	
	IN to OUTP, OUTN signal delay (50% – 90%)	ISO224B, unfiltered output, see 図 1		3	3.5	µs
		ISO224A, unfiltered output, see 図 1		3.8	4.8	
t_{AS}	Analog startup time	VDD1 step to 4.5 V with VDD2 ≥ 4.5 V, to OUTP, OUTN valid, 0.1% settling		250		µs

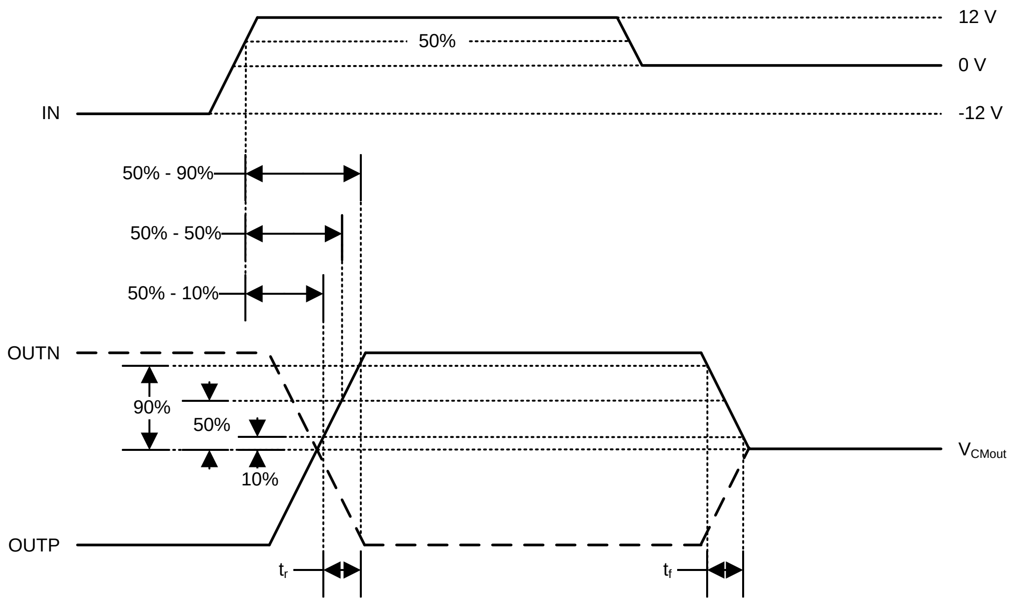


図 1. Delay Time Test Waveforms

7.11 Insulation Characteristics Curves

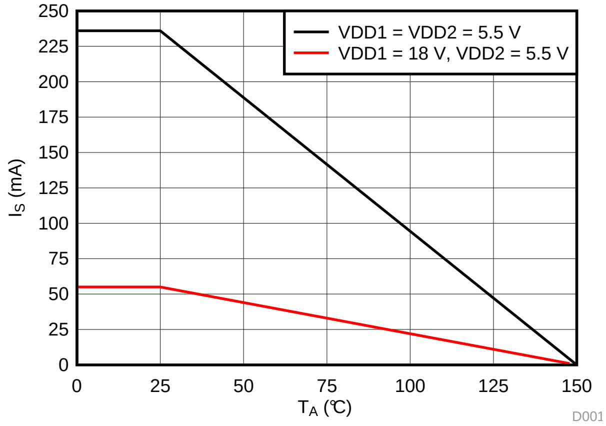


図 2. Thermal Derating Curve for Safety-Limiting Current per VDE

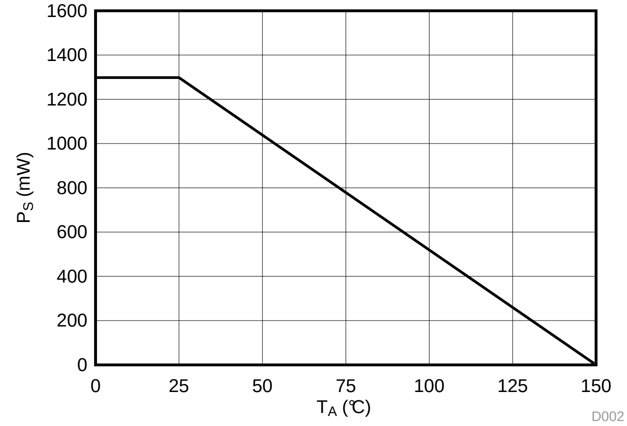
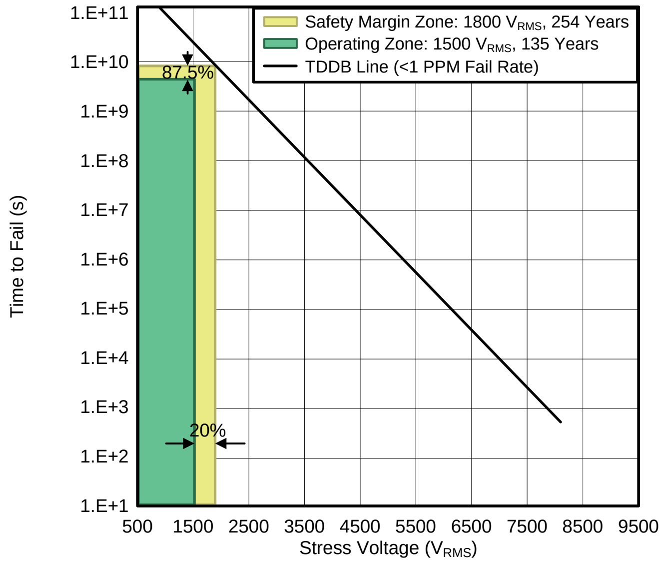


図 3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1500 V_{RMS}, operating lifetime = 135 years

図 4. Reinforced Isolation Capacitor Lifetime Projection

7.12 Typical Characteristics

at T_A = 25°C, VDD1 = VDD2 = 5 V, and VINP = –12 V to 12 V, unless otherwise noted.

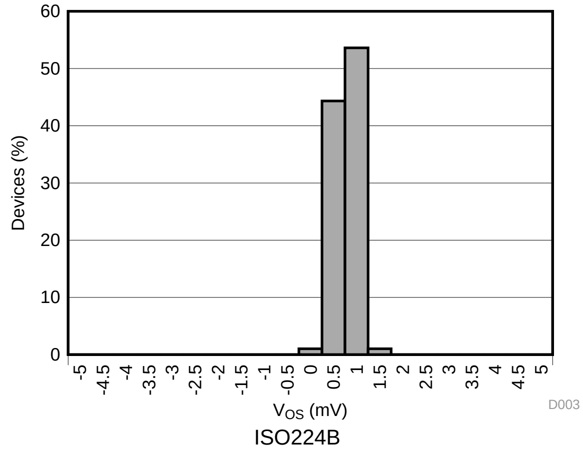


図 5. Input Offset Voltage Histogram

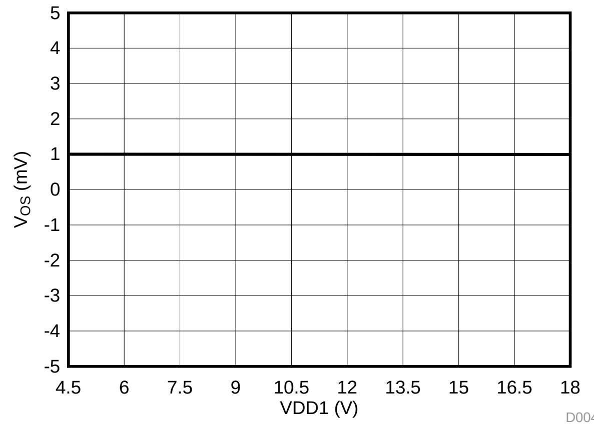


図 6. Input Offset Voltage vs High-Side Supply Voltage

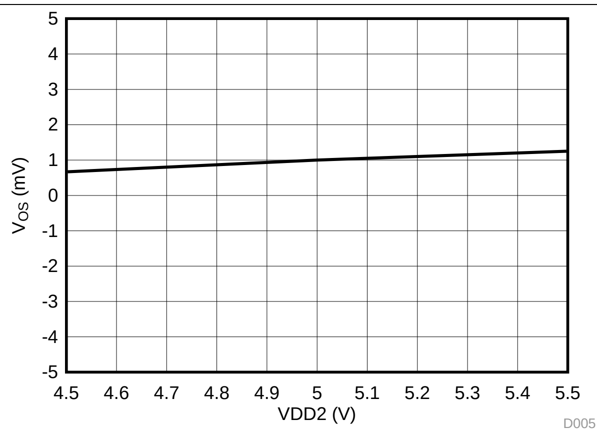


図 7. Input Offset Voltage vs Low-Side Supply Voltage

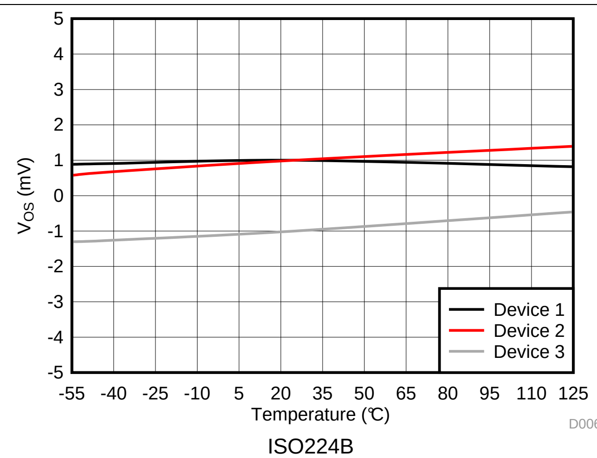


図 8. Input Offset Voltage vs Temperature

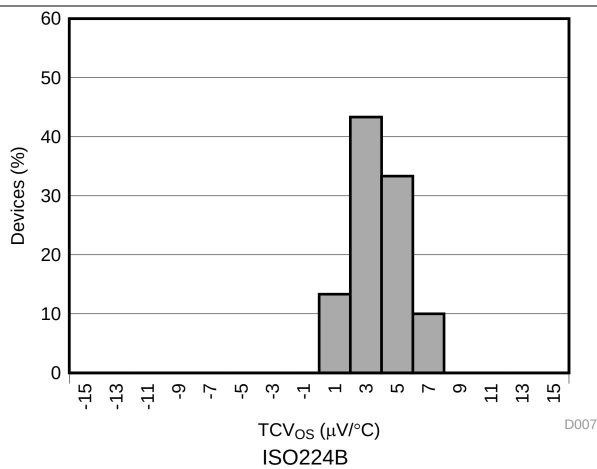


図 9. Input Offset Drift Histogram

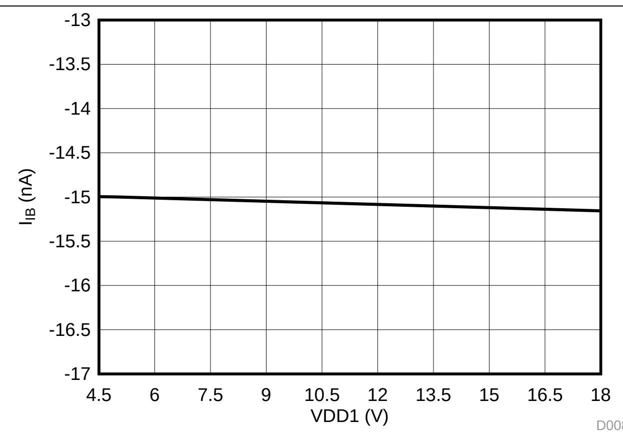


図 10. Input Bias Current vs High-Side Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, VDD1 = VDD2 = 5 V, and VINP = –12 V to 12 V, unless otherwise noted.

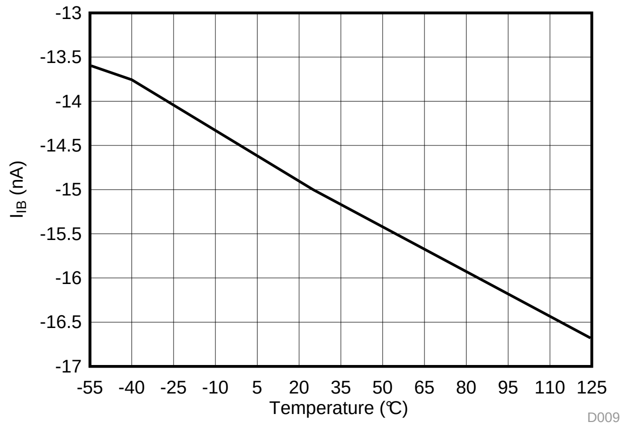
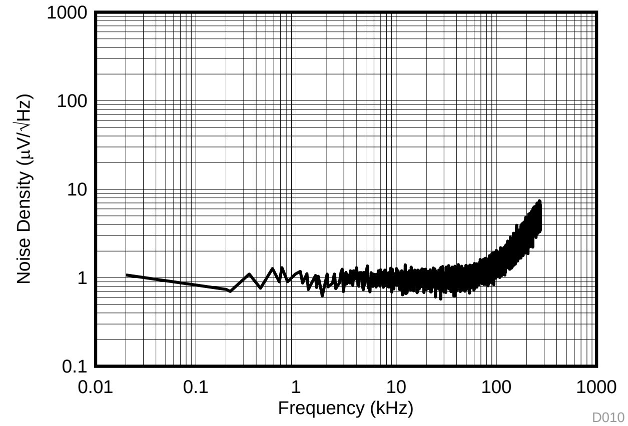
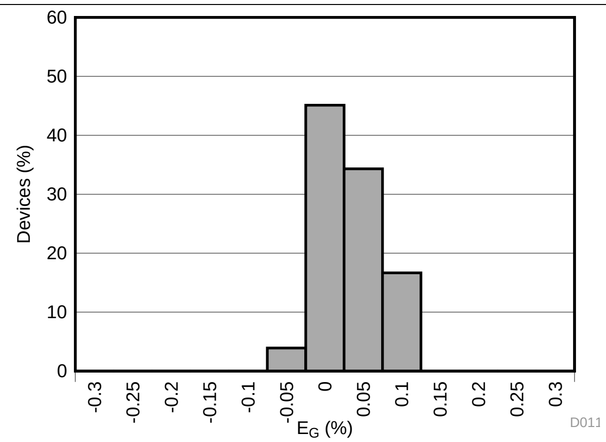


図 11. Input Bias Current vs Temperature



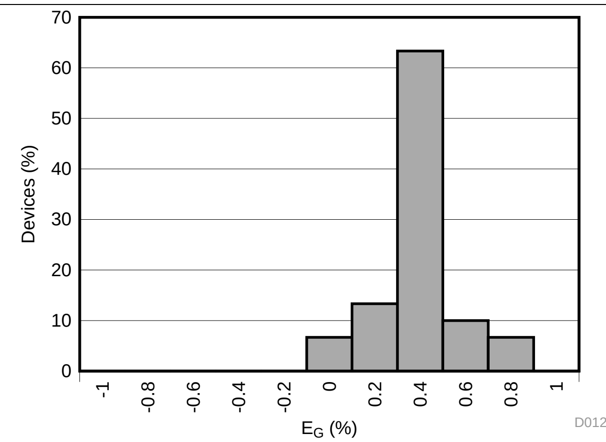
ISO224B

図 12. Input-Referred Noise Density vs Frequency



ISO224B

図 13. Gain Error Histogram



ISO224A

図 14. Gain Error Histogram

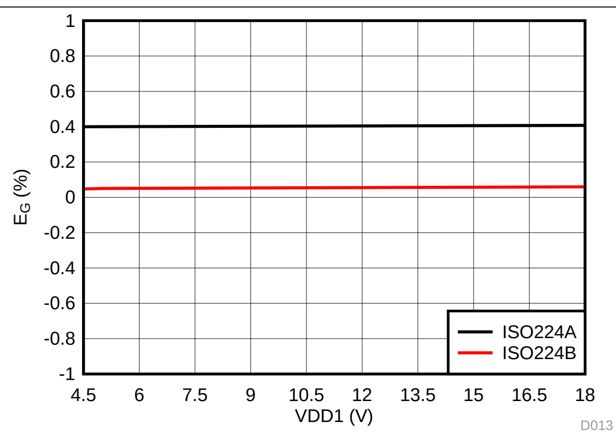


図 15. Gain Error vs High-Side Supply Voltage

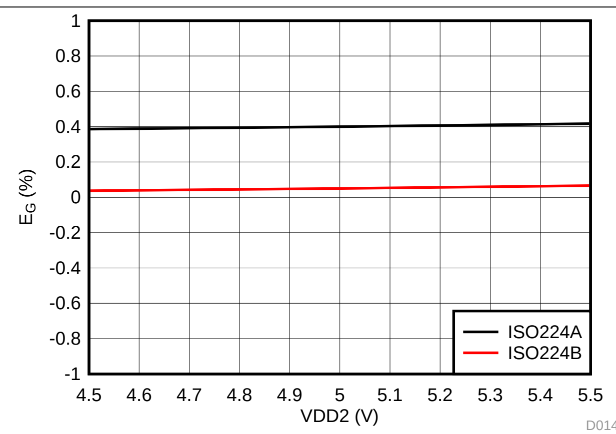


図 16. Gain Error vs Low-Side Supply Voltage

Typical Characteristics (continued)

at T_A = 25°C, VDD1 = VDD2 = 5 V, and VINP = –12 V to 12 V, unless otherwise noted.

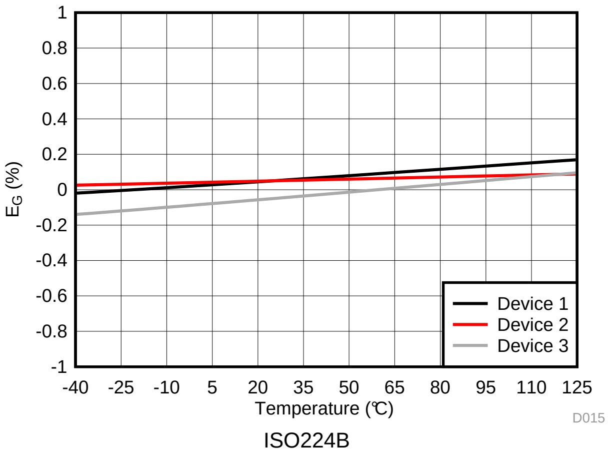


図 17. Gain Error vs Temperature

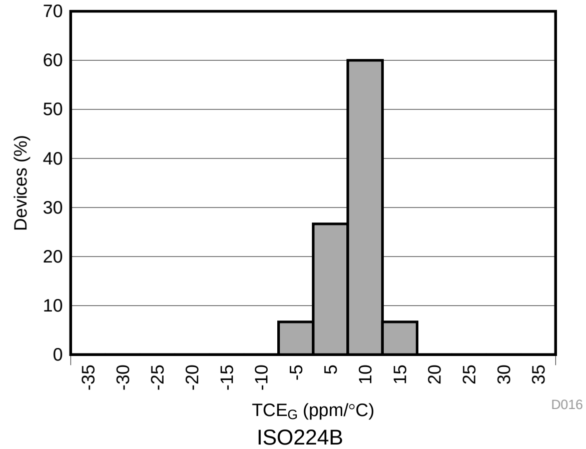


図 18. Gain Error Drift Histogram

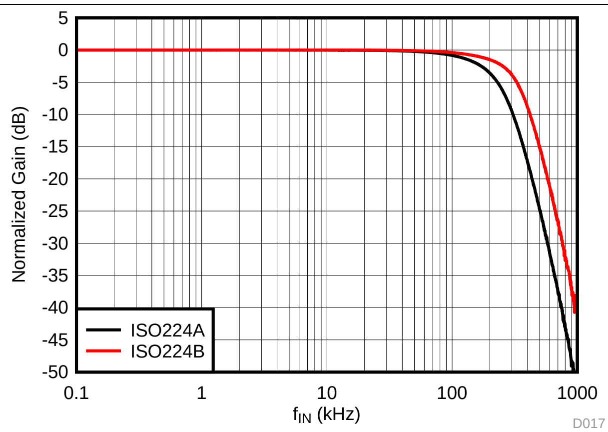


図 19. Normalized Gain vs Input Frequency

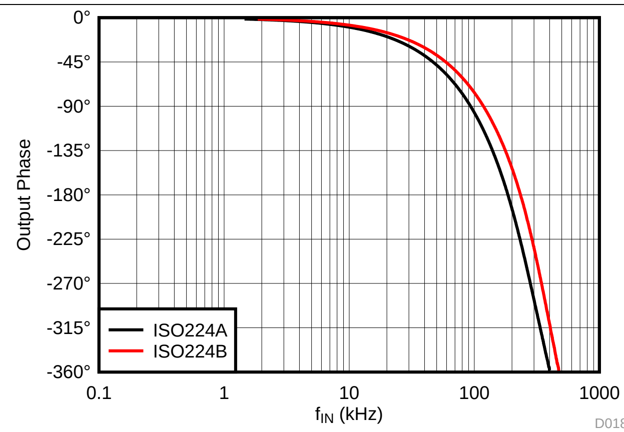


図 20. Output Phase vs Input Frequency

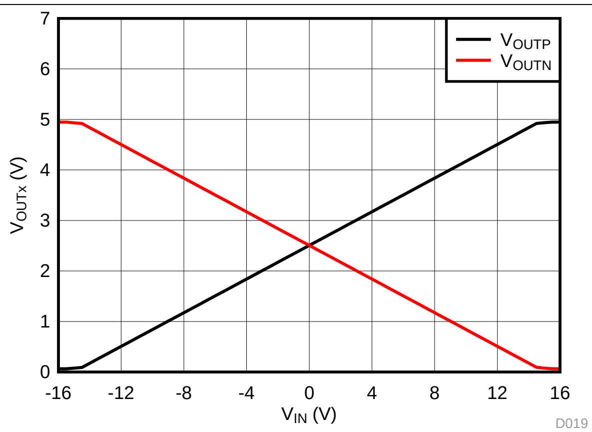


図 21. Output Voltage vs Input Voltage

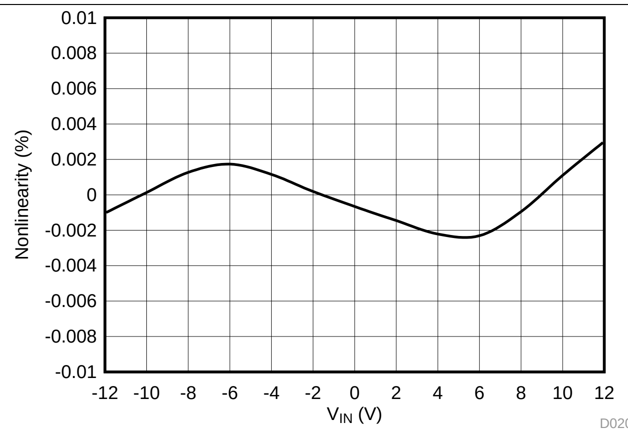


図 22. Nonlinearity vs Input Voltage

Typical Characteristics (continued)

at T_A = 25°C, VDD1 = VDD2 = 5 V, and VINP = –12 V to 12 V, unless otherwise noted.

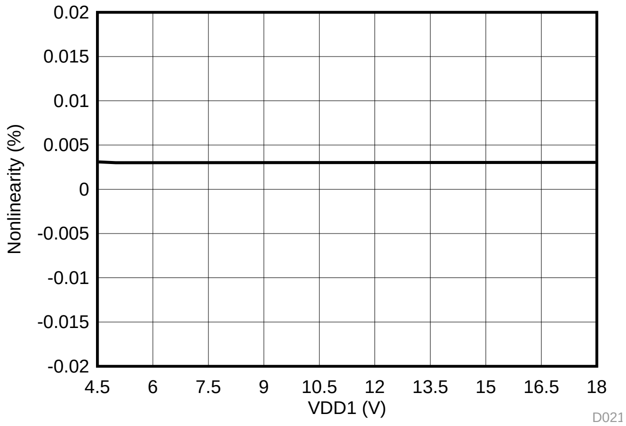


図 23. Nonlinearity vs High-Side Supply Voltage

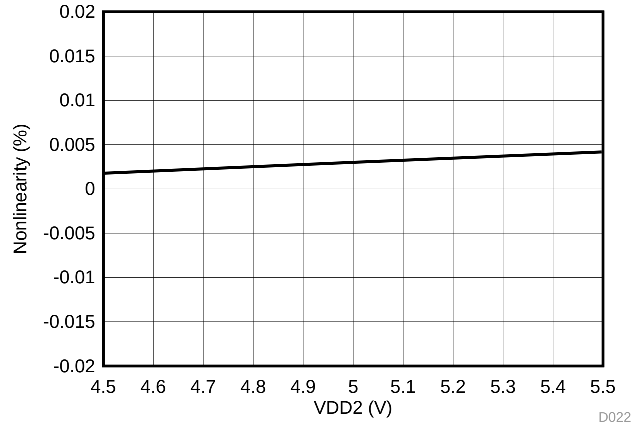


図 24. Nonlinearity vs Low-Side Supply Voltage

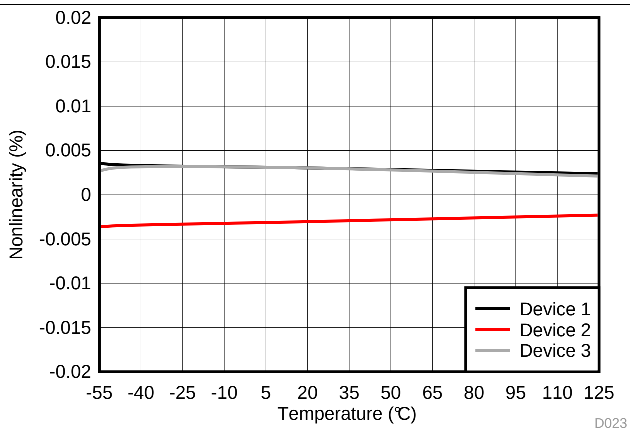


図 25. Nonlinearity vs Temperature

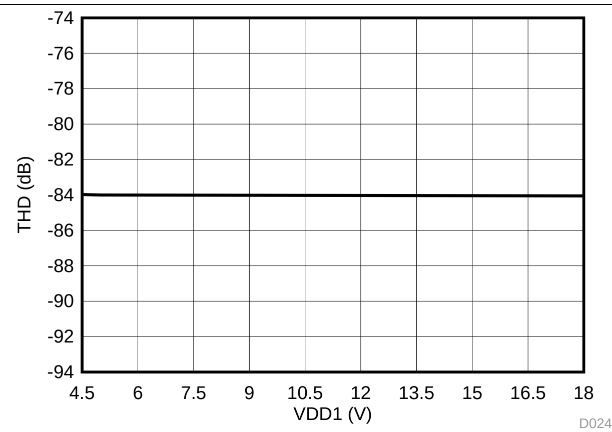


図 26. Total Harmonic Distortion vs High-Side Supply Voltage

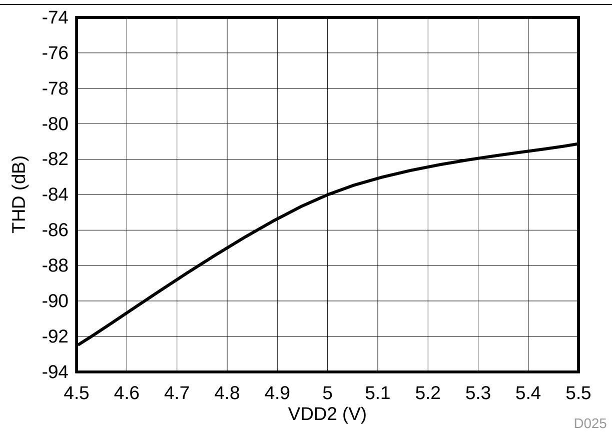


図 27. Total Harmonic Distortion vs Low-Side Supply Voltage

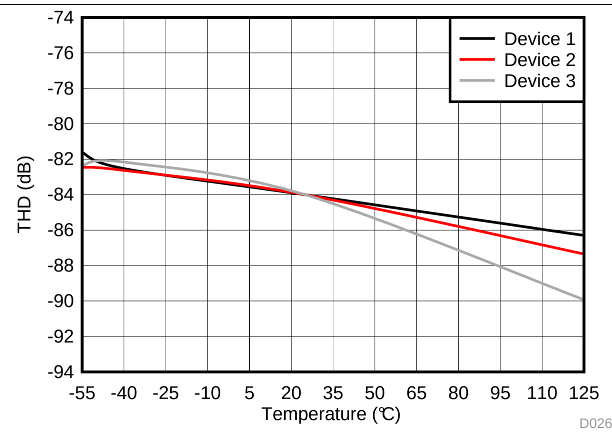


図 28. Total Harmonic Distortion vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, VDD1 = VDD2 = 5 V, and VINP = –12 V to 12 V, unless otherwise noted.

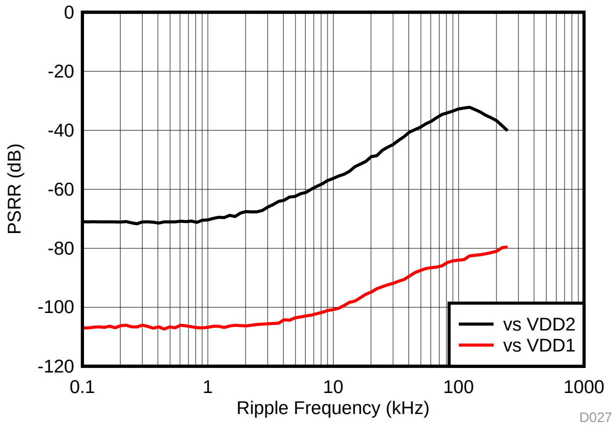


図 29. Power-Supply Rejection Ratio vs Ripple Frequency

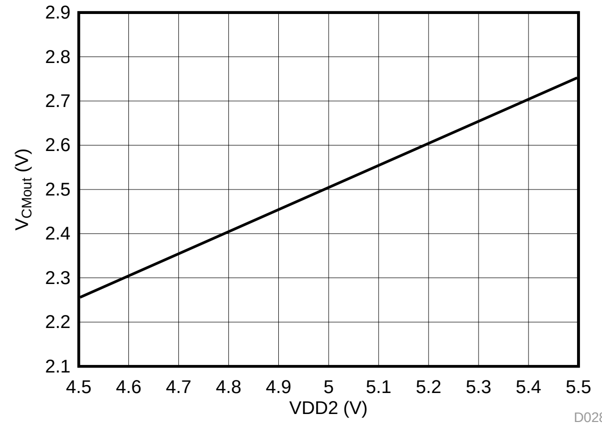


図 30. Output Common-Mode Voltage vs Low-Side Supply Voltage

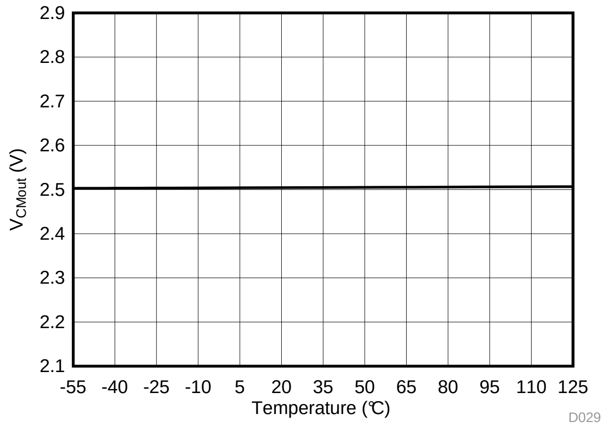


図 31. Output Common-Mode Voltage vs Temperature

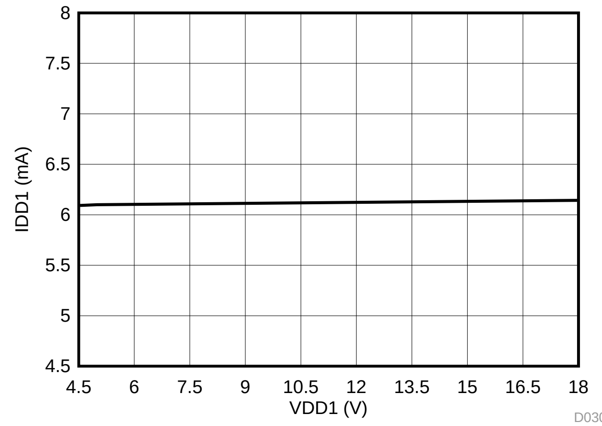


図 32. High-Side Supply Current vs High-Side Supply Voltage

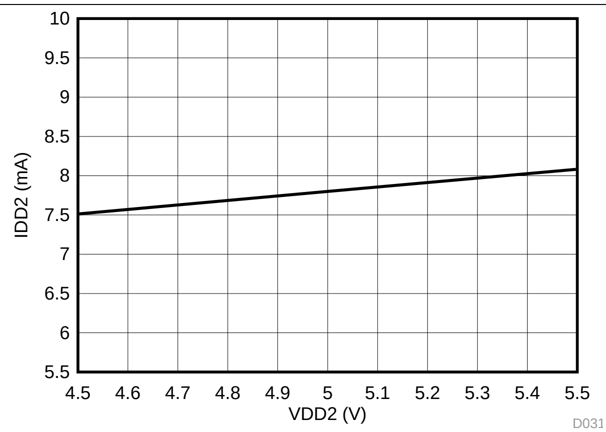


図 33. Low-Side Supply Current vs Low-Side Supply Voltage

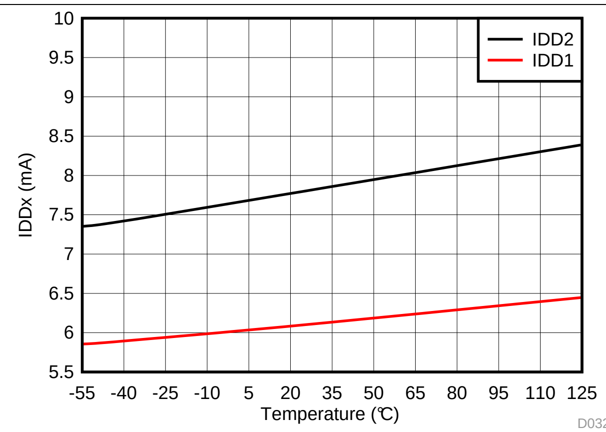


図 34. Supply Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, VDD1 = VDD2 = 5 V, and VINP = –12 V to 12 V, unless otherwise noted.

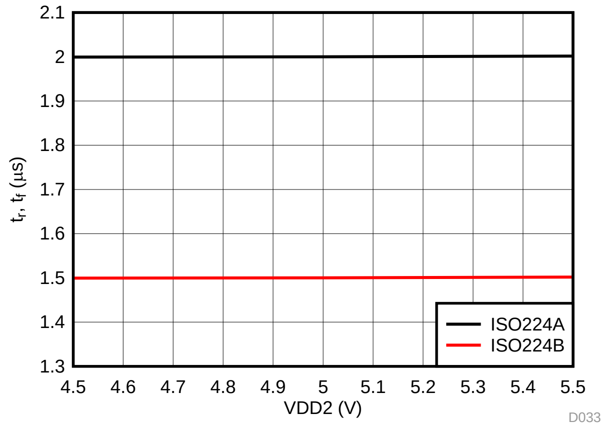


図 35. Output Rise and Fall Time vs Low-Side Supply Voltage

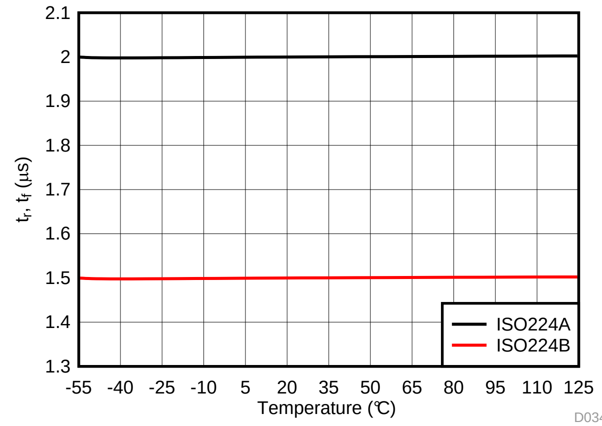


図 36. Output Rise and Fall Time vs Temperature

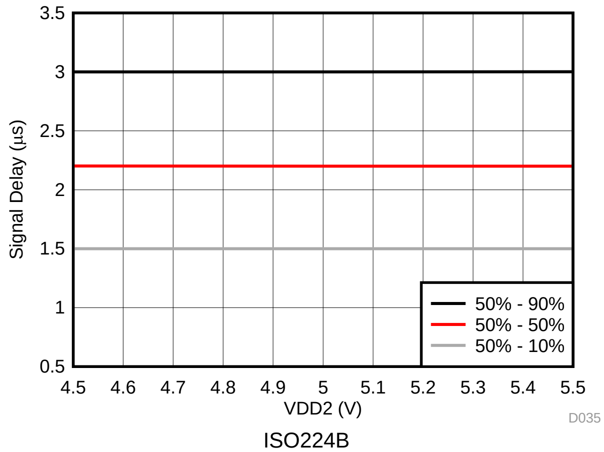


図 37. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

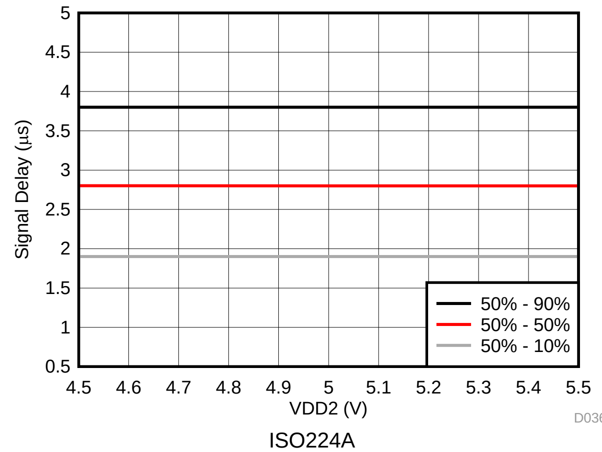


図 38. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

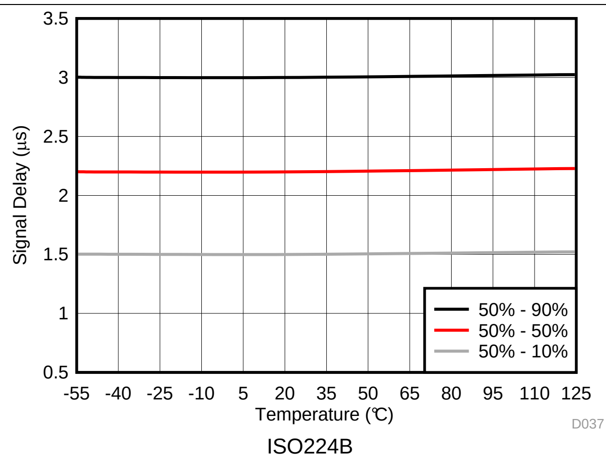


図 39. V_{IN} to V_{OUT} Signal Delay vs Temperature

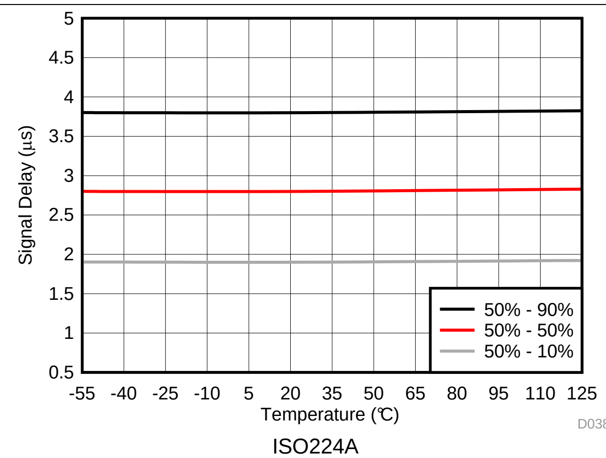


図 40. V_{IN} to V_{OUT} Signal Delay vs Temperature

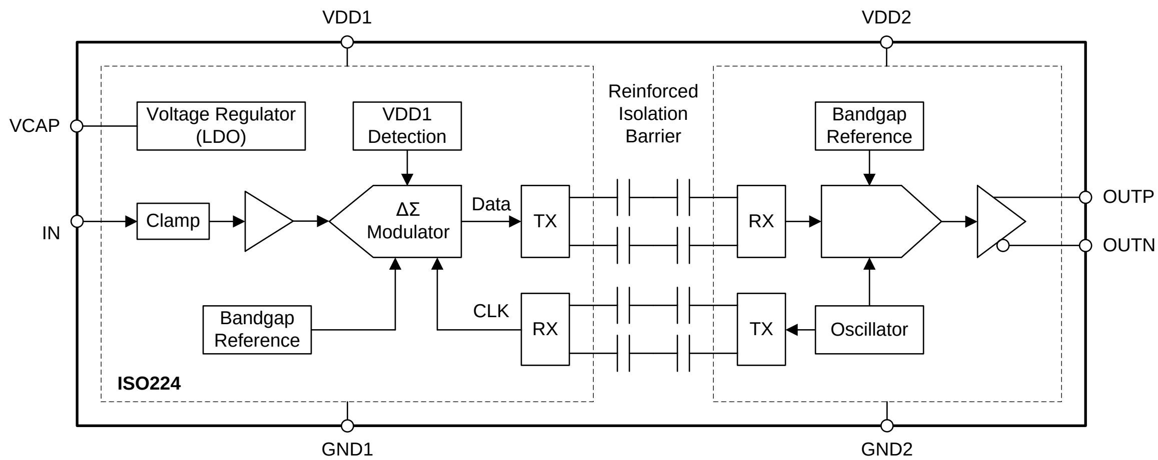
8 Detailed Description

8.1 Overview

The ISO224 is a precision, isolated amplifier with a high input impedance and wide input voltage range suitable for wide range of industrial applications. The input stage of the device drives a delta-sigma (ΔΣ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called *TX* in the *Functional Block Diagram* section) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a digital-to-analog conversion stage on the low-side and presented as a differential analog output.

The SiO_2-based, double-capacitive isolation barrier supports a high level of magnetic field immunity, as described in *ISO72x Digital Isolator Magnetic-Field Immunity*. The digital modulation used in the ISO224 and the isolation barrier characteristics result in high reliability and high common-mode transient immunity.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Analog Input

The input stage of the ISO224 feeds a switched capacitor, feed-forward ΔΣ modulator. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Isolation Channel Signal Transmission* section. The high-impedance and low bias-current input of the ISO224 makes the device suitable for isolated voltage sensing applications.

図 41 visualizes the difference in the transfer function of the ISO224 depending on the input signal V_{IN}, as specified in the *Recommended Operating Conditions* table. With the input voltage within the specified full-scale range V_{FSR}, the output of the device changes in a linear way with small error as specified by the nonlinearity parameter in the *Electrical Characteristics* table. If the input signal exceeds the V_{FSR} range, the nonlinearity of the output signals increases and the amplitude clips at V_{IN} = $V_{CLIPPING}$.

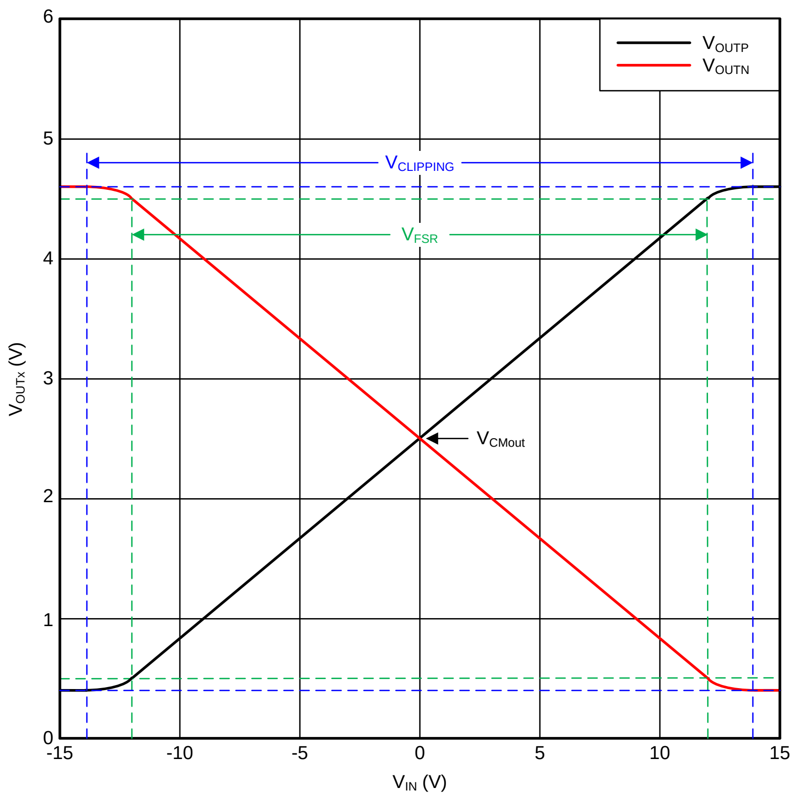


図 41. Transfer Function of the ISO224

There are two restrictions on the analog input signal at the IN pin. First, if the input voltage V_{IN} exceeds the range of –15 V to 15 V, the current must be limited to 10 mA to prevent damage to the input clamp, see the *Input Clamp Protection Circuit* section for further information. In addition, the linearity and noise performance of the ISO224 are ensured only when the analog input voltage remains within the specified linear full-scale range (V_{FSR}).

Feature Description (continued)

8.3.2 Input Clamp Protection Circuit

As illustrated in the *Functional Block Diagram*, the ISO224 features an internal clamp protection circuit on the analog input IN. Using external protection circuits is recommended as a secondary protection scheme to protect the device against surges, ESD events, and electrical fast transient (EFT) conditions.

図 42 shows a typical current versus voltage characteristic curve for the input clamp. Limit either the voltage V_{IN} at the input pin IN to the voltage range as defined in the *Recommended Operating Conditions* table or the input current to the limits as defined in the *Absolute Maximum Ratings* table.

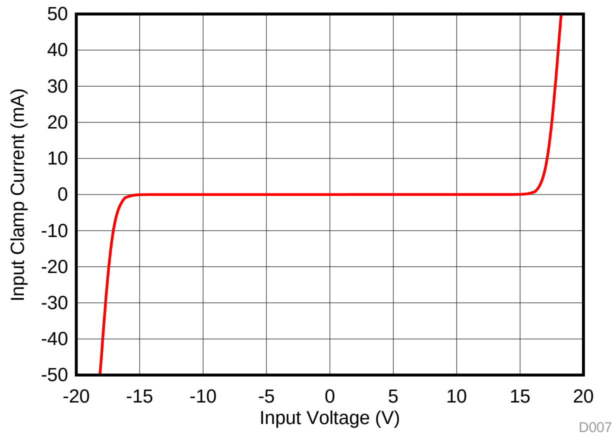


図 42. I-V Curve of the Input Clamp Protection Circuit

図 43 shows a simple method to limit the input current with an external series resistor that is also used as part of the input low-pass filter.

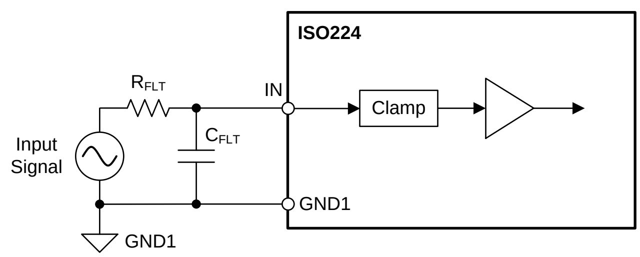


図 43. Series Resistor-Based Input Current Limitation on the Analog Inputs of ISO224

The input overvoltage protection clamp on the ISO224 is intended to control transient excursions on the input pins. Leaving the device in a state such that the clamp circuit is activated for extended periods of time in normal or power-down mode is not recommended because this fault condition can degrade device performance and reliability.

Feature Description (continued)

8.3.3 Isolation Channel Signal Transmission

The ISO224 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. As shown in 図 44, the transmitter modulates the bitstream at TX IN with an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent the digital *zero*. The nominal frequency of the carrier used inside the ISO224 is 480 MHz.

The receiver demodulates the signal after advanced signal conditioning and produces the output. The ISO224 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

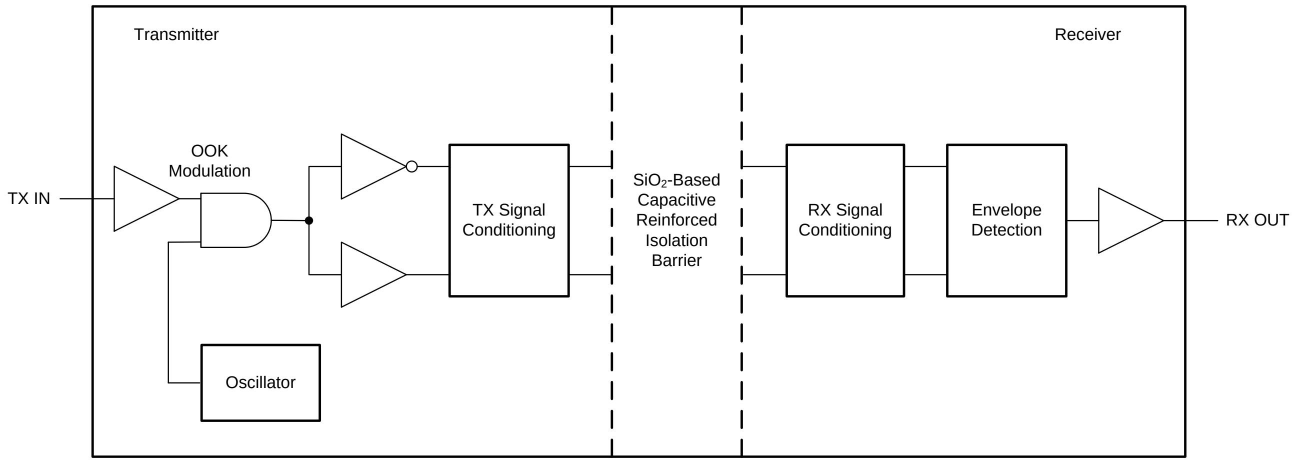


図 44. Block Diagram of an Isolation Channel

図 45 shows the concept of the OOK scheme.

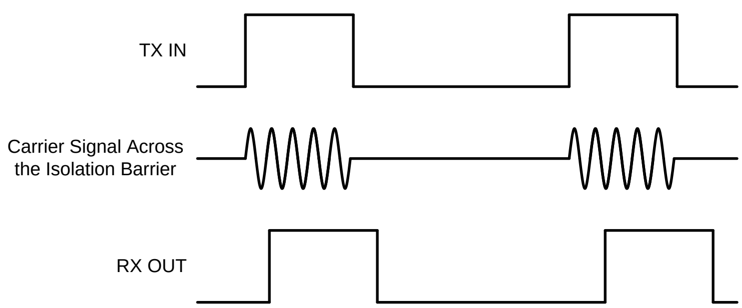


図 45. OOK-Based Modulation Scheme

Feature Description (continued)

8.3.4 Fail-Safe Output

The ISO224 offers a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active when the high-side power supply VDD1 of the device is missing, independent of the input signal at the IN pin. 図 46 shows that in that case both outputs, OUTP and OUTN, of the device are actively driven close to GND2 (see the $V_{FAILSAFE}$ specification in the *Electrical Characteristics* table for details). For easy visualization, an example with the input signal V_{IN} = 0 V is shown for the valid VDD1 range of 4.5 V to 5.5 V.

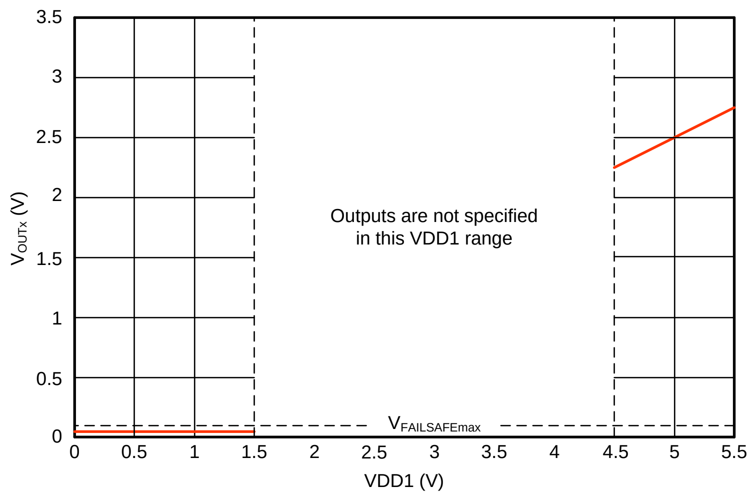


図 46. ISO224 Failsafe Output Behavior With V_{IN} = 0 V

The *ISO224 Fail-Safe Output Feature* application report describes an example of a comparator-based circuit that detects the missing high-side supply in a system.

8.4 Device Functional Modes

The ISO224 is operational when the power supplies VDD1 and VDD2 are applied, as specified in the *Recommended Operating Conditions* table.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO224 enables high-precision measurement of ±10-V signals that are used in a harsh environment in a wide range of industrial applications. The high input resistance of the device simplifies the connection of its input to different sensors or other signal sources. The very low nonlinearity, AC and DC errors, and temperature drift make the ISO224 a robust, high-performance, isolated amplifier for applications where high voltage isolation is required. The differential output with a full-scale voltage of 4 V offers high immunity to noise and allows connection to a wide range of analog-to-digital converters (ADCs) powered on a 5-V nominal supply.

9.2 Typical Application

Isolated amplifiers are often used for data acquisition in industrial applications to safely separate the low-voltage portion of the system from the high common-mode voltage input of the system. The input structure of the ISO224 is optimized for isolated voltage sensing in this kind of application.

図 47 shows a typical operation of the device for voltage sensing as used in power line monitoring systems. The phase voltage amplitude is reduced with a resistive divider to match the input voltage range of the ISO224. The high input voltage range and the high common-mode transient immunity of the device ensure reliable and accurate operation even in high-noise environments.

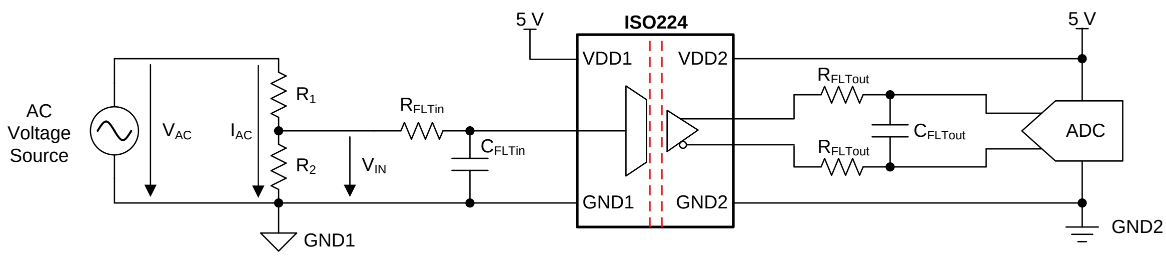


図 47. Using the ISO224 for AC Voltage Sensing

9.2.1 Design Requirements

表 1 summarizes the typical design requirements for an AC power line voltage sensing application.

表 1. Design Requirements

PARAMETER	VALUE
AC voltage range, V_{AC}	50 V to 750 V
Bandwidth	600 Hz (minimum)
Current through the resistive divider, I_{AC}	1 mA (maximum)

9.2.2 Detailed Design Procedure

The high-side power supply (VDD1) for the device is generated with a suitable isolated power source. An example of such a circuit is provided in the *Power Supply Recommendations* section.

The floating ground reference (GND1) is derived from one of the ends of the shunt resistor that is connected to the negative input of the device (VINN). If a four-pin shunt is used, the inputs of the device are connected to the inner leads and GND1 is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the minimum total resistance of the resistive divider to limit the cross current I_{AC} to the desired value: $R_1 + R_2 = V_{AC} / I_{AC}$. The input voltage at the ISO224 results from the resistance ratio of R_1 and R_2 and the actual AC voltage: $V_{IN} = V_{AC} \times R_2 / (R_1 + R_2)$.

Consider the following two restrictions to choose the proper value of the R_1 and R_2 resistors:

- The voltage drop on R_2 caused by the nominal AC voltage range of the system must not exceed the recommended input voltage range V_{IN} of the ISO224
- The voltage drop on R_2 caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: $V_{IN} \leq V_{Clipping}$

表 2 lists examples of nominal E96-series (1% accuracy) resistor values for AC systems using 120 V, 240 V, and 400 V as nominal voltages.

表 2. Resistor Value Examples

PARAMETER	120-V_{AC} SYSTEM	240-V_{AC} SYSTEM	400-V_{AC} SYSTEM
Resistive divider resistor R_1	115 kΩ	237 kΩ	392 kΩ
Resistive divider resistor R_2	12.7 kΩ	12.4 kΩ	12.1 kΩ
Resulting current through resistive divider I_{AC}	0.93 mA	0.93 mA	0.98 mA
Resulting input voltage V_{IN}	±11.934 V	±11.933 V	±11.977 V

For systems using single-ended input ADCs with a 5-V supply, 図 48 shows an example of a TLV6001-based signal conversion and filter circuit. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

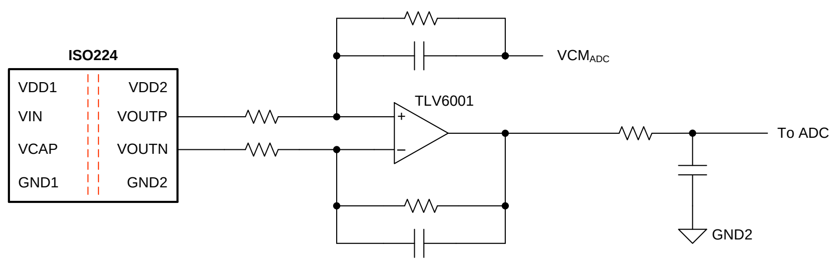


図 48. Connecting the ISO224 Output to a Single-Ended Input 5-V ADC

For systems using single-ended, ±10-V input ADCs, the ISO224EVM offers a signal path based on an OPA277 that converts the differential output of the ISO224 and limits the signal bandwidth to 50 kHz.

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, consult the *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power* TI Precision Designs, available for download at www.ti.com.

9.2.3 Application Curves

In some applications the system must be protected in case of an overvoltage condition. To allow for fast powering off of the system, a low delay caused by the isolated amplifier is required. 図 49 shows the typical full-scale step response of the device. Consider the delay of the required window comparator and the MCU to calculate the overall response time of the system.

図 49. Step Response of the ISO224

図 50 shows the typical AC response of the device with a full-scale sine wave with a frequency of 20 kHz applied at the input.

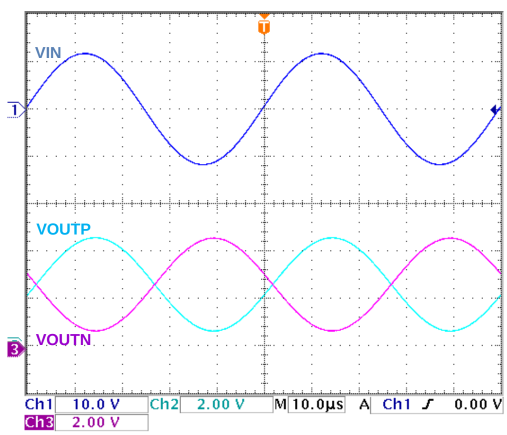


図 50. AC Response of the ISO224 at f_{IN} = 20 kHz

9.3 What to Do and What Not to Do

Do not leave the input of the ISO224 unconnected (floating) when the device is powered up. If the device input is left floating, both outputs are at the common-mode output voltage level V_{CMout} as specified in the *Switching Characteristics* table. See the *ISO224 Fail-Safe Output Feature* application report for more details.

10 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the ISO224 is generated from the low-side supply (VDD2) of the device by an isolated DC/DC converter circuit. A low-cost solution is based on the push-pull driver SN6501 and a transformer that supports the desired isolation voltage ratings. TI recommends using a low-ESR decoupling capacitor of 0.1 µF and an additional capacitor of a minimum 1 µF for both supplies of the ISO224. 図 51 shows the recommended placement of these decoupling capacitors as close as possible to the ISO224 power-supply pins to minimize supply current loops and electromagnetic emissions.

To decouple the output of the integrated LDO, use a 0.22-µF capacitor placed as close to the VCAP pin of the ISO224 as possible.

The ISO224 does not require any specific power up sequencing. Consider the analog settling time t_{AS} as specified in the *Switching Characteristics* table after ramp up of the VDD1 high-side supply.

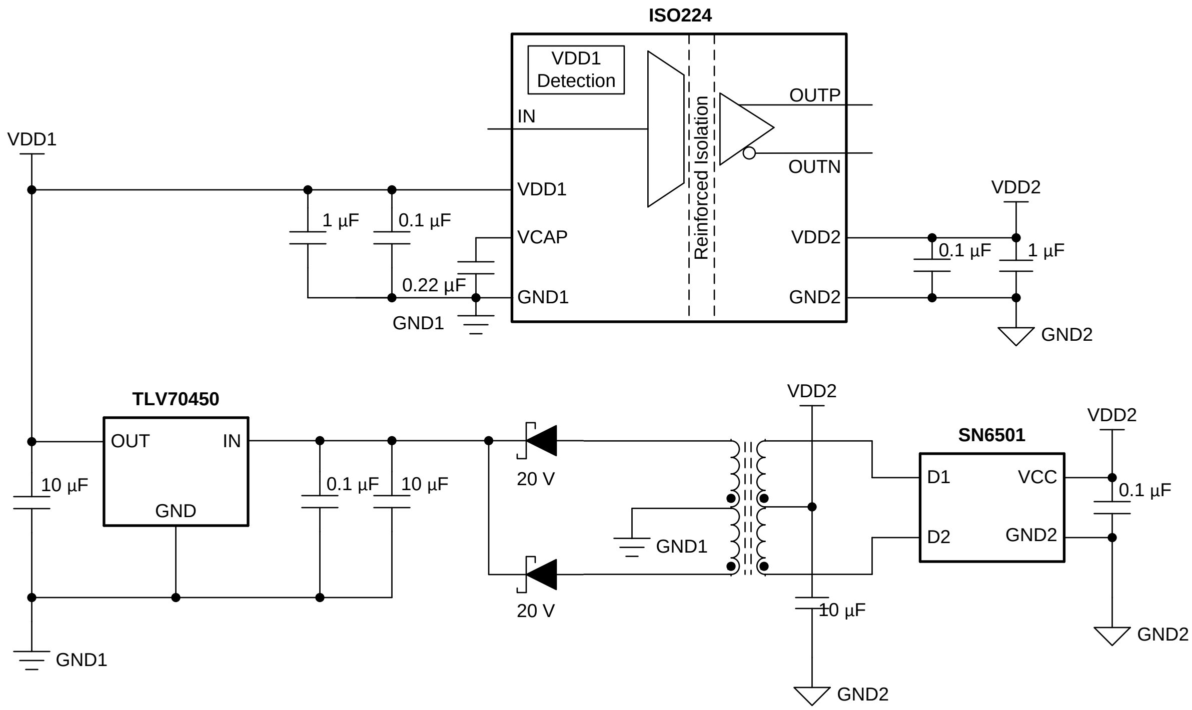


図 51. SN6501-Based, High-Side Power Supply

11 Layout

11.1 Layout Guidelines

For best performance, place the 0.22-µF capacitor (C7, as shown in 図 52) required for decoupling of the internal LDO output as close as possible to the ISO224 VCAP pin. The 0.1-µF ceramic decoupling capacitors for both power supplies (C8 and C9) are located as close as possible to the corresponding VDDx pins followed by the additional 1-µF ceramic capacitors for lower-frequency decoupling (C3 and C12). The resistor and capacitor used for the analog input (R1 and C2) are placed next to the decoupling capacitors. For best performance, use 0603-size or 1206-size, SMD-type, ceramic capacitors with low ESR. Connect the supply voltage sources in a way that allows the supply current to flow through the pads of the decoupling capacitors before powering the device.

図 52 shows this approach as implemented on the ISO224EVM. Capacitors C3 and C8 decouple the high-side supply VDD1 and capacitors C9 and C12 are used to support the low-side supply VDD2 of the ISO224.

11.2 Layout Example

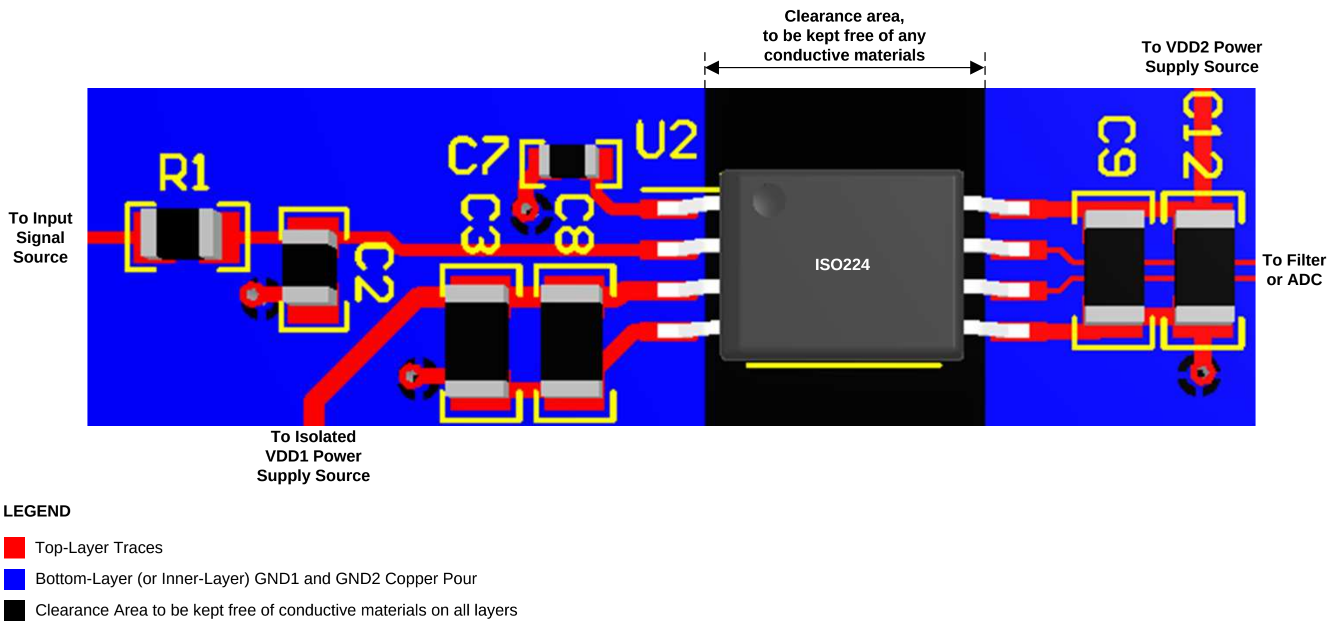


図 52. Recommended Layout of the ISO224

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*『絶縁の用語集』アプリケーション・レポート*
- テキサス・インスツルメンツ、*『ADS794x　14ビット、2MSPS、デュアル・チャネル、差動/シングルエンド、超低消費電力A/Dコンバータ』データシート*
- テキサス・インスツルメンツ、*『半導体およびICパッケージの熱指標』アプリケーション・レポート*
- テキサス・インスツルメンツ、*『ISO72x デジタルアイソレータ磁界耐性』アプリケーション・レポート*
- テキサス・インスツルメンツ、*『ISO224 フェイルセーフ出力機能』アプリケーション・レポート*
- テキサス・インスツルメンツ、*『TLV600x　低電力、レール・ツー・レール入出力、1MHzオペアンプ、低コスト・システム用』データシート*
- テキサス・インスツルメンツ、*『OPAx277 高精度オペアンプ』データシート*
- テキサス・インスツルメンツ、*『歪みとノイズが最低になるよう最適化された18ビット、1MSPSデータ収集ブロック(DAQ)』* TI Design
- テキサス・インスツルメンツ、*『消費電力が最低になるよう最適化された18ビット、データ収集ブロック(DAQ)』* TI Design
- テキサス・インスツルメンツ、*『SN6501 絶縁電源用の変圧器ドライバ』データシート*
- テキサス・インスツルメンツ、*『TLV704 24V入力電圧、150mA、超低I_Q低ドロップアウト・レギュレータ』データシート*
- テキサス・インスツルメンツ、*『ISO224EVM 評価モジュール』ユーザー・ガイド*

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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12.4 商標

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO224ADWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO224A	Samples
ISO224ADWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO224A	Samples
ISO224BDWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO224B	Samples
ISO224BDWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	ISO224B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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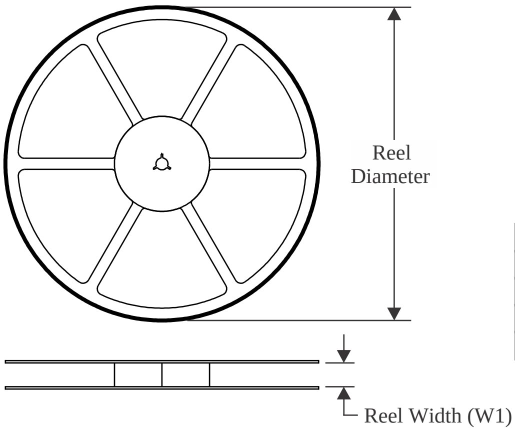
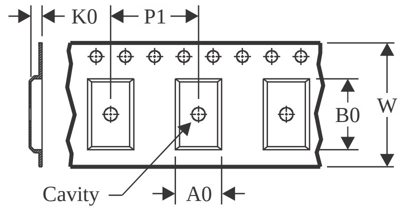
TAPE AND REEL INFORMATION

REEL DIMENSIONS

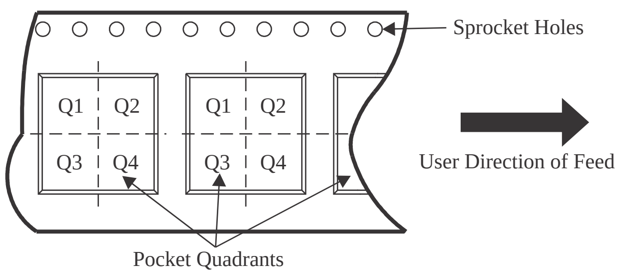


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

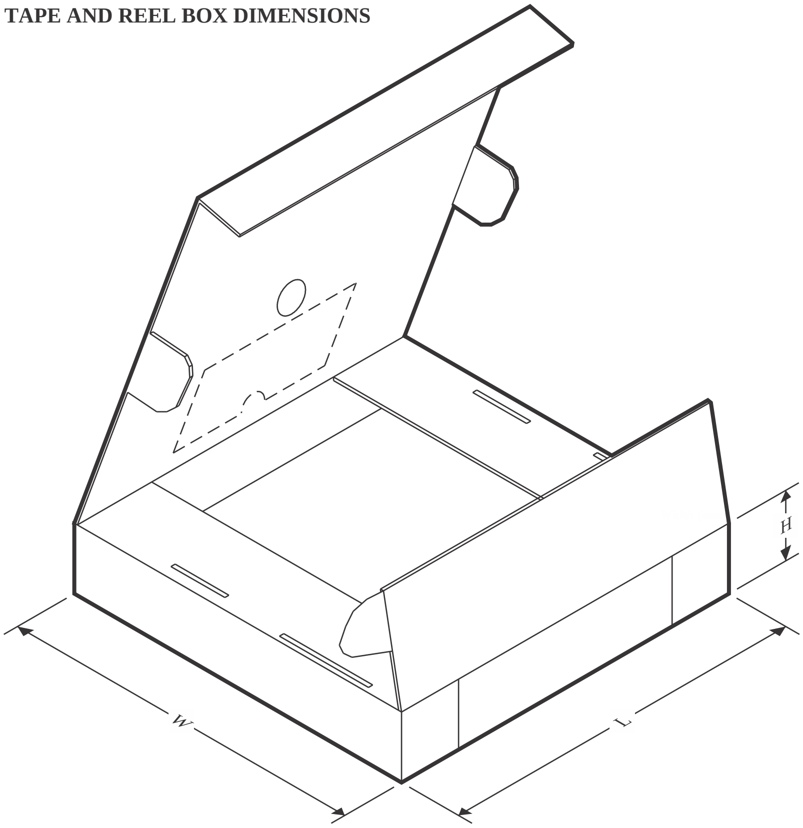
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO224ADWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1
ISO224BDWVR	SOIC	DWV	8	1000	330.0	16.4	12.05	6.15	3.3	16.0	16.0	Q1

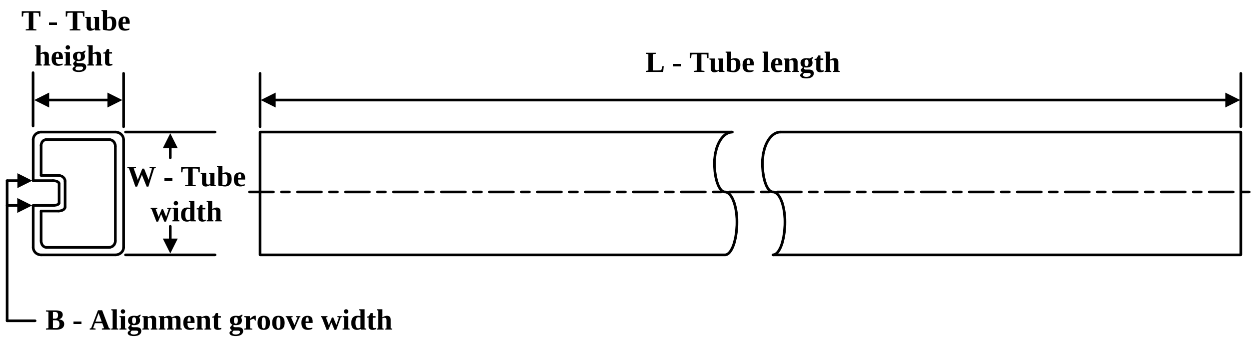
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO224ADWVR	SOIC	DWV	8	1000	350.0	350.0	43.0
ISO224BDWVR	SOIC	DWV	8	1000	350.0	350.0	43.0

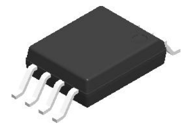
TUBE



*All dimensions are nominal

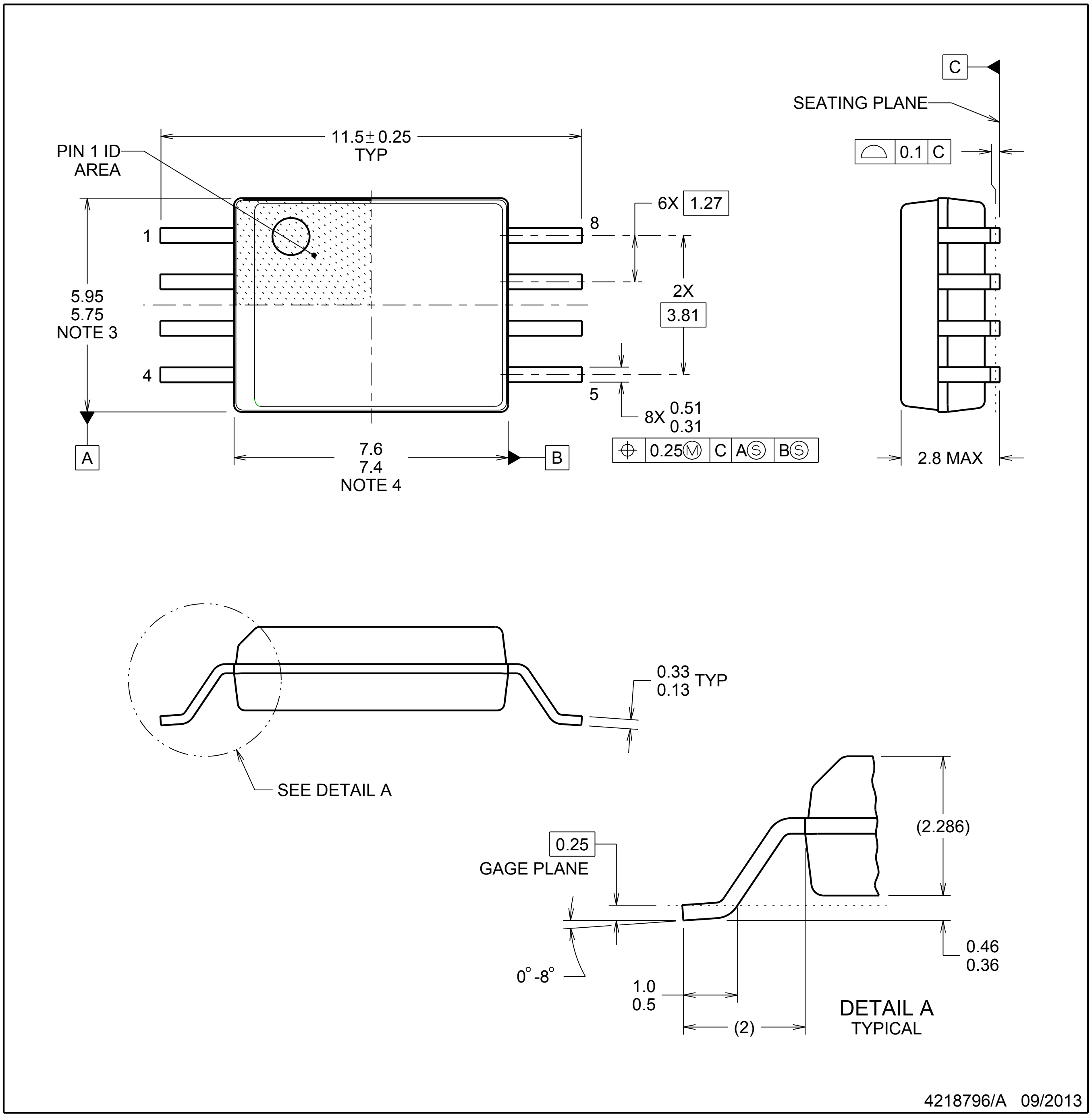
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO224ADWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6
ISO224BDWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6

DWV0008A



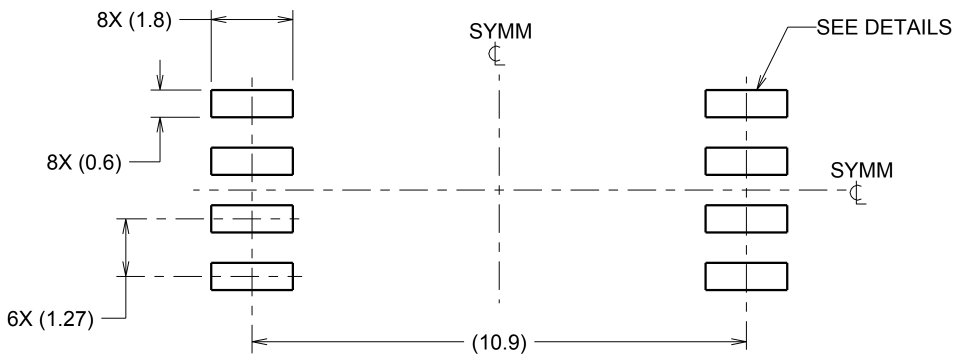
SOIC - 2.8 mm max height

SOIC

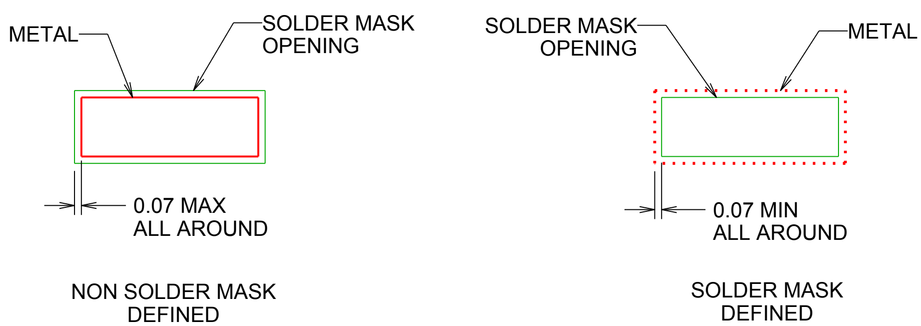


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X

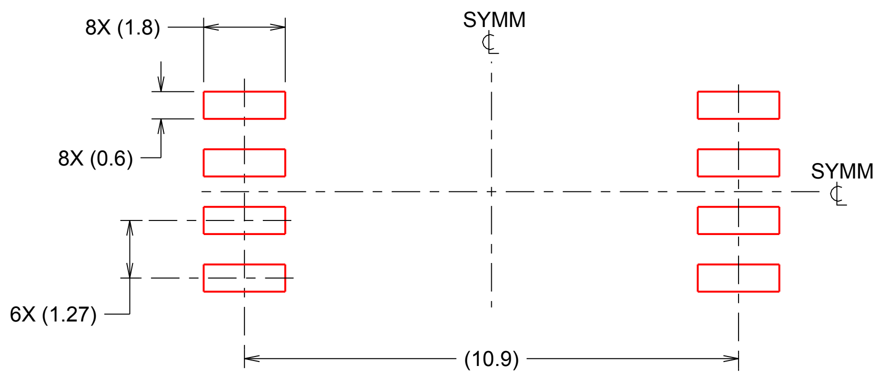


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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