TPS732 コンデンサ不要、NMOS、250mA、低ドロップアウト レギュレータ、逆電流保護機能搭載

1 特長

- 出力コンデンサなし、または任意の値またはタイプのコンデンサで安定動作
- 入力電圧範囲:1.7V～5.5V
- 非常に低いドロップアウト電圧:250mA において 40mV (標準値)
- オプションの出力コンデンサの有無にかかわらず非常に優れた負荷過渡応答
- NMOS トポロジにより、低い逆リーク電流を実現
- 低ノイズ:30μV_{RMS} (標準値、10kHz～100kHz)
- 0.5% の初期精度
- 1% の総合精度 (ライン、負荷、温度)
- シャットダウン モードの最大 I_Q:1µA 未満
- サーマル シャットダウン、仕様規定された最小 / 最大電流制限保護
- 複数の出力電圧バージョンが利用可能:
  - 固定出力:1.2V～5V
  - 可変出力:1.2V～5.5V
  - カスタム出力品も提供

2 アプリケーション

- 携帯型およびバッテリ駆動の機器
- スイッチング電源のポスト レギュレーション
- ノイズの影響を受けやすい回路 (VCO など)
- DSP、FPGA、ASIC、マイクロプロセッサのポイント オブ ロード レギュレーション

3 概要

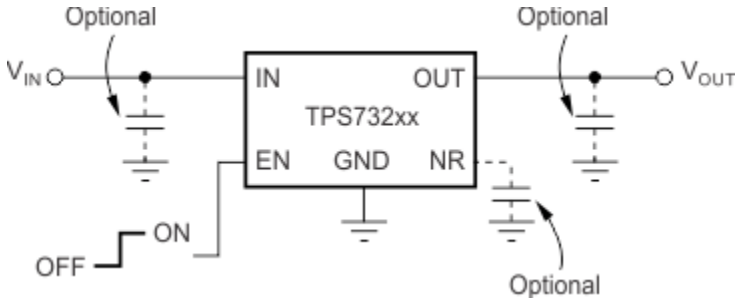
TPS732 低ドロップアウト (LDO) 電圧レギュレータは、NMOS パス トランジスタを電圧フォロワ構成で使用します。このトポロジは、低等価直列抵抗 (ESR) の出力コンデンサを使用して安定に動作し、コンデンサを使用しなくても動作できます。また、このデバイスは逆耐圧が高く (低逆電流)、グランド ピン電流が全出力電流値にわたってほぼ一定です。

TPS732 は、非常に低いドロップアウト電圧と小さいグランド ピン電流を実現すると同時に、先進の BiCMOS プロセスを使用することで高い精度を達成しています。ディセーブル時の消費電流は 1µA 未満であり、携帯型アプリケーション向けに設計されています。非常に小さい出力ノイズ (0.1µF の C_{NR} で 30μV_{RMS}) は、VCO への電力供給向けに設計されています。このデバイスは、サーマル シャットダウンとフォールドバック電流制限によって保護されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS732	DBV (SOT-23、5)	2.9mm × 2.8 mm
	DCQ (SOT-223、6)	6.5mm × 7.06 mm
	DRB (VSON、8)	3mm × 3 mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション回路(固定電圧バージョン)

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4 Pin Configuration and Functions

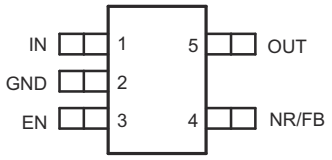


図 4-1. DBV Package, 5-Pin SOT-23 (Top View)

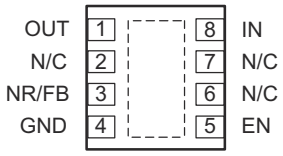


図 4-2. DRB Package, 8-Pin VSON With Exposed Thermal Pad (Top View)

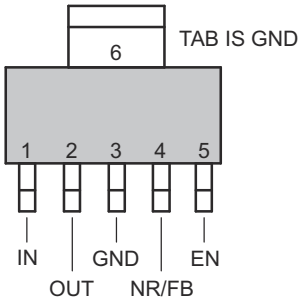


図 4-3. DCQ Package, 6-Pin SOT-223 (Top View)

表 4-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	NO.				
	SOT-23	SOT-223	VSON		
IN	1	1	8	I	Input supply.
GND	2	3, 6	4, Pad	—	Ground.
EN	3	5	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the *Enable Pin and Shutdown* section under *Feature Description* for more details. Connect EN to IN if not used.
NR	4	4	3	—	Fixed voltage versions only—connecting an external capacitor to this pin bypasses noise generated by the internal band gap, reducing output noise to very low levels.
FB	4	4	3	I	Adjustable voltage version only—this pin is the input to the control loop error amplifier, and is used to set the output voltage of the device.
OUT	5	2	1	O	Output of the regulator. There are no output capacitor requirements for stability.

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	Input, V_{IN}	–0.3	6	V
	Enable, V_{EN}	–0.3	6	
	Output, V_{OUT}	–0.3	5.5	
	V_{NR}, V_{FB}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See Thermal Information		
Temperature	Operating junction, T_J	–55	150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	1.7		5.5	V
I_{OUT}	Output current	0		250	mA
T_J	Operating junction temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS732 M3 new silicon		UNIT
		DRB (VSON)	DCQ (SOT-223)	
		8 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.7	76	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.9	46.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.6	18.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.4	8.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20.6	17.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Thermal Information

THERMAL METRIC[1] [2]		TPS732 Legacy silicon[3]			UNIT
		DRB (VSON)	DCQ (SOT-223)	DBV (SOT-23)	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.3	53.1	205.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	93.8	35.2	119	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	72.8	7.8	35.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.7	2.9	12.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25	7.7	34.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.
(3) Thermal data for the DRB, DCQ, and DBV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
(a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.
ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array.
iii. DBV: There is no exposed pad with the DBV package.
(b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
iii. DBV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
(c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the Power Dissipation section of this data sheet.

5.6 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5V (1) , I_{OUT} = 10mA, V_{EN} = 1.7V , and C_{OUT} = 0.1µF , unless otherwise noted. Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range(1)			1.7		5.5	V
V_{FB}	Internal reference (TPS73201)	T_J = 25°C		1.198	1.204	1.210	V
V_{OUT}	Output voltage range (TPS73201)(2)			V_{FB}		5.5 - V_{DO}	V
	Accuracy(1) (3)	Nominal	T_J = 25°C	–0.5		0.5	%
		V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5V ≤ V_{IN} ≤ 5.5V; 10mA ≤ I_{OUT} ≤ 250mA	–1	±0.5	1	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation (1)	$V_{OUT(NOM)}$ + 0.5V ≤ V_{IN} ≤ 5.5V			0.01		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	1mA ≤ I_{OUT} ≤ 250mA			0.002		%/mA
		10mA ≤ I_{OUT} ≤ 250mA			0.0005		
V_{DO}	Dropout voltage(4) (V_{IN} = $V_{OUT(NOM)}$ - 0.1V)	I_{OUT} = 250mA			40	150	mV
$Z_{O(do)}$	Output impedance in dropout	1.7V ≤ V_{IN} ≤ V_{OUT} + V_{DO}			0.25		Ω
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(nom)}$		250	425	600	mA
I_{SC}	Short-circuit current	V_{OUT} = 0V			300		mA
I_{REV}	Reverse leakage current(5) (-I_{IN})	V_{EN} ≤ 0.5V, 0V ≤ V_{IN} ≤ V_{OUT}			0.1	10	µA
I_{GND}	Ground pin current	I_{OUT} = 10mA (I_Q), legacy silicon			400	550	µA
		I_{OUT} = 10mA (I_Q), new silicon, M3 suffix			400	630	
I_{GND}	Ground pin current	I_{OUT} = 250mA			650	950	µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V, –40°C ≤ T_J ≤ 100°C, legacy silicon			0.02	1	µA
		V_{EN} ≤ 0.5V, V_{OUT} ≤ V_{IN} ≤ 5.5V, new silicon, M3 suffix			0.02	1	
I_{FB}	Feedback pin current (TPS73201)				0.1	0.3	µA
PSRR	Power-supply rejection ratio (ripple rejection)	f = 100Hz, I_{OUT} = 250mA			58		dB
		f = 10kHz, I_{OUT} = 250mA			37		
V_N	Output noise voltage, BW = 10Hz to 100kHz	C_{OUT} = 10µF, no C_{NR}			27 x V_{OUT}		μV_{RMS}
		C_{OUT} = 10µF, C_{NR} =0.01µF			8.5 x V_{OUT}		
$V_{EN(high)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(high)}$	Enable pin current (enabled)	V_{EN} = 5.5V			0.02	0.1	µA
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			160		°C
		Reset, temperature decreasing			140		
T_J	Operating junction temperature			–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7V, whichever is greater.
(2) TPS73201 is tested at VOUT = 2.5V.
(3) Tolerance of external resistors not included in this specification.
(4) V_{DO} is not measured for output versions with $V_{OUT(nom)}$ < 1.8V, because minimum V_{IN} = 1.7V.
(5) Fixed-voltage versions only; refer to *Application Information* section for more information.

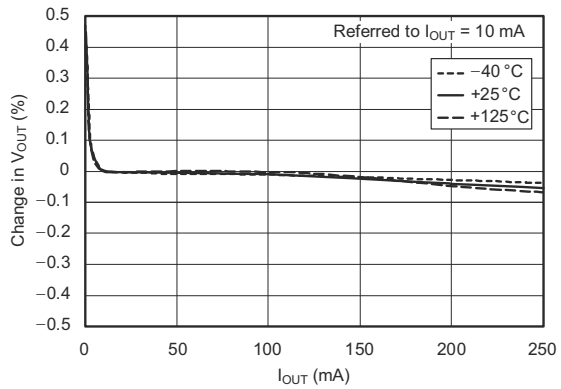
5.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-up time	V_{OUT} = 3V, R_L = 30Ω, C_{OUT} = 1µF, C_{NR} = 0.01µF		600		µs

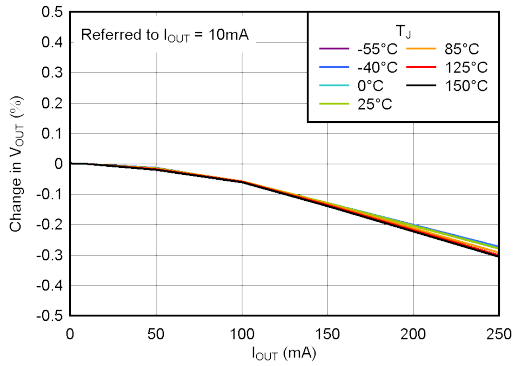
5.8 Typical Characteristics

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



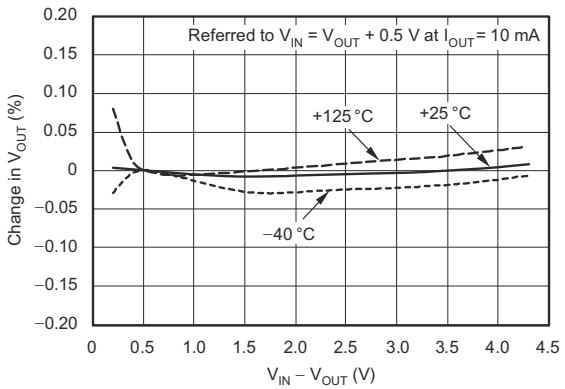
Legacy silicon

図 5-1. Load Regulation



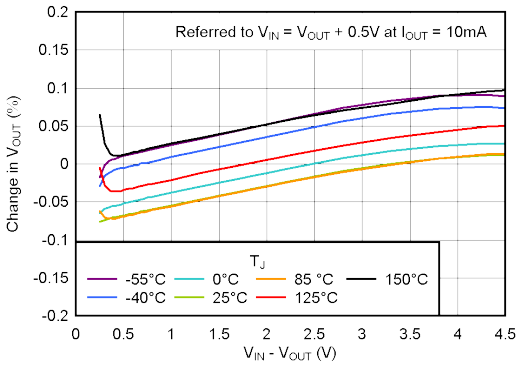
New silicon, M3 suffix

図 5-2. Load Regulation



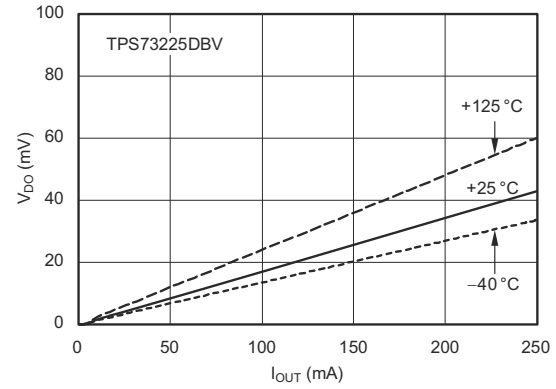
Legacy silicon

図 5-3. Line Regulation



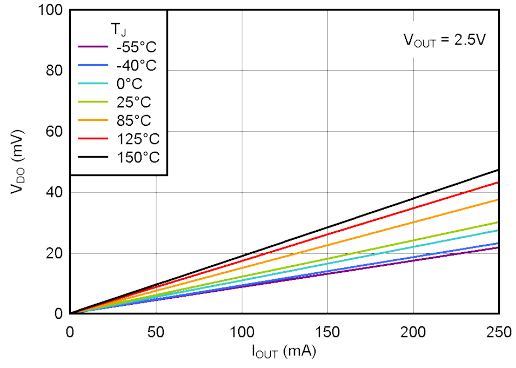
New silicon, M3 suffix

図 5-4. Line Regulation



Legacy silicon

図 5-5. Dropout Voltage vs Output Current

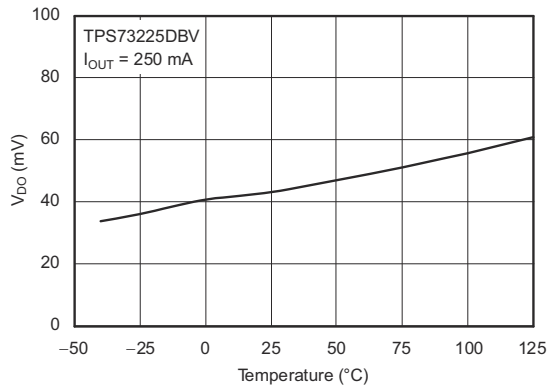


New silicon, M3 suffix

図 5-6. Dropout Voltage vs Output Current

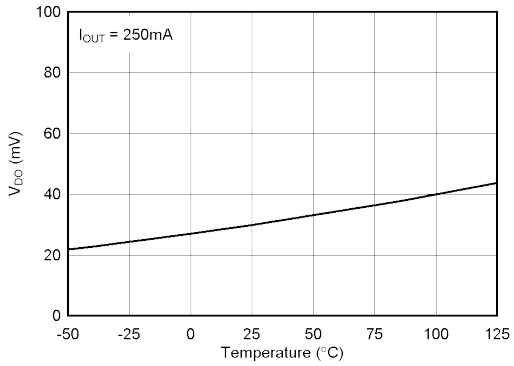
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



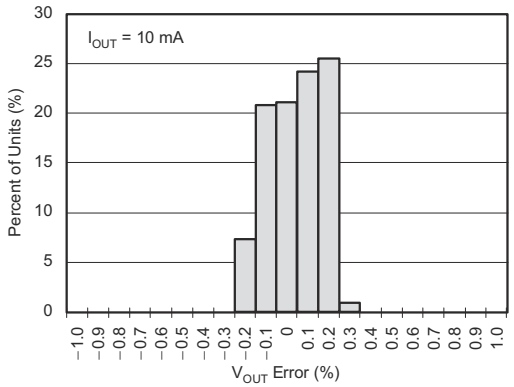
Legacy silicon

図 5-7. Dropout Voltage vs Temperature



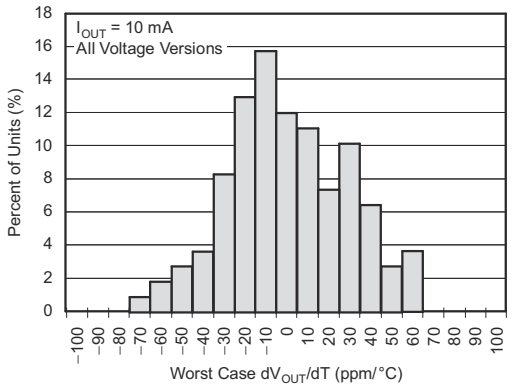
New silicon, M3 suffix

図 5-8. Dropout Voltage vs Temperature



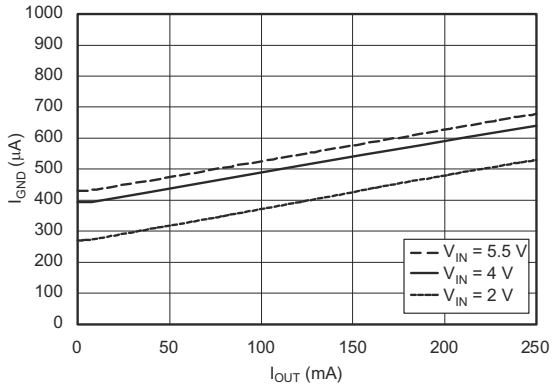
Legacy silicon

図 5-9. Output Voltage Accuracy Histogram



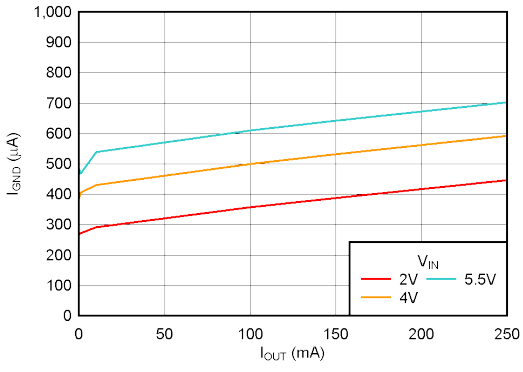
Legacy silicon

図 5-10. Output Voltage Drift Histogram



Legacy silicon

図 5-11. Ground Pin Current vs Output Current

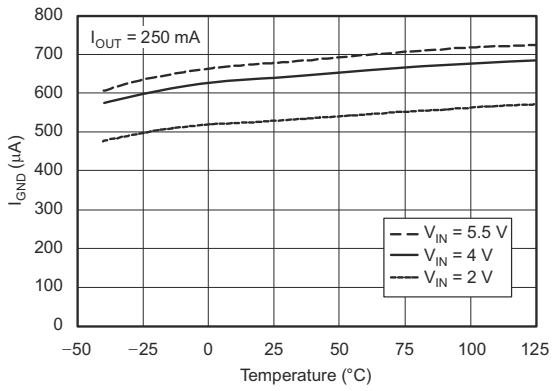


New silicon, M3 suffix

図 5-12. Ground Pin Current vs Output Current

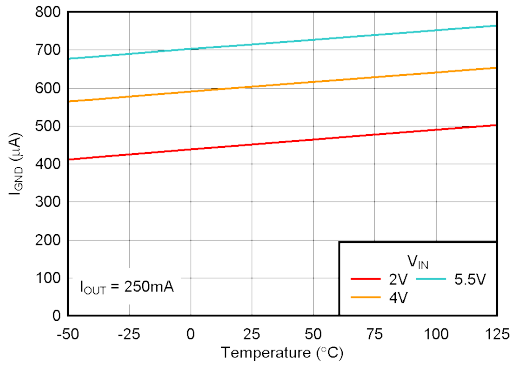
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



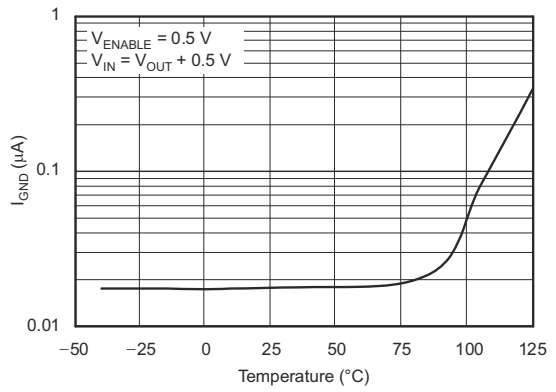
Legacy silicon

図 5-13. Ground Pin Current vs Temperature



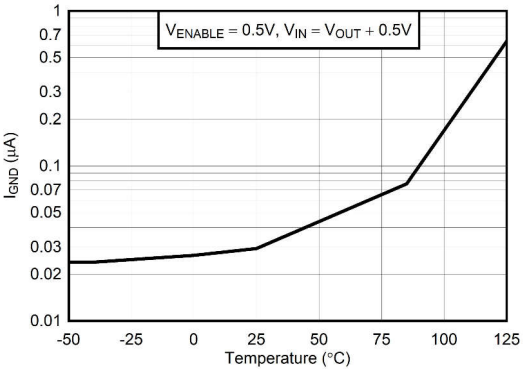
New silicon, M3 suffix

図 5-14. Ground Pin Current vs Temperature



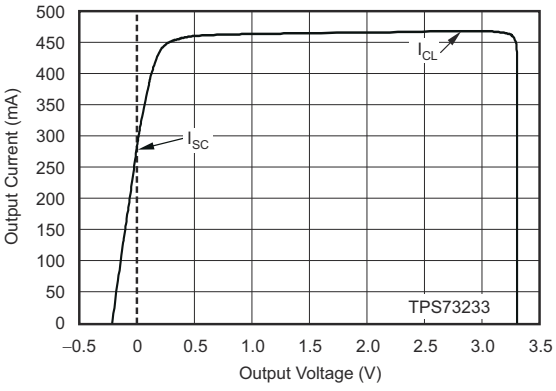
Legacy silicon

図 5-15. Ground Pin Current in Shutdown vs Temperature



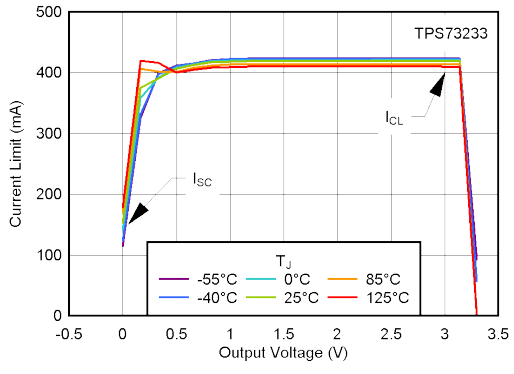
New silicon, M3 suffix

図 5-16. Ground Pin Current in Shutdown vs Temperature



Legacy silicon

図 5-17. Current Limit vs V_{OUT} (Foldback)

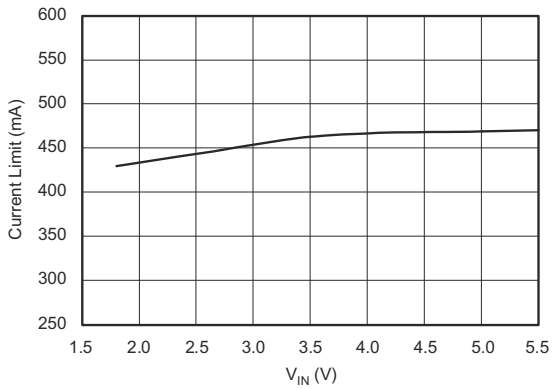


New silicon, M3 suffix

図 5-18. Current Limit vs V_{OUT} (Foldback)

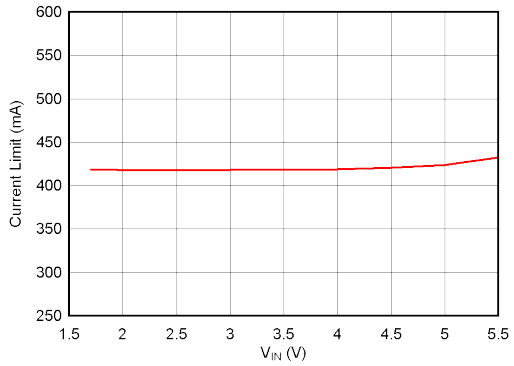
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



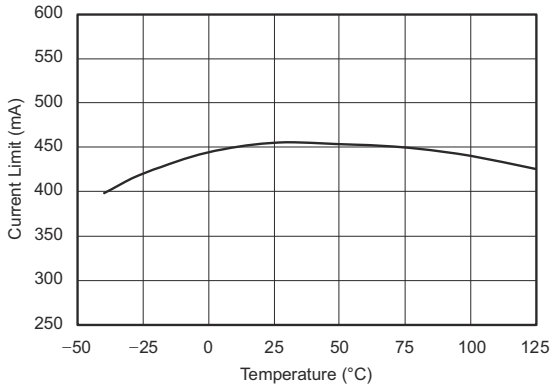
Legacy silicon

図 5-19. Current Limit vs V_{IN}



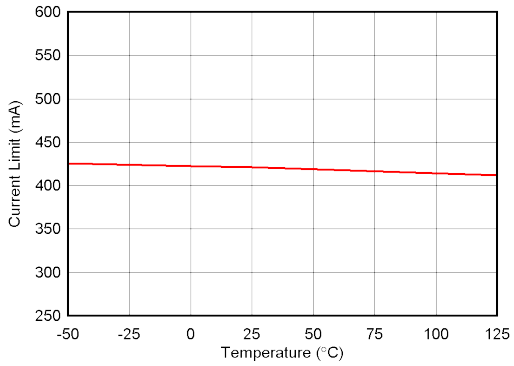
New silicon, M3 suffix

図 5-20. Current Limit vs V_{IN}



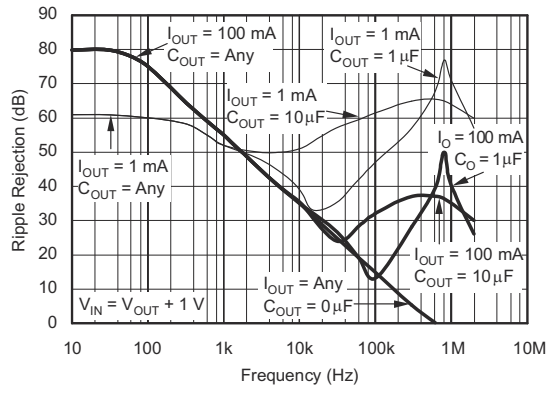
Legacy silicon

図 5-21. Current Limit vs Temperature



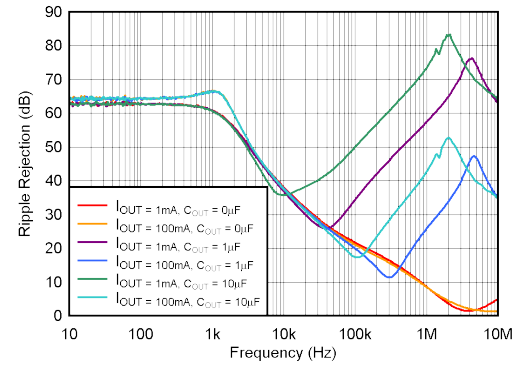
New silicon, M3 suffix

図 5-22. Current Limit vs Temperature



Legacy silicon

図 5-23. PSRR (Ripple Rejection) vs Frequency

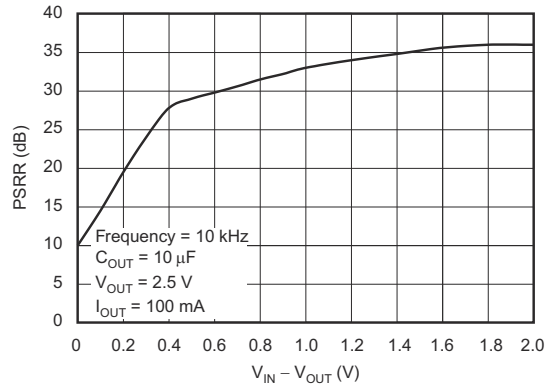


New silicon, M3 suffix

図 5-24. PSRR (Ripple Rejection) vs Frequency

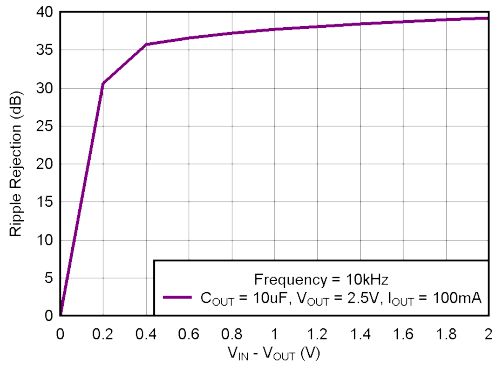
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



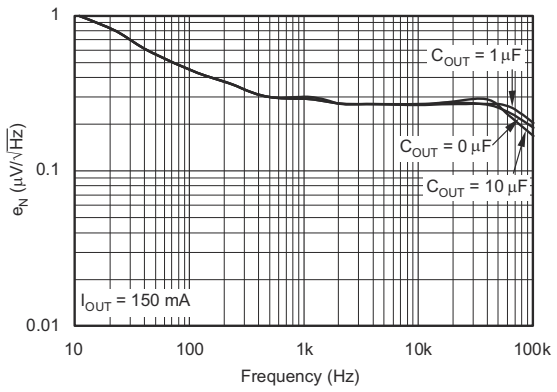
Legacy silicon

図 5-25. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})



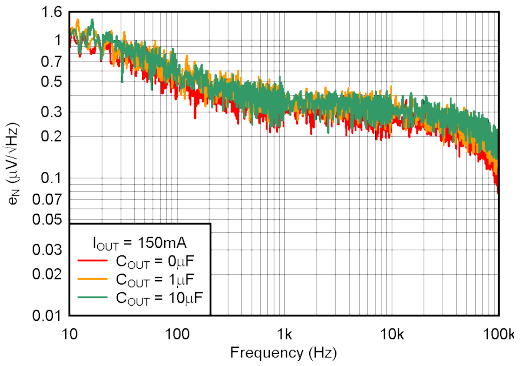
New silicon, M3 suffix

図 5-26. PSRR (Ripple Rejection) vs (V_{IN} – V_{OUT})



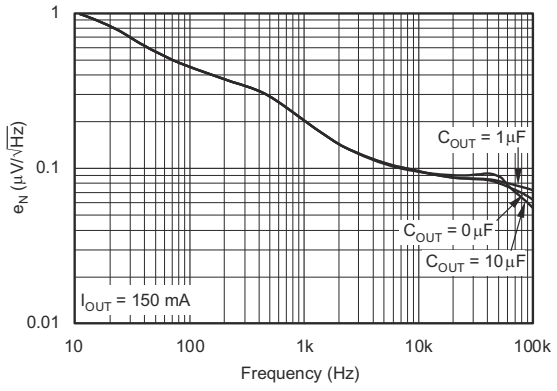
Legacy silicon

図 5-27. Noise Spectral Density C_{NR} = 0µF



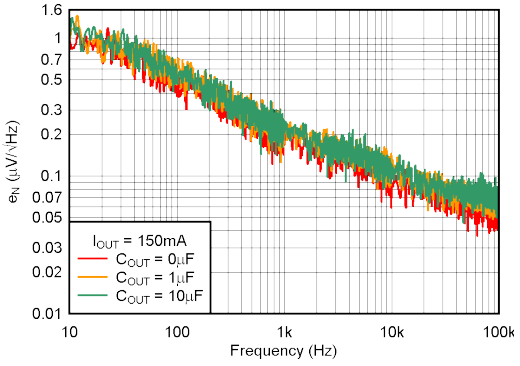
New silicon, M3 suffix

図 5-28. Noise Spectral Density C_{NR} = 0µF



Legacy silicon

図 5-29. Noise Spectral Density C_{NR} = 0.01µF

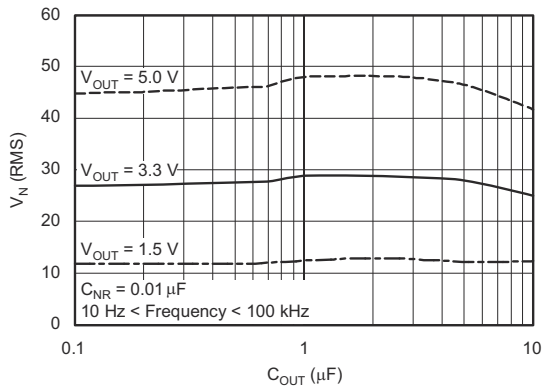


New silicon, M3 suffix

図 5-30. Noise Spectral Density C_{NR} = 0.01µF

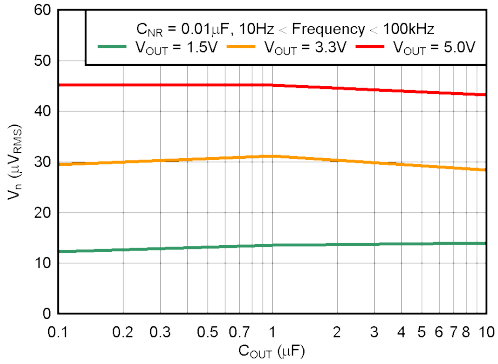
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



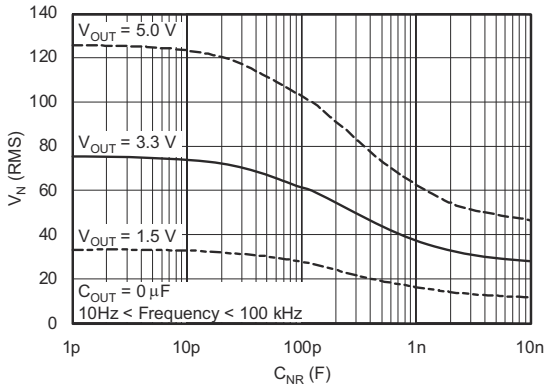
Legacy silicon

図 5-31. RMS Noise Voltage vs C_{OUT}



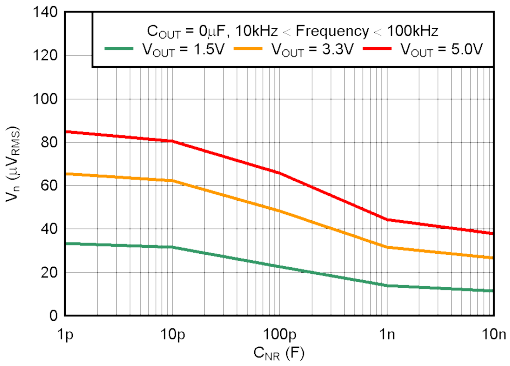
New silicon, M3 suffix

図 5-32. RMS Noise Voltage vs C_{OUT}



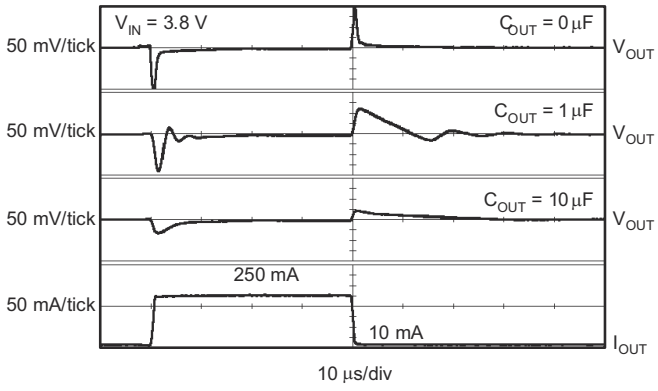
Legacy silicon

図 5-33. RMS Noise Voltage vs C_{NR}



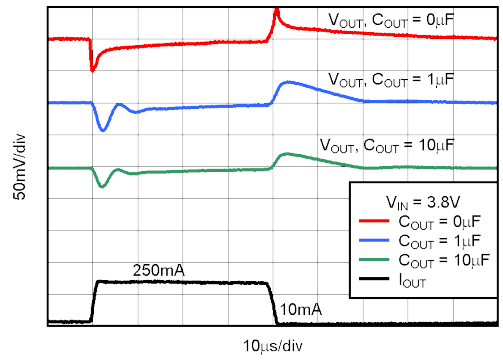
New silicon, M3 suffix

図 5-34. RMS Noise Voltage vs C_{NR}



Legacy silicon

図 5-35. TPS73233 Load Transient Response

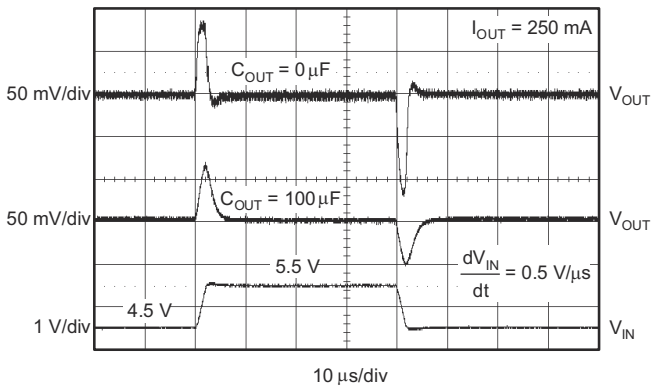


New silicon, M3 suffix

図 5-36. TPS73233 Load Transient Response

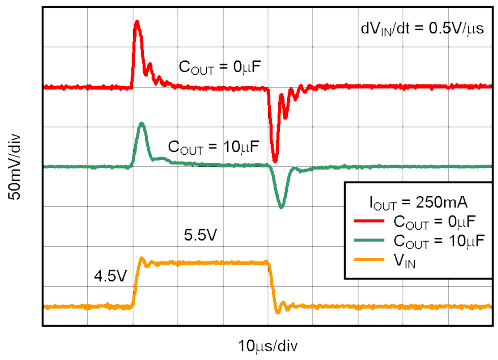
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



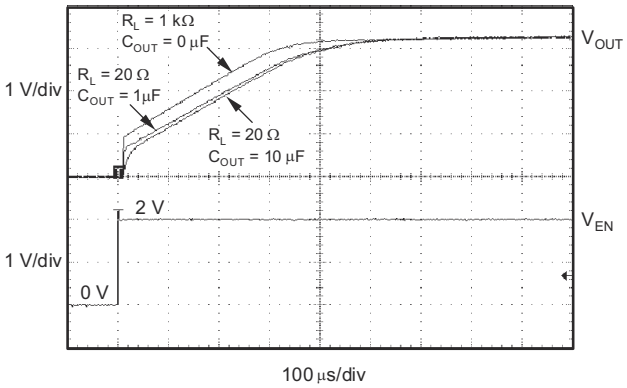
Legacy silicon

図 5-37. TPS73233 Line Transient Response



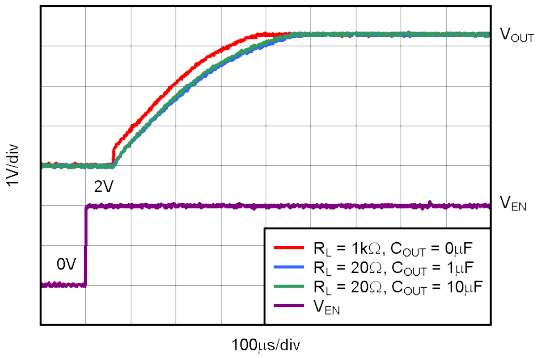
New silicon, M3 suffix

図 5-38. TPS73233 Line Transient Response



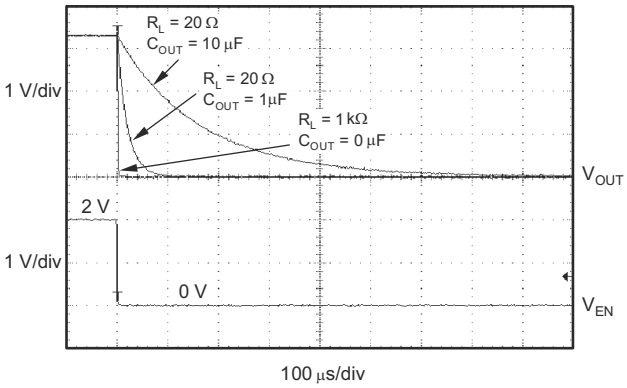
Legacy silicon

図 5-39. TPS73233 Turn-On Response



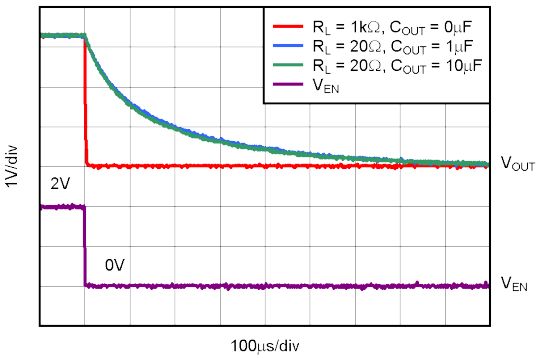
New silicon, M3 suffix

図 5-40. TPS73233 Turn-On Response



Legacy silicon

図 5-41. TPS73233 Turn-Off Response

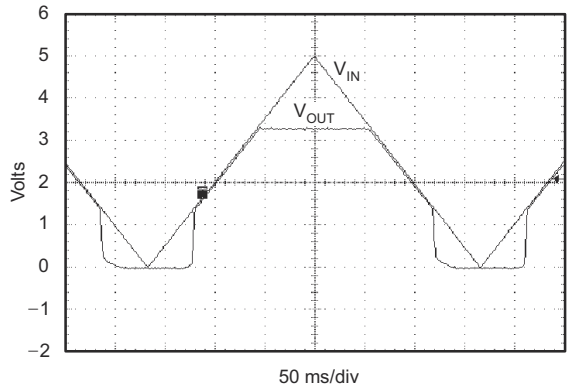


New silicon, M3 suffix

図 5-42. TPS73233 Turn-Off Response

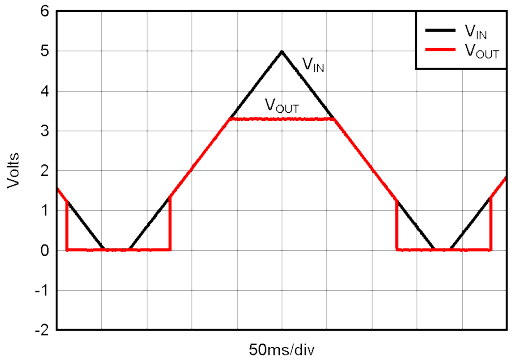
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



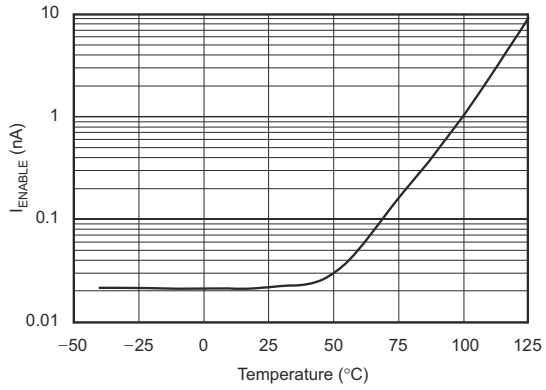
Legacy silicon

図 5-43. TPS73233 Power-Up and Power-Down



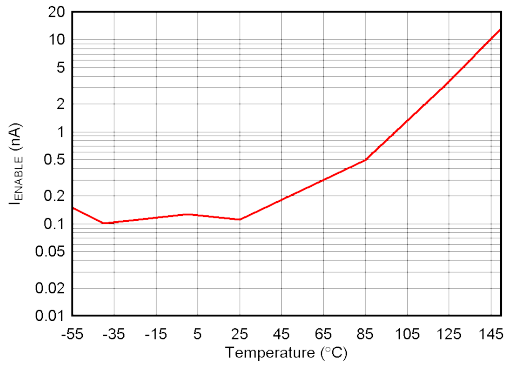
New silicon, M3 suffix

図 5-44. TPS73233 Power-Up and Power-Down



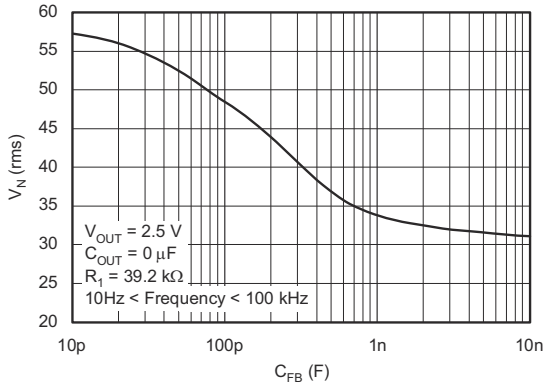
Legacy silicon

図 5-45. I_{ENABLE} vs Temperature



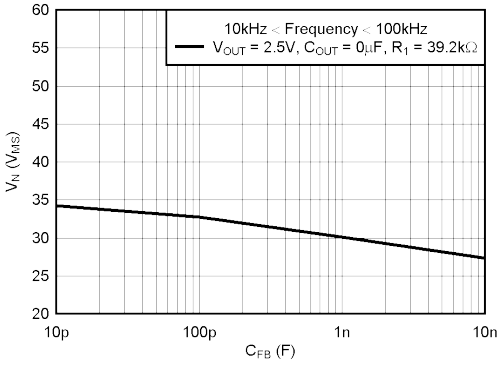
New silicon, M3 suffix

図 5-46. I_{ENABLE} vs Temperature



Legacy silicon

図 5-47. TPS73201 RMS Noise Voltage vs C_{FB}

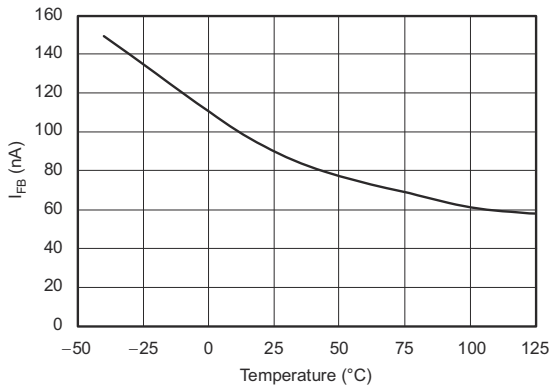


New silicon, M3 suffix

図 5-48. TPS73201 RMS Noise Voltage vs C_{FB}

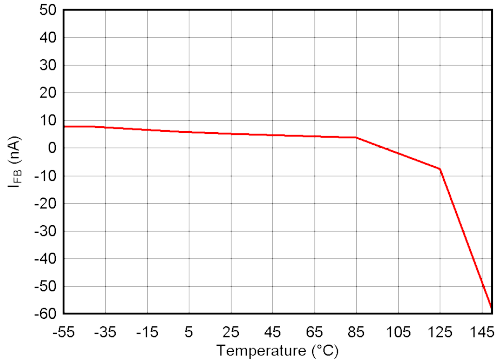
5.8 Typical Characteristics (continued)

for all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5V, I_{OUT} = 10mA, V_{EN} = 1.7V, and C_{OUT} = 0.1µF (unless otherwise noted)



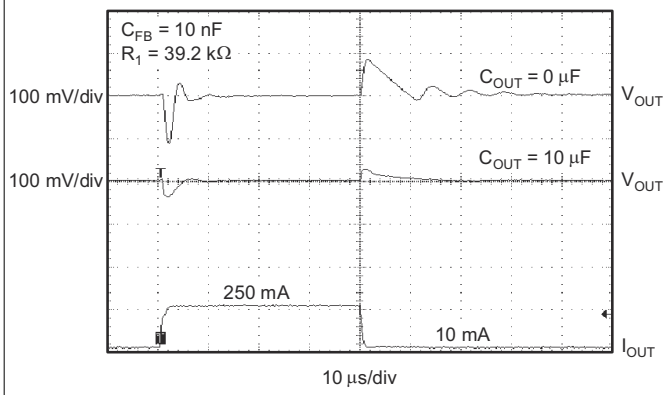
Legacy silicon

図 5-49. TPS73201 I_{FB} vs Temperature



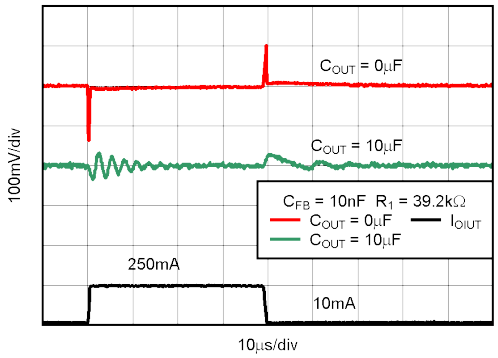
New silicon, M3 suffix

図 5-50. TPS73201 I_{FB} vs Temperature



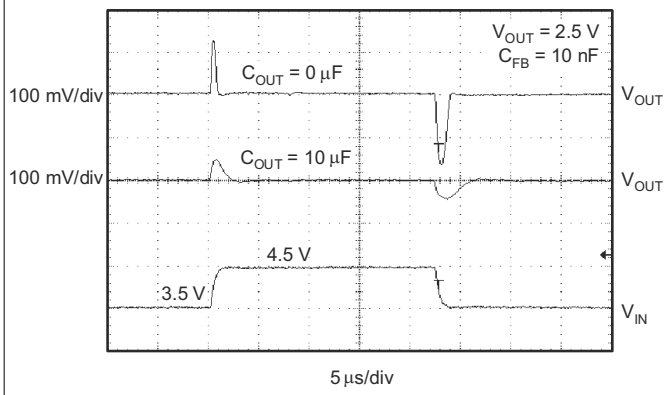
Legacy silicon

図 5-51. TPS73201 Load Transient, Adjustable Version



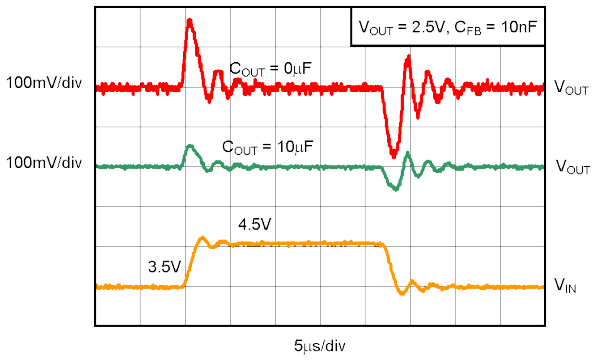
New silicon, M3 suffix

図 5-52. TPS73201 Load Transient, Adjustable Version



Legacy silicon

図 5-53. TPS73201 Line Transient, Adjustable Version



New silicon, M3 suffix

図 5-54. TPS73201 Line Transient, Adjustable Version

6 Detailed Description

6.1 Overview

The TPS732 low-dropout linear regulator operates down to an input voltage of 1.7V and supports output voltages down to 1.2V while sourcing up to 250mA of load current. This linear regulator uses an NMOS pass transistor with an integrated 4MHz charge pump to provide a dropout voltage of less than 150mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. Furthermore, the TPS732 does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this linear regulator designed for powering a load where the effective capacitance is unknown.

The TPS732 also features a noise-reduction (NR) pin that allows for additional reduction of the output noise. With a noise reduction capacitor of 0.01µF connected from the NR pin to GND, the TPS73215 typical output noise is 12.75µV_{RMS}. The low noise output featured by the TPS732 makes the device designed for powering VCOs or any other noise-sensitive load.

6.2 Functional Block Diagrams

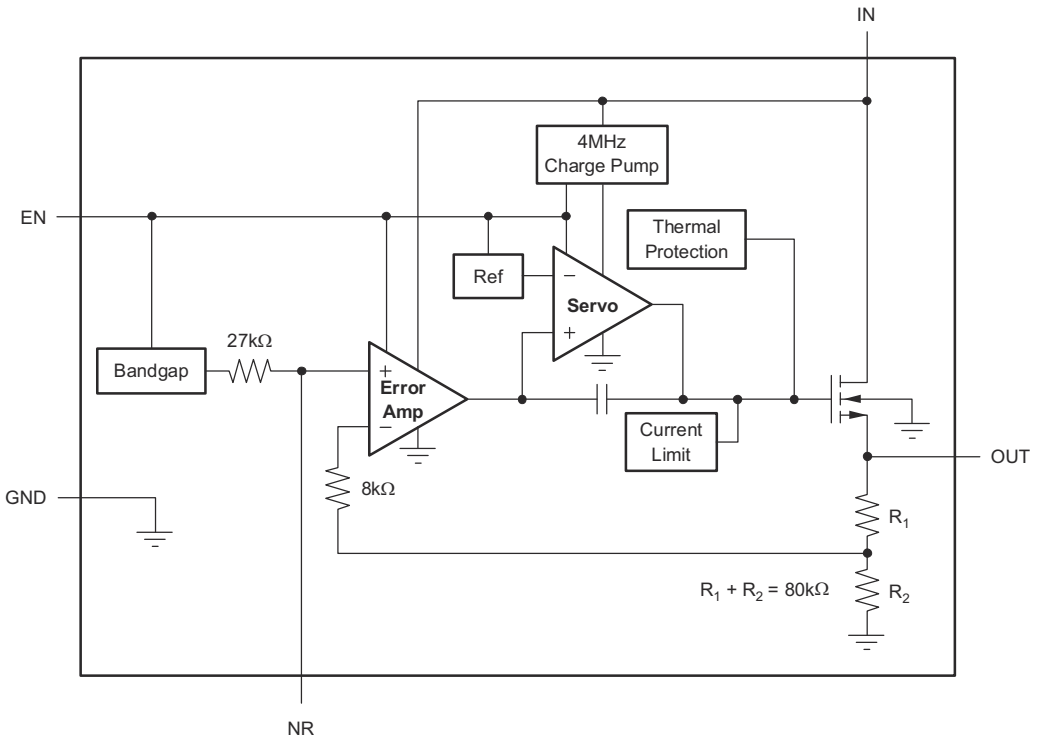


図 6-1. Fixed-Voltage Version

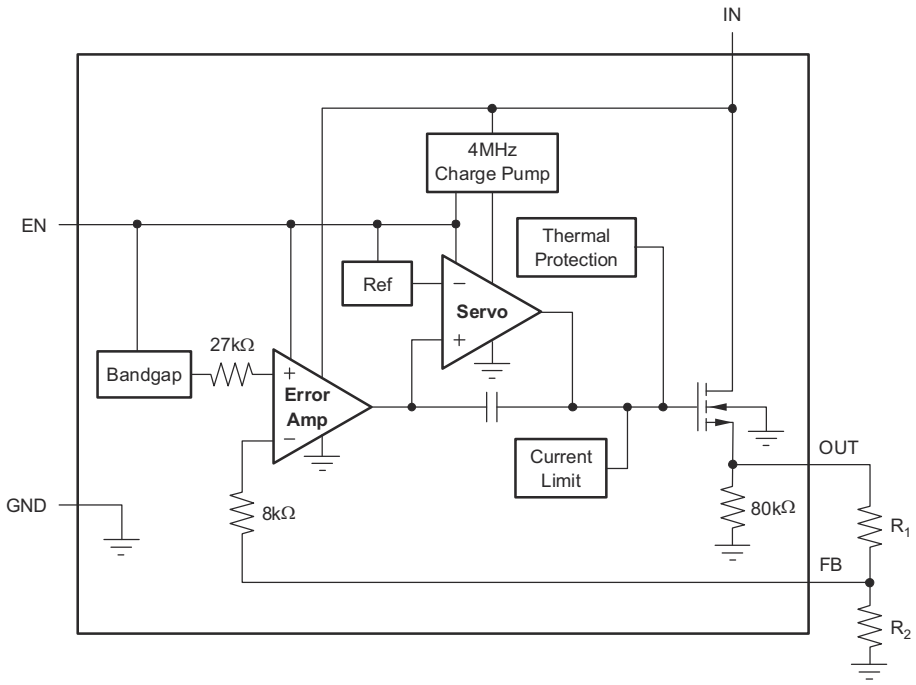


Table 1. Standard 1% Resistor Values for Common Output Voltages

V_O	R_1	R_2
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$; $R_1 || R_2 \cong 19k\Omega$ for best accuracy.

図 6-2. Adjustable-Voltage Version

6.3 Feature Description

6.3.1 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS732 and generates approximately $32\mu V_{RMS}$ (10Hz to 100kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \left(\frac{R_1 + R2}{R_2} \right) = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Because the value of V_{REF} is 1.2V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (2)$$

An internal 27kΩ resistor in series with the noise-reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise-reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10nF, the total noise in the 10Hz to 100kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (3)$$

for C_{NR} = 10nF.

This noise-reduction effect is shown as *RMS Noise Voltage vs C_{NR}* (図 5-33) in the *Typical Characteristics* section.

The TPS73201 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the feedback pin (FB) reduces output noise and improves load transient performance.

The TPS732 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass transistor above V_{OUT}. The charge pump generates approximately 250µV of switching noise at approximately 4MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

6.3.2 Internal Current Limit

The TPS732 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5V. See 図 5-17 in the *Typical Characteristics* section for a graph of I_{OUT} vs V_{OUT}.

From 図 5-17 approximately –0.2V of V_{OUT} results in a current limit of 0mA. Therefore, if OUT is forced below –0.2V before EN goes high, the device potentially does not start up. In applications that work with both a positive and negative voltage supply, enable the TPS732 first.

6.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5V (maximum) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shut down the regulator, all charge is removed from the pass transistor gate. A V_{EN} above 1.7V (minimum) turns the regulator on and the output ramps back up to a regulated V_{OUT} (see 図 5-39).

When shutdown capability is not required, connect EN to V_{IN}. However, the pass transistor potentially does not discharge using this configuration, causing the pass transistor to be left on (enhanced) for a significant time after V_{IN} is removed. This scenario results in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output potentially overshoots upon power up.

Current limit foldback prevents device start-up under some conditions. See the *Internal Current Limit* section.

6.3.4 Dropout Voltage

The TPS732 uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the NMOS pass transistor.

For large step changes in load current, the TPS732 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the DC dropout. Values of (V_{IN} – V_{OUT}) above this line provide normal transient response.

Operating in the transient dropout region causes an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to DC dropout levels], the TPS732 takes a couple of hundred microseconds to return to the specified regulation accuracy.

6.3.5 Reverse Current

The NMOS pass transistor of the TPS732 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass transistor is pulled low. To make sure all charge is removed from the gate of the pass transistor, drive the EN pin low before the input voltage is removed. If this process is not done, the pass transistor is potentially left on because of stored charge on the transistor.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin resulting from the voltage applied on the OUT pin. Additional current flows into the OUT pin from the 80kΩ internal resistor divider to ground (see 図 6-1 and 図 6-2).

For the TPS73201, reverse current potentially flows when V_{FB} is more than 1V above V_{IN}.

6.4 Device Functional Modes

6.4.1 Normal Operation With 1.7V ≤ V_{IN} ≤ 5.5V and V_{EN} ≥ 1.7V

The TPS732 requires an input voltage of at least 1.7V to function properly and attempt to maintain regulation.

When operating the device near 5.5V, suppress any transient spikes that exceed the 6V absolute maximum voltage rating. Never operate the device at a DC voltage greater than 5.5V.

7 Application and Implementation

注

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7.1 Application Information

The TPS732 LDO regulator uses an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732 designed for portable applications. This regulator offers a wide selection of fixed-output voltage versions and an adjustable-output version. All versions have thermal and overcurrent protection, including foldback current limit.

7.2 Typical Application

図 7-1 shows the basic circuit connections for the fixed-voltage models. 図 7-2 gives the connections for the adjustable-voltage version (TPS73201).

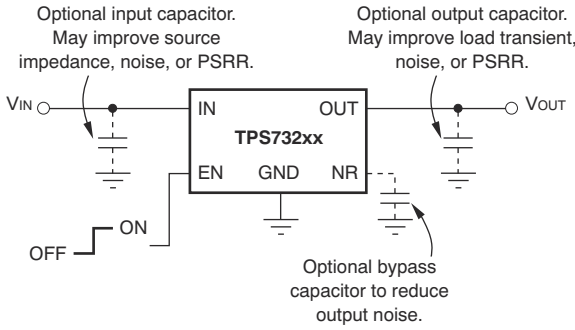


図 7-1. Typical Application Circuit for Fixed-Voltage Versions

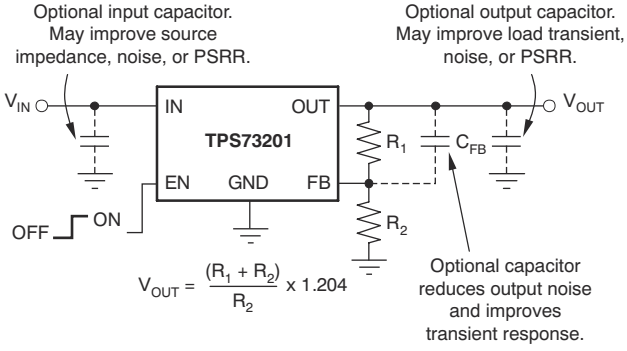


図 7-2. Typical Application Circuit for Adjustable-Voltage Version

7.2.1 Design Requirements

R_1 and R_2 are calculated for any output voltage using the formula in 図 7-2. Sample resistor values for common output voltages are given in 図 6-2.

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19kΩ. This 19kΩ, in addition to the internal 8kΩ resistor, presents the same impedance to the error amplifier as the 27kΩ band-gap reference output. This impedance helps compensate for leakages into the error amplifier terminals.

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1µF to 1µF, low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor is necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732 does not require an output capacitor for stability and has maximum phase margin with no capacitor. The device is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing potentially occurs when the product of C_{OUT} and total ESR drops below 50nF × Ω. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.2.2.2 Transient Response

The low open-loop output impedance provided by the NMOS pass transistor in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1µF) from the OUT pin to ground reduces undershoot magnitude but increases the duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the OUT pin to the FB pin also improves transient response.

The TPS732 does not have active pulldown when the output is overvoltage. This feature allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This feature also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot is reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal or external load resistance. The rate of decay is given by:

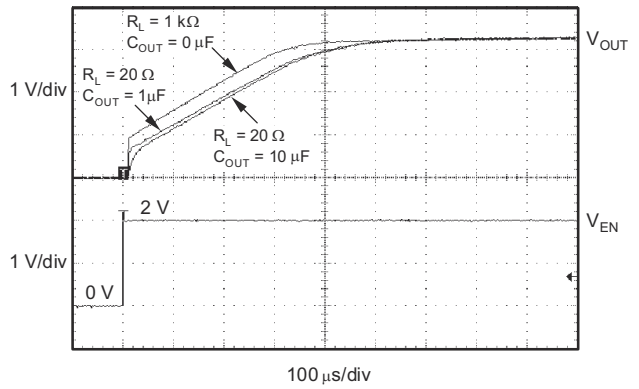
(Fixed voltage versions)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \,||\, R_{LOAD}} \quad (4)$$

(Adjustable voltage version)

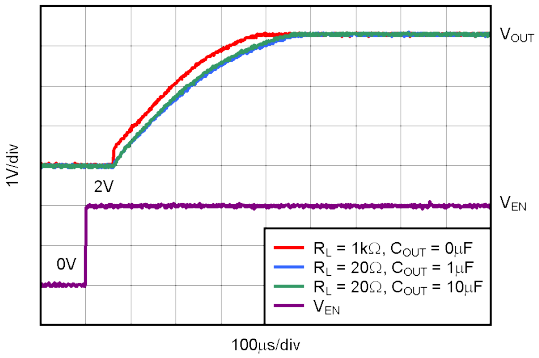
$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80k\Omega \,||\, (R_1 + R_2) \,||\, R_{LOAD}} \quad (5)$$

7.2.3 Application Curves



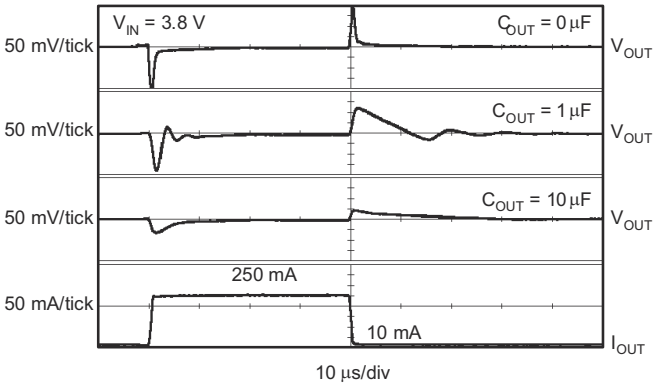
Legacy silicon

図 7-3. TPS73233 Turn-On Response



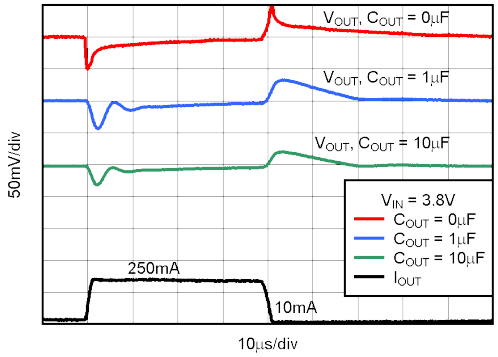
New silicon, M3 suffix

図 7-4. TPS73233 Turn-On Response



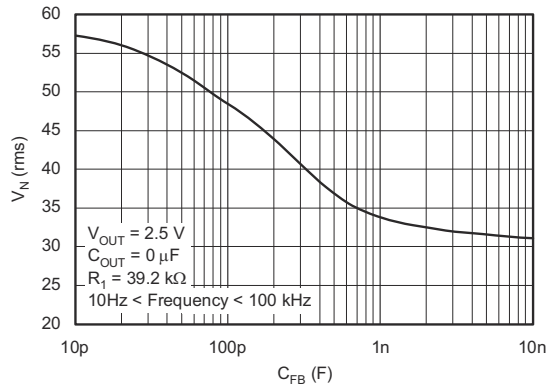
Legacy silicon

図 7-5. TPS73233 Load Transient Response



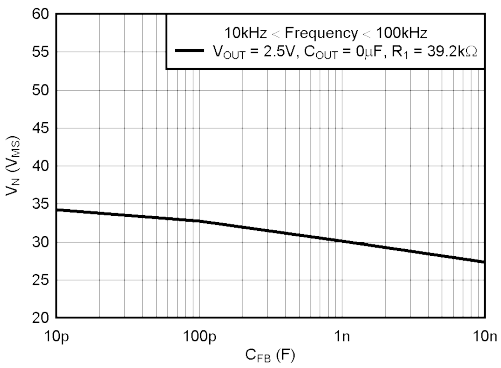
New silicon, M3 suffix

図 7-6. TPS73233 Load Transient Response



Legacy silicon

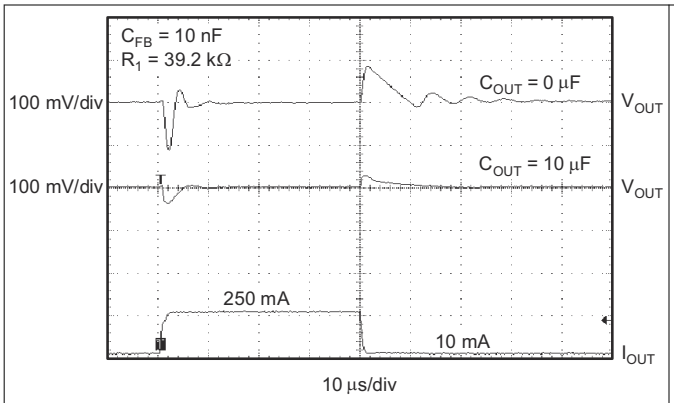
図 7-7. TPS73201 RMS Noise Voltage vs C_{FB}



New silicon, M3 suffix

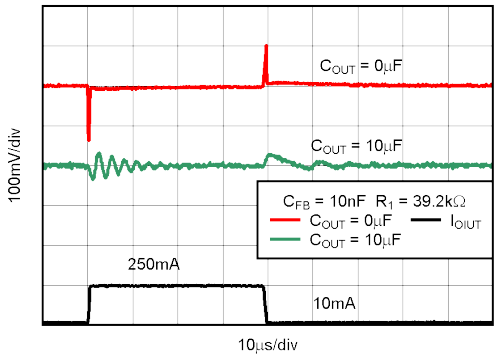
図 7-8. TPS73201 RMS Noise Voltage vs C_{FB}

7.2.3 Application Curves (continued)



Legacy silicon

図 7-9. TPS73201 Load Transient, Adjustable Version



New silicon, M3 suffix

図 7-10. TPS73201 Load Transient, Adjustable Version

7.3 Power Supply Recommendations

This device is designed to operate from an input voltage supply range between 1.7V and 5.5V. The input voltage range provides adequate headroom for the device to have a regulated output. Make sure this input supply is well regulated. If the input supply is noisy, additional input capacitors with low ESR help improve output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, design the PCB with ground plane connections for V_{IN} and V_{OUT} capacitors, and connect the ground plane at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

7.4.1.1 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit potentially cycles on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage caused by overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least 35°C above the maximum expected ambient condition of the application. This level produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS732 into thermal shutdown degrades device reliability.

7.4.1.1.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass transistor (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation is minimized by using the lowest possible input voltage necessary to provide the required output voltage.

7.4.2 Layout Examples

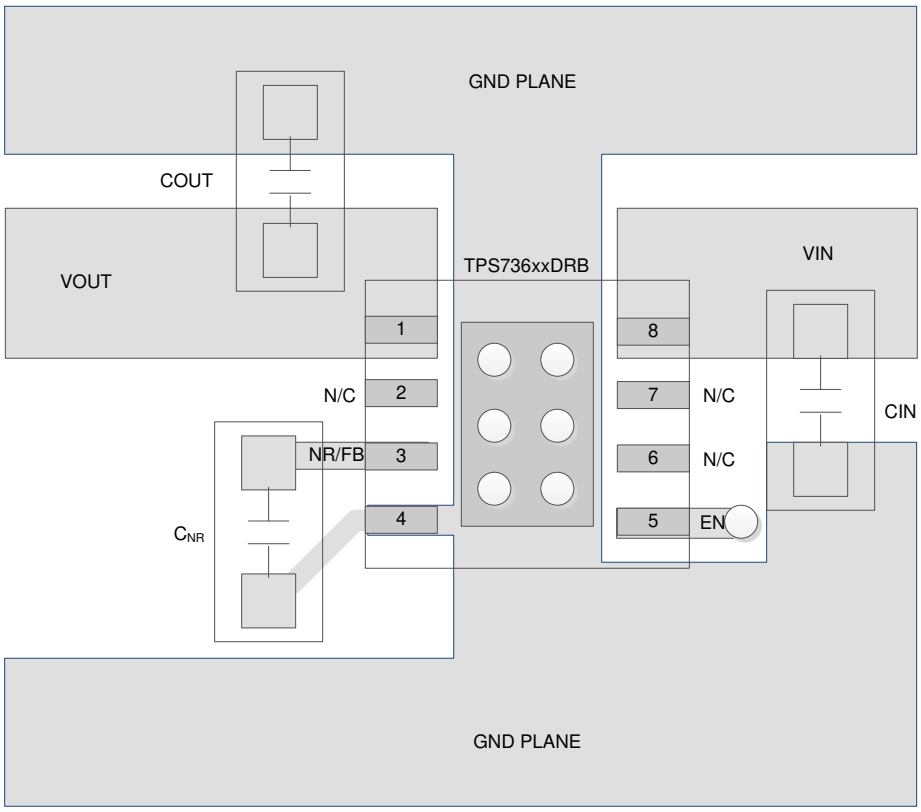


図 7-11. Fixed Output Voltage Option Layout (DRB Package)

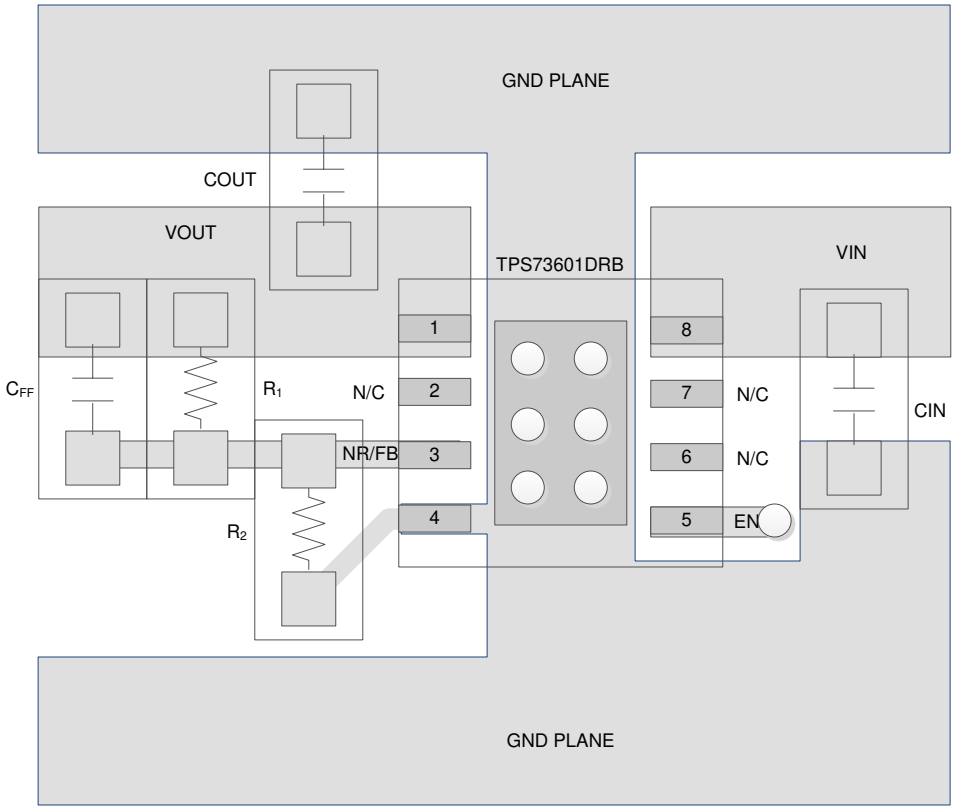


図 7-12. Adjustable Output Voltage Option Layout (DRB Package)

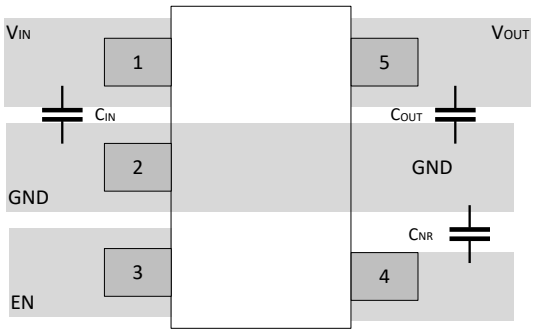


図 7-13. Layout Example for the DBV Package Fixed Version

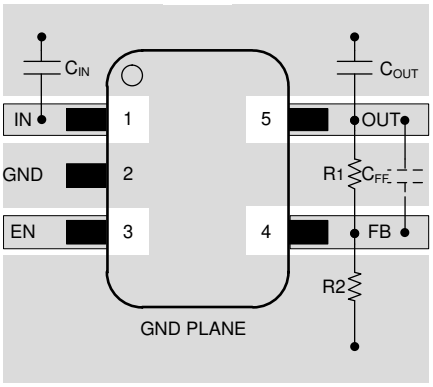


図 7-14. Layout Example for the DBV Package Adjustable Version

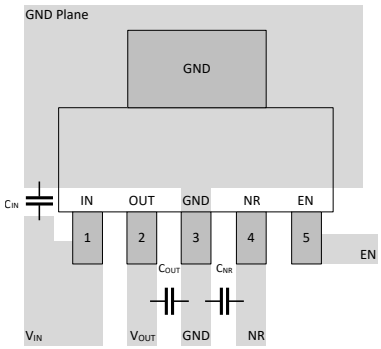


図 7-15. Layout Example for the DCQ Package Fixed Version

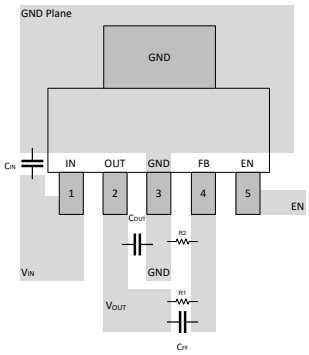


図 7-16. Layout Example for the DCQ Package Adjustable Version

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS732. Request the TPS73201DRBEVM-518 evaluation module (and related user guide) at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS732 is available through the product folders under *Simulation Models*.

8.1.2 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT(1)	V_{OUT}
TPS732**xxyyyz*(M3)***	**xx** is the nominal output voltage (for example, 25 = 2.5V; 01 = Adjustable). **yyy** is the package designator. **z** is the tape and reel quantity (R = 3000, T = 250). **M3** is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the *legacy silicon* (CSO: DLN) or the *new silicon* (CSO: RFB). The reel packaging label provides CSO information to distinguish which chip is being used. Device performance for new and legacy chips is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

- Texas Instruments, *Regulating V_{OUT} Below 1.2 V Using an External Reference* application note
- Texas Instruments, *TPS73x01DRBEVM-518 User's Guide*

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

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8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision P (December 2015) to Revision Q (September 2024) **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- ドキュメント全体で「SON」を「VSON」に変更 ... 1
- Changed VFB typical value ... 6
- Added M3 ground pin current spec ... 6
- Added M3 shutdown current spec ... 6
- Added new silicon plots to *Typical Characteristics* ... 7
- Changed load current max source from *500mA* to *250mA* and dropout voltage from *250mV* to *150mV* in *Overview* section ... 16
- Changed *total ESR drops below 50nΩF* to *total ESR drops below 50nF* × Ω in *Input and Output Capacitor Requirements* section ... 21
- Added new silicon plots to *Application Curves* section ... 22
- Changed *Layout Guidelines* section ... 23
- Added DBV and DCQ layout figures to *Layout Examples* section ... 24
- Added M3 information to *Device Nomenclature* ... 27

Changes from Revision O (August 2010) to Revision P (December 2015) **Page**

- 「特長」で NMOS トポロジに関する箇条書き項目を変更、「新規」を削除 ... 1
- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1
- 「概要」セクションの最初の段落を変更、NMOS トポロジを「新規」としていた説明を削除 ... 1
- Changed Pin Configuration and Functions section; updated table format ... 3

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73201DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DCQ	OBSOLETE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125	PS73201	
TPS73201DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS73201	Samples
TPS73201DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DRBRG4	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DRBRM3	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJEQ	Samples
TPS73201DRBT	OBSOLETE	SON	DRB	8		TBD	Call TI	Call TI	-40 to 125	PJEQ	
TPS73213DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BWD	Samples
TPS73215DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T38	Samples
TPS73215DCQ	OBSOLETE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125	PS73215	
TPS73215DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73215	Samples
TPS73216DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50	Samples
TPS73216DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T50	Samples
TPS73218DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T37	Samples
TPS73218DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	T37	
TPS73218DCQ	OBSOLETE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125	PS73218	
TPS73218DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS73218	Samples
TPS73219DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CGE	Samples
TPS73219DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	CGE	
TPS73225DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73225DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples
TPS73225DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T36	Samples
TPS73225DCQ	OBSOLETE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125	PS73225	
TPS73225DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73225	Samples
TPS73230DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T39	Samples
TPS73230DBVT	OBSOLETE	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	T39	
TPS73230DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73230	Samples
TPS73233DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40	Samples
TPS73233DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T40	Samples
TPS73233DCQ	OBSOLETE	SOT-223	DCQ	6		TBD	Call TI	Call TI	-40 to 125	PS73233	
TPS73233DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	PS73233	Samples
TPS73250DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41	Samples
TPS73250DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T41	Samples
TPS73250DCQR	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73250	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS732 :

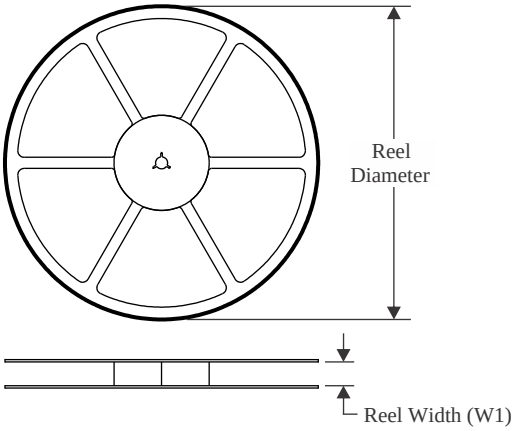
- Automotive : TPS732-Q1

NOTE: Qualified Version Definitions:

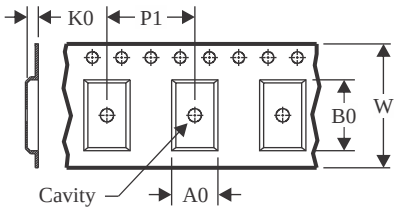
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

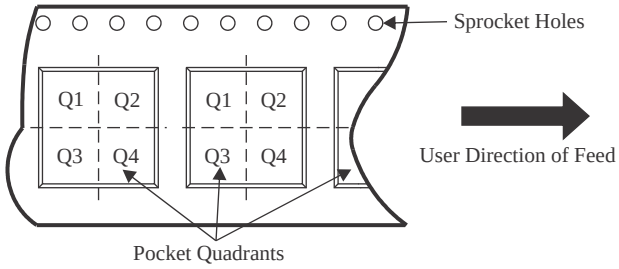


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

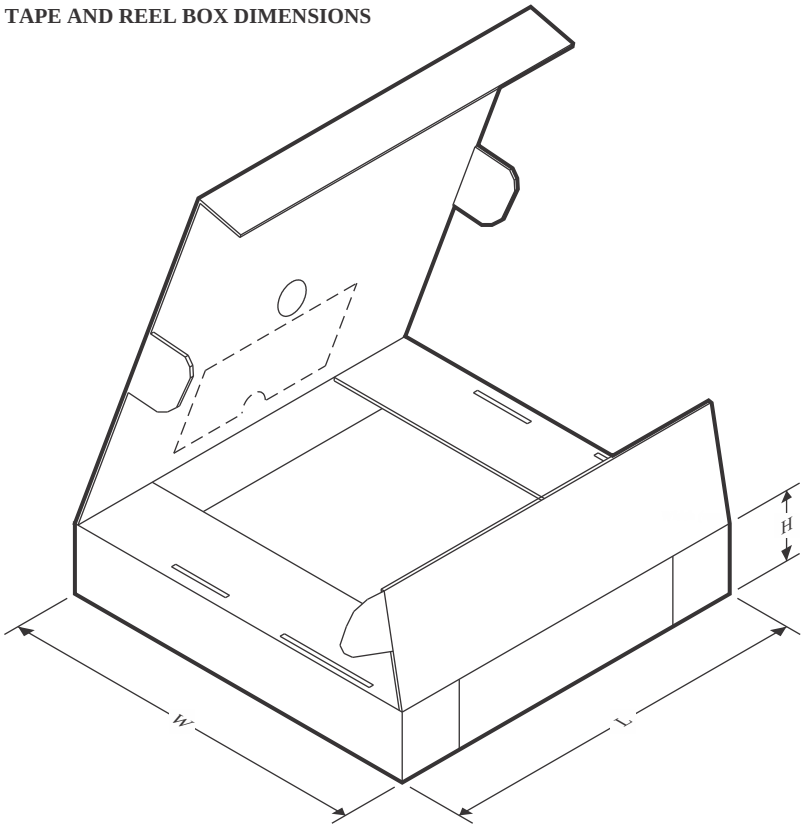


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73201DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73201DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73201DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73201DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73213DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73215DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73216DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73218DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73218DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73219DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73225DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73230DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73230DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73233DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73233DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73233DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73250DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73250DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73250DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73201DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73201DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0
TPS73201DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73201DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73213DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73215DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73215DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73216DBVT	SOT-23	DBV	5	250	213.0	191.0	35.0
TPS73218DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73218DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73219DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73225DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73225DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73225DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73230DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73230DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73233DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73233DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73233DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73250DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73250DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73250DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0

GENERIC PACKAGE VIEW

DRB 8

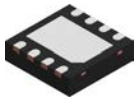
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

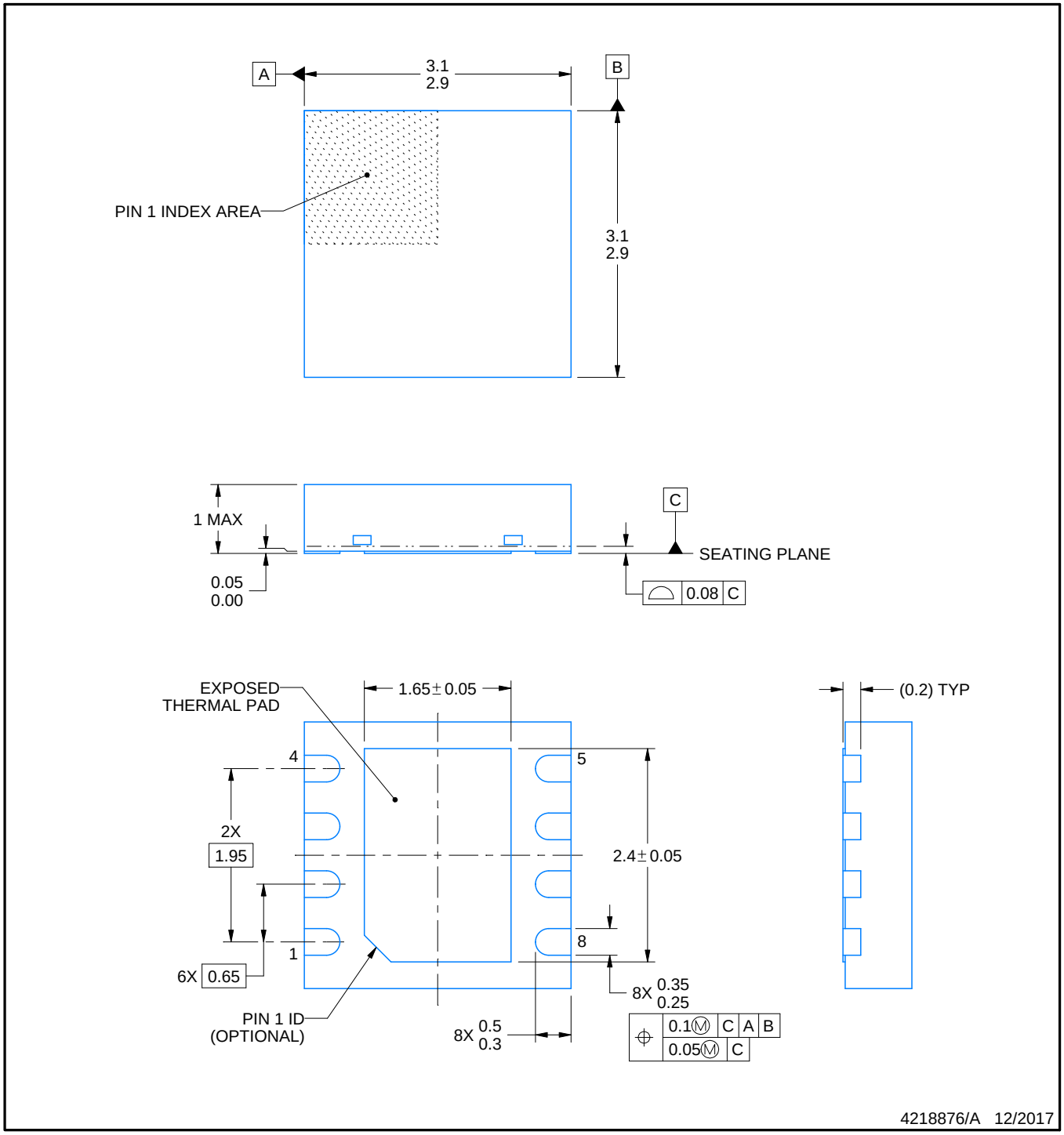
DRB0008B



PACKAGE OUTLINE

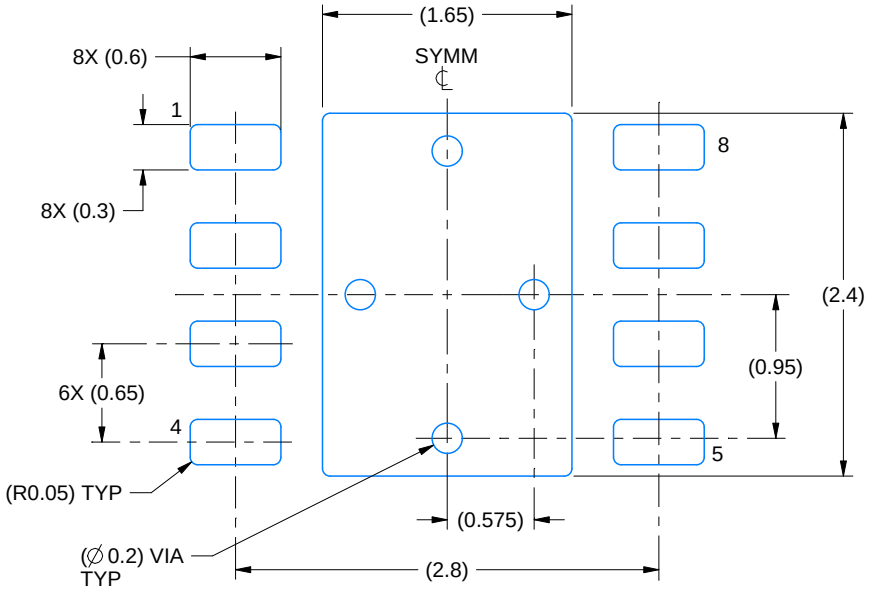
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

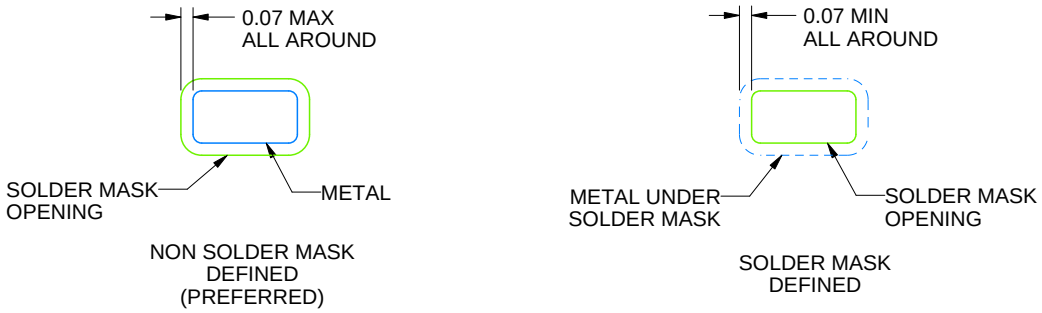


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

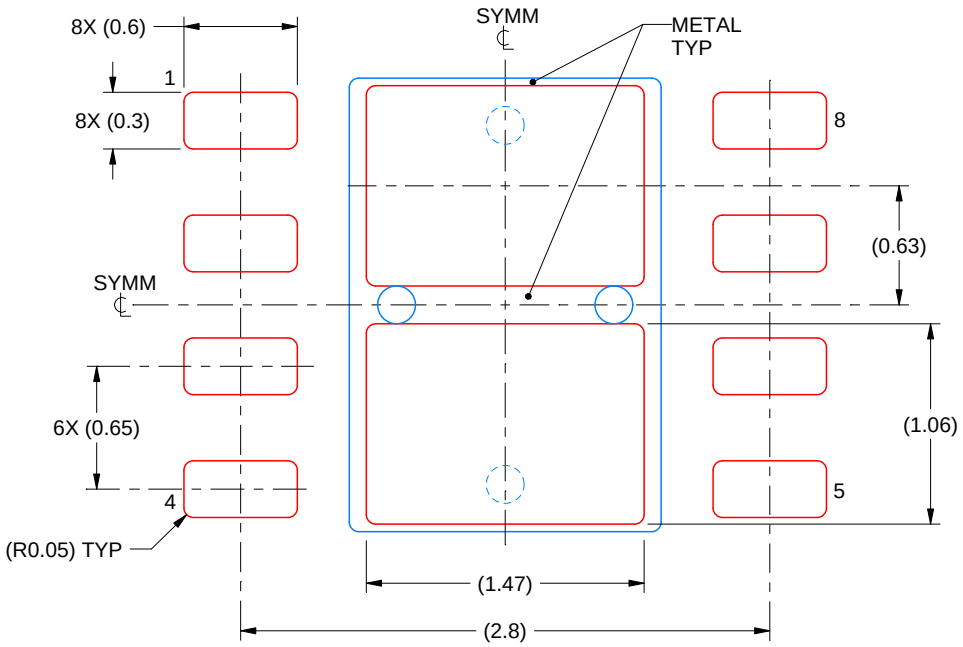


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

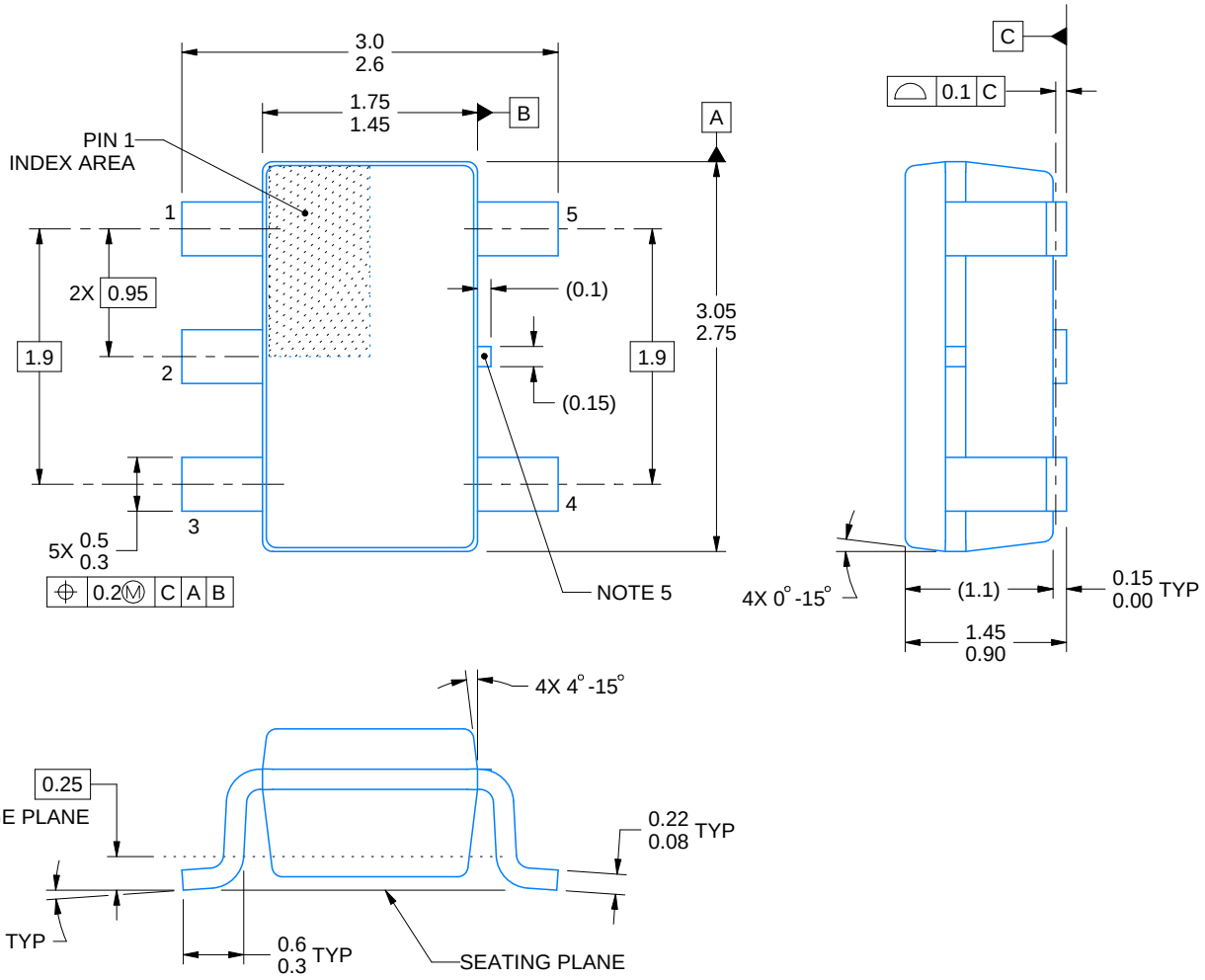
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

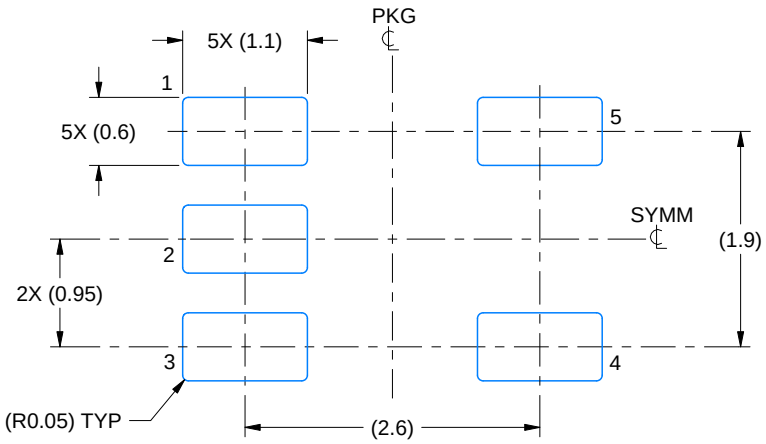
SMALL OUTLINE TRANSISTOR



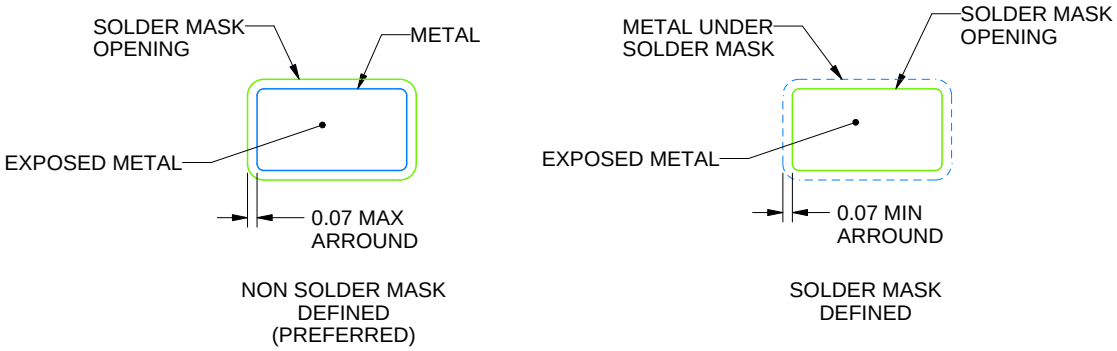
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

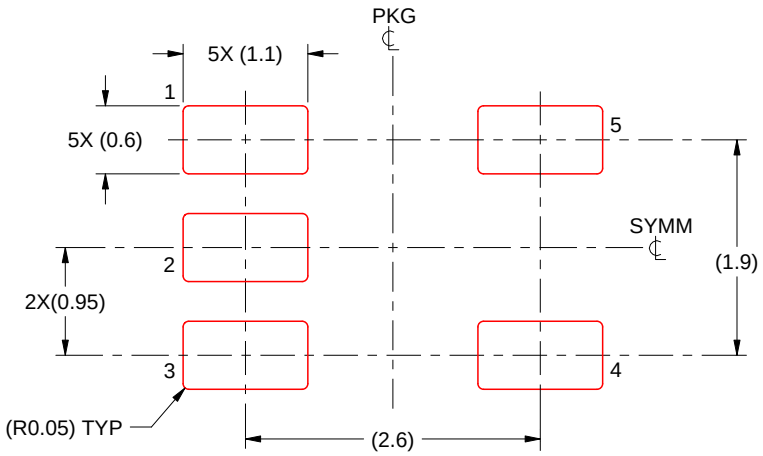


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

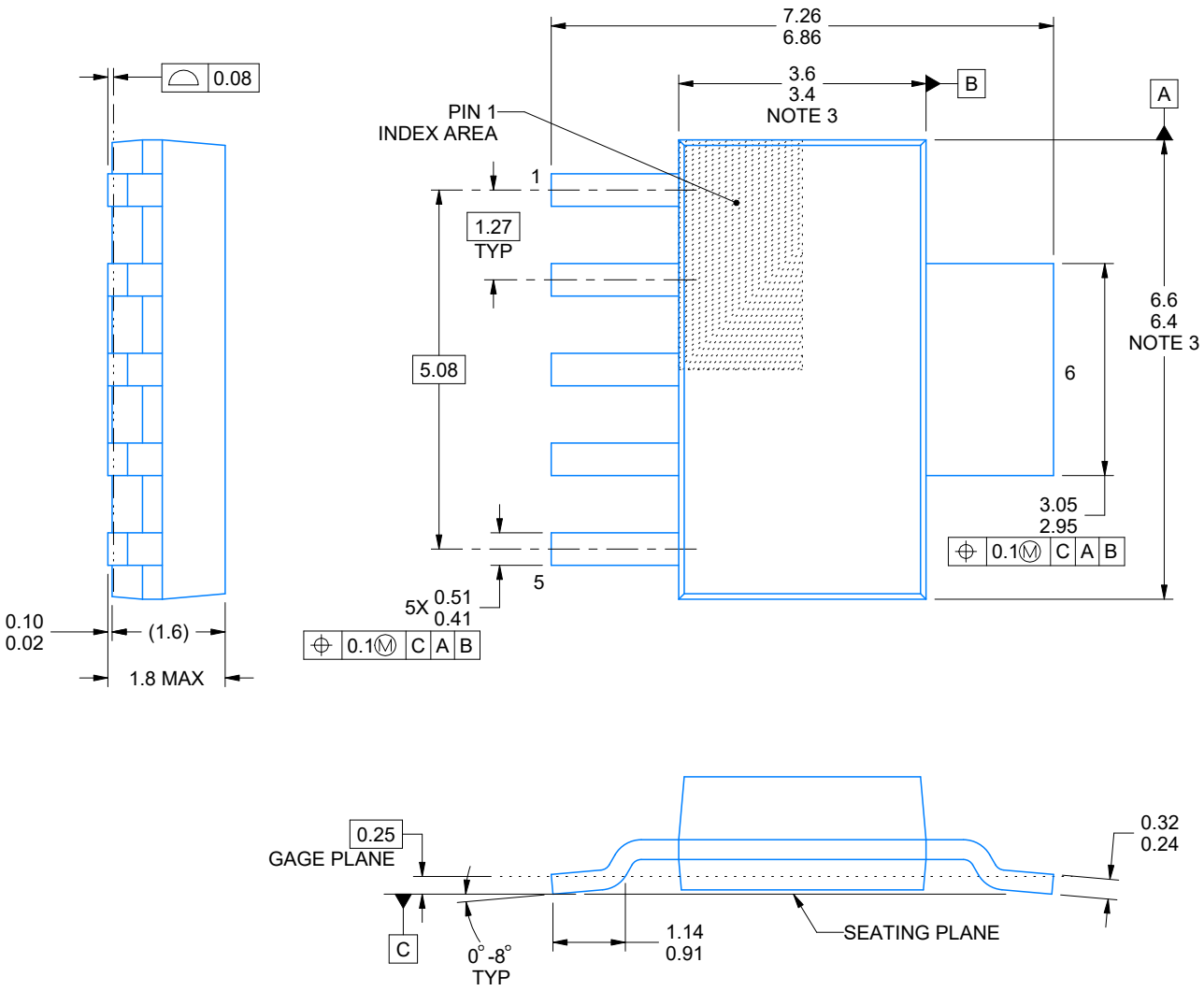
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

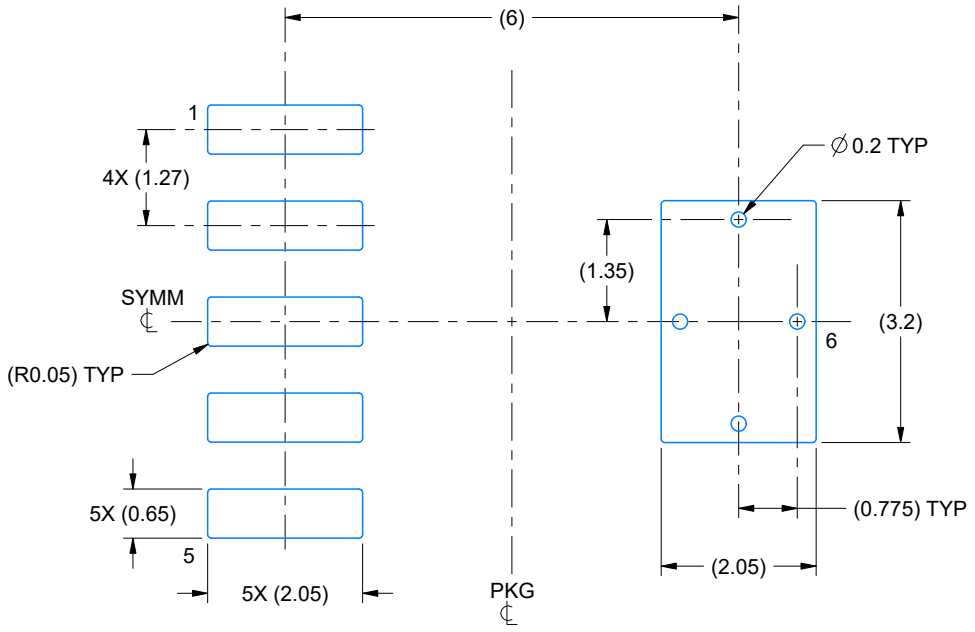
PLASTIC SMALL OUTLINE



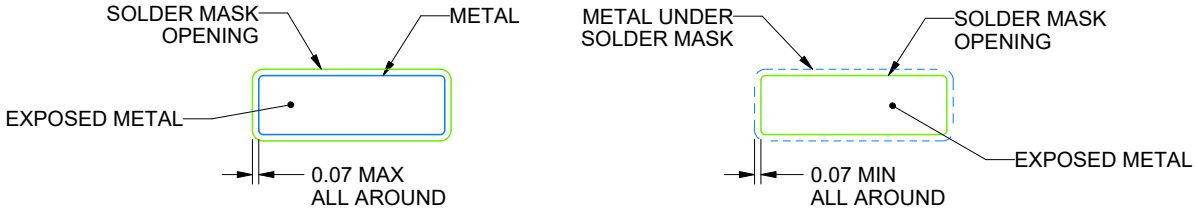
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

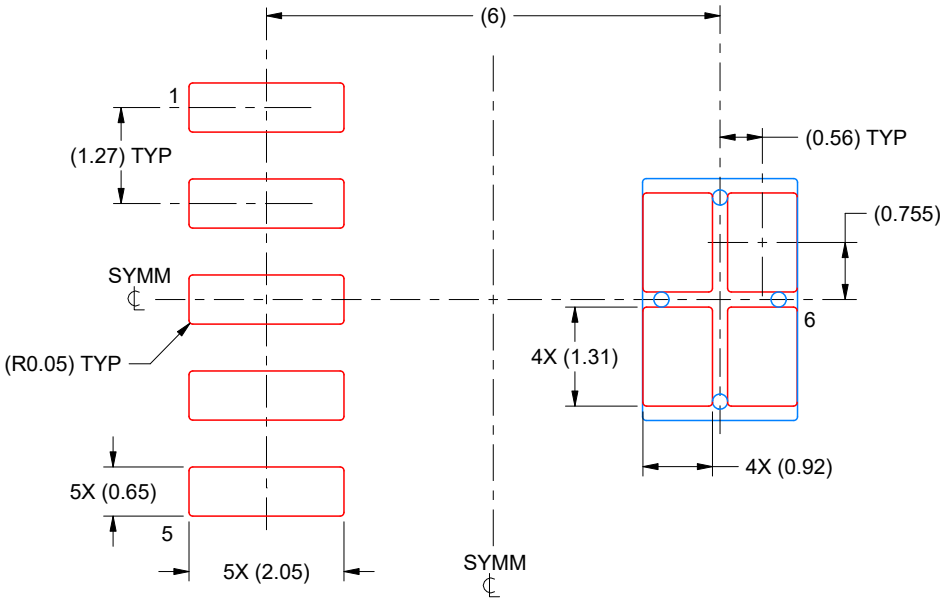


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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