Technical Article

Generating Bias Current Networks with Arbitrary Magnitudes - Part Two

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In the previous post in this series, an equation was derived to describe the ratio of the Nth R_{SET} resistor in Figure 1 below.

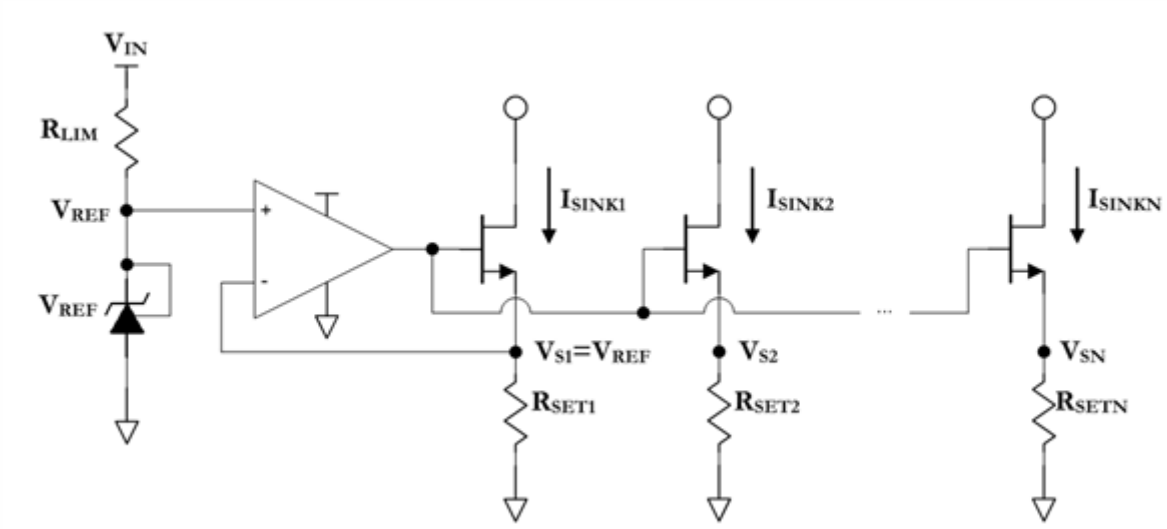

Figure 1. Current Sink Network

That equation, again, is as follows:

$$M_{RN} = M_{IN} \times \left[\left(1 - \sqrt{M_{IN}}\right) \times \left(1 + \sqrt{\frac{2}{K_n \times R_{SET1} \times V_{REF}}}\right) + \sqrt{M_{IN}}\right]^{-1} \quad (1)$$

So, what can be said about Equation 1? First of all, for an M_{IN} ratio of 1, the corresponding M_{RN} ratio will also be 1, as would be expected. Second, for values of M_{IN} greater than 1, notice that the two terms of the denominator of Equation 1 take on different signs. This means that depending on certain physical quantities involved (K_n, R_{SET1}, V_{REF}), M_{RN} can become arbitrarily large. Thus, this region should be avoided, instead favoring the $M_{IN} \leq 1$ region; that is, by ensuring that I_{SINKN} is less than or equal to I_{SINK1} for all N.

Notice that allowing the denominator of the root term in Equation 1 (the K_n, R_{SET1}, V_{REF} product) to become large results in a 1:1 linear relationship between M_{RN} and M_{IN} in the limit. Ultimately, the range of usable values that V_{REF} and R_{SET1} can take on to increase this product are going to be limited by the headroom required for the sink; though it is worth noting that for a fixed I_{SINK1} value, increasing V_{REF} requires an increase in R_{SET1} as well. The final variable in the product, K_n, is the process transconductance of the MOSFET and can be maximized through device selection. The effect of K_n on the linearity of the M_{RN}, M_{IN} relationship (across five decades of K_n values) is illustrated in Figure 2 below.

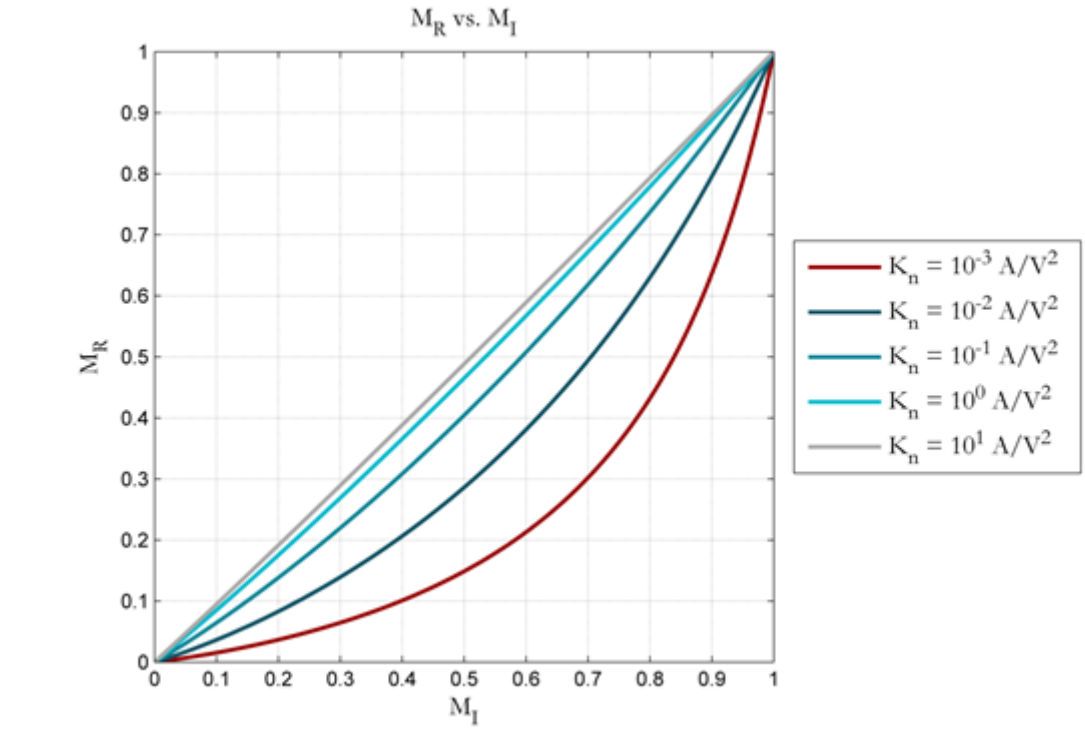

Figure 2. Resistor Ratio vs. Current Ratio across Process Transconductance

The process transconductance is so named due to its dependence on carrier mobility, oxide permittivity, and oxide thickness (μ, ε_{ox}, t_{ox})—all material and process properties:

$$K_n = {k_n}^1 \, x \, \frac{W}{L} = \mu_n \, x \, C_{ox} \, x \, \frac{W}{L} = \mu_n \, x \, \frac{E_{ox}}{t_{ox}} \, x \, \frac{W}{L} \tag{2}$$

However, it is also dependent on the W/L ratio of the device, so in general larger devices will result in increasingly linear behavior in Equation 1. While most datasheets will not include K_n, it can be calculated from a common datasheet parameter, the forward transconductance, often listed as g_m or g_{FS}:

$$g_m = g_{FS} = \frac{\partial I_{Dn}}{\partial V_{GS}} = \frac{\partial}{\partial V_{GS}} \left(\frac{1}{2} \, x \, K_n \, x \, (V_{GS} - V_T)^2 \right) = K_n \, x \, (V_{GS} - V_T) \tag{3}$$

Recall that the drain current equation for an NMOS operating in the saturation region is:

$$I_{Dn} = \frac{1}{2} \, x \, K_n \, x \, (V_{GS} - V_T)^2 \, x \, (1 + \lambda \, x \, V_{DS}) \tag{4}$$

Neglecting channel length modulation and rewriting the terms of Equation 4:

$$V_{GS} - V_T = \sqrt{\frac{2 \, x \, I_D}{K_n}} \tag{5}$$

This result can be substituted into Equation 3 and ultimately solved for K_n:

$$g_m = K_n \, x \sqrt{\frac{2 \, x \, I_D}{K_n}} = \sqrt{2 \, x \, I_D \, x \, K_n} \tag{6}$$

$$K_n = \frac{{g_m}^2}{2 \, x \, I_D} \tag{7}$$

Thus, using Equation 7 it is possible to select optimal MOSFET devices for the bias network. Further, having obtained this value, it can be utilized in Equation 1 to calculate (more accurately) required R_{SETN} resistor values to produce desired I_{SINKN} currents.

It is important to note that Equation 1 tends to overestimate the R_{SETN} resistance in the $M_{IN} \leq 1$ region; that is, it results in currents that are lower than the desired value. However, the ideal transistor case ($M_{IN}=M_{RN}$) will always underestimate the R_{SETN} resistance in this region. Thus, calculating these two values will ultimately bound the exact value required. Consider two randomly chosen NFETs, N-channel MOSFET A and N-channel MOSFET B, as represented in Table 1, which have listed g_{FS} values of 5.5A/V^2 (at I_D=9A) and 15A/V^2 (at I_D=31A), respectively. Suppose these are used to implement an M_{IN} ratio of ¼; the corrected R_{SETN} and M_{RN} ratios are calculated using Equation 1 (along with some straightforward design values) in Table 1 below.

Table 1. Circuit Parameters and Calculated R_{SETN} And M_{RN} For M_{IN}=¼

	g_{FS} (S)	I_D (A)	K_N (A/V^2)	V_{REF} (V)	I_{SINK1} (A)	I_{SINKN} (A)	M_{IN}	R_{SET1} (Ω)	R_{SETN} (Ω)	M_{RN}
N-channel MOSFET A	5.5	9.0	1.68	1.25	1.0	0.25	0.25	1.25	7.18	0.174
N-channel MOSFET B	15.0	31.0	3.63	1.25	1.0	0.25	0.25	1.25	6.48	0.193

Using the conditions listed above for the N-channel MOSFET B, Figure 3 displays the results of a TINA-TI simulation of the circuit in Figure 1 implemented with R_{SETN} values calculated from the ideal case (5Ω under these conditions), the corrected case (Equation 1), and the average of these two.

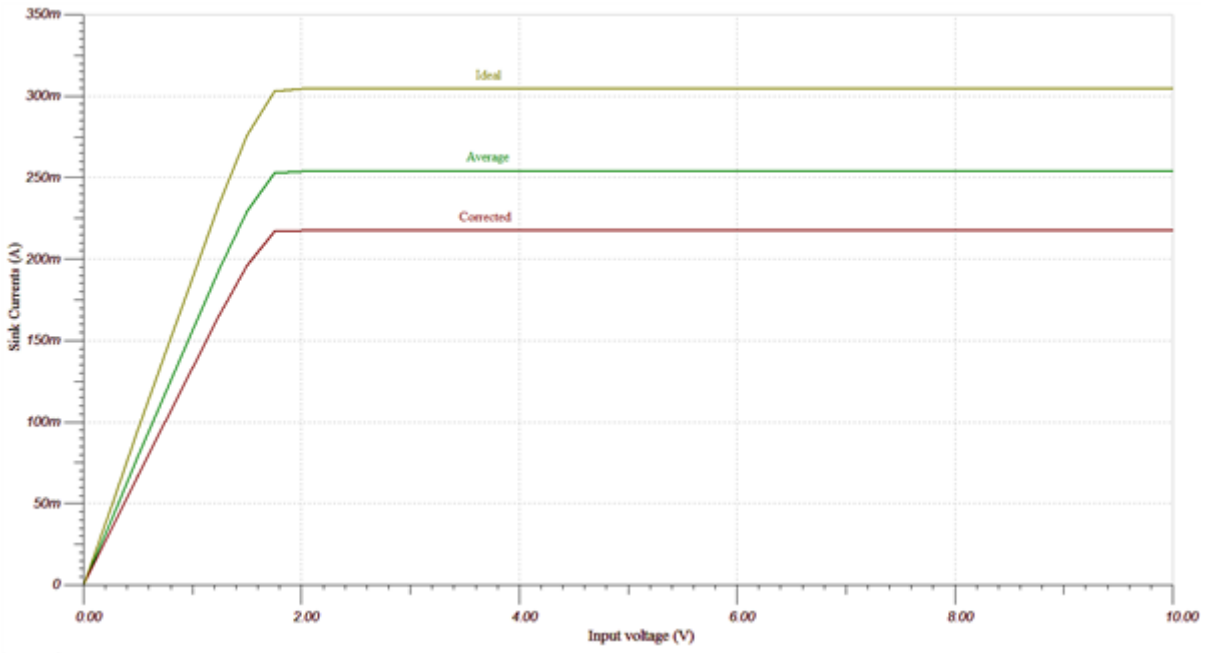

Figure 3. Sink Current vs. Drain Voltage for Ideal, Corrected, and Average R_{SETN} Values

The results for simulations using both the N-channel MOSFET A and N-channel MOSFET B with the three R_{SETN} values (as described above) are summarized along with corresponding percent error calculations in Table 2 below.

Table 2. R_{SETN} Calculation Methods and Resulting Accuracy

	Ideal			Corrected			Average		
	R_{SETN} (Ω)	I_{SINKN} (A)	Error (%)	R_{SETN} (Ω)	I_{SINKN} (A)	Error (%)	R_{SETN} (Ω)	I_{SINKN} (A)	Error (%)
N-channel MOSFET A	5.0	0.304	21.6	7.2	0.218	-12.8	6.1	0.254	1.5
N-channel MOSFET B	5.0	0.283	13.2	6.5	0.221	-11.6	5.7	0.248	-0.8

Ultimately a single feedback device can be used to derive a bias network of arbitrary values so long as certain conditions are met: particularly that the current in the primary feedback driven leg is the largest in the network, and the proper headroom is maintained in each leg. Thus, from a single voltage reference, a bias network is established.

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