UCC23525 5A ソース、5A シンク、5kV$_{RMS}$ 強化絶縁、フォトカプラ互換、シングル チャネル絶縁型ゲート ドライバ

1 特長

- フォトカプラ互換入力付き 5kV$_{RMS}$ シングル チャネル絶縁型ゲートドライバ
- 光絶縁型ゲートドライバに対して、ピン互換で置き換え可能
- ソース 5A、シンク 5A のピーク出力電流
- 最大 36V の出力ドライバ電源電圧
- 12V VDD 低電圧ロックアウト
- レール ツー レール出力
- 伝搬遅延:100ns 以下
- 部品間遅延ばらつき:25ns 以下
- パルス幅歪み:30ns 以下
- 同相過渡耐性 (CMTI):200kV/µs 以上
- 絶縁バリアの寿命:>50 年
- 沿面距離と空間距離が >8.5mm のストレッチ SO-6 パッケージ
- 動作時の接合部温度、T$_J$:-40℃～+150℃

2 アプリケーション

- 産業用モータ制御ドライブ
- ソーラー インバータ
- 産業用電源、UPS
- 誘導加熱

3 概要

UCC23525 ドライバは、IGBT、MOSFET、SiC MOSFET 用の、フォトカプラ互換、シングル チャネル絶縁型ゲート ドライバです。ソース 5A、シンク 5A のピーク電流を出力でき、5kV$_{RMS}$ の 強化絶縁定格を持っています。電源電圧範囲が 30V と高いため、バイポーラ電源を使用して IGBT および SiC パワー FET を効果的に駆動できます。UCC23525 は、ローサイドとハイサイドの両方のパワー FET を駆動できます。主な機能と特性は、標準的なオプトカプラ ベースのゲートドライバに比べて性能と信頼性を大幅に向上させると同時に、回路設計とレイアウト設計の両方でピン互換性を維持しています。

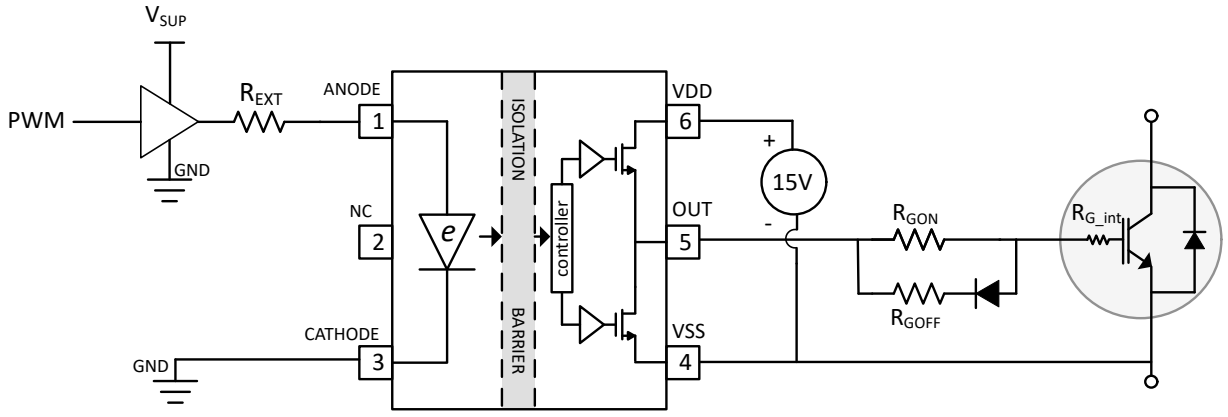
特に、高い同相過渡耐性 (CMTI)、低伝搬遅延、小さなパルス幅歪みは、性能の大きな特長です。厳密なプロセス制御により、部品間スキューも小さくなっています。入力段はダイオード エミュレーション (e-diode) であり、フォトカプラ ゲートドライバで使われている従来型 LED に比べて、長期的な信頼性と優れた経時特性を実現します。UCC23525 は、5kV$_{RMS}$ の強化絶縁定格に対応するストレッチ SO-6 パッケージで提供されます。ストレッチ SO-6 パッケージは、沿面距離と空間距離がどちらも >8.5mm であり、材料グループ I (比較トラッキング指数 (CTI) >600V のモールド コンパウンドを使用しています。

UCC23525 は高性能で信頼性が高いため、あらゆる種類のモータ ドライブ、ソーラー インバータ、産業用電源、家電機器に理想的 です。高い温度で動作するため、従来のフォトカプラでは対応できなかったアプリケーションで活用する機会が広がります。

製品情報

部品番号	パッケージ (1)	UVLO レベル
UCC23525CDWYR	DWY (ストレッチ SO-6)	12V

(1) 供給されているすべてのパッケージについては、セクション 13 を参照してください。



代表的なアプリケーション回路図

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4 Pin Configuration and Function

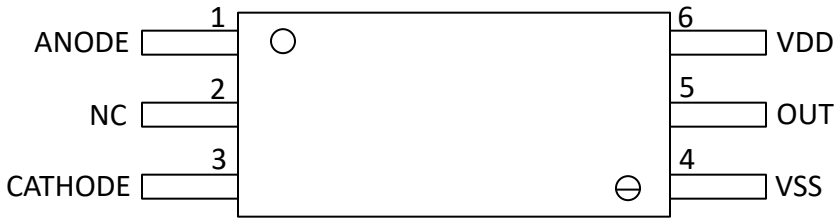

図 4-1. UCC23525 DWY Package SO-6 Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
ANODE	1	I	Anode
CATHODE	3	I	Cathode
NC	2	-	No Connection
VDD	6	P	Positive output supply rail
VSS	4	P	Negative output supply rail
OUT	5	O	Gate-drive output

(1) P = Power, G = Ground, I = Input, O = Output

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5 Specifications

5.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input Steady State Forward Current	$I_{F(DC)}$	-	25	mA
Peak Transient Input Current	$I_{F(TRAN)}$ <1us pulse, 300pps		1	A
Reverse Input Voltage	$V_{R(MAX)}$		6	V
Output supply voltage	V_{DD} – V_{SS}	-0.3	36	V
Output DC Steady State Voltage	$V_{OUT(DC)}$	V_{SS}-0.5	V_{DD}+0.5	V
Output Transient Voltage	$V_{OUT(TRAN)}$	V_{SS}-5	V_{DD}+5	V
Junction temperature	T_J (2)	-40	150	°C
Storage temperature	T_{stg}	-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) To maintain the recommended operating conditions for T_J, see Section 6.5 Power Ratings.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Output Supply Voltage(V_{DD} – V_{SS}) - 12V UVLO	13		30	V
I_F (ON)	Input Diode Forward Current (Diode "ON")	5		20	mA
V_F (OFF)	Anode voltage - Cathode voltage (Diode "OFF")	-5		0.8	V
T_A	Ambient temperature	-40		125	°C
T_J	Junction temperature	-40		150	°C

5.4 Thermal Information

THERMAL METRIC(1)		UCC23525 SO6 6 Pins	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	138	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	79.2	°C/W
R_{qJB}	Junction-to-board thermal resistance	76.4	°C/W
Y_{JT}	Junction-to-top characterization parameter	44.9	°C/W
Y_{JB}	Junction-to-board characterization parameter	72.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation on input and output(1)	V_{DD} - V_{SS} = 20 V, C_{Load}=2.2-nF, I_F= 20mA, T_A=25ºC, F_{SW}=780-kHz, 50% duty cycle, square wave			750	mW
P_{D1}	Maximum input power dissipation(2)				20	mW
P_{D2}	Maximum output power dissipation				730	mW

(1) Derate at 8 mW/°C beyond 25°C ambient temperature
(2) Recommended maximum P_{D1} = 40mW. Absolute maximum P_{D1} = 50mW

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5.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
General				
CLR	External clearance (1)	Shortest terminal-to-terminal distance through air	>8.5	mm
CPG	External Creepage (1)	Shortest terminal-to-terminal distance across the package surface	>8.5	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>17	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material Group	According to IEC 60664-1	I	
	Overvoltage category	Rated mains voltage ≤ 600 V_{RMS}	I-III	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	
DIN EN IEC 60747-17 (VDE 0884-17) (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test	1063	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7071	V_{PK}
V_{IMP}	Maximum inpulse voltage (3)	Tested in air, 1.2/50-µs waveform per IEC 62368-1	7692	V_{PK}
V_{IOSM}	Maximum surge isolation voltage (4)	$V_{IOSM} \geq 1.3 \times V_{IMP}$;Tested in oil (qualification test), 1.2/50-µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge (5)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1: At routine test (100% production) and preconditioning (type test): $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	
C_{IO}	Barrier capacitance, input to output (6)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	1	pF
R_{IO}	Insulation resistance, input to output (6)	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed-circuit board are used to help increase these specifications.
(2) UCC23525 is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier tied together creating a two-pin device.

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5.7 Safety Limiting Values

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	R_{qJA} = 138°C/W, V_{DD} - V_{SS} = 15 V, T_J = 150°C, T_A = 25°C			59	mA
		R_{qJA} = 138°C/W, V_{DD} - V_{SS} = 25 V, T_J = 150°C, T_A = 25°C			35	
P_S	Safety input, output, or total power	R_{qJA} = 138°C/W, T_J = 150°C, T_A = 25°C			900	mW
T_S	Maximum safety temperature(1)				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J , specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively. The maximum limits of I_S and P_S should not be exceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, R_{qJA}, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{qJA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{qJA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum supply voltage.

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5.8 Electrical Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at TA = 25°C, VDD–VSS= 15V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
I_{FLH}	Input Forward Threshold Current Low to High	V_{DD} - V_{SS} = 15V		1	2.5	mA
V_F	Input Forward Voltage	I_F =10 mA	1.4	1.7	2	V
$\Delta V_F/\Delta T$	Temp Coefficient of Input Forward Voltage	I_F =10 mA		0.7		mV/ºC
V_R	Input Reverse Breakdown Voltage	I_R= 10 uA	6			V
C_{IN}	Input Capacitance	F = 0.5 MHz		4		pF
OUTPUT						
I_{OH}	Output Peak Source Current	C_{Load}=220nF		-5		A
I_{OL}	Output Peak Sink Current	C_{Load}=220nF		5		A
R_{OH}	Output Pull-up Resistance	I_O = -1A		2.5	3.5	Ω
R_{OL}	Output Pull-down Resistance	I_O = 1A		0.7	1.5	Ω
I_{DD_H}	Output Supply Current (Diode On)	I_F = 10 mA, I_O= 0 mA			2.2	mA
I_{DD_L}	Output Supply Current (Diode Off)	V_F = 0 V, I_O= 0 mA			2	mA
UNDER VOLTAGE LOCKOUT						
$UVLO_R$	Under Voltage Lockout V_{DD} rising (12V UVLO)	I_F=10 mA	11.4	12	12.6	V
$UVLO_F$	Under Voltage Lockout V_{DD} falling (12V UVLO)	I_F=10 mA	10.45	11	11.55	V
$UVLO_{HYS}$	UVLO Hysteresis (12V UVLO)	I_F=10 mA		1.0		V
$V_{DD\_UVLO\_FIL}$	VDD UVLO Deglitch Time	V_{DD}>5.3V		5		µs

5.9 Switching Characteristics

Over recommended operating conditions unless otherwise noted. All typical values are at T_A = 25°C, VDD–VSS= 15V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output-signal Rise Time	C_{Load} = 1.8nF, V_{DD}=15V, 20% to 80%		5		ns
t_f	Output-signal Fall Time	C_{Load} = 1.8nF, V_{DD}=15V, 90% to 10%		11		ns
t_{PLH}	Propagation Delay, Low to High	C_{Load} = 1.8nF, V_{DD}=15V, I_F=10mA F_{SW} = 20 kHz, (50% Duty Cycle) measure with Input I_{FLH} to output 10%			100	ns
t_{PHL}	Propagation Delay, High to Low	C_{Load} = 1.8nF, V_{DD}=15V, I_F=10mA F_{SW} = 20 kHz, (50% Duty Cycle) measure with Input I_{FLH} to output 90%			100	ns
t_{PWD}	Pulse Width Distortion $\lvert t_{PHL} - t_{PLH} \rvert$	C_{Load} = 1.8nF, V_{DD}=15V, I_F=10mA F_{SW} = 20 kHz, (50% Duty Cycle)			30	ns
$t_{sk(pp)}$	Part-to-Part Skew in Propagation Delay Between any Two Parts(1)	C_{Load} = 1.8nF, V_{DD}=15V, I_F=10mA F_{SW} = 20 kHz, (50% Duty Cycle)			25	ns
$t_{UVLO\_HI\_OUT}$	VDD UVLO HI Delay to OUT 10% HI	I_F=10mA	2	5	8	µs
$t_{UVLO\_LO\_OUT}$	VDD UVLO LO Delay to OUT 90% LO	I_F=10mA, V_{DD}>6.2V		6	10	µs
$CMTI_H$	Common-mode Transient Immunity (Output High)(2)	I_F = 10 mA, V_{CM} = 1000 V	200			V/ns
$CMTI_L$	Common-mode Transient Immunity (Output Low) (2)	V_F = 0 V, V_{CM} = 1000 V	200			V/ns
t_{PWmin}	Minimum Input Pulse Width That Passes to Output	C_{Load} = 1.8nF, V_{DD}=15V, I_F=10mA	9	12	43	ns

(1) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads ensured by characterization.

(2) For best CMTI performance, we recommend connecting single resistor to the Anode pin, and connecting Cathode pin directly to GND.

5.10 Thermal Derating Curves

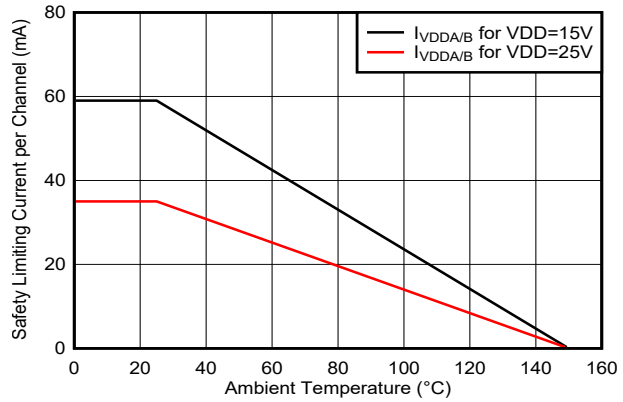


図 5-1. Thermal Derating Curve for Safety Limiting Current

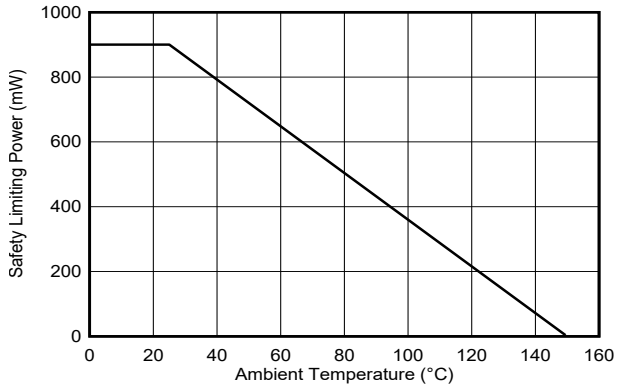
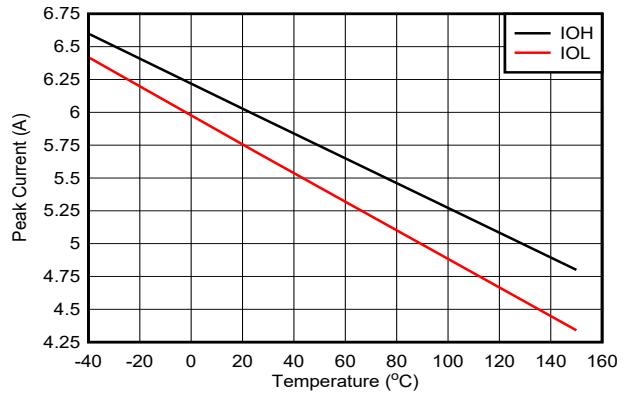


図 5-2. Thermal Derating Curve for Safety Limiting Power

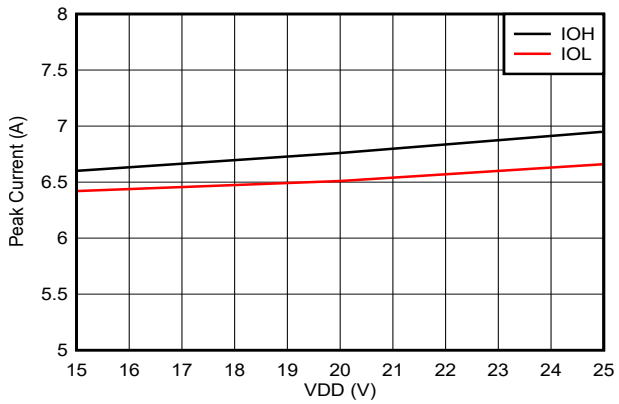
5.11 Typical Characteristics

V_{DD}= 15 V, 1-µF capacitor from V_{DD} to V_{SS}, C_{Load} = 1.8 nF for timing tests and 220nF for I_{OH} and I_{OL} tests, T_J = –40°C to +150°C, (unless otherwise noted)



C_{LOAD} = 220-nF

図 5-3. Output Drive currents versus Temperature



C_{LOAD} = 220-nF, T_A = 25°C

図 5-4. Output Drive currents versus VDD

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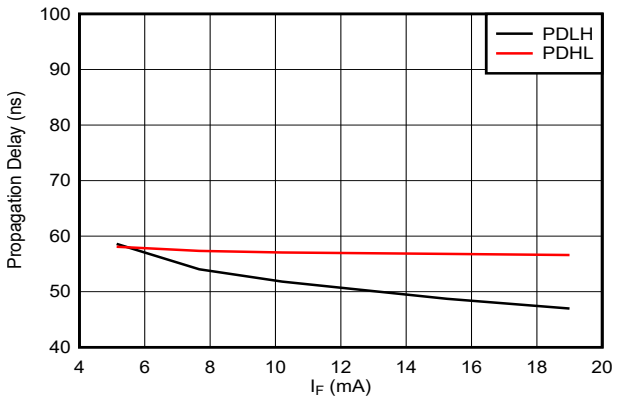
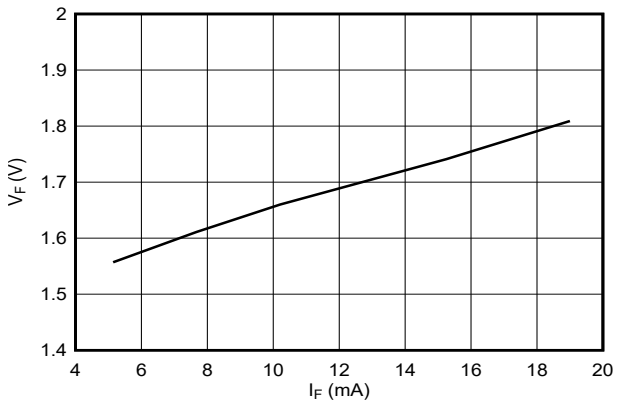
5.11 Typical Characteristics (continued)

V_{DD}= 15 V, 1-µF capacitor from V_{DD} to V_{SS}, C_{Load} = 1.8 nF for timing tests and 220nF for I_{OH} and I_{OL} tests, T_J = –40°C to +150°C, (unless otherwise noted)



C_{LOAD} = 1.8-nF, T_A = 25°C

図 5-5. Propagation delay versus Forward current



T_A = 25°C

図 5-6. Forward voltage drop versus Forward current

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6 Parameter Measurement Information

6.1 Propagation Delay, Rise Time and Fall Time

図 6-1 shows the propagation delay from the input forward current I_F, to V_{OUT}. This figures also shows the circuit used to measure the rise (t_r) and fall (t_f) times and the propagation delays t_{PDLH} and t_{PDHL}.

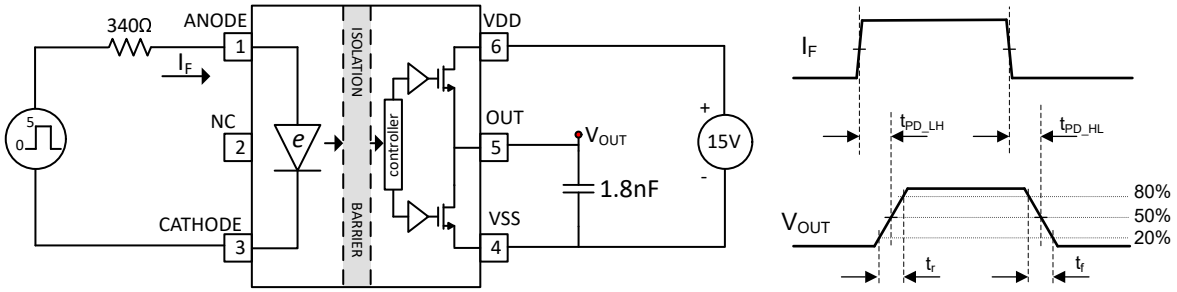

図 6-1. I_F to V_{OUT} Propagation Delay, Rise Time and Fall Time

6.2 I_{OH} and I_{OL} Testing

図 6-2 shows the circuit used to measure the output drive currents I_{OH} and I_{OL}. A load capacitance of 220nF is used at the output. The current is measured using high bandwidth current shunt placed between the V_{OUT} pin and the load to determine the peak source and sink currents of the gate driver.

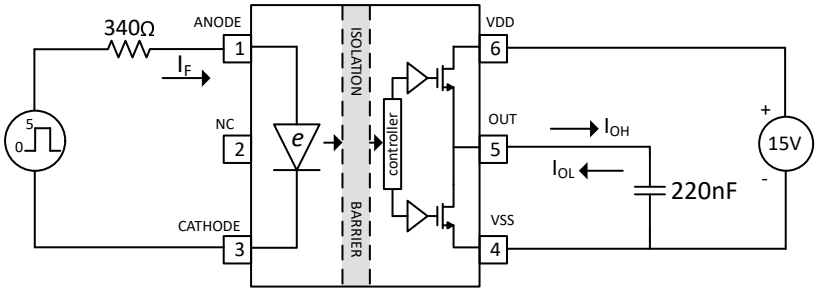

図 6-2. I_{OH} and I_{OL}

6.3 CMTI Testing

図 6-3 is the simplified diagram of the CMTI testing. Common mode voltage is set to 1000V. The test is performed with I_F = 10mA (VOUT= High) and I_F = 0mA (V_{OUT} = LOW). The diagram also shows the fail criteria for both cases. During the application on the CMTI pulse with I_F = 10mA, if V_{OUT} drops from VDD to ½VDD it is considered as a failure. With I_F= 0mA, if V_{OUT} rises above 1V, it is considered as a failure.

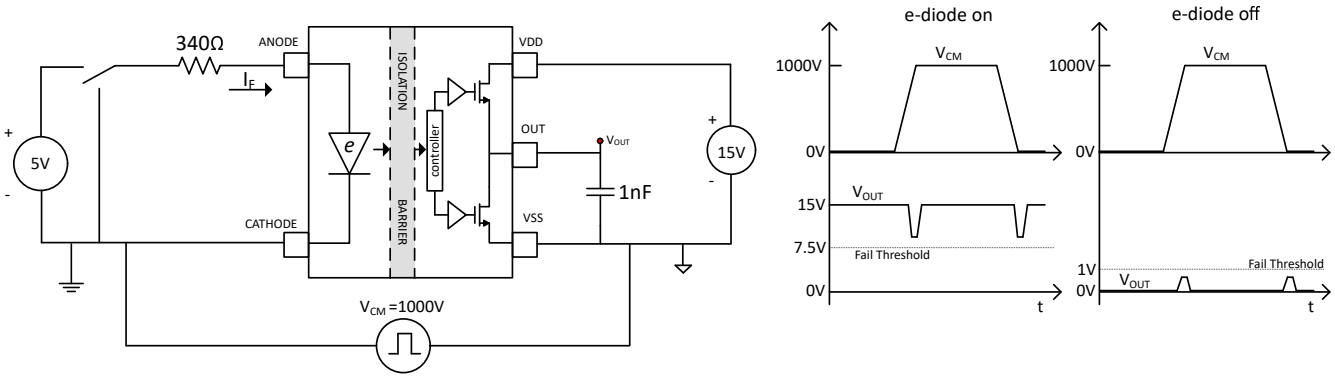

図 6-3. CMTI Test Circuit for UCC23525

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7 Detailed Description

7.1 Overview

UCC23525 is a single channel isolated gate driver, with an opto-compatible input stage, that can drive IGBTs, MOSFETs and SiC FETs. It has 5A peak output current capability with max output driver supply voltage of 30V. The inputs and the outputs are galvanically isolated. UCC23525 is offered in an industry standard 6 pin (SO6) package with >8.5mm creepage and clearance. It has a working voltage of 1063-V_{RMS}, reinforced isolation rating of 5-kV_{RMS} for 60s and a surge rating of 10-kV_{PK}. It is pin-to-pin compatible with standard opto isolated gate drivers. While standard opto isolated gate drivers use an LED as the input stage, UCC23525 uses an emulated diode (or "e-diode") as the input stage which does not use light emission to transmit signals across the isolation barrier. The input stage is isolated from the driver stage by TI's proprietary silicon dioxide-based (SiO2) isolation barrier, that not only provides reinforced isolation but also offers superior common mode transient immunity of > 100 kV/us. The e-diode input stage along with silicon dioxide isolation barrier technology gives UCC23525 several performance advantages over standard opto isolated gate drivers. They are as follows:

1. Since the e-diode does not use light emission for its operation, the reliability and aging characteristics of UCC23525 are naturally superior to those of standard opto isolated gate drivers.
2. Higher ambient operating temperature range of 125°C, compared to only 105°C for most opto isolated gate drivers
3. The e-diode forward voltage drop has less part-to-part variation and smaller variation across temperature. Hence, the operating point of the input stage is more stable and predictable across different parts and operating temperature.
4. Higher common mode transient immunity than opto isolated gate drivers
5. Smaller propagation delay than opto isolated gate drivers
6. Due to superior process controls achievable in the SiO2 isolation compared to opto isolation, there is less part-to-part skew in the prop delay, making the system design simpler and more robust
7. Smaller pulse width distortion than opto isolated gate drivers

The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see 図 7-1). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC23525 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. 図 7-2 shows conceptual detail of how the OOK scheme works.

7.2 Functional Block Diagram

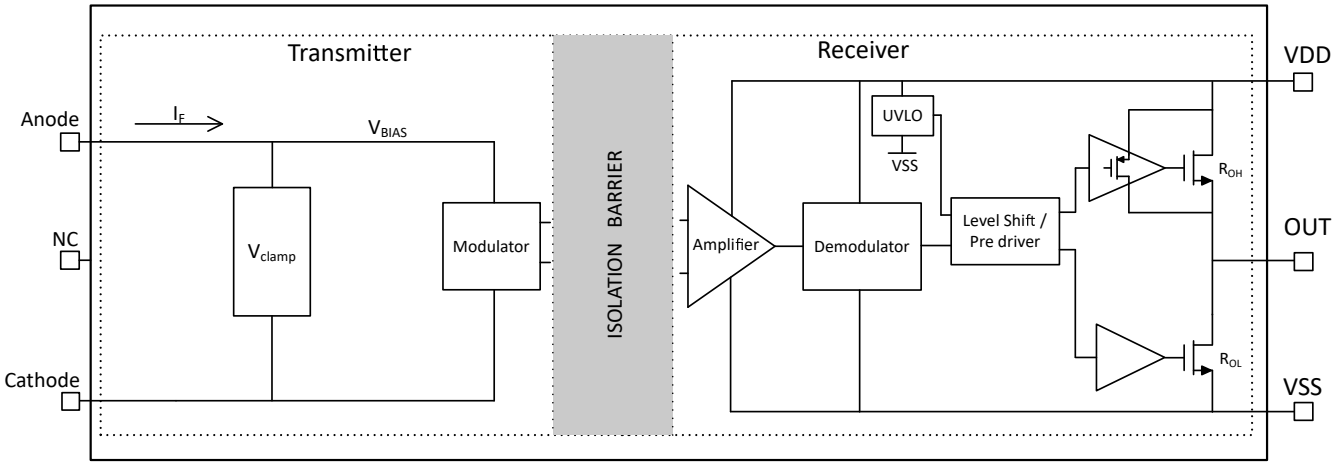

図 7-1. Conceptual Block Diagram of a Isolated Gate Driver with an Opto Emulated Input Stage (SO6 pkg)

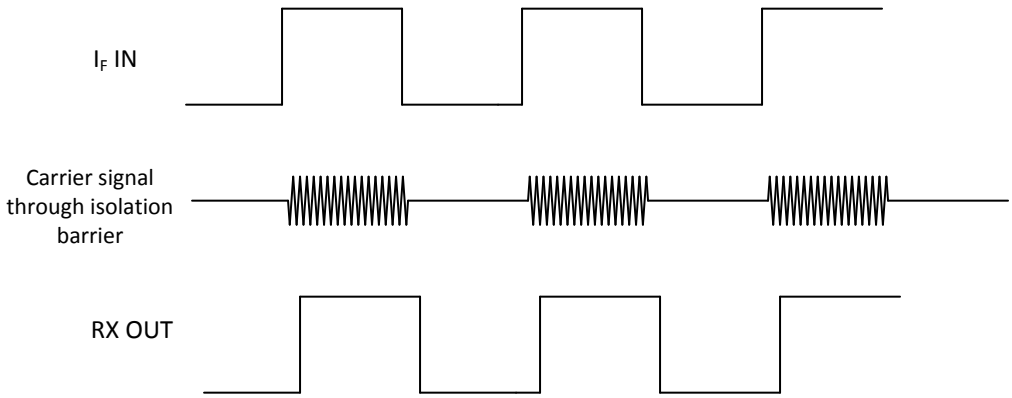

図 7-2. On-Off Keying (OOK) Based Modulation Scheme

7.3 Feature Description

7.3.1 Power Supply

Since the input stage is an emulated diode, no power supply is needed at the input.

The output supply, VDD, supports a voltage range from 13V to 30V. For operation with bipolar supplies, the power device is turned off with a negative voltage on the gate with respect to the emitter or source. This configuration prevents the power device from unintentionally turning on because of current induced from the Miller effect. The typical values of the V_{DD} and V_{SS} output supplies for bipolar operation are 15V and -8V with respect to GND for IGBTs, and 18V and -5V for SiC MOSFETs.

For operation with unipolar supply, the VDD supply is connected to 15V with respect to GND for IGBTs, and 18V for SiC MOSFETs. The VSS supply is connected to 0V.

7.3.2 Input Stage

The input stage of UCC23525 is simply the e-diode and therefore has an Anode (Pin 1) and a Cathode (Pin 3). Pin 2 has no internal connection and can be left open or connected to ground. The input stage does not have a power and ground pin. When the e-diode is forward biased by applying a positive voltage to the Anode with respect to the Cathode, a forward current I_F flows into the e-diode. The forward voltage drop across the e-diode is 1.7V (typ). An external resistor should be used to limit the forward current. The recommended range for the forward current is 5mA to 20mA. When I_F exceeds the threshold current I_{FLH}(1mA typ.) a high frequency signal is transmitted across the isolation barrier. The HF signal is detected by the receiver and V_{OUT} is driven high. See セクション 8.2.2.1 for information on selecting the input resistor. The dynamic impedance of the e-diode is very small(<1.0Ω) and the temperature coefficient of the e-diode forward voltage drop is <0.7mV/°C. This leads to excellent stability of the forward current I_F across all operating conditions. If the Anode voltage drops below V_{F_HL} (0.8V), or reverse biased, the gate driver output is driven low. The reverse breakdown voltage of the e-diode is >6V. So for normal operation, a reverse bias of up to 5V is allowed. The large reverse breakdown voltage of the e-diode enables UCC23525 to be operated in interlock architecture (see example in 図 7-3) where V_{SUP} can be as high as 5V. The system designer has the flexibility to choose a 3.3V or 5.0V signal source to drive the input stage of UCC23525 using an appropriate input resistor. The example shows two gate drivers driving a set of IGBTs. The inputs of the gate drivers are connected as shown and driven by two buffers that are controlled by the microcontroller unit (MCU). Interlock architecture prevents both the e-diodes from being "ON" at the same time, preventing shoot through in the IGBTs. It also ensures that if both PWM signals are erroneously stuck high (or low) simultaneously, both gate driver outputs will be driven low.

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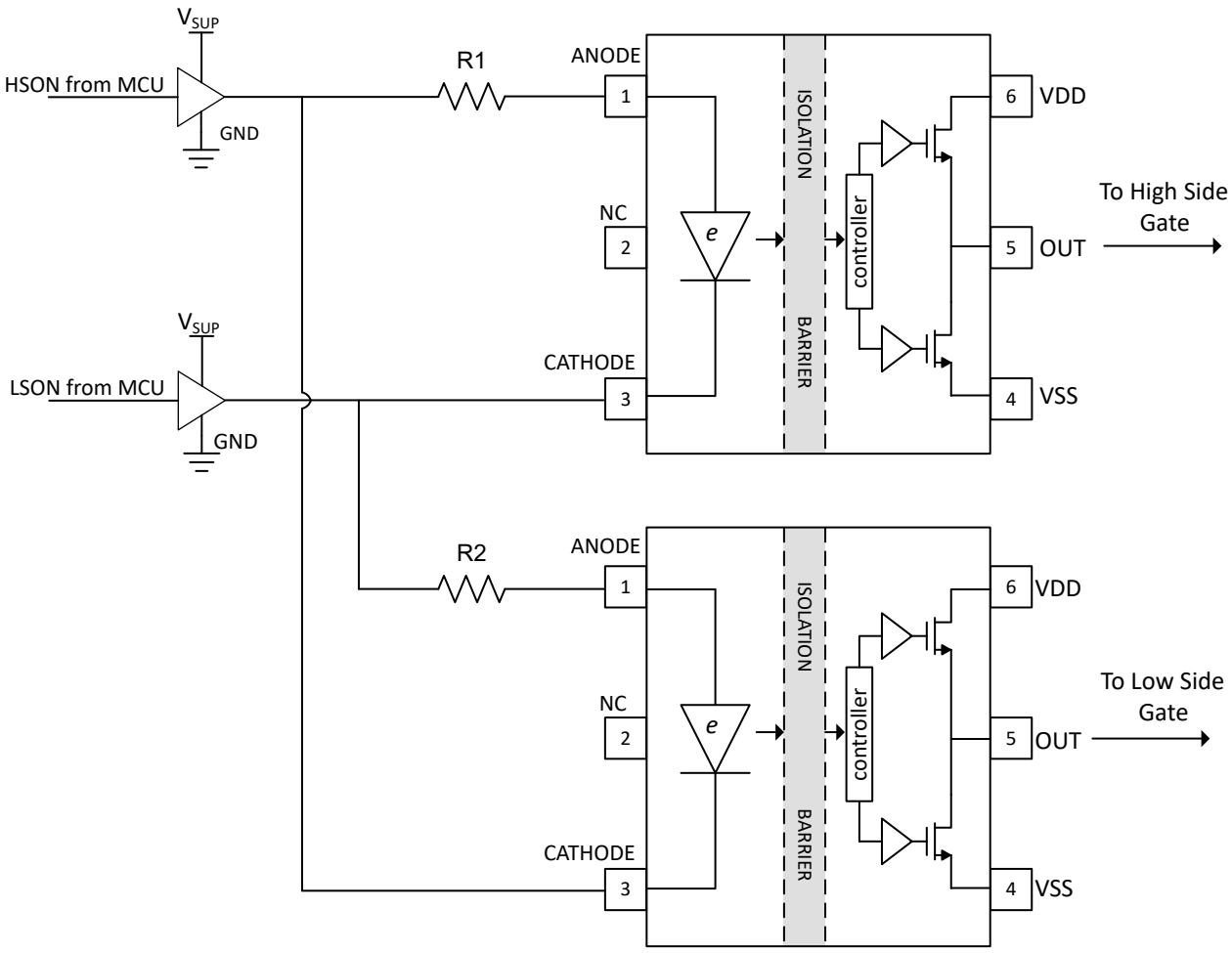

図 7-3. Interlock

7.3.3 Output Stage

The device has ±5-A peak drive strength and is suitable for high power applications. The high drive strength can drive a SiC MOSFET module, IGBT module or paralleled discrete devices directly without extra buffer stage. The device can also be used to drive higher power modules or parallel modules with extra buffer stage. Regardless of the values of VDD, the peak sink and source current can be kept at 5 A. The driver features an important safety function wherein, when the input pins are in floating condition, the OUT is held in low state. The output stage of the driver stage is depicted in 図 7-4. The driver has rail-to-rail output by implementing an NMOS pull-up with intrinsic bootstrap gate drive. Under DC conditions, a PMOS is used to keep OUT tied to VDD as shown in the figure. The low pullup impedance of the NMOS results in strong drive strength during the turn-on transient, which shortens the charging time of the input capacitance of the power semiconductor and reduces the turn on switching loss.

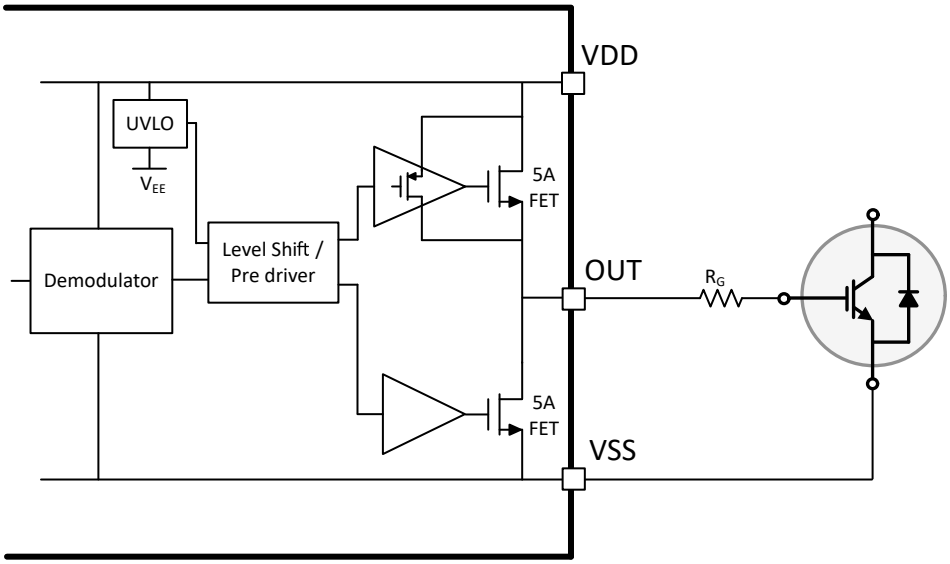

図 7-4. Output Stage

7.3.4 Protection Features

7.3.4.1 Undervoltage Lockout (UVLO)

UVLO function is implemented for VDD and VSS pins to prevent an under-driven condition on IGBTs and MOSFETs. When V_{DD} is lower than $UVLO_R$ at device start-up or lower than $UVLO_F$ after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input forward current as shown in 表 7-1. The VDD UVLO protection has a hysteresis feature ($UVLO_{hys}$). This hysteresis prevents chatter when the power supply produces ground noise which allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly.

When V_{DD} drops below $UVLO_F$, a delay, t_{UVLO_rec} occurs on the output when the supply voltage rises above $UVLO_R$ again.

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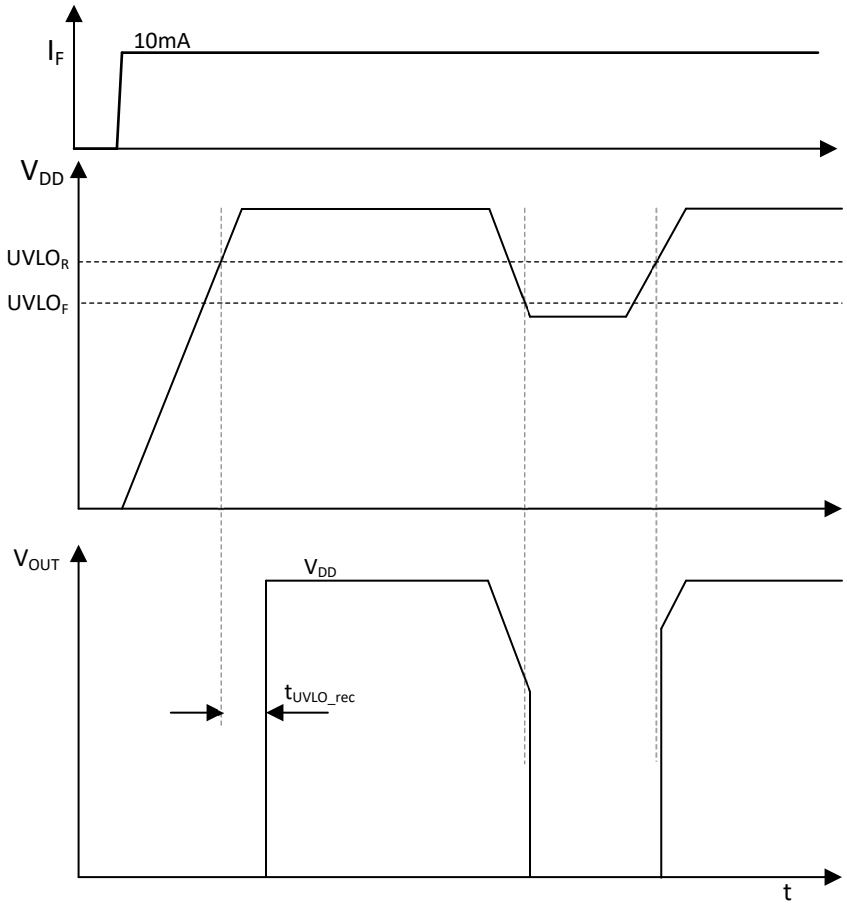

図 7-5. UVLO functionality

7.3.4.2 Active Pulldown

The active pull-down function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the VDD supply. This feature prevents false IGBT and MOSFET turn-on by clamping VOUT pin to approximately 2V.

7.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the output pin voltage V_{OUT} slightly higher than the V_{DD} voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the VDD pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10 µs and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

7.3.4.4 ESD Structure

図 7-6 shows the multiple diodes involved in the ESD protection components of the UCC23525 device. This provides pictorial representation of the absolute maximum rating for the device.

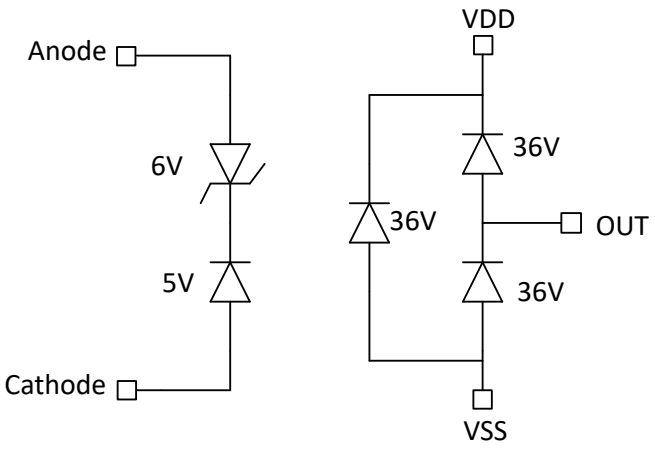

図 7-6. ESD Structure

7.4 Device Functional Modes

表 7-1 lists the functional modes for UCC23525.

表 7-1. Function Table for UCC23525 with V_{DD} Rising

e-diode	V_{DD}	V_{OUT}
OFF (I_F< I_{FLH})	0V - 30V	Low
ON (I_F> I_{FLH})	0V - $UVLO_R$	Low
ON ((I_F> I_{FLH})	$UVLO_R$ - 30V	High

表 7-2. Function Table for UCC23525 with V_{DD} Falling

e-diode	V_{DD}	V_{OUT}
OFF (I_F< I_{FLH})	0V - 30V	Low
ON (I_F> I_{FLH})	$UVLO_F$- 0V	Low
ON ((I_F> I_{FLH})	30V - $UVLO_F$	High

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8 Application and Implementation

注

以下のアプリケーションに関するセクションの情報は、TI の部品仕様の一部ではなく、TI はこれらの情報の正確性や完全性を保証しません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

UCC23525 is a single channel, isolated gate driver with opto-compatible input for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. It is intended for use in applications such as motor control, industrial inverters, and switched-mode power supplies. It differs from standard opto isolated gate drivers as it does not have an LED input stage. Instead of an LED, it has an emulated diode (e-diode). To turn the e-diode "ON", a forward current in the range of 5mA to 20mA should be driven into the Anode. This will drive the gate driver output high and turn on the power FET. Typically, MCU's are not capable of providing the required forward current. In this case, a buffer should be used between the MCU and the input stage of UCC23525. Typical buffer power supplies are either 5V or 3.3V. A resistor is needed between the buffer and the input stage of the UCC23525 to limit the current. It is simple, but important to choose the right value of resistance. The resistor tolerance, buffer supply voltage tolerance and output impedance of the buffer, have to be considered in the resistor selection. This will ensure that the e-diode forward current stays within the recommended range of 5mA to 20mA. Detailed design recommendations are given in the セクション 8.1. The current driven input stage offers excellent noise immunity that is need in high power motor drive systems, especially in cases where the MCU cannot be located close to the isolated gate driver. UCC23525 offers best in class CMTI performance of >200kV/us at 1000V common mode voltages.

The e-diode is capable of 25mA continuous in the forward direction. The forward voltage drop of the e-diode has a very tight part to part variation (1.4V min to 2V max). The temperature coefficient of the forward drop is <0.9mV/°C. The dynamic impedance of the e-diode in the forward biased region is ~1Ω. All of these factors contribute in excellent stability of the e-diode forward current. To turn the e-diode "OFF", the Anode - Cathode voltage should be <0.8V, or I_F should be <I_{FLH}. The e-diode can also be reverse biased up to 5V (6V abs max) in order to turn it off and bring the gate driver output low. The large reverse breakdown voltage of the input stage provides system designers the flexibility to drive the input stage with 5V PWM signals in interlock structure without the need for an additional clamping circuit on the Anode and Cathode pin.

The output power supply for UCC23525 can be as high as 30V (36V abs max). The output power supply can be configured externally as a single isolated supply up to 30V or isolated bipolar supply such that V_{DD}-V_{SS} does not exceed 30V, or it can be bootstrapped (with external diode & capacitor) if the system uses a single power supply with respect to the power ground. Maximum quiescent power supply current from V_{DD} is 2.2mA.

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8.2 Typical Application

The circuit in 図 8-1, shows a typical application for driving IGBTs.

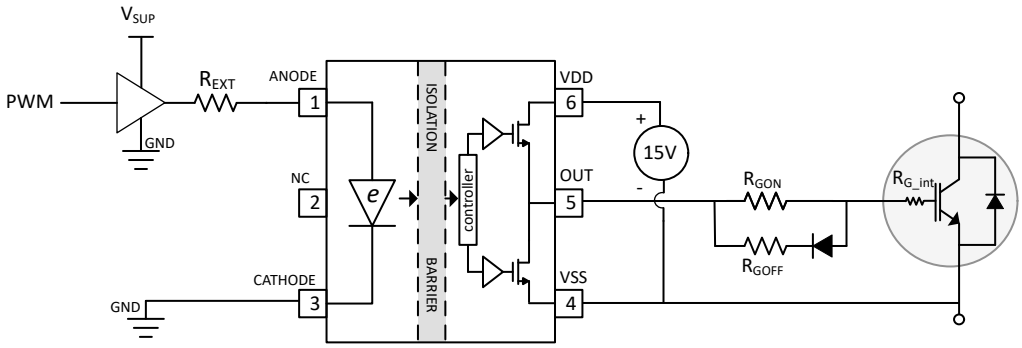

図 8-1. Typical Application Circuit for UCC23525 to Drive IGBT

8.2.1 Design Requirements

表 8-1 lists the recommended conditions to observe the input and output of the UCC23525 gate driver.

表 8-1. UCC23525 Design Requirements

PARAMETER	VALUE	UNIT
V_{DD}	15	V
I_F	10	mA
Switching frequency	10	kHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the Input Resistor

The input resistor limits the current that flows into the e-diode when it is forward biased. The threshold current I_{FLH} is 1 mA typ. The recommended operating range for the forward current is 5 mA to 20 mA (e-diode ON). All the electrical specifications are ensured in this range. The resistor should be selected such that for typical operating conditions, I_F is 10 mA. Following are the list of factors that will affect the exact value of this current:

1. Supply Voltage V_{SUP} variation
2. Manufacturer's tolerance for the resistor and variation due to temperature
3. e-diode forward voltage drop variation (at I_F=10 mA, V_F= typ 1.7 V, min 1.4 V, max 2 V, with a temperature coefficient < 0.9 mV/°C and dynamic impedance < 1 Ω)

See 図 8-2 for the schematic using a single buffer and anode resistor combination to drive the input stage of UCC23525. The input resistor can be selected using 式 1.

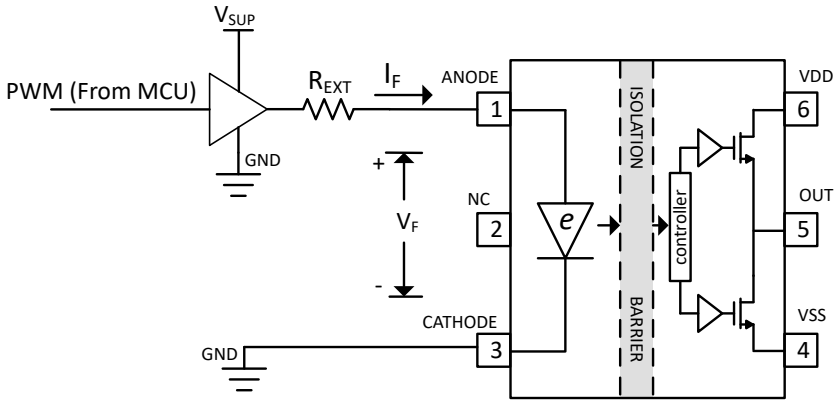

図 8-2. Driving the Input Stage of UCC23525 with One Buffer and Anode Resistor

$$R_{EXT} = \frac{V_{SUP} - V_F}{I_F} - R_{OH\_buf} \quad (1)$$

表 8-2 shows the range of values for R_{EXT} for 図 8-2. The assumptions used in deriving the range for R_{EXT} are as follows:

1. Target forward current I_F is 5 mA min, 10 mA typ and 20 mA max
2. e-diode forward voltage drop is 1.4 V to 2.
3. V_{SUP} (Buffer supply voltage) is 5 V with ±5% tolerance
4. Manufacturer's tolerance for R_{EXT} is 1%
5. R_{OH} (buffer output impedance in output "High" state) is 13 Ω min, 18 Ω typ and 22 Ω max

表 8-2. R_{EXT} Values to Drive the Input Stage

	R_{EXT} Ω		
Configuration	Min	Typ	Max
Single Buffer and R_{EXT}	115	312	757

8.2.2.2 Gate Driver Output Resistor

The external gate-driver resistors, $R_{G(ON)}$ and $R_{G(OFF)}$ are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

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The output stage has a pull up with a peak source current of 5 A. Use 式 2 to estimate the peak source current as an example.

$$I_{OH} = \min\left[5A, \frac{V_{DD} - V_{GDF}}{\left(R_{OH} + R_{GON} + R_{GFET_{INT}}\right)}\right] \quad (2)$$

where

- R_{GON} is the external turnon resistance.
- R_{GFET_Int} is the power transistor internal gate resistance, found in the power transistor data sheet. We will assume 0Ω for our example
- I_{OH} is the peak source current which is the minimum value between 5 A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance.
- V_{GDF} is the forward voltage drop for each of the diodes in series with R_{GON} and R_{GOFF}. The diode drop for this example is 0.7 V.

In this example, the peak source current is approximately 1.15A as calculated in 式 3.

$$I_{OH} = \min\left[5A, \frac{15}{2.5\Omega + 10\Omega + 0\Omega}\right] = 1.2A \quad (3)$$

Similarly, use 式 4 to calculate the peak sink current.

$$I_{OL} = \min\left[5A, \frac{V_{DD} - V_{GDF}}{R_{OL} + R_{GON} \,||\, R_{GOFF} + R_{GFET_{INT}}}\right] \quad (4)$$

where

- R_{GOFF} is the external turnoff resistance.
- I_{OL} is the peak sink current which is the minimum value between 5 A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance.

In this example, the peak sink current is the minimum of 5 A and 式 5.

$$I_{OL} = \min\left[5A, \frac{15 - 0.7}{0.7\Omega + 10\Omega \,||\, 10\Omega + 0\Omega}\right] = 2.51A \quad (5)$$

The diodes shown in series with R_{GOFF}, in 図 8-1 ensure the gate drive current flows through the intended path, respectively, during turn-on and turn-off. Note that the diode forward drop will reduce the voltage level at the gate of the power switch. To achieve rail-to-rail gate voltage levels, add a resistor from the V_{OUT} pin to the power switch gate, with a resistance value approximately 20 times higher than R_{GOFF}. For the examples described in this section, a good choice is 100 Ω to 200 Ω.

注

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the input capacitance of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

8.2.2.3 Estimate Gate-Driver Power Loss

The total loss, P_G, in the gate-driver subsystem includes the power losses (P_{GD}) of the UCC23525 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

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The P_{GD} value is the key power loss which determines the thermal safety-related limits of the UCC23525 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes power dissipated in the input stage (P_{GDQ_IN}) as well as the quiescent power dissipated in the output stage (P_{GDQ_OUT}) when operating with a certain switching frequency under no load. P_{GDQ_IN} is determined by I_F and V_F and is given by 式 6. The P_{GDQ_OUT} parameter is measured on the bench with no load connected to V_{OUT} pin at a given V_{DD}, switching frequency, and ambient temperature. In this example, V_{DD} is 15 V. The current on the power supply, with PWM switching at 10 kHz, is measured to be I_{DD} = 1.33 mA . Therefore, use 式 7 to calculate P_{GDQ_OUT}.

$$P_{GDQ_{IN}} = \frac{1}{2} \times V_F \times I_F \tag{6}$$

$$P_{GDQ_{OUT}} = V_{DD} \times I_{DD} \tag{7}$$

The total quiescent power (without any load capacitance) dissipated in the gate driver is given by the sum of 式 6 and 式 7 as shown in 式 8.

$$P_{GDQ} = P_{GDQ_{IN}} + P_{GDQ_{OUT}} = 9\text{mW} + 20\text{mW} = 29\text{mW} \tag{8}$$

The second component is the switching operation loss, P_{GDSW}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use 式 9 to calculate the total dynamic loss from load switching, P_{GSW}.

$$P_{GSW} = V_{DD} \times Q_G \times f_{SW} \tag{9}$$

where

- Q_G is the gate charge of the power transistor at V_{DD}.

So, for this example application the total dynamic loss from load switching is approximately 18 mW as calculated in 式 10.

$$P_{GSW} = 15\text{V} \times 120\text{nC} \times 10\text{kHz} = 18\text{mW} \tag{10}$$

Q_G represents the total gate charge of the power transistor switching 520 V at 50 A, and is subject to change with different testing conditions. The UCC23525 gate-driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} is equal to P_{GSW} if the external gate-driver resistance and power-transistor internal resistance are 0 Ω, and all the gate driver-loss will be dissipated inside the UCC23525. If an external turn-on and turn-off resistance exists, the total loss is distributed between the gate driver pull-up/down resistance, external gate resistance, and power-transistor internal resistance. Importantly, the pull-up/down resistance is a linear and fixed resistance if the source/sink current is not saturated to 5A/5A, however, it will be non-linear if the source/sink current is saturated. Therefore, P_{GDO} is different in these two scenarios.

Case 1 - Linear Pull-Up/Down Resistor:

$$P_{GDO} = \frac{P_{GSW}}{2}\left[\frac{R_{OH}}{R_{OH} + R_{GON} + R_{GFET_{int}}} + \frac{R_{OL}}{R_{OL} + R_{GON} \,||\, R_{GOFF} + R_{GFET_{int}}}\right] \tag{11}$$

In this design example, all the predicted source and sink currents are less than 5 A and 5 A, therefore, use 式 11 to estimate the UCC23525 gate-driver loss.

$$P_{GDO} = \frac{18\text{mW}}{2}\left[\frac{2.5\Omega}{2.5\Omega + 10\Omega + 0\Omega} + \frac{0.7\Omega}{0.7\Omega + 10\Omega \,||\, 10\Omega + 0\Omega}\right] \tag{12}$$

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Case 2 - Nonlinear Pull-Up/Down Resistor:

$$P_{GDO} = f_{sw} \times \left[\int_0^{T_{R_{Sys}}} 5A \times (V_{DD} - V_{OUT}(t))dt + \int_0^{T_{R_{Sys}}} 5A \times V_{OUT}(t)\, dt \right] \quad (13)$$

where

- $V_{OUT(t)}$ is the gate-driver OUT pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (5 A at turnon and 5 A at turnoff) charging or discharging a load capacitor. Then, the $V_{OUT(t)}$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

For some scenarios, if only one of the pullup or pulldown circuits is saturated and another one is not, the P_{GDO} is a combination of case 1 and case 2, and the equations can be easily identified for the pullup and pulldown based on this discussion.

Use 式 14 to calculate the total gate-driver loss dissipated in the UCC23525 gate driver, P_{GD}.

$$P_{GD} = P_{GDQ} + P_{GDO} = 29mW + 2.9mW = 31.9mW \quad (14)$$

8.2.2.4 Estimating Junction Temperature

Use 式 15 to estimate the junction temperature (T_J) of UCC23525.

$$T_J = T_C + \Psi_{JT} \times P_{GD} \quad (15)$$

where

- T_C is the UCC23525 case-top temperature measured with a thermocouple or some other instrument.
- Ψ_{JT} is the junction-to-top characterization parameter from the table.

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The $R_{\theta JC}$ resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of $R_{\theta JC}$ will inaccurately estimate the true junction temperature. The Ψ_{JT} parameter is experimentally derived by assuming that the dominant energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

8.2.2.5 Selecting V_{DD} Capacitor

Bypass capacitors for V_{DD} is essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances. A 50-V, 10-µF MLCC and a 50-V, 0.22-µF MLCC are selected for the C_{VDD} capacitor. If the bias power supply output is located a relatively long distance from the V_{CC} pin, a tantalum or electrolytic capacitor with a value greater than 10 µF should be used in parallel with C_{VDD}.

注

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1-µF X7R capacitor is measured to be only 500 nF when a DC bias of 15-V_{DC} is applied.

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9 Power Supply Recommendations

The recommended input supply voltage (V_{DD}) for the UCC23525 device is from 13V to 30V. The lower limit of the range of output bias-supply voltage (V_{DD}) is determined by the internal UVLO protection feature of the device. V_{DD} voltage should not fall below the UVLO threshold for normal operation, or else the gate-driver outputs can become clamped low for more than TBD µs by the UVLO protection feature. The higher limit of the V_{DD} range depends on the maximum gate voltage of the power device that is driven by the UCC23525 device, and should not exceed the recommended maximum V_{DD} of 30 V. A local bypass capacitor should be placed between the VDD and VSS pins, with a value of 220-nF to 10-µF for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended.

If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* data sheet and *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

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10 Layout

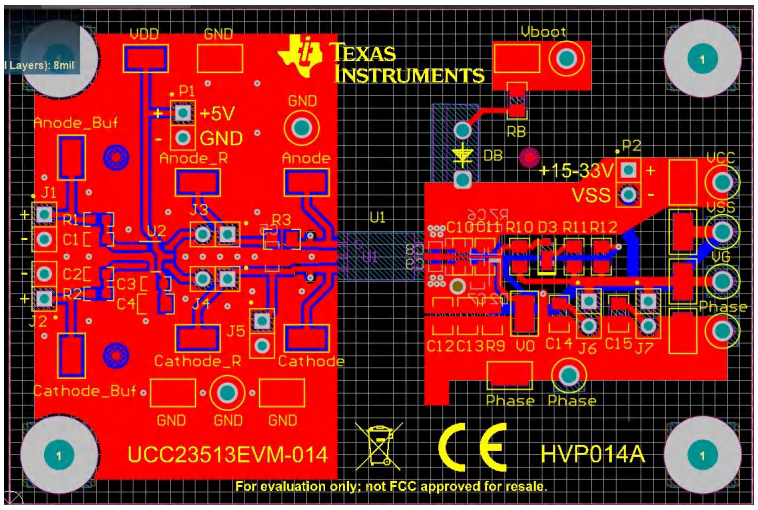
10.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the UCC23525. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the VDD and VSS pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the VSS pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. A PCB cutout or groove is recommended in order to prevent contamination that may compromise the isolation performance.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC23525 if the driving voltage is high, the load is heavy, or the switching frequency is high. Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - Increasing the PCB copper connecting to the VDD and VSS pins is recommended, with priority on maximizing the connection to VSS. However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the VDD and VSS pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

10.2 Layout Example

図 10-1 shows a PCB layout example with the signals and key components labeled.



A. No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

図 10-1. Layout Example

図 10-2 and 図 10-3 show the top and bottom layer traces and copper.

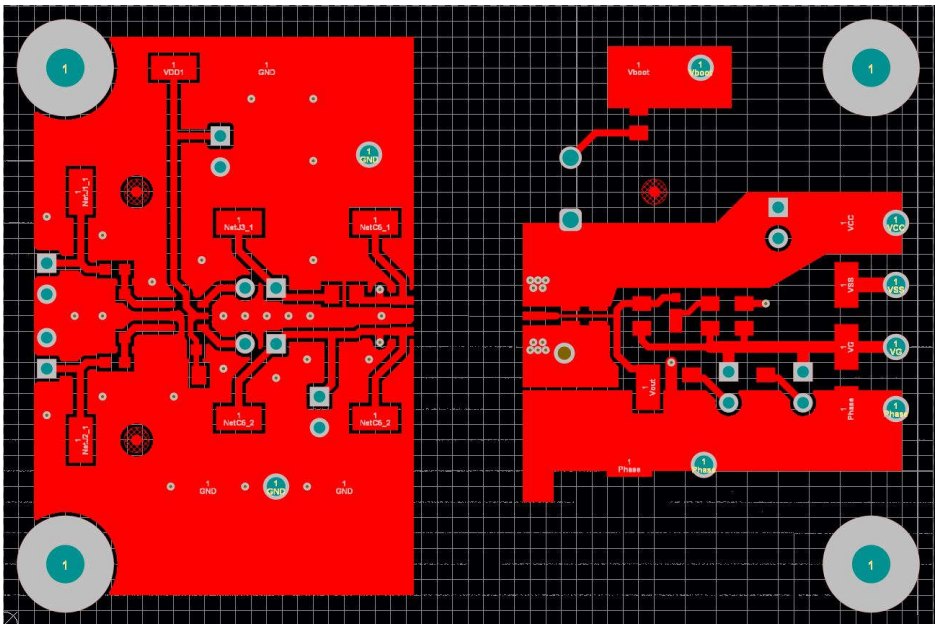


図 10-2. Top-Layer Traces and Copper

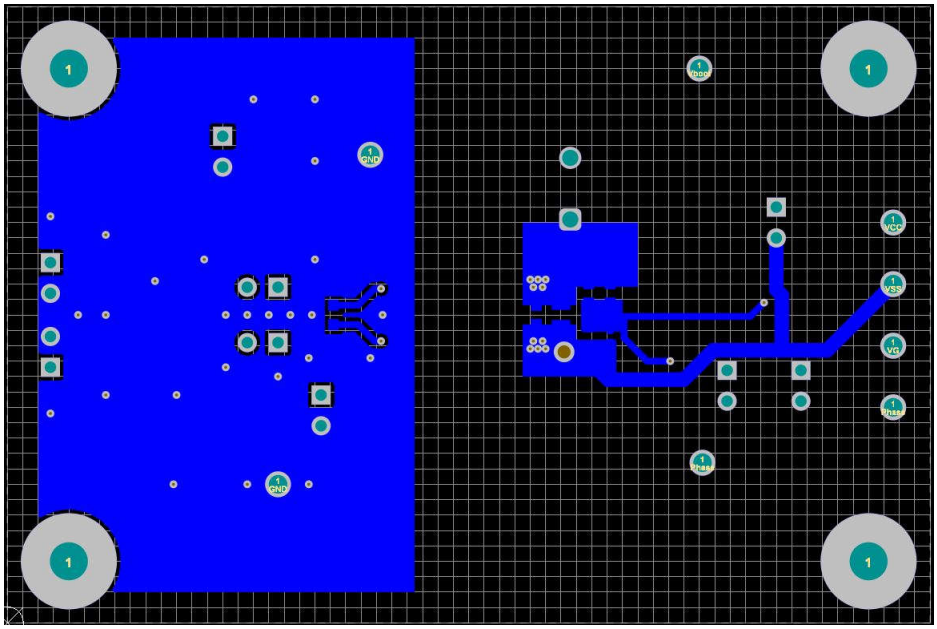


図 10-3. Bottom-Layer Traces and Copper (Flipped)

図 10-4 shows the 3D layout of the top view of the PCB.

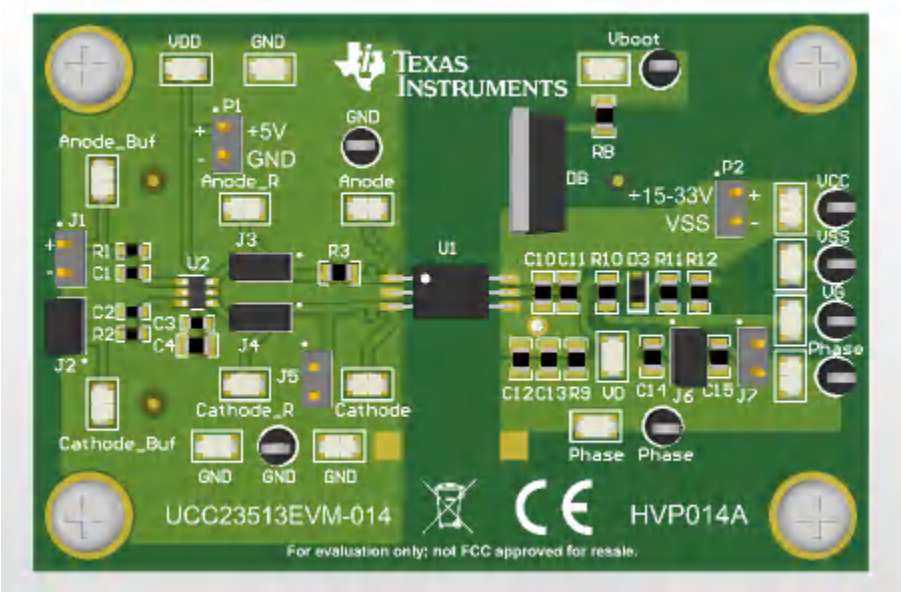


図 10-4. 3-D PCB View

10.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

11 Device and Documentation Support

11.1 Device Support

11.1.1 サード・パーティ製品に関する免責事項

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11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Digital Isolator Design Guide*
- *Isolation Glossary*
- *SN6501 Transformer Driver for Isolated Power Supplies*
- *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies*

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2023) to Revision A (April 2024)	Page
• 「非公開」から「公開事前情報リリース」に変更	1

ADVANCE INFORMATION

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
UCC23525CDWYR	PREVIEW	SOIC	DWY	6	850	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

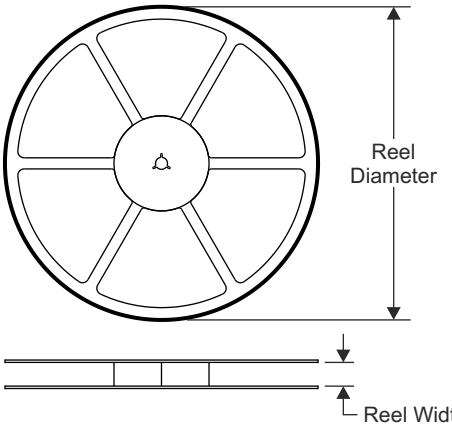
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

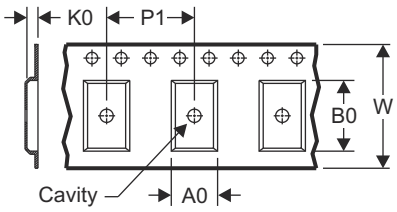
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

13.2 Tape and Reel Information

REEL DIMENSIONS

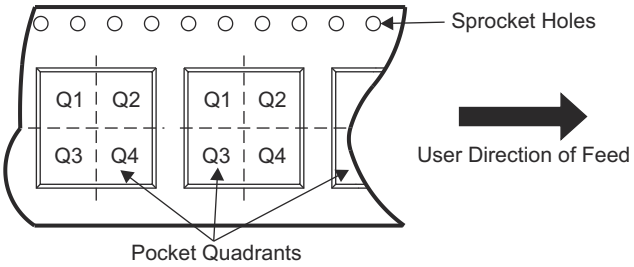


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

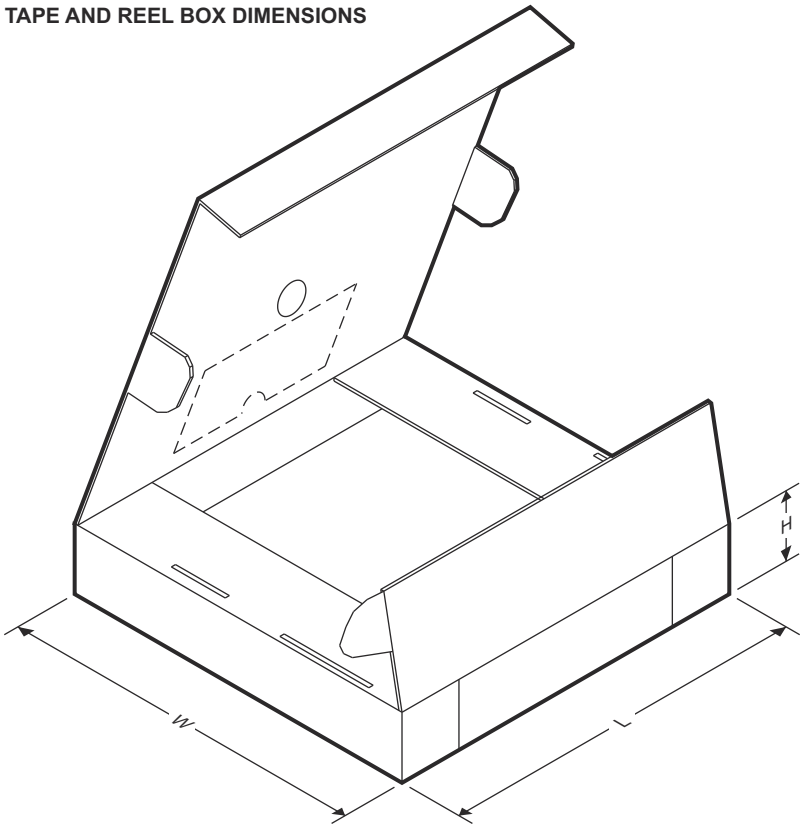
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC23525CDWYR	SOIC	DWY	6	850	330.0	16.4	12.15	5.0	3.9	16.0	16.0	Q1

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC23525CDWYR	SOIC	DWY	6	850	356.0	356.0	35.0

ADVANCE INFORMATION

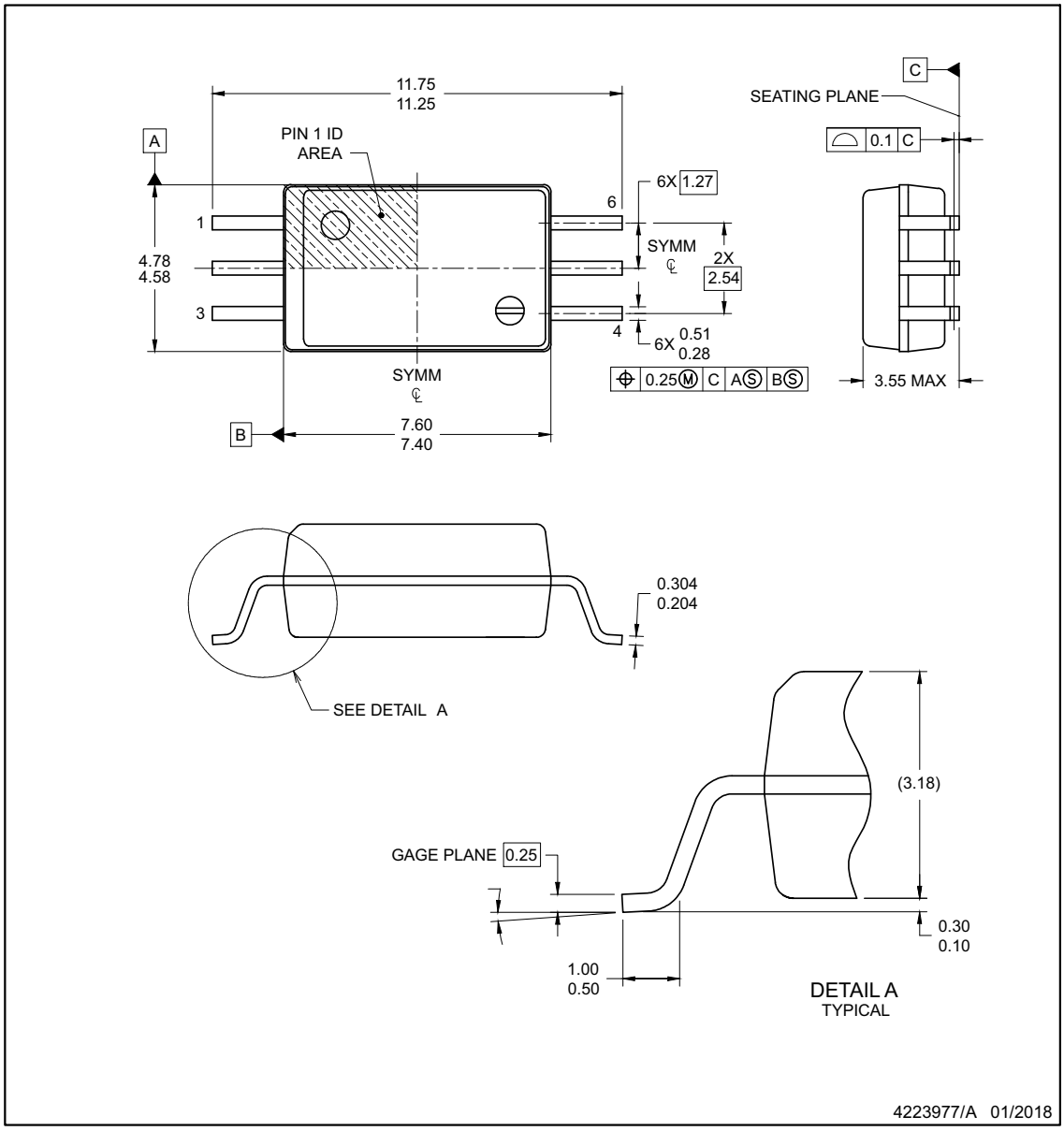
ADVANCE INFORMATION

13.3 Mechanical Data

PACKAGE OUTLINE

DWY0006A — **SOIC -3.55 mm max height**

SOIC



NOTES:

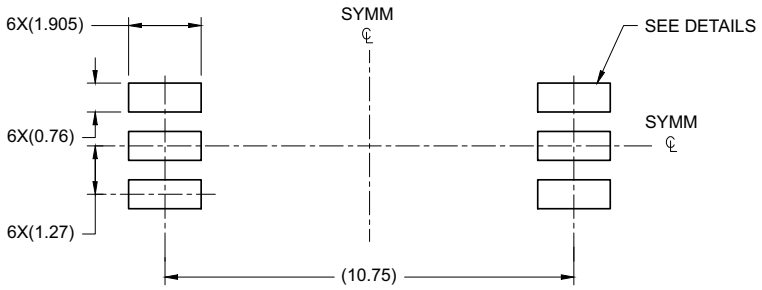
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.70 per side.

EXAMPLE BOARD LAYOUT

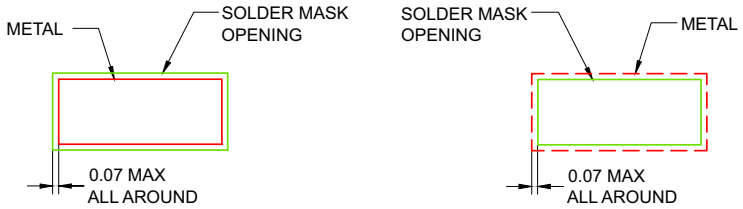
DWY0006A

SOIC - 3.55 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAAILS

4223977/A 01/2018

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

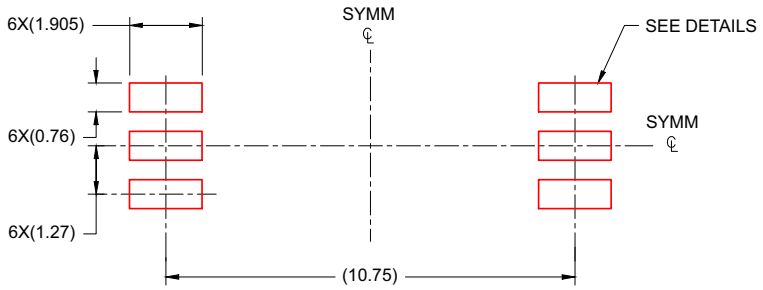
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DWY0006A — **SOIC - 3.55 mm max height**

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 6X

4223977/A 01/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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