参考資料

TUSB216I
JAJSLB7A – MARCH 2021 – REVISED DECEMBER 2023

TUSB216I USB 2.0 高速シグナル・コンディショナ、BC 1.2 コントローラ付き

1 特長

- 広い電源電圧範囲:2.3～6.5V
- USB 切断時およびシャットダウン時の非常に低い消費電力
- USB 2.0 High Speed 信号のコンディショニングを提供
- USB 2.0、OTG 2.0、BC 1.2 に対応
- Low-Speed、Full-Speed、High-Speed 信号処理のサポート
- BC 1.2 CDP バッテリ充電コントローラを内蔵
- 特定のホストやデバイスに非依存
- 最大 5m のケーブルをサポート
  - 外付けのプルダウン抵抗により 4 つの信号ブースト (エッジ・ブーストと DC ブースト) 設定を選択可能
  - プルアップまたはプルダウンで選択可能な 3 つの RX 感度設定により、損失が大きいアプリケーションの ISI ジッタを補償
- 2 つの TUSB216I デバイスを使って最大 10m のケーブル長に対応
- スケーラブルなソリューション - 損失が大きいアプリケーションに対応するため、デバイスをデイジー・チェーン接続可能
- TUSB211A、212、214、217A (3.3V) とピン互換

2 アプリケーション

- ラップトップ、デスクトップまたはドッキング・ステーション
- 携帯電子機器
- タブレット
- 携帯電話
- テレビ
- アクティブ・ケーブル、延長ケーブル、バックプレーン

3 概要

TUSB216I は第 3 世代 USB 2.0 High Speed 信号コンディショナーで、伝送チャネルでの AC 損失 (容量性負荷による) および DC 損失 (抵抗損失による) を補償するように設計されています。

TUSB216I には、エッジ・ブースタにより USB 2.0 High Speed 信号の遷移エッジを高速化し、DC ブースト機能により静的電圧レベルを上げる特許取得済みの設計が採用されています。

また、TUSB216I はプリイコライゼーション機能を備えているため、レシーバ感度を高め、長いケーブルを使用するアプリケーションで ISI (符号間干渉) ジッタを補償できます。USB Low Speed および Full Speed 信号特性は、TUSB216I による影響を受けません。

TUSB216I は、パケット・タイミングを変更せず、また、伝搬遅延やレイテンシを追加せずに、信号品質を向上させることができます。

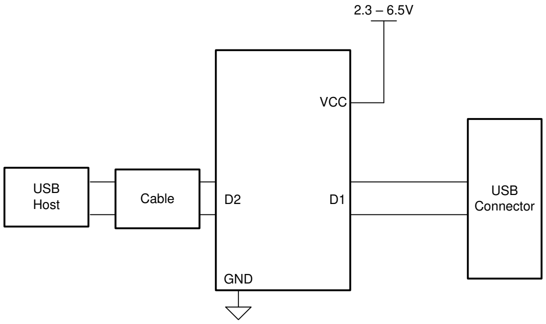
TUSB216I により、最長 5 メートルのケーブルを使用したシステムで、USB 2.0 High Speed 近端アイ・コンプライアンスに合格することが可能になります。

TUSB216I は USB On-The-Go (OTG) および Battery Charging (BC 1.2) プロトコルにも対応しています。内蔵の BC 1.2 バッテリ充電コントローラは、制御ピンを使って有効化できます。

製品情報

部品番号 (1)	パッケージ(2)	動作温度 (T_A) ℃	パッケージ サイズ (3)
TUSB216	RWB (X2QFN、12)	0～70	1.6mm × 1.6mm
TUSB216I		-40～85	
TUSB216-Q1		-40～105	

(1) 製品比較表を参照してください。
(2) 詳細については、セクション 11 を参照してください。
(3) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

English Data Sheet: SLLSFM9

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4 Device Comparison

	TUSB211A	TUSB212	TUSB214	TUSB216	TUSB217A
Industrial Variant Available	Y	Y	Y	Y	Y
Automotive Variant Available	Y	Y	Y	Y	Y
Supply (V)	2.3 to 6.5	3.3	3.3	2.3 to 6.5	2.3 to 6.5
DC Boost	Tandem with AC Boost	3 levels	3 levels	Tandem with AC Boost	Tandem with AC Boost
I2C Control	N	Y	Y	Y	Y
RX pre-equalization for ISI compensation	N/A	N/A	N/A	3 levels	3 levels
Charging Downstream Port (CDP) controller	N/A	N/A	Always ON	Pin Controlled	Always ON. Dynamically selected by DCP/CDP pin
Dedicated Charging Port (DCP) controller	N/A	N/A	N/A	N/A	Always ON. Dynamically selected by DCP/CDP pin
Cable length compensation for near-end high-speed eye mask Compliance (pre-channel before redriver/post-channel after redriver) (meter - gauge)	6/3 - 28AWG (10 - 24AWG with one redriver on each end)	4/2 - 28AWG	4/2 - 28AWG	6/3 - 28AWG (10 - 24AWG with one redriver on each end)	6/3 - 28AWG (10 - 24AWG with one redriver on each end)
Cable length compensation for far-end high-speed eye mask Compliance (pre-channel before redriver/post-channel after redriver) (meter - gauge)	10/8 - 26AWG (10 - 28AWG with one redriver on each end)	8/6 - 28AWG	8/6 - 28AWG	10/8 - 26AWG (10 - 28AWG with one redriver on each end)	10/8 - 26AWG (10 - 28AWG with one redriver on each end)

5 Pin Configuration and Functions

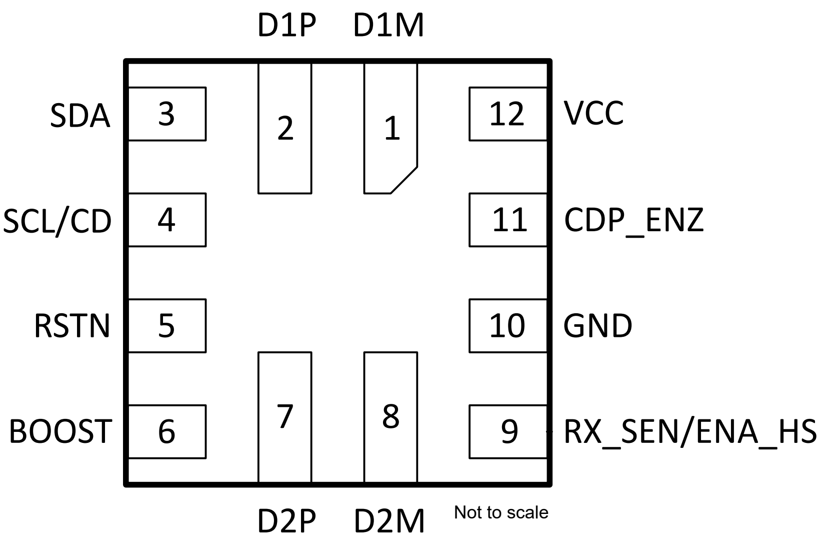

図 5-1. TUSB216I RWB Package, 12-Pin X2QFN (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
BOOST	6	I	N/A	USB High-speed boost select via external pull down resistor. Both edge boost and DC boost are controlled by a single pin in non-I2C mode. In I2C mode edge boost and DC boost can be individually controlled. Sampled upon power up. Does not recognize real time adjustments. Auto selects BOOST LEVEL = 3 when left floating.
CDP_ENZ	11	I	500 kΩ PU	Set CDP_ENZ is low to enable BC 1.2 CDP controller
RX_SEN[3]/ENA_HS	9	I/O	N/A	In I2C mode: Reserved for TI test purpose. In non-I2C mode: At reset: 3-level input signal RX_SEN. USB High-speed RX Sensitivity Setting to Compensate ISI Jitter H (pin is pulled high) – high RX sensitivity (high loss channel) M (pin is left floating) – medium RX sensitivity (medium loss channel) L (pin is pulled low) – low RX sensitivity (low loss channel) After reset: Output signal ENA_HS. Flag indicating that channel is in High-speed mode. Asserted upon: 1. Detection of USB-IF High-speed test fixture from an unconnected state followed by transmission of USB TEST_PACKET pattern. 2. Squelch detection following USB reset with a successful HS handshake [HS handshake is declared to be successful after single chirp J chirp K pair where each chirp is within 18 µs – 128 µs].

表 5-1. Pin Functions (続き)

PIN		TYPE[1]	INTERNAL PULLUP/PULLDOWN	DESCRIPTION
NAME	NO.			
D2P	7	I/O	N/A	USB High-speed positive port.
D2M	8	I/O	N/A	USB High-speed negative port.
GND	10	P	N/A	Ground
D1M	1	I/O	N/A	USB High-speed negative port..
D1P	2	I/O	N/A	USB High-speed positive port.
SDA[2]	3	I/O	500 kΩ PU 1.8 MΩ PD	I2C Mode: Bidirectional I2C data pin [7-bit I2C slave address = 0x2C]. In non I2C mode: Reserved for TI test purpose.
VCC	12	P	N/A	Supply power
RSTN	5	I	500 kΩ PU 1.8 MΩ PD	Device disable/enable. Low – Device is at reset and in shutdown, and High - Normal operation. Recommend 0.1-μF external capacitor to GND to ensure clean power on reset if not driven. If the pin is driven, it must be held low until the supply voltage for the device reaches within specifications.
SCL[2]/CD	4	I/O	When RSTN asserted there is a 500 kΩ PD	In I2C mode: I2C clock pin [I2C address = 0x2C]. Non I2C mode: After reset: Output CD. Flag indicating that a USB device is attached (connection detected). Asserted from an unconnected state upon detection of DP or DM pull-up resistor. De-asserted upon detection of disconnect.

(1) I = input, O = output, P = power
(2) Pull-up resistors for SDA and SCL pins in I^2C mode should be $R_{Pull\text{-}up}$ (depending on I2C bus voltage). If both SDA and SCL are pulled up at power-up the device enters into I^2C mode.
(3) Pull-down and pull-up resistors for RX_SEN pin must follow R_{RXSEN1} and R_{RXSEN2} resistor recommendations in non I^2C mode.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage range	VCC	–0.3	7	V
Voltage range USB data	DxP, DxM	–0.3	5.5	V
Voltage range on BOOST pin	BOOST	-0.3	1.98	V
Voltage range other pins	RX_SEN, CDP_ENZ, SDA, SCL, RSTN	-0.3	5.5	V
Storage temperature, T_{stg}		–65	150	°C
Maximum junction temperature, $T_{J\,(max)}$			125	°C

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(1) *Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.*

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

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(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.3	5	6.5	V
T_A	Operating free-air temperature (Industrial)	–40		85	°C
T_J	Junction temperature (Industrial)			105	°C
V_{I2C_BUS}	I2C Bus Voltage	1.62		3.6	V
DxP, DxM	Voltage range USB data	0		3.6	V
BOOST	Voltage range BOOST pin	0		1.98	V
DIGITAL	Voltage range other pins (SCL, SDA, RSTN, CDP_ENZ)	0		3.6	V
RX_SEN	Voltage range RX_SEN pin	0		5.0	V

6.4 Thermal Information

THERMAL METRIC (1)		RWB (X2QFN)	UNIT
		12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	137.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	62	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	67.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

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(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
POWER						
I_{ACTIVE_HS}	High Speed Active Current	USB channel = HS mode. 480 Mbps traffic. V_{CC} supply stable, with Boost = Max		22	36	mA
I_{IDLE_HS}	High Speed Idle Current	USB channel = HS mode, no traffic. V_{CC} supply stable, Boost = Max		22	36	mA
$I_{HS\_SUPSPEND}$	High Speed Suspend Current	USB channel = HS Suspend mode. V_{CC} supply stable		0.75	1.4	mA
I_{FS}	Full-Speed Current	USB channel = FS mode, 12 Mbps traffic, V_{cc} supply stable		0.75	1.4	mA
$I_{DISCONN}$	Disconnect Power	Host side application. No device attachment.		0.80	1.4	mA
I_{SHUTDN}	Shutdown Power	RSTN driven low, V_{CC} supply stable		60	115	µA
CONTROL PIN LEAKAGE						
I_{LKG_FS}	Pin failsafe leakage current for SDA, RSTN	V_{CC} = 0 V, pin at $V_{IH,\ max}$		10	15	µA
I_{LKG_FS}	Pin failsafe leakage current for RX_SEN	V_{CC} = 0 V, pin at $V_{IH,\ max}$		6	15	µA
I_{LKG_FS}	Pin failsafe leakage current for SCL	V_{CC} = 0 V, pin at $V_{IH,\ max}$			70	nA
INPUT RSTN						
V_{IH}	High level input voltage		1.5		3.6	V
V_{IL}	Low-level input voltage		0		0.5	V
I_{IH}	High level input current	V_{IH} = 3.6 V, R_{PU} enabled			±15	µA
I_{IL}	Low level input current	V_{IL} = 0V, R_{PU} enabled			±20	µA
INPUT DIGITAL						
V_{IH}	High level input voltage (CDP_ENZ)		1.5		3.6	V
V_{IL}	Low-level input voltage (CDP_ENZ)		0		0.5	V
I_{IL}	Low level input current	V_{IL} = 0V			±20	µA
I_{IH}	High level input current	V_{IH} = 3.6 V			±15	µA
INPUT RX_SEN (3-level input, for mid level leave pin floating)						
$V_{IH(Max)}$	Maximum High level input voltage	VCC = 2.3V to 6.5V			5.0	V
$V_{IH(Min)}$	Minimum High level input voltage	VCC > 4.5V	3.3			V
		VCC = 2.3V to 4.5V (% of VCC)	75			%
V_{IL}	Low level input voltage	VCC > 4.5V			0.75	V
		VCC = 2.3V to 4.5V (% of VCC)			15	%
INPUT BOOST						
R_{BOOST_LVL0}	External pulldown resistor for BOOST Level 0				160	Ω
R_{BOOST_LVL1}	External pulldown resistor for BOOST Level 1		1.5	1.8	2	kΩ
R_{BOOST_LVL2}	External pulldown resistor for BOOST Level 2		3.4	3.6	3.96	kΩ
R_{BOOST_LVL3}	External pulldown resistor for BOOST Level 3 to remove upper limit for resistor value, can be left open		7.5			kΩ
OUTPUTS CD, ENA_HS						
V_{OH}	High level output voltage for CD and ENA_HS	I_O = –50 µA, VCC >= 3.0V	2.5			V
V_{OH}	High level output voltage for CD	I_O = –25 µA, VCC = 2.3V	1.7			V

6.5 Electrical Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
V_{OH}	High level output voltage for ENA_HS	I_O = –25 µA, VCC = 2.3V	1.8			V
V_{OL}	Low level output voltage for CD and ENA_HS	I_O = 50 µA			0.3	V
I2C						
C_{I2C_BUS}	I^2C Bus Capacitance		4		150	pF
I_{OL}	I^2C open drain output current	V_{OL} = 0.4V	1.5			mA
V_{IL}	2.3V<= VCC<= 4.3V, V_{I2C_BUS} = 1.8V +/-10%	$R_{Pull\text{-}up}$ =1.6kΩ to 2.5kΩ, % of V_{I2C_BUS}			25	%
V_{IL}	V_{I2C_BUS} = 3.3V +/-10%	$R_{Pull\text{-}up}$ =2.8kΩ to 7kΩ, % of V_{I2C_BUS}			25	%
V_{IH}	2.3V<= VCC<= 4.3V, V_{I2C_BUS} = 1.8V +/-10%	$R_{Pull\text{-}up}$ =1.6kΩ to 2.5kΩ, % of V_{I2C_BUS}	80			%
V_{IH}	V_{I2C_BUS} = 3.3V +/-10%	$R_{Pull\text{-}up}$ =2.8kΩ to 7kΩ, % of V_{I2C_BUS}	75			%
$R_{Pull\text{-}up}$	V_{I2C_BUS} = 1.8V +/-10%		1.6	2	2.5	kΩ
$R_{Pull\text{-}up}$	V_{I2C_BUS} = 3.3V +/-10%		2.8	4.7	7	kΩ
SCL Frequency					400	kHz
DxP, DxM						
C_{IO_DXX}	Capacitance to GND	Measured with VNA at 240 MHz, V_{CC} supply stable, Redriver off		2.5		pF

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
DxP, DxM USB Signals						
F_{BR_DXX}	Bit Rate	USB channel = HS mode. 480 Mbps traffic. V_{CC} supply stable			480	Mbps
t_{R/F_DXX}	Rise/Fall time		100			ps

(1) All typical values are at V_{CC} = 5 V, and T_A = 25°C.

6.7 Timing Requirements

		MIN	NOM	MAX	UNIT
POWER UP TIMING					
T_{RSTN_PW}	Minimum width to detect a valid RSTN signal assert when the pin is actively driven low	100			µs
T_{STABLE}	VCC must be stable before RSTN de-assertion	300			µs
T_{READY}	Maximum time needed for the device to be ready after RSTN is de-asserted.			500	µs
T_{RAMP}	V_{CC} ramp time			100	ms
T_{RAMP}	V_{CC} ramp time	0.2			ms
I2C (STD)					
t_{SUSTO}	Stop setup time, SCL (T_r=600ns-1000ns), SDA (T_f=6.5ns-106.5ns), 100kHz STD	4			µs
t_{HDSTA}	Start hold time, SCL (Tr=600ns-1000ns), SDA (Tf=6.5ns-106.5ns), 100kHz STD	4			µs
t_{SUSTA}	Start setup time, SCL (T_r=600ns-1000ns), SDA (T_f=6.5ns-106.5ns), 100kHz STD	4.7			µs
t_{SUDAT}	Data input or False start/stop, setup time, SCL (T_r=600ns-1000ns), SDA (T_f=6.5ns-106.5ns), 100kHz STD	250			ns
t_{HDDAT}	Data input or False start/stop, hold time, SCL (T_r=600ns-1000ns), SDA (T_f=6.5ns-106.5ns), 100kHz STD	5			µs
t_{BUF}	Bus free time between START and STOP conditions	4.7			µs
t_{LOW}	Low period of the I2C clock	4.7			µs
t_{HIGH}	High period of the I2C clock	4			µs
t_F	Fall time of both SDA and SCL signals			300	ns
t_R	Rise time of both SDA and SCL signals			1000	ns
I2C (FM)					
t_{SUSTO}	Stop setup time, SCL (T_r=180ns-300ns), SDA (T_f=6.5ns-106.5ns), 400 kHz FM	0.6			µs
t_{HDSTA}	Start hold time, SCL (T_r=180ns-300ns), SDA (T_f=6.5ns-106.5ns), 400 kHz FM	0.6			µs
t_{SUSTA}	Start setup time, SCL (T_r=180ns-300ns), SDA (T_f=6.5ns-106.5ns), 400 kHz FM	0.6			µs
t_{SUDAT}	Data input or False start/stop, setup time, SCL (T_r=180ns-300ns), SDA (T_f=6.5ns-106.5ns), 400 kHz FM	100			ns
t_{HDDAT}	Data input or False start/stop, hold time, SCL (T_r=180ns-300ns), SDA (T_f=6.5ns-106.5ns), 400 kHz FM	0			µs
t_{BUF}	Bus free time between START and STOP conditions	1.3			µs
t_{LOW}	Low period of the I2C clock	1.3			µs
t_{HIGH}	High period of the I2C clock	0.6			µs
t_F	Fall time of both SDA and SCL signals			300	ns
t_R	Rise time of both SDA and SCL signals			300	ns

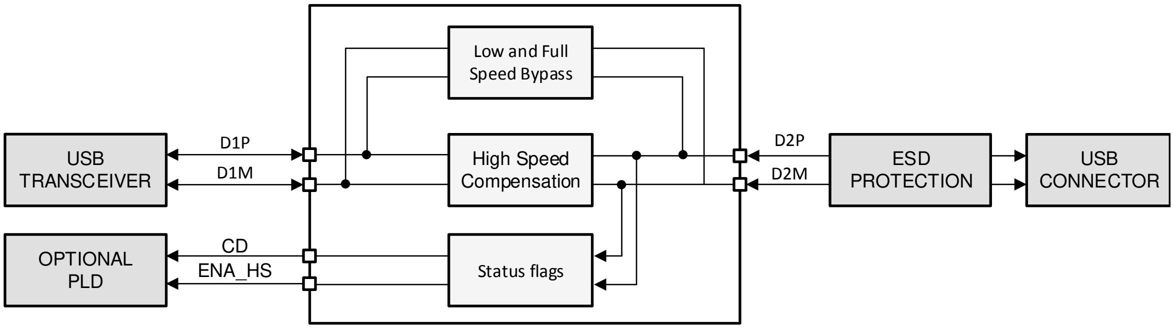
7 Detailed Description

7.1 Overview

The TUSB216I is a USB High-Speed (HS) signal conditioner designed to compensate for ISI signal loss in a transmission channel. TUSB216I has a patented design for USB Low Speed (LS) and Full Speed (FS) signals. It does not alter the signal characteristics. HS signals are compensated. The design is compatible with USB On-The-Go (OTG) and Battery Charging (BC) specifications.

Programmable signal gain through an external resistor permits fine tuning device performance to optimize signals. This helps pass USB HS electrical compliance tests at the connector. Additional RX sensitivity, tuned by external pull-up resistor and pull-down resistor, allows to overcome attenuation in cables. The TUSB216I allows application in series to cover longer distances, or high loss transmission paths. A maximum of 4 devices can be daisy-chained.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 High-Speed Boost

The high-speed booster (combination of edge boost and DC boost) improves the eye width for USB2.0 high-speed signals. It is direction independent and by that is compatible to OTG systems. The BOOST pin is configuring the booster strength with different values of pull down resistors to set 4 levels of boosts, alternatively the boost level can be set through the I2C register according to セクション 7.4.6. Internal circuitry of the signal conditioner reduces possible overshoot.

7.3.2 RX Sensitivity

The RX_SEN pin is a tri-level pin. It is used to set the gain of the device according to system channel loss. RX sensitivity can be increased to recover incoming signals with low vertical eye opening to be able to boost weak signals and helps overcoming high attenuation.

7.4 Device Functional Modes

7.4.1 Low-Speed (LS) Mode

TUSB216I automatically detects a LS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low.

7.4.2 Full-Speed (FS) Mode

TUSB216I automatically detects a FS connection and does not enable signal compensation. CD pin is asserted high but ENA_HS will be low

7.4.3 High-Speed (HS) Mode

TUSB216I automatically detects a HS connection and will enable signal compensation as determined by the configuration of the RX_SEN pin and the external pull down resistance on its BOOST pin.

CD pin and ENA_HS pin are asserted high when high-speed boost is active.

7.4.4 High-Speed Downstream Port Electrical Compliance Test Mode

TUSB216I will detect HS compliance test fixture and enter downstream port high-speed eye diagram test mode. CD pin will be low and ENA_HS pin is asserted high when TUSB216I is in HS eye compliance test mode.

If RSTN pin is asserted low and de-asserted high while TUSB216I is operating in HS functional mode, TUSB216I will transition to HS eye compliance test mode and CD asserts low and ENA_HS remains high. When this occurs signal compensation is enabled.

7.4.5 Shutdown Mode

TUSB216I can be disabled when its RSTN pin is asserted low. DP, DM traces are continuous through the device in shutdown mode. The USB channel is still fully operational, but there is neither signal compensation, nor any indication from the CD pin as to the status of the channel.

表 7-1. CD and ENA_HS Pins in Different Modes

MODE	CD	ENA_HS
Low-speed	HIGH	LOW
Full-speed	HIGH	LOW
High-speed	HIGH	HIGH
High-speed downstream port electrical test	LOW	HIGH
Shutdown	LOW	LOW

7.4.6 I^{2}C Mode

TUSB216I supports 100 and 400 kHz I2C for device configuration, status read back and test purposes. For detail electrical and functional specifications refer to I2C Bus Specification – STANDARD and FAST MODE. This controller is enabled after SCL and SDA pins are sampled high shortly after return from shutdown. In this mode, the CSR can be accessed by I2C read/write transaction to 7-bit slave address 0x2C. It is advised to set CFG_ACTIVE bit before changing values. This halts the FSM, and reset it after all changes are made. This ensure proper startup into high-speed mode.

7.4.7 BC 1.2 Battery Charging Controller

The TUSB216I main function is a signal conditioner offering the boost and pre-equalization features to the incoming DP/DM signals. For applications in which USB host or hub does not provide USB BC charging controller functionality, the TUSB216I can perform this task when CDP_ENZ is low and BC 1.2 CDP Controller is enabled. When battery charging CDP controller feature is enabled (CDP_ENZ=low) TUSB216I supports CDP charging downstream port functionality. CDP_ENZ has an internal pull up when the pin is left unconnected CDP controller will be disabled.

表 7-2. TUSB216I Battery Charging Controller Modes

Pin 11 (CDP_ENZ)	CDP
High	NO
Low	YES

7.5 TUSB216 Registers

表 7-3 lists the memory-mapped registers for the TUSB216 registers. All register offset addresses not listed in 表 7-3 should be considered as reserved locations and the register contents should not be modified.

表 7-3. TUSB216 Registers

Offset	Acronym	Register Name	Section
0x1	EDGE_BOOST	This register is setting EDGE BOOST level.	Go
0x3	CONFIGURATION	This register is selecting device mode.	Go

表 7-3. TUSB216 Registers (続き)

Offset	Acronym	Register Name	Section
0xE	DC_BOOST	This register is setting DC BOOST level.	Go
0x25	RX_SEN	This register is setting RX Sensitivity level.	Go

Complex bit access types are encoded to fit into small table cells. 表 7-4 shows the codes that are used for access types in this section.

表 7-4. TUSB216 Access Type Codes

Access Type	Code	Description
Read Type		
RH	H R	Set or cleared by hardware Read
Write Type		
W	W	Write
Reset or Default Value		
-*n*		Value after reset or the default value

7.5.1 EDGE_BOOST Register (Offset = 0x1) [reset = X]

EDGE_BOOST is shown in 図 7-1 and described in 表 7-5.

Return to Summary Table.

This register is setting EDGE BOOST level.

図 7-1. EDGE_BOOST Register

7	6	5	4	3	2	1	0
ACB_LVL				RESERVED			
RH/W-X				RH/W-X			

表 7-5. EDGE_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ACB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range 0x0 = BOOST PIN LEVEL 0 (lowest edge boost setting) 0x3 = BOOST PIN LEVEL 1 0x6 = BOOST PIN LEVEL 2 0xA = BOOST PIN LEVEL 3 0xF = (highest edge boost setting)
3-0	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values

7.5.2 CONFIGURATION Register (Offset = 0x3) [reset = X]

CONFIGURATION is shown in 図 7-2 and described in 表 7-6.

Return to Summary Table.

This register is selecting device mode.

図 7-2. CONFIGURATION Register

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="7">RESERVED</td><td>CFG_ACTIVE</td></tr>
<tr><td colspan="7">RH/W-X</td><td>RH/W-0x1</td></tr>
</table>

表 7-6. CONFIGURATION Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values
0	CFG_ACTIVE	RH/W	0x1	Configuration mode After reset, if I2C mode is true (SCL and SDA are both pulled high) set the bit to get into configuration mode and clear to return to normal mode. 0x0 = NORMAL MODE 0x1 = CONFIGURATION MODE

7.5.3 DC_BOOST Register (Offset = 0xE) [reset = X]

DC_BOOST is shown in 図 7-3 and described in 表 7-7.

Return to Summary Table.

This register is setting DC BOOST level.

図 7-3. DC_BOOST Register

<table>
<tr><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td colspan="4">RESERVED</td><td colspan="4">DCB_LVL</td></tr>
<tr><td colspan="4">RH/W-X</td><td colspan="4">RH/W-X</td></tr>
</table>

表 7-7. DC_BOOST Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	RH/W	X	These bits are reserved bits and set by hardware at reset. When this register is modified the software should first read these reserved bits and rewrite with the same values
3-0	DCB_LVL	RH/W	X	XXXXb (sampled at startup from BOOST pin) 0000b to 1111b range 0x0 = BOOST PIN LEVEL 0 (lowest dc boost setting) 0x2 = BOOST PIN LEVEL 1 and 2 0x6 = BOOST PIN LEVEL 3 0xF = (highest dc boost setting)

7.5.4 RX_SEN Register (Offset = 0x25) [reset = X]

RX_SEN is shown in 図 7-4 and described in 表 7-8.

Return to Summary Table.

This register is setting RX Sensitivity level.

図 7-4. RX_SEN Register

7	6	5	4	3	2	1	0
RX_SEN							
RH/W-X							

表 7-8. RX_SEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RX_SEN	RH/W	X	XXXXb (sampled at startup from RX_SEN pin) 00000000b to 11111111b range 0x0 = RX_SEN LEVEL LOW 0x33 = RX_SEN LEVEL MID 0x66 = RX_SEN LEVEL HIGH 0xFF = (highest setting)

8 Application and Implementation

注

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8.1 Application Information

The purpose of the TUSB216I is to re-store the signal integrity of a USB High-speed channel up to the USB connector. The loss in signal quality stems from reduced channel bandwidth due to high loss PCB trace and other components that contribute a capacitive load. This can cause the channel to fail the USB near end eye mask. Proper use of the TUSB216I can help to pass this eye mask.

A secondary purpose is to use the CD pin of the TUSB216I to control other blocks on the customer platform, if so desired.

8.2 Typical Application

A typical application for TUSB216I is shown in 図 8-1. In this setup, D2P and D2M face the USB connector while D1P and D1M face the USB host. The orientation may be reversed [that is, D2 faces transceiver and D1 faces connector].

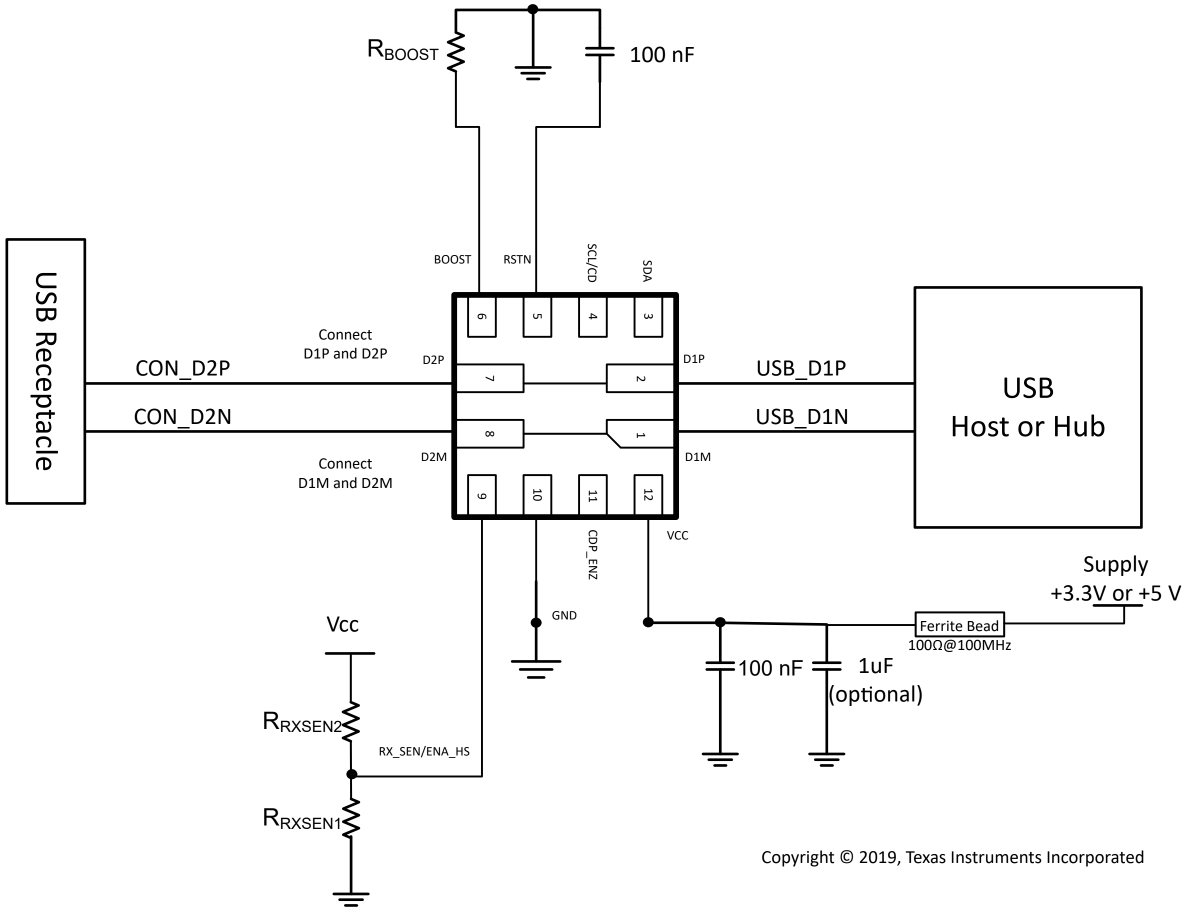

図 8-1. TUSB216I Reference Schematic (Design Example with CDP disabled), CDP_ENZ Can Be Left Floating but an Option for a Decoupling Capacitor of 0.1 µF is Recommended So the Design is Compatible with Older Devices: TUSB211, TUSB212, TUSB214

8.2.1 Design Requirements

TUSB216I requires a valid reset signal as described in the *Power Supply Recommendations* section. The capacitor at RSTN pin is not required if a micro controller drives the RSTN pin according to recommendations.

For this design example, use the parameters shown in 表 8-1, 表 8-2 and 表 8-3.

表 8-1. Design Parameters for 5-V Supply With High Loss System

PARAMETER				VALUE[(1)]
V_{CC}				5 V ±10%
I^2C support required in system (Yes/No)				No
Edge and DC Boost		**R_{BOOST}**	**BOOST Level**	Boost Level 1: R_{BOOST} = 1.8 kΩ
		0-Ω	0	
		1.8 kΩ ±1%	1	
		3.6 kΩ ± 1%	2	
		Do Not Install (DNI)	3	
RX Sensitivity	**R_{RXSEN1}**	**R_{RXSEN2}**	**RX_SEN Level**	High RX Sensitivity Level: R_{RXSEN1} = 37.5 kΩ R_{RXSEN2} = 12.5 kΩ
	22 kΩ - 40 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37.5 kΩ[(2)]	12.5 kΩ	High	

(1) These parameters are starting values for a high loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 5 V supply system could be applicable to 3.3 V supply system as well.
(2) This resistor is needed for a 5 V supply to divide the voltage down so the RX_SEN pin voltage does not exceed 5.0 V.

表 8-2. Design Parameters for 3.3-V Supply With Low to Medium Loss System

PARAMETER				VALUE[(1)]
V_{CC}				3.3 V ±10%
I^2C support required in system (Yes/No)				No
Edge and DC Boost		**R_{BOOST}**	**BOOST Level**	Boost Level 0: R_{BOOST} = 0-Ω
		0-Ω	0	
		1.8 kΩ ±1%	1	
		3.6 kΩ ±1%	2	
		Do Not Install (DNI)	3	
RX Sensitivity	**R_{RXSEN1}**	**R_{RXSEN2}**	**RX_SEN Level**	Medium RX Sensitivity Level: R_{RXSEN1} = DNI R_{RXSEN2} = DNI
	22 kΩ – 40 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	Do Not Install (DNI)	22 kΩ – 40 kΩ (27 kΩ typical)	High	

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 3.3 V supply system could be applicable to 5 V supply system as well.

表 8-3. Design Parameters for 2.3-V to 4.3-V VBAT Supply With Low to Medium Loss System

PARAMETER				VALUE(1)
V_{CC}				2.3 V to 4.3V
I^2C support required in system (Yes/No)				No
Edge and DC Boost		**R_{BOOST}**	**BOOST Level**	Boost Level 0: R_{BOOST} = 0-Ω
		0-Ω	0	
		1.8 kΩ ±1%	1	
		3.6 kΩ ±1%	2	
		Do Not Install (DNI)	3	
RX Sensitivity	**R_{RXSEN1}**	**R_{RXSEN2}**	**RX_SEN Level**	Medium RX Sensitivity Level: R_{RXSEN1} = DNI R_{RXSEN2} = DNI
	22 kΩ – 40 kΩ (27 kΩ typical)	Do Not Install (DNI)	Low	
	Do Not Install (DNI)	Do Not Install (DNI)	Medium	
	37.5 kΩ(2)	12.5 kΩ	High	

(1) These parameters are starting values for a low to medium loss system. Further tuning might be required based on specific host or device as well as cable length and loss profile. These settings are not specific to a 2.3 V – 4.3 V supply system could be applicable to 5 V supply system as well.

(2) This resistor is needed for a VBAT supply (2.3 V – 4.3 V) to divide the voltage down so the RX_SEN pin voltage does not exceed 5.0 V.

8.2.2 Detailed Design Procedure

The ideal BOOST setting is dependent upon the signal chain loss characteristics of the target platform. The recommendation is to start with BOOST level 0, and then increment to BOOST level 1, and so on. Same applies to the RX sensitivity setting where it is recommended to plan for the required pads or connections to change boost settings, but to start with RX sensitivity level Low.

In order for the TUSB216I to recognize any change to the BOOST setting, the RSTN pin must be toggled. This is because the BOOST pin is latched on power up and the pin is ignored thereafter.

注

The TUSB216I compensates for extra attenuation in the signal path according to the configuration of the RX_SEN pin. This maximum recommended voltage for this pin is 5 V when selecting the highest RX sensitivity level.

Placement of the device is also dependent on the application goal. 表 8-4 summarizes our recommendations.

表 8-4. Platform Placement Guideline

PLATFORM GOAL	SUGGESTED TUSB216I PLACEMENT
Pass USB Near End Mask at the receptacle	Close to measurement point (connector)
Pass USB Far End Eye Mask at the plug	Close to USB PHY
Cascade multiple TUSB216Is to improve device enumeration	Midway between each USB interconnect

表 8-5. Table of Recommended Settings

BOOST and RX_SEN settings [(1)](#) for channel loss		
Pre-channel cable length (Between USB PHY and TUSB216I)	**BOOST**	**RX_SEN**
0-3 meter	Level 0	Medium or High
2-5 meter	Level 1	Medium or High
Post-channel cable length (Between TUSB216I and inter-connect)	**BOOST**	**RX_SEN**
0-2 meter	Level 0	Medium or High
1-4 meter	Level 1	Medium or High

(1) These parameters are starting values for different cable lengths. Further tuning might be required based on specific host or device as well as cable length and loss profile.

8.2.2.1 Test Procedure to Construct USB High-speed Eye Diagram

注

USB-IF certification tests for High-speed eye masks require the *mandated use* of the USB-IF developed test fixtures. These test fixtures do not require the use of oscilloscope probes. Instead they use SMA cables. More information can be found at the USB-IF Compliance Updates Page. It is located under the *Electrical Specifications* section, ID 86 dated March 2013.

The following procedure must be followed before using any oscilloscope compliance software to construct a USB High-speed Eye Mask:

8.2.2.1.1 For a Host Side Application

1. Configure the TUSB216I to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB216I
3. Using SMA cables, connect the oscilloscope and the USB-IF host-side test fixture to the TUSB216I
4. Enable the host to transmit USB TEST_PACKET
5. Execute the oscilloscope USB compliance software.
6. Repeat the above steps in order to re-test TUSB216I with a different BOOST setting (must reset to change)

8.2.2.1.2 For a Device Side Application

1. Configure the TUSB216I to the desired BOOST setting
2. Power on (or toggle the RSTN pin if already powered on) the TUSB216I
3. Connect a USB host, the USB-IF device-side test fixture, and USB device to the TUSB216I. Ensure that the USB-IF device test fixture is configured to the ‘INIT’ position
4. Allow the host to enumerate the device
5. Enable the device to transmit USB TEST_PACKET
6. Using SMA cables, connect the oscilloscope to the USB-IF device-side test fixture and ensure that the device-side test fixture is configured to the ‘TEST’ position.
7. Execute the oscilloscope USB compliance software.
8. Repeat the above steps in order to re-test TUSB216I with a different BOOST setting (must reset to change)

8.2.3 Application Curves

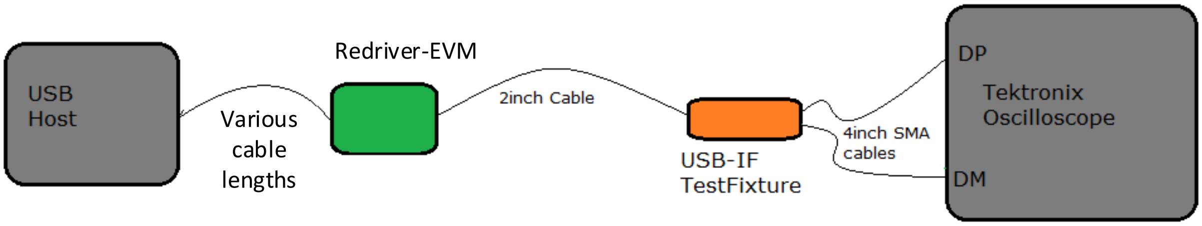

図 8-2. Near End Eye Measurement Set-Up With Pre-Channel Cable

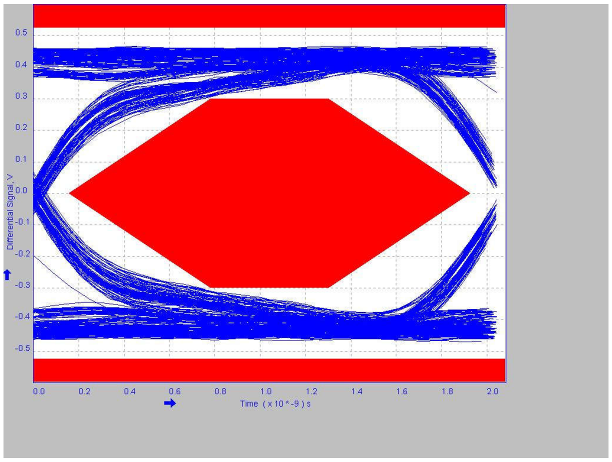

図 8-3. 2 Meter Pre-Channel Without TUSB216I

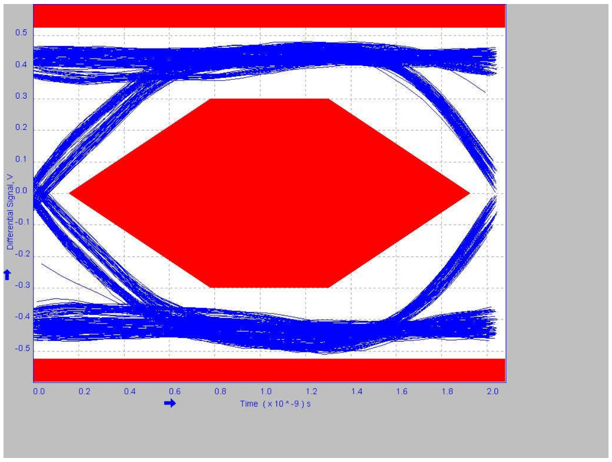

図 8-4. 2 Meter Pre-Channel With TUSB216I BOOST=1 RX_SEN=MED

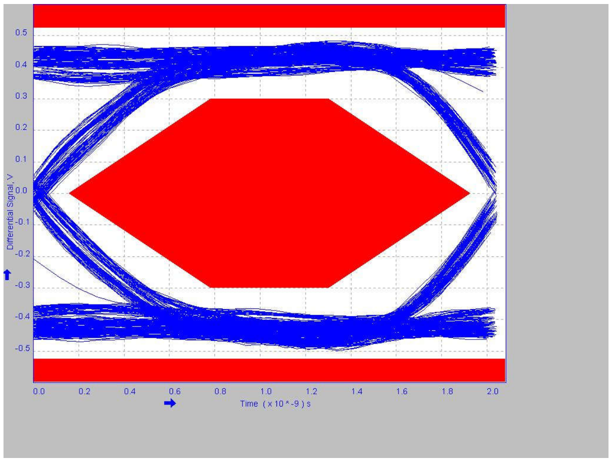

図 8-5. 2 Meter Pre-Channel With TUSB216I BOOST=0 RX_SEN=HIGH

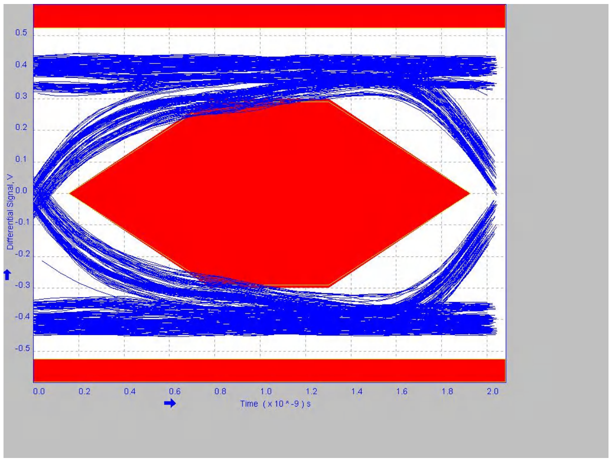

図 8-6. 3 Meter Pre-Channel Without TUSB216I

8.2.3 Application Curves (continued)

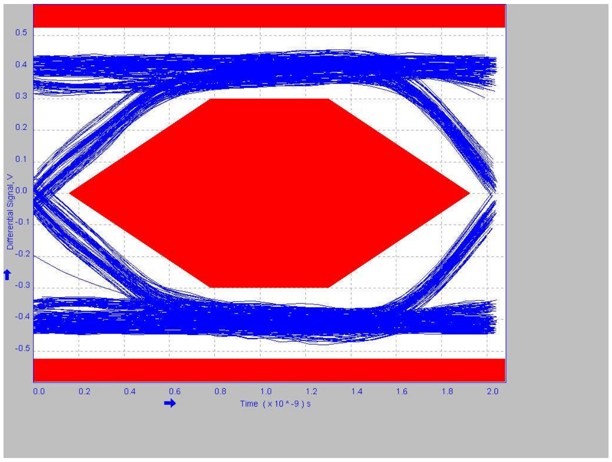

図 8-7. 3 Meter Pre-Channel With TUSB216I BOOST=0 RX_SEN=HIGH

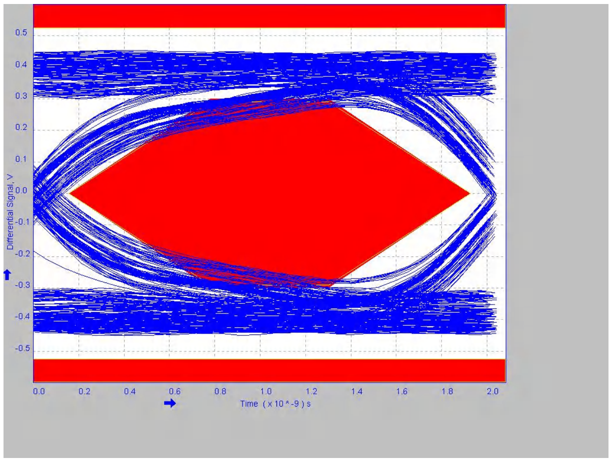

図 8-8. 5 Meter Without TUSB216I

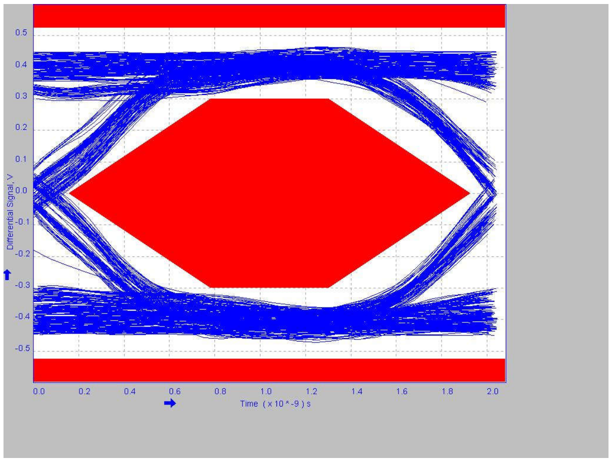

図 8-9. 5 Meter Pre-Channel With TUSB216I BOOST=1 RX_SEN=MED

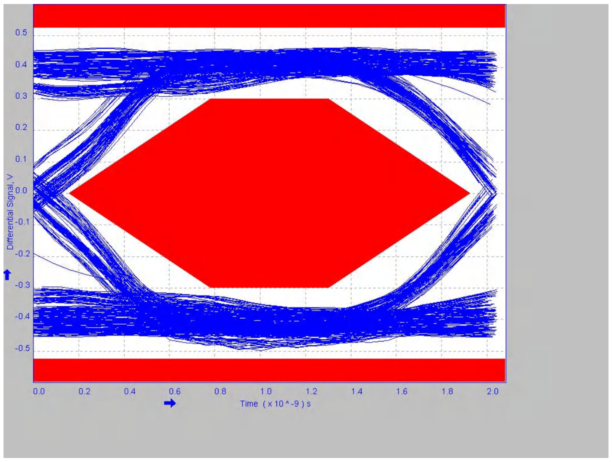

図 8-10. 5 Meter Pre-Channel With TUSB216I BOOST=2 RX_SEN=MED

8.2.3 Application Curves

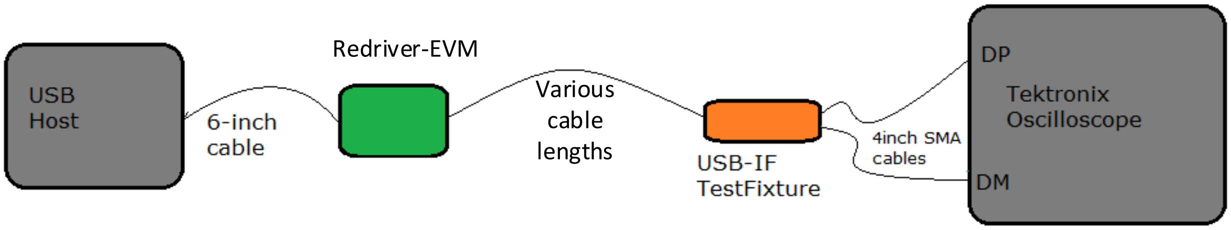

図 8-11. Near End Eye Measurement Set-Up With Post-Channel Cable

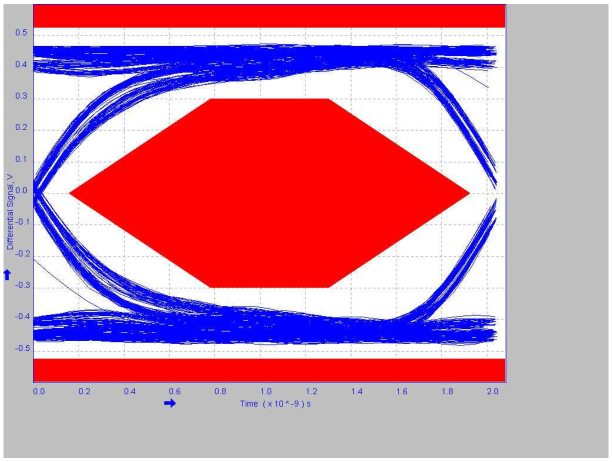

図 8-12. 6 Inches Post Channel Without TUSB216I

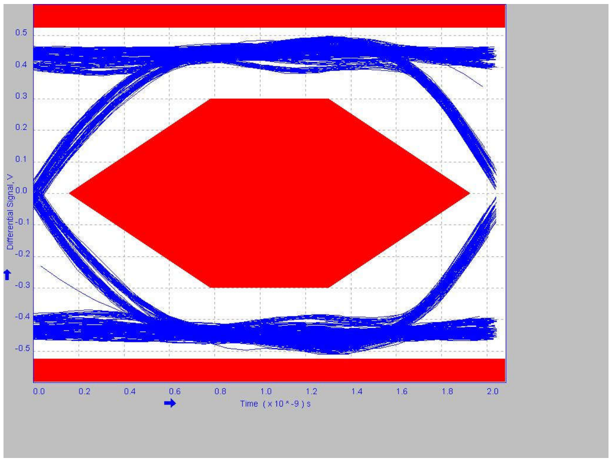

図 8-13. 6 Inches Post-Channel With TUSB216I BOOST=0 RX_SEN=HIGH

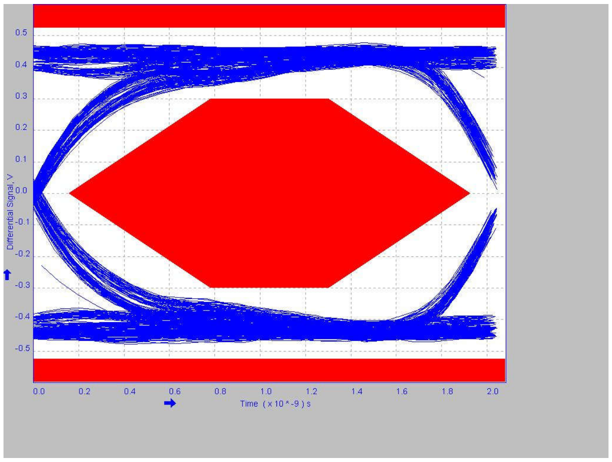

図 8-14. 1 Meter Post-Channel Without TUSB216I

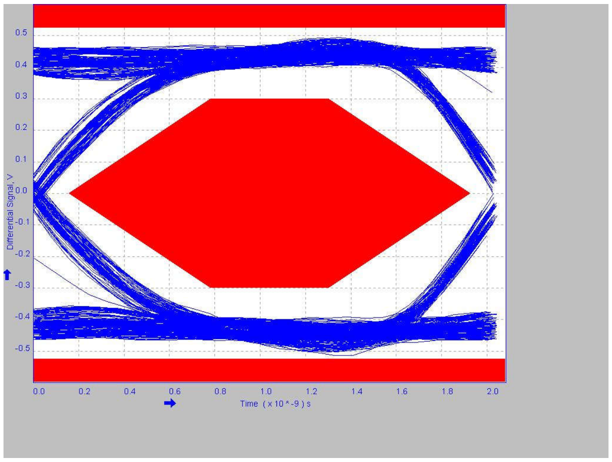

図 8-15. 1 Meter Post-Channel With TUSB216I BOOST=0 RX_SEN=MED

8.2.3 Application Curves (continued)

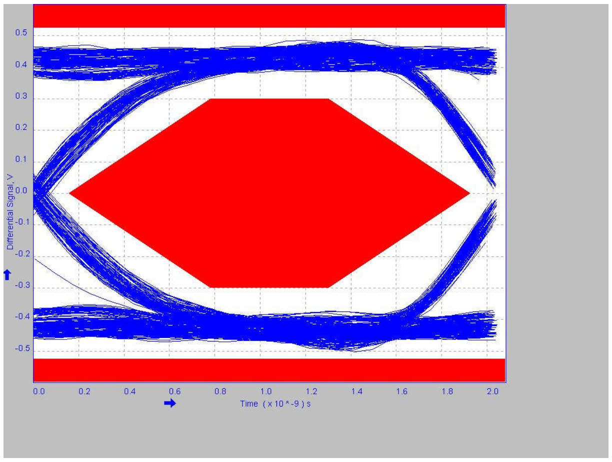

図 8-16. 1 Meter Post-Channel With TUSB216I BOOST=0 RX_SEN=HIGH

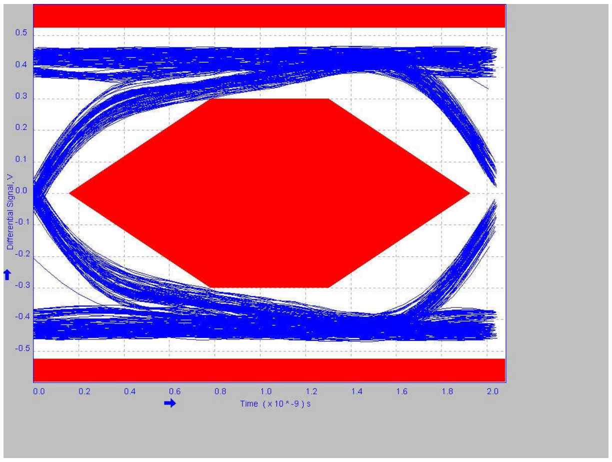

図 8-17. 2 Meter Post-Channel Without TUSB216I

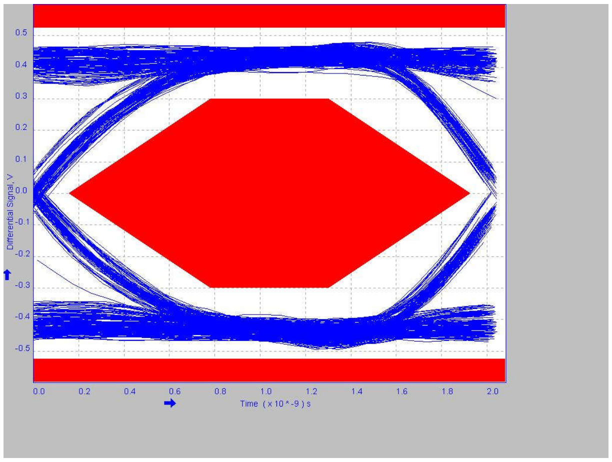

図 8-18. 2 Meter Post-Channel With TUSB216I BOOST=1 RX_SEN=MED

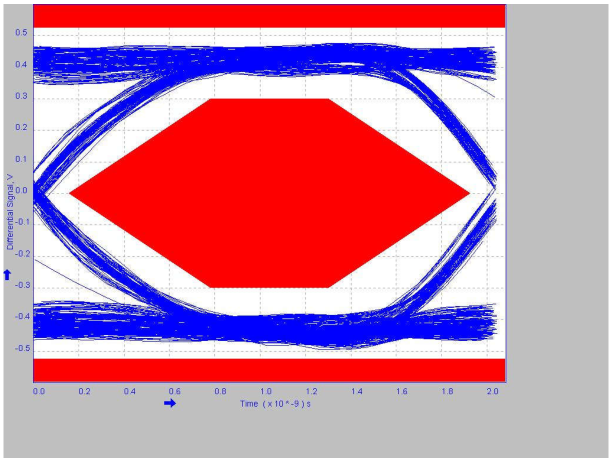

図 8-19. 2 Meter Post-Channel With TUSB216I BOOST=1 RX_SEN=HIGH

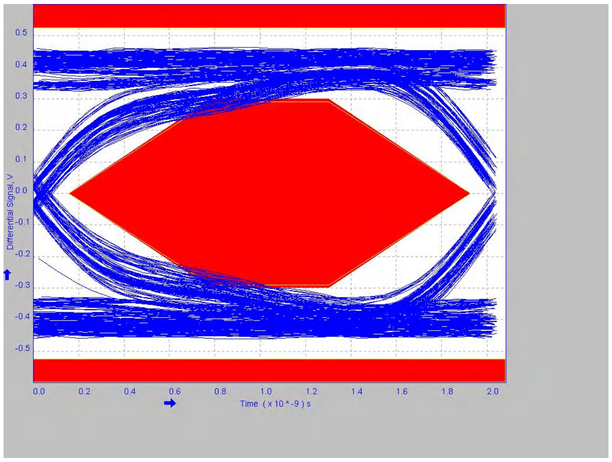

図 8-20. 4 Meter Post-Channel Without TUSB216I

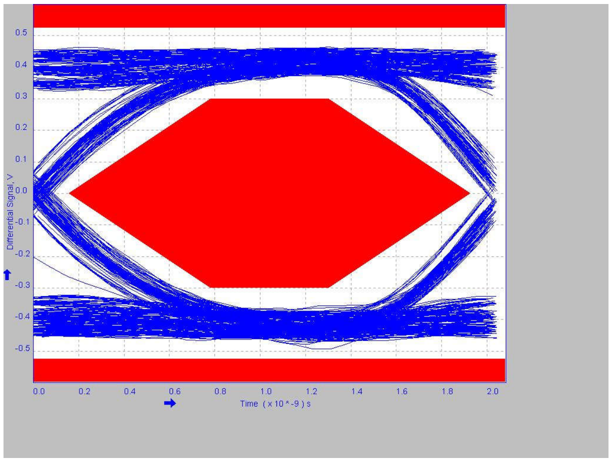

図 8-21. 4 Meter Post-Channel With TUSB216I BOOST=2 RX_SEN=MED

8.3 Power Supply Recommendations

On power up, the interaction of the RSTN pin and power on ramp could result in digital circuits not being set correctly. The device should not be enabled until the power on ramp has settled to minimum recommended supply voltage or higher to ensure a correct power on reset of the digital circuitry. If RSTN cannot be held low by microcontroller or other circuitry until the power on ramp has settled, then an external capacitor from the RSTN pin to GND is required to hold the device in the low power reset state.

The RC time constant should be larger than five times of the power on ramp time (0 to V_{CC}). With a typical internal pullup resistance of 500 kΩ, the recommended minimum external capacitance is calculated as:

$$[\text{Ramp Time x } 5] \div [500\ \text{k}\Omega] \tag{1}$$

8.4 Layout

8.4.1 Layout Guidelines

Although the land pattern has matched trace width to pad width, optimal impedance control is based on the user's own PCB stack-up. The recommendation is to maintain 90 Ω differential routing underneath the device.

8.4.2 Layout Example

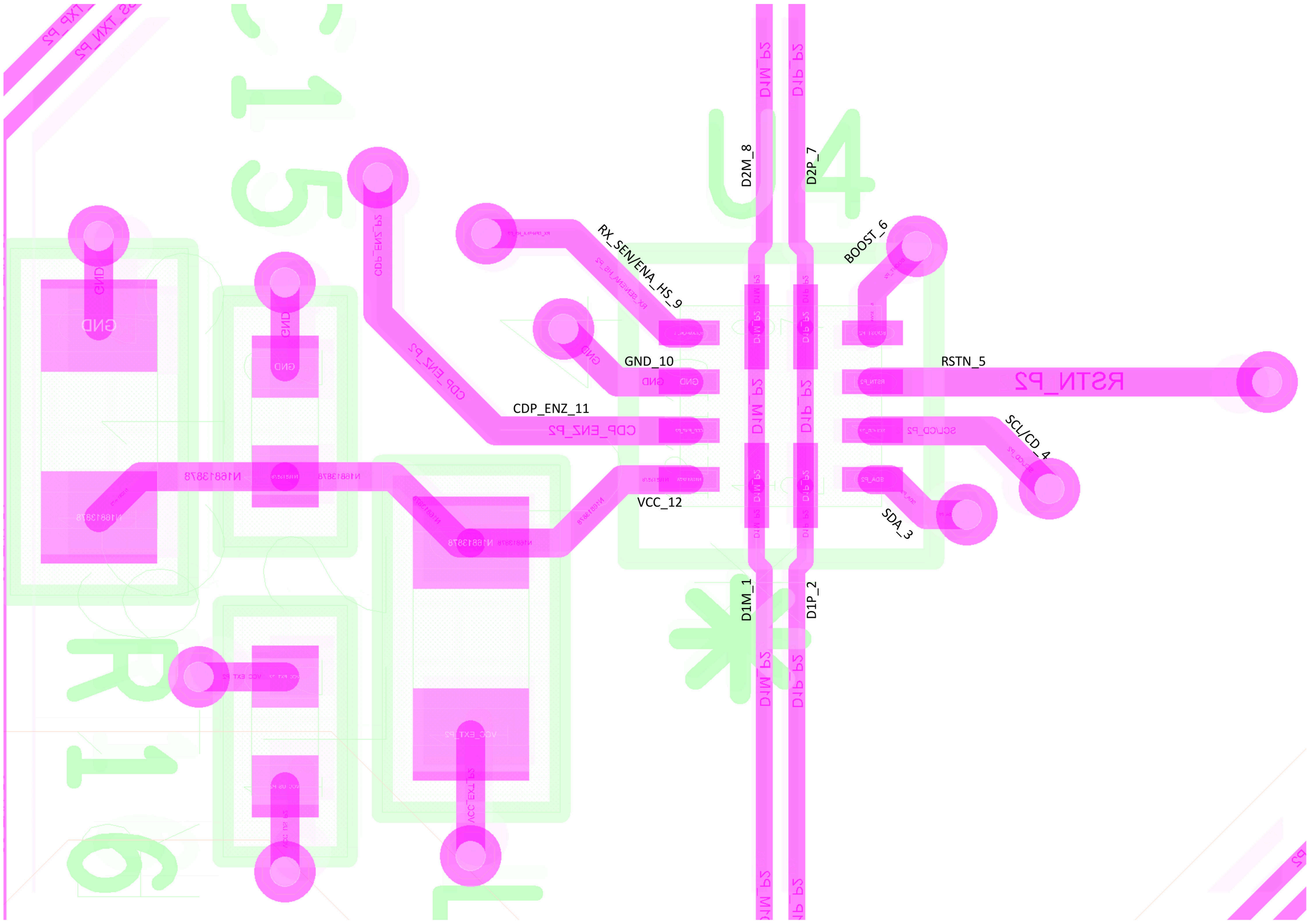

図 8-22. Layout Example

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2021) to Revision A (December 2023)	Page
• Added *Device Comparison* section	2
• Added 400 kHz I2C support	6
• Added timing table for 400 kHz I2C Fast Mode	8
• Added I2C standard and fast mode support in Detailed Description	10

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TUSB216IRWBR	ACTIVE	X2QFN	RWB	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6I	Samples
TUSB216IRWBT	ACTIVE	X2QFN	RWB	12	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	6I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

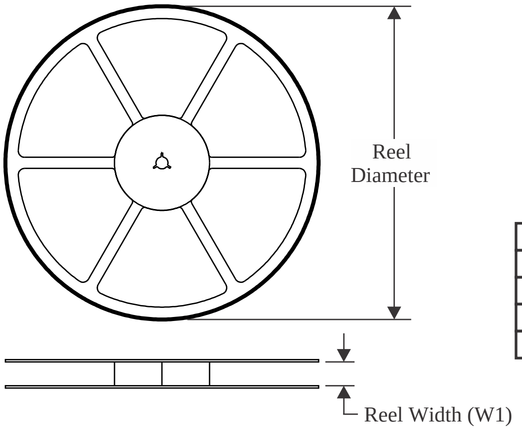
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

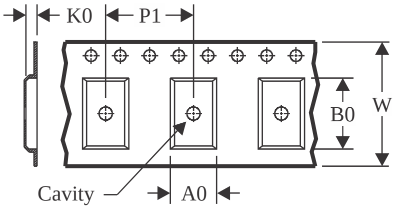
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

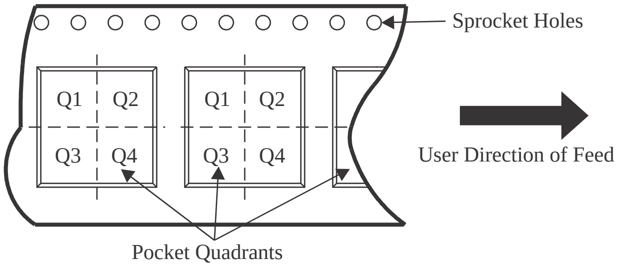


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

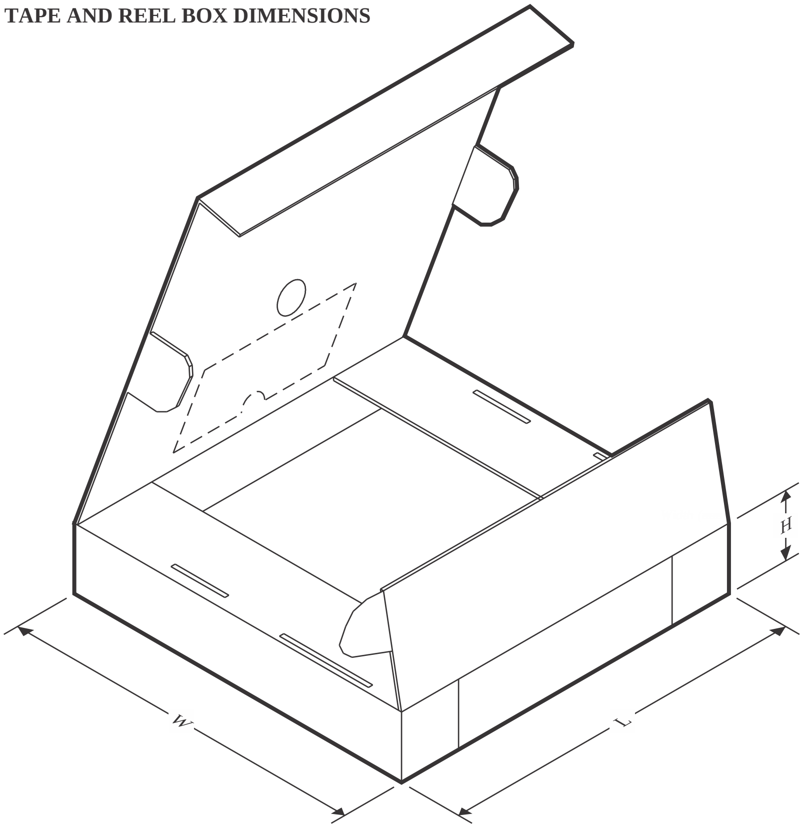
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

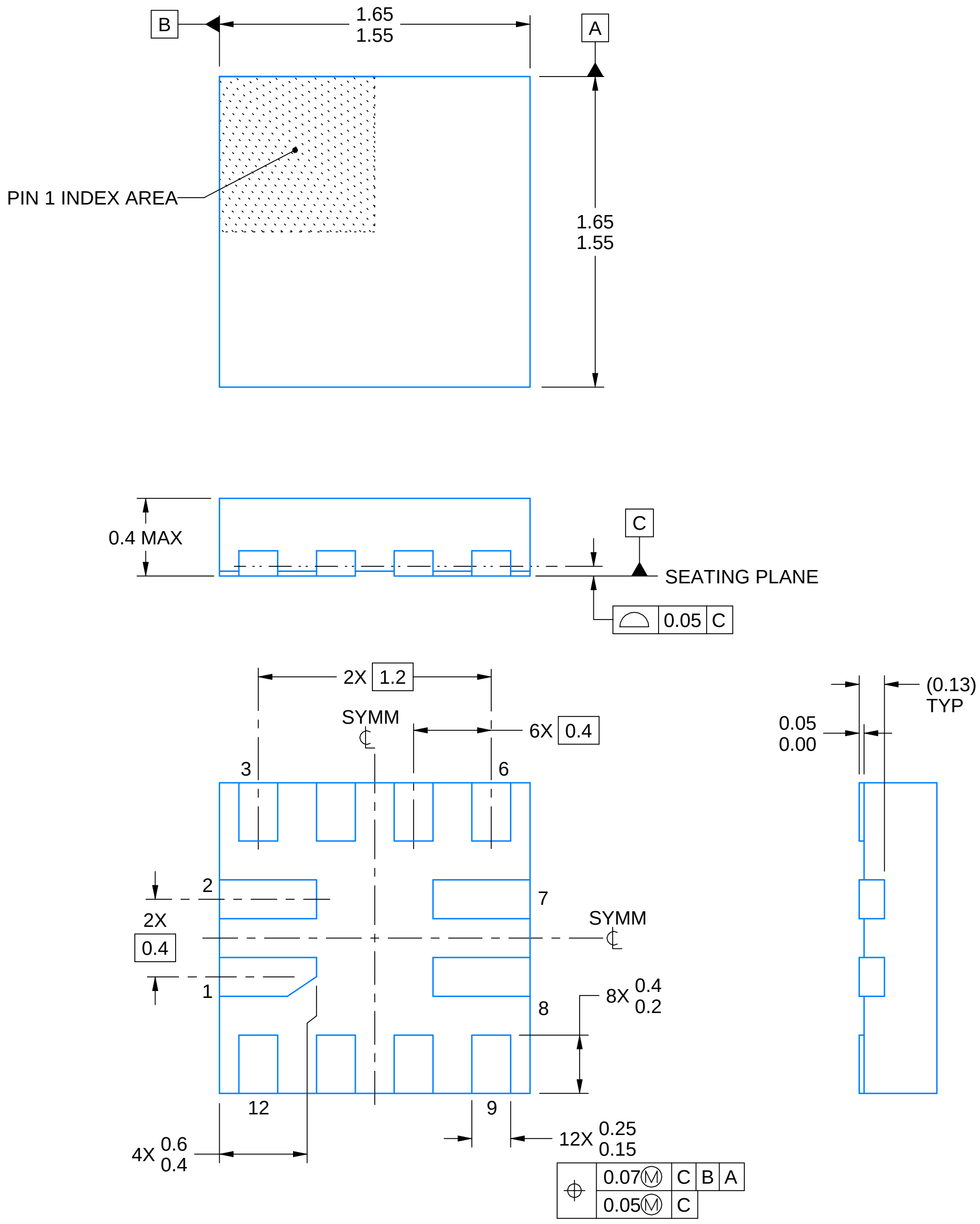
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB216IRWBR	X2QFN	RWB	12	3000	180.0	9.5	1.8	1.8	0.45	4.0	8.0	Q1
TUSB216IRWBT	X2QFN	RWB	12	250	180.0	9.5	1.8	1.8	0.45	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB216IRWBR	X2QFN	RWB	12	3000	189.0	185.0	36.0
TUSB216IRWBT	X2QFN	RWB	12	250	189.0	185.0	36.0



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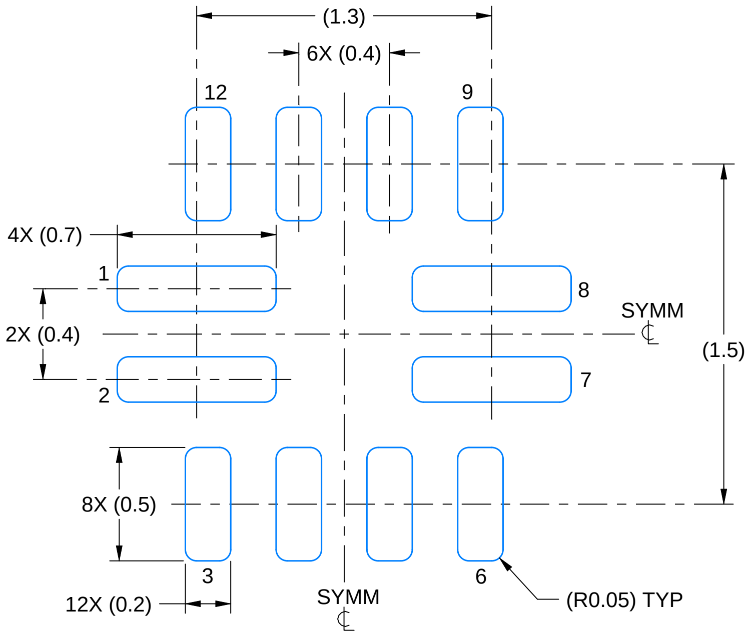
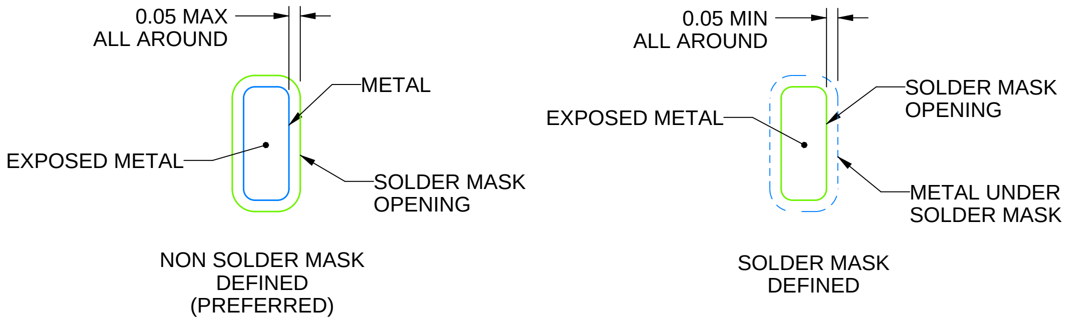
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDER MASK DETAILS

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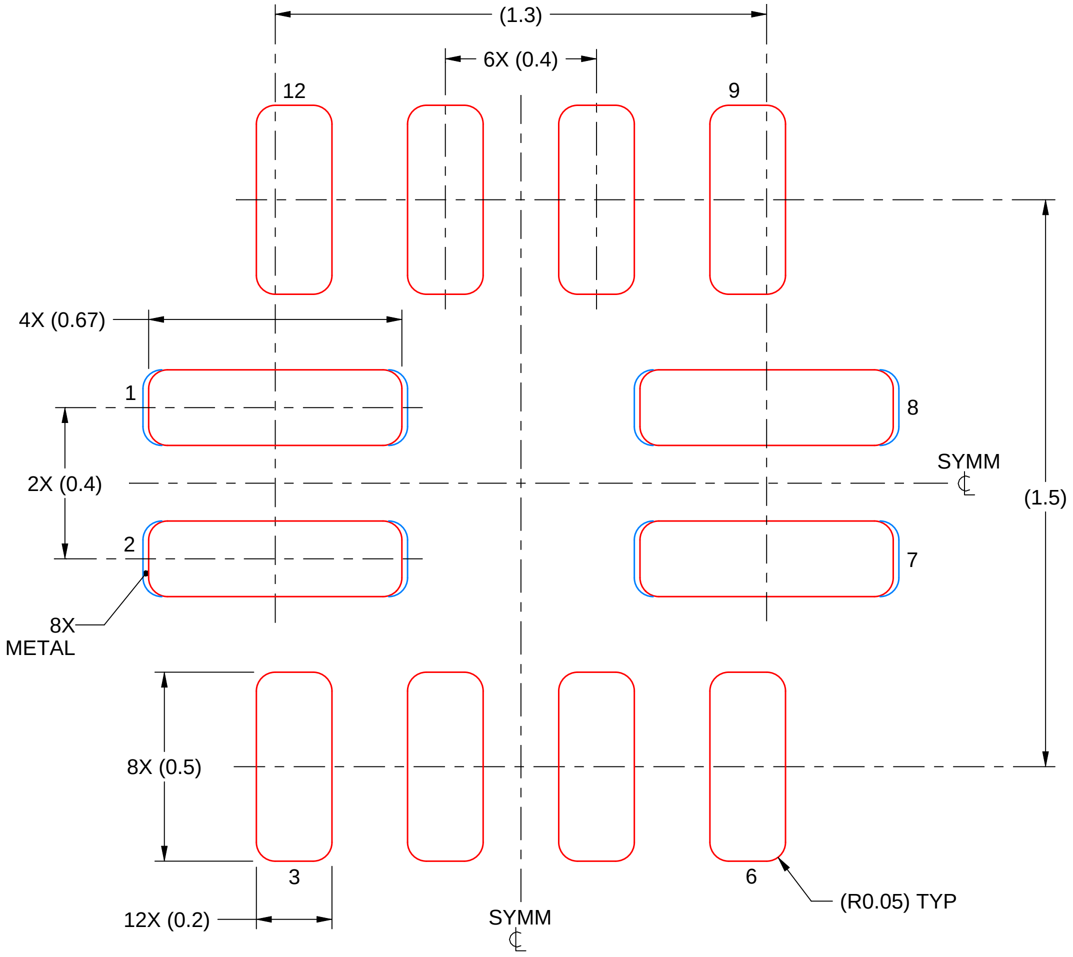
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PADS 1,2,7 & 8
96% PRINTED SOLDER COVERAGE BY AREA
SCALE:50X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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