TS5A3167 0.9Ω、1チャネルの1:1 SPSTアナログ・スイッチ

1 特長

- 電源オフ・モード、V_{CC} = 0時に絶縁
- 低いオン抵抗(0.9Ω)
- 制御入力は5.5V許容
- 低い電荷注入
- 低い全高調波歪(THD)
- 1.65V～5.5Vの単電源で動作
- JESD 78, Class II準拠で100mA超のラッチアップ性能
- ESD性能はJESD 22に準拠しテスト済み
  - 人体モデルで2000V (A114-B、クラスII)
  - 1000V、荷電デバイス・モデル(C101)

2 アプリケーション

- 携帯電話
- PDA
- ポータブル機器
- オーディオおよびビデオ信号のルーティング
- 低電圧のデータ収集システム
- 通信用回路
- モデム
- ハードディスク
- コンピュータ・ペリフェラル
- ワイヤレス端末およびペリフェラル
- マイクロフォンのスイッチ - ノートブック・ドッキング

3 概要

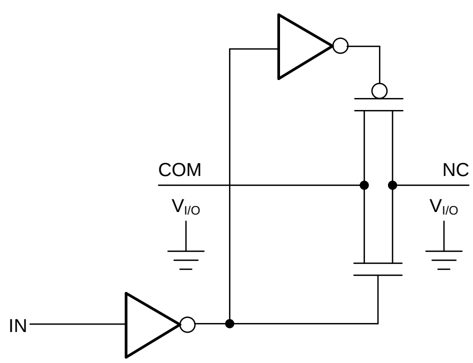
TS5A3167は双方向、シングル・チャネルの単極双投(SPDT)アナログ・スイッチであり、1.65V～5.5Vで動作するよう設計され、オン抵抗が低い特徴があります。このデバイスは全高調波歪み(THD)特性が非常に優れており、極めて低消費電力です。これらの特長から、このデバイスは携帯用オーディオ・アプリケーションに適しています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TS5A3167	SOT-23	2.90mm×1.60mm
	SC70	2.00mm×1.25mm
	DSBGA	1.50mm×0.90mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

単純な回路図



English Data Sheet: SCDS187

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (March 2017) から **Revision C** に変更 — **Page**

- 「*製品情報*」表でDSBGA本体サイズを「1.50mm×9.00mm」から「1.50mm×0.90mm」に変更 ... 1
- Changed the YZP package pinout view From: Top View To: Bottom View ... 3

Revision A (October 2012) から **Revision B** に変更 — **Page**

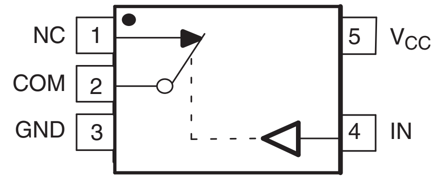
- 「*製品情報*」表、「*ピン構成および機能*」セクション、「*ESD定格*」セクション、「*推奨動作条件*」セクション、「*熱に関する情報*」セクション、「*詳細説明*」セクション、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト、デバイス、およびドキュメントのサポート*」セクションを追加 ... 1
- 「*注文情報*」表を削除 ... 1

2005年2月 発行のものから更新 — **Page**

- 「*注文情報*」表を更新 ... 1

5 Pin Configuration and Functions

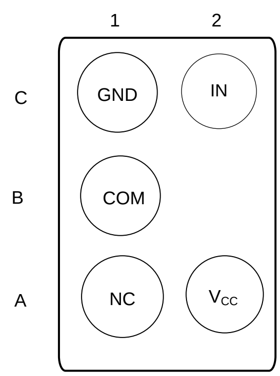
DBV or DCK Package
5- Pin (SOT-23 or SC70)
Top View



Pin Functions

PIN NUMBER	NAME	DESCRIPTION
1	NC	Normally Closed
2	COM	Common
3	GND	Ground
4	IN	Digital control pin, COM connected to NC when logic low
5	V_{CC}	Power Supply

YZP Package
5-Pin (DSBGA)
Bottom View



Pin Functions

PIN NUMBER	NAME	DESCRIPTION
A1	NC	Normally Closed
B1	COM	Common
C1	GND	Ground
A2	V_{CC}	Power Supply
C2	IN	Digital control pin, COM connected to NC when logic low

6 Specifications

6.1 Absolute Maximum Ratings[1][2]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range[3]		–0.5	6.5	V
V_{NC} V_{COM}	Analog voltage range[3][4][5]		–0.5	V_{CC} + 0.5	V
I_K	Analog port diode current	V_{NC}, V_{COM} < 0	–50		mA
I_{NC} I_{COM}	On-state switch current	V_{NC}, V_{COM} = 0 to V_{CC}	–200	200	mA
	On-state peak switch current[6]		–400	400	
V_I	Digital input voltage range[3][4]		–0.5	6.5	V
I_{IK}	Digital clamp current	V_I < 0	–50		mA
I_{CC}	Continuous current through V_{CC}			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(5) This value is limited to 5.5 V maximum.
(6) Pulse at 1-ms duration < 10% duty cycle.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	1.65	5.5	V
V_{NC} V_{COM}	Analog voltage range	0	V_{CC}	V
V_I	Digital input voltage range	0	V_{CC}	V

6.4 Thermal Information

THERMAL METRIC[1]		TS5A3167			UNIT
		DBV (SOT-23)	DCK (SOT-23)	YZP (DSBGA)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	230.3	268.0	146.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	111.9	171.8	1.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	69.5	64.5	39.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	33.0	40.5	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	69.0	62.9	39.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics for 5-V Supply(1)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_{CC}$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.8	1.1	Ω
				Full				1.2	
ON-state resistance	r_{on}	V_{NC} = 2.5 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.75	0.9	Ω
				Full				1	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_{CC}$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	4.5 V		0.2		Ω
		V_{NC} = 1 V, 1.5 V, 2.5 V, I_{COM} = –100 mA,		25°C			0.15	0.25	
				Full				0.25	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 4.5 V, or V_{NC} = 4.5 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	0	4	20	nA
				Full		–150		150	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 5.5 V, V_{COM} = 5.5 V to 0,		25°C	0 V	–10	0.2	10	μA
				Full		–50		50	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 4.5 V, or V_{COM} = 4.5 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	5.5 V	0	4	20	nA
				Full		–150		150	
	$I_{COM(PWROFF)}$	V_{COM} = 5.5 V to 0, V_{NC} = 0 to 5.5 V,		25°C	0 V	–10	0.2	10	μA
				Full		–50		50	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 4.5 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–5	0.4	5	nA
				Full		–50		50	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 4.5 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	5.5 V	–5	0.4	5	nA
				Full		–20		20	
Digital Control Inputs (IN)									
Input logic high	V_{IH}			Full		2.4		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	5.5 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.6 Electrical Characteristics for 5-V Supply(1) (continued)

V_{CC} = 4.5 V to 5.5 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	VCC	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	1	4.5	7.5	ns
				Full	4.5 V to 5.5 V	1		9	
Turn-off time	t_{OFF}	V_{COM} = V_{CC}, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	5 V	4.5	8	11	ns
				Full	4.5 V to 5.5 V	3.5		13	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0 ,	C_L = 1 nF, See Figure 20	25°C	5 V		6		pC
NC OFF capacitance	$C_{NC(OFF)}$	V_{NC} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	5 V		19		pF
COM OFF capacitance	$C_{COM(OFF)}$	V_{COM} = V_{CC} or GND,	Switch OFF, See Figure 16	25°C	5 V		18		pF
NC ON capacitance	$C_{NC(ON)}$	V_{NC} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	5 V		35.5		pF
COM ON capacitance	$C_{COM(ON)}$	V_{COM} = V_{CC} or GND,	Switch ON, See Figure 16	25°C	5 V		35.5		pF
Digital input capacitance	C_I	V_I = V_{CC} or GND,	See Figure 16	25°C	5 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 18	25°C	5 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	5 V		–62		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	5 V		0.005%		
Supply									
Positive supply current	I_{CC}	V_I = V_{CC} or GND,	Switch ON or OFF	25°C	5.5 V		0.01	0.1	µA
				Full				1	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.7 Electrical Characteristics for 3.3-V Supply(1)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	$0 \le V_{NC} \le V_{CC}$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1.3	1.6	Ω
				Full				1.8	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		1.1	1.5	Ω
				Full				1.7	
ON-state resistance flatness	$r_{on(flat)}$	$0 \le V_{NC} \le V_{CC}$, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	3 V		0.3		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.15	0.25	
				Full				0.25	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–5	0.5	5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–5	0.1	5	µA
				Full		–25		25	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	3.6 V	–5	0.5	5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 3.6 V to 0, V_{NC} = 0 to 3.6 V,		25°C	0 V	–5	0.1	5	µA
				Full		–25		25	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
Input logic high	V_{IH}			Full		2		5.5	V
Input logic low	V_{IL}			Full		0		0.8	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	3.6 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.8 Electrical Characteristics for 3.3-V Supply[(1)] (continued)

V_{CC} = 3 V to 3.6 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	VCC	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	1.5	5	9.5	ns
				Full	3 V to 3.6 V	1.0		10	
Turn-off time	t_{OFF}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	3.3 V	4.5	8.5	11	ns
				Full	3 V to 3.6 V	3		12.5	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 20	25°C	3.3 V		6		pC
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_{CC}$ or GND,	Switch OFF, See Figure 16	25°C	3.3 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND,	Switch OFF, See Figure 16	25°C	3.3 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_{CC}$ or GND,	Switch ON, See Figure 16	25°C	3.3 V		36		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND,	Switch ON, See Figure 16	25°C	3.3 V		36		pF
Digital input capacitance	C_I	$V_I = V_{CC}$ or GND,	See Figure 16	25°C	3.3 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 18	25°C	3.3 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	3.3 V		–62		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	3.3 V		0.01%		
Supply									
Positive supply current	I_{CC}	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	3.6 V		0.001	0.05	µA
				Full				0.3	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.9 Electrical Characteristics for 2.5-V Supply[1]

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.8	2.4	Ω
				Full				2.6	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		1.2	2.1	Ω
				Full				2.4	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	2.3 V		0.7		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			0.4	0.6	
				Full				0.6	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2	0.05	2	µA
				Full		–15		15	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	2.7 V	–5	0.3	5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 3.6 V to 0, V_{NC} = 0 to 3.6 V,		25°C	0 V	–2	0.05	2	µA
				Full		–15		15	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
Input logic high	V_{IH}			Full		1.8		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	2.7 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.10 Electrical Characteristics for 2.5-V Supply(1) (continued)

V_{CC} = 2.3 V to 2.7 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	VCC	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	2	6	10	ns
				Full	2.3 V to 2.7 V	1		12	
Turn-off time	t_{OFF}	$V_{COM} = V_{CC}$, R_L = 50 Ω,	C_L = 35 pF, See Figure 17	25°C	2.5 V	4.5	8	10.5	ns
				Full	2.3 V to 2.7 V	3		15	
Charge injection	Q_C	V_{GEN} = 0, R_{GEN} = 0,	C_L = 1 nF, See Figure 20	25°C	2.5 V		4		pC
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_{CC}$ or GND,	Switch OFF, See Figure 16	25°C	2.5 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND,	Switch OFF, See Figure 16	25°C	2.5 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_{CC}$ or GND,	Switch ON, See Figure 16	25°C	2.5 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND,	Switch ON, See Figure 16	25°C	2.5 V		36.5		pF
Digital input capacitance	C_I	$V_I = V_{CC}$ or GND,	See Figure 16	25°C	2.5 V		2		pF
Bandwidth	BW	R_L = 50 Ω,	Switch ON, See Figure 18	25°C	2.5 V		150		MHz
OFF isolation	O_{ISO}	R_L = 50 Ω, f = 1 MHz,	Switch OFF, See Figure 19	25°C	2.5 V		–62		dB
Total harmonic distortion	THD	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, See Figure 21	25°C	2.5 V		0.02%		
Supply									
Positive supply current	I_{CC}	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	2.7 V		0.001	0.02	µA
				Full				0.25	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.11 Electrical Characteristics for 1.8-V Supply(1)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	V_{CC}	MIN	TYP	MAX	UNIT
Analog Switch									
Peak ON resistance	r_{peak}	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		4.2	25	Ω
				Full				30	
ON-state resistance	r_{on}	V_{NC} = 2 V, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		1.6	3.9	Ω
				Full				4.0	
ON-state resistance flatness	$r_{on(flat)}$	0 ≤ V_{NC} ≤ V_{CC}, I_{COM} = –100 mA,	Switch ON, See Figure 13	25°C	1.65 V		2.8		Ω
		V_{NC} = 2 V, 0.8 V, I_{COM} = –100 mA,		25°C			4.1	22	
				Full				27	
NC OFF leakage current	$I_{NC(OFF)}$	V_{NC} = 1 V, V_{COM} = 3 V, or V_{NC} = 3 V, V_{COM} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
	$I_{NC(PWROFF)}$	V_{NC} = 0 to 3.6 V, V_{COM} = 3.6 V to 0,		25°C	0 V	–2		2	µA
				Full		–10		10	
COM OFF leakage current	$I_{COM(OFF)}$	V_{COM} = 1 V, V_{NC} = 3 V, or V_{COM} = 3 V, V_{NC} = 1 V,	Switch OFF, See Figure 14	25°C	1.95 V	–5		5	nA
				Full		–50		50	
	$I_{COM(PWROFF)}$	V_{COM} = 0 to 3.6 V, V_{NC} = 3.6 V to 0,		25°C	0 V	–2		2	µA
				Full		–10		10	
NC ON leakage current	$I_{NC(ON)}$	V_{NC} = 1 V, V_{COM} = Open, or V_{NC} = 3 V, V_{COM} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
COM ON leakage current	$I_{COM(ON)}$	V_{COM} = 1 V, V_{NC} = Open, or V_{COM} = 3 V, V_{NC} = Open,	Switch ON, See Figure 15	25°C	1.95 V	–2		2	nA
				Full		–20		20	
Digital Control Inputs (IN)									
Input logic high	V_{IH}			Full		1.5		5.5	V
Input logic low	V_{IL}			Full		0		0.6	V
Input leakage current	I_{IH}, I_{IL}	V_I = 5.5 V or 0		25°C	1.95 V	–2	0.3	2	nA
				Full		–20		20	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.12 Electrical Characteristics for 1.8-V Supply(1) (continued)

V_{CC} = 1.65 V to 1.95 V, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		T_A	VCC	MIN	TYP	MAX	UNIT
Dynamic									
Turn-on time	t_{ON}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	1.8 V	3	9	18	ns
				Full	1.65 V to 1.95 V	1		20	
Turn-off time	t_{OFF}	$V_{COM} = V_{CC}$, $R_L = 50\ \Omega$,	C_L = 35 pF, See Figure 17	25°C	1.8 V	5	10	15.5	ns
				Full	1.65 V to 1.95 V	4		18.5	
Charge injection	Q_C	$V_{GEN} = 0$, $R_{GEN} = 0$,	C_L = 1 nF, See Figure 20	25°C	1.8 V		2		pC
NC OFF capacitance	$C_{NC(OFF)}$	$V_{NC} = V_{CC}$ or GND,	Switch OFF, See Figure 16	25°C	1.8 V		19.5		pF
COM OFF capacitance	$C_{COM(OFF)}$	$V_{COM} = V_{CC}$ or GND,	Switch OFF, See Figure 16	25°C	1.8 V		18.5		pF
NC ON capacitance	$C_{NC(ON)}$	$V_{NC} = V_{CC}$ or GND,	Switch ON, See Figure 16	25°C	1.8 V		36.5		pF
COM ON capacitance	$C_{COM(ON)}$	$V_{COM} = V_{CC}$ or GND,	Switch ON, See Figure 16	25°C	1.8 V		36.5		pF
Digital input capacitance	C_I	$V_I = V_{CC}$ or GND,	See Figure 16	25°C	1.8 V		2		pF
Bandwidth	BW	$R_L = 50\ \Omega$,	Switch ON, See Figure 18	25°C	1.8 V		150		MHz
OFF isolation	O_{ISO}	$R_L = 50\ \Omega$, f = 1 MHz,	Switch OFF, See Figure 19	25°C	1.8 V		–62		dB
Total harmonic distortion	THD	$R_L = 600\ \Omega$, C_L = 50 pF,	f = 20 Hz to 20 kHz See Figure 21	25°C	1.8 V		0.055%		
Supply									
Positive supply current	I_{CC}	$V_I = V_{CC}$ or GND,	Switch ON or OFF	25°C	1.95 V		0.001	0.01	µA
				Full				0.15	

(1) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

6.13 Typical Performance

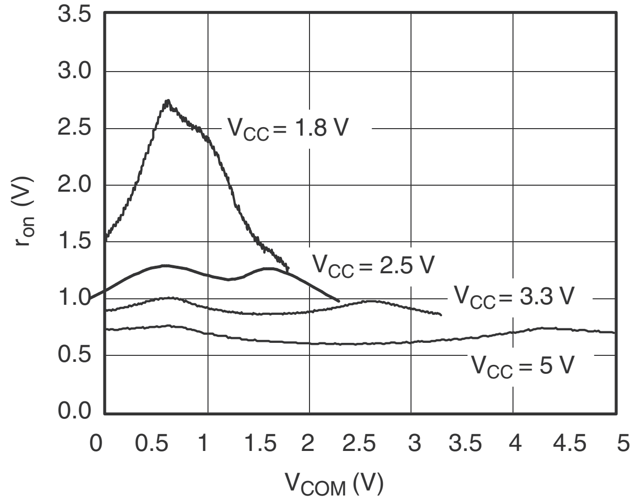


Figure 1. r_{on} vs V_{COM}

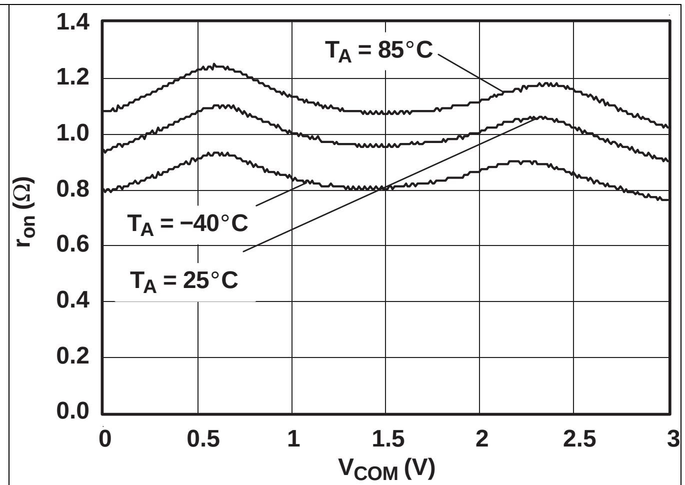


Figure 2. r_{on} vs V_{COM} (V_{CC} = 3 V)

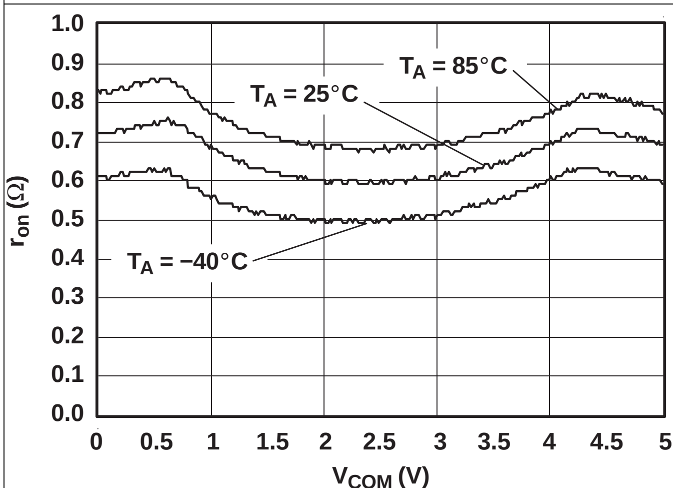


Figure 3. r_{on} vs V_{COM} (V_{CC} = 5 V)

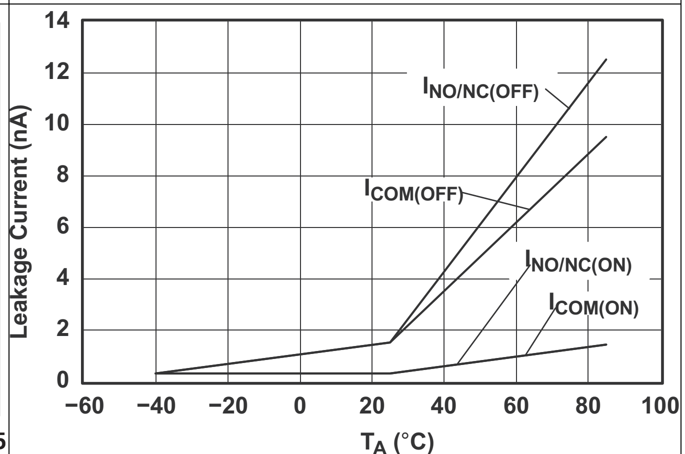


Figure 4. Leakage Current vs Temperature (V_{CC} = 5.5 V)

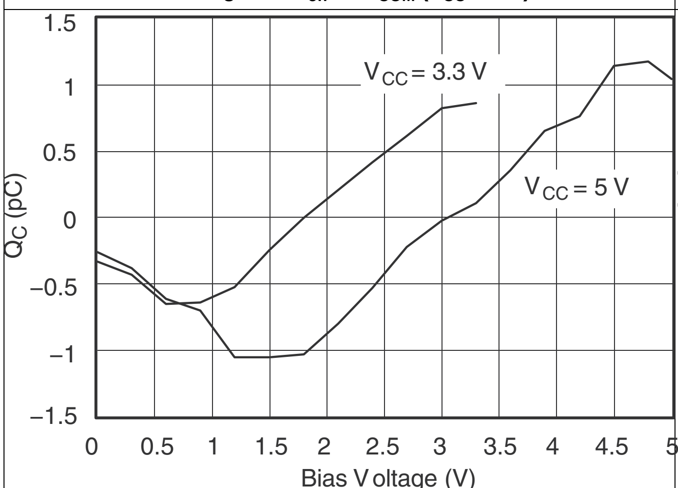


Figure 5. Charge Injection (Q_C) vs V_{COM}

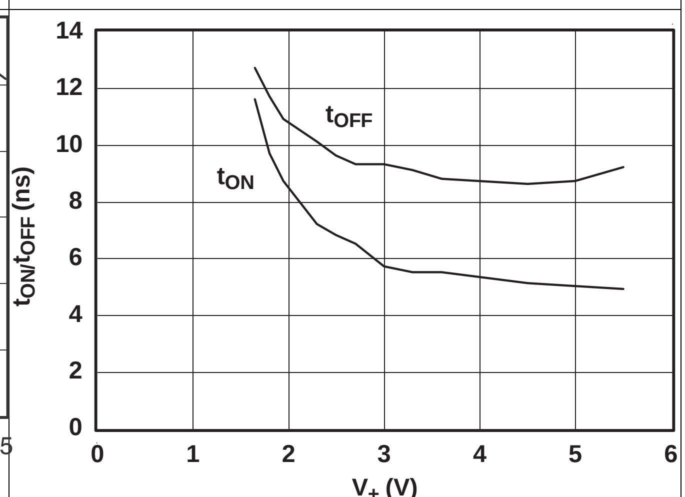


Figure 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Performance (continued)

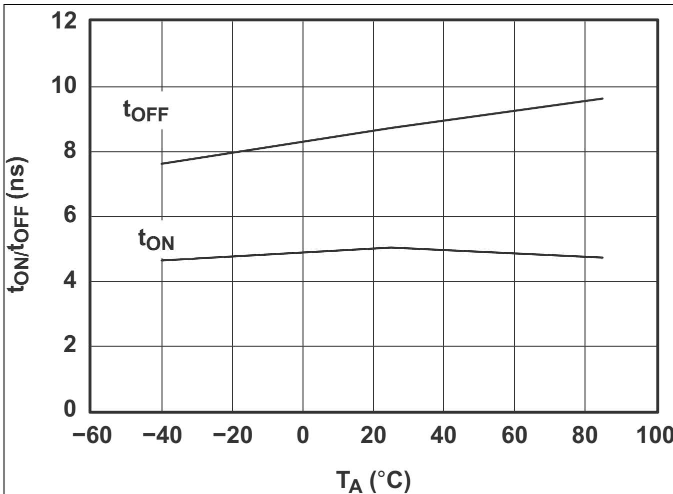


Figure 7. t_{ON} and t_{OFF} vs Temperature (V_{CC} = 5 V)

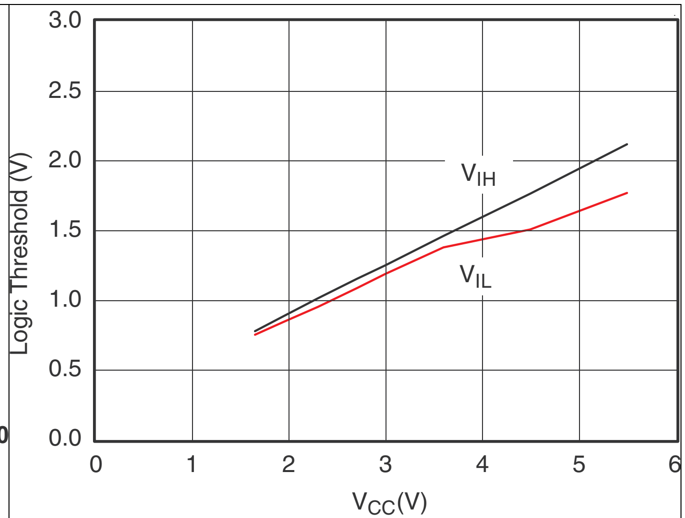


Figure 8. Logic Threshold vs V_{CC}

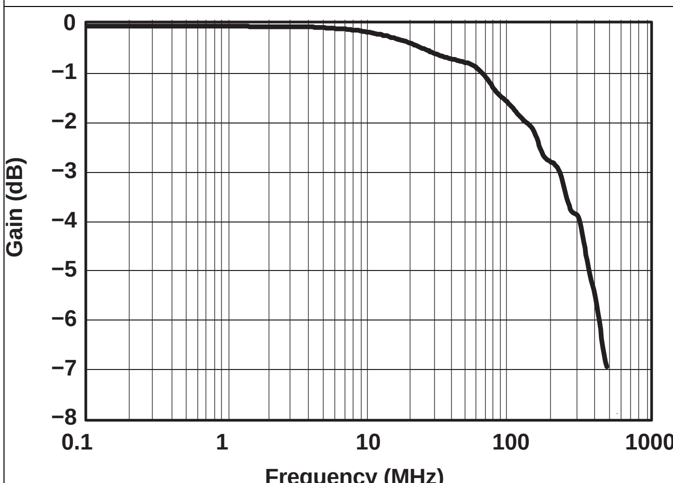


Figure 9. Gain vs Frequency (V_{CC} = 5 V)

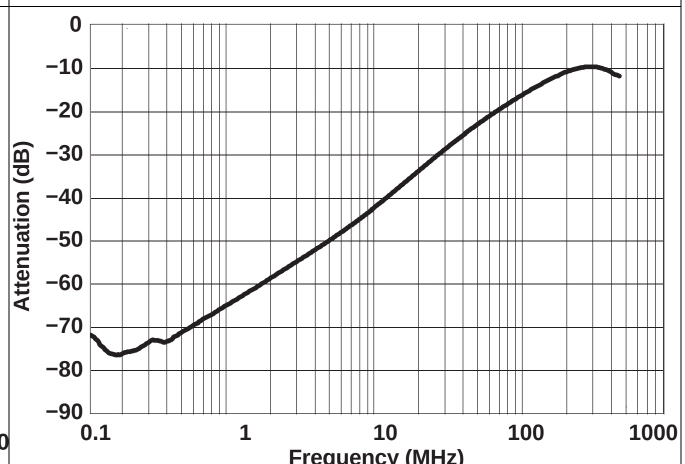


Figure 10. OFF Isolation vs Frequency (V_{CC} = 5 V)

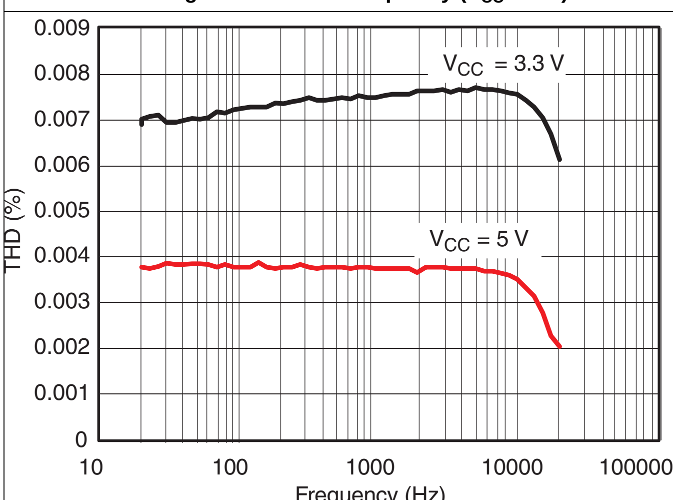


Figure 11. Total Harmonic Distortion vs Frequency (V_{CC} = 5 V)

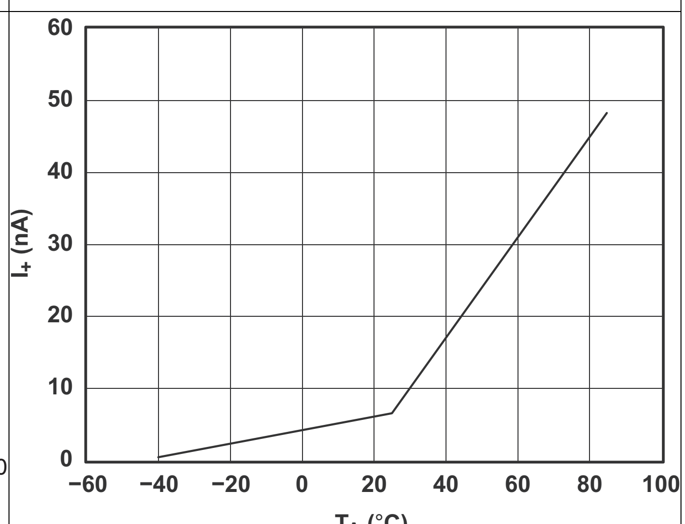


Figure 12. Power-Supply Current vs Temperature (V_{CC} = 5 V)

7 Parameter Measurement Information

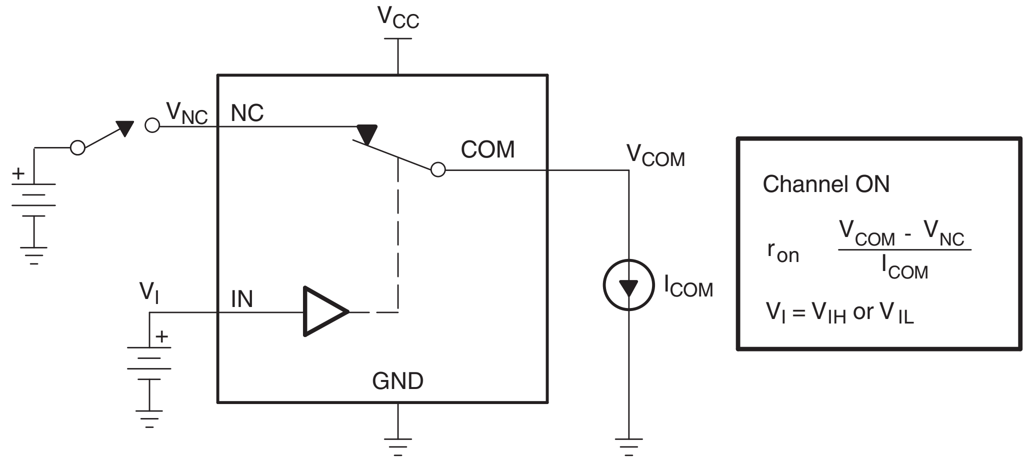


Figure 13. ON-State Resistance (r_{on})

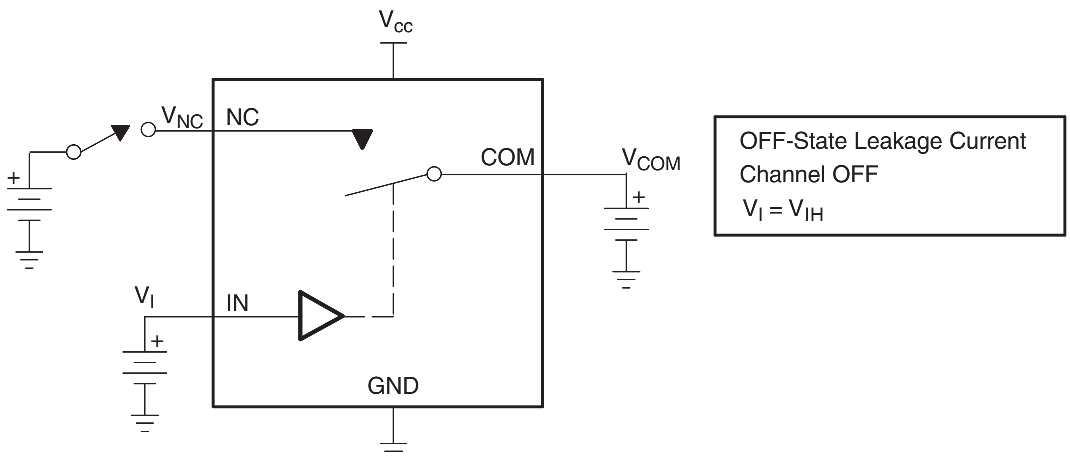


Figure 14. OFF-State Leakage Current ($I_{COM(OFF)}$, $I_{NC(OFF)}$, $I_{COM(PWROFF)}$, $I_{NC(PWROFF)}$)

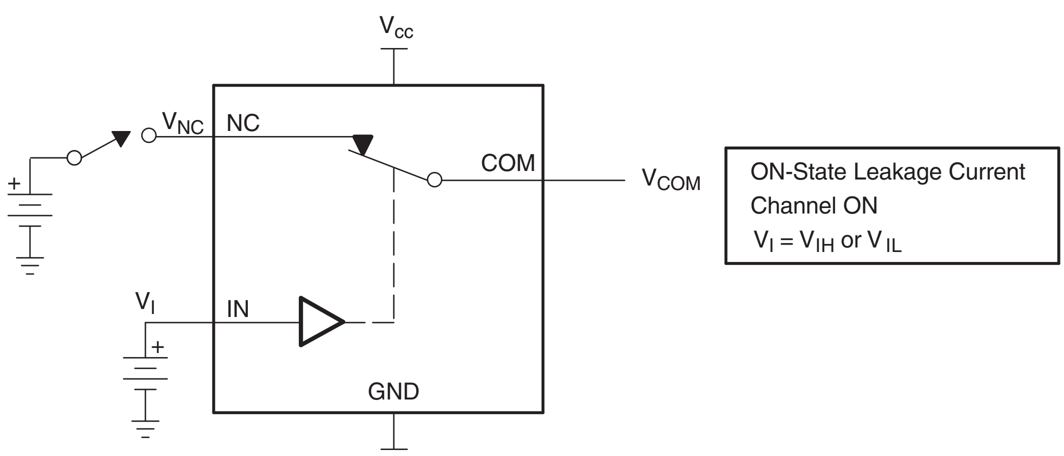


Figure 15. ON-State Leakage Current ($I_{COM(ON)}$, $I_{NC(ON)}$)

Parameter Measurement Information (continued)

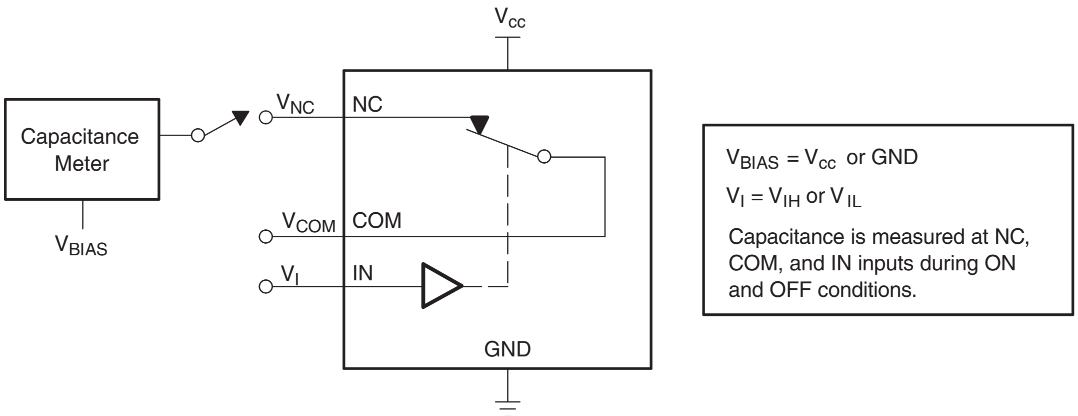
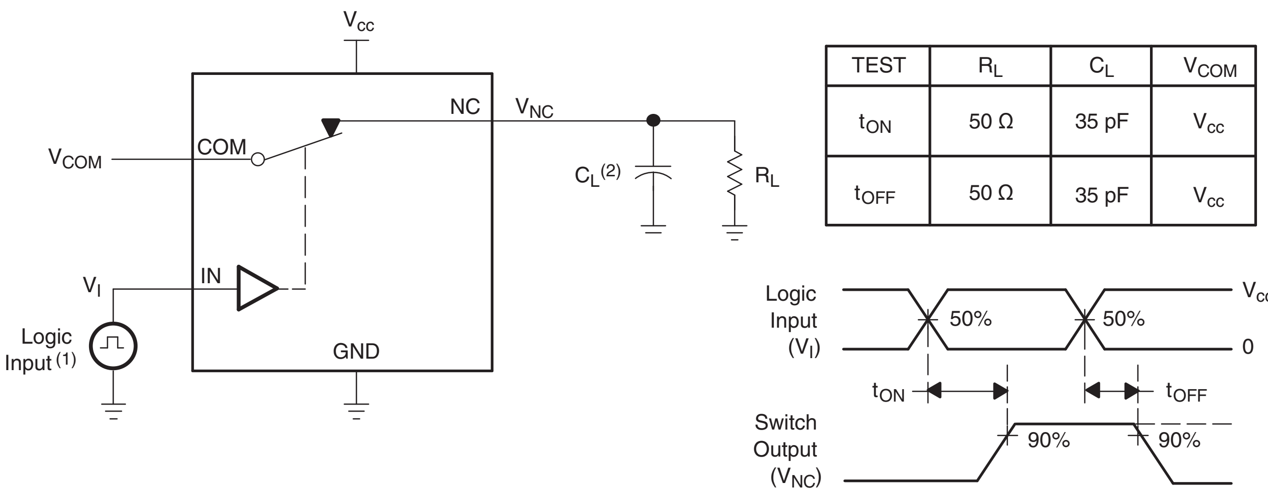


Figure 16. Capacitance (C_I, $C_{COM(OFF)}$, $C_{COM(ON)}$, $C_{NC(OFF)}$, $C_{NC(ON)}$)



TEST	R_L	C_L	V_{COM}
t_{ON}	50 Ω	35 pF	V_{CC}
t_{OFF}	50 Ω	35 pF	V_{CC}

(1) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

(2) C_L includes probe and jig capacitance.

Figure 17. Turn-On (t_{ON}) and Turn-Off Time (t_{OFF})

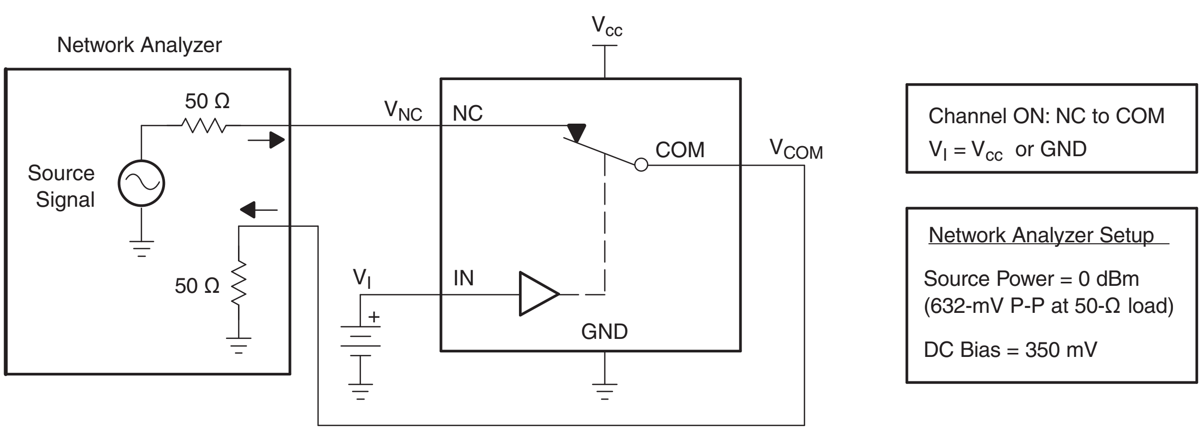


Figure 18. Bandwidth (BW)

Parameter Measurement Information (continued)

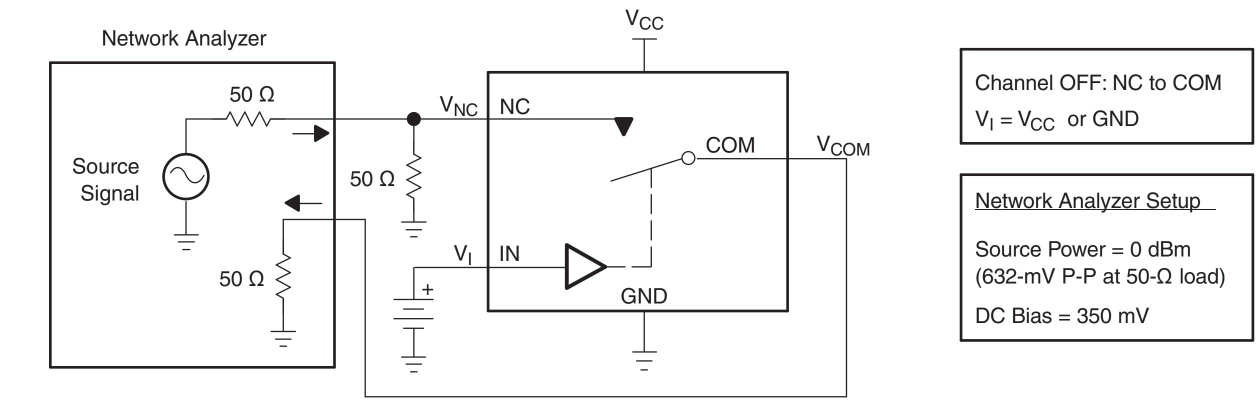
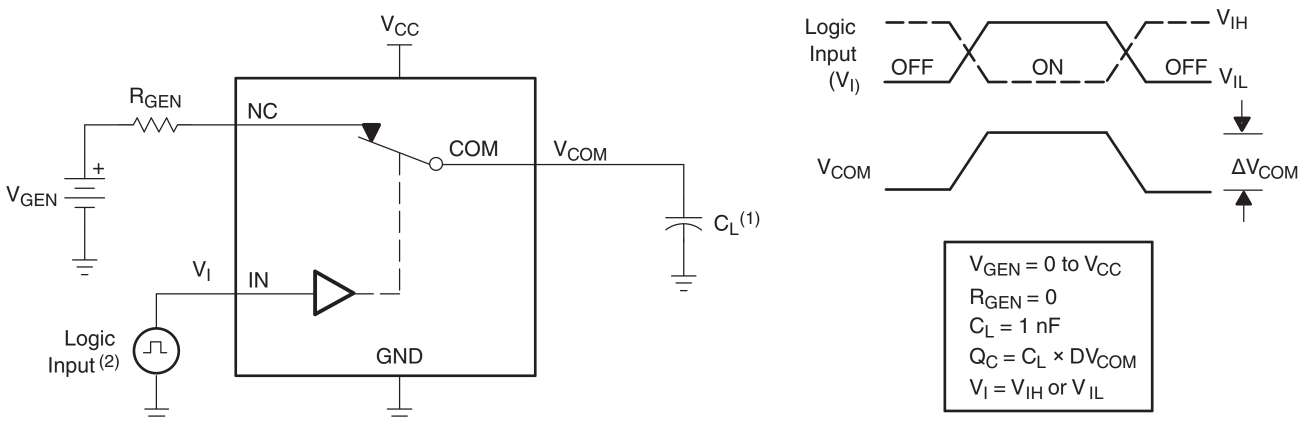


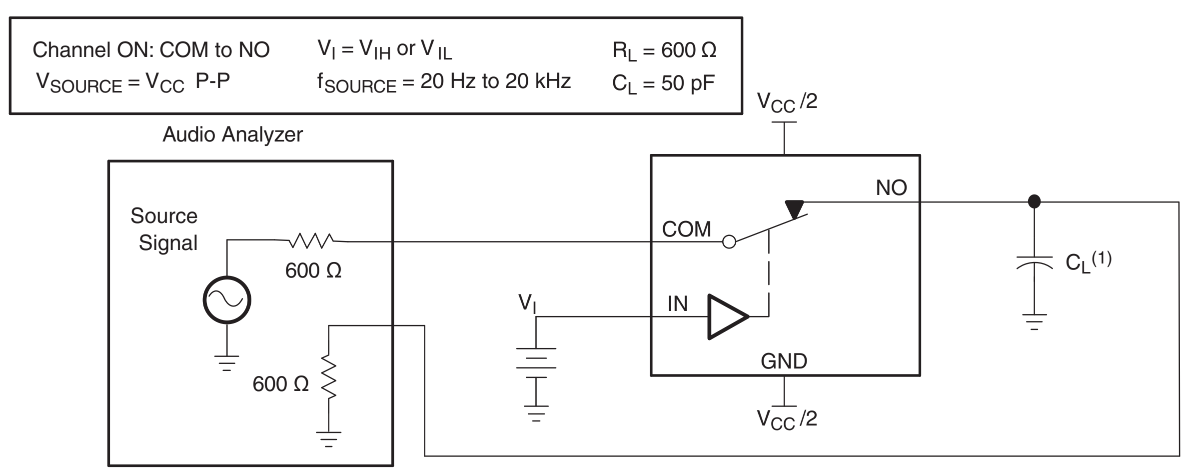
Figure 19. OFF Isolation (O_{ISO})



(1) C_L includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

Figure 20. Charge Injection (Q_C)



(1) C_L includes probe and jig capacitance.

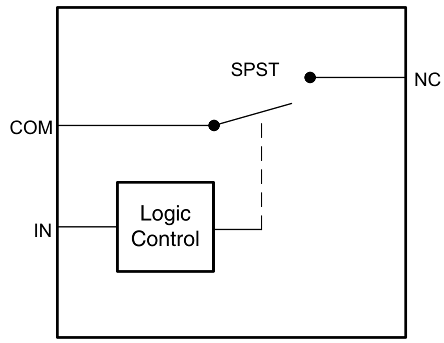
Figure 21. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS5A3167 is a bidirectional, single-channel, single-pole single-throw (SPST) analog switch that is designed to operate from 1.65 V to 5.5 V. This device provides a signal switching solution while maintaining excellent signal integrity, which makes the TS5A3367 suitable for a wide range of applications in various markets including personal electronics, portable instrumentation, and test and measurement equipment. The device maintains the signal integrity by its low ON-state resistance, excellent ON-state resistance matching, and total harmonic distortion (THD) performance. The device consumes very low power and provides isolation when VCC = 0.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Isolation in Powered-Off Mode, V_{CC} = 0

When power is not supplied to the V_{CC} pin, V_{CC} = 0 , the signal paths NC and COM are high impedance. This is specificed in the electrical characterisitics table under the COM and NC OFF leakage current when V_{CC} = 0. Because the device is high impedance when it is not powered, you may connect other signals to the signal chain without interference of the TS5A3167.

8.4 Device Functional Modes

Placing a logic low signal on the IN pin of the device will turn on the switch and provide a low impedance path from NC to COM.

Table 1. Function Table

IN	NC TO COM, COM TO NC
L	ON
H	OFF

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS5A3167 switch is bidirectional, so the NC and COM pins can be used as either inputs or outputs. This switch is typically used when there is one signal path that needs to be isolated at certian times.

9.2 Typical Application

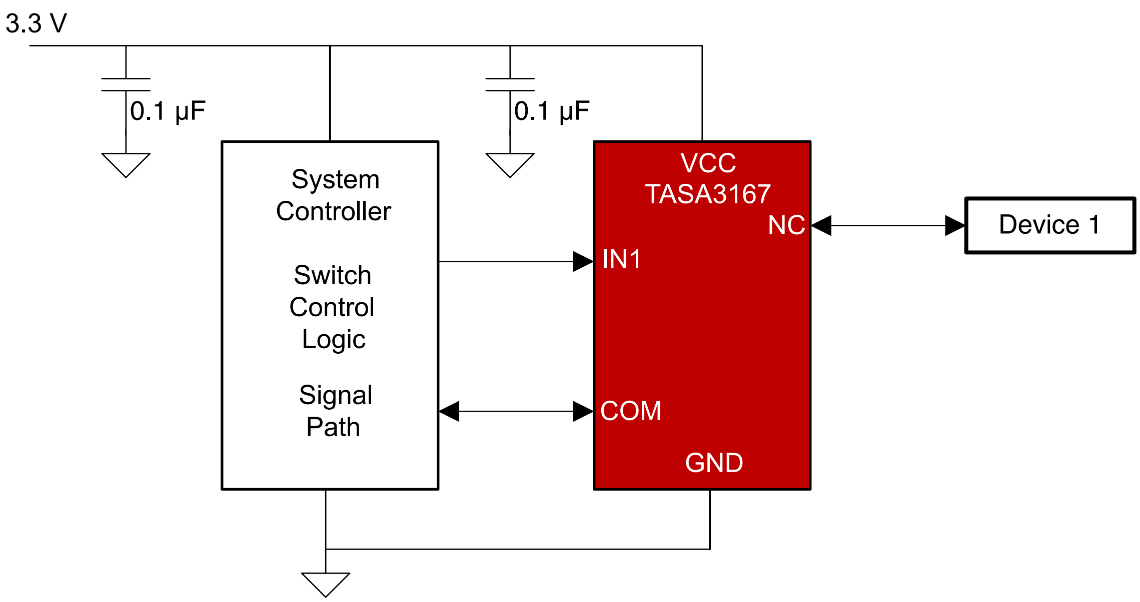


Figure 22. Typical Application

9.2.1 Design Requirements

The TS5A3167 device can be properly operated without any external components.

Unused pin may be left floating or connected to ground.

TI recommends pulling up the digital control pin (IN) to V_{CC} or pulling down to GND to avoid undesired switch positions that could result from the floating pin. A floating digital pin could cause excess current consumption refer to *Implications of Slow or Floating CMOS Inputs*.

9.2.2 Detailed Design Procedure

Select the appropriate supply voltage to cover the entire voltage swing of the signal passing through the switch because the TS5A3167 input and output signal swing through NC and COM are dependent on the supply voltage V_{CC}. For example, if the desired signal level to pass through the switch is 5 V, V_{CC} must be greater than or equal to 5 V. V_{CC} = 3.3 V would not be valid for passing a 5-V signal since the analog signal voltage cannot exceed the supply.

Typical Application (continued)

9.2.3 Application Curves

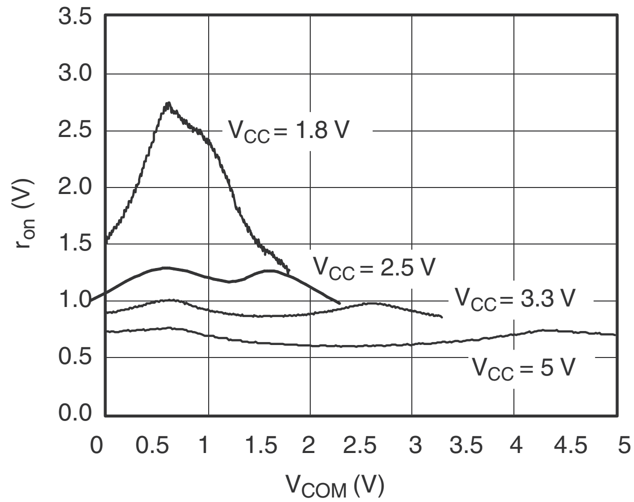


Figure 23. r_{on} vs V_{COM}

10 Power Supply Recommendations

TI recommends proper power-supply sequencing for all CMOS devices. Do not exceed the absolute maximum ratings, because stresses beyond the listed ratings can cause permanent damage to the device. It is recommended that V_{CC} is powered on first, followed by NC or COM but not required because of the Isolation in Powered-Off Mode, V_{CC} = 0 feature.

Although it is not required, power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{CC} supply to other components. A 0.1-µF capacitor, connected from V_{CC} to GND, is adequate for most applications.

11 Layout

11.1 Layout Guidelines

TI recommends following common printed-circuit board layout guidelines to ensure reliability of the device.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.

11.2 Layout Example

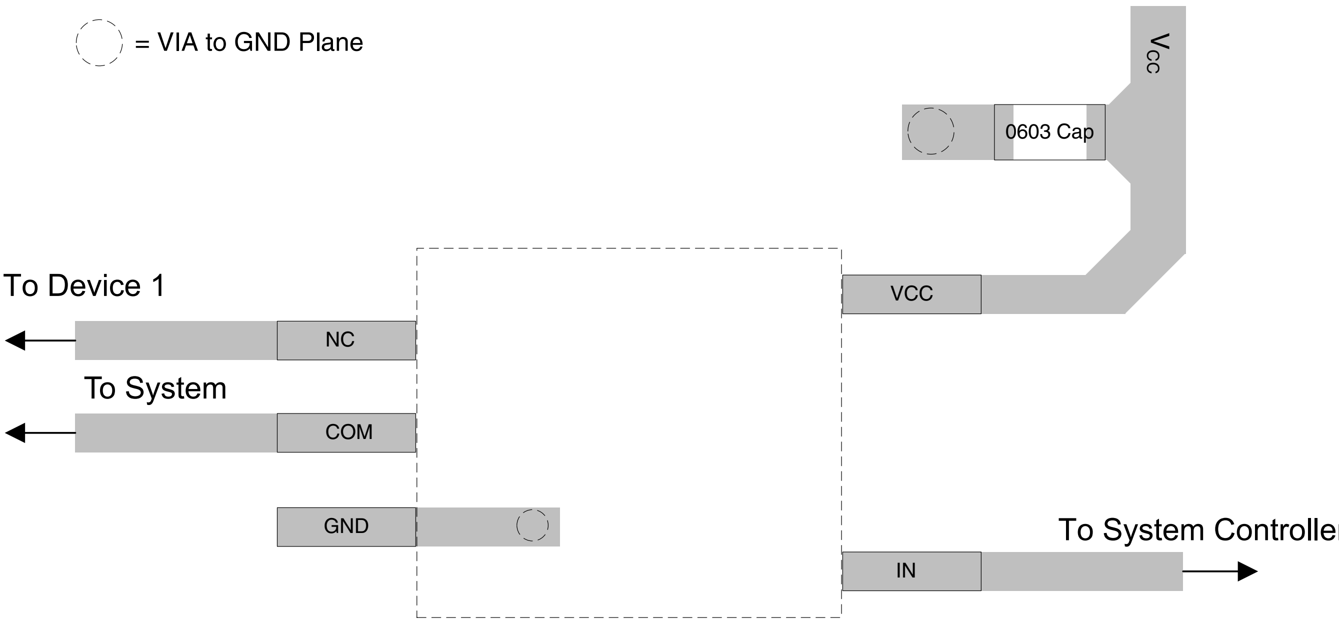


Figure 24. Example Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

表 2. パラメータの説明

記号	説明
V_{COM}	COM電圧。
V_{NC}	NC電圧。
r_{on}	チャネルがオンのときのCOMとNOポート間の抵抗
r_{peak}	規定電圧範囲内でのピーク・オン抵抗
$r_{on(flat)}$	規定の条件の範囲における、チャネルのr_{on}の最大値と最小値との差。
$I_{NC(OFF)}$	対応チャネル(NCからCOM)がオフ状態のとき、NCポートで測定されるリーク電流、ワーストケースの入力および出力条件
$I_{NC(PWROFF)}$	パワーダウン状況、V_{CC} = 0のとき、NCポートで測定されるリーク電流
$I_{COM(OFF)}$	ワーストケースの入力および出力条件で、対応チャネル(COMからNC)がオフ状態のとき、COMポートで測定されるリーク電流
$I_{COM(PWROFF)}$	パワーダウン状況、V_{CC} = 0のとき、COMポートで測定されるリーク電流
$I_{NC(ON)}$	対応チャネル(NCからCOM)がオン状態、出力(COM)がオープンのとき、NCポートで測定されるリーク電流
$I_{COM(ON)}$	対応チャネル(COMからNC)がオン状態、出力(NC)がオープンのとき、COMポートで測定されるリーク電流
V_{IH}	制御入力(IN)の論理HIGHの最小入力電圧。
V_{IL}	制御入力(IN)の論理LOWの最大入力電圧。
V_I	制御入力(IN)の電圧。
I_{IH}、I_{IL}	制御入力(IN)で測定されるリーク電流。
t_{ON}	スイッチのターンオン時間。このパラメータは、規定された条件の範囲で、スイッチがオンになるときのデジタル制御(IN)信号とアナログ出力(COM、NC)信号との間の伝搬遅延により測定されます。
t_{OFF}	スイッチのターンオフ時間。このパラメータは、規定された条件の範囲で、スイッチがオフになるときのデジタル制御(IN)信号とアナログ出力(COM、NC)信号との間の伝搬遅延により測定されます。
Q_C	電荷注入は、制御(IN)入力からアナログ(NC、COM)出力への、望ましくない信号のカップリングの測定値です。この値はクーロン(C)単位で、制御入力のスイッチングによって誘導される合計電荷により測定されます。電荷注入$Q_C = C_L \times \Delta V_{COM}$で、$C_L$は負荷容量、$\Delta V_{COM}$はアナログ出力電圧の変化です。
$C_{NC(OFF)}$	対応チャネル(NCからCOM)がオフのときのNCポートの容量。
$C_{COM(OFF)}$	対応チャネル(COMからNC)がオフのときのCOMポートの容量。
$C_{NC(ON)}$	対応チャネル(NCからCOM)がオンのときのNCポートの容量。
$C_{COM(ON)}$	対応チャネル(COMからNC)がオンのときのCOMポートの容量。
C_I	制御入力(IN)の容量。
O_{ISO}	スイッチのオフ絶縁は、オフ状態のスイッチのインピーダンス測定値です。これは、対応チャネル(NCからCOM)がオフ状態のとき、特定の周波数についてdB単位で測定されます。
BW	スイッチの帯域幅。オン状態のチャネルのゲインがDCゲインより-3dB低くなる周波数です。
THD	全高調波歪は、アナログ・スイッチにより発生する信号の歪みです。この値は、2次、3次、およびさらに高次の高調波の二乗平均(RMS)値と、基本波の絶対振幅との比として定義されます。
I_{CC}	制御(IN)ピンがV_{CC}またはGNDであるときの静的消費電流

12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.3 コミュニティ・リソース

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コミュニティ・リソース (continued)

し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.4 商標

E2E is a trademark of Texas Instruments.

12.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5A3167DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(JATF, JATR) (JATH, JATP)	Samples
TS5A3167DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(JG5, JGF, JGR) (JGH, JGP, JGS)	Samples
TS5A3167YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	JGN	Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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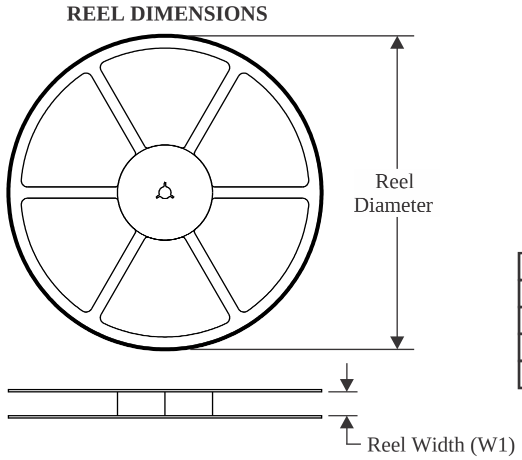
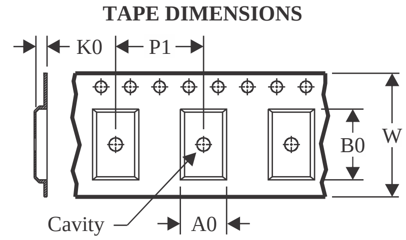
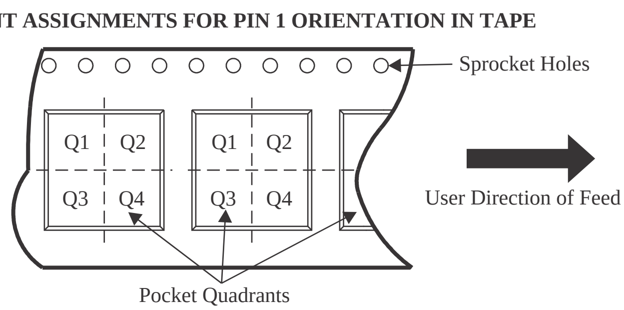
TAPE AND REEL INFORMATION





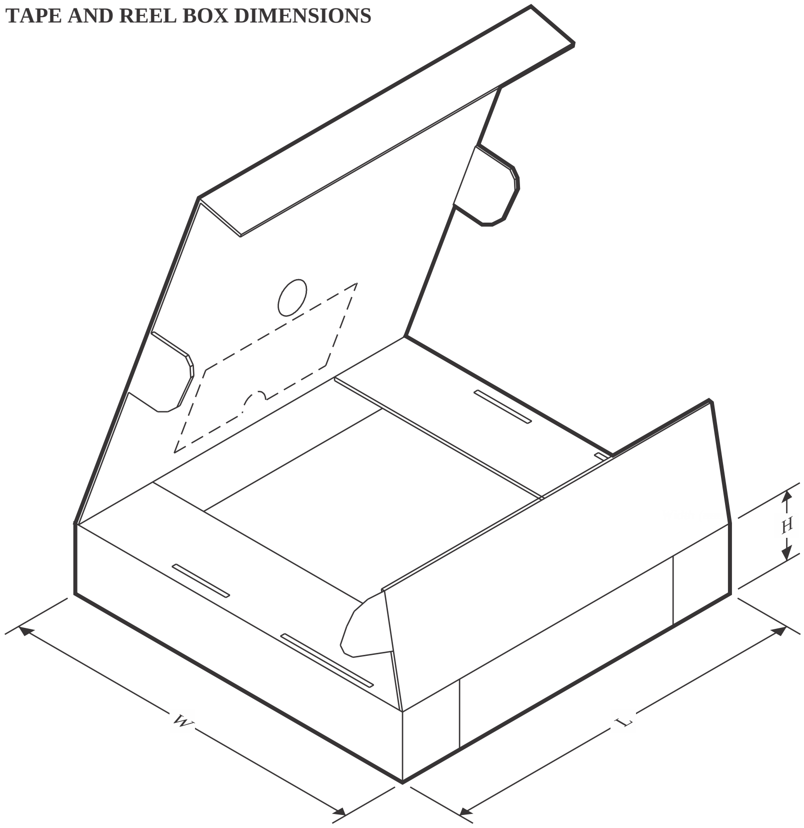
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

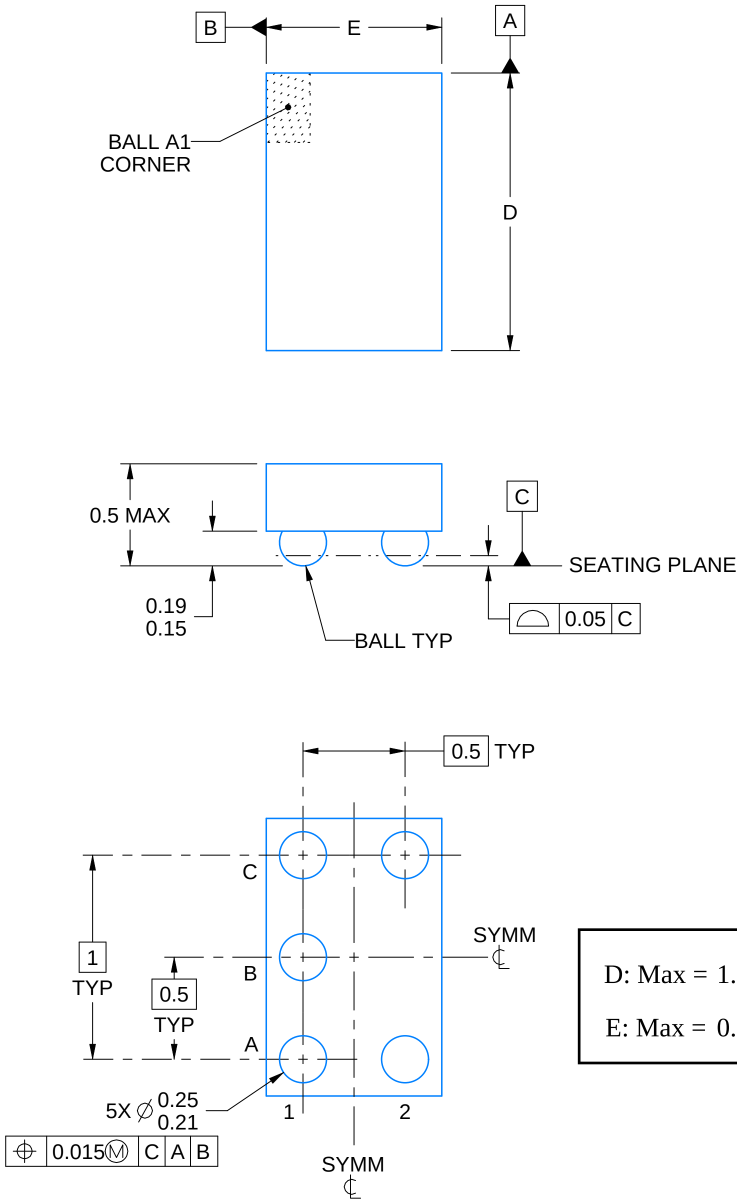
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5A3167DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TS5A3167DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TS5A3167YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5A3167DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TS5A3167DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
TS5A3167YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0



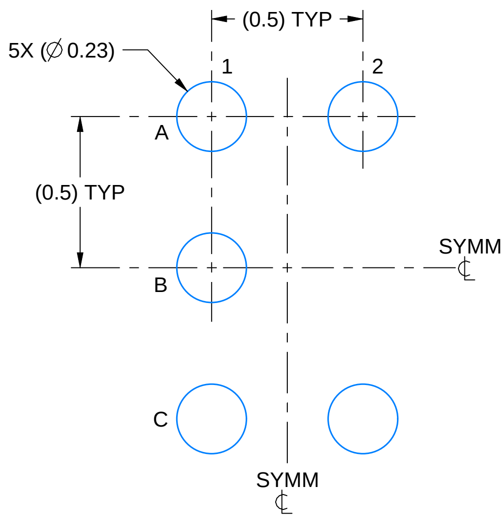
D: Max = 1.418 mm, Min =1.358 mm

E: Max = 0.918 mm, Min =0.858 mm

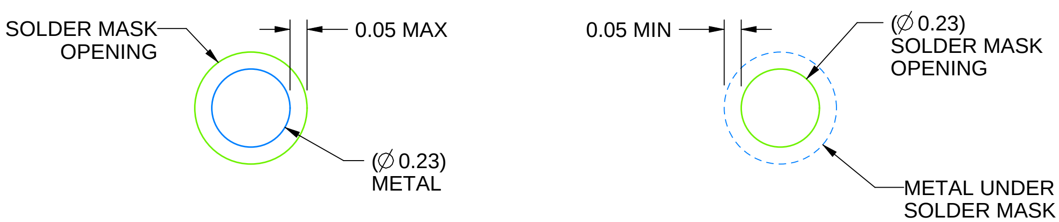
4219492/A 05/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



NON-SOLDER MASK DEFINED (PREFERRED)

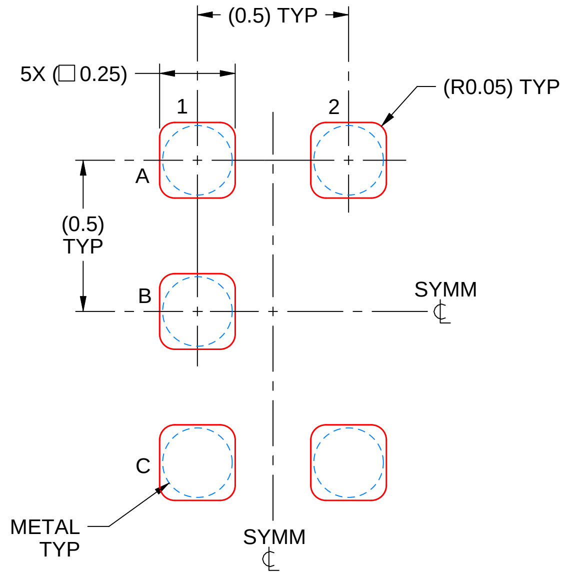
SOLDER MASK DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

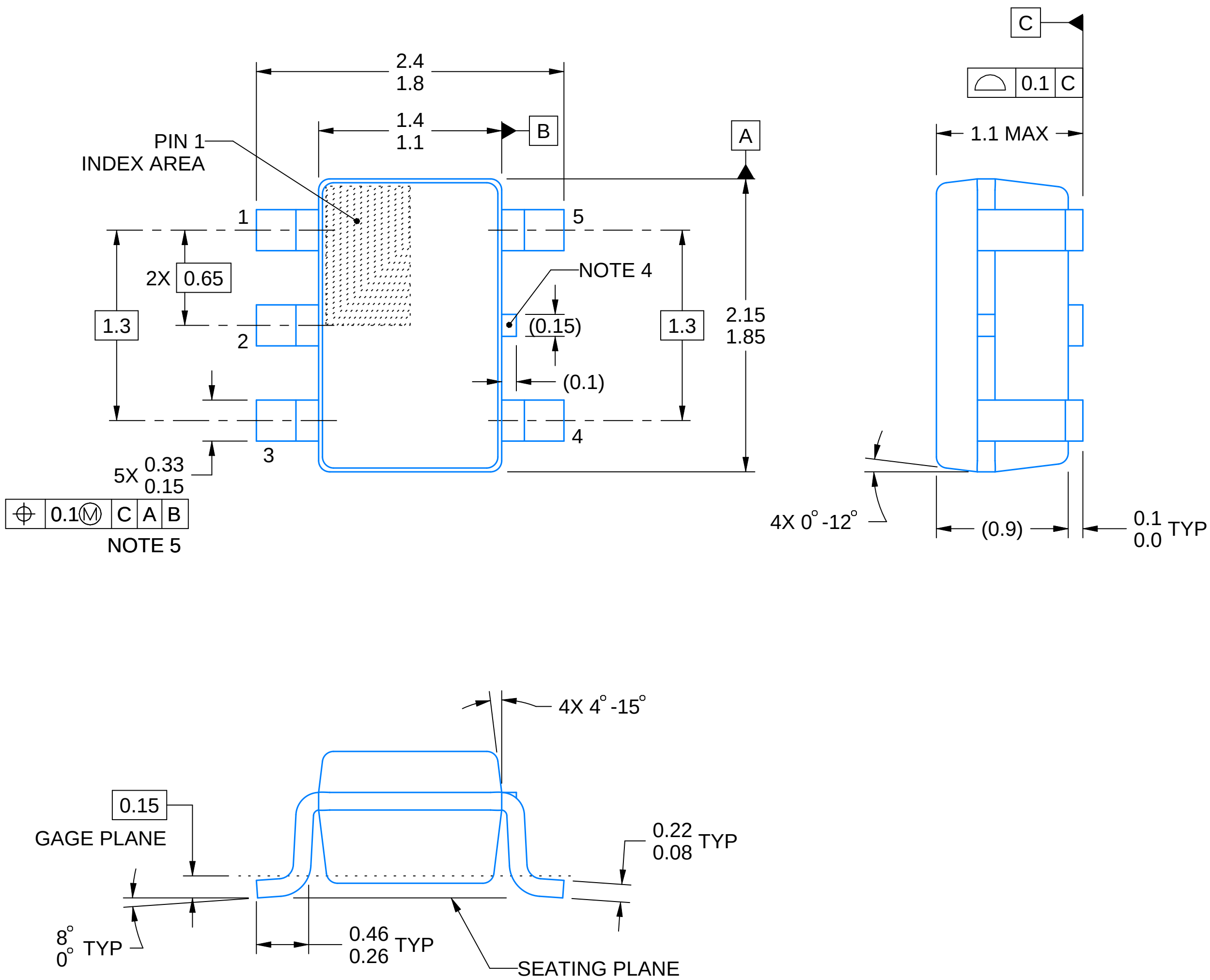


SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

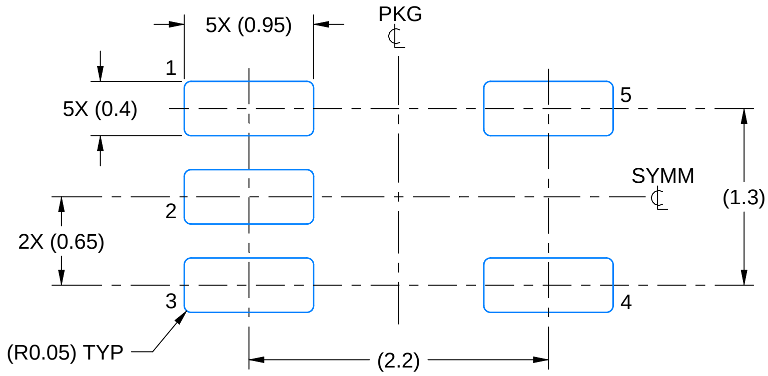
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



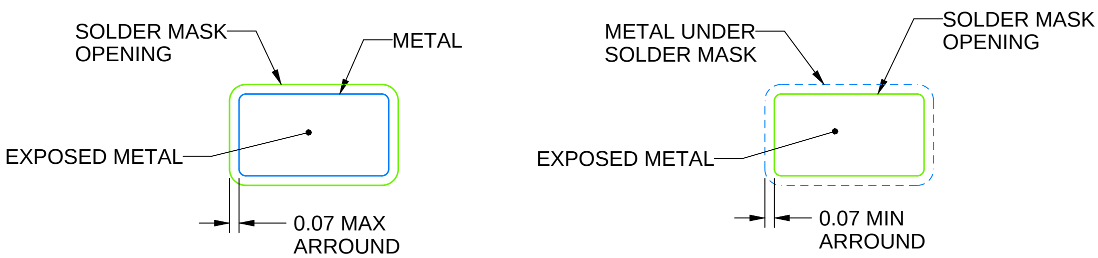
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK DEFINED (PREFERRED)

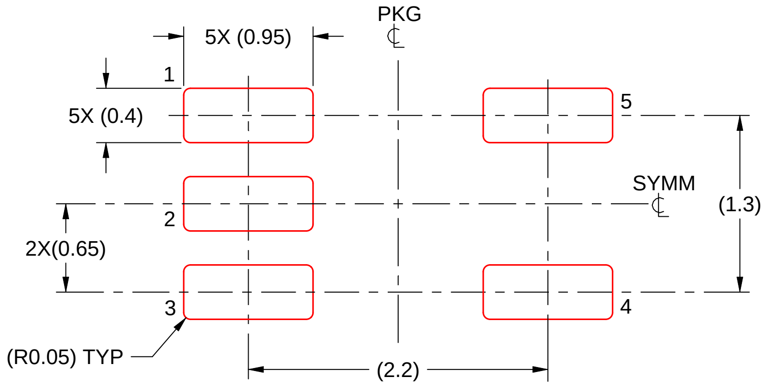
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

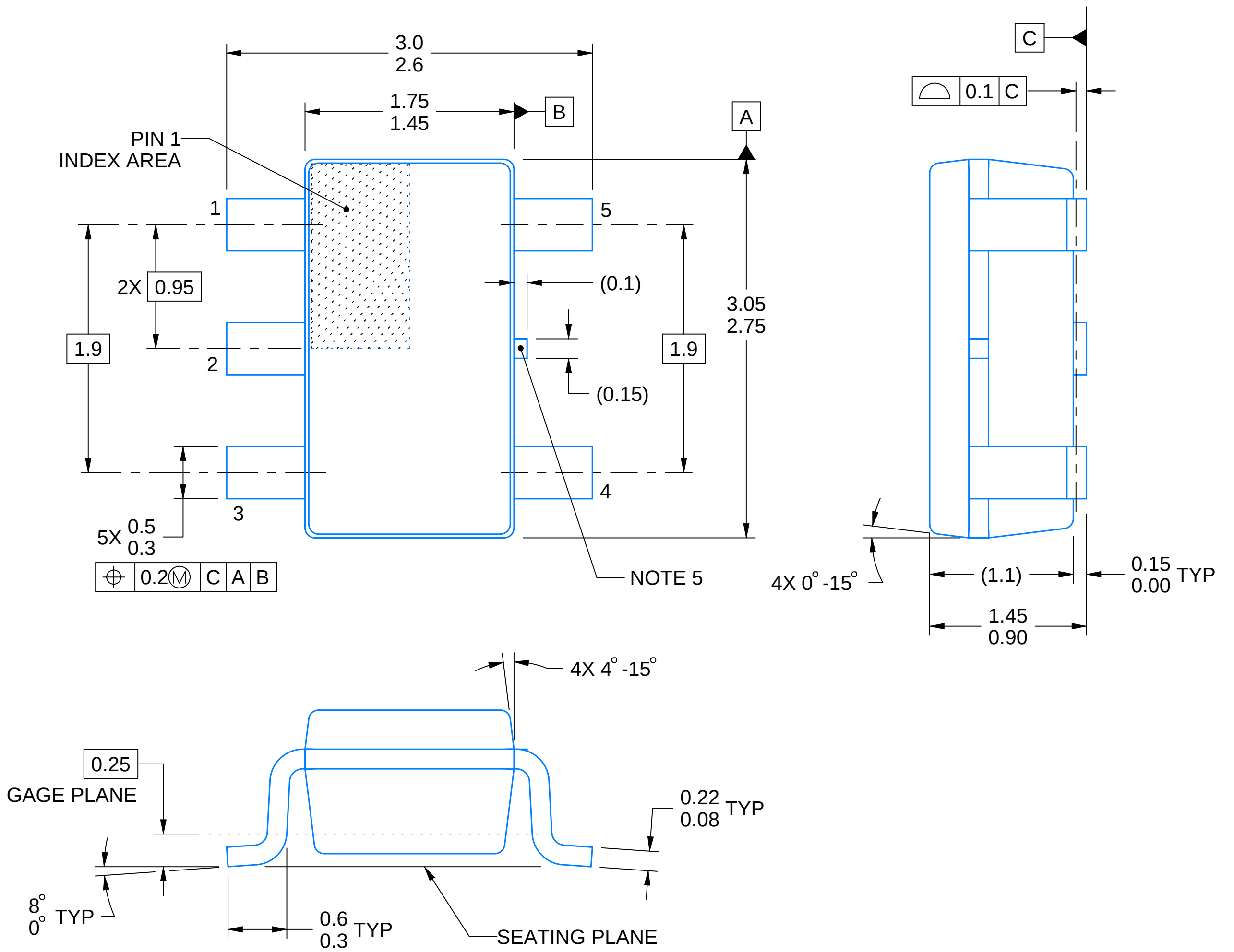
NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

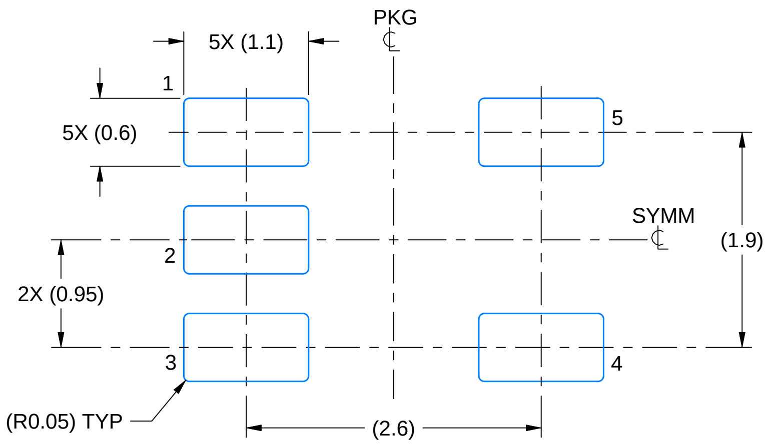
SMALL OUTLINE TRANSISTOR



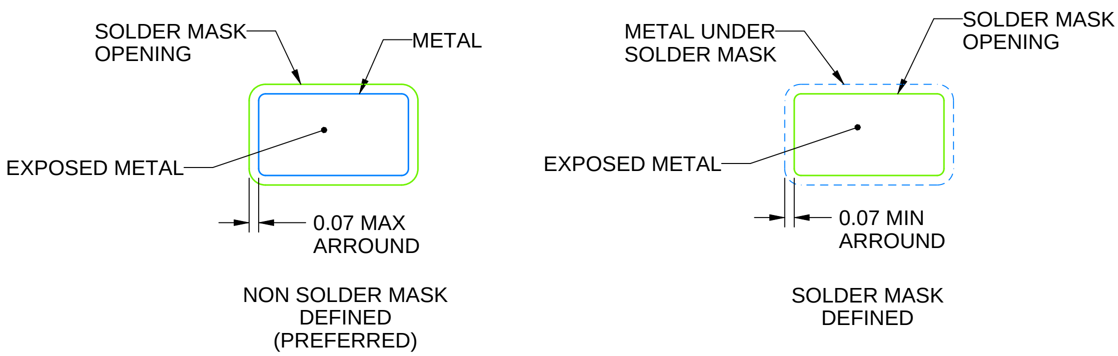
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

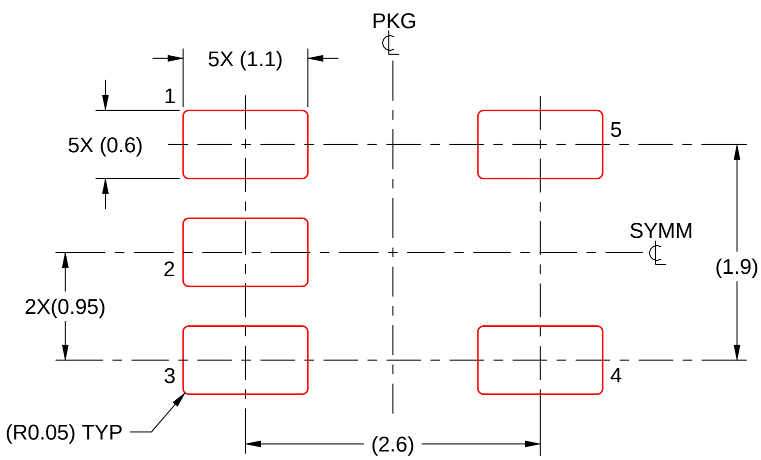


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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