参考資料

TS3A5017-Q1
JAJSGF3 – OCTOBER 2018

TS3A5017-Q1 2チャネル、4:1の車載アプリケーション用アナログ・スイッチ

1 特長

- 車載アプリケーション用にAEC-Q100認定済み
  - デバイス温度: T_A -40°C～125°C
  - デバイスHBM分類レベル: ±1500V
  - デバイスCDM分類レベル: ±1000V
- 電源オフ保護に対応：V_{CC} = 0V時、I/OピンはHi-Z
- 低いオン抵抗
- 低い電荷注入
- 1Ωのオン抵抗マッチング
- 全高調波歪(THD+N): 0.25%
- 2.3V～3.6Vの単電源で動作
- JESD 78, Class II準拠で100mA超のラッチアップ性能

2 アプリケーション

- サンプル・アンド・ホールド回路
- インフォテインメントのオーディオおよびビデオ信号のルーティング
- テレマティクス制御ユニット

3 概要

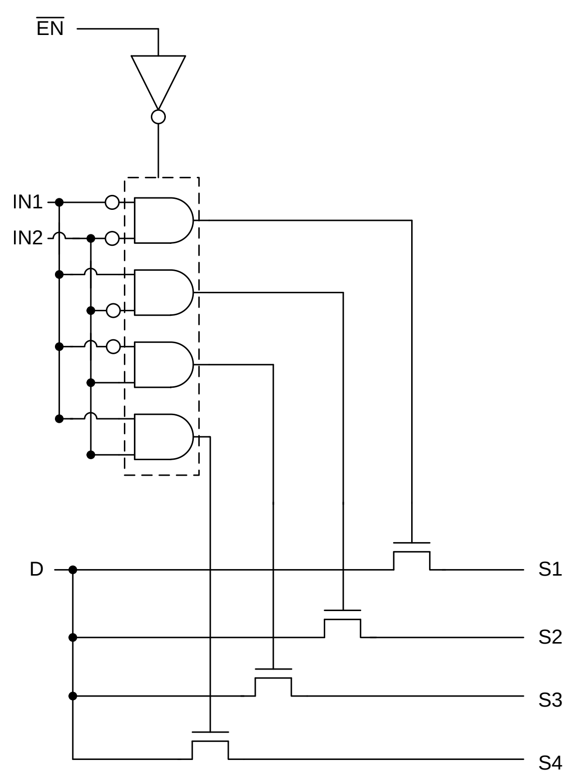
TS3A5017-Q1デバイスは2チャネル、4:1のマルチプレクサで、2.3V～3.6Vで動作するよう設計されています。このデバイスは双方向で、デジタルとアナログ両方の信号を処理できます。このデバイスの電源オフ保護機能により、V_{CC} = 0Vのときは信号パスが高インピーダンスになることが保証され、電源シーケンシングが簡単になり、システムの信頼性が向上します。

製品情報[(1)]

型番	パッケージ	本体サイズ(公称)
TS3A5017-Q1	VQFN (16)	4.00mm×3.50mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



English Data Sheet: SCDS387

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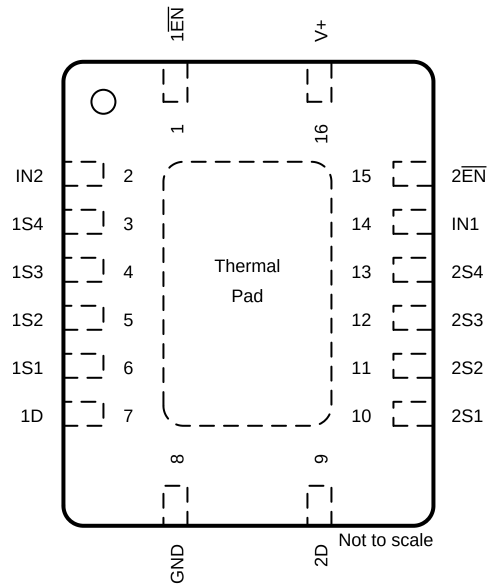
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

日付	リビジョン	注
2018年10月	*	初版

5 Pin Configuration and Functions

**RGY Package
16-Pin VQFN
(Top View)**



If exposed thermal pad is used, it must be connected as a secondary ground or left electrically open.

Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
7	1D	I/O	Common path for switch 1
1	$1\overline{EN}$	I	Active-low enable for switch 1
6	1S1	I/O	Switch 1 channel 1
5	1S2	I/O	Switch 1 channel 2
4	1S3	I/O	Switch 1 channel 3
3	1S4	I/O	Switch 1 channel 4
9	2D	I/O	Common path for switch 2
15	$2\overline{EN}$	I	Active-low enable for switch 2
10	2S1	I/O	Switch 2 channel 1
11	2S2	I/O	Switch 2 channel 2
12	2S3	I/O	Switch 2 channel 3
13	2S4	I/O	Switch 2 channel 4
8	GND	–	Ground
14	IN1	I	Switch 1 input select
2	IN2	I	Switch 2 input select
16	V+	–	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
V_+	Supply voltage(3)		–0.5	4.6	V
V_S, V_D	Analog voltage(3) (4)		–0.5	4.6	V
I_{SK}, I_{DK}	Analog port clamp current	V_S, V_D < 0	–50		mA
I_S, I_D	ON-state switch current	V_S, V_D = 0 to 7 V	–128	128	mA
V_I	Digital input voltage		–0.5	4.6	V
I_{IK}	Digital input clamp current(3) (4)	V_I < 0	–50		mA
I_+	Continuous current through V_+			100	mA
I_{GND}	Continuous current through GND		–100		mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under*Absolute Maximum Ratings* may cause permanent damage to thedevice. These are stress ratings only, and functional operation of the device at these or any otherconditions beyond those indicated under *Recommended OperatingConditions* is not implied. Exposure to absolute-maximum-rated conditions for extendedperiods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is aminimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwisespecified.
(4) The input and output voltage ratings may be exceeded if theinput and output clamp-current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{I/O}$	Switch input/output voltage range	0	3.6	V
V+	Supply voltage range	2.3	3.6	V
V_I	Control input voltage range	0	3.6	V
T_A	Operating Temperature Range	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TS3A5017-Q1 RGY (VQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	58.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.0	°C/W

(1) For more information about traditional and new thermalmetrics, see the *IC Package ThermalMetrics* application report .

6.5 Electrical Characteristics for 3.3-VSupply

V_+ = 2.7 V to 3.6 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Analog Switch								
V_D, V_S	Analog signal range				0		V_+	V
r_{on}	ON-state resistance	0 ≤ V_S ≤ V_+, I_D = –32 mA,	Switch ON, see 図 12	T_A = 25°C V_+ = 3 V		11		Ω
				T_A = Full V_+ = 3 V			16	
Δr_{on}	ON-state resistance match between channels	V_S = 2.1 V, I_D = –32 mA,	Switch ON, see 図 12	T_A = 25°C V_+ = 3 V		1		Ω
				T_A = Full V_+ = 3 V			5	
$r_{on(flat)}$	ON-state resistance flatness	0 ≤ V_S ≤ V_+, I_D = –32 mA,	Switch ON, see 図 12	T_A = 25°C V_+ = 3 V		7		Ω
				T_A = Full V_+ = 3 V			12	
$I_{S(OFF)}$	S OFF leakage current	V_S = 1 V, V_D = 3 V, or V_S = 3 V, V_D = 1 V,	Switch OFF, see 図 13	T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–0.3		0.3	
$I_{SPWR(OFF)}$		V_S = 0 to 3.6 V, V_D = 3.6 V to 0,		T_A = 25°C V_+ = 0 V		0.5		
				T_A = Full V_+ = 0 V	–10		10	
$I_{D(OFF)}$	D OFF leakage current	V_S = 1 V, V_D = 3 V, or V_S = 3 V, V_D = 1 V,	Switch OFF, see 図 13	T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–0.3		0.3	
$I_{DPWR(OFF)}$		V_D = 0 to 3.6 V, V_S = 3.6 V to 0,		T_A = 25°C V_+ = 0 V		0.5		
				T_A = Full V_+ = 0 V	–20		20	
$I_{S(ON)}$	S ON leakage current	V_S = 1 V, V_D = Open, or V_S = 3 V, V_D = Open,	Switch ON, see 図 14	T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–0.3		0.3	
$I_{D(ON)}$	D ON leakage current	V_D = 1 V, V_S = Open, or V_D = 3 V, V_S = Open,	Switch ON, see 図 14	T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–0.3		0.3	
Digital Control Inputs (IN1, IN2, $\overline{EN}$)(2)								
V_{IH}	Input logic high			T_A = Full	2		V_+	V
V_{IL}	Input logic low			T_A = Full	0		0.8	V
I_{IH}, I_{IL}	Input leakage current	V_I = V_+ or 0		T_A = 25°C V_+ = 3.6 V		0.05		µA
				T_A = Full V_+ = 3.6 V	–1		1	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 0.1 nF,	See 図 21	T_A = 25°C V_+ = 3.3 V		5		pC
$C_{S(OFF)}$	S OFF capacitance	V_S = V_+ or GND, Switch OFF,	See 図 15	T_A = 25°C V_+ = 3.3 V		4.5		pF
$C_{D(OFF)}$	D OFF capacitance	V_D = V_+ or GND, Switch OFF,	See 図 15	T_A = 25°C V_+ = 3.3 V		19		pF
$C_{S(ON)}$	S ON capacitance	V_S = V_+ or GND, Switch ON,	See 図 15	T_A = 25°C V_+ = 3.3 V		27		pF

(1) The algebraic convention, whereby the most negative value is aminimum and the most positive value is a maximum
(2) All unused digital inputs of the device must be held atV_+ or GND to ensure proper device operation. Refer to the TI applicationreport, *Implications of Slow or Floating CMOS Inputs*, literaturenumber SCBA004.

Electrical Characteristics for 3.3-VSupply (continued)

V_+ = 2.7 V to 3.6 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$C_{D(ON)}$	D ON capacitance	V_D = V_+ or GND, Switch ON,	See 図 15	T_A = 25°C V_+ = 3.3 V		27		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 図 15	T_A = 25°C V_+ = 3.3 V		3		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 図 17	T_A = 25°C V_+ = 3.3 V		165		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	See 図 18	T_A = 25°C V_+ = 3.3 V		–69		dB
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	See 図 18	T_A = 25°C V_+ = 3.3 V		–49		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See 図 19	T_A = 25°C V_+ = 3.3 V		–69		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	R_L = 50 Ω, f = 1 MHz,	See 図 20	T_A = 25°C V_+ = 3.3 V		–80		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 図 22	T_A = 25°C V_+ = 3.3 V		0.25		%
Supply								
I_+	Positive supply current	V_I = V_+ or GND,	Switch ON or OFF	T_A = 25°C V_+ = 3.6 V		2.5	7	µA
				T_A = Full V_+ = 3.6 V			10	

6.6 Electrical Characteristics for 2.5-VSupply

V_+ = 2.3 V to 2.7 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Analog Switch								
V_D, V_S	Analog signal range				0		V_+	V
r_{on}	ON-state resistance	$0 \le V_S \le V_+$, I_D = –24 mA,	Switch ON, see 図 12	T_A = 25°C V_+ = 2.3 V		22		Ω
				T_A = Full V_+ = 2.3 V			28	
Δr_{on}	ON-state resistance match between channels	V_S = 1.6 V, I_D = –24 mA,	Switch ON, see 図 12	T_A = 25°C V_+ = 2.3 V		1		Ω
				T_A = Full V_+ = 2.3 V			5	
$r_{on(flat)}$	ON-state resistance flatness	$0 \le V_S \le V_+$, I_D = –24 mA,	Switch ON, see 図 12	T_A = 25°C V_+ = 2.3 V		18		Ω
				T_A = Full V_+ = 2.3 V			24	
$I_{S(OFF)}$	S OFF leakage current	V_S = 0.5 V, V_D = 2.2 V, or V_S = 2.2 V, V_D = 0.5 V,	Switch OFF, see 図 13	T_A = 25°C V_+ = 2.7 V		0.05		µA
				T_A = Full V_+ = 2.7 V	–0.3		0.3	
$I_{SPWR(OFF)}$		V_S = 0 to 2.7 V, V_D = 2.7 V to 0,		T_A = 25°C V_+ = 0 V		0.5		
				T_A = Full V_+ = 0 V	-15		15	

(1) The algebraic convention, whereby the most negative value is aminimum and the most positive value is a maximum

Electrical Characteristics for 2.5-VSupply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$I_{D(OFF)}$	D OFF leakage current	V_S = 0.5 V, V_D = 2.2 V, or V_S = 2.2 V, V_D = 0.5V,	Switch OFF, see 図 13	T_A = 25°C V_+ = 2.7 V		0.05		µA
				T_A = Full V_+ = 2.7 V	–0.3		0.3	
$I_{DPWR(OFF)}$		V_D = 0 to 2.7 V, V_S = 2.7 V to 0,		T_A = 25°C V_+ = 0 V		0.5		
				T_A = Full V_+ = 0 V	-20		20	
$I_{S(ON)}$	S ON leakage current	V_S = 0.5 V, V_D = Open, or V_S = 2.2 V, V_D = Open,	Switch ON, see 図 14	T_A = 25°C V_+ = 2.7 V		0.05		µA
				T_A = Full V_+ = 2.7 V	–0.3		0.3	
$I_{D(ON)}$	D ON leakage current	V_D = 0.5 V, V_S = Open, or V_D = 2.2 V, V_S = Open,	Switch ON, see 図 14	T_A = 25°C V_+ = 2.7 V		0.05		µA
				T_A = Full V_+ = 2.7 V	–0.3		0.3	
Logic Inputs (IN1, IN2, $\overline{EN}$)(2)								
V_{IH}	Input logic high			T_A = Full	1.7		V_+	V
V_{IL}	Input logic low			T_A = Full	0		0.7	V
I_{IH}, I_{IL}	Input leakage current	V_I = V_+ or 0		T_A = 25°C V_+ = 2.7 V		0.05		µA
				T_A = Full V_+ = 2.7 V	–1		1	
Q_C	Charge injection	V_{GEN} = 0, R_{GEN} = 0, C_L = 0.1 nF,	See 図 21	T_A = Full V_+ = 2.5 V		3		pC
$C_{S(OFF)}$	S OFF capacitance	V_S = V_+ or GND, Switch OFF,	See 図 15	T_A = Full V_+ = 2.5 V		4.5		pF
$C_{D(OFF)}$	D OFF capacitance	V_D = V_+ or GND, Switch OFF,	See 図 15	T_A = Full V_+ = 2.5 V		18.5		pF
$C_{S(ON)}$	S ON capacitance	V_S = V_+ or GND, Switch ON,	See 図 15	T_A = Full V_+ = 2.5 V		26		pF
$C_{D(ON)}$	D ON capacitance	V_D = V_+ or GND, Switch ON,	See 図 15	T_A = Full V_+ = 2.5 V		26		pF
C_I	Digital input capacitance	V_I = V_+ or GND,	See 図 15	T_A = Full V_+ = 2.5 V		3		pF
BW	Bandwidth	R_L = 50 Ω, Switch ON,	See 図 17	T_A = Full V_+ = 2.5 V		165		MHz
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 1 MHz,	See 図 18	T_A = Full V_+ = 2.5 V		–69		dB
O_{ISO}	OFF isolation	R_L = 50 Ω, f = 10 MHz,	See 図 18	T_A = Full V_+ = 2.5 V		–49		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, f = 1 MHz,	See 図 19	T_A = Full V_+ = 2.5 V		–69		dB
$X_{TALK(ADJ)}$	Crosstalk adjacent	R_L = 50 Ω, f = 1 MHz,	See 図 20	T_A = Full V_+ = 2.5 V		–85		dB
THD	Total harmonic distortion	R_L = 600 Ω, C_L = 50 pF,	f = 20 Hz to 20 kHz, see 図 22	T_A = Full V_+ = 2.5 V		0.3		%
Supply								

(2) All unused digital inputs of the device must be held atV_+ or GND to ensure proper device operation. Refer to the TI applicationreport, *Implications of Slow or Floating CMOS Inputs*, literaturenumber SCBA004.

Electrical Characteristics for 2.5-VSupply (continued)

V_+ = 2.3 V to 2.7 V, T_A = –40°C to125°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_+	Positive supply current	$V_I = V_+$ or GND,	Switch ON or OFF	T_A = Full V_+ = 2.7 V		2.5	7	µA
				T_A = Full V_+ = 2.7 V			10	

6.7 Switching Characteristics for 3.3-VSupply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turnon time(1)	V_D = 2 V, R_L = 300 Ω,	C_L = 35 pF, see 図 16	T_A = 25°C V_+ = 3.3 V		5	9.5	ns
				T_A = Full V_+ = 3 V to 3.6 V			10.5	
t_{OFF}	Turnoff time(1)	V_D = 2 V, R_L = 300 Ω,	C_L = 35 pF, see 図 16	T_A = 25°C V_+ = 3.3 V		1.5	3.5	ns
				T_A = Full V_+ = 3 V to 3.6 V			4.5	

(1) Specified by design, not tested in production

6.8 Switching Characteristics for 2.5-VSupply

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{ON}	Turnon time(1)	V_{COM} = 2 V, R_L = 300 Ω,	C_L = 35 pF, see 図 16	T_A = 25°C V_+ = 2.5 V		5	8	ns
				T_A = Full V_+ = 2.3 V to 2.7 V			10	
t_{OFF}	Turnoff time(1)	V_{COM} =2 V, R_L = 300 Ω,	C_L = 35 pF, see 図 16	T_A = 25°C V_+ = 2.5 V		2	4.5	ns
				T_A = Full V_+ = 2.3 V to 2.7 V			6	

(1) Specified by design, not tested in production.

6.9 Typical Characteristics

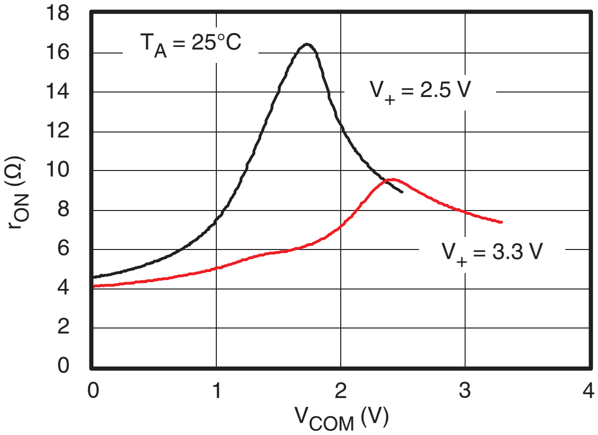


図 1. r_{on} vs V_{COM}

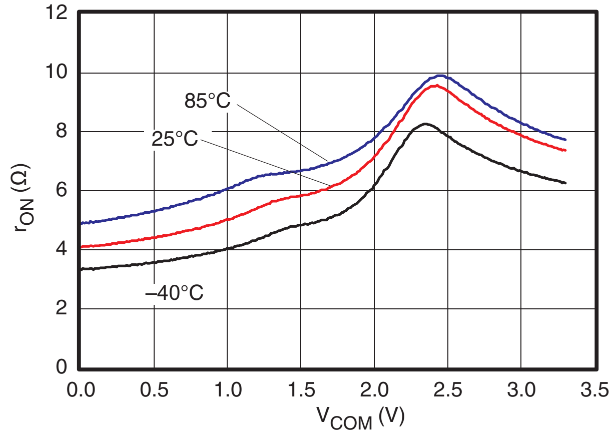


図 2. r_{on} vs V_{COM} (V_+ = 3.3 V)

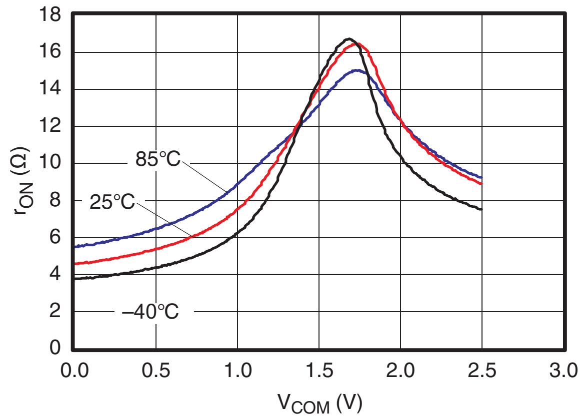


図 3. r_{on} vs V_{COM} (V_+ = 2.5 V)

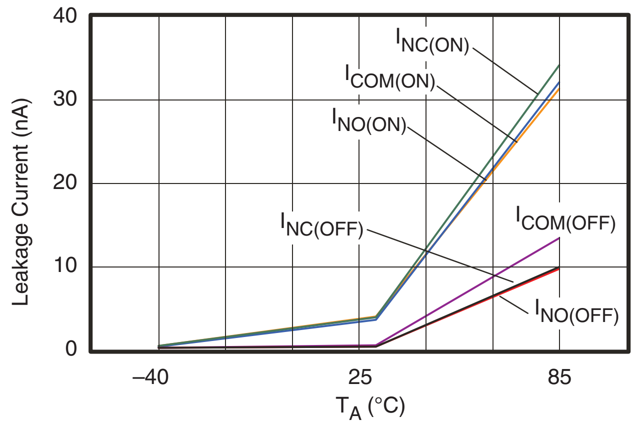


図 4. Leakage Current vs Temperature (V_+ = 3.6 V)

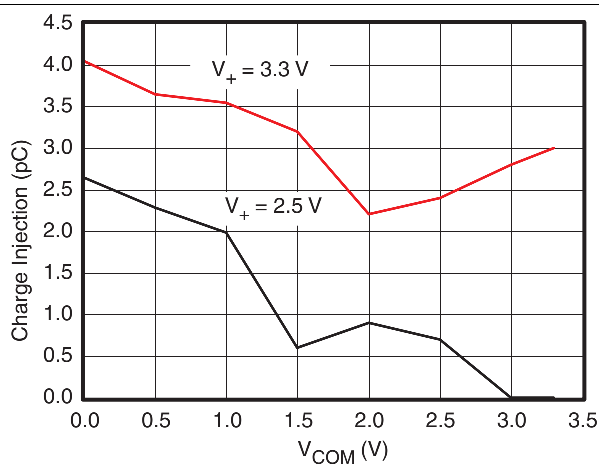


図 5. Charge Injection (Q_C) vs V_{COM}

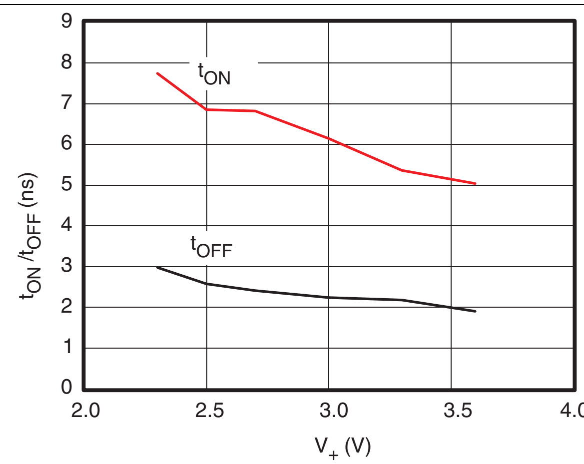


図 6. t_{ON} and t_{OFF} vs Supply Voltage

Typical Characteristics (continued)

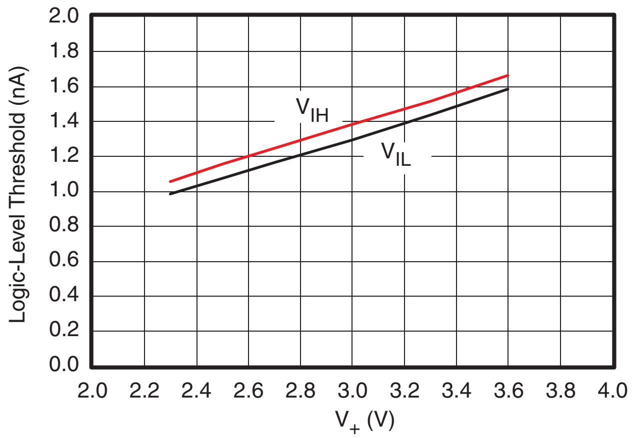


図 7. Logic-Level Threshold vs V_+

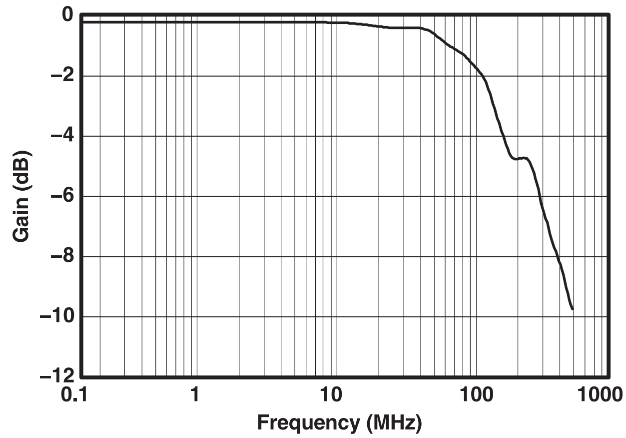


図 8. Bandwidth (Gain vs Frequency) (V_+ = 3.3 V)

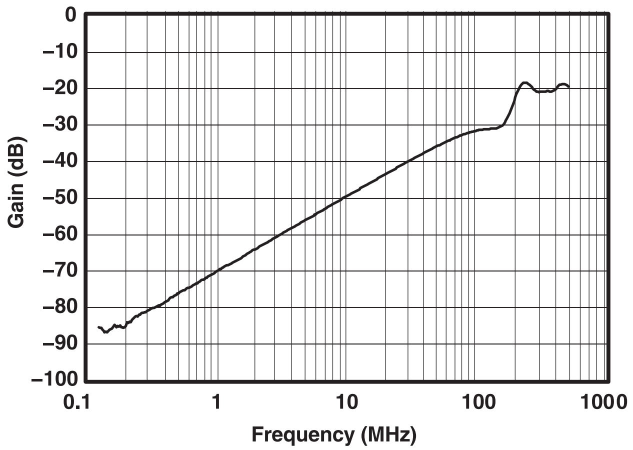


図 9. OFF Isolation and Crosstalk vs Frequency (V_+ = 3.3 V)

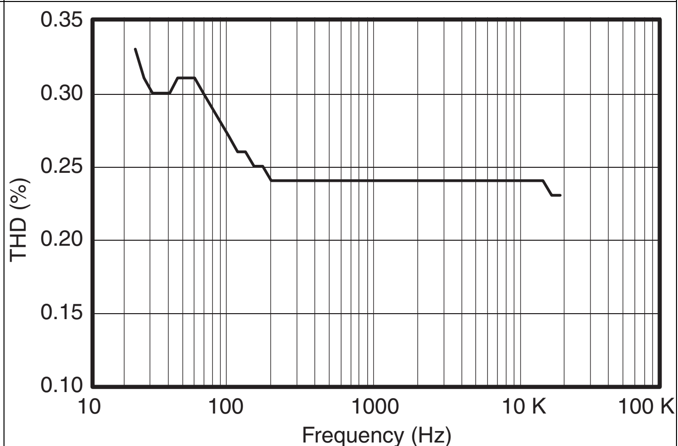


図 10. Total Harmonic Distortion vs Frequency

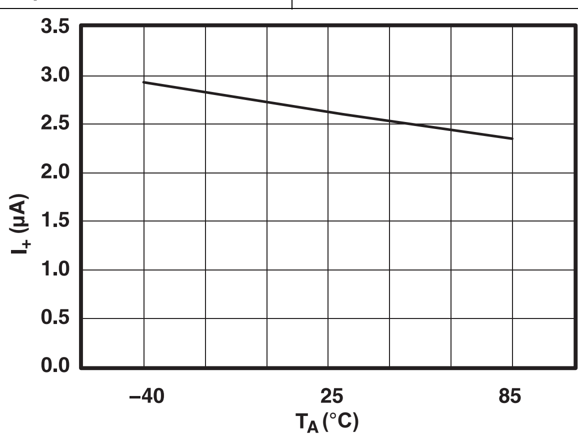
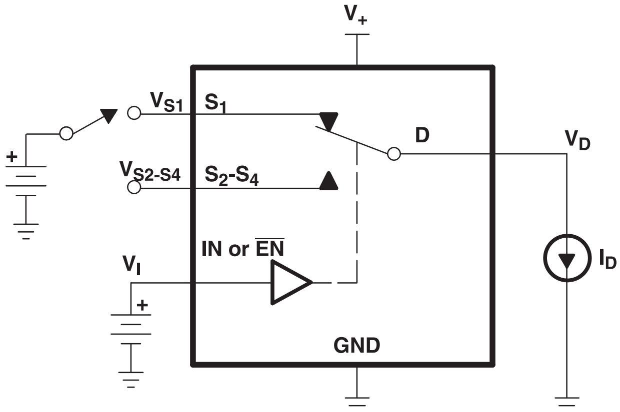


図 11. Power-Supply Current vs Temperature (V_+ = 3.6 V)

7 Parameter Measurement Information

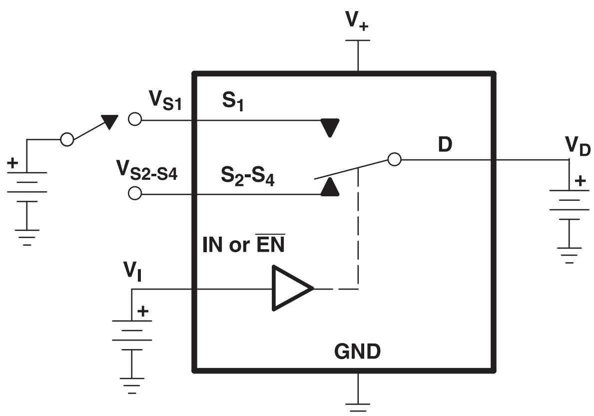


Channel ON

$r_{on} = \frac{V_D - V_{S2\text{-}S4} \text{ or } V_{s1}}{I_D}\ \Omega$

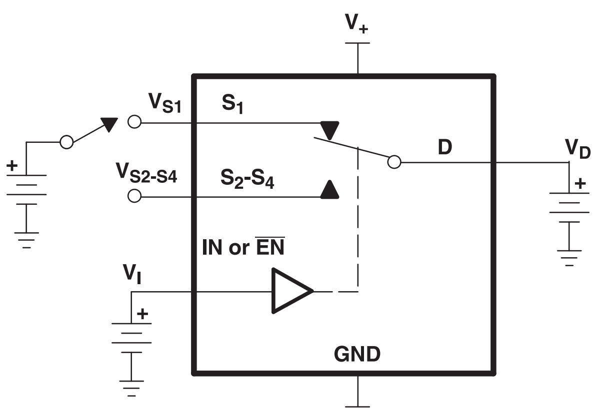
$V_I = V_{IH}$ or V_{IL}

図 12. ON-State Resistance (r_{on})



OFF-State Leakage Current
Channel OFF
$V_I = V_{IH}$ or V_{IL}
V_{S1} or $V_{S2\text{-}S4}$ = 0 to V_+
and
$V_D = V_+$ to 0

図 13. OFF-State Leakage Current ($I_{D(OFF)}$, $I_{S(OFF)}$)



ON-State Leakage Current
Channel ON
$V_I = V_{IH}$ or V_{IL}

図 14. ON-State Leakage Current ($I_{D(ON)}$, $I_{S(ON)}$)

Parameter Measurement Information (continued)

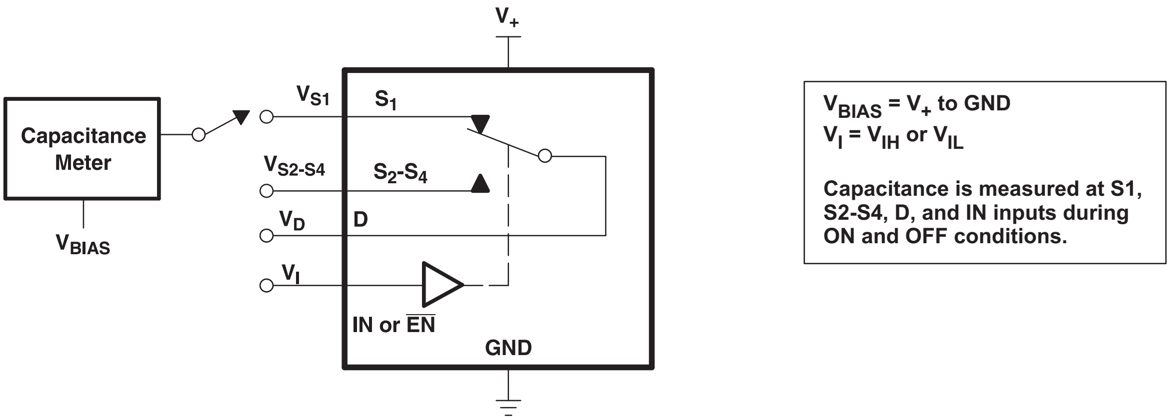
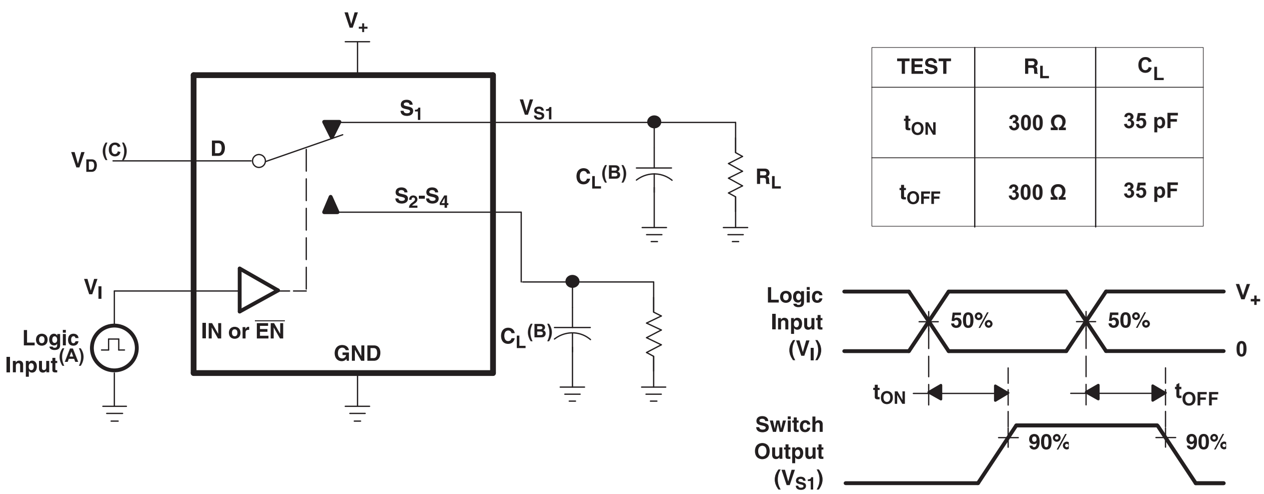


図 15. Capacitance (C_I, $C_{D(OFF)}$, $C_{D(ON)}$, $C_{S(OFF)}$, $C_{S(ON)}$)



TEST	R_L	C_L
t_{ON}	300 Ω	35 pF
t_{OFF}	300 Ω	35 pF

A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

C. See Electrical Characteristics for V_D.

図 16. Turnon (t_{ON}) and Turnoff Time (t_{OFF})

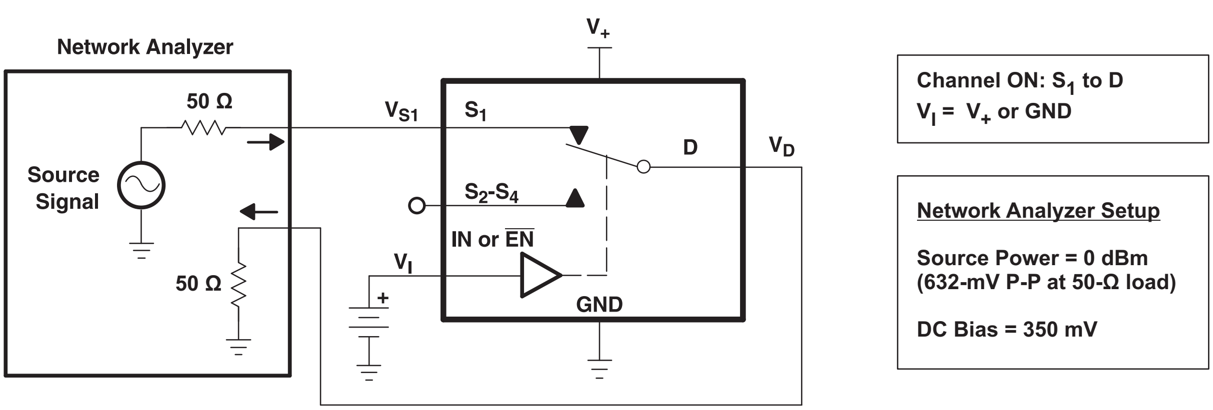


図 17. Bandwidth (BW)

Parameter Measurement Information (continued)

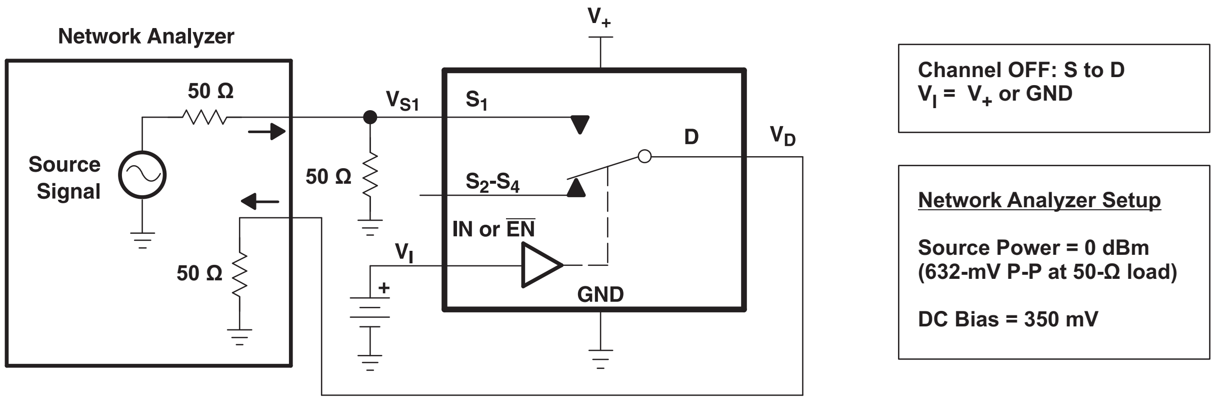


図 18. OFF Isolation (O_{ISO})

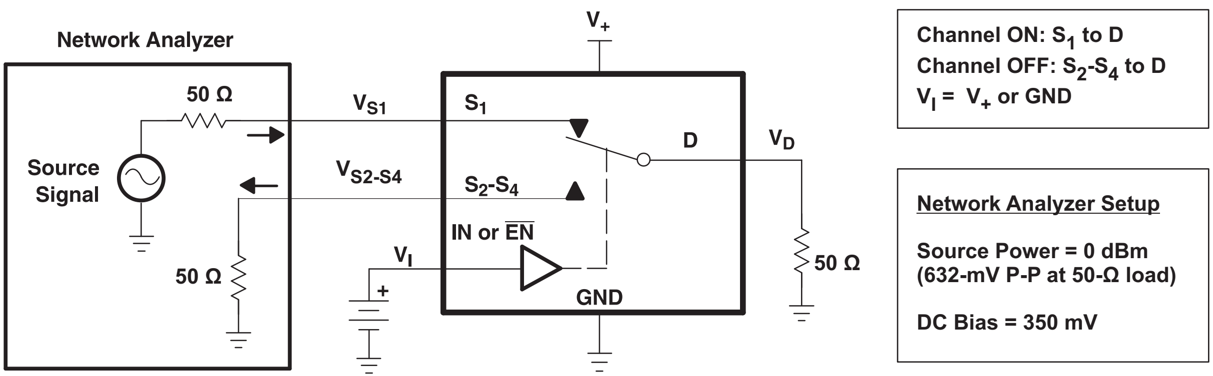


図 19. Crosstalk (X_{TALK})

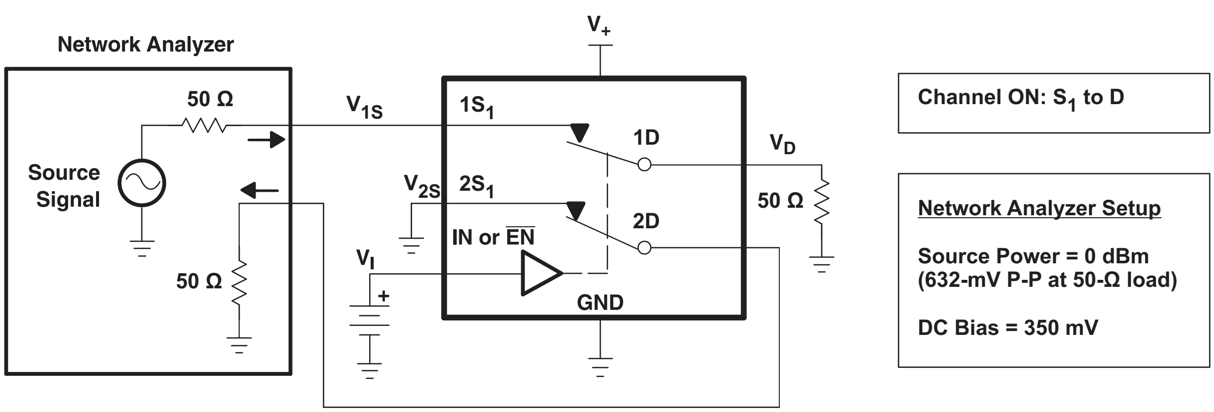
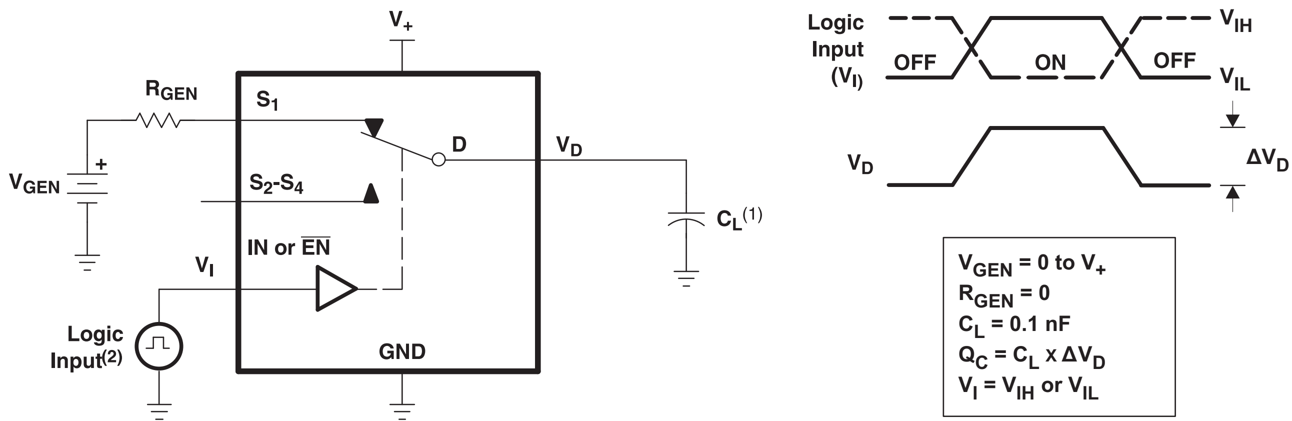


図 20. Adjacent Crosstalk (X_{TALK})

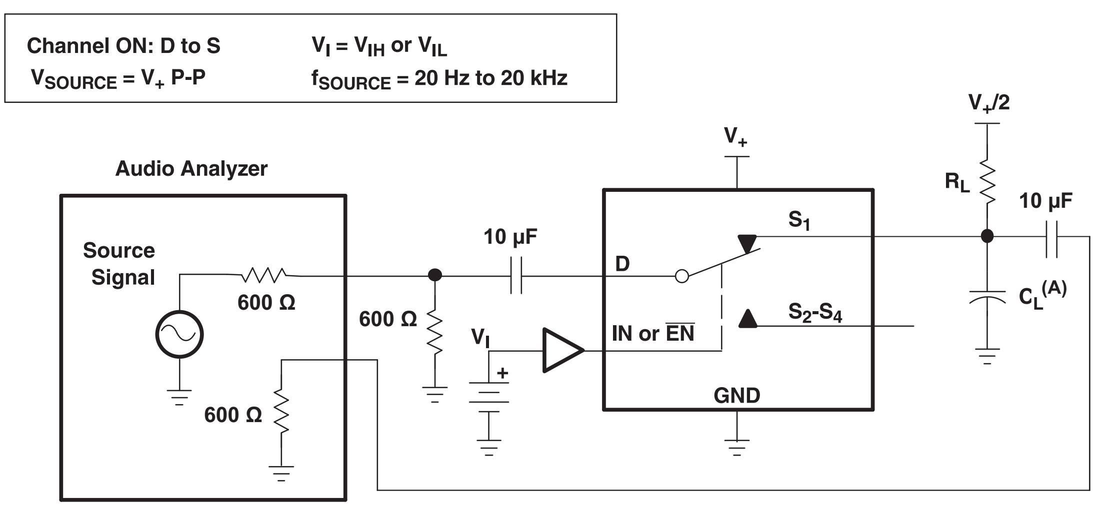
Parameter Measurement Information (continued)



A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r < 5 ns, t_f < 5 ns.

B. C_L includes probe and jig capacitance.

図 21. Charge Injection (Q_C)



A. C_L includes probe and jig capacitance.

図 22. Total Harmonic Distortion (THD)

8 Detailed Description

8.1 Overview

The TS3A5017-Q1 is a dual Single-Pole-4-Throw (SP4T) solid-state analog switch. The TS3A5017-Q1, like all analog switches, is bidirectional. Each D pin connects to its four respective S pins, with the switch connection dependent on the status of $\overline{EN}$, IN2, and IN1. See 表 1 for the switch configuration truth table.

8.2 Functional Block Diagram

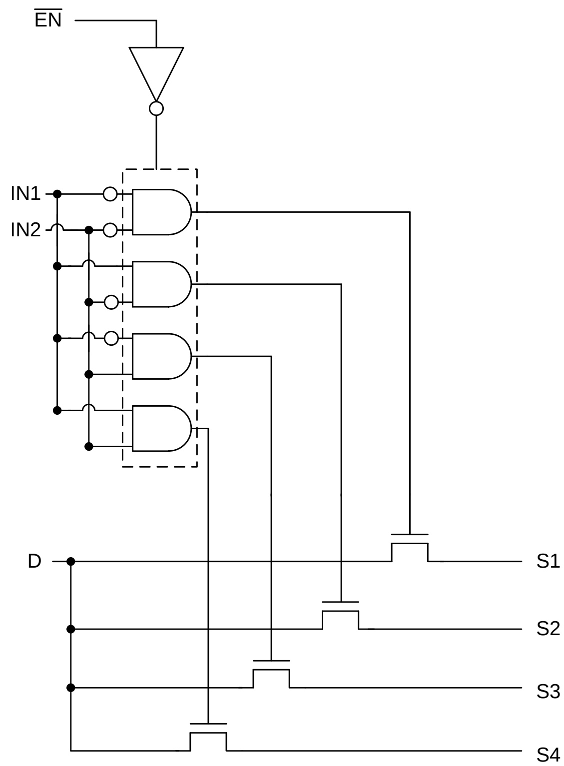


図 23. Functional Block Diagram (Each Switch)

8.3 Feature Description

Isolation in powered-down mode allows signals to be present at the inputs while the switch is powered off without causing damage to the device. The low ON-state resistance and low charge injection give the TS3A5017-Q1 better performance at higher speeds.

8.4 Device Functional Modes

表 1. Function Table

$\overline{EN}$	IN2	IN1	D TO S, S TO D
L	L	L	D = S_1
L	L	H	D = S_2
L	H	L	D = S_3
L	H	H	D = S_4
H	X	X	OFF

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TS3A5017-Q1 can be used in a variety of customer systems. The TS3A5017-Q1 can be used anywhere multiple analog or digital signals must be selected to pass across a single line.

9.2 Typical Application

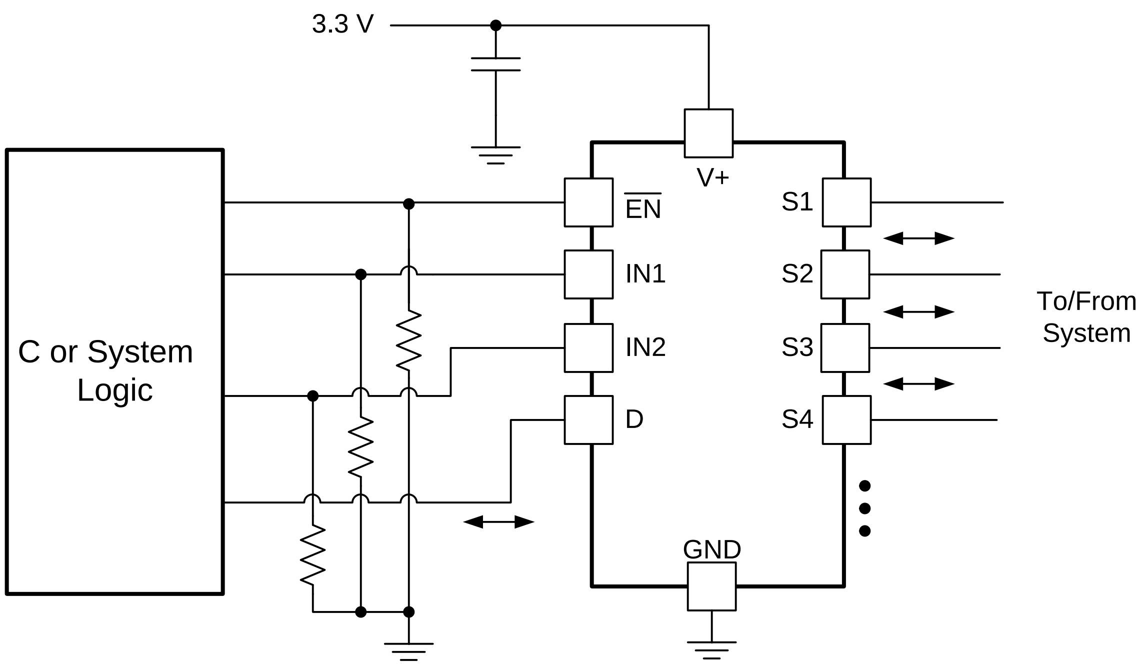


図 24. System Schematic for TS3A5017-Q1

9.2.1 Design Requirements

In this particular application, V+ was 3.3 V, although V+ is allowed to be any voltage specified in *Recommended Operating Conditions*. A decoupling capacitor is recommended on the V+ pin. See *Power Supply Recommendations* for more details.

9.2.2 Detailed Design Procedure

In this application, $\overline{EN}$, IN1, and IN2 are, by default, pulled low to GND. Choose these resistor sizes based on the current driving strength of the GPIO, the desired power consumption, and the switching frequency (if applicable). If the GPIO is open-drain, use pullup resistors instead.

Typical Application (continued)

9.2.3 Application Curve

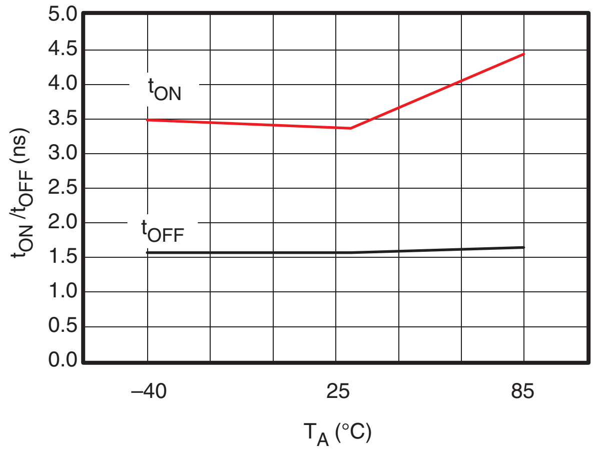


図 25. t_{ON} and t_{OFF} vs Temperature (V_+ = 3.3 V)

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operation Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-µF bypass capacitor is recommended. If there are multiple pins labeled V_{CC}, then a 0.01-µF or 0.022-µF capacitor is recommended for each V_{CC} because the V_{CC} pins will be tied together internally. For devices with dual-supply pins operating at different voltages, for example V_{CC} and V_{DD}, a 0.1-µF bypass capacitor is recommended for each supply pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

11 Layout

11.1 Layout Guidelines

Reflections and matching are closely related to loop antenna theory, but different enough to warrant their own discussion. When a PCB trace turns a corner at a 90° angle, a reflection can occur. This is primarily due to the change of width of the trace. At the apex of the turn, the trace width is increased to 1.414 times its width. This upsets the transmission line characteristics, especially the distributed capacitance and self–inductance of the trace — resulting in the reflection. It is a given that not all PCB traces can be straight, and the traces will turn corners. 図 26 shows progressively better techniques of rounding corners. Only the last example maintains constant trace width and minimizes reflections.

Unused switch I/Os, such as NO, NC, and COM, can be left floating or tied to GND. However, the IN1, IN2, and $\overline{EN}$ pins must be driven high or low. Due to partial transistor turnon when control inputs are at threshold levels, floating control inputs can cause increased I_{CC} or unknown switch selection states. See *Implications of Slow or Floating CMOS Inputs,* SCBA004 for more details.

11.2 Layout Example

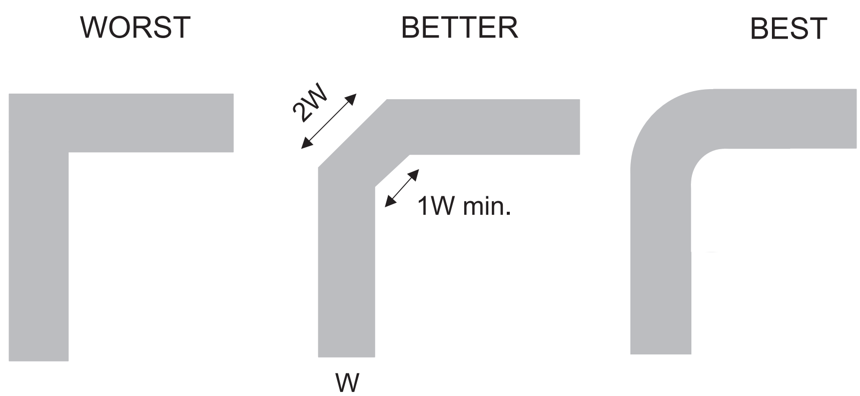


図 26. Trace Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの項目表記

表 2. パラメータの説明

記号	説明
V_{COM}	COM電圧
V_{NC}	NC電圧
V_{NO}	NO電圧
r_{on}	チャネルがオンのときのCOMとNCポート間、またはCOMとNOポート間の抵抗
Δr_{on}	特定デバイスでのチャネル間のr_{on}の差
$r_{on(flat)}$	規定の条件の範囲における、チャネルのr_{on}の最大値と最小値との差
$I_{NC(OFF)}$	対応チャネル(NCからCOM)がオフ状態のとき、NCポートで測定されるリーク電流
$I_{NC(ON)}$	対応チャネル(NCからCOM)がオン状態、出力(COM)がオープンのとき、NCポートで測定されるリーク電流
$I_{NO(OFF)}$	対応チャネル(NOからCOM)がオフ状態のとき、NOポートで測定されるリーク電流
$I_{NO(ON)}$	対応チャネル(NOからCOM)がオン状態、出力(COM)がオープンのとき、NOポートで測定されるリーク電流
$I_{COM(OFF)}$	対応チャネル(COMからNCまたはNO)がオフ状態のとき、COMポートで測定されるリーク電流
$I_{COM(ON)}$	対応チャネル(COMからNCまたはNO)がオン状態、出力(NCまたはNO)がオープンのとき、COMポートで測定されるリーク電流
V_{IH}	制御入力(IN、$\overline{EN}$)の論理HIGHの最小入力電圧
V_{IL}	制御入力(IN、$\overline{EN}$)の論理LOWの最大入力電圧
V_I	制御入力(IN、$\overline{EN}$)の電圧
I_{IH}、I_{IL}	制御入力(IN、$\overline{EN}$)で測定されるリーク電流
t_{ON}	スイッチのターンオン時間。このパラメータは、規定された条件の範囲で、スイッチがオンになるときのデジタル制御(IN)信号とアナログ出力(NCまたはNO)信号との間の伝搬遅延により測定されます。
t_{OFF}	スイッチのターンオフ時間。このパラメータは、規定された条件の範囲で、スイッチがオフになるときのデジタル制御(IN)信号とアナログ出力(NCまたはNO)信号との間の伝搬遅延により測定されます。
Q_C	電荷注入は、制御(IN)入力からアナログ(NCまたはNO)出力への、望ましくない信号のカップリングの測定値です。この値はクーロン(C)単位で、制御入力のスイッチングによって誘導される合計電荷により測定されます。電荷注入$Q_C = C_L \times \Delta V_{COM}$で、$C_L$は負荷容量、$\Delta V_{COM}$はアナログ出力電圧の変化です。
$C_{NC(OFF)}$	対応チャネル(NCからCOM)がオフのときのNCポートの容量
$C_{NC(ON)}$	対応チャネル(NCからCOM)がオンのときのNCポートの容量
$C_{NO(OFF)}$	対応チャネル(NOからCOM)がオフのときのNCポートの容量
$C_{NO(ON)}$	対応チャネル(NOからCOM)がオンのときのNCポートの容量
$C_{COM(OFF)}$	対応チャネル(COMからNC)がオフのときのCOMポートの容量
$C_{COM(ON)}$	対応チャネル(COMからNC)がオンのときのCOMポートの容量
C_I	制御入力(IN、$\overline{EN}$)の容量
O_{ISO}	スイッチのオフ絶縁は、オフ状態のスイッチのインピーダンス測定値です。これは、対応チャネル(NCからCOM)がオフ状態のとき、特定の周波数についてdB単位で測定されます。
X_{TALK}	クロストークは、オンのチャネルからオフのチャネル(NC1からNO1)への、望ましくない信号カップリングの測定値です。隣接クロストークは、オンのチャネルから隣接するオンのチャネル(NC1からNC2)への、望ましくない信号カップリングの測定値です。この値は特定の周波数において、dB単位で測定されます。
BW	スイッチの帯域幅。オン状態のチャネルのゲインがDCゲインより-3dB低くなる周波数です。
THD	全高調波歪は、アナログ・スイッチにより発生する信号の歪みを示します。この値は、2次、3次、およびさらに高次の高調波の二乗平均(RMS)値と、基本波の絶対振幅との比として定義されます。
I_+	制御(IN)ピンがV_+またはGNDであるときの静的消費電流

12.2 ドキュメントのサポート

12.2.1 関連資料

- *『低速またはフローティングCMOS入力の影響』*SCBA004

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

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12.5 商標

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3A5017QRGYRQ1	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5017Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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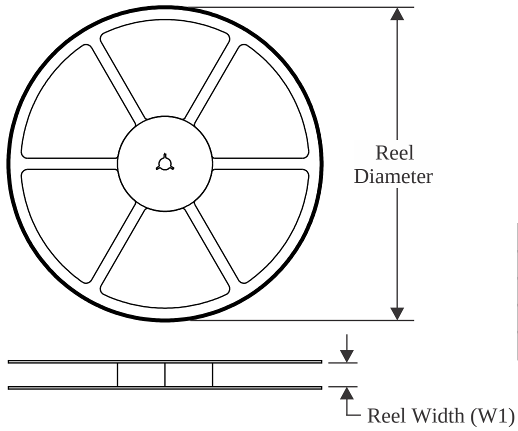
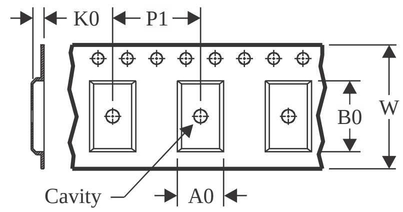
TAPE AND REEL INFORMATION

REEL DIMENSIONS

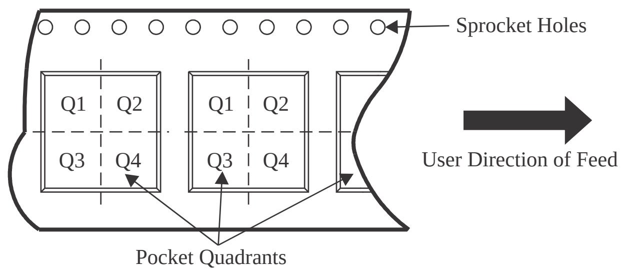


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

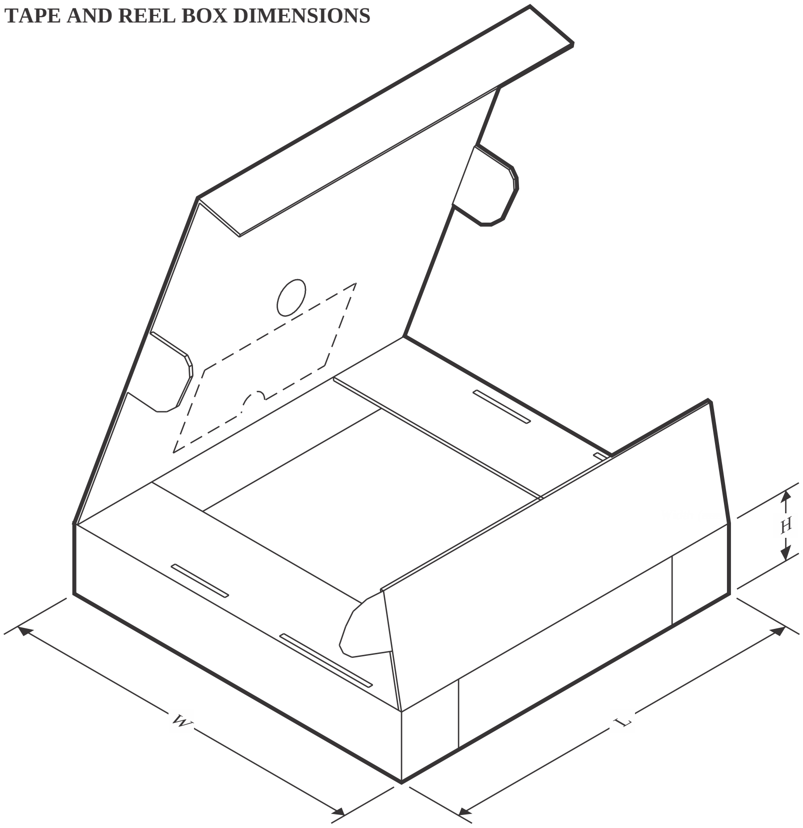
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3A5017QRGYRQ1	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

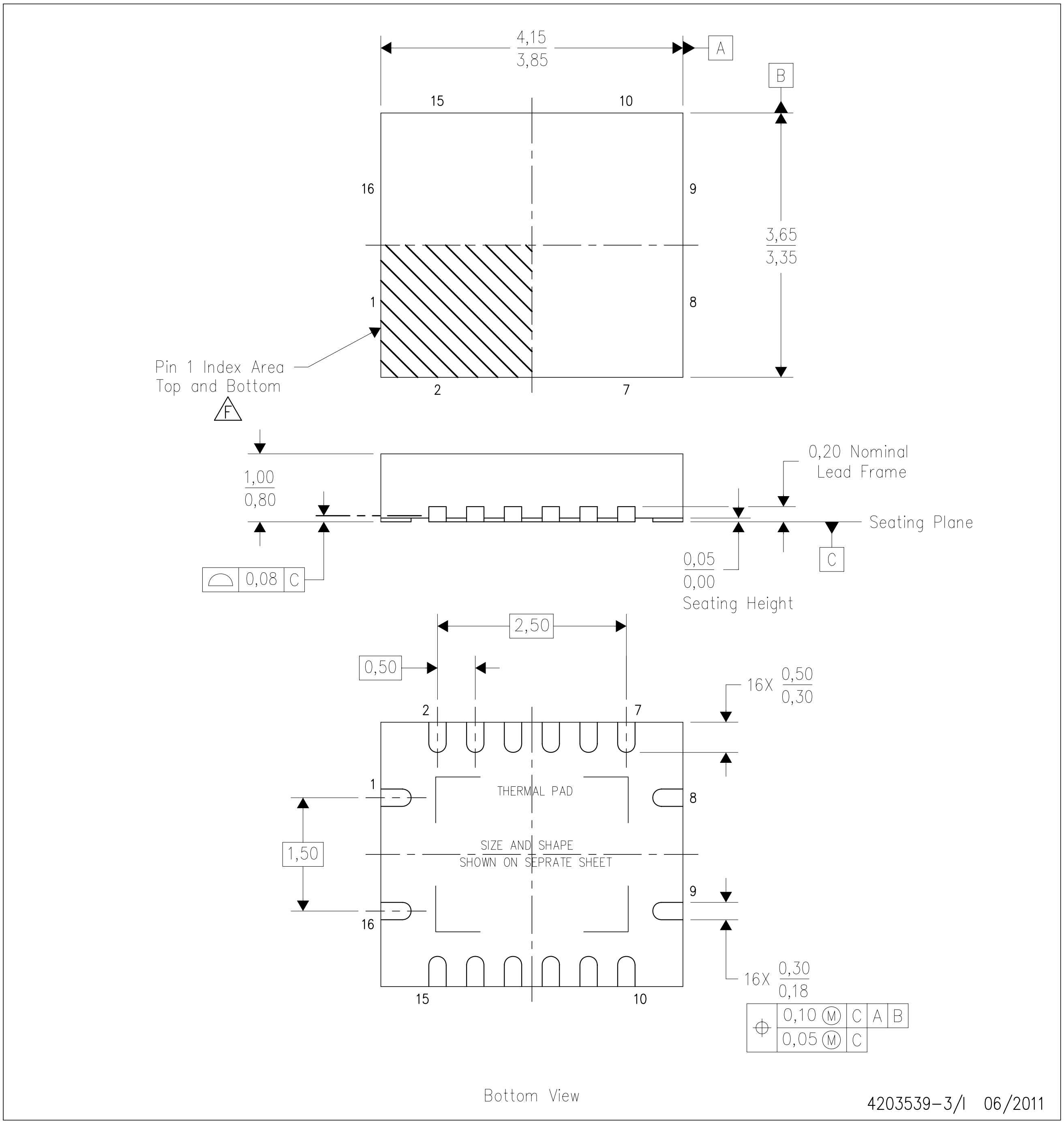
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3A5017QRGYRQ1	VQFN	RGY	16	3000	367.0	367.0	35.0

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

重要なお知らせと免責事項

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