

TRF1305B1 シングルチャネル、DC から 7GHz 超、3dB 帯域幅、RF 完全差動アンプ

1 特長

- 性能が最適化された 3 つのパワー ゲインのバリエーション:
 - 15dB (TRF1305A1)
 - 10dB (TRF1305B1)
 - 5dB (TRF1305C1)
- 固定ゲインは外付け抵抗で低減可能
- 幅広い大信号 RF 帯域幅:
 - TRF1305B1: 7.2GHz (3dB)、6.4GHz (1dB)
- OP1dB (差動 100Ω 負荷):
 - 15.6dBm (2GHz)、12.9dBm (4GHz)
- OIP3: 34.5dBm (2GHz)、25.5dBm (4GHz)
- ノイズ フィギュア: 10.4dB (2GHz)、13.4dB (4GHz)
- スルーレート: 25kV/μs
- 広い入力 (±1V) および出力 (±0.5V) の同相電圧範囲
- 柔軟な構成とモード:
 - シングルエンド入力、差動出力 (S2D)
 - 差動入力、差動出力 (D2D)
 - シングルエンド出力 (性能に制限あり)
 - AC 結合または DC 結合の入出力
 - 調整可能な出力同相電圧
 - 同相入力範囲拡張モード
- 5V、柔軟な単一または分割電源をサポート
- アクティブな消費電力: 475 mW
- (パワーダウン モード時)

2 アプリケーション

- RF サンプリングまたは GSPS ADC ドライバ
- 試験および測定機器
- ワイヤレス通信テスト
- RF デジタイザ
- オシロスコープ (DSO)
- 高速デジタイザ
- スペクトル アナライザ
- ベクトル信号トランシーバ (VST)
- 質量分析システム
- 同相モード レベル シフト
- IQ ミキサ インターフェイス

3 概要

TRF1305B1 は、非常に高性能な閉ループの シングルチャネル RF アンプで、真の DC から 7GHz を超える動作帯域幅を持ちます。このデバイスは、[ADC12DJ5200RF](#) や [ADC32RF5x](#) などの高速で高性能な ADC を、DC 結合または AC 結合のインターフェイスで駆動する優れた性能を備えています。このアンプは、RF、ゼロ IF、複素 IF、および高速の時間領域アプリケーションでの使用に最適化されています。このデバイスは、固定ゲイン構成での性能に最適化されています。より低いゲインが必要な場合は、外付け抵抗を使用します。

TRF1305B1 は、異なる出力同相電圧と入力同相電圧を設定できる VOVM ピンを備えています (たとえば、レベルシフトや、異なる DC 同相電圧を持つほとんどの IQ 降圧コンバータの ADC インターフェイス アプリケーション用)。また TRF1305B1 は、2 レールのフローティング分割または単一電源のオプションと、入力同相範囲を電源に近い範囲に拡張できる MODE ピンを備えています。

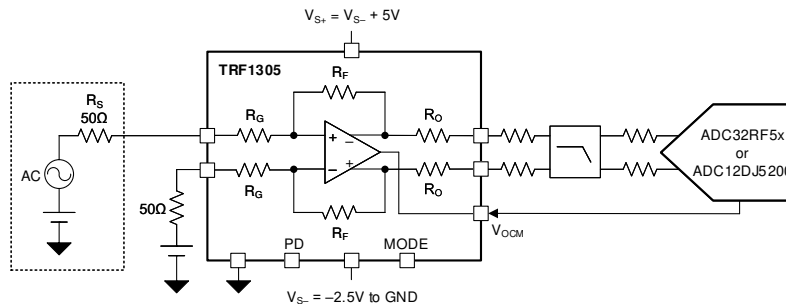
TRF1305B1 には、パワー ダウン機能があります。このデバイスは、テキサス・インスツルメンツ独自の高度な BiCMOS プロセスで製造されており、省スペースの 2mm × 2mm、12 ピンの WQFN-FCRLF パッケージで供給されます。

製品情報

部品番号 ⁽¹⁾	D2D パワー ゲイン	パッケージ ⁽²⁾
TRF1305A1 ⁽³⁾	15 dB	RPV (WQFN-FCRLF, 12)
TRF1305B1	10 dB	
TRF1305C1 ⁽³⁾	5 dB	

- (1) [セクション 4](#) を参照してください。
- (2) 詳細については、[セクション 11](#) を参照してください。
- (3) プレビュー情報 (量産データではありません)。





S2D 構成で高速 ADC を駆動する TRF1305x1

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4 Device Comparison Table

DEVICE	GAIN	CHANNEL COUNT
TRF1305A1 (preview)	15dB	1
TRF1305B1	10dB	
TRF1305C1 (preview)	5dB	
TRF1305A2 (preview)	15dB	2
TRF1305B2	10dB	
TRF1305C2 (preview)	5dB	

5 Pin Configuration and Functions

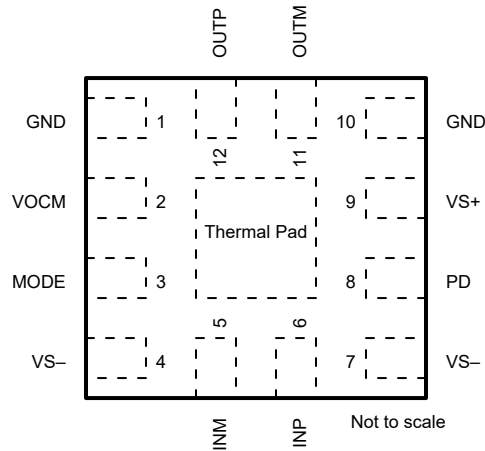


図 5-1. RPV Package, 12-Pin WQFN-FCRLF (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	1, 10	Ground	Ground. Reference for RF signals and PD control signal. Connect to ground plane on the board. Internally shorted to the thermal pad.
INM	5	Input	Negative side of differential input signal
INP	6	Input	Positive side of differential input signal
MODE	3	Input	Mode selection pin. See also MODE Pin section .
OUTM	11	Output	Negative side of differential output signal
OUTP	12	Output	Positive side of differential output signal
PD	8	Input	Power-down signal, referenced to GND. Supports both 1.8V and 3.3V logic. Logic 0 or open = device enabled. Logic 1 = device powered down.
VOCM	2	Input	Output common-mode voltage input pin. Floating the pin sets the output common-mode voltage to $V_{S-} + 2.5V$.
VS-	4, 7	Power	Negative supply voltage
VS+	9	Power	Positive supply voltage
Thermal Pad	Pad	Ground	Thermal pad. Connect to heat-dissipating ground plane on the board. Internally shorted to GND.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{S-}	Negative supply voltage, referenced to GND	-3	0.3	V
V_{S+}	Positive supply voltage	-0.3	$V_{S-} + 5.5$	V
V_S	Total supply voltage, $V_S = V_{S+} - V_{S-}$	-0.3	5.5	V
P_{IN}	Input RF power ⁽²⁾		20	dBm
V_{PD}	PD pin voltage, referenced to GND, $V_{S+} \geq 3.3V$	-0.3	3.6	V
	PD pin voltage, referenced to GND, $V_{S+} < 3.3V$	-0.3	$V_{S+} + 0.3$	
V_{OCM}	VOCM pin voltage	$V_{S-} + 1$	$V_{S-} + 4$	V
V_{MODE}	MODE pin voltage	$V_{S-} - 0.3$	$V_{S-} + 3.3$	V
T_J	Junction temperature	-40	150	°C
T_{stg}	Storage temperature	-40	150	°C

- Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- When device supplies are present; otherwise, limit swing at the device pins to $V_{S-} \pm 0.3V$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±500	

- JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{S-}	Negative supply voltage	-2.5		0	V
V_S	Total supply voltage, $V_S = V_{S+} - V_{S-}$	4.75	5	5.25	V
T_J	Junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TRF1305x1	UNIT
		RPV (WQFN-FCRLF)	
		12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	62.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	29.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	26.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	18.8	°C/W

- For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics - TRF1305B1

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output with differential source impedance (Z_S) = 100Ω, differential output load (Z_L) = 100Ω, external input resistor network (see [Figure 8-3](#)), and inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
AC PERFORMANCE							
SSBW	Small-signal bandwidth (3dB)	$P_{\text{IN}} = -20\text{dBm}$ at each input			7.3		GHz
	Small-signal bandwidth (1dB)	$P_{\text{IN}} = -20\text{dBm}$ at each input			6.4		
LSBW	Large-signal bandwidth (3dB)	Differential $P_{\text{IN}} = -3\text{dBm}$			7.2		GHz
	Large-signal bandwidth (1dB)	Differential $P_{\text{IN}} = -3\text{dBm}$			6.4		
Sdd21	Power gain	$f = 500\text{MHz}$			9.8		dB
		$f = 4\text{GHz}$			10		
	Gain variation over temperature	$f = 4\text{GHz}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$			2		dB
Sdd11	Input return loss	$f = 10\text{MHz}$ to 5GHz			-13		dB
Sdd12	Reverse isolation	$f < 5\text{GHz}$ (device enabled)			-23		dB
G_{IMB}	Differential gain imbalance	$f < 5\text{GHz}$, S2D, $P_{\text{IN}} = -20\text{dBm}$ with $50\Omega Z_S$			± 0.2		dB
PH_{IMB}	Differential phase imbalance	$f < 5\text{GHz}$, S2D, $P_{\text{IN}} = -20\text{dBm}$ with $50\Omega Z_S$			± 2		°
OP1dB	Output 1dB compression point	$f = 500\text{MHz}$			15.5		dBm
		$f = 1\text{GHz}$			15.8		
		$f = 2\text{GHz}$			15.6		
		$f = 3\text{GHz}$			14.9		
		$f = 4\text{GHz}$			12.9		
		$f = 5\text{GHz}$			11		
HD2	Second-order harmonic distortion	$V_O = 2V_{\text{PP}}$	$f = 500\text{MHz}$		-87		dBc
			$f = 1\text{GHz}$		-72		
			$f = 2\text{GHz}$		-60		
			$f = 3\text{GHz}$		-55		
			$f = 4\text{GHz}$		-53		
HD3	Third-order harmonic distortion	$V_O = 2V_{\text{PP}}$	$f = 500\text{MHz}$		-70		dBc
			$f = 1\text{GHz}$		-63		
			$f = 2\text{GHz}$		-67.5		
			$f = 3\text{GHz}$		-50		
			$f = 4\text{GHz}$		-48		
OIP2	Output second-order intercept point	$P_O = 1\text{dBm}$ per tone, 2MHz spacing	$f = 500\text{MHz}$		90		dBm
			$f = 1\text{GHz}$		73		
			$f = 2\text{GHz}$		61		
			$f = 3\text{GHz}$		56		
			$f = 4\text{GHz}$		55		
			$f = 5\text{GHz}$		58		
OIP3	Output third-order intercept point	$P_O = 1\text{dBm}$ per tone, 2MHz spacing	$f = 500\text{MHz}$		43.5		dBm
			$f = 1\text{GHz}$		40		
			$f = 2\text{GHz}$		34.5		
			$f = 3\text{GHz}$		32.5		
			$f = 4\text{GHz}$		25.5		
			$f = 5\text{GHz}$		20		

6.5 Electrical Characteristics - TRF1305B1 (続き)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output with differential source impedance (Z_S) = 100Ω, differential output load (Z_L) = 100Ω, external input resistor network (see [Figure 8-3](#)), and inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NF	Noise figure	f = 500MHz		8		dB
		f = 1GHz		8.6		
		f = 2GHz		10.4		
		f = 3GHz		11.6		
		f = 4GHz		13.4		
		f = 5GHz		13.2		
NSD	Output noise spectral density	f = 500MHz		-156.2		dBm/Hz
		f = 1GHz		-155.5		
		f = 2GHz		-153.6		
		f = 3GHz		-152.3		
		f = 4GHz		-150.5		
		f = 5GHz		-150.8		
DC PERFORMANCE						
V _{OD-MAX}	Max differential output voltage	f = 1GHz		4		V _{PP}
	Slew rate	2V V _O step, S2D configuration, V _{S+} = 2.5V, V _{S-} = -2.5V		25		kV/μs
	Output differential offset voltage			±3		mV
	Overdrive recovery time	From 2 × overdrive of each SE output to each output voltage settling to < ±50mV		6		ns
COMMON-MODE						
V _{ICM}	Input common-mode voltage	Default range ⁽¹⁾	V _{S-} + 1.5	V _{S-} + 3.5		V
V _{OCM}	Output common-mode voltage		V _{S-} + 2	V _{S-} + 3		V
	Output common-mode offset voltage from V _{OCM} voltage			±10		mV
IMPEDANCE						
Z _{in-SE}	Single-ended input impedance	At INP pin with appropriate termination on INM pin		47		Ω
Z _{O-DIFF}	Differential output impedance	f = near dc		8		Ω
POWER SUPPLY						
I _{QA}	Active quiescent current			95		mA
I _{QPD}	Power-down quiescent current			13.5		mA
POWER DOWN						
V _{PD_Hi}	PD pin logic high	Referenced to GND, see Section 6.1	1.35			V
V _{PD_Lo}	PD pin logic low	Referenced to GND, see Section 6.1			0.3	V
I _{PD_Bias}	PD bias current (current on PD pin)	PD = high (1.8V logic)		10.5	15	μA
		PD = high (3.3V logic)		19	30	
t _{ON}	Turn-on time	From 50% V _{PD} transition to 90% RF out		25		ns
t _{OFF}	Turn-off time	From 50% V _{PD} transition to 10% RF out		20		ns

(1) V_{ICM} range can be extended closer to V_{S+} or V_{S-} in D2D configuration. See also [Section 7.4.1](#).

6.6 Typical Characteristics - TRF1305B1

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, $V_{\text{ICM}} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\Omega$, $Z_L = 100\Omega$, external input resistor network (see [8-3](#)), inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)

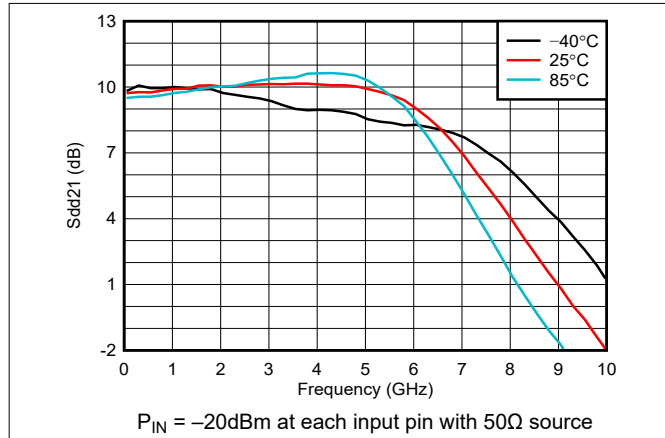


图 6-1. Power Gain (Sdd21) Across Temperature

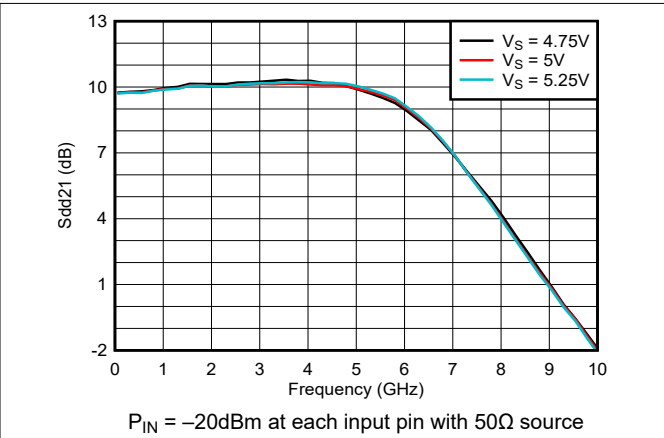


图 6-2. Power Gain (Sdd21) Across Supply Voltage

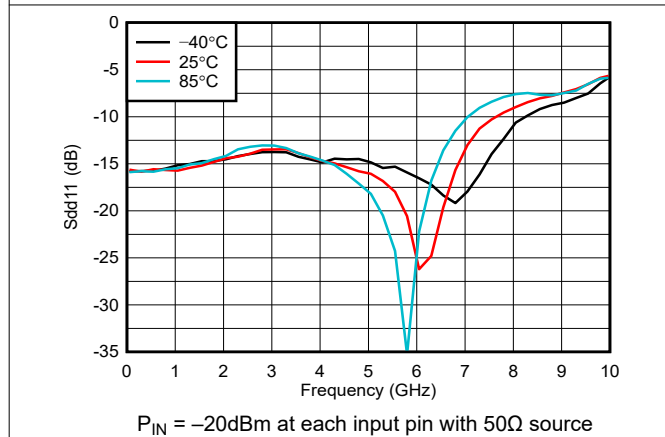


图 6-3. Input Return Loss (Sdd11) Across Temperature

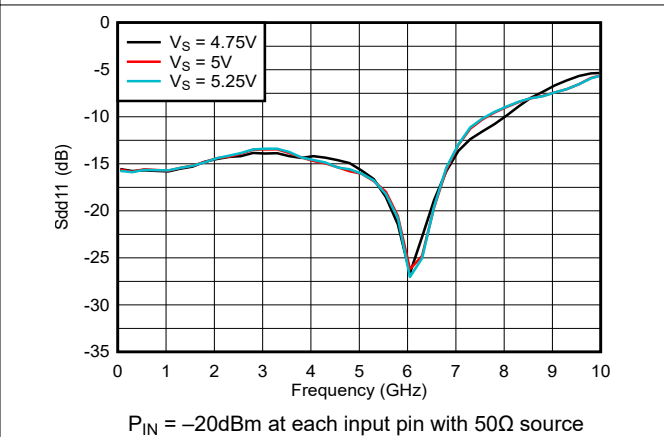


图 6-4. Input Return Loss (Sdd11) Across Supply Voltage

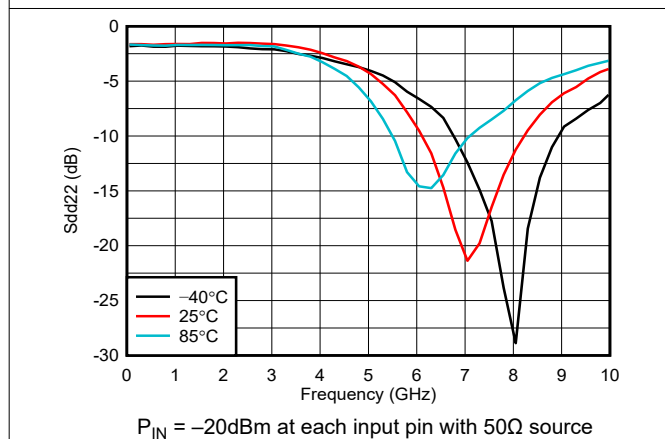


图 6-5. Output Return Loss (Sdd22) Across Temperature

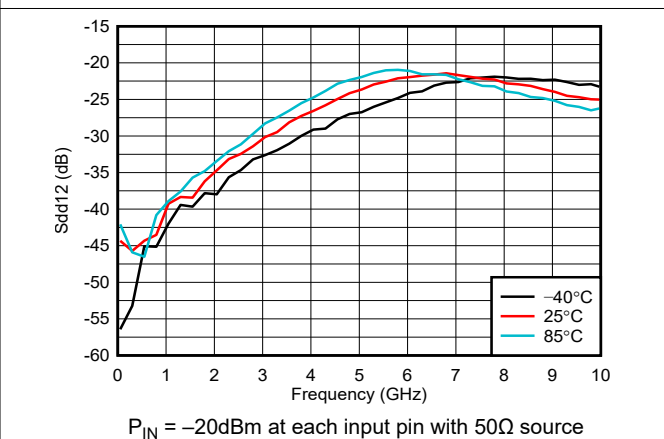


图 6-6. Reverse Isolation (Sdd12) Across Temperature

6.6 Typical Characteristics - TRF1305B1 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, $V_{\text{ICM}} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\Omega$, $Z_L = 100\Omega$, external input resistor network (see [Figure 8-3](#)), inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)

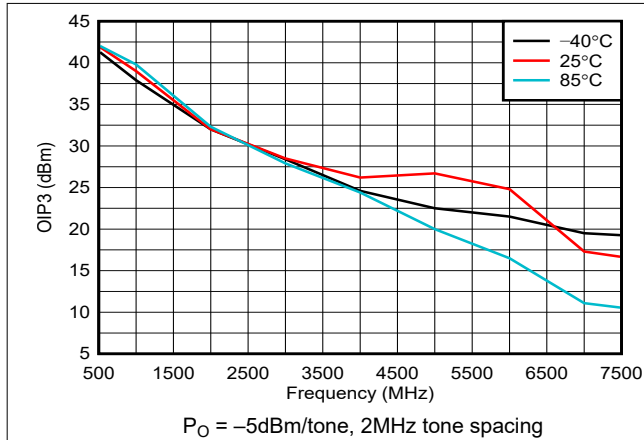


Figure 6-7. OIP3 Across Temperature

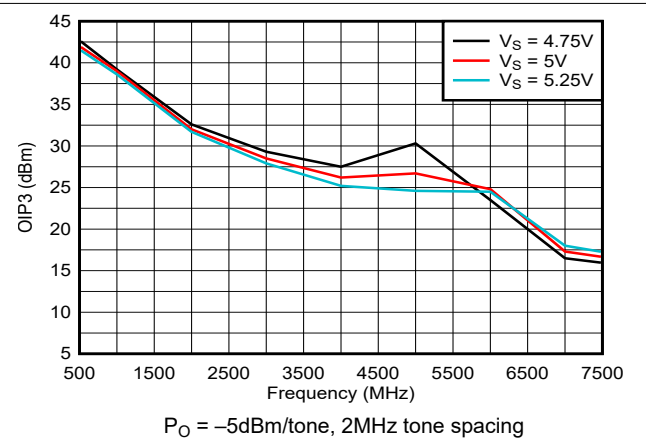


Figure 6-8. OIP3 Across Supply Voltage

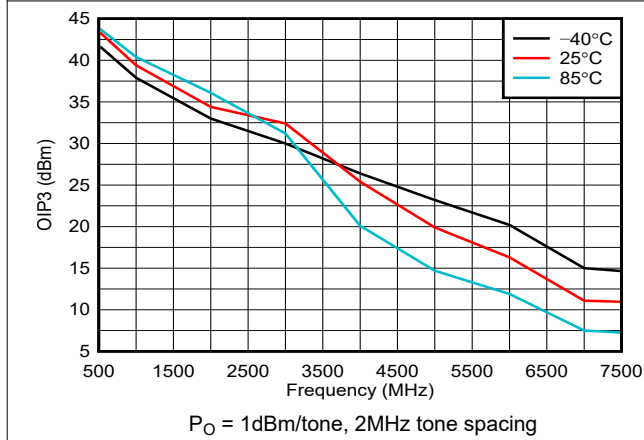


Figure 6-9. OIP3 Across Temperature

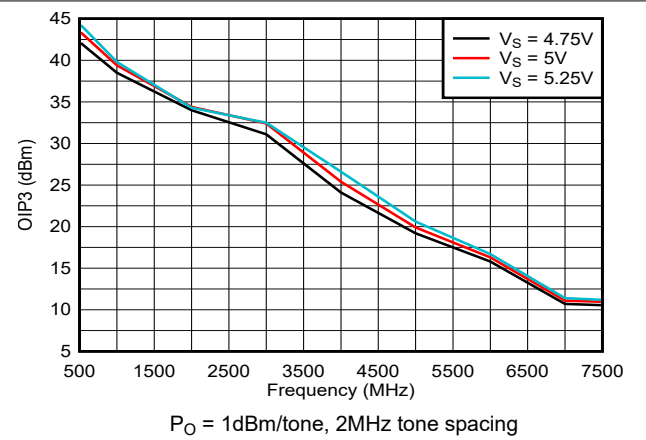


Figure 6-10. OIP3 Across Supply Voltage

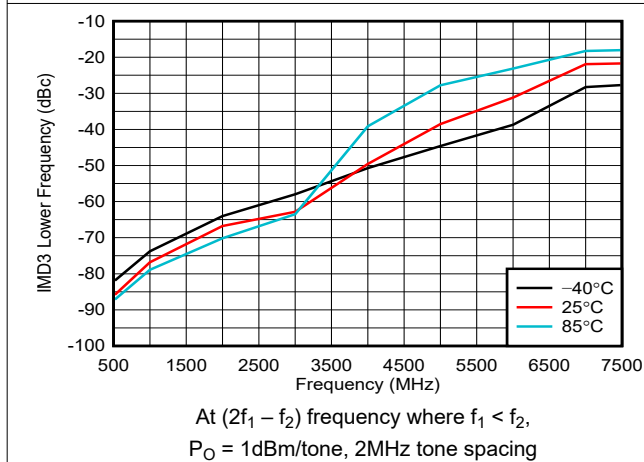


Figure 6-11. IMD3 Lower Across Temperature

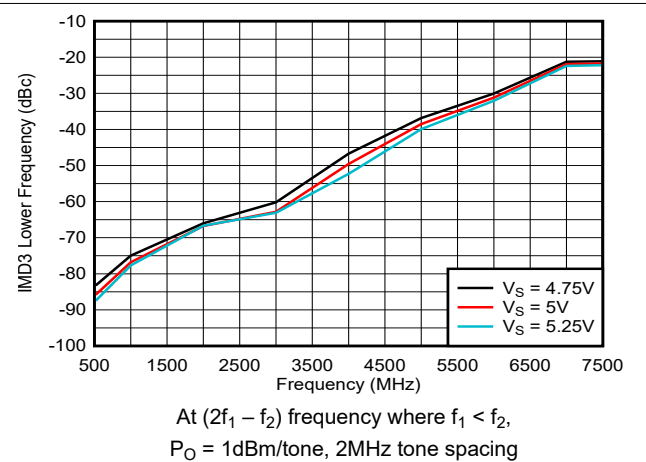
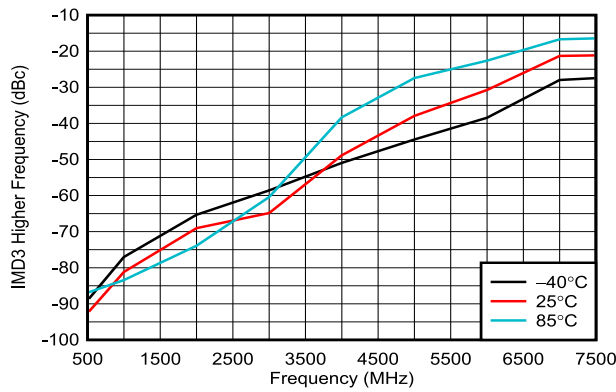


Figure 6-12. IMD3 Lower Across Supply Voltage

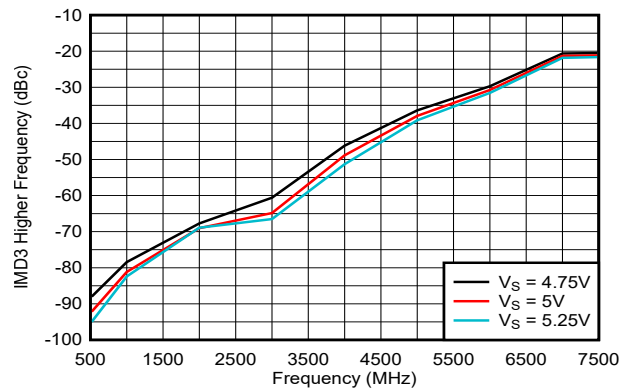
6.6 Typical Characteristics - TRF1305B1 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, V_{ICM} = midsupply, D2D ac-coupled input/output configuration with $Z_S = 100\Omega$, $Z_L = 100\Omega$, external input resistor network (see [8-3](#)), inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



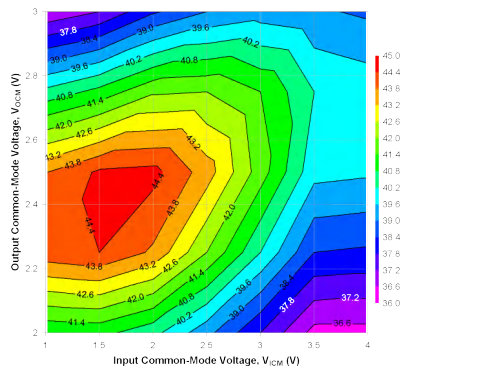
At $(2f_2 - f_1)$ frequency where $f_1 < f_2$,
 $P_O = 1\text{dBm/tone}$, 2MHz tone spacing

6-13. IMD3 Higher Across Temperature



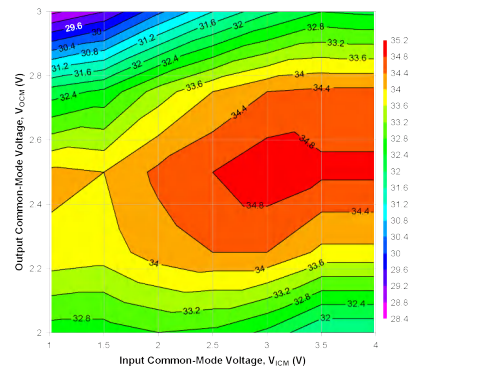
At $(2f_2 - f_1)$ frequency where $f_1 < f_2$,
 $P_O = 1\text{dBm/tone}$, 2MHz tone spacing

6-14. IMD3 Higher Across Supply Voltage



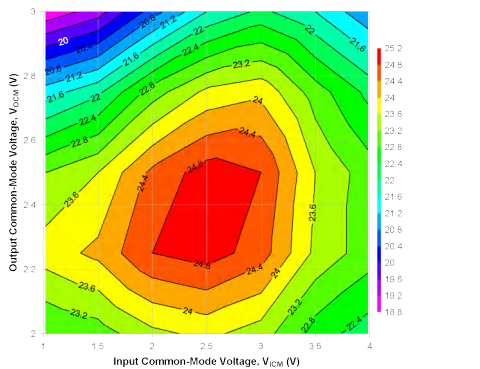
$P_O = 1\text{dBm/tone}$, 2MHz tone spacing,
 dc-coupled inputs with V_{ICM} forced through bias tees

6-15. OIP3 Across V_{ICM} and V_{OCM} at 500MHz



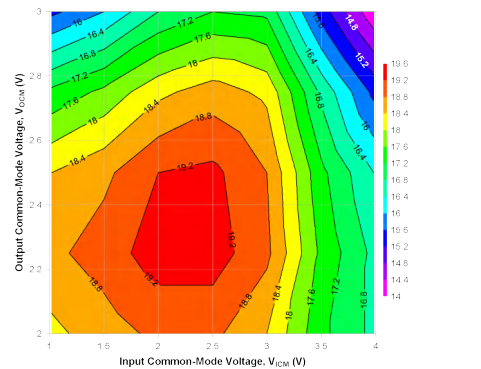
$P_O = 1\text{dBm/tone}$, 2MHz tone spacing,
 dc-coupled inputs with V_{ICM} forced through bias tees

6-16. OIP3 Across V_{ICM} and V_{OCM} at 2GHz



$P_O = 1\text{dBm/tone}$, 2MHz tone spacing,
 dc-coupled inputs with V_{ICM} forced through bias tees

6-17. OIP3 Across V_{ICM} and V_{OCM} at 4GHz

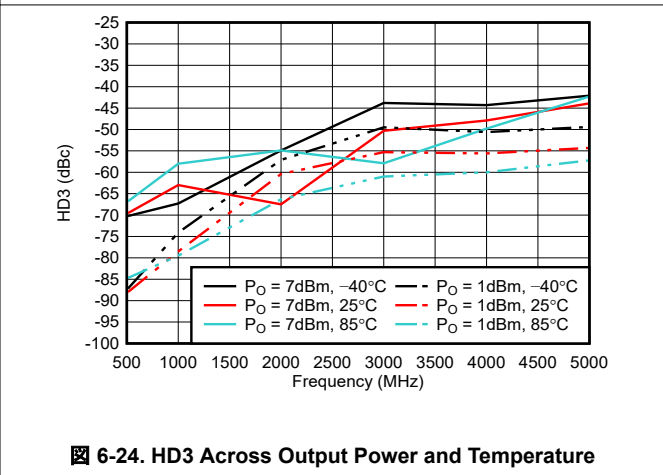
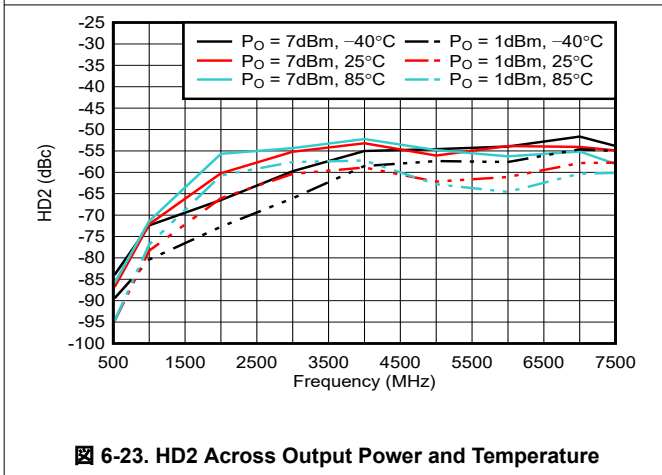
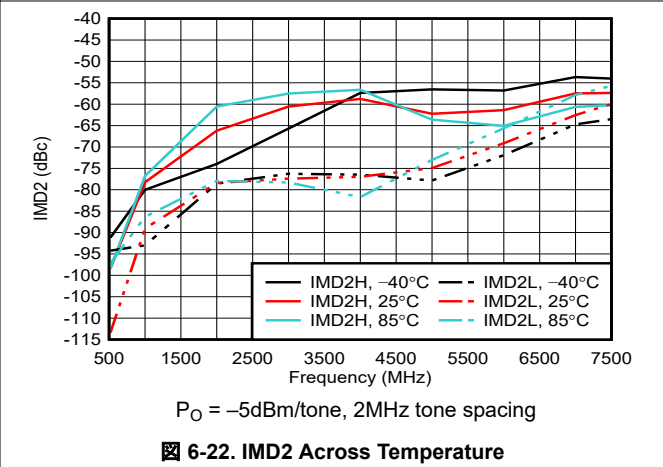
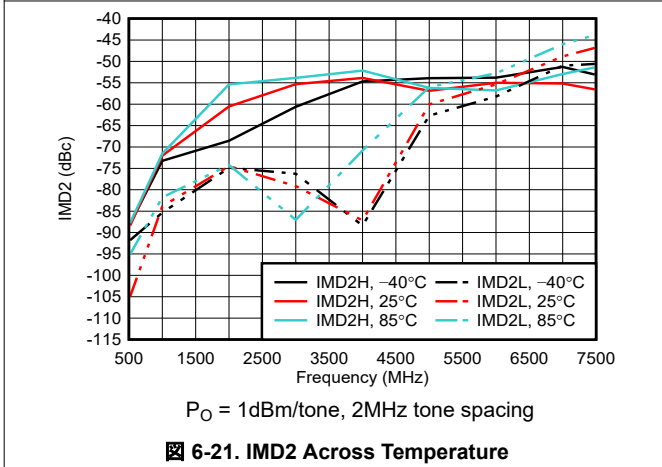
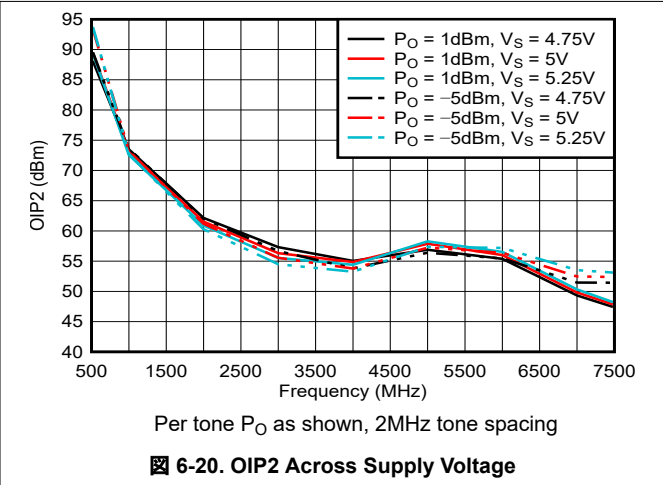
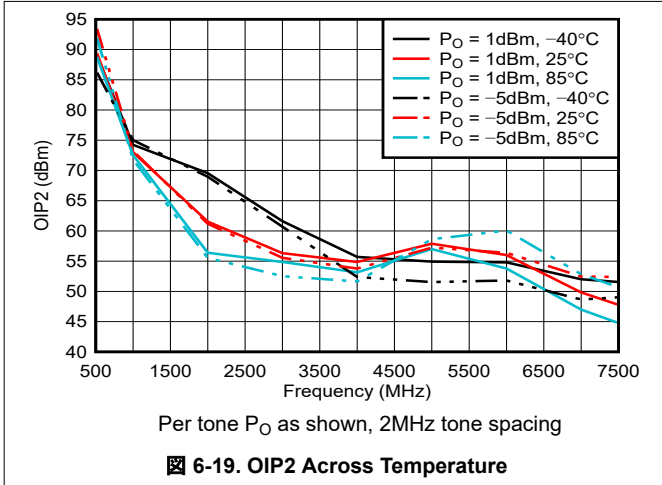


$P_O = 1\text{dBm/tone}$, 2MHz tone spacing,
 dc-coupled inputs with V_{ICM} forced through bias tees

6-18. OIP3 Across V_{ICM} and V_{OCM} at 5GHz

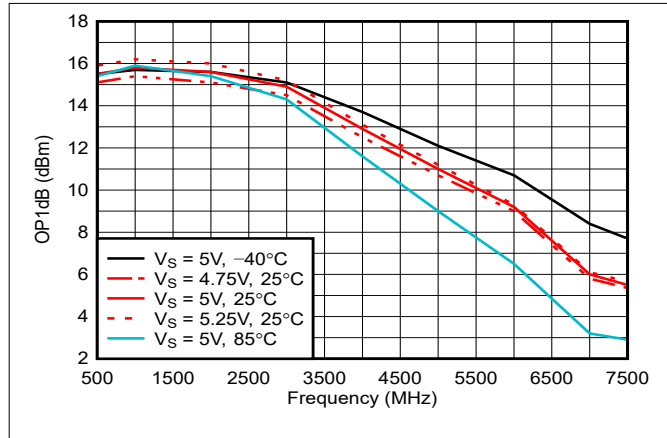
6.6 Typical Characteristics - TRF1305B1 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, $V_{\text{ICM}} = \text{mid supply}$, D2D ac-coupled input/output configuration with $Z_S = 100\Omega$, $Z_L = 100\Omega$, external input resistor network (see [8-3](#)), inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)

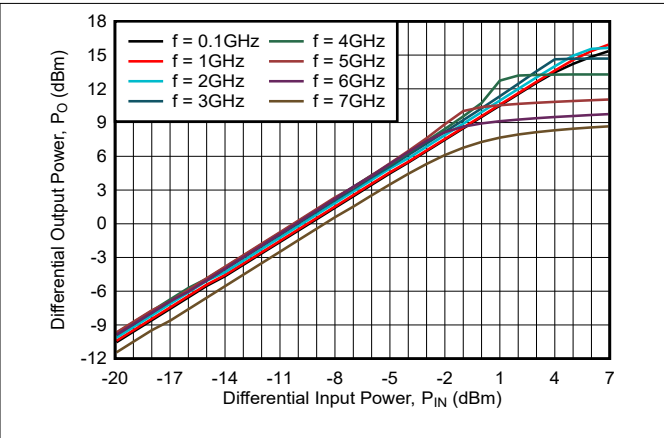


6.6 Typical Characteristics - TRF1305B1 (continued)

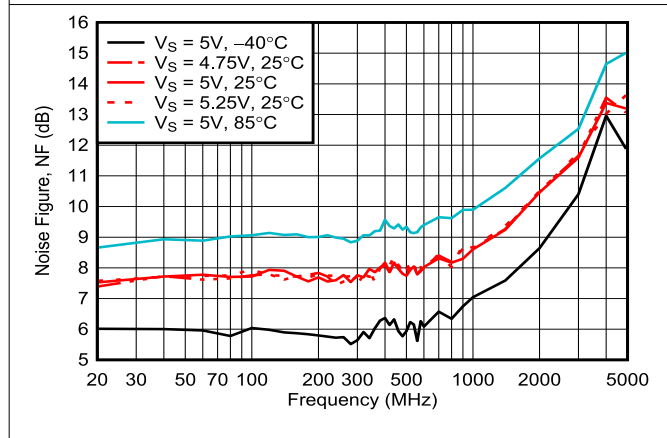
at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, $V_{\text{ICM}} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\Omega$, $Z_L = 100\Omega$, external input resistor network (see [8-3](#)), inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



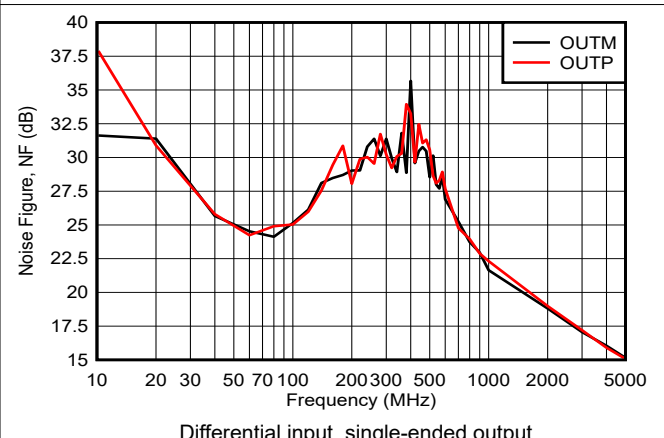
6-25. OP1dB Across Supply Voltage and Temperature



6-26. Differential Input vs Differential Output Power



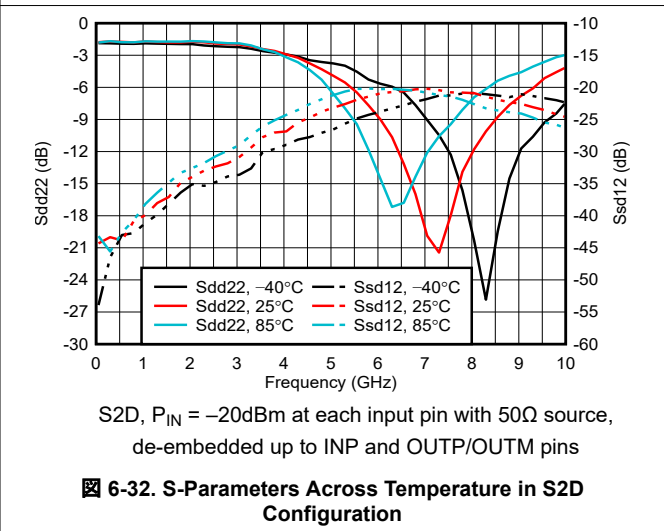
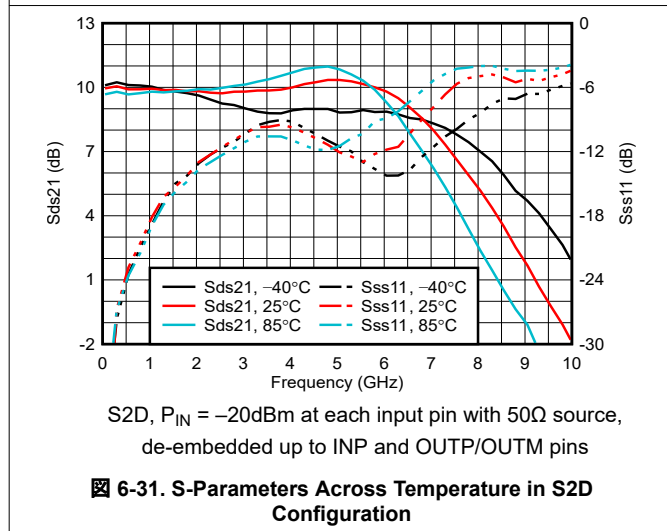
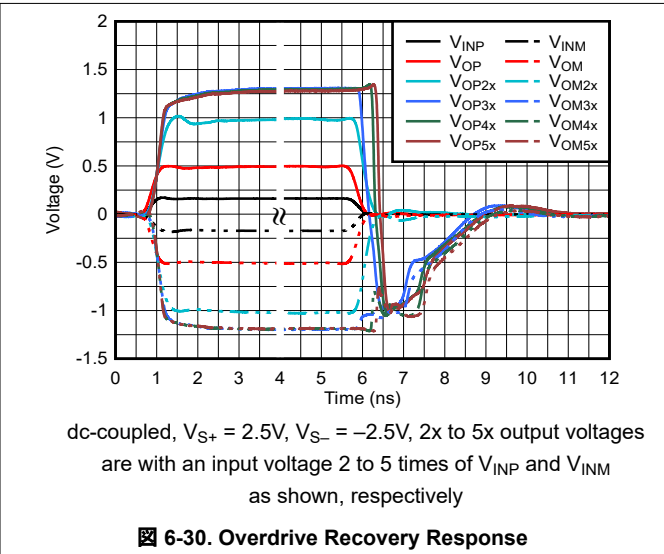
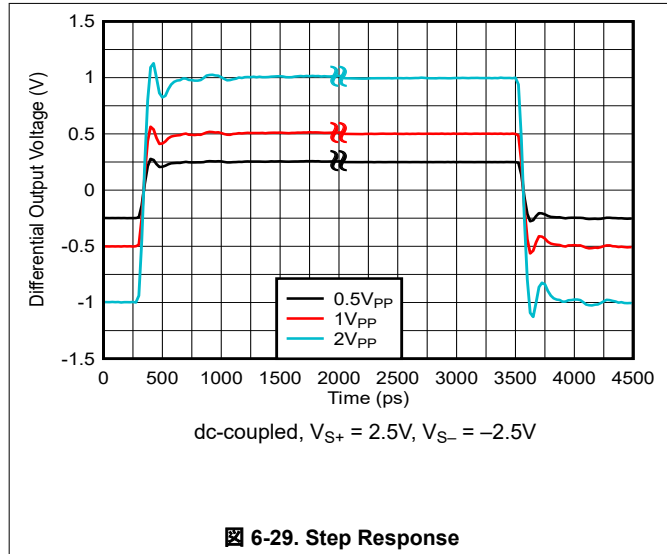
6-27. Noise Figure Across Temperature



6-28. Noise Figure at Each Single-Ended Output

6.6 Typical Characteristics - TRF1305B1 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, $V_{ICM} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\Omega$, $Z_L = 100\Omega$, external input resistor network (see [Figure 8-3](#)), inputs de-embedded up to R_{IN_SER} and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



6.6 Typical Characteristics - TRF1305B1 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, $V_{\text{ICM}} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\Omega$, $Z_L = 100\Omega$, external input resistor network (see [8-3](#)), inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)

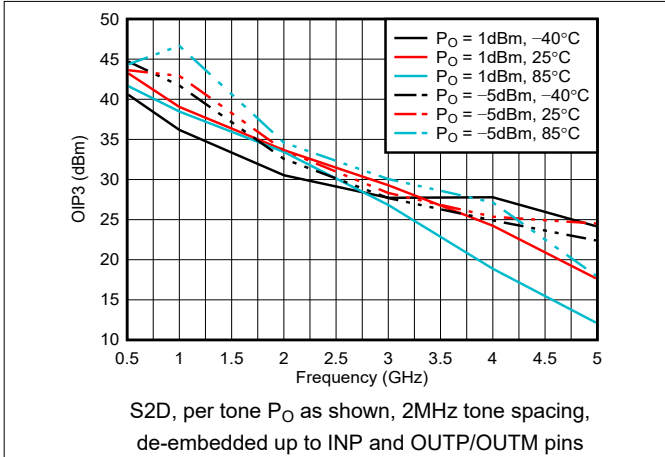


图 6-33. OIP3 Across Temperature and Output Power

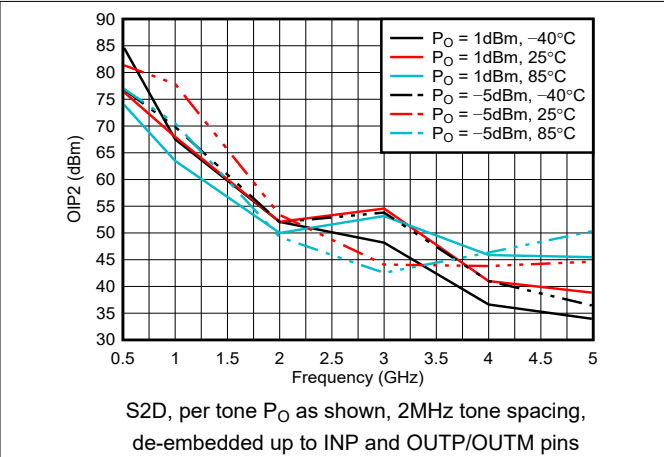


图 6-34. OIP2 Across Temperature and Output Power

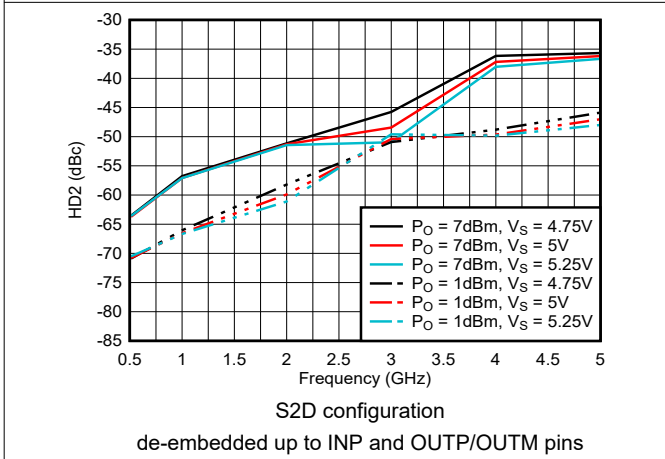


图 6-35. HD2 Across Supply Voltage and Output Power

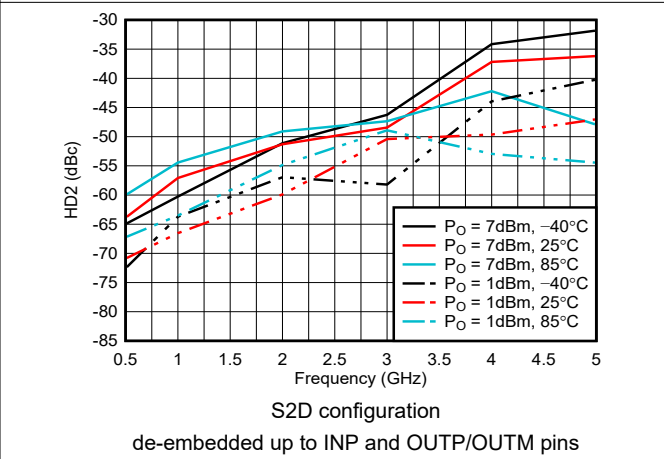
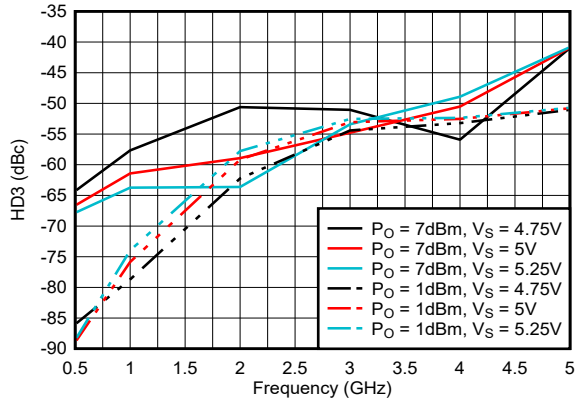


图 6-36. HD2 Across Temperature and Output Power

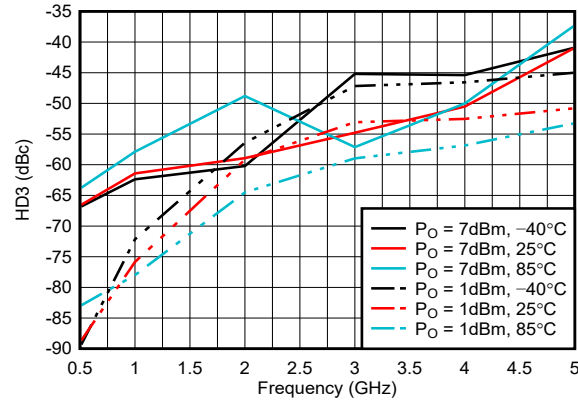
6.6 Typical Characteristics - TRF1305B1 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, $V_{\text{ICM}} = \text{mid supply}$, D2D ac-coupled input/output configuration with $Z_S = 100\Omega$, $Z_L = 100\Omega$, external input resistor network (see [8-3](#)), inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



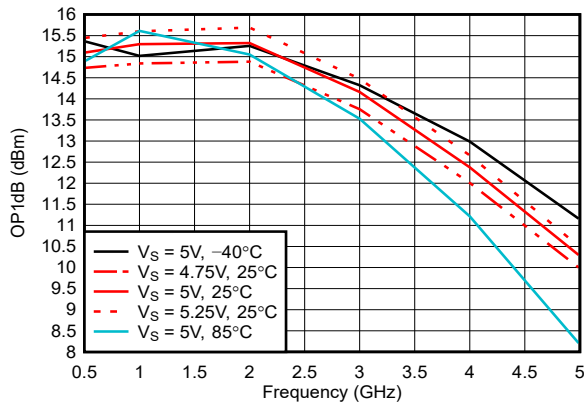
S2D configuration
de-embedded up to INP and OUTP/OUTM pins

6-37. HD3 Across Supply Voltage and Output Power



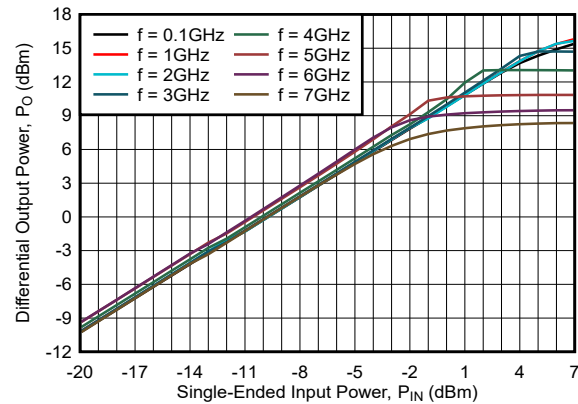
S2D configuration
de-embedded up to INP and OUTP/OUTM pins

6-38. HD3 Across Temperature and Output Power



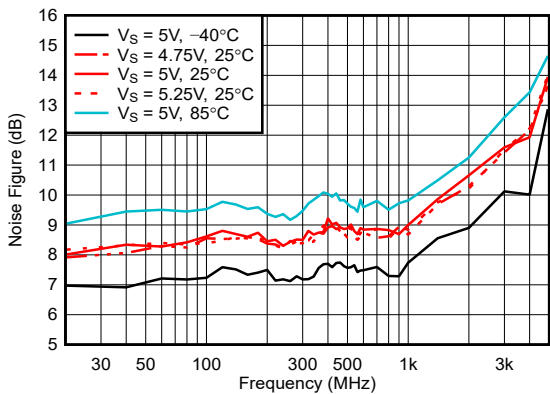
S2D, de-embedded up to INP and OUTP/OUTM pins

6-39. OP1dB Across Supply Voltage and Temperature



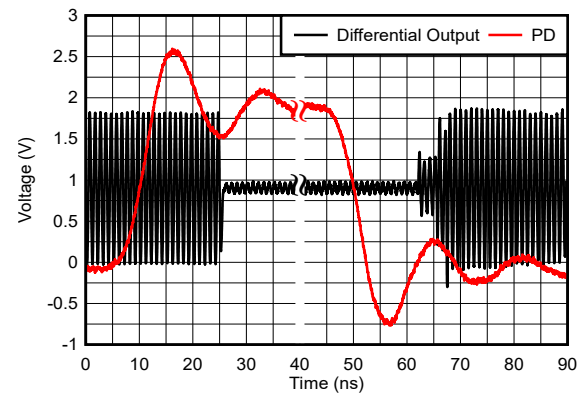
S2D, de-embedded up to INP and OUTP/OUTM pins

6-40. Single-Ended Input vs Differential Output Power



S2D, de-embedded up to INP and OUTP/OUTM pins

6-41. Noise Figure in S2D Configuration

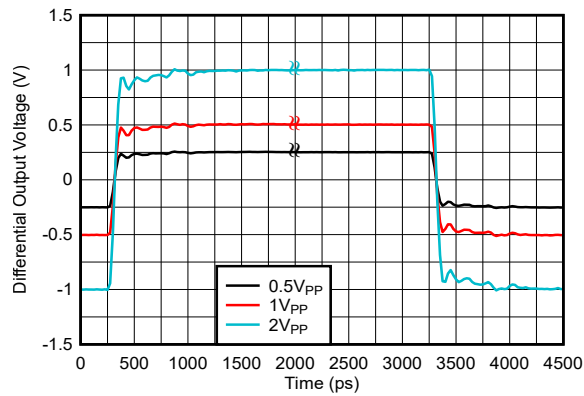


S2D, dc-coupled, $V_{S+} = 2.5\text{V}$, $V_{S-} = -2.5\text{V}$

6-42. Power Up and Power Down Timing

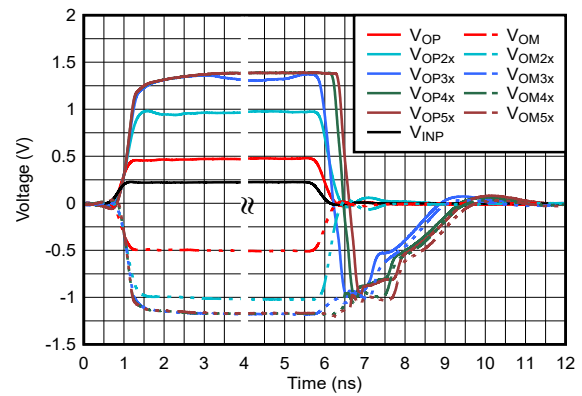
6.6 Typical Characteristics - TRF1305B1 (continued)

at $T_A = 25^\circ\text{C}$, $V_{S+} = 5\text{V}$, $V_{S-} = 0\text{V}$, floating VO_{CM}, PD, and MODE pins, $V_{\text{ICM}} = \text{midsupply}$, D2D ac-coupled input/output configuration with $Z_S = 100\Omega$, $Z_L = 100\Omega$, external input resistor network (see [8-3](#)), inputs de-embedded up to $R_{\text{IN_SER}}$ and outputs up to the device pins, ambient temperatures shown, and resistor network included as part of DUT characteristic plots (unless otherwise noted)



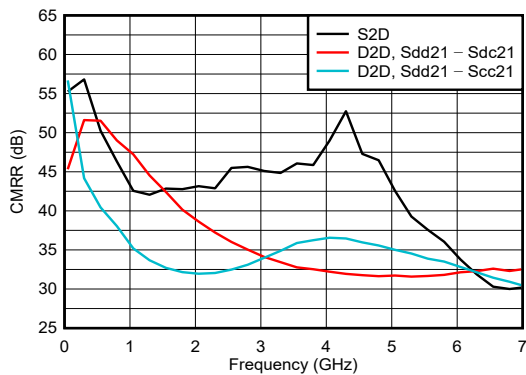
S2D, dc-coupled, $V_{S+} = 2.5\text{V}$, $V_{S-} = -2.5\text{V}$

Figure 6-43. S2D Step Response



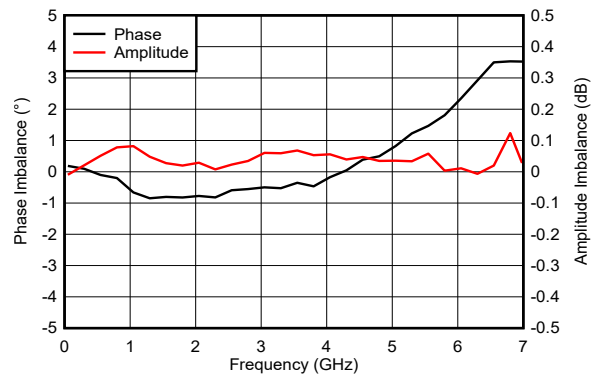
S2D, dc-coupled, $V_{S+} = 2.5\text{V}$, $V_{S-} = -2.5\text{V}$,
2x to 5x output voltages are with an input voltage 2 to 5 times
that of V_{INP} as shown, respectively

Figure 6-44. S2D Overdrive Recovery Response



$P_{\text{IN}} = -20\text{dBm}$ at each driven input pin with 50Ω source,
c in Sdc21 and Scc21 is for common-mode

Figure 6-45. Common-Mode Rejection Ratio (CMRR)



S2D, $P_{\text{IN}} = -20\text{dBm}$ at each input pin with 50Ω source

Figure 6-46. Amplitude and Phase Imbalance

7 Detailed Description

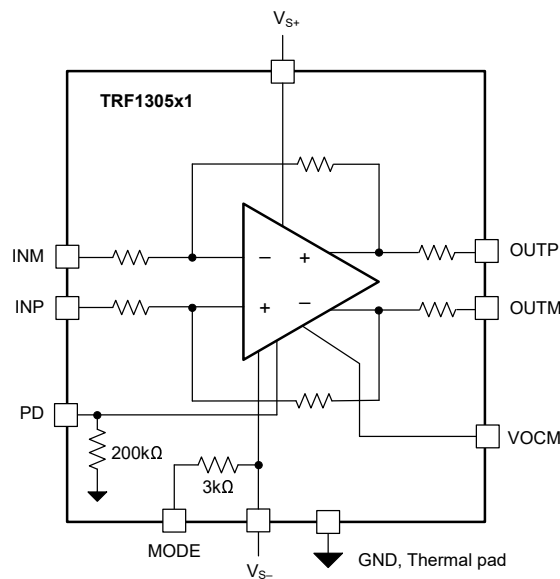
7.1 Overview

The TRF1305A1, TRF1305B1, and TRF1305C1 (TRF1305x1) devices are シングル チャネル, high-performance fully differential RF amplifiers optimized for very wideband signals from dc to > 7GHz. This device family is primarily designed to interface with high-speed and RF data converters that often require differential input (ADCs) and output (DACs) signaling. The TRF1305x1 can be dc or ac coupled, and configured as single-ended input and differential output (S2D) or differential input and differential output (D2D). The devices feature an output common-mode pin (VOCM) that allows the flexibility to set a desired common-mode output voltage. The amplifier allows the data converters to interface with a dc-coupled IQ demodulator or modulator if used in a direct conversion system. The TRF1305x1 family comes in three fixed power gain variants (15dB, 10dB, and 5dB), and has a closed-loop feedback-amplifier architecture.

The devices are powered using two-rail supplies with a typical differential voltage of 5V between the positive and negative supplies, and usable in split- or single-supply configurations. A power-down feature is also available that allows the amplifier to be powered down.

The output of the amplifiers is low impedance. Use appropriate external series termination or resistive pad to match to an arbitrary impedance.

7.2 Functional Block Diagram



7.3 Feature Description

The TRF1305x1 includes the following key features:

- Two-rail floating supply with supply-independent thermal pad
 - Connect the thermal pad to GND
 - RF signals and PD pin are referenced to GND
- Single-supply or split-supply operation
- Supports single-ended and differential input configurations
- Performance-optimized preset fixed-gain variants
- Output common-mode control
- MODE pin: V_{ICM} range extension closer to V_{S+} or V_{S-} modes
- Digital-logic-controllable power-down option

7.3.1 Fully Differential RF Amplifier

The TRF1305x1 is a voltage-feedback fully differential amplifier (FDA) with wide bandwidth. The amplifier is designed for a differential power gain of 15dB, 10dB, or 5dB depending on the device variant. This amplifier has excellent time-domain specifications with high slew rate, high input and output common-mode ranges, and fast transient settling time.

The output average voltage (common-mode) of the FDA device is controlled by a separate common-mode loop. The target output common-mode voltage is set by the VO_{CM} input pin.

7.3.2 Output Common-Mode Control

Figure 7-1 shows a functional diagram of the output common-mode control. Internally, the VO_{CM} pin potential is set by the LDO output voltage that is equal to $V_{S-} + 2.5V$ connected through a 2.5k Ω resistor.

Floating the VO_{CM} pin is allowed. The output common-mode voltage at the output pins, O_{UTP} and O_{UTM}, defaults to the LDO output voltage of $V_{S-} + 2.5V$ when VO_{CM} pin is floated. Floating the VO_{CM} pin results in a V_{OCM} voltage equal to midsupply when $V_S = 5V$. If the VO_{CM} pin is driven, then drive the pin from a low-impedance source. Limit the value of R_{OCM} to less than 25 Ω for accurate reflection of the forced V_{OCM} voltage at the device outputs.

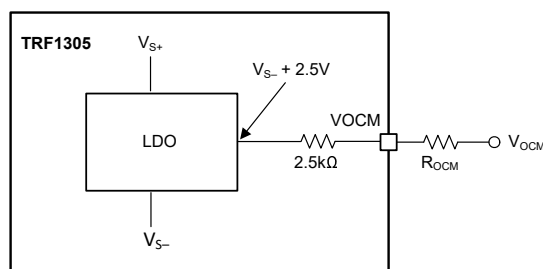


Figure 7-1. Output Common-Mode Control

7.3.3 Internal Resistor Configuration

Figure 7-2 shows the internal resistor configurations of TRF1305x1. Table 7-1 provides the values of these resistors for different gain variants.

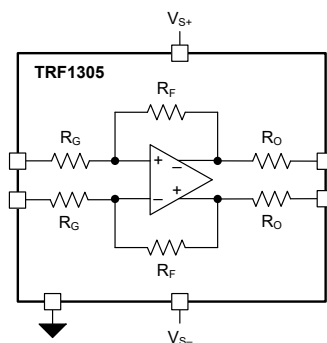


Figure 7-2. TRF1305x1 Internal Resistor Configuration

Table 7-1. Resistor Values

DEVICE NAME	GAIN (dB)	R _G (Ω)	R _F (Ω)	R _O (Ω)
TRF1305A1	15	6.25	258	4
TRF1305B1	10	12.5	161	4
TRF1305C1	5	17	97	4

7.4 Device Functional Modes

7.4.1 MODE Pin

The TRF1305x1 have additional useful features that can be configured using the MODE pin. To select the device mode, either connect a $\pm 2\%$ maximum tolerance pullup resistor between the MODE pin and V_{S+} , or force a voltage on the MODE pin. Internally, the MODE pin is referenced to V_{S-} through a 3k Ω resistor (see [セクション 7.2](#)).

[表 7-2](#) provides the value of the pullup resistor for each mode, the expected voltage, V_{MODE} , at the MODE pin when the pullup resistor is used or the necessary V_{MODE} voltage to set the device mode, and the mode configurations. The V_{MODE} voltage thresholds are approximately midway between the adjacent modes typical V_{MODE} voltage. If the mode functionality is used, use a decoupling capacitor on the MODE pin.

表 7-2. MODE Pin Configuration

MODE NUMBER	PULLUP RESISTOR TO V_{S+} ($\pm 2\%$ MAXIMUM TOLERANCE)	MODE PIN VOLTAGE, V_{MODE} (V)	V_{ICM} RANGE EXTENSION ⁽¹⁾
0	OPEN	V_{S-}	Default V_{ICM} range
1	28.7k Ω	$V_{S-} + 0.5V$	Low side, extends V_{ICM} range closer to V_{S-}
2	12.7k Ω	$V_{S-} + 1V$	High side, extends V_{ICM} range closer to V_{S+}
N/A	Do not use pullup resistor < 10k Ω or do not set $V_{MODE} > V_{S-} + 1.15V$		

(1) Only available in D2D configuration.

To switch the mode without turning the supplies off, use a switch or MUX connected between the pullup resistor options and V_{S+} , or force a mode-appropriate V_{MODE} voltage. However, powering down the device using the [power-down feature](#) between mode changes is preferred. The low-side and high-side V_{ICM} range extension modes source and sink currents, respectively (see also [セクション 7.4.1.1](#)). Ensure that the external circuitry is ready to sink or source these currents before the device is put in the active mode from the powered-down state.

7.4.1.1 Input Common-Mode Extension

The TRF1305x1 supports a V_{ICM} voltage closer to either V_{S+} or V_{S-} voltage than the default specified input common-mode range in the *Electrical Characteristics*, when configured in one of the V_{ICM} extension modes. The V_{ICM} extension mode can only be used in D2D configuration.

When configured in the low-side V_{ICM} extension mode, TRF1305B1 supports a 450mV lower input common-mode voltage than the default option. For example, the lower limit of V_{ICM} voltage range extends from a default value of $V_{S-} + 1.5V$ to $V_{S-} + 1.05V$ for the TRF1305B1 variant, and the higher limit also shifts lower from a default value of $V_{S-} + 3.5V$ to $V_{S-} + 3.05V$. At the lowest V_{ICM} voltage, approximately 15mA current must be sunk by the external circuitry connected to the INP and INM pins.

When configured in the high-side V_{ICM} extension mode, TRF1305B1 supports a 450mV higher input common-mode voltage than the default option. For example, the higher limit of V_{ICM} voltage range extends from a default value of $V_{S-} + 3.5V$ to $V_{S-} + 3.95V$ for the TRF1305B1 variant, and the lower limit also shifts up from a default of $V_{S-} + 1.5V$ to $V_{S-} + 1.95V$. At the highest V_{ICM} voltage, approximately 15mA current must be sourced by the external circuitry connected to the INP and INM pins.

Either resistors connected to supplies or external current sources can be used to sink or source the currents flowing out or into to the INP and INM pins during the low-side or high-side V_{ICM} extension modes, respectively.

7.4.2 Power-Down Mode

The TRF1305x1 have two bias modes, active and power-down, that are controlled by the voltage on the PD pin. The PD pin is referenced to GND through a 200k Ω resistor; see also [セクション 7.2](#). If the $V_{S+} \geq 3.3V$ configuration is used, ensure that the PD voltage does not exceed the *Absolute Maximum Ratings* in case the high PD voltage is derived from V_{S+} .

Both 1.8V and 3.3V digital logic is supported for power-down control.

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Input and Output Interface Considerations

8.1.1.1 Single-Ended Input

In the single-ended input configuration, one of the amplifier input pins is driven from a source while the other input is terminated with an external resistor. [図 8-1](#) shows an ac-coupled, single-ended input configuration driven from and matched to a 50Ω source. [図 8-1](#) shows how the non-driven INM pin is terminated with a 50Ω external resistor to match to a source with the same 50Ω impedance at the INP pin. The configuration shown in [図 8-1](#) works for all gain versions of TRF1305x1.

To configure the design in [図 8-1](#) for single-ended, dc-coupled input, replace the ac-coupling capacitors with shorts, and externally bias both INP and INM pins to a voltage close to the mid-supply or within the common-mode limits of the amplifier.

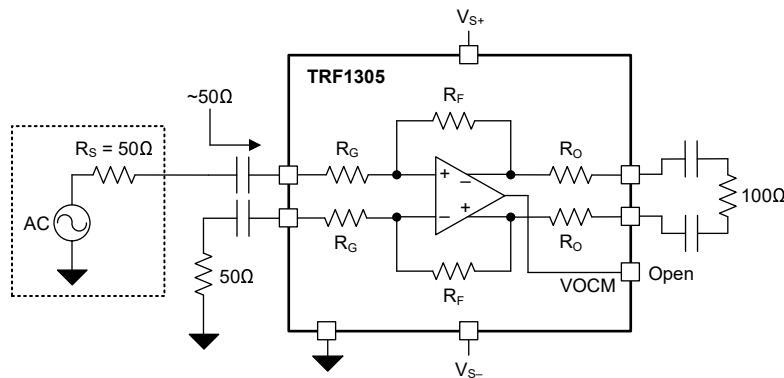


図 8-1. AC-Coupled, Single-Ended Input Matched to a 50Ω Source

8.1.1.2 Differential Input

[図 8-2](#) shows how a simple network consisting of three resistors is used to match the differential input to a 100Ω differential source. Though the 1kΩ shunt resistor, R_{IN_SH} , does not have any impact at dc to low frequencies, the resistor is necessary to get the full wideband performance from TRF1305x1. [図 8-3](#) shows the configuration for ac-coupled differential input designs. The resistors values shown in [図 8-2](#) and [図 8-3](#) work for all gain versions of the TRF1305x1 for an 100Ω input match to a 100Ω differential source.

Use small foot-print resistors (0201 preferred), and RF quality for high-frequency matching.

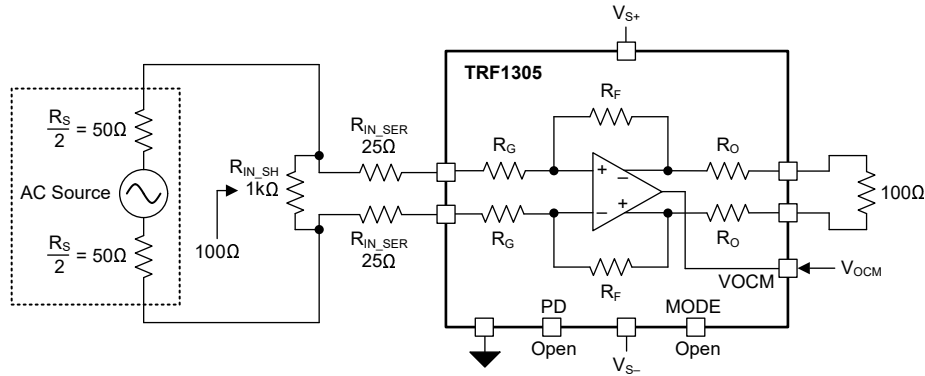


Figure 8-2. DC-Coupled Differential Input Matched to a 100Ω Differential Source

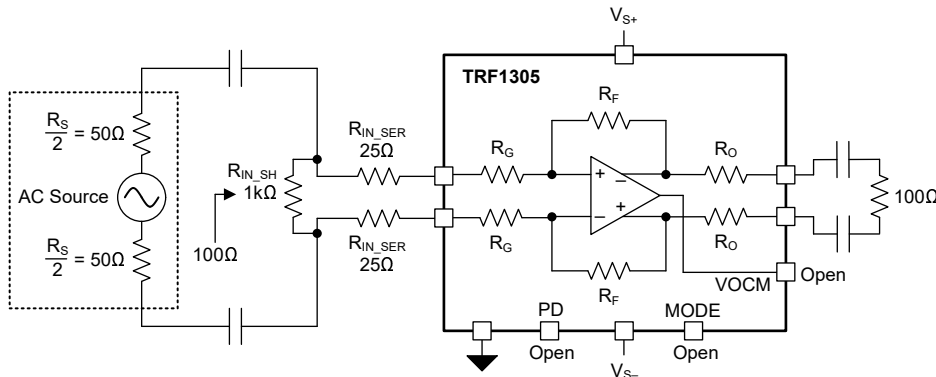


Figure 8-3. AC-Coupled Differential Input Matched to a 100Ω Differential Source

8.1.1.3 DC Coupling Considerations

The TRF1305x1 accepts a wide range of input dc common-mode (CM) voltages. Take into consideration the dc current loading of the source when the TRF1305x1 is dc-coupled at the input. Figure 8-4 shows that when the input CM voltage, V_{ICM} , is different than the output CM voltage, V_{OCM} , a net dc current flow from or to the source occurs. Equation 1 shows the relationship that the source or sink current, I_{CM} , has with the input and output CM voltages:

$$I_{CM} = \frac{(V_{OCM} - V_{ICM})}{(R_F + R_G)} \quad (1)$$

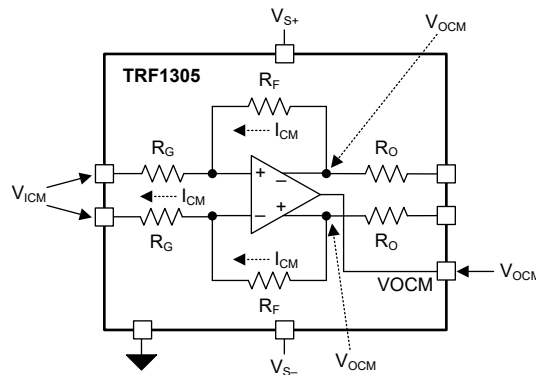


Figure 8-4. Net DC Current Flow When Input and Output Common-Mode Voltages are not Equal

8.1.2 Gain Adjustment With External Resistors in a Differential Input Configuration

The TRF1305x1 allow minor gain adjustments by configuring the input external resistive network that is part of the differential input configuration. [Figure 8-5](#) shows the external input network that comprises of a shunt resistor, R_{IN_SH} , and two series input resistors, R_{IN_SER} , connected to the input pins of the amplifier.

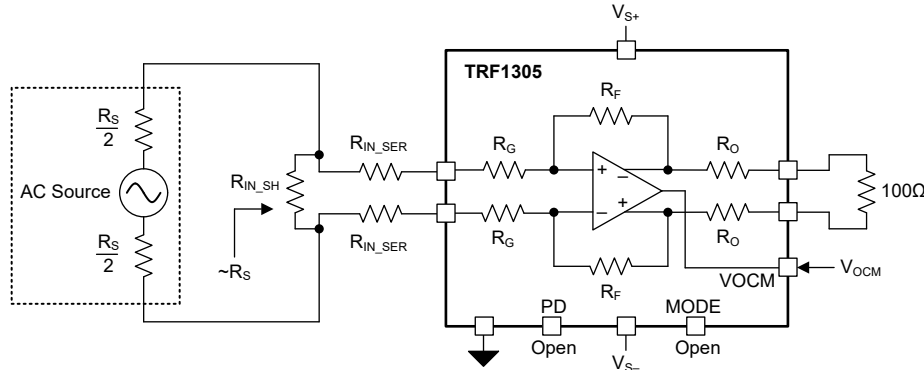


Figure 8-5. Gain Adjustment With External Resistor Network

[Table 8-1](#) provides resistor configurations for a 100Ω differential source impedance.

Table 8-1. Resistor Table for $R_S = 100\Omega$

TRF1305B1		
POWER GAIN (dB)	R_{IN_SH} (Ω)	R_{IN_SER} (Ω)
10	1000	25
9	408	30
8	267	35
7	204	41
6	169	47
5	146	54

Use external resistive attenuation network only for small gain adjustments because there is a dB-to-dB noise figure degradation with the resistive attenuators. Use an amplifier version that requires minimal attenuation for achieving the overall gain.

8.2 Typical Application

8.2.1 TRF1305x1 as ADC Driver in a Zero-IF Receiver

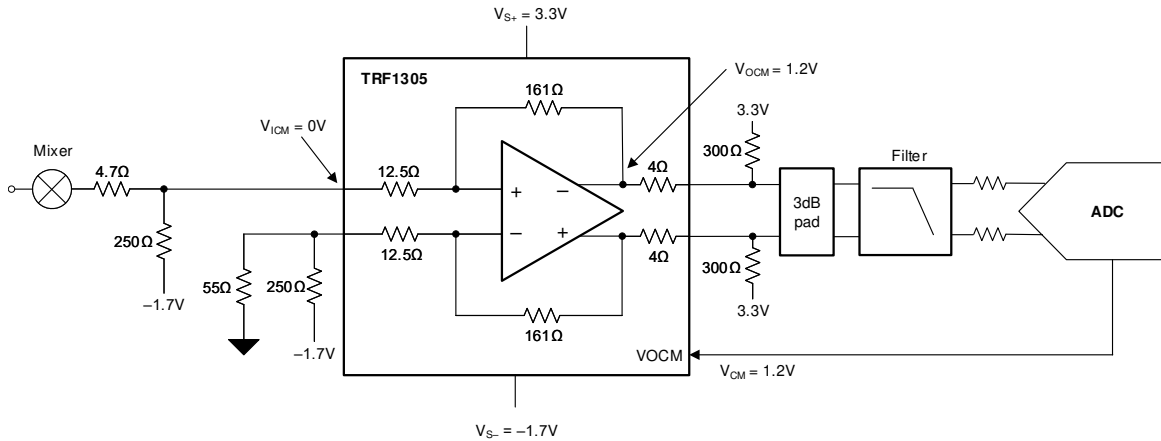


図 8-6. TRF1305x1 as ADC Driver in a Zero-IF Receiver

Consider a zero-IF (direct down conversion) application with an IQ demodulator interfaced to a pair of ADCs. In this case, the TRF1305x1 is used as an interface amplifier between the demodulator and the ADCs. The dc common-mode of the demodulator output and ADC input are different. The TRF1305x1 dc couples the demodulator to ADC without degrading the signal integrity of the signal chain.

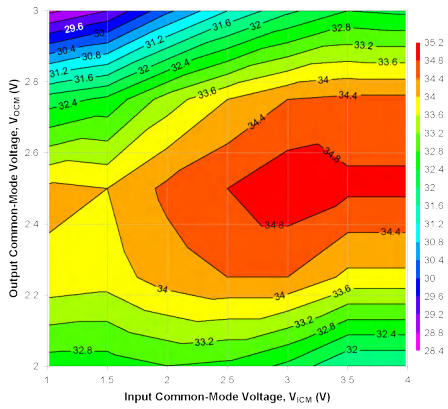
8.2.1.1 Design Requirements

The primary design requirement for an IQ demodulator application is to interface a pair of passive mixers with an RF ADC. The mixers have a 0-V common-mode voltage. The ADC requires an input common-mode voltage of 1.2V with full-scale swing of 1.35V_{PP}. Choose the power supplies, and design the input/output network for the TRF1305x1 as the ADC driver amplifier, to perform the dc level shifting and amplification function.

8.2.1.2 Detailed Design Procedure

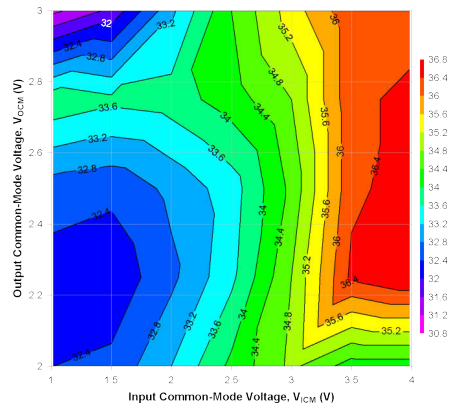
The first step is to choose the TRF1305x1 supplies. Ensure that the midsupply voltage, $V_{MIDSUPPLY}$, is between the ADC common-mode (CM) voltage and the mixer CM voltage. $V_{MIDSUPPLY}$ is typically positioned closer to the ADC CM because the output CM range of the amplifier is less than the input CM range. Ensure that the dc of the signal at the input and output of the amplifier are within the valid operating common-mode voltage range. Use the MODE pin for cases where an extended range of the input CM is required.

8.2.1.3 Application Curves



$f = 2\text{GHz}$, $P_{O}/\text{tone} = 1\text{dBm}$, 2MHz tone spacing

8-8. OIP3 Across Input and Output Common-Mode Voltage



$f = 2\text{GHz}$, $P_{O}/\text{tone} = -5\text{dBm}$, 2MHz tone spacing

8-9. OIP3 Across Input and Output Common-Mode Voltage

8.3 Power Supply Recommendations

8.3.1 Supply Voltages

For the TRF1305x1, the typical differential supply between VS+ and VS– is 5V. The VS+ and VS– supply pins can be floated with respect to ground within the specified range listed in the *Absolute Maximum Ratings* and *Recommended Operating Conditions*.

8.3.2 Single-Supply Operation

The VS– pin is connected to ground in the single-supply configuration. Single-supply operation is most convenient in ac-coupled configurations because the dc common-mode voltages of the source at the inputs and the driven circuit at the outputs are inherently decoupled.

8.3.3 Split-Supply Operation

In split-supply configuration, choose the VS+ and VS– voltages to be within the ranges specified in the *Absolute Maximum Ratings* and *Recommended Operating Conditions*. The TRF1305x1 allows choosing negative voltages for the VS– supply, thereby allowing the flexibility to choose input and output common-mode voltages according to the input network and output network requirements.

8.3.4 Supply Decoupling

The VS+ and VS– supply pins are decoupled individually to ground using external capacitors. Place the decoupling capacitors close to the device supply pins.

8.4 Layout

8.4.1 Layout Guidelines

The TRF1305x1 devices are wideband closed-loop feedback amplifiers. When designing with wideband RF amplifiers that have high gain, take certain board layout precautions to maintain stability and optimized performance. Use a multilayer board to maintain signal integrity, power integrity, and thermal performance.

Route the RF input and output lines as grounded coplanar waveguide (GCPW) lines. Ground pins are the reference for the RF signals. Ensure that the second layer of the PCB has a continuous ground layer without any ground cutouts in the vicinity of the amplifier. To minimize phase imbalance, match the length of the output differential lines of both channels. Length matching the input traces is also important, especially if the input configuration is differential. Use small-footprint, passive components wherever possible.

For good heat dissipation, connect the device thermal pad to the board ground planes using thermal vias under the device. For improved heat dissipation, connect the device thermal pad to the top layer ground plane of the board.

8.4.1.1 Thermal Considerations

The TRF1305x1 are packaged in a WQFN-FCRLF package that has excellent thermal properties. Connect the thermal pads underneath the devices to the thermally dissipative ground plane on the board. For good thermal design, use thermal vias to connect the thermal pad plane on the top layer of the PCB to the ground planes in the inner layers.

8.4.2 Layout Example

Figure 8-10 shows an example layout for TRF1305x1 with a differential input configuration. Key areas are highlighted in the figure.

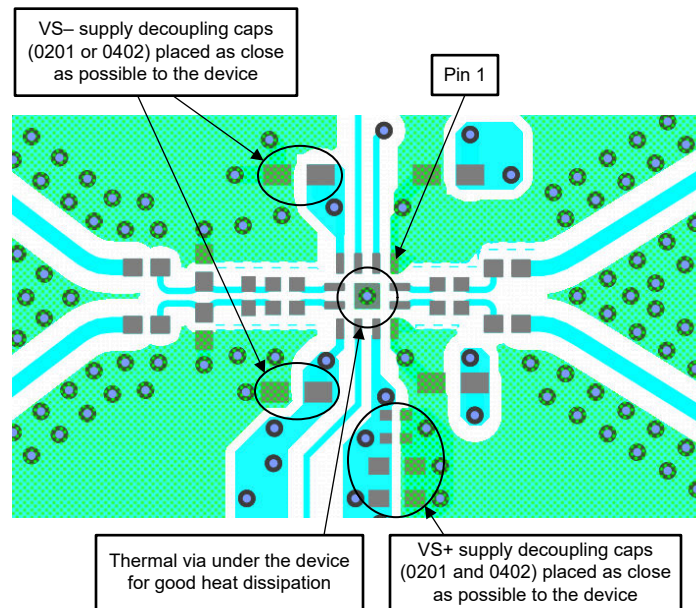


Figure 8-10. Layout Example: TRF1305x1 With Differential Input

The TRF1305x1 can be evaluated using EVM boards that can be ordered from the [TRF1305B1](#) product folder. For more information about the evaluation board construction and test setup, see the [TRF1305x1 EVM User's Guide](#).

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [TRF1305x1-D2D EVM User's Guide](#)

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.6 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2024) to Revision A (December 2024) Page

- | | |
|---|---|
| • TRF1305B1 のステータスを「事前情報」から「量産データ」(アクティブ)に変更..... | 1 |
|---|---|

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTRF1305B1RPVR	ACTIVE	WQFN-HR	RPV	12	3000	TBD	Call TI	Call TI	-40 to 125		Samples
TRF1305B1RPVR	ACTIVE	WQFN-HR	RPV	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	135B	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1305B1RPVR	WQFN-HR	RPV	12	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

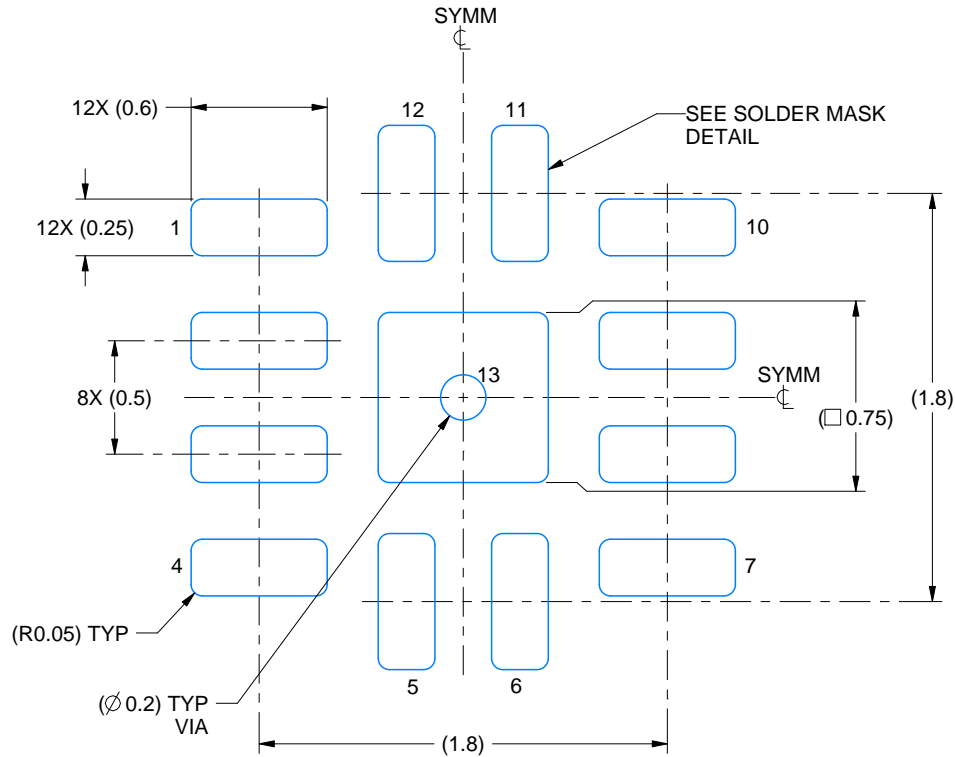
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1305B1RPVR	WQFN-HR	RPV	12	3000	210.0	185.0	35.0

EXAMPLE BOARD LAYOUT

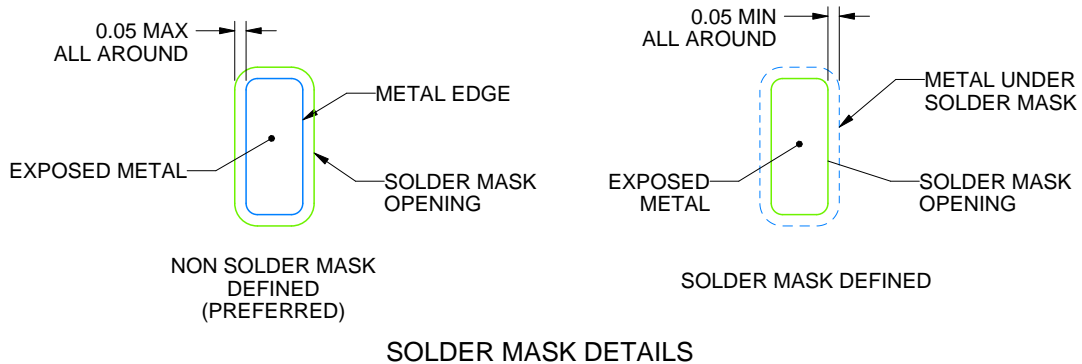
RPV0012A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4225258/B 04/2020

NOTES: (continued)

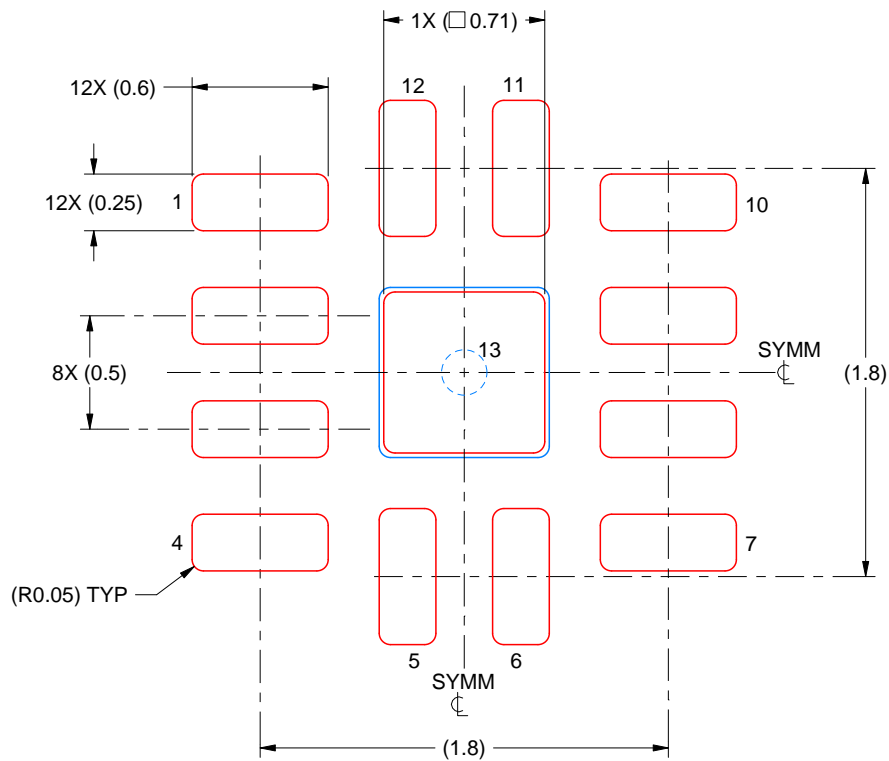
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RPV0012A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

EXPOSED PAD 13
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225258/B 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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