

TRF1213 DC 近傍から 14GHz、3dB 帯域幅、RF シングルエンド/差動アンプ

1 特長

- シングルエンド入力、差動出力
- RF ADC を駆動する優れた性能
- 14dB の固定ゲイン
- 帯域幅 (3dB): 14GHz 超
- ゲイン平坦性:
 - +1.2dB (12GHz)
 - -1dB (14.8GHz)
- OP1dB:
 - 4GHz: 14.4dBm
 - 10GHz: 14.6dBm
- OIP3:
 - 4GHz: 34dBm
 - 10GHz: 31dBm
- NF:
 - 4GHz: 8.6 dB
 - 10GHz: 11.8 dB
- ゲイン不平衡および位相不平衡: $\pm 0.3\text{dB}$ および $\pm 3^\circ$
- パワーダウン機能
- 5V 単一電源動作
- 動作電流: 174mA

2 アプリケーション

- RF サンプリングまたは GSPS ADC ドライバ
- 航空宇宙および防衛
- レーダー追跡フロントエンド
- フェーズドアレイレーダー
- 軍用無線
- 試験および測定機器
- 高速デジタイザ
- ベクトル信号トランシーバ (VST)
- 4G/5G ワイヤレス BTS

3 概要

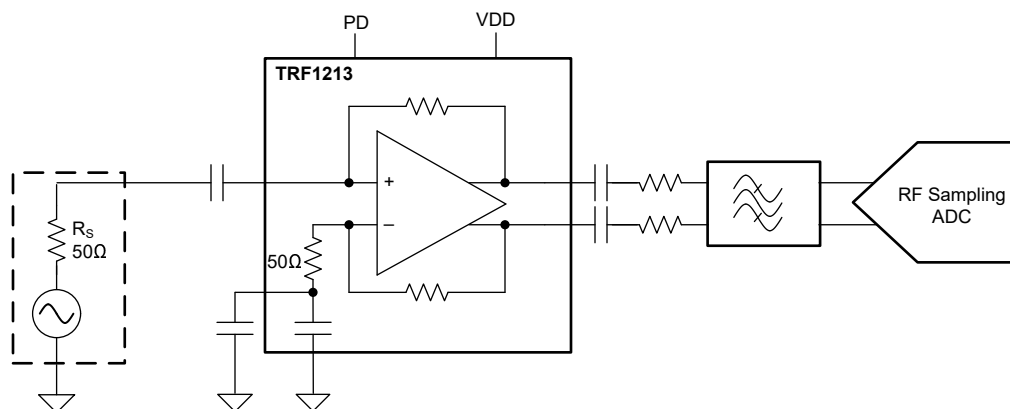
TRF1213 は、非常に高性能な無線周波数 (RF) アンプで、RF アプリケーション用に最適化されています。このデバイスは、高性能 AFE7950 または ADC12DJ5200RF などの RF サンプリング A/D コンバータ (ADC) を駆動する際に、シングルエンドから差動形式への変換を必要とする AC 結合アプリケーションに最適です。このデバイスは、広帯域ゲインブロックと広帯域パッシブバランの機能を組み合わせたものです。オンチップのマッチング部品により、プリント基板 (PCB) の実装が簡素化され、使用可能な帯域幅全体にわたって最高の性能を実現できます。このデバイスは、TI の先進的な相補型 BiCMOS プロセスで製造され、省スペースの WQFN-FCRLF パッケージで供給されます。

TRF1213 はシングルレール電源で動作し、消費有効電流は約 174mA です。またパワーダウン機能を利用して、消費電力を削減することも可能です。

製品情報

| 部品番号 | パッケージ (1) | パッケージ サイズ (2) |
|---------|----------------------|---------------|
| TRF1213 | RPV (WQFN-FCRLF, 12) | 2mm × 2mm |

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



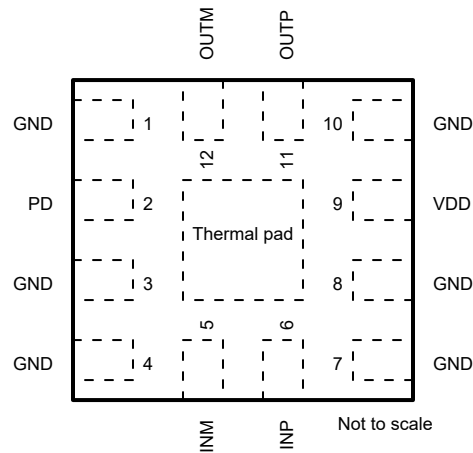
TRF1213 RF サンプリング ADC の駆動



Table of Contents

| | | | |
|--|-----------|---|-----------|
| 1 特長 | 1 | 7 Application and Implementation | 16 |
| 2 アプリケーション | 1 | 7.1 Application Information..... | 16 |
| 3 概要 | 1 | 7.2 Typical Applications..... | 18 |
| 4 Pin Configuration and Functions | 3 | 7.3 Power Supply Recommendations..... | 20 |
| 5 Specifications | 4 | 7.4 Layout..... | 20 |
| 5.1 Absolute Maximum Ratings..... | 4 | 8 Device and Documentation Support | 21 |
| 5.2 ESD Ratings..... | 4 | 8.1 Device Support..... | 21 |
| 5.3 Recommended Operating Conditions..... | 4 | 8.2 Documentation Support | 21 |
| 5.4 Thermal Information..... | 4 | 8.3 ドキュメントの更新通知を受け取る方法..... | 21 |
| 5.5 Electrical Characteristics..... | 5 | 8.4 サポート・リソース..... | 21 |
| 5.6 Typical Characteristics..... | 7 | 8.5 Trademarks..... | 21 |
| 6 Detailed Description | 14 | 8.6 静電気放電に関する注意事項..... | 21 |
| 6.1 Overview..... | 14 | 8.7 用語集..... | 21 |
| 6.2 Functional Block Diagram..... | 14 | 9 Revision History | 21 |
| 6.3 Feature Description..... | 15 | 10 Mechanical, Packaging, and Orderable | |
| 6.4 Device Functional Modes..... | 15 | Information | 21 |

4 Pin Configuration and Functions



**図 4-1. RPV Package,
12-Pin WQFN-FCRLF
(Top View)**

表 4-1. Pin Functions

| PIN | | TYPE | DESCRIPTION |
|-------------|-------------------|--------|--|
| NAME | NO. | | |
| GND | 1, 3, 4, 7, 8, 10 | Ground | Ground |
| INM | 5 | Input | External ac coupling capacitor on negative input. Typical value 100nF. |
| INP | 6 | Input | Single ended input |
| OUTM | 12 | Output | Differential signal output, negative |
| OUTP | 11 | Output | Differential signal output, positive |
| PD | 2 | Input | Power-down signal. Supports 1.8V and 3.3V Logic. 0 = Chip enabled 1 = Power down |
| VDD | 9 | Power | 5V supply |
| Thermal pad | Pad | — | Thermal pad. Connect to ground on board. |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|------------------------|------|---------------------|------|
| V _{DD} | Supply voltage | −0.3 | 5.5 | V |
| P _{INP} | INP input pin power | | 20 ⁽²⁾ | dBm |
| V _{INM} | INM input pin voltage | −0.3 | 3.3 ⁽³⁾ | V |
| V _{PD} | Power-down pin voltage | −0.3 | 3.45 ⁽³⁾ | V |
| T _J | Junction temperature | | 150 | °C |
| T _{stg} | Storage temperature | −40 | 150 | °C |

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) When V_{DD} = 0V, maximum value is 0dBm.
- (3) When V_{DD} = 0V, maximum value is 0.3V.

5.2 ESD Ratings

| | | | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾ | ±1000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾ | ±250 | |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------|------------------------------|------|-----|------|------|
| V _{DD} | Supply voltage | 4.75 | 5 | 5.25 | V |
| T _A | Ambient free-air temperature | −40 | 25 | | °C |
| T _J | Junction temperature | | | 125 | °C |

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TRF1213 | | UNIT |
|-------------------------------|--|------------------|--|------|
| | | RPV (WQFN-FCRLF) | | |
| | | 12 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 66.7 | | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 35.3 | | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 31.1 | | °C/W |
| Ψ _{JT} | Junction-to-top characterization parameter | 0.6 | | °C/W |
| Ψ _{JB} | Junction-to-board characterization parameter | 31.1 | | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 10.7 | | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, 50Ω single-ended input, and 100Ω differential output (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------------------|--|---|------------|-----|------|-----|---------|
| AC PERFORMANCE | | | | | | | |
| Sds21 | Power gain | f = 0.5GHz | | | 13.8 | | dB |
| | | f = 2GHz | | | 14 | | |
| | | f = 4GHz | | | 14 | | |
| | | f = 8GHz | | | 13.8 | | |
| | | f = 10GHz | | | 14.5 | | |
| | | f = 12GHz | | | 15.2 | | |
| Sss11 | Input return loss | f = 10MHz to 12GHz | | | -12 | | dB |
| Ssd12 | Reverse isolation | f = 10GHz | | | -34 | | dB |
| I _{mb} _{GAIN} | Gain imbalance | f = 10MHz to 12GHz | | | ±0.3 | | dB |
| I _{mb} _{PHASE} | Phase imbalance | f = 10MHz to 12GHz | | | ±3 | | degrees |
| CMRR | Common-mode rejection ratio ⁽¹⁾ | f = 10GHz | | | -32 | | dB |
| HD2 | Second-order harmonic distortion | $P_O = 3\text{dBm}$ | f = 0.5GHz | | -72 | | dBc |
| | | | f = 2GHz | | -59 | | |
| | | | f = 4GHz | | -56 | | |
| | | | f = 6GHz | | -47 | | |
| HD3 | Third-order harmonic distortion | $P_O = 3\text{dBm}$ | f = 0.5GHz | | -76 | | dBc |
| | | | f = 2GHz | | -64 | | |
| | | | f = 4GHz | | -55 | | |
| IMD2 | Second-order intermodulation distortion | $P_O = -5\text{dBm}$ per tone, 10MHz spacing | f = 0.5GHz | | -72 | | dBc |
| | | | f = 2GHz | | -61 | | |
| | | | f = 4GHz | | -58 | | |
| | | | f = 8GHz | | -53 | | |
| | | | f = 10GHz | | -68 | | |
| IMD3 | Third-order intermodulation distortion | $P_O = -5\text{dBm}$ per tone, 10MHz spacing | f = 0.5GHz | | -92 | | dBc |
| | | | f = 2GHz | | -82 | | |
| | | | f = 4GHz | | -78 | | |
| | | | f = 8GHz | | -74 | | |
| | | | f = 10GHz | | -72 | | |
| OP1dB | Output 1dB compression point | f = 0.5GHz | | | 12.7 | | dBm |
| | | f = 2GHz | | | 13.3 | | |
| | | f = 4GHz | | | 14.4 | | |
| | | f = 8GHz | | | 15.2 | | |
| | | f = 10GHz | | | 14.6 | | |
| | | f = 12GHz | | | 14.8 | | |
| OIP2 | Output second-order intercept point | $P_O = -5\text{dBm}$ per tone, 10MHz spacing | f = 0.5GHz | | 67 | | dBm |
| | | | f = 2GHz | | 56 | | |
| | | | f = 4GHz | | 53 | | |
| | | | f = 8GHz | | 48 | | |
| | | | f = 10GHz | | 63 | | |
| | | | f = 12GHz | | 64 | | |

at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{V}$, 50Ω single-ended input, and 100Ω differential output (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|-------------------------------------|---|---------------------|------|-----|---------------|
| OIP3 | Output third-order intercept point | $P_O = -5\text{dBm}$ per tone, 10MHz spacing | $f = 0.5\text{GHz}$ | 41 | | dBm |
| | | | $f = 2\text{GHz}$ | 36 | | |
| | | | $f = 4\text{GHz}$ | 34 | | |
| | | | $f = 8\text{GHz}$ | 32 | | |
| | | | $f = 10\text{GHz}$ | 31 | | |
| | | | $f = 12\text{GHz}$ | 28.5 | | |
| NF | Noise figure | $f = 0.5\text{GHz}$ | | 7.9 | | dB |
| | | $f = 2\text{GHz}$ | | 8.2 | | |
| | | $f = 4\text{GHz}$ | | 8.6 | | |
| | | $f = 8\text{GHz}$ | | 10.8 | | |
| | | $f = 10\text{GHz}$ | | 11.8 | | |
| | | $f = 12\text{GHz}$ | | 12 | | |
| IMPEDANCE | | | | | | |
| Z_{O-DIFF} | Differential output impedance | $f = \text{dc}$ (internal to the device) | | 12 | | Ω |
| R_{INM} | Internal INM resistance | | | 50 | | Ω |
| C_{INM} | Internal INM capacitance | | | 12 | | pF |
| POWER SUPPLY | | | | | | |
| I_{QA} | Active current | Current on V_{DD} pin, PD = 0 | | 174 | | mA |
| I_{QPD} | Power-down quiescent current | Current on V_{DD} pin, PD = 1 | | 11 | | mA |
| ENABLE | | | | | | |
| V_{PDHIGH} | PD pin logic high | | 1.45 | | | V |
| V_{PDLLOW} | PD pin logic low | | | | 0.8 | V |
| I_{PDBIAS} | PD bias current (current on PD pin) | PD = high (1.8V logic) | | 40 | 100 | μA |
| | | PD = high (3.3V logic) | | 200 | 250 | |
| C_{PD} | PD pin capacitance | | | 2 | | pF |

(1) Calculated using the formula $(S21 - S31) / (S21 + S31)$. Port-1: INP, Port-2: OUTP, Port-3: OUTM.

5.6 Typical Characteristics

at $T_A = 25^\circ\text{C}$, temperature curves specify ambient temperature, $V_{DD} = 5\text{V}$, 50Ω single-ended input, and 100Ω differential output (unless otherwise noted)

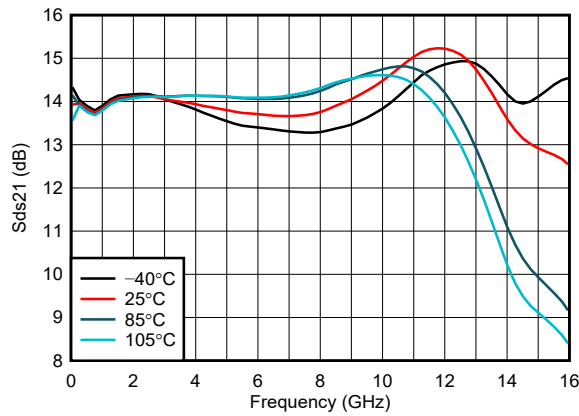


図 5-1. Power Gain Across Temperature

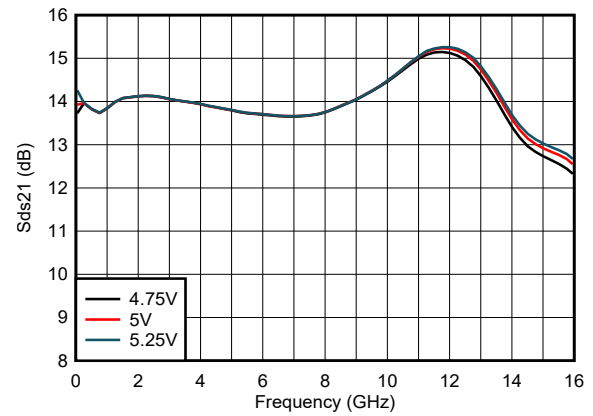


図 5-2. Power Gain Across V_{DD}

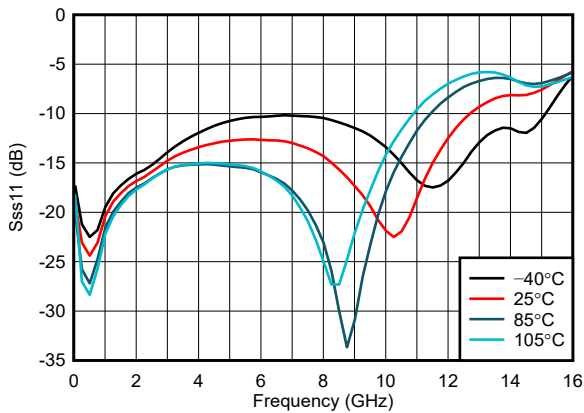


図 5-3. Return Loss Across Temperature

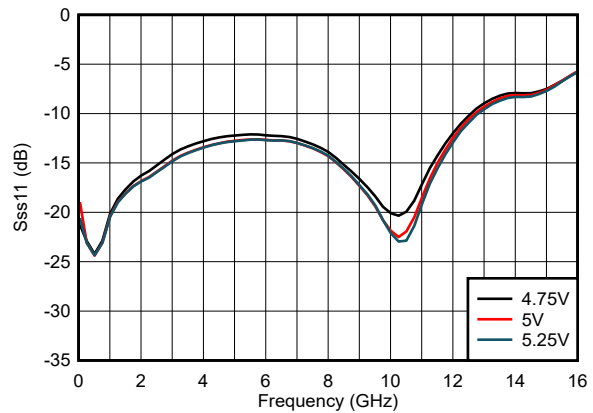


図 5-4. Return Loss Across V_{DD}

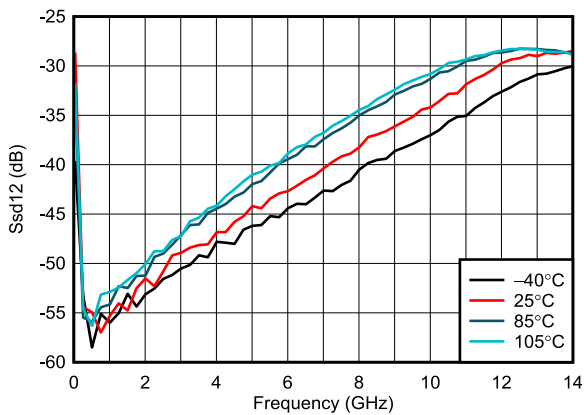


図 5-5. Reverse Isolation Across Temperature

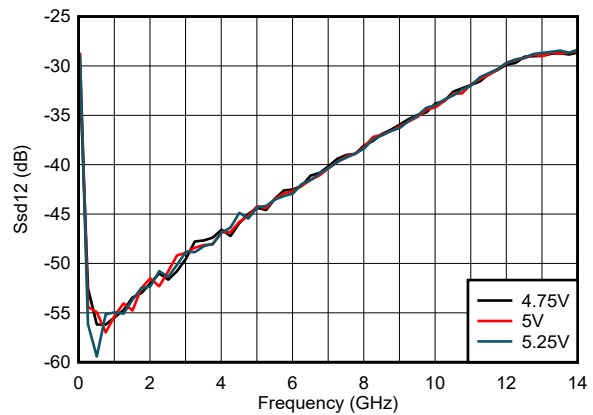
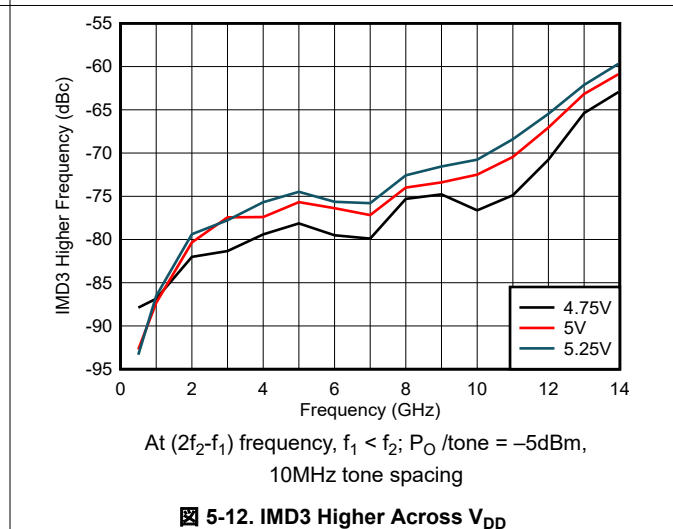
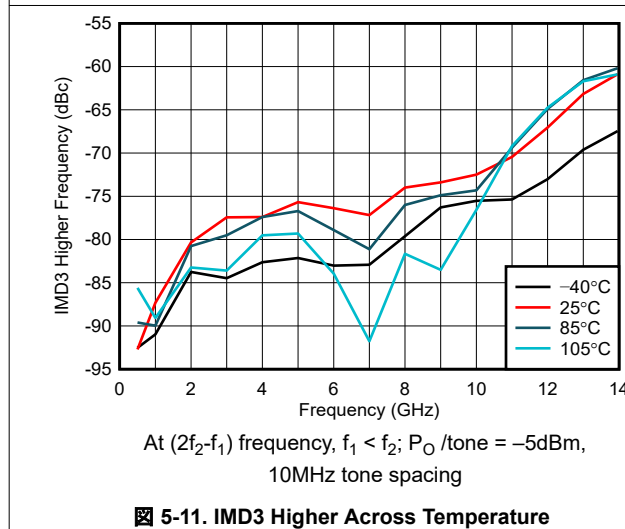
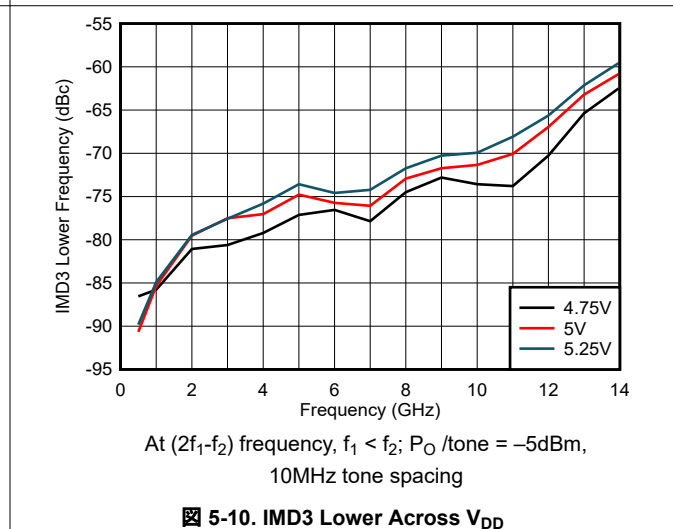
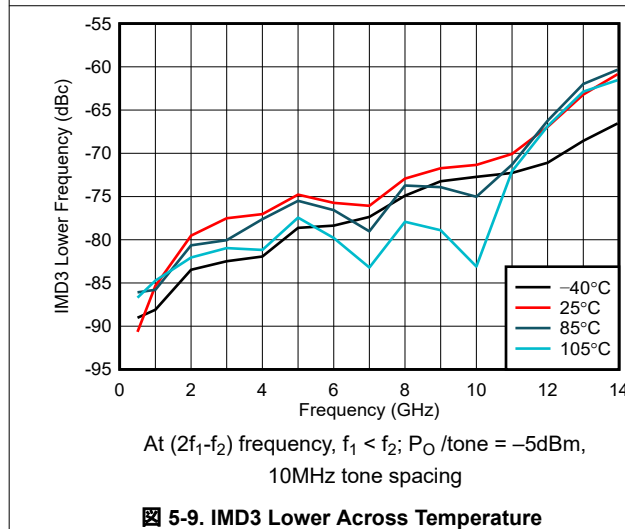
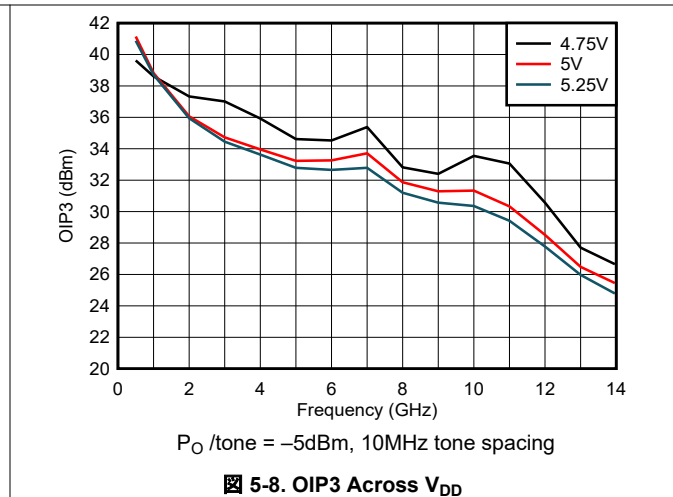
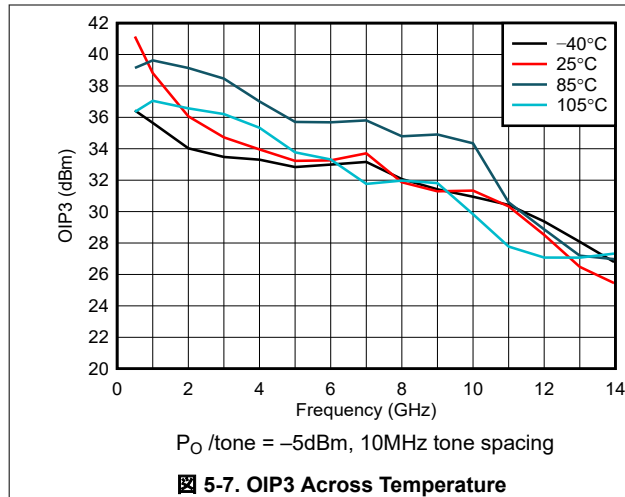


図 5-6. Reverse Isolation Across V_{DD}

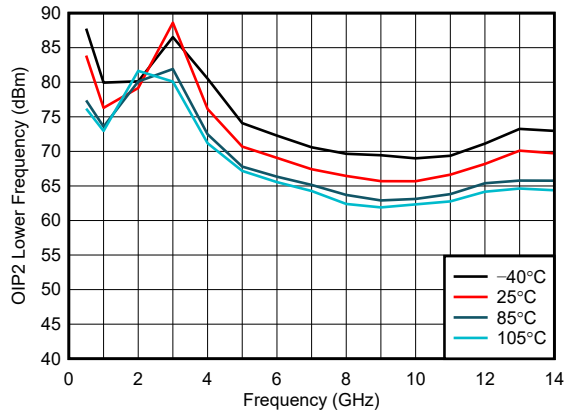
5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, temperature curves specify ambient temperature, $V_{DD} = 5\text{V}$, 50Ω single-ended input, and 100Ω differential output (unless otherwise noted)



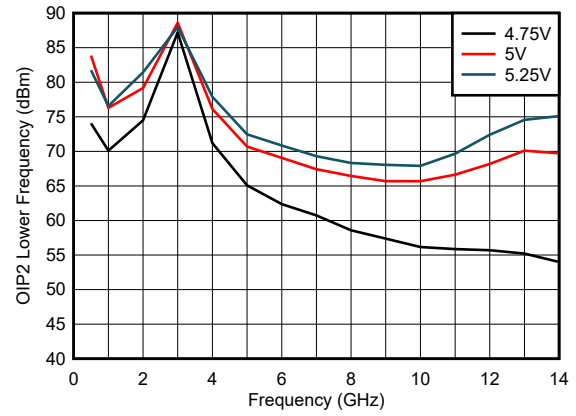
5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, temperature curves specify ambient temperature, $V_{DD} = 5\text{V}$, 50Ω single-ended input, and 100Ω differential output (unless otherwise noted)



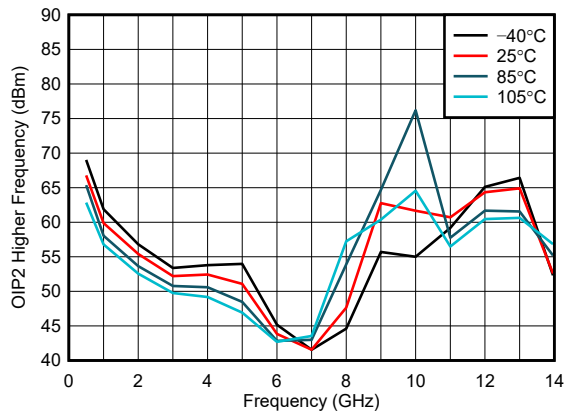
At (f_2-f_1) frequency, $f_2 > f_1$; $P_O / \text{tone} = -5\text{dBm}$,
10MHz tone spacing

5-13. OIP2 Lower Across Temperature



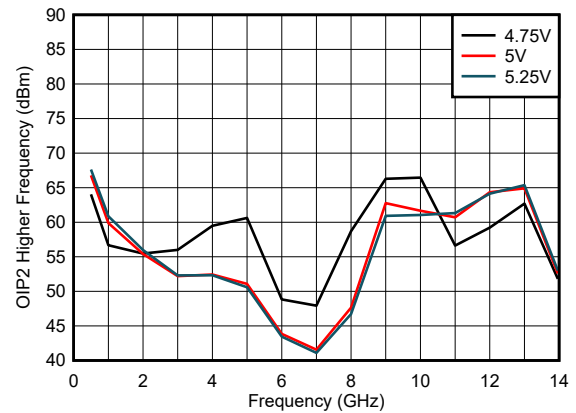
At (f_2-f_1) frequency, $f_2 > f_1$; $P_O / \text{tone} = -5\text{dBm}$,
10MHz tone spacing

5-14. OIP2 Lower Across V_{DD}



At (f_2+f_1) frequency, $f_2 > f_1$; $P_O / \text{tone} = -5\text{dBm}$,
10MHz tone spacing

5-15. OIP2 Higher Across Temperature

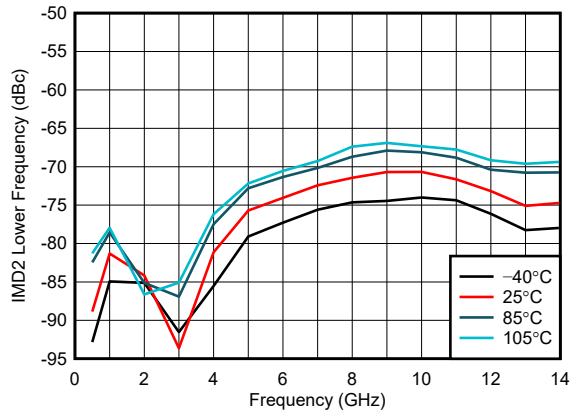


At (f_2+f_1) frequency, $f_2 > f_1$; $P_O / \text{tone} = -5\text{dBm}$,
10MHz tone spacing

5-16. OIP2 Higher Across V_{DD}

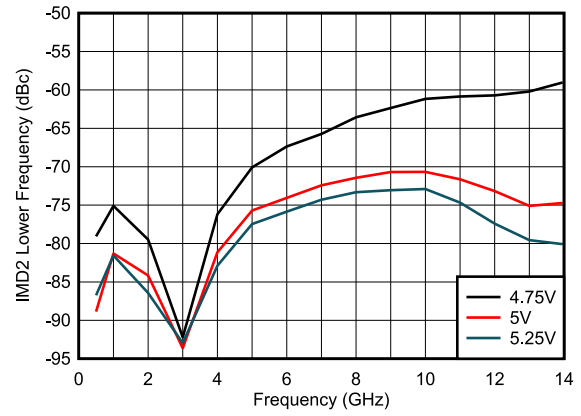
5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, temperature curves specify ambient temperature, $V_{DD} = 5\text{V}$, 50Ω single-ended input, and 100Ω differential output (unless otherwise noted)



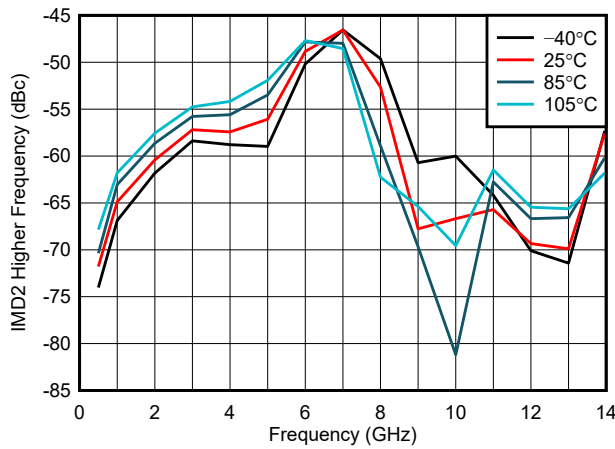
At (f_2-f_1) frequency, $f_2 > f_1$; $P_O / \text{tone} = -5\text{dBm}$,
 10MHz tone spacing

图 5-17. IMD2 Lower Across Temperature



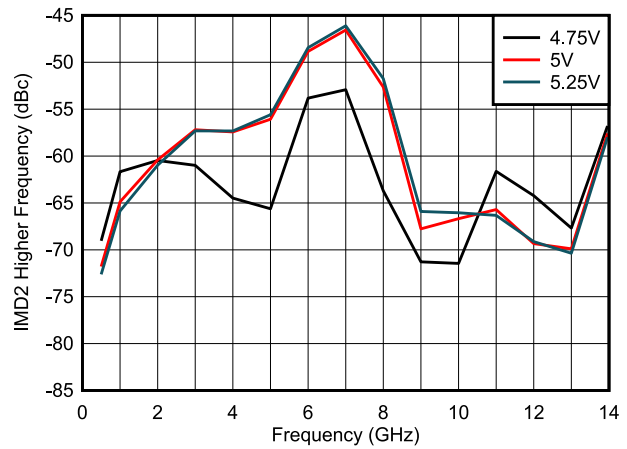
At (f_2-f_1) frequency, $f_2 > f_1$; $P_O / \text{tone} = -5\text{dBm}$,
 10MHz tone spacing

图 5-18. IMD2 Lower Across V_{DD}



At (f_2+f_1) frequency, $f_2 > f_1$; $P_O / \text{tone} = -5\text{dBm}$,
 10MHz tone spacing

图 5-19. IMD2 Higher Across Temperature



At (f_2+f_1) frequency, $f_2 > f_1$; $P_O / \text{tone} = -5\text{dBm}$,
 10MHz tone spacing

图 5-20. IMD2 Higher Across V_{DD}

5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, temperature curves specify ambient temperature, $V_{DD} = 5\text{V}$, 50Ω single-ended input, and 100Ω differential output (unless otherwise noted)

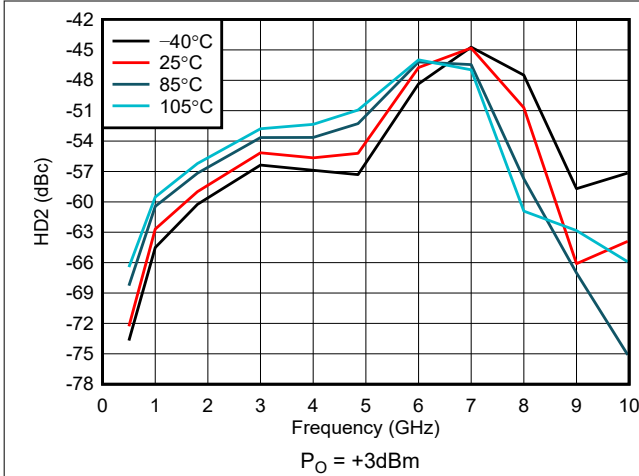


Figure 5-21. HD2 Across Temperature

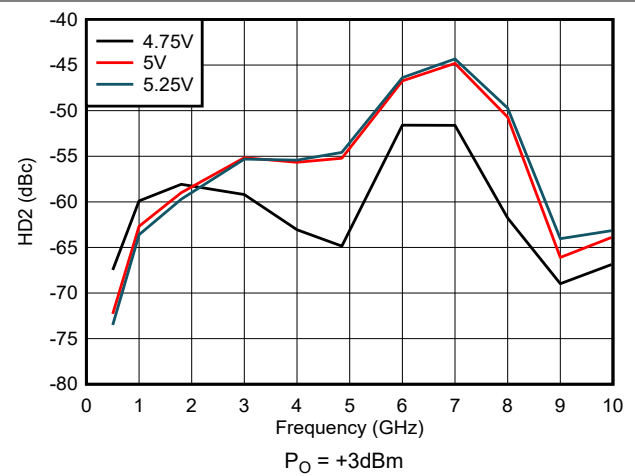


Figure 5-22. HD2 Across V_{DD}

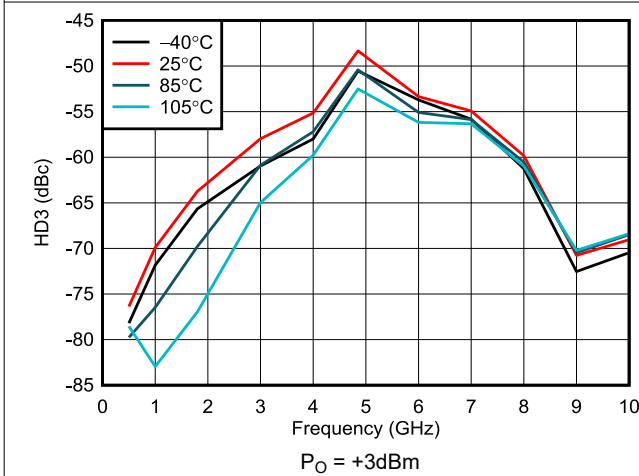


Figure 5-23. HD3 Across Temperature

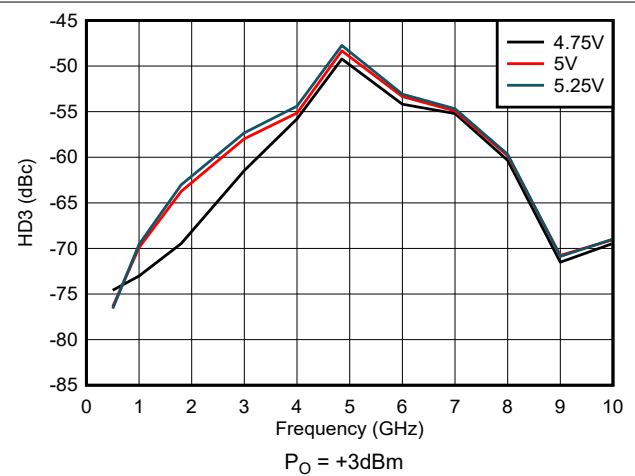


Figure 5-24. HD3 Across V_{DD}

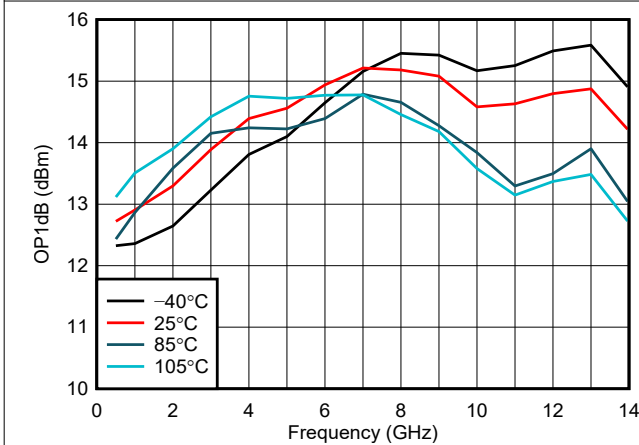


Figure 5-25. Output P1dB Across Temperature

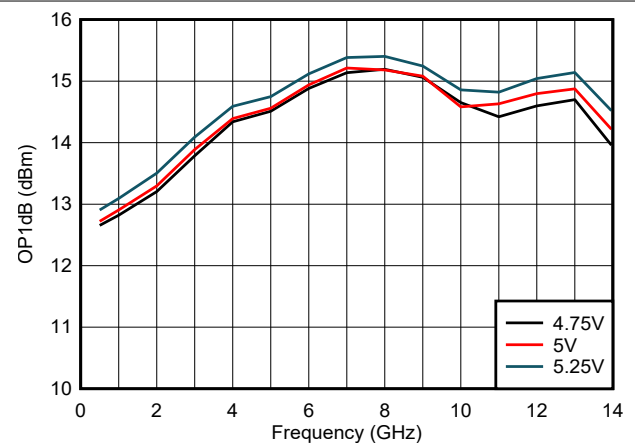
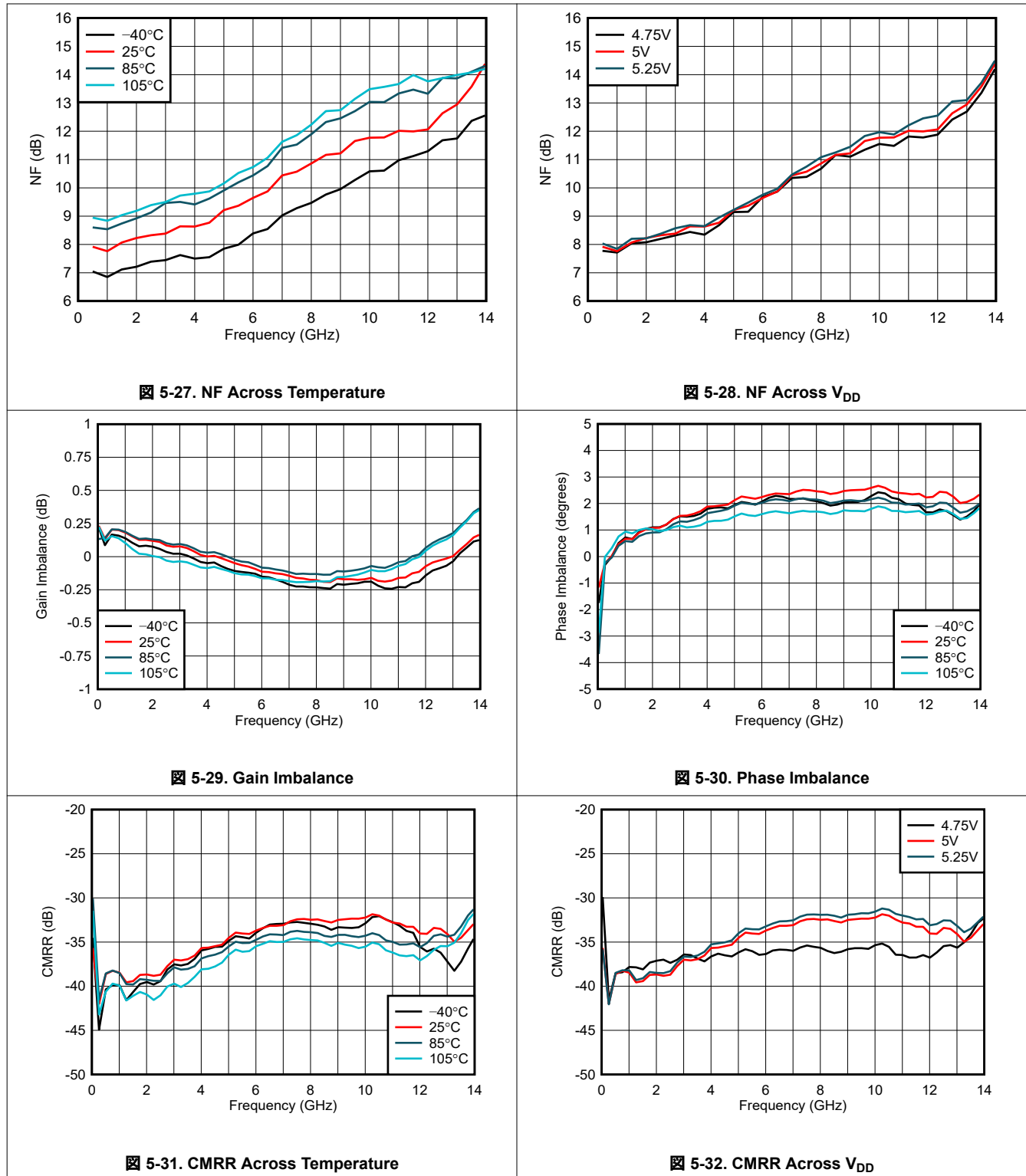


Figure 5-26. Output P1dB Across V_{DD}

5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, temperature curves specify ambient temperature, $V_{DD} = 5\text{V}$, 50Ω single-ended input, and 100Ω differential output (unless otherwise noted)



5.6 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, temperature curves specify ambient temperature, $V_{DD} = 5\text{V}$, 50Ω single-ended input, and 100Ω differential output (unless otherwise noted)

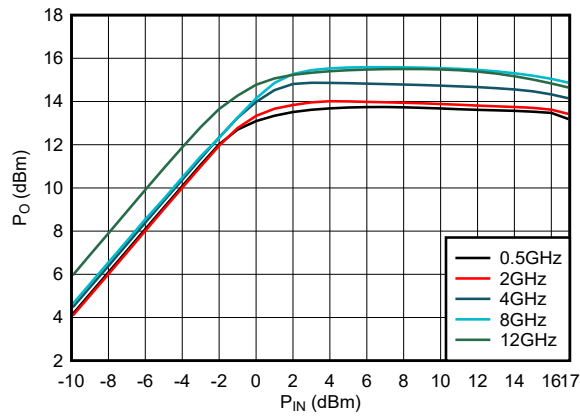


Figure 5-33. Output Power Across Input Power

6 Detailed Description

6.1 Overview

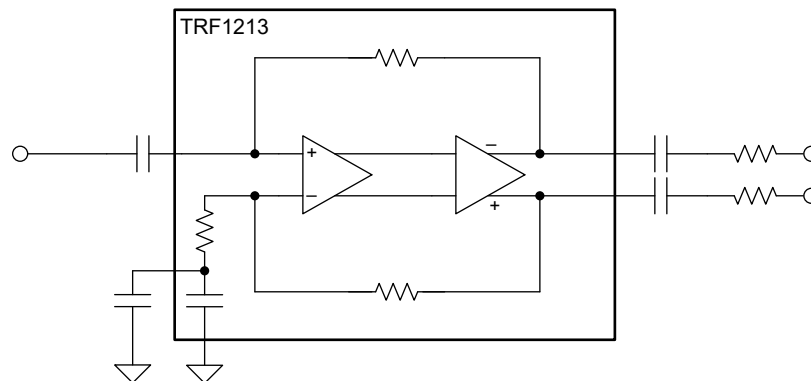
The TRF1213 is a very high-performance, single-ended-to-differential RF amplifier optimized for radio frequency (RF) and intermediate frequency (IF) applications with signal bandwidths up to 14GHz. The low frequency response is limited only by the ac-coupling capacitor on the PCB. The device has flat pass-band response up to 12GHz making this device an excellent choice for wideband applications, from HF to X band. The device is designed for ac-coupled applications that require a single-ended-to-differential conversion when driving an RF sampling analog-to-digital converter (ADC). The device has a two-stage architecture and provides approximately 14dB of gain when the single-ended input is driven by a 50Ω source.

This device does not require any pullup or pulldown components on the PCB, and thereby simplifies layout and provides the highest performance over the entire bandwidth.

The input and output are ac coupled. The TRF1213 is powered with 5V supply. A power-down feature is also available.

6.2 Functional Block Diagram

The following figure shows the functional block diagram of TRF1213. The device essentially has two stages with a voltage-feedback configuration.



6.3 Feature Description

The TRF1213 incorporates a voltage-feedback fully differential amplifier (FDA), with on-chip INM termination resistor and feedback resistors. The on-chip resistors reduce the effect of parasitics, and provide flat pass-band response over 12GHz of bandwidth. The input and output bias voltages are set internally simplifying applications by placing ac-coupling capacitors on the RF input and output pins.

The TRF1213 operates as a single-ended to differential amplifier with a fixed gain of 15.5dB.

The amplifier has non-linearity cancellation circuits that provide excellent linearity performance over a wide range of frequencies.

The input return loss is lower than 10dB over wide bandwidth eliminating the requirement for input matching network. The output of the amplifier has a low dc impedance. Therefore, if required, a series resistor or attenuator pad can be added at the output to provide output impedance.

The TRF1213 operates on a single 5V supply. Single-supply operation simplifies the board design.

6.3.1 Fully-Differential Amplifier

The TRF1213 incorporates a voltage-feedback fully differential amplifier (FDA), with on-chip INM termination resistor and feedback resistors. The on-chip resistors reduce the effect of parasitics, and provide flat pass-band response over 12GHz of bandwidth. The input and output bias voltages are set internally simplifying applications by placing ac-coupling capacitors on the RF input and output pins.

The TRF1213 operates as a single-ended to differential amplifier with a fixed gain of 15.5dB.

The amplifier has non-linearity cancellation circuits that provide excellent linearity performance over a wide range of frequencies.

The input return loss is lower than 10dB over wide bandwidth eliminating the requirement for input matching network. The output of the amplifier has a low dc impedance. Therefore, if required, a series resistor or attenuator pad can be added at the output to provide output impedance.

The TRF1213 operates on a single 5V supply. Single-supply operation simplifies the board design.

6.3.2 Single Supply Operation

The TRF1213 operates on a single 3.3-V supply. The input and output bias voltages are set internally. Therefore, ac-couple the signal path on the board at all four RF input and output pins. Single-supply operation simplifies the board design.

6.4 Device Functional Modes

The TRF1213 has two functional modes: active and power-down. These functional modes are controlled by the PD pin as described in the next section.

6.4.1 Power-Down Mode

The device features a power-down option. The PD pin is used to power down the amplifier. This pin supports both 1.8-V and 3.3-V digital logic, and is referenced to ground. A logic 1 turns the device off and places the device into a low-quiescent-current state.

When disabled, the signal path is still present through the internal circuits. Input signals applied to a disabled device still appear at the outputs at some lower level through this path, as is the case for any disabled feedback amplifier.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Driving a High-Speed ADC

A common application for the TRF1213 is driving a high-speed ADC that has a differential input (such as the ADC12DJ5200 or AFE7950). Conventionally, passive baluns are used to drive giga-samples-per-second (GSPS) ADCs as a result of the low availability of high-bandwidth, linear amplifiers. The TRF1213 is a single-ended to differential (S2D) RF amplifier that has excellent bandwidth flatness, gain, and phase imbalance comparable to or exceeding costly, passive RF baluns.

Figure 7-1 shows a typical interface circuit for ADC12DJ5200. Depending on the ADC and system requirement, this circuit can be simplified or more complex.

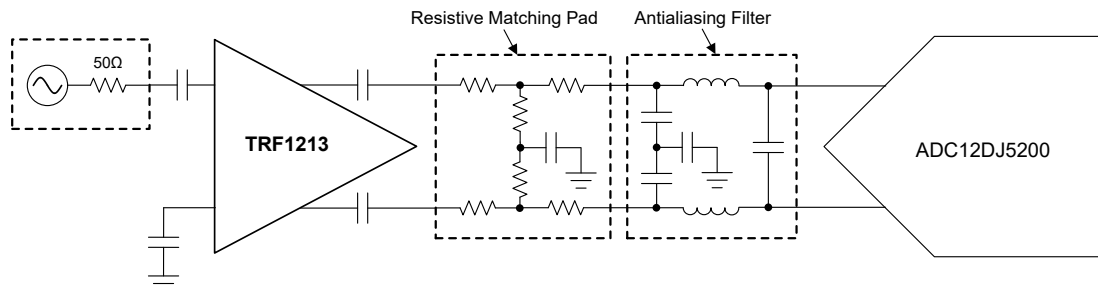
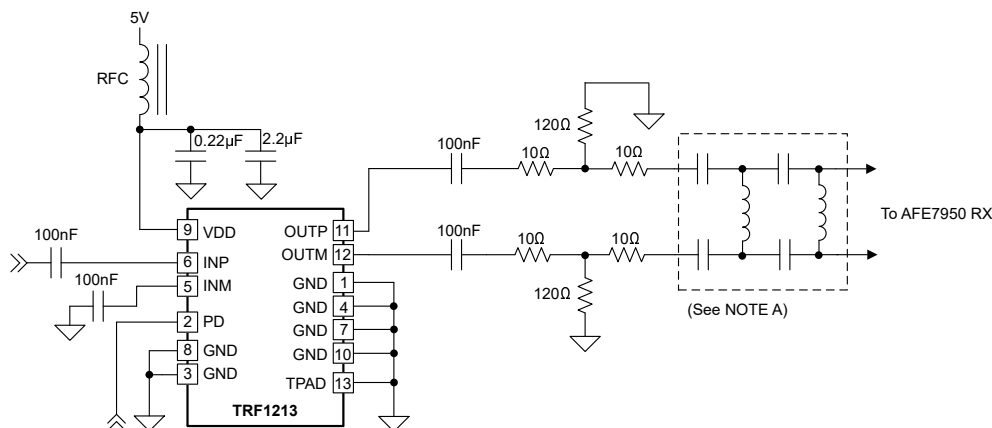


Figure 7-1. Interfacing With the ADC12DJ5200RF

Figure 7-1 shows two sections of the circuit between the driver amp and the ADC: namely, the matching pad (or attenuator pad) and the antialiasing filter. Use small-form-factor, RF-quality, passive components for these circuits. The output swing of the TRF1213 is designed to drive these ADCs to full-scale, while at the same time not overdrive the ADC. This functionality avoids the need for any voltage limiting device at the ADC.

Figure 7-2 shows a typical interface circuit for the AFE7950, where the TRF1213 is the S2D amplifier.



A. AFE matching network: component type (L or C) and values depend on the channel (A, B, C, D, FB1, FB2) and frequency band.

Figure 7-2. Interfacing With the AFE7950 RX

7.1.2 Calculating Output Voltage Swing

This section gives a quick reference of the output voltage swings for different input power levels. In this example, the output is terminated with a 100Ω differential load and a power gain of 14dB is assumed.

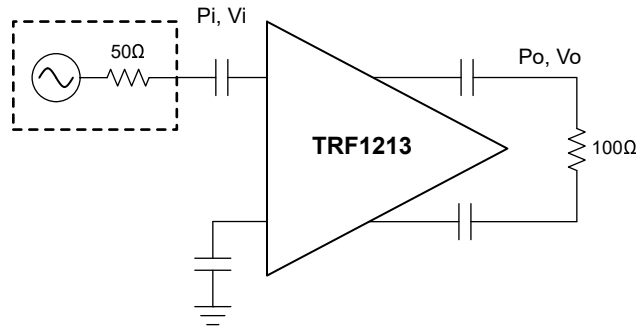


图 7-3. Power and Voltage Levels

$$\text{Voltage gain} = 20 \times \log(V_O / V_I) \quad (1)$$

$$\text{Power gain} = 10 \times \log(P_O / P_I) = 10 \times \log((V_O^2 / 100) / (V_I^2 / 50)) = 20 \times \log(V_O / V_I) - 3\text{dB} \quad (2)$$

表 7-1. Output Voltage Swings for Different Input Power Levels

| SINGLE-ENDED INPUT | | DIFFERENTIAL OUTPUT (TRF1213) | |
|----------------------------|--------------------------|----------------------------------|--------------------------|
| P_I (dBm ₅₀) | V_I (V _{PP}) | P_O (dBm ₁₀₀) | V_O (V _{PP}) |
| -18 | 0.080 | -4 | 0.564 |
| -13 | 0.142 | 1 | 1.004 |
| -8 | 0.252 | 6 | 1.785 |
| -7 | 0.283 | 7 | 2.002 |

7.1.3 Thermal Considerations

The TRF1213 is available in a 2mm × 2mm, WQFN-FCRLF package that has excellent thermal properties. Connect the thermal pad underneath the chip to a ground plane. Short the ground plane to the other ground pins of the chip, if possible, to allow heat propagation to the top layer of PCB. Use a thermal via that connects the thermal pad plane on the top layer of the PCB to the inner layer ground planes to allow heat propagation to the inner layers.

7.2 Typical Applications

An example of the TRF1213 acting as an S2D amplifier for the AFE7950 is explained in this section.

7.2.1 TRF1213 in Receive Chain

This section describes an RF receiver chain in which the TRF1213 operates as a single-ended-to-differential (S2D) amplifier and drives a receive channel of AFE7950.

Figure 7-4 shows a generic schematic of a design in which TRF1213 drives an AFE7950 receive channel. The exact values of the components depend on the frequency band for which the AFE7950 front-end is matched.

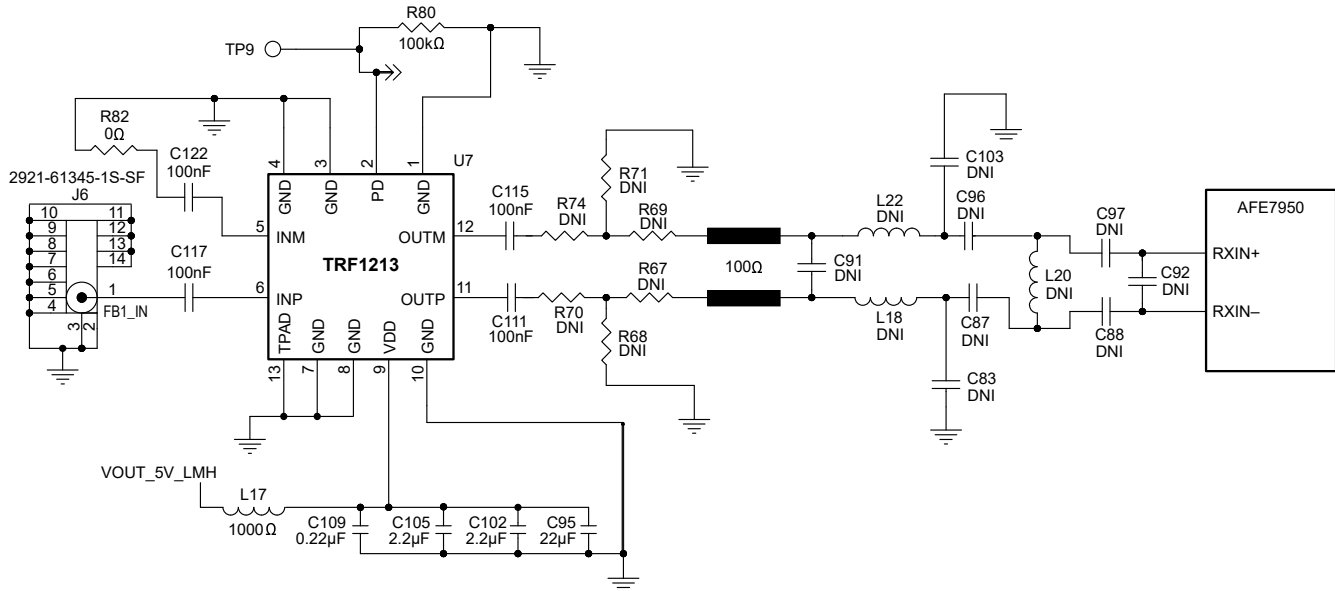


Figure 7-4. TRF1213 in a Receive Chain With the AFE7950

7.2.1.1 Design Requirements

The AFE7950 channel is required to be matched to 9.6GHz.

7.2.1.2 Detailed Design Procedure

The TRF1213 is configured as an S2D amplifier. The section close to TRF1213 output is an attenuator pad that is meant for robust matching. The section close to the AFE7950 is the matching network for the AFE7950 ADC input that is channel dependent. The matching components are chosen based on the AFE7950 return-loss data and some final optimization because the manufactured board parameters can influence the exact component values needed.

Table 7-2 shows the bill of materials (BOM) values of the design for RXC channel that is matched to center frequency of 9.6GHz.

表 7-2. Component Values of RX Chain With Center Frequency = 9.6GHz

| SECTION | DESIGNATOR | TYPE | VALUE | INSTALL OR DO NOT INSTALL |
|--------------|------------|-----------|-------|---------------------------|
| DC block cap | C117 | Capacitor | 100nF | Install |
| DC block cap | C115 | Capacitor | 100nF | Install |
| DC block cap | C111 | Capacitor | 100nF | Install |
| DC block cap | C122 | Capacitor | 100nF | Install |
| INM term | R82 | Resistor | 0Ω | Install |
| Attenuator | R74 | Resistor | 10Ω | Install |
| Attenuator | R70 | Resistor | 10Ω | Install |
| Attenuator | R69 | Resistor | 10Ω | Install |
| Attenuator | R67 | Resistor | 10Ω | Install |
| Attenuator | R71 | Resistor | 120Ω | Install |
| Attenuator | R68 | Resistor | 120Ω | Install |
| Matching | C91 | — | — | Do not install |
| Matching | C103 | — | — | Do not install |
| Matching | C83 | — | — | Do not install |
| Matching | L22 | Inductor | 0.1nH | Install |
| Matching | L18 | Inductor | 0.1nH | Install |
| Matching | C96 | Inductor | 0.1nH | Install |
| Matching | C87 | Inductor | 0.1nH | Install |
| Matching | L20 | Inductor | 0.6nH | Install |
| Matching | C97 | Capacitor | 0.3pF | Install |
| Matching | C88 | Capacitor | 0.3pF | Install |
| Matching | C92 | — | — | Do not install |

7.2.1.3 Application Curve

図 7-5 shows the in-band output response for the design in the previous section. The response is measured by AFE7950 on RXC channel with an input power of -35dBm at the input of TRF1213.

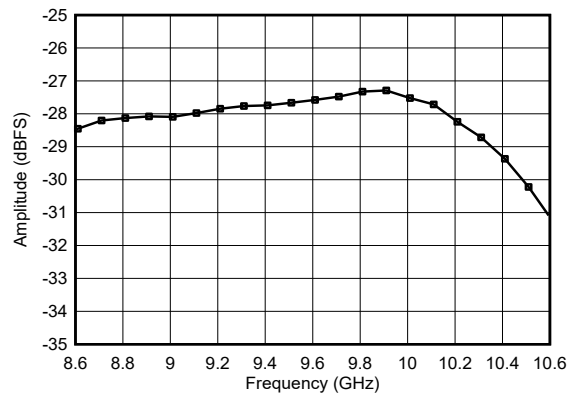



図 7-5. In-Band Output Response

7.3 Power Supply Recommendations

The TRF1213 requires a single 5V supply. Supply decoupling is critical to high-frequency performance. Typically two or three capacitors are used for supply decoupling. For the lowest-value capacitor, use a small, form-factor component that is placed closest to the V_{DD} pin of the device. Use a bulk decoupling capacitor of a larger value and size that can be placed next to the small capacitor. See also [セクション 7.4](#).

7.4 Layout

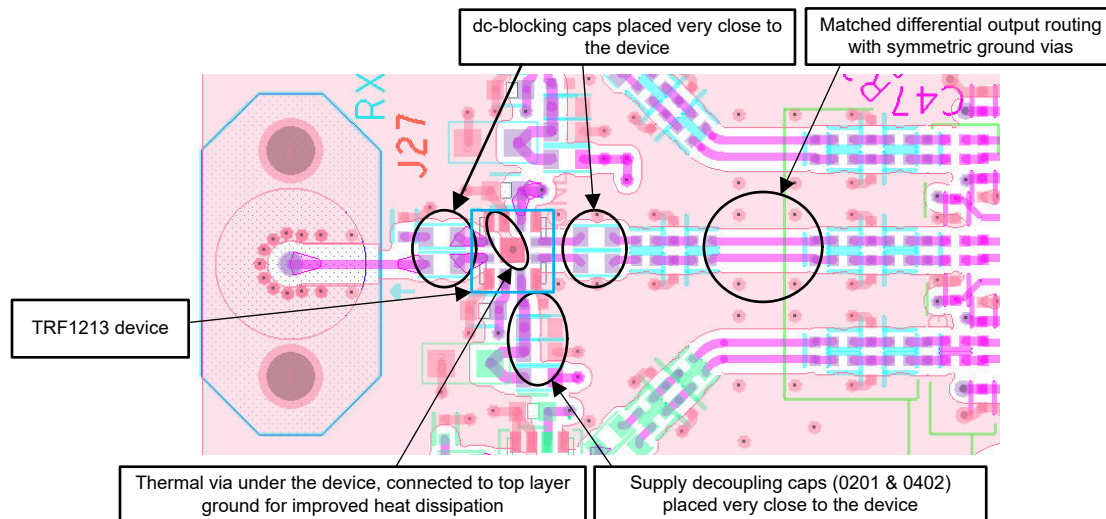
7.4.1 Layout Guidelines

TRF1213 is a wide-band, voltage-feedback amplifier with approximately 14dB of gain. When designing with a wide-band RF amplifier with relatively high gain, take precautions with board layout to maintain stability and optimized performance. Use a multilayer board to maintain signal and power integrity and thermal performance.  7-6 shows an example of a good layout. This figure shows only the top layer.

Route the RF input and output lines as grounded coplanar waveguide (GCPW) lines. For the second layer, use a continuous ground layer without any ground-cuts near the amplifier area. Match the output differential lines in length to minimize phase imbalance. Use small-footprint passive components wherever possible. Also take care of the input side layout. Use a 50Ω line for the INP routing, and ensure that the termination on INM pin has low parasitics by placing the ac-coupling capacitor very close to the device. Ensure that the ground planes on the top and internal layers are well stitched with vias.

Place thermal vias under the device that connect the top thermal pad with ground planes in the inner layers of the PCB. For improved heat dissipation, connect the thermal pad to the top-layer ground plane through the ground pins (see also [セクション 7.4.2](#)).

7.4.2 Layout Example



 7-6. Layout Example – Placement and Top Layer Layout

The TRF1213 device can be evaluated using the TRF1213 EVM board. Additional information about the evaluation board construction and test setup is given in the [TRF1213EVM user's guide](#).

8 Device and Documentation Support

8.1 Device Support

8.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [TRF1213EVM user's guide](#)

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](#) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

[テキサス・インスツルメンツ E2E™ サポート・フォーラム](#) は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

8.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE | REVISION | NOTES |
|---------------|----------|-----------------|
| December 2024 | * | Initial Release |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TRF1213RPVR | ACTIVE | WQFN-HR | RPV | 12 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 105 | 1213 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

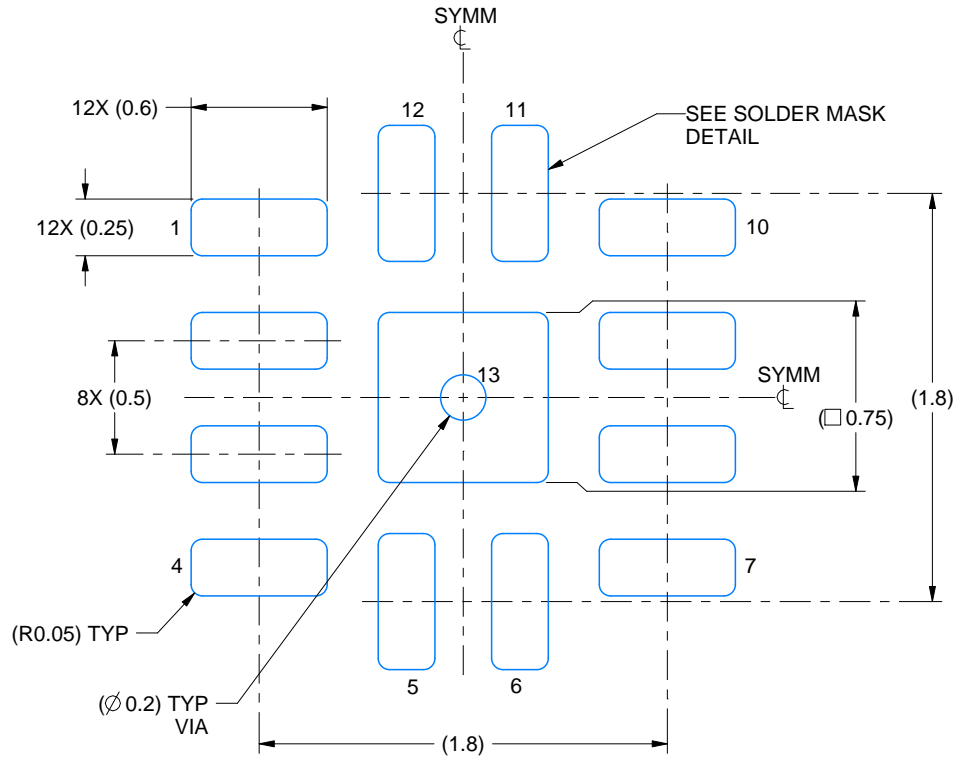
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

EXAMPLE BOARD LAYOUT

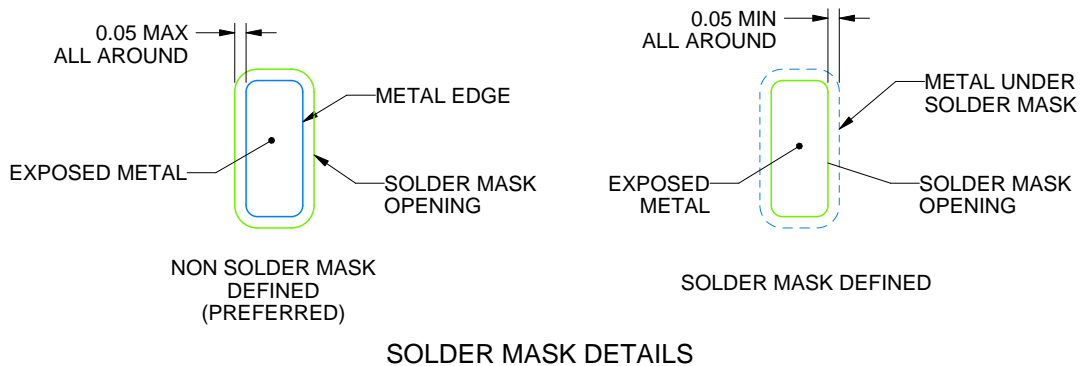
RPV0012A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

4225258/B 04/2020

NOTES: (continued)

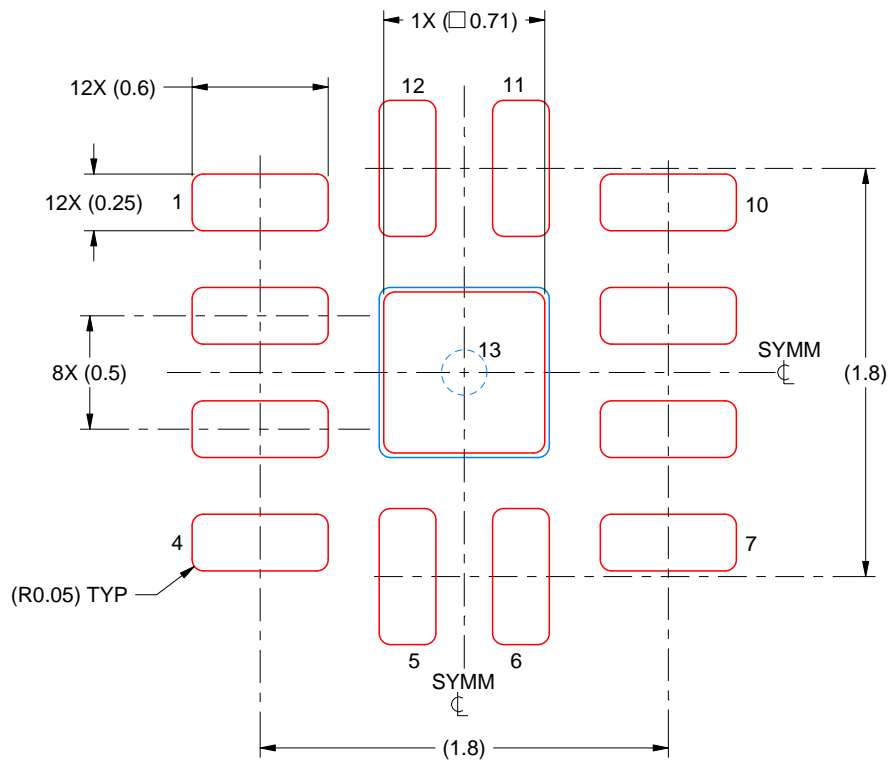
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RPV0012A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

EXPOSED PAD 13
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4225258/B 04/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated