TPSM828301, TPSM828302, TPSM828303
JAJSNB5B – JULY 2023 – REVISED JUNE 2024

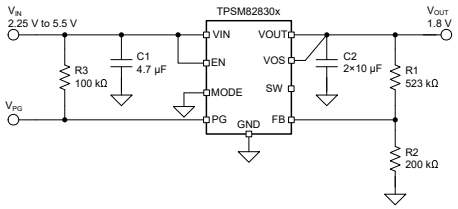
TPSM82830x、低 EMI、2.25V～5.5V 入力、1A、2A、3A 降圧パワー モジュール、インダクタ内蔵、QFN および MagPack™ パッケージ

1 特長

- EMI 性能の最適化
- CISPR 11/32 準拠が容易
  - オンチップのノイズ フィルタリング コンデンサを内蔵
  - CISPR に準拠した測定値を使用可能
- 調整可能な出力電圧:0.5V～4.5V
- 1% の FB 電圧精度 (-40℃～125℃ T_J)
- 55mΩ ドロップアウト抵抗
- 入力電圧範囲:2.25V～5.5V
- 2.0MHz のスイッチング周波数
- 動作時静止電流:7μA
- DCS-Control トポロジ
- 優れた過度応答
- MODE ピンにより、強制 PWM とパワー セーブ モードを選択
- 1.2V GPIO をサポート
- 100% デューティ サイクル動作による最小のドロップアウト電圧
- アクティブ出力放電
- パワー グッド出力
- サーマル シャットダウン保護機能
- ヒカップまたはラッチオフ OCP/OVP
- PSpice と SIMPLIS のモデルを使用可能
- 0.5mm ピッチの 2 つのパッケージ オプション
  - 標準 QFN
  - シールド付き MagPack
- WEBENCH® Power Designer により、TPSM828303 を使用するカスタム設計を作成

2 アプリケーション

- 産業用 PC
- LPDDR5 0.5V VDDQ 電源
- ASIC、SoC、MCU の電源
- ファクトリ オートメーション / 制御
- 医療用患者モニタ
- 一般的なポイント オブ ロード (POL)



代表的なアプリケーション回路図

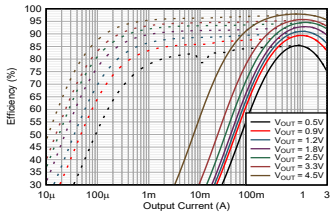
3 概要

TPSM82830x は、内蔵インダクタおよび EMI 低減技術を備えた使いやすい同期整流式降圧 DC/DC モジュール ファミリです。これらのデバイスは DCS-Control トポロジをベースとしており、出力静電容量が小さく、高速過渡応答を実現します。出力電圧は最小 0.5V に設定でき、動作時の接合部温度範囲全体にわたって 1% の高い帰還電圧精度を維持します。MODE ピンにより、省電力モードと強制 PWM モードを選択できます。省電力モードでは、低出力電流時のバッテリ駆動時間が延長され、強制 PWM モードではインダクタの連続導通が維持され、一定のスイッチング周波数でリップルが低減されます。内部のソフトスタート回路によって電圧が上昇し、厳密に制御されてパワー グッド信号によって正しい出力電圧が示されます。これらのデバイスは 100% モードをサポートしています。ヒカップ短絡保護機能と、サーマル シャットダウンの組み合わせにより、デバイスおよびアプリケーションを保護します。このファミリは 3.0mm × 3.0mm × 1.95mm の QFN パッケージと 2.5mm × 2.6mm × 1.95mm の MagPack パッケージで供給されます。

製品情報

部品番号(3)	出力電流	パッケージ(1)	パッケージ サイズ(2)
TPSM828301	1A	RDS (QFN、9)	3.0mm × 3.0mm
TPSM828302	2A		
TPSM828303	3A		
TPSM828303	3A	VCB (QFN、10)(4)	2.5mm × 2.6mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 「デバイスのオプション」表を参照してください。
(4) 事前情報 (量産データではありません)。



V_{IN} = 5V での効率、VCB パッケージ

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4 Device Options

PART NUMBER	OUTPUT CURRENT	OCP MODE	PACKAGE	OUTPUT VOLTAGE
TPSM828301ARDSR	1 A	Hiccup(2)	QFN RDS	Adjustable(1)
TPSM828302ARDSR	2 A	Hiccup(2)	QFN RDS	
TPSM828303ARDSR	3 A	Hiccup(2)	QFN RDS	
TPSM828303PVCBR(3)	3 A	Hiccup(2)	QFN VCB	

(1) For fixed output voltage versions, please contact Marketing for availability.
(2) For versions with OCP/OVP Latch-off, please contact Marketing for availability.
(3) Advance information (not Production Data).

5 Pin Configuration and Functions

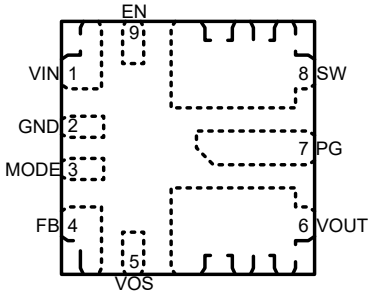


図 5-1. RDS Package, 9-Pin QFN-FCMOD Top View

表 5-1. Pin Functions: RDS Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Input voltage pin. Connect the input capacitor as close as possible between V_{IN} and GND.
GND	2	PWR	Ground pin
MODE	3	I	The device runs in PSM/PWM mode when this pin pulls low and in forced-PWM mode when pulled high. This action can also be done when the device is in-operation. Do not leave this pin floating.
FB	4	I	Feedback pin. Connect the resistive output voltage divider to this pin.
VOS	5	I	Output voltage sense pin. Connect this pin directly after the inductor.
VOUT	6	PWR	Output voltage pin
PG	7	O	Power good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating.
SW	8	PWR	Switch pin of the converter, which is connected to the internal power MOSFET and the inductor. Avoid connecting this pin to larger traces as this can increase EMI. this pin can stay unconnected or be soldered to a small pad for thermal improvement.
EN	9	I	Device enable pin. To enable the device, pull this pin high. Pulling this pin low disables the device. Do not leave this pin unconnected.

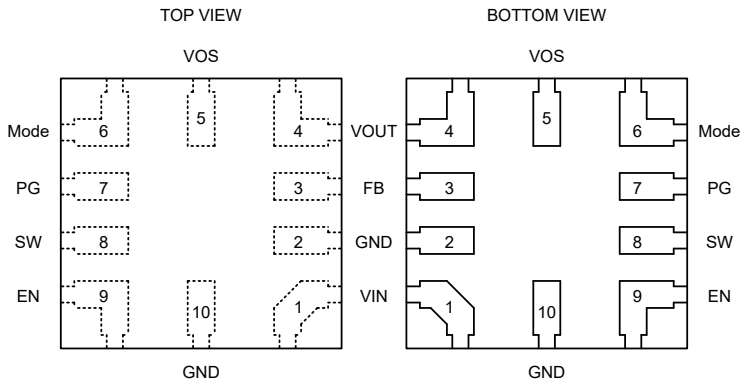


図 5-2. VCB Package, 10-Pin QFN-FCMOD

表 5-2. Pin Functions: VCB Package

PIN		TYPE	DESCRIPTION
NAME	NO.		
VIN	1	PWR	Input voltage pin. Connect the input capacitor as close as possible between V_{IN} and GND.
GND	2, 10	PWR	Ground pins
FB	3	I	Feedback pin. Connect the resistive output voltage divider to this pin.
VOUT	4	PWR	Output voltage pin
VOS	5	I	Output voltage sense pin. Connect this pin directly after the inductor.
MODE	6	I	The device runs in PSM/PWM mode when this pin pulls low and in forced-PWM mode when pulled high. This action can also be done when the device is in operation. Do not leave this pin floating.
PG	7	O	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave this pin floating.
SW	8	PWR	Switch pin of the converter, which is connected to the internal power MOSFET and the inductor. Avoid connecting this pin to larger traces as this action can increase EMI. This pin can stay unconnected or be soldered to a small pad for thermal improvement.
EN	9	I	Device enable pin. To enable the device, pull this pin high. Pulling this pin low disables the device. Do not leave this pin unconnected.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage (2)	V_{IN}, EN, MODE, FB, PG, V_{OUT}	–0.3	6	V
T_J	Operating junction temperature	–40	125	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	± 2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	± 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	2.25		5.5	V
V_{OUT}	Output voltage range	0.5		4.5	V
C_{IN}	Effective input capacitance (1)	3			µF
C_{OUT}	Effective output capacitance (1)	12		200	µF
I_{OUT}	Output current range; TPSM828301			1	A
I_{OUT}	Output current range; TPSM828302			2	A
I_{OUT}	Output current range; TPSM828303 (2)			3	A
I_{PG}	Power-good input current capability			1	mA
T_J	Operating junction temperature(2)	–40		125	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied.
(2) In applications where high power dissipation and high ambient temperatures are present, the maximum output current must be derated to operate the module within its operating temperature range.

6.4 Thermal Information RDS Package

THERMAL METRIC (1)		TPSM82830xARDSR		UNIT
		RDS		
		9 pins (JEDEC board)	9 pins (EVM board)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	59.4	49.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.5	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.8	n/a(2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	16.7	23.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.
(2) Not applicable to an EVM.

6.5 Thermal Information VCB Package

THERMAL METRIC[1]		TPSM828303PVCBR		UNIT
		VCB		
		10 pins (JEDEC board)	10 pins (EVM board)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.1	66.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.1	n/a[2]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	n/a[2]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	(-1.7)[3]	(-1.6)[3]	°C/W
ψ_{JB}	Junction-to-board characterization parameter	27.2	35.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics report.
(2) Not applicable to an EVM.
(3) Case top temperature can be higher than temperature of active circuit because of inductor power dissipation. This results in a negative Junction-to-top characterization parameter.

6.6 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 2.25 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating quiescent current	EN = V_{IN}, I_{OUT} = 0 mA, V_{OUT} = 1.8 V, MODE = GND, device not switching		7	17	µA
I_{SD}	V_{IN} shutdown supply current	EN = low, T_J = –40ºC to 85ºC		100	700	nA
$V_{UVLO(+)}$	Rising UVLO threshold voltage (V_{IN})		2.05	2.15	2.25	V
$V_{UVLO(hys)}$	UVLO hysteresis (V_{IN})		90	120		mV
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	T_J rising		150		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C
LOGIC PINs						
$V_{EN(+)}$	High-level input voltage (EN)		0.8			V
$V_{EN(-)}$	Low-level input voltage (EN)				0.35	V
$V_{MODE(+)}$	High-level input voltage (MODE)		0.8			V
$V_{MODE(-)}$	Low-level input voltage (MODE)				0.35	V
$I_{EN(LKG)}$	EN Input leakage current	V_{EN} = HIGH		10	100	nA
$I_{MODE(LKG)}$	MODE Input leakage current	V_{MODE} = HIGH		10	100	nA
STARTUP						
t_{SS}	Internal fixed soft-start time	From V_{OUT} = 0 to V_{OUT} = 95%	180	300	440	µs
$t_{d(EN)}$	Enable delay time	From EN HIGH to device starts switching		120	220	µs
REFERENCE VOLTAGE						
V_{FB}	Feedback voltage accuracy	PWM mode	495	500	505	mV
V_{FB}	Feedback voltage accuracy	PWM mode	–1		+1	%
V_{FB}	Feedback voltage accuracy	PFM mode, $C_{OUT,eff}$ ≥ 15 µF, L = 0.47 µH	–1		+2	%
$I_{FB(LKG)}$	FB input leakage current, adjustable version	V_{FB} = 0.5 V		10	70	nA
$I_{VOS(LKG)}$	VOS input leakage current	V_{EN} = low		100	500	nA
POWER GOOD						
$V_{PG,UV(+)}$	Rising power-good threshold voltage (output undervoltage)	Power Good low, V_{FB} rising	94	96	98	%
$V_{PG,UV(-)}$	Falling power-good threshold voltage (output undervoltage)	Power Good high, V_{FB} falling	90	92	94	%
$V_{PG,OV(+)}$	Rising power-good threshold voltage (output overvoltage)	Power Good high, V_{FB} rising	108	110	112	%
$V_{PG,OV(-)}$	Falling power-good threshold voltage (output overvoltage)	Power Good low, V_{FB} falling	102.5	105	107	%
$t_{d(PG)}$	Power good delay at start-up	Low-to-high transition on the PG pin at start up		128		µs

6.6 Electrical Characteristics (続き)

T_J = –40°C to +125°C, V_{IN} = 2.25 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(PG)}$	Power good deglitch delay during operation	High-to-low or low-to-high transition on the PG pin	30	45	60	µs
$I_{PG(LKG)}$	PG pin Leakage current when open drain output is high	V_{PG} = 5.0 V		10	100	nA
$V_{PG,OL}$	PG pin low-level output voltage	I_{PG} = 1 mA			0.4	V
POWER STAGE						
R_{DP}	Dropout resistance	TPSM82830x, V_{IN} ≥ 5 V, 100% mode, T_J = 25°C, VCB package		55		mΩ
R_{DP}	Dropout resistance	TPSM82830x, V_{IN} ≥ 5 V, 100% mode, T_J = 25°C, RDS package		61		mΩ
R_{DP}	Dropout resistance	TPSM82830x, V_{IN} = 2.7 V, 100% mode, T_J = 25°C		78	105	mΩ
f_{SW}	Switching frequency, PWM mode	I_{OUT} = 1 A, V_{OUT} = 1.8 V		2.0		MHz
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	TPSM828301	1.8	2.1	2.6	A
$I_{HS(OC)}$	High-side peak current limit	TPSM828302	2.7	3.3	3.9	A
$I_{HS(OC)}$	High-side peak current limit	TPSM828303	4.0	4.6	5.4	A
$I_{LS(NOC)}$	Low-side negative current limit	Sinking current limit on LS FET		–1.8		A
OUTPUT DISCHARGE						
I_{DIS}	Output discharge current on SW pin	V_{IN} > 2 V, V_{SW} = 0.4 V, EN = LOW	75	400		mA

6.7 Typical Characteristics

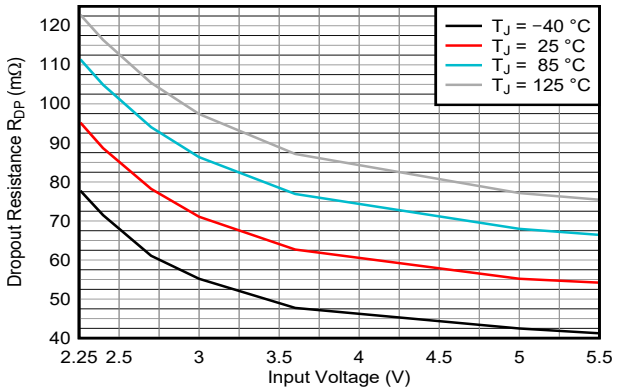


図 6-1. TPSM82830x Dropout Resistance RDS Package

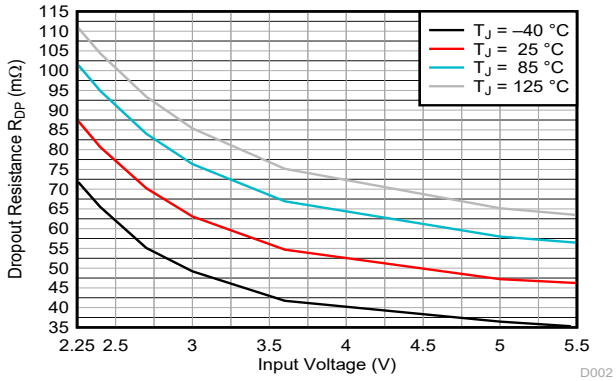


図 6-2. TPSM82830x Dropout Resistance VCB Package

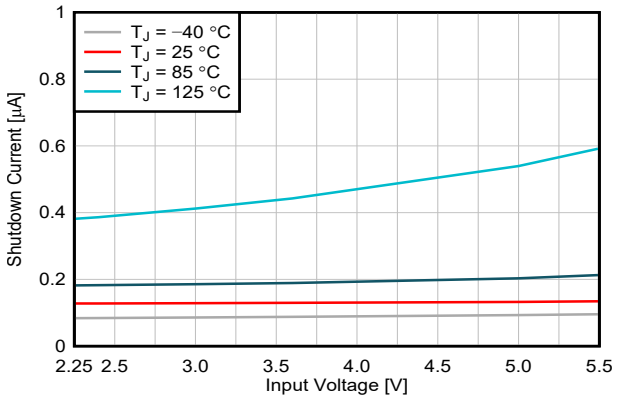


図 6-3. Shutdown Current

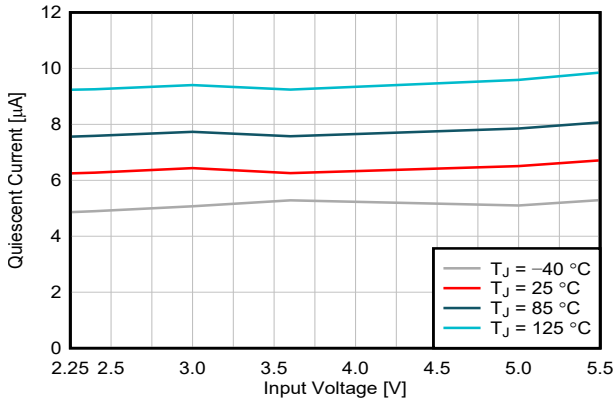


図 6-4. Quiescent Current

7 Detailed Description

7.1 Overview

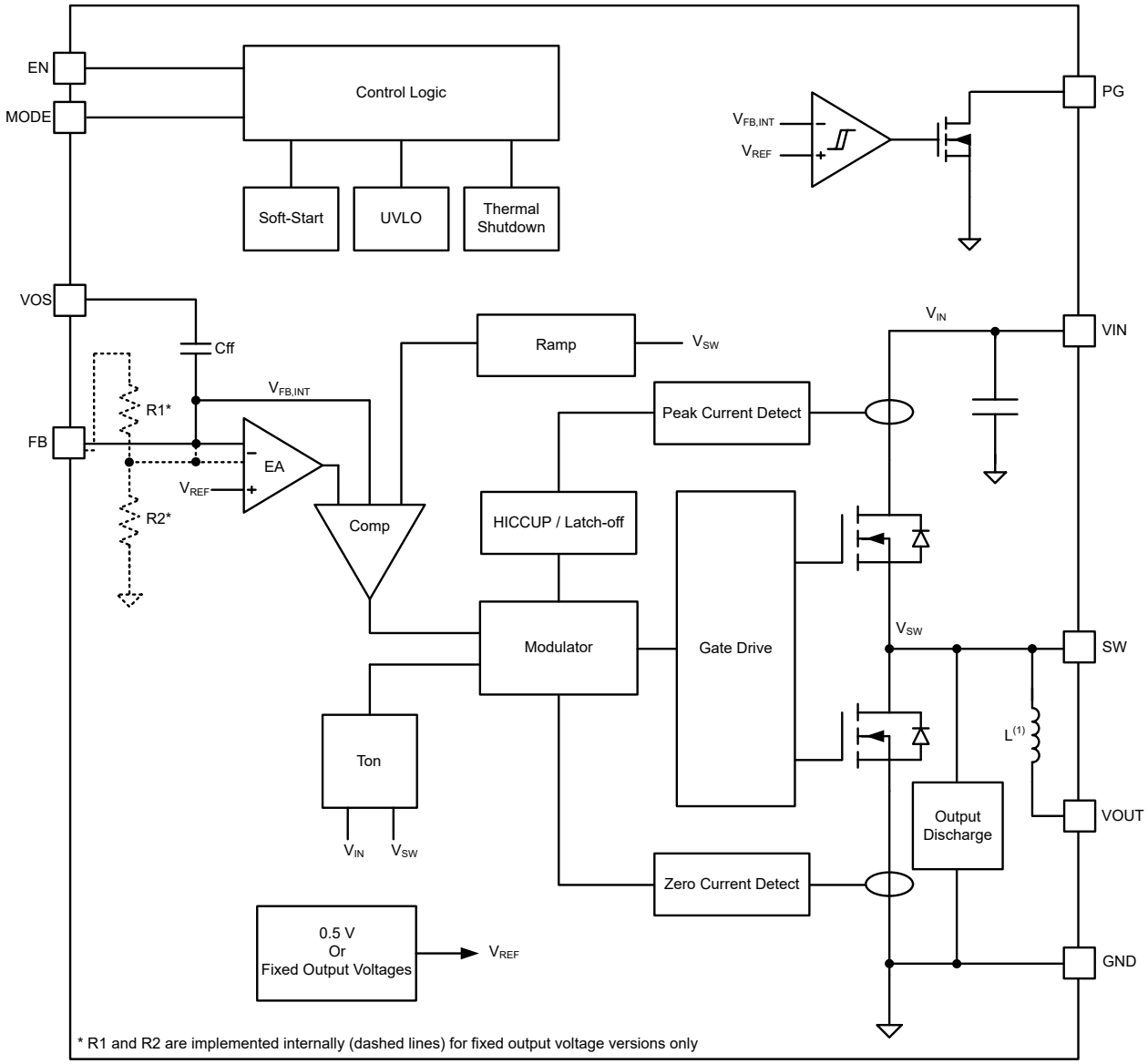
The TPSM82830x is a family of low-voltage step-down modules available in 1-, 2- and 3-A versions. These devices use a DCS-Control scheme which transitions seamlessly from pulse-width modulation (PWM) at medium and high output currents to pulsed-frequency modulation (PFM) at low output currents. During PWM operation, the devices switch at 2 MHz; during PFM operation, the switching frequency varies with the load current and reduces as the load current decreases. For applications that require the lowest possible output voltage ripple or a constant switching frequency, a high logic level on the MODE pin forces the devices to use PWM under all load conditions (at the expense of lower efficiency at low output currents). An external resistor-divider sets the output voltage anywhere from 0.5 V to 4.5 V and the nominal switching frequency is 2 MHz with a controlled variation over the input voltage range.

Device variants are available that support both hiccup and latch-off protection behavior.

The TPSM82830x devices offer two significant advantages compared to previous devices in this series: Transient performance has improved significantly by usage of a fast comparator in both PFM and PWM modes, and EMI is reduced by an optimized gate driver and on-chip decoupling capacitors.

The VCB package version uses MagPack technology for even further EMI reduction. MagPack, a Texas Instruments proprietary integrated-magnetics packaging technology, delivers the highest-performance power module design. Besides EMI reduction, MagPack enhances efficiency and thermal properties of power modules. This feature enables an industry-leading power density.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Pulse Width Modulation (PWM) Operation

If the MODE pin is LOW and at load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM) as shown in 図 7-1. The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times 500ns \quad (1)$$

If the MODE pin is HIGH, the converter maintains a forced-PWM operation for all load currents.

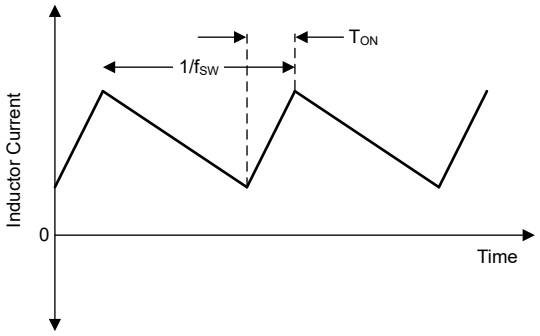


図 7-1. Continuous Conduction Mode (PWM-CCM) Current Waveform

7.3.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This event happens when the output current becomes smaller than half of the ripple current of the inductor. The device operates with a fixed on-time, and the switching frequency decreases proportional to the load current as shown in 図 7-2. Calculate as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{T_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \quad (2)$$

Use L=470nH for the RDS package and L=340nH for the VCB package.

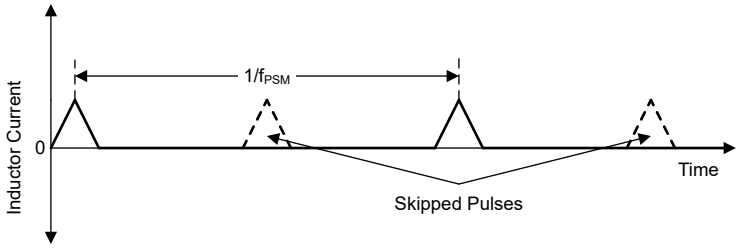


図 7-2. Discontinuous Conduction Mode (PSM-DCM) Current Waveform

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device does not enter PSM and maintains output regulation in PWM mode.

7.3.3 Start-Up and Soft Start

When the EN voltage goes High, the device starts loading the default values into the device registers. This action typically is done within 120 µs. After that, the internal soft-start circuitry controls the output voltage during start-up. This control avoids excessive inrush current and makes sure of a controlled output voltage ramp. This control also prevents unwanted voltage drops from high-impedance power sources or batteries. Finally, the PG signal has a delay up to 180 µs at start-up. 図 7-3 shows a start-up sequence, where the EN pin is pulled up to VIN.

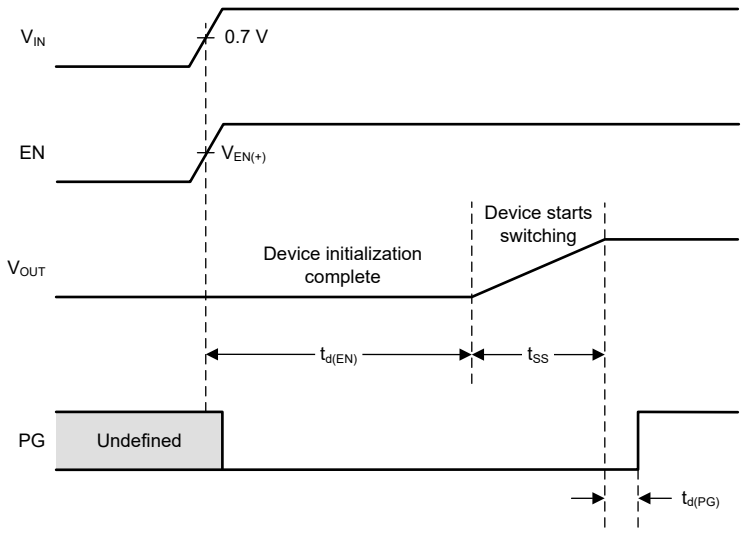


図 7-3. Start-Up Timing When EN is Pulled Up to VIN

図 7-4 shows a start-up sequence, where an external signal is connected to the EN pin.

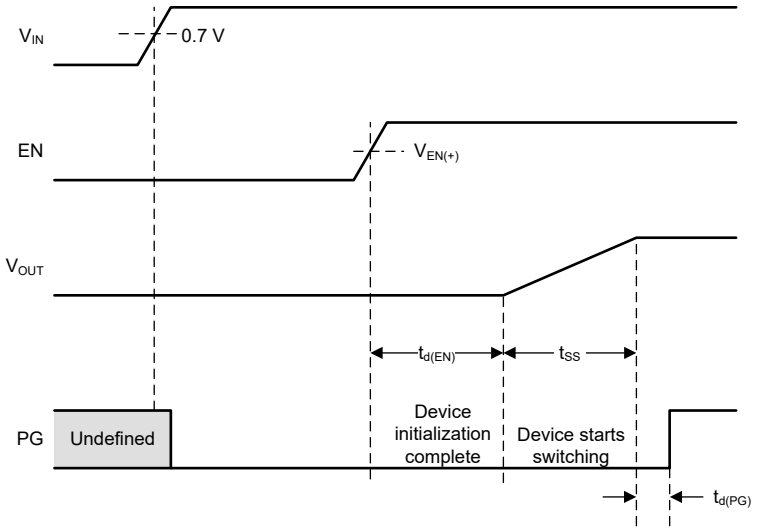


図 7-4. Start-Up Timing When an External Signal is Connected to the EN Pin

The TPSM82830x can start into a prebiased output if enabled for the first time. For a new prebiased operation, a power cycle is needed to disable the active output discharge. 図 7-5 shows a start-up into a prebiased output voltage.

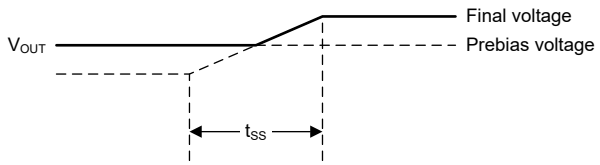


図 7-5. Start-Up into a Prebiased Output

7.3.4 Switch Cycle-by-Cycle Current Limit

All the devices in the family have a cycle-by-cycle current limit function. When the device detects that the current in the high-side FET exceeds the high-side current limit, either due to a heavy load or a short-circuit condition, the device immediately turns off the high-side FET and turns on the low-side FET. The high-side FET turns on again at the start of the next switching cycle. Note that because of the propagation delay in the current limit comparator (typically 60 ns), the current flowing in the high-side FET when the device detects a current limit condition can be slightly higher than the current limit specified in the device Electrical Characteristics.

7.3.5 Undervoltage Lockout

The undervoltage lockout (UVLO) function prevents misoperation of the device if the input voltage drops below the UVLO threshold.

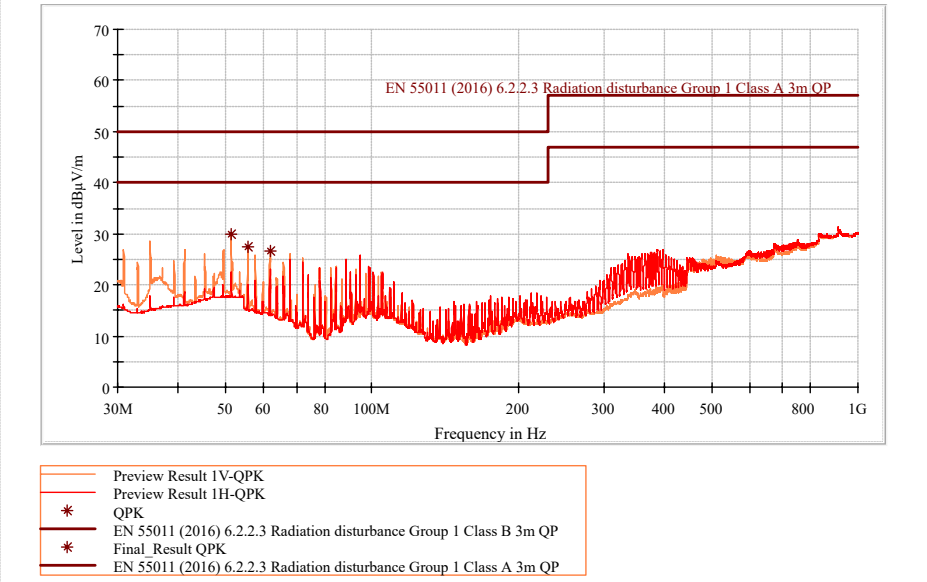
7.3.6 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typical), the device goes in thermal shutdown with a hysteresis of typically 20°C. After T_J has decreased enough, the device resumes normal operation.

7.3.7 Optimized EMI Performance

TPSM82830x devices incorporate advanced techniques to minimize Electromagnetic Interference (EMI) and makes complying with stringent EMI standards simple. By integrating capacitors directly onto the silicon, parasitic elements are reduced and loop area is minimized, effectively reducing high-frequency noise emissions primarily above 450 MHz. The on-chip capacitors ensure low-inductance paths for high-frequency AC switching current and damping voltage ringing.

Additionally to the on-chip capacitors, the gate driver has been improved with advanced slew rate control mechanisms and by smoothing the supply voltage. The switch node voltage is controlled in a way to reduce sharp edges and minimize voltage overshoot, consequently diminishing EMI.



The above plot is measured on the EVM with the TPSM828303ARDSR and standard BOM.

I_{OUT} = 3 A V_{IN} = 5.5 V V_{OUT} = 1.8 V

図 7-6. Radiated EMI Performance (CISPR11 Radiated Emission Test with Class A and Class B Limits)

7.4 Device Functional Modes

7.4.1 Enable, Disable, and Output Discharge

The device starts operation when Enable (EN) is set High. The input threshold levels are typically 0.8 V for rising and 0.35 V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled Low with a shutdown current of typically 100 nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore VIN must remain present for the discharge to function.

7.4.2 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles because, even at very low duty cycles, the switching frequency is reduced as needed to always make sure of a proper regulation.

If the output voltage (V_{OUT}) comes close to the input voltage (V_{IN}), the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. This action is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The difference between V_{IN} and V_{OUT} is determined by the voltage drop across the high-side FET and the DC resistance of the inductor. The minimum V_{IN} that is needed to maintain a specific V_{OUT} value is estimated as:

$$V_{IN,min} = V_{OUT} + I_{OUT,MAX} \times R_{DP} \quad (3)$$

where

- $V_{IN,min}$ = Minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ = Maximum output current
- R_{DP} = Resistance from VIN to VOUT, which includes the high-side MOSFET on-resistance and DC resistance of the inductor

7.4.3 Power Good

The TPSM82830x has a built-in power-good (PG) function. The PG pin goes high impedance when the output voltage has reached the nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low (see 表 7-1). The PG function is formed with a window comparator, which has an upper and lower voltage threshold. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5 V.

表 7-1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH Z	LOW
Enable	EN = High, V_{FB} ≥ 0.48 V	√	
	EN = High, V_{FB} ≤ 0.56 V		√
	EN = High, V_{FB} ≤ 0.525 V	√	
	EN = High, V_{FB} ≥ 0.55 V		√
Shutdown	EN = Low		√
Thermal shutdown	$T_J > T_{JSD}$		√
UVLO	0.7 V < V_{IN} < V_{UVLO}		√
Power supply removal	V_{IN} < 0.7 V	√	

The PG signal can be used for sequencing of multiple rails by connecting the PG signal to the EN pin of other converters. Leave the PG pin unconnected when not used. The PG rising edge and falling edge has a 40 µs blanking time, as shown in 図 7-7. At start-up, the delay of PG signal is typically 125 µs after soft start is finished.

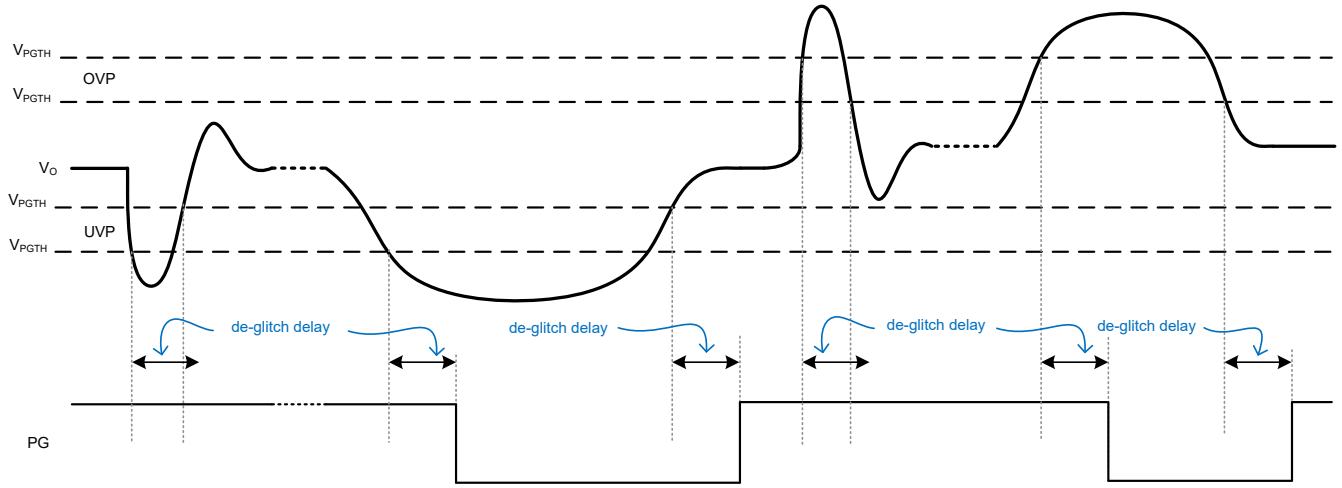


図 7-7. Power-Good Behavior

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

The TPSM82830x is a synchronous step-down converter power module, where the required power inductor is integrated inside the package. The inductance value is 0.47 µH with a ±20% tolerance for the RDS package and 0.34 µH with a ±20 % tolerance for the VCB package. The family members within a package category are pin-to-pin and BOM-to-BOM compatible with each other.

8.2 Typical Application

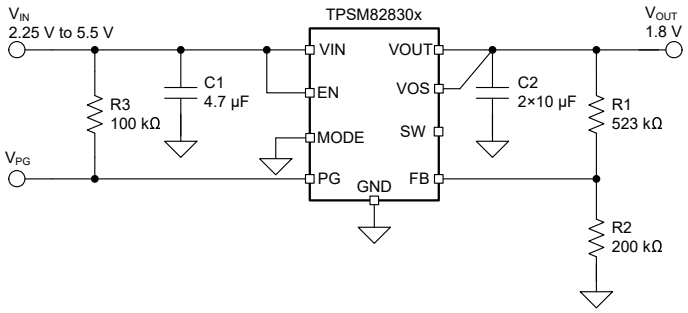


図 8-1. Typical Application of TPSM82830x

8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1 as the input parameters.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.25 V to 5.5 V
Output voltage	1.8 V
Output ripple voltage	< 15 mV

表 8-2 lists the components used for the example.

表 8-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	4.7 µF, Ceramic capacitor, 6.3 V, X7R, size 0603, JMK107BB7475KA-T	Taiyo Yuden
C2	2 × 10 µF, Ceramic capacitor, 10 V, X7R, size 0603, GRM188Z71A106KA73D	Murata
R1	Depending on the output voltage, 1%, size 0402	Std
R2	200 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std
R3	100 kΩ, Chip resistor, 1/16 W, 1%, size 0402	Std

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM82830x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to 式 4:

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.5\,V} - 1\right) \quad (4)$$

R2 can be any value between 200 kΩ and 600 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

8.2.2.3 Input Capacitor Selection

The input capacitor is the low-impedance energy source for the converter, which helps provide stable operation. Because the buck converter has a pulsating input current, a low ESR ceramic input capacitor is required for best input voltage filtering to minimize input voltage spikes. Place the capacitor between VIN and GND pins and as close as possible to those pins.

For most applications, a minimum effective input capacitance of 3 µF is sufficient, though a larger value reduces input current ripple and is recommended. When operating from a high impedance source, TI recommends a larger input buffer capacitor ≥10 µF to avoid voltage drops during start-up and load transients. Additionally, small de-coupling capacitors can also be used in case of noise at the input if the device. The input capacitor can be increased without any limit for better input voltage filtering.

表 8-3 shows a list of recommended capacitors.

表 8-3. List of Recommended Capacitors

NOMINAL CAPACITANCE [µF]	VOLTAGE RATING [V]	DIMENSIONS [mm]	MFR PART NUMBER(1)
4.7	6.3	1.6 × 0.8 × 0.8	MSASJ168BB7475MTNA01, Taiyo Yuden
4.7	10	2.0 × 1.25 × 1.25	C2012X7R1A475K125AC, TDK
10	10	1.6 × 0.8 × 0.8	GRM188Z71A106KA73#, MuRata

(1) See the *Third-party Products Disclaimer*

8.2.2.4 Output Capacitor Selection

The DCS-Control scheme of the TPSM82830x allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. To keep low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. At light load currents, the converter operates in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. A larger output capacitors can be used reducing the output voltage

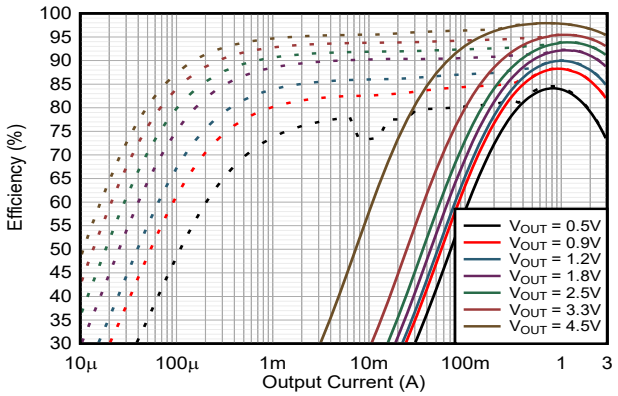
ripple. Considering the DC-bias derating the capacitance, the recommended minimum effective output capacitance is 12 µF. The recommended typical output capacitor value is 2 × 10 µF or 1 × 22 µF with an X5R or X7R dielectric. 表 8-4

表 8-4. List of Recommended Capacitors

NOMINAL CAPACITANCE [µF]	VOLTAGE RATING [V]	DIMENSIONS [mm]	MFR PART NUMBER(1)
10	6.3	2.0 × 1.5 × 1.25	MSASJ21GAB7106MTNA01, Taiyo Yuden
10	10	2.0 × 1.25 × 1.25	C2012X7R1A106K125AC, TDK
10	10	1.6 × 0.8 × 0.8	GRM188Z71A106KA73#, MuRata
10	10	1.6 × 0.8 × 0.8	C1608X5R1A106K080AC, TDK
22	10	2.0 × 1.25 × 1.25	GRM21BZ71A226ME15#, MuRata
22	10	1.6 × 0.8 × 0.8	C1608X5R1A226M080AC, TDK

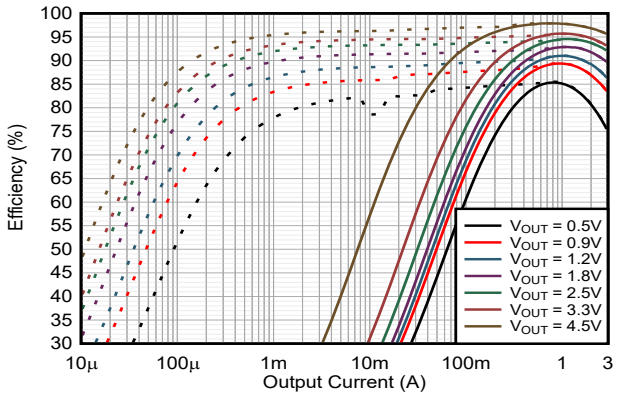
8.2.3 Application Curves

T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.8 V, BOM = 表 8-2 unless otherwise noted.



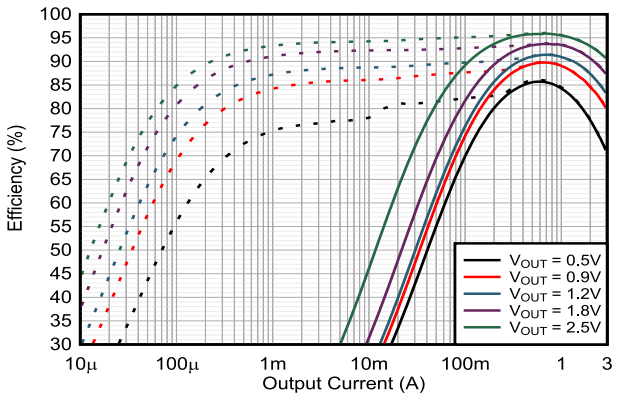
V_{IN} = 5 V RDS package T_A = 25 °C

図 8-2. Efficiency versus Output Current



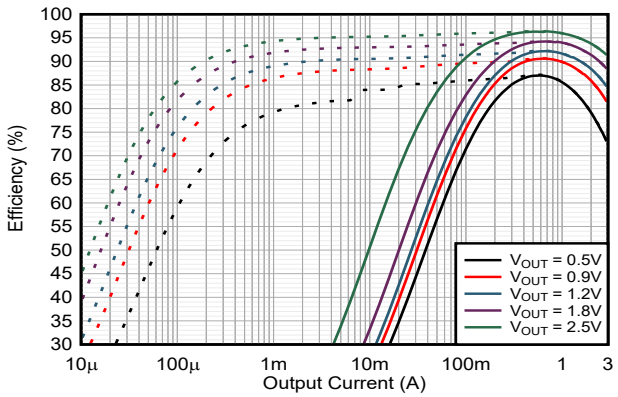
V_{IN} = 5 V VCB package T_A = 25 °C

図 8-3. Efficiency versus Output Current



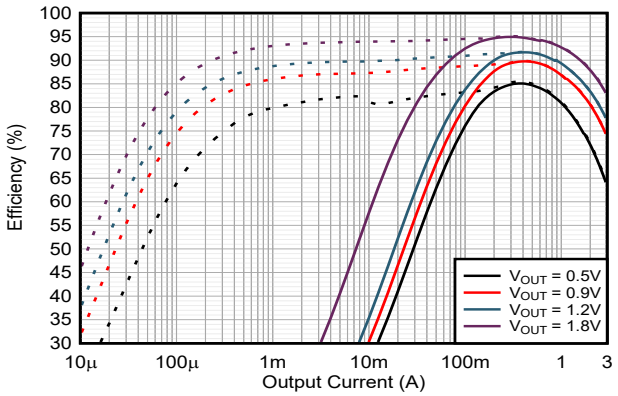
V_{IN} = 3.3 V RDS package T_A = 25 °C

図 8-4. Efficiency versus Output Current



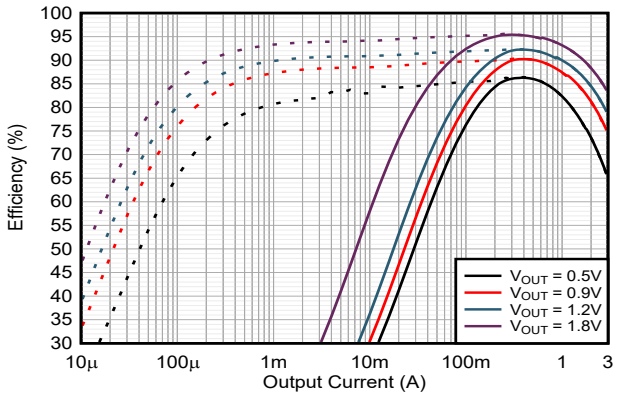
V_{IN} = 3.3 V VCB package T_A = 25 °C

図 8-5. Efficiency versus Output Current



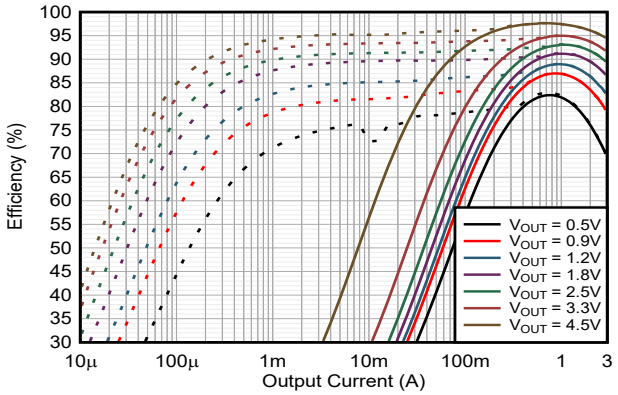
V_{IN} = 2.25 V RDS package T_A = 25 °C

図 8-6. Efficiency versus Output Current



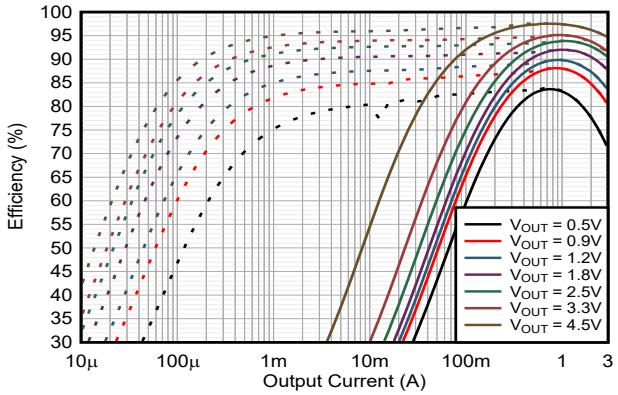
V_{IN} = 2.25 V VCB package T_A = 25 °C

図 8-7. Efficiency versus Output Current



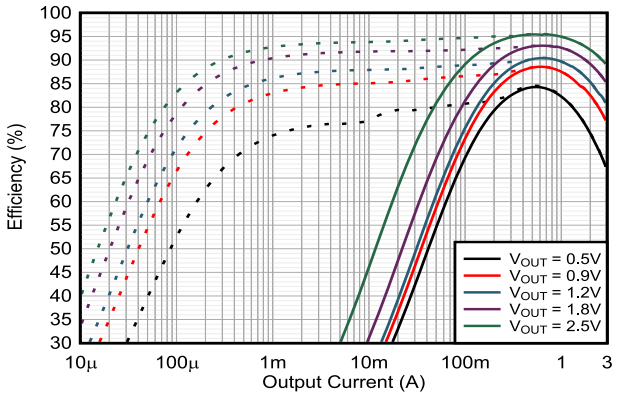
V_{IN} = 5 V RDS package T_A = 85°C

図 8-8. Efficiency versus Output Current



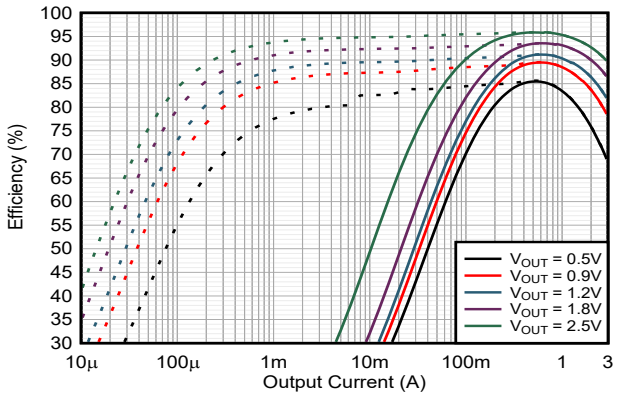
V_{IN} = 5 V VCB package T_A = 85°C

図 8-9. Efficiency versus Output Current



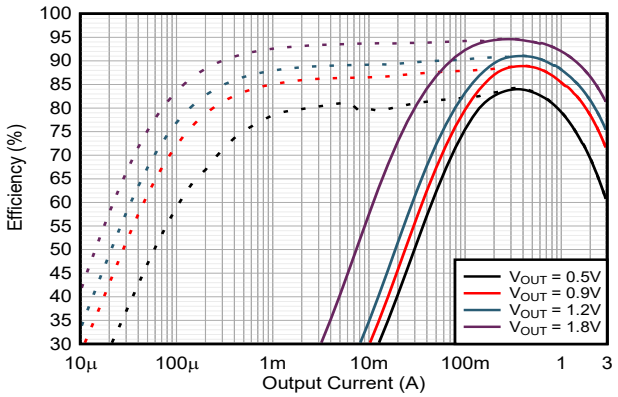
V_{IN} = 3.3 V RDS package T_A = 85°C

図 8-10. Efficiency versus Output Current



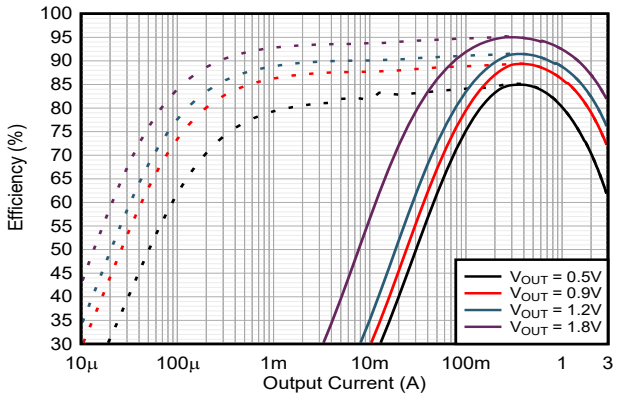
V_{IN} = 3.3 V VCB package T_A = 85°C

図 8-11. Efficiency versus Output Current



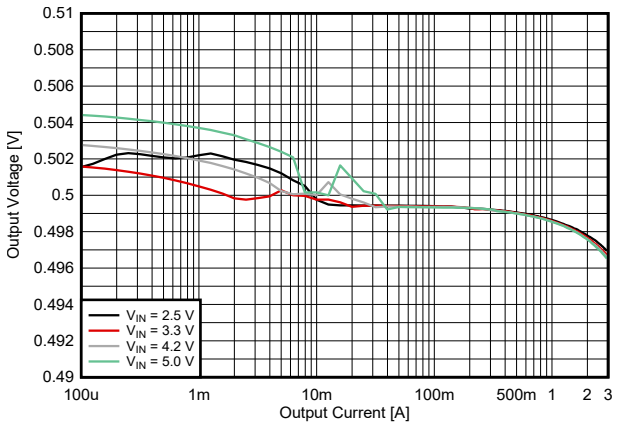
V_{IN} = 2.25V RDS package T_A = 85°C

図 8-12. Efficiency versus Output Current



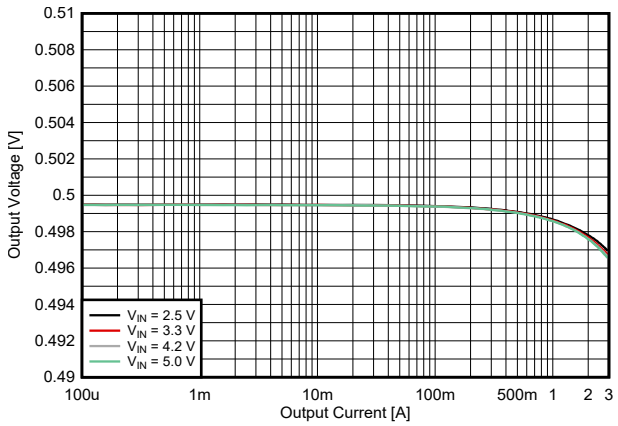
V_{IN} =2.25 V VCB package T_A = 85°C

図 8-13. Efficiency versus Output Current



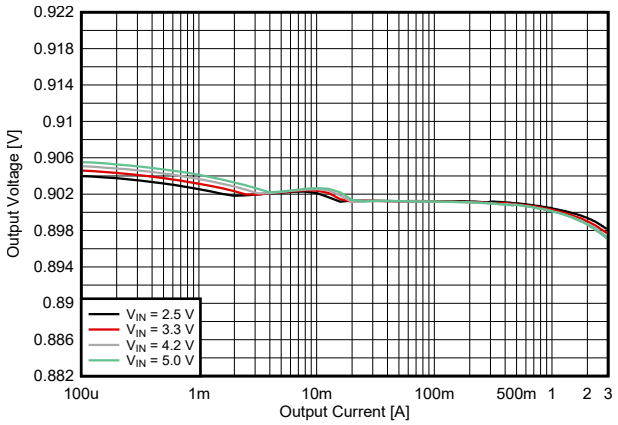
V_{OUT} = 0.5 V PFM

図 8-14. Output Voltage versus Output Current



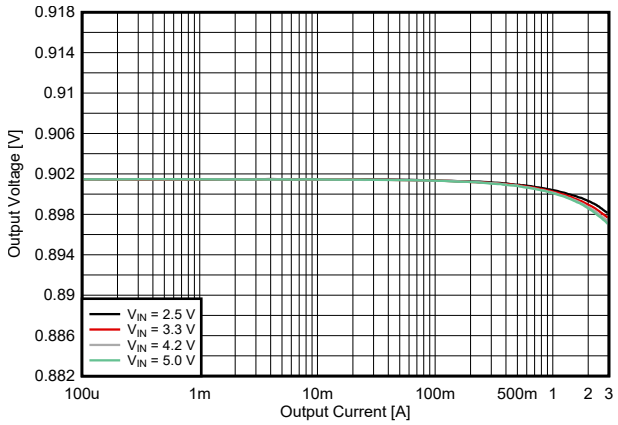
V_{OUT} = 0.5 V PWM

図 8-15. Output Voltage versus Output Current



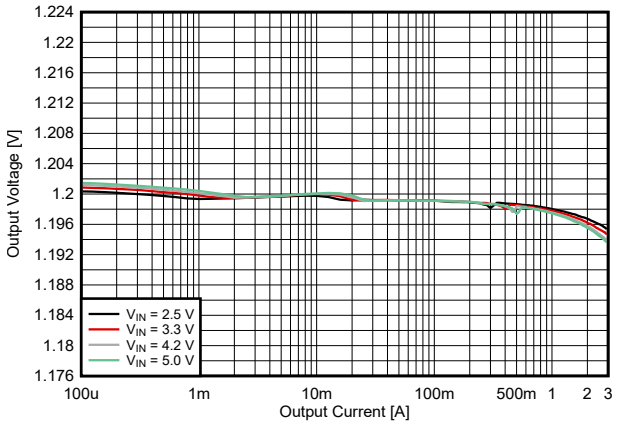
V_{OUT} = 0.9 V PFM

図 8-16. Output Voltage versus Output Current



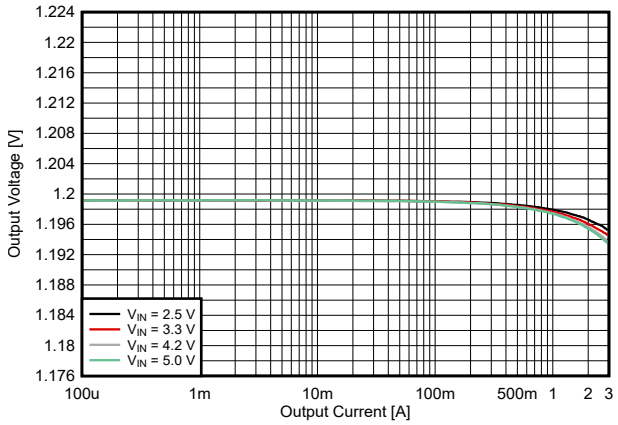
V_{OUT} = 0.9 V PWM

図 8-17. Output Voltage versus Output Current



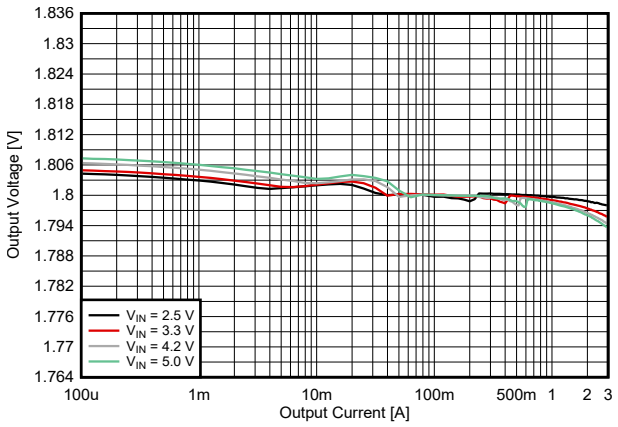
V_{OUT} = 1.2 V PFM

図 8-18. Output Voltage versus Output Current



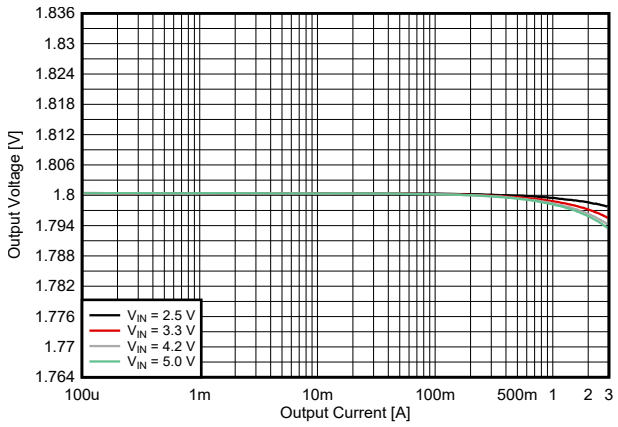
V_{OUT} = 1.2 V PWM

図 8-19. Output Voltage versus Output Current



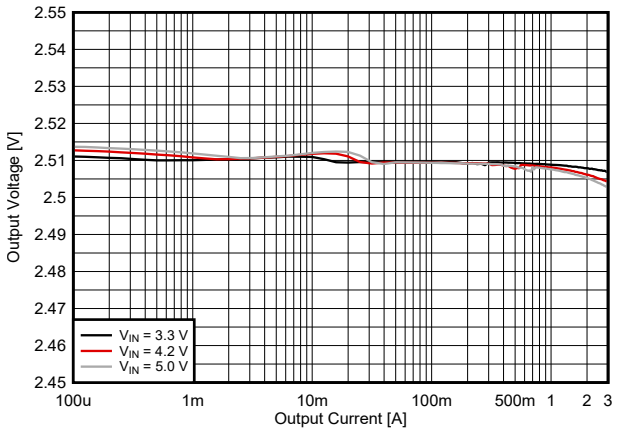
V_{OUT} = 1.8 V PFM

図 8-20. Output Voltage versus Output Current



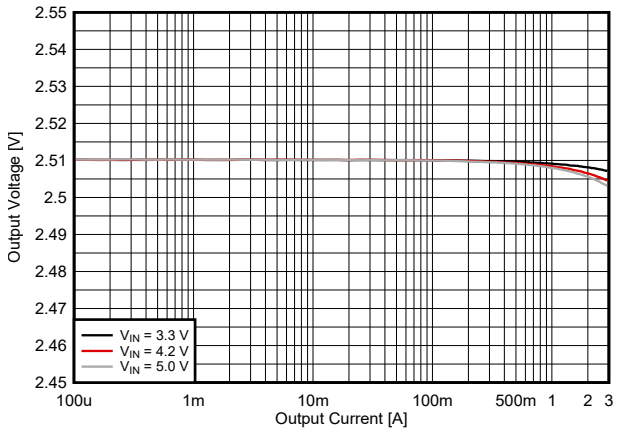
V_{OUT} = 1.8 V PWM

図 8-21. Output Voltage versus Output Current



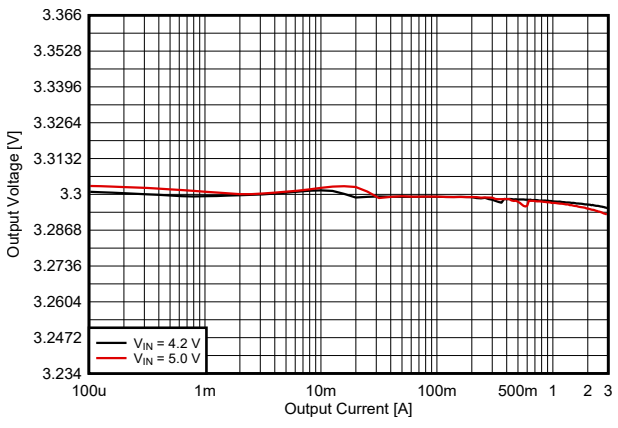
V_{OUT} = 2.5 V PFM

図 8-22. Output Voltage versus Output Current



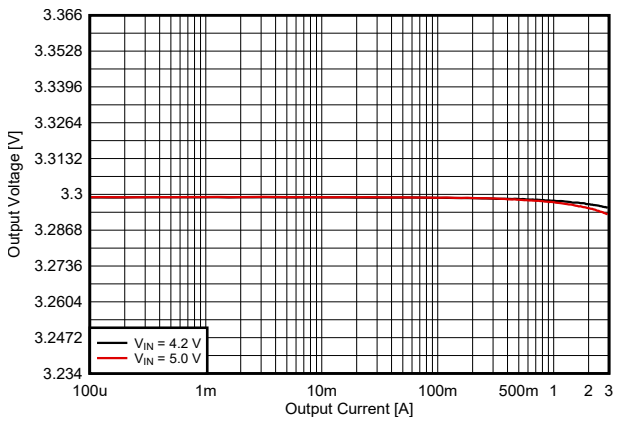
V_{OUT} = 2.5 V PWM

図 8-23. Output Voltage versus Output Current



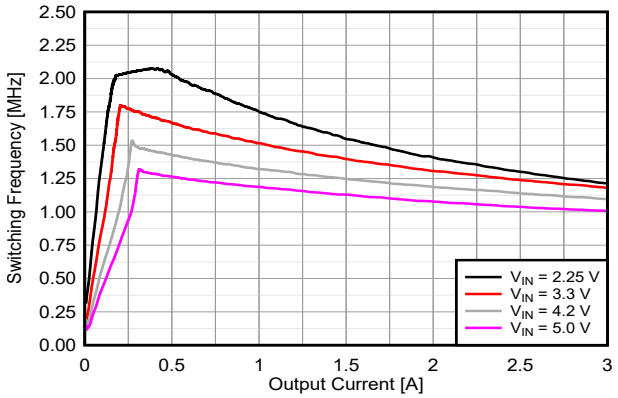
V_{OUT} = 3.3 V PFM

図 8-24. Output Voltage versus Output Current



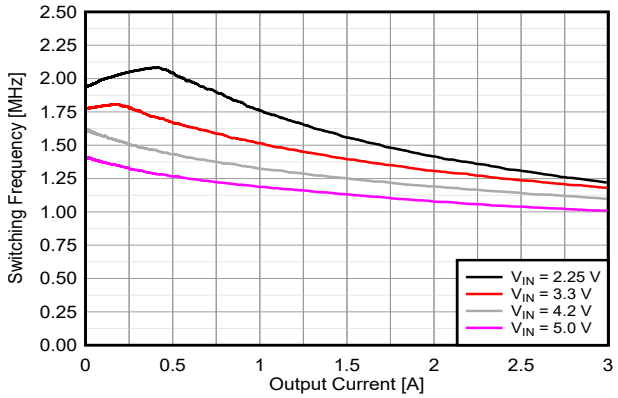
V_{OUT} = 3.3 V PWM

図 8-25. Output Voltage versus Output Current



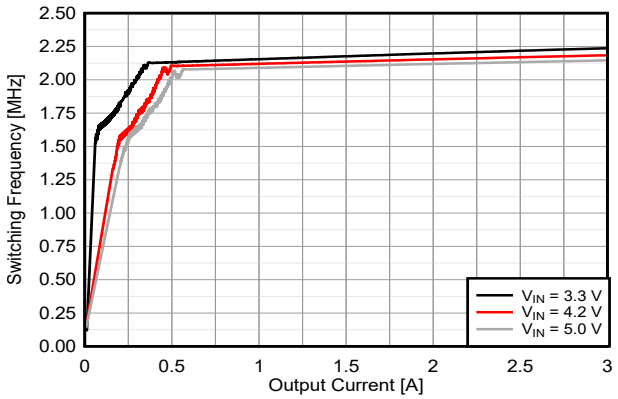
V_{OUT} = 0.5 V PFM

図 8-26. Switching Frequency versus Output Current



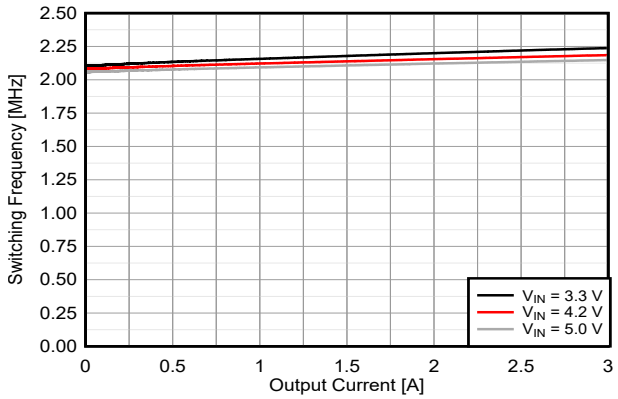
V_{OUT} = 0.5 V PWM

図 8-27. Switching Frequency versus Output Current



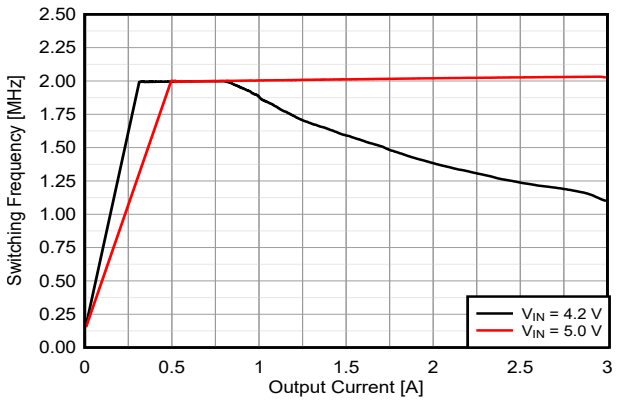
V_{OUT} = 1.8 V PFM

図 8-28. Switching Frequency versus Output Current



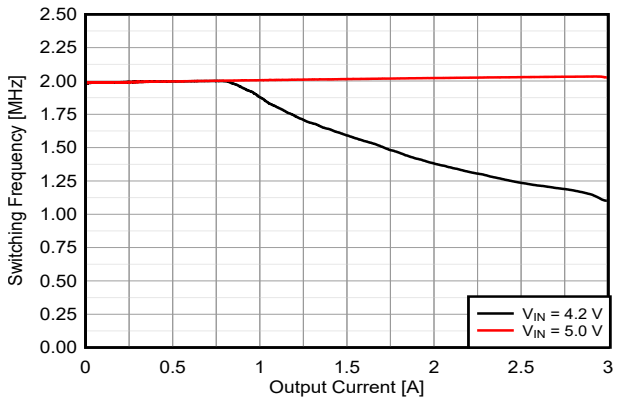
V_{OUT} = 1.8 V PWM

図 8-29. Switching Frequency versus Output Current



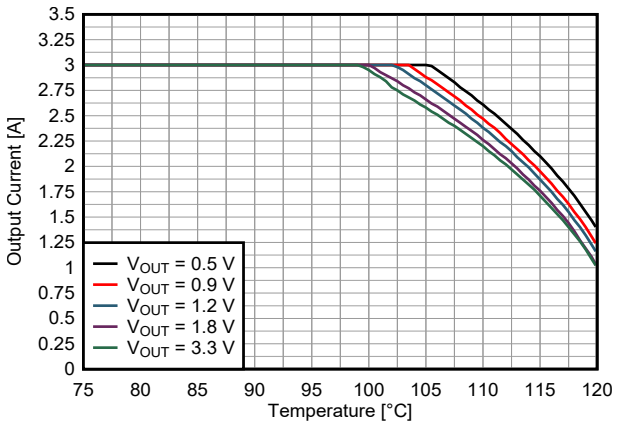
V_{OUT} = 3.3 V PFM

図 8-30. Switching Frequency versus Output Current



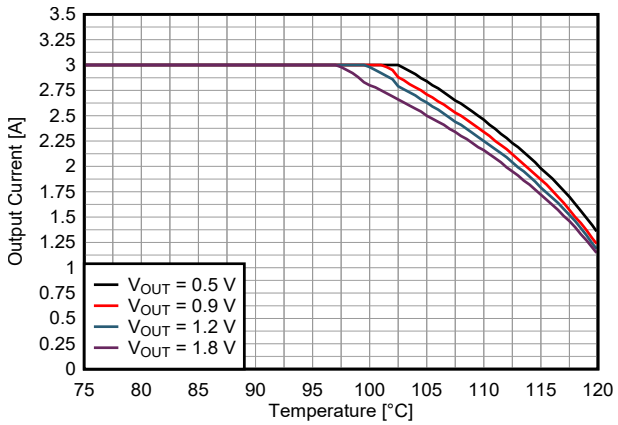
V_{OUT} = 3.3 V PWM

図 8-31. Switching Frequency versus Output Current



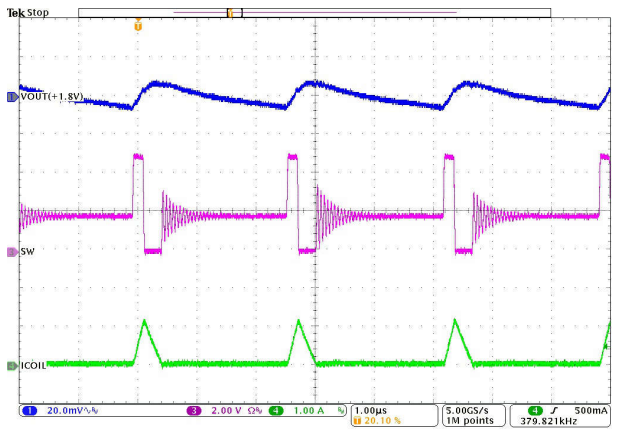
V_{IN} = 5.0 V T_{Jmax} = 125°C θ_{JA}= 49.8°C/W

図 8-32. Thermal Derating (Safe Operating Area)



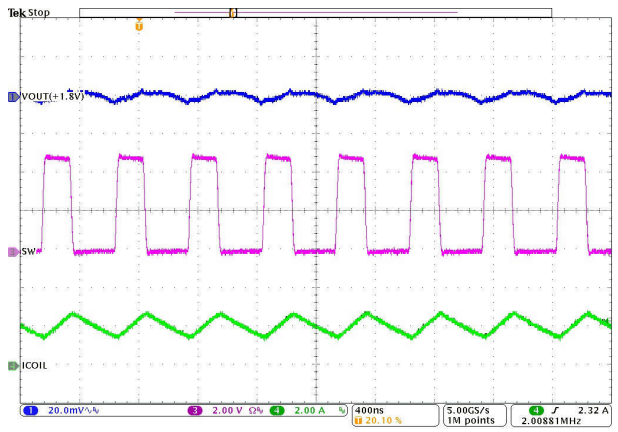
V_{IN} = 3.3 V T_{Jmax} = 125°C θ_{JA} = 49.8°C/W

図 8-33. Thermal Derating (Safe Operating Area)



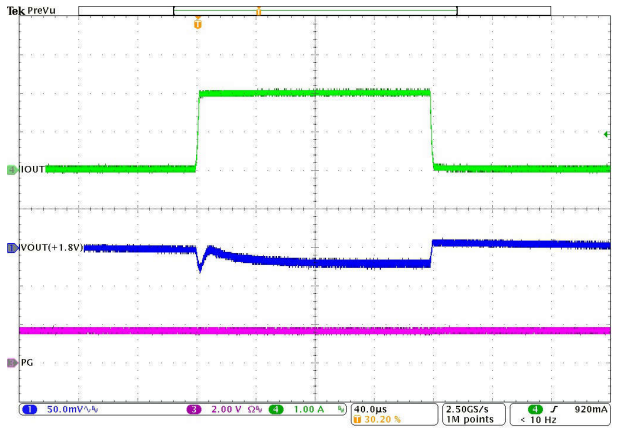
I_{OUT} = 100 mA PFM

図 8-34. Output Voltage Ripple



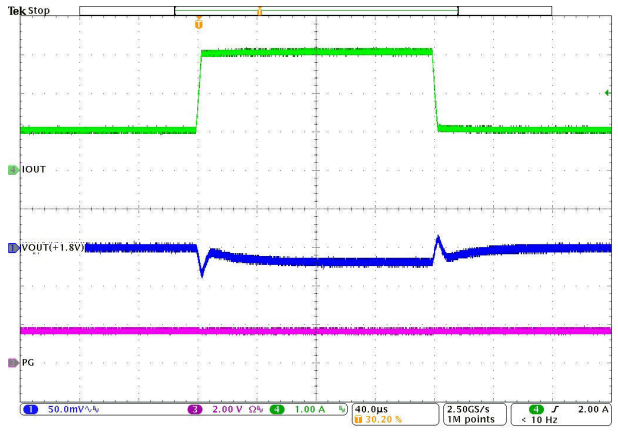
I_{OUT} = 2 A PWM

図 8-35. Output Voltage Ripple



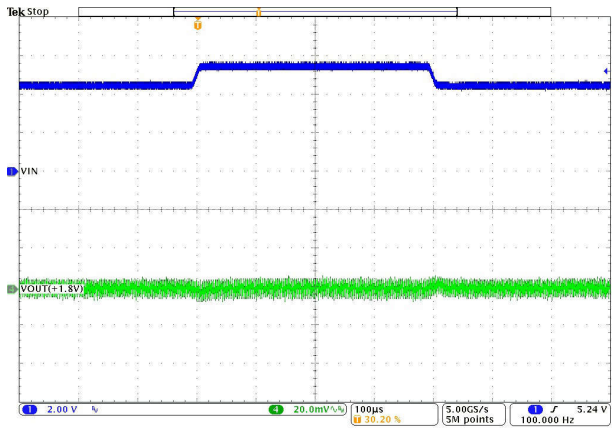
I_{OUT} = 1 mA to 2 A PFM Slew rate = 1 A/µs

図 8-36. Load Transient



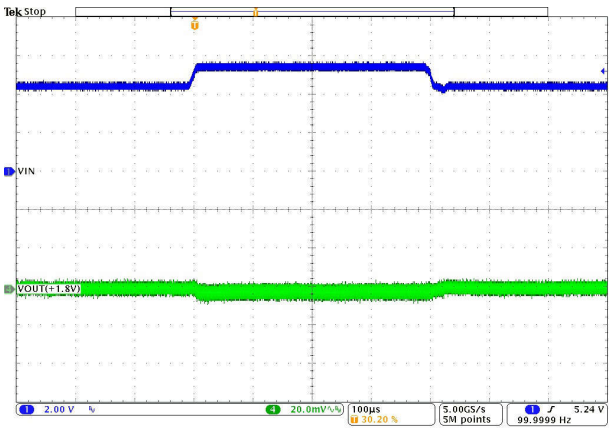
I_{OUT} = 0 mA to 1 A PWM Slew rate = 1 A/µs

図 8-37. Load Transient



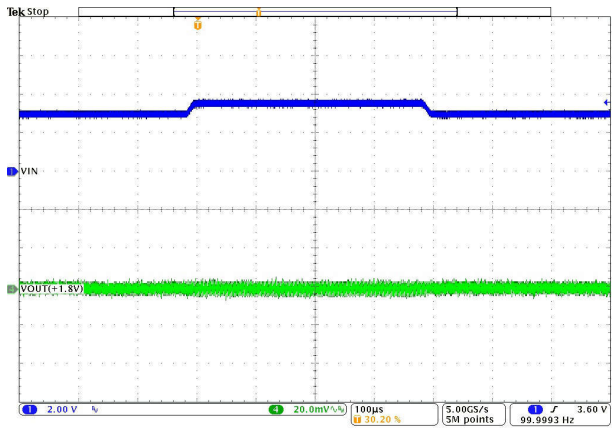
V_{IN} = 4.5 V to 5.5 V PFM I_{OUT} = 100 mA

図 8-38. Line Transient



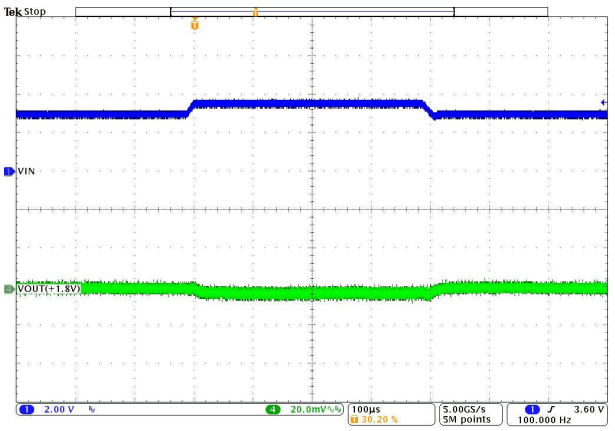
V_{IN} = 4.5 V to 5.5 V PFM or PWM I_{OUT} = 2 A

図 8-39. Line Transient



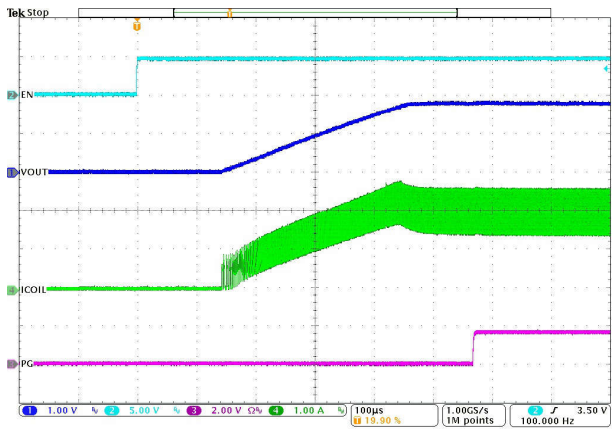
V_{IN} = 3.0 V to 3.6 V PFM I_{OUT} = 100 mA
V_{OUT} = 1.8 V

図 8-40. Line Transient



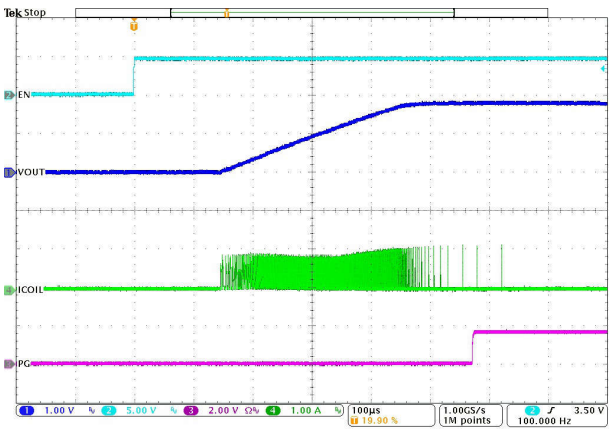
V_{IN} = 3.0 V to 3.6 V PFM or PWM I_{OUT} = 2 A
V_{OUT} = 1.8 V

図 8-41. Line Transient



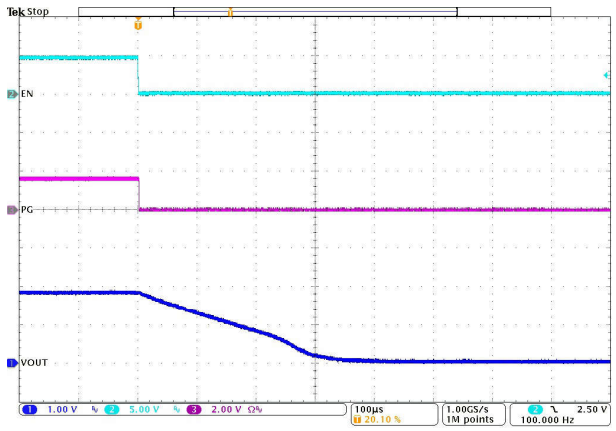
I_{OUT} = 2 A PFM or PWM

図 8-42. Start-Up With Load



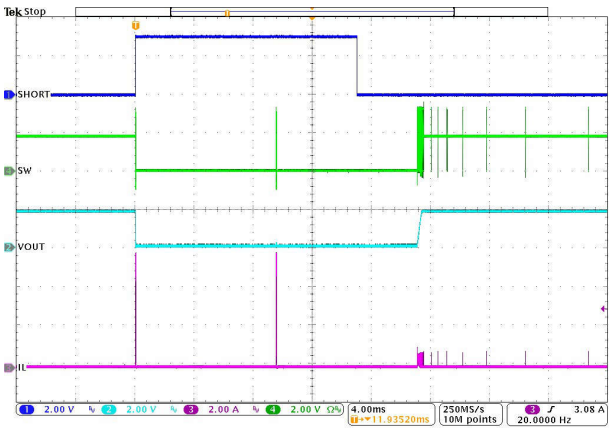
I_{OUT} = 0 mA PFM

図 8-43. Start-Up With No Load



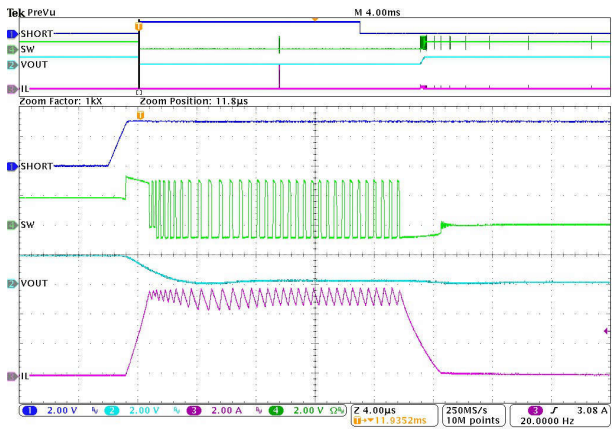
I_{OUT} = 0 mA PFM

図 8-44. Disable, Active Output Discharge at No Load



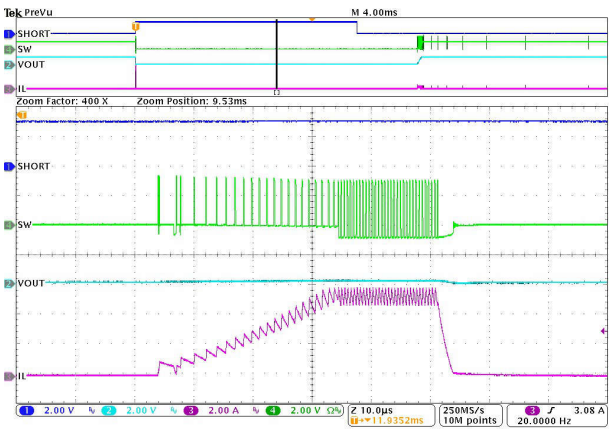
I_{OUT} = 1 A PFM or PWM

図 8-45. HICCUP Short-Circuit Protection



I_{OUT} = 1.0 A PFM or PWM

図 8-46. HICCUP Short-Circuit Protection (Zoom In)



I_{OUT} = 1.0 A PFM or PWM

図 8-47. HICCUP Short-Circuit Protection (Zoom In - Second Hiccup)

8.3 Power Supply Recommendations

The TPSM82830x family does not have special requirements for the input power supply and is designed to operate from an input voltage supply range from 2.25 V to 5.5 V. The output current of the input power supply must be rated according to the supply voltage, output voltage, and output current of the device.

8.4 Layout

8.4.1 Layout Guidelines

The printed-circuit-board (PCB) layout is an important step to maintain the high performance of the device. See *Layout Example* for the recommended low EMI PCB layout.

- Place the input and output capacitors as close as possible to the IC. This action keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
- Connect the low side of the input and output capacitors properly to the GND pin to avoid a ground potential shift.

- Take special care to avoid noise being induced. The sense traces connected to FB is a signal trace. Keep these traces away from SW nodes. The connection of the output voltage trace for the FB resistors must be made at the output capacitor.
- Refer to *Layout Example* for an example of component placement, routing, and thermal design with good EMI performance.

8.4.2 Layout Example

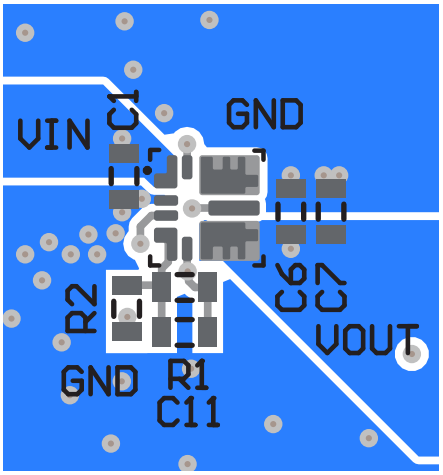


図 8-48. PCB Layout Recommendation (RDS Package)

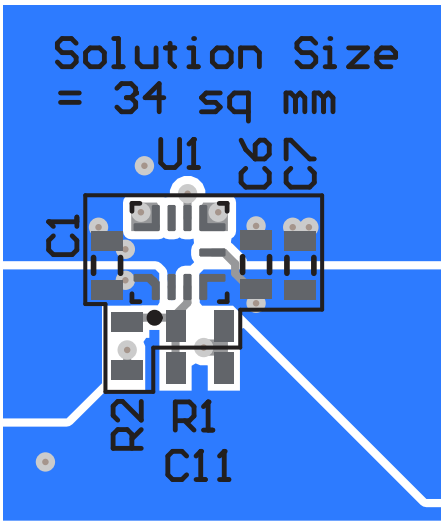


図 8-49. PCB Layout Recommendation (VCB Package)

8.4.2.1 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component.

Two basic approaches for enhancing thermal performance are:

- Improving the power dissipation capability of the PCB design
- Introducing airflow in the system

The Thermal Data section in *Thermal Information Module* provides the thermal metric of the device on the EVM after considering the PCB design of real applications. The big copper planes connecting to the pads of the IC on the PCB improve the thermal performance of the device. For more details on how to use the thermal parameters, see the Thermal Characteristics application notes, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.1.2 Development Support

9.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM82830x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application note

9.3 サポート・リソース

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9.5 静電気放電に関する注意事項

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9.6 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (December 2023) to Revision B (June 2024)	Page
• TPSM828303PVCBR (事前情報) を追加	1

Changes from Revision * (July 2023) to Revision A (December 2023)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

11 Mechanical, Packaging, and Orderable Information

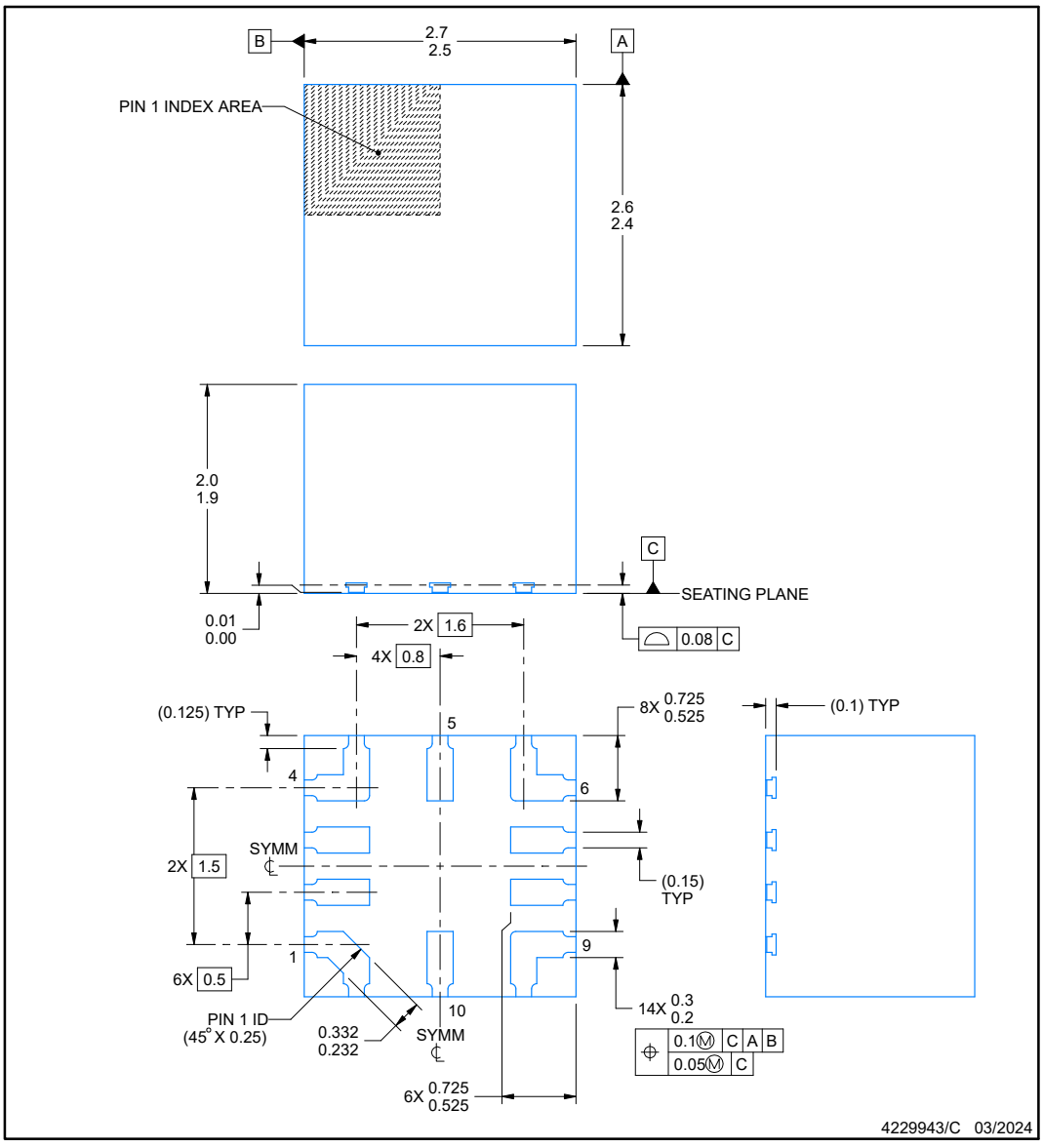
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

VCB0010A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

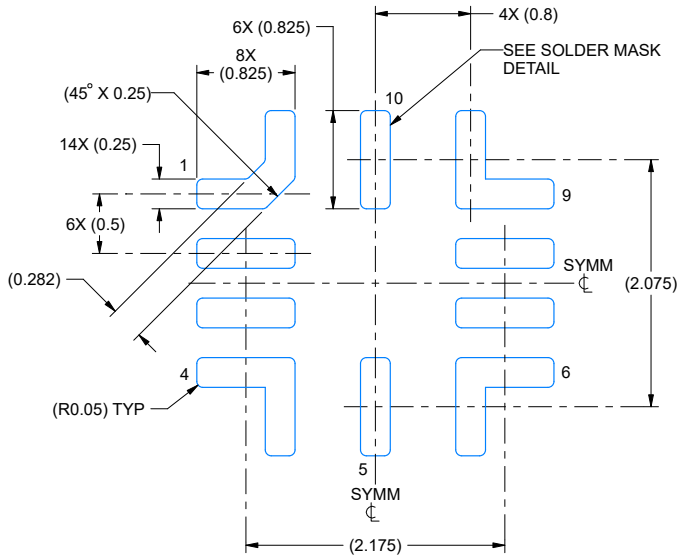
TEXAS INSTRUMENTS
www.ti.com

EXAMPLE BOARD LAYOUT

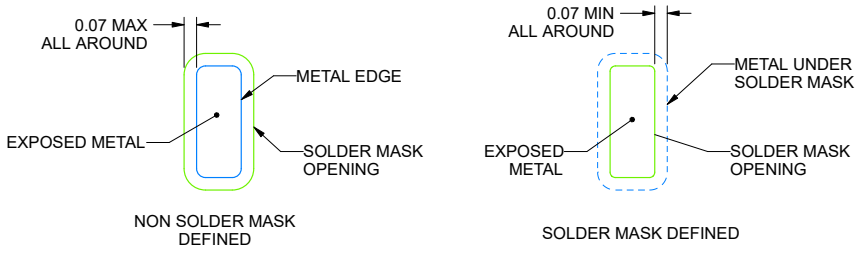
VCB0010A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4229943/C 03/2024

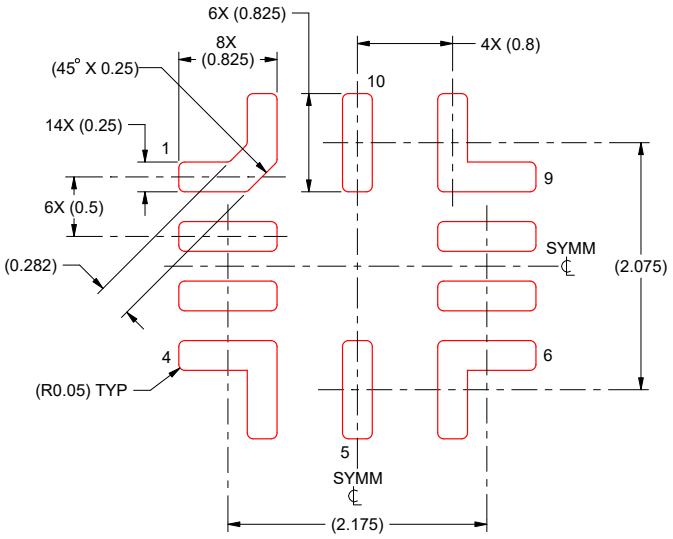
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

VCB0010A — **QFN-FCMOD - 2 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

4229943/C 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM828301ARDSR	ACTIVE	QFN-FCMOD	RDS	9	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	TM8301	Samples
TPSM828302ARDSR	ACTIVE	QFN-FCMOD	RDS	9	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	TM8302	Samples
TPSM828303ARDSR	ACTIVE	QFN-FCMOD	RDS	9	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 125	TM8303	Samples
XPSM828303PVCBR	ACTIVE	QFN-FCMOD	VCB	10	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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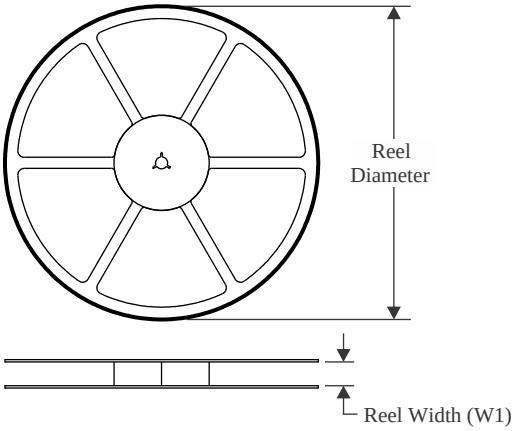
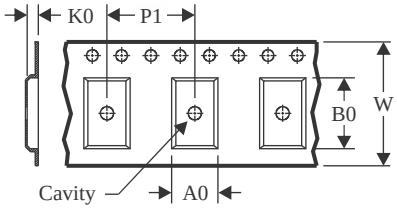
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

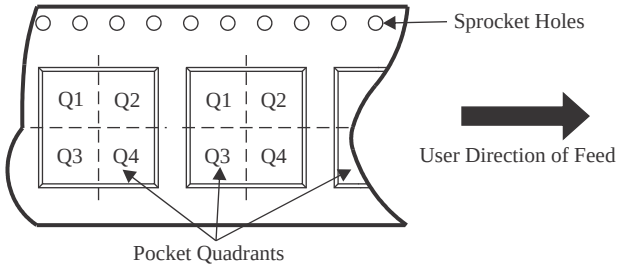


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

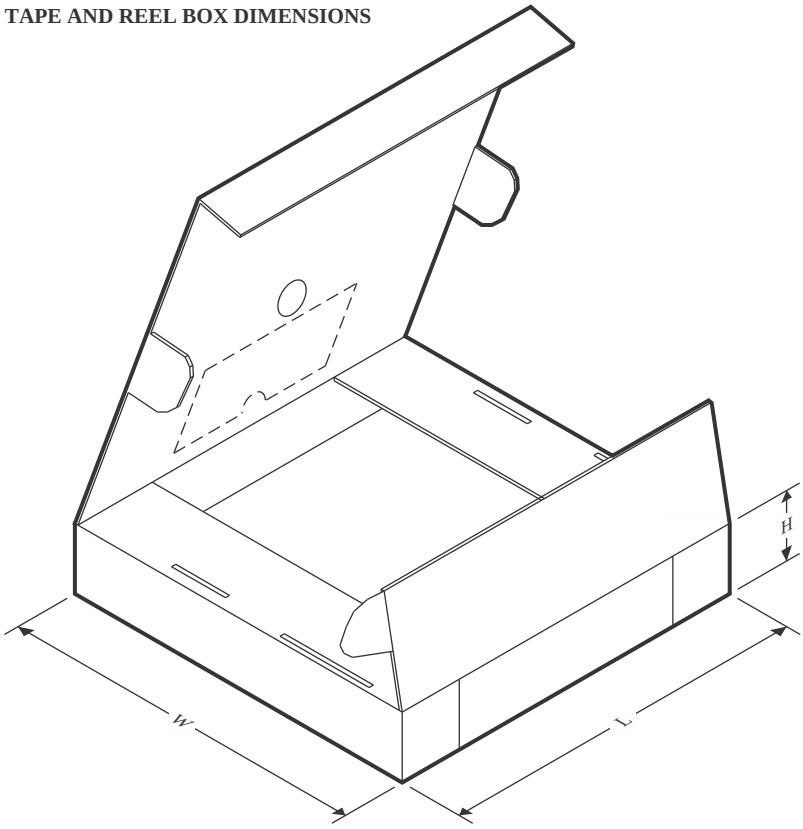
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM828301ARDSR	QFN-FCMOD	RDS	9	3000	330.0	17.6	3.3	3.3	2.25	8.0	12.0	Q2
TPSM828302ARDSR	QFN-FCMOD	RDS	9	3000	330.0	17.6	3.3	3.3	2.25	8.0	12.0	Q2
TPSM828303ARDSR	QFN-FCMOD	RDS	9	3000	330.0	17.6	3.3	3.3	2.25	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

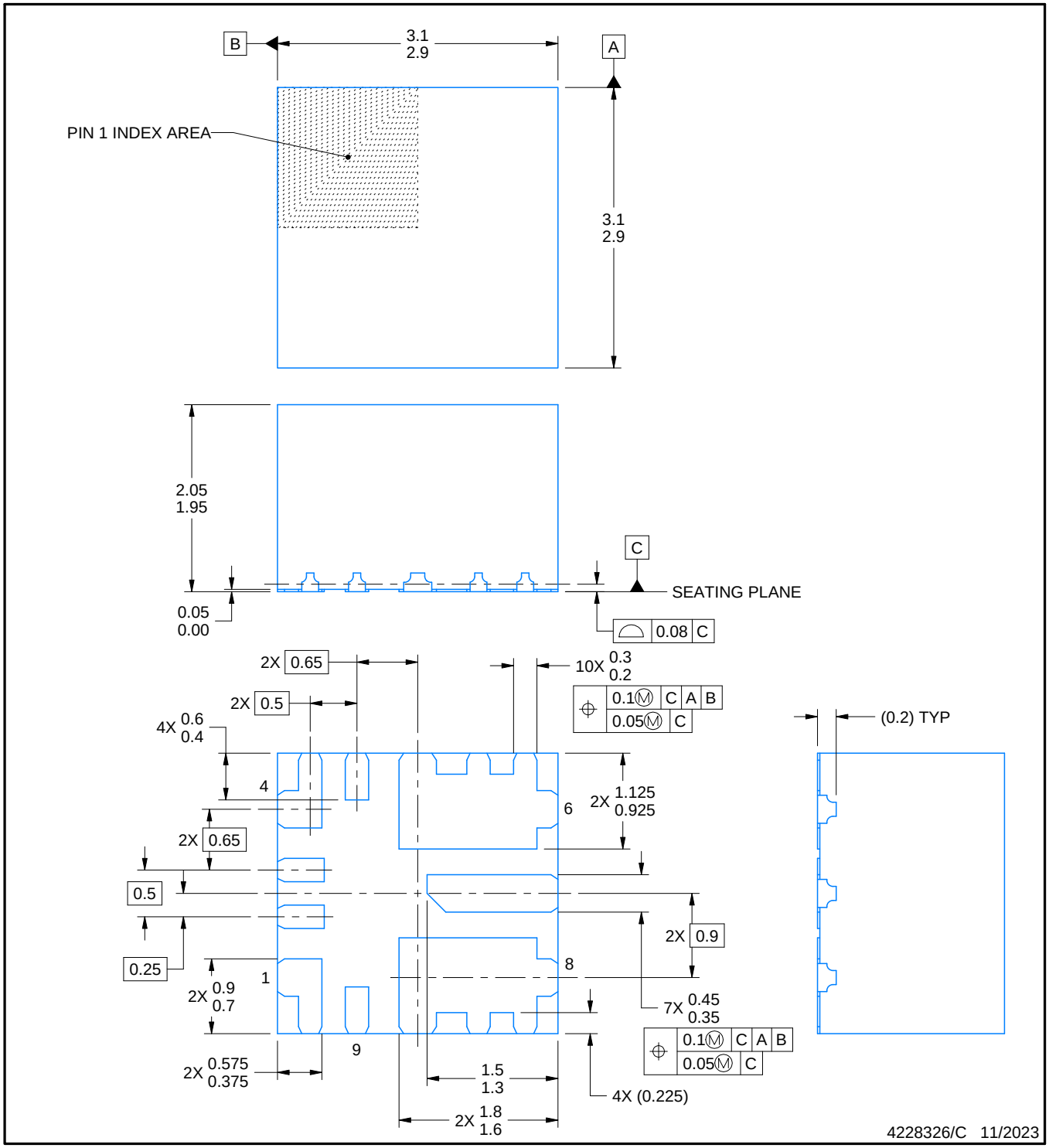
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM828301ARDSR	QFN-FCMOD	RDS	9	3000	336.0	336.0	48.0
TPSM828302ARDSR	QFN-FCMOD	RDS	9	3000	336.0	336.0	48.0
TPSM828303ARDSR	QFN-FCMOD	RDS	9	3000	336.0	336.0	48.0

PACKAGE OUTLINE

RDS0009A

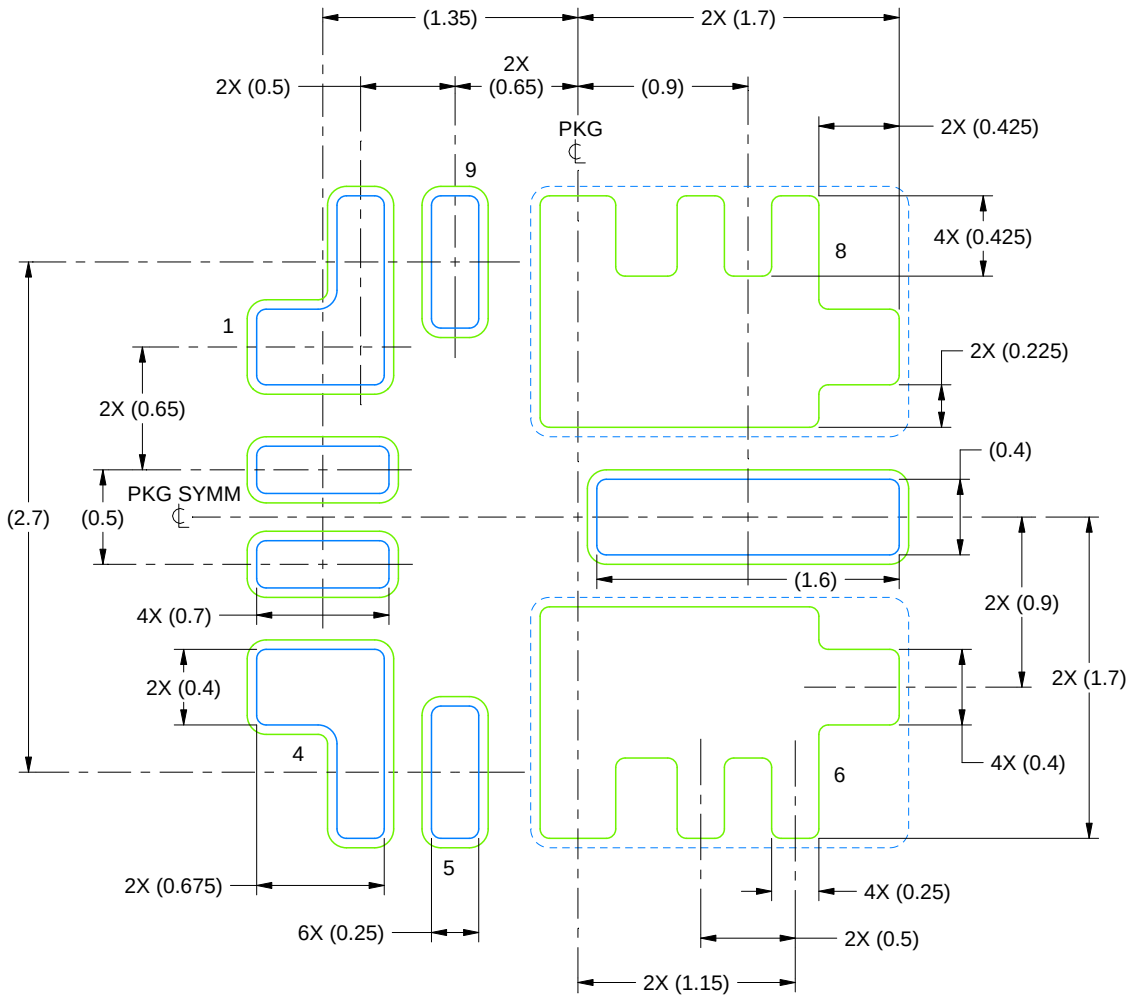
QFN-FCMOD - 2.05 mm max height

QUAD FLATPACK - NO LEAD

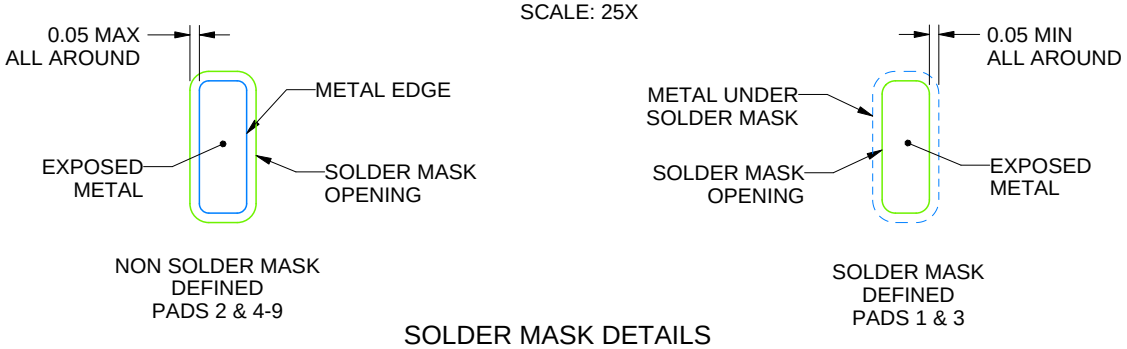


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE: 25X



SOLDER MASK DETAILS

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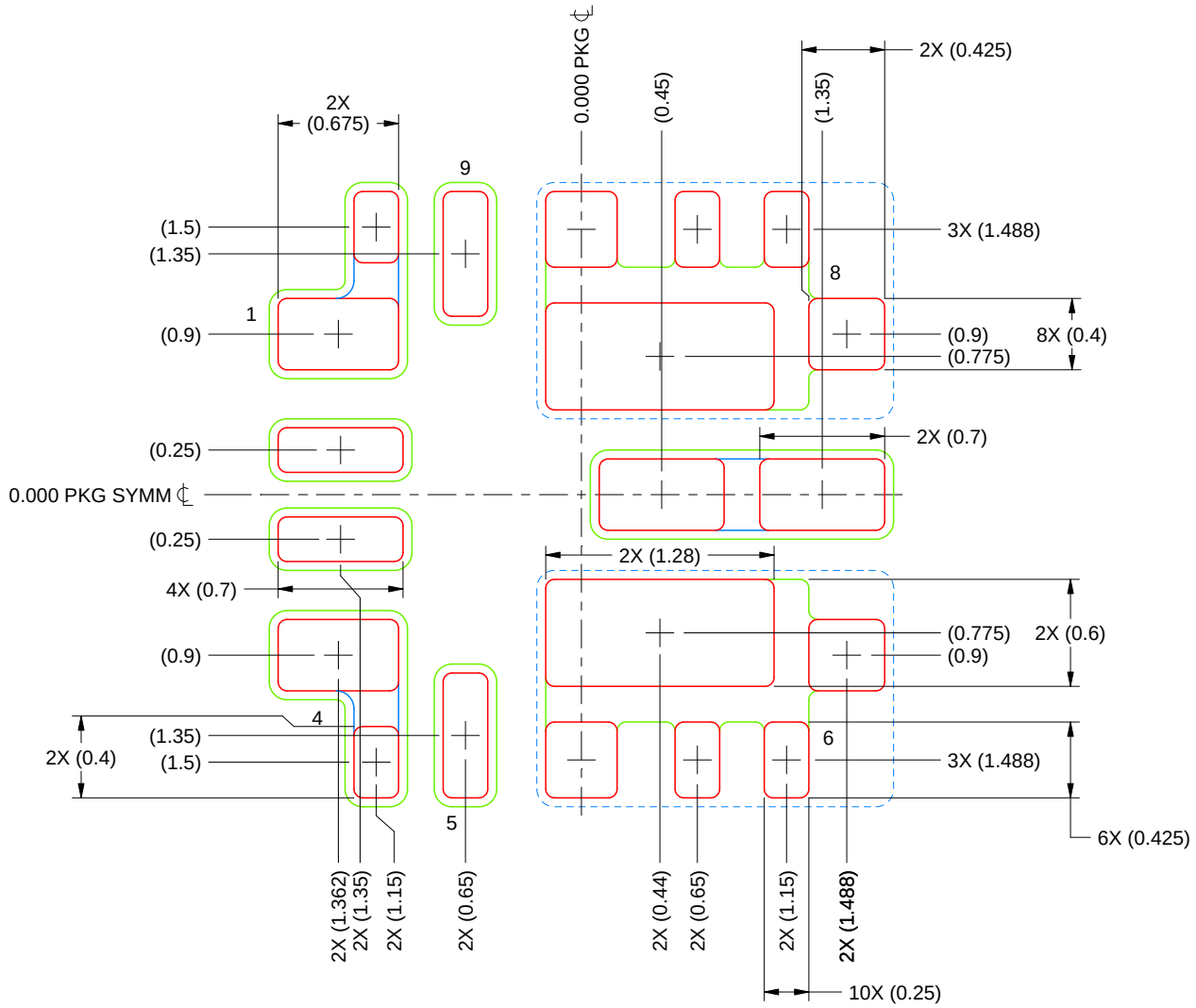
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 1 & 3: 76%
PADS 2, 5 & 8: 88%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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