

TPS7H1121-SP、2.25V~14V 入力、2A、耐放射線低ドロップアウト (LDO) リニアレギュレータ

1 特長

- 吸収線量放射線特性評価済み。
 - 放射線耐性保証 (RHA): 100krad(Si) または 50krad(Si)
- シングル イベント効果 (SEE) の特性
 - シングル イベント ラッチアップ (SEL)、シングル イベント バーンアウト (SEB)、シングル イベント ゲート ラプチャー (SEGR) の線エネルギー付与 (LET) = 75MeV-cm²/mg に対する耐性
 - LET = 75MeV-cm²/mg で、シングル イベント機能 割り込み (SEFI) 特性評価済み
 - LET = 75MeV-cm²/mg でシングル イベント過渡 (SET) 特性評価済み
- ワイド V_{IN} 範囲: 2.25V~14V
- 2A の最大出力電流
- 3V を超える V_{IN} の負荷および温度に対する精度: ±1.5%
- 3V 未満の V_{IN} の負荷および温度に対する精度: ±1.8%
- 外付けコンデンサによるソフトスタート (SS) 制御
- 電源シーケンス用、オープンドレインのパワー グッド (PG) 出力
- 外付け抵抗 (CL) でプログラム可能な電流制限
- STAB ピンを活用したオプションの外部制御ループ補償が可能
- 非常に優れた負荷 / ライン過渡応答
- ASTM E595 に準拠した脱ガス試験済みのプラスチック パッケージ
- 軍用温度範囲: -55°C~125°C

2 アプリケーション

- 衛星用電源システム (EPS)
- クリーンなアナログ電源要件
- コマンドとデータの処理 (C&DH)
- 光学画像処理ペイロード
- レーダー画像処理ペイロード

3 概要

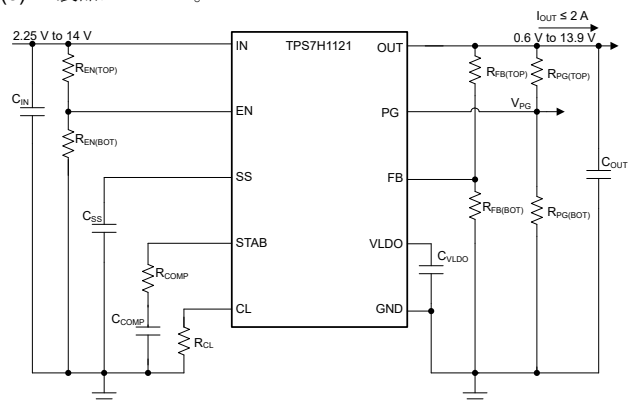
TPS7H1121 は、耐放射線特性をもった低ドロップアウトのリニアレギュレータ (LDO) で、広い入力電圧範囲で動作し、宇宙環境で使用されるデバイスへの電力供給に最適化されています。2.25V~14V の入力に対して、最大 2A の電流を供給できます。

このデバイスは安定性が優れており、広い範囲で調整可能な電流制限機能を搭載しています。FPGA、DSP、マイクロコントローラの複雑な電力要件に対応するため、TPS7H1121 にはイネーブル オンおよびオフ機能、ソフトスタートのプログラム機能、パワー グッドのオープンドレイン出力が搭載されています。

製品情報

部品番号 (1)	グレード	パッケージ (2)
5962R2320301VXC	QMLV-RHA	22 ピン セラミック
TPS7H1121HFT/EM	エンジニアリング サンプル	6.21mm×7.69mm 質量 = 415.6mg
5962R2320302PYE (3)	QMLP-RHA	24 ピン プラスチック
TPS7H1121MPWPTSEP (3)	SEP	4.40mm x 7.80mm 質量は未定

- 詳細は、「デバイス オプション」表をご覧ください。
- 寸法と質量の値は公称値です。
- 製品プレビュー。



代表的なアプリケーション回路



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4 Device Options

GENERIC PART NUMBER	RADIATION RATING ⁽¹⁾	GRADE ⁽²⁾	PACKAGE	ORDERABLE PART NUMBER
TPS7H1121-SP	TID of 100krad(Si) RLAT, DSEE free to 75MeV-cm ² /mg	QMLV-RHA	22-pin CFP HFT	5962R2320301VXC
		QMLP-RHA	24 pin HTSSOP PWP	5962R2320302PYE ⁽⁴⁾
	None	Engineering model ⁽³⁾	22-pin CFP HFT	TPS7H1121HFT/EM
TPS7H1121-SEP	TID of 50krad(Si) RLAT, DSEE free to 43MeV-cm ² /mg	Space Enhanced Plastic	24 pin HTSSOP PWP	TPS7H1121MPWPTSEP ⁽⁴⁾

- (1) TID is total ionizing dose and DSEE is destructive single event effects. Additional information is available in the associated TID reports and SEE reports for each product.
- (2) For additional information about part grade, view [SLYB235](#).
- (3) These units are intended for engineering evaluation only. They are processed to a non-compliant flow (such as no burn-in and only 25°C testing). These units are not suitable for qualification, production, radiation testing, or flight use. Parts are not warranted as to performance over temperature or operating life.
- (4) Product preview.

5 Pin Configuration and Functions

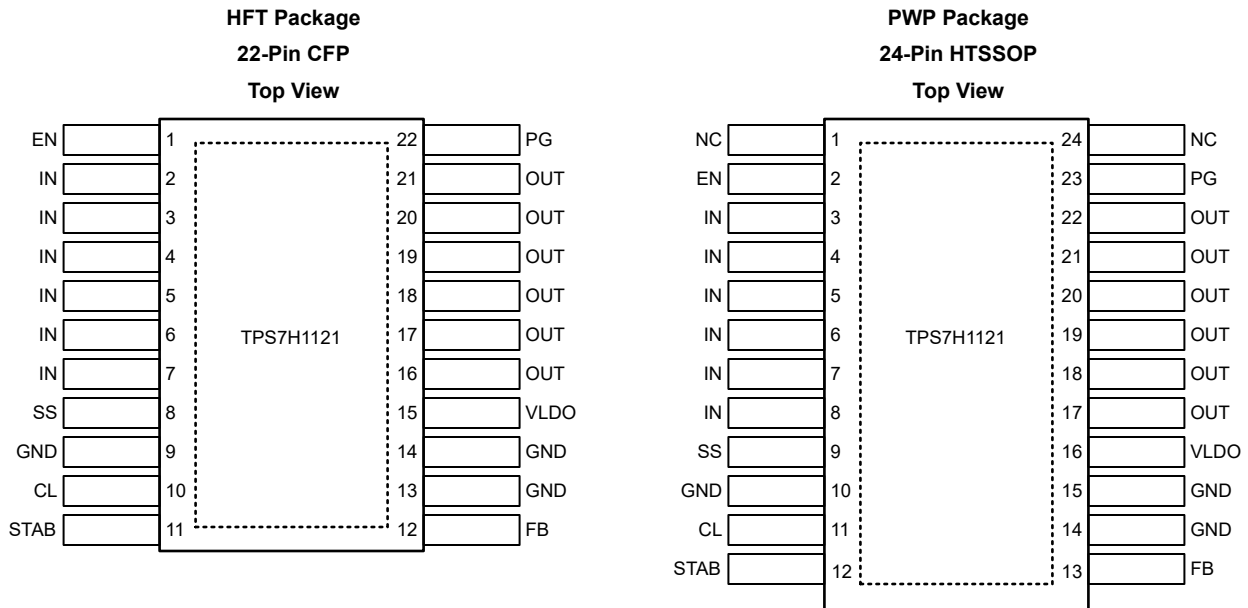


表 5-1. Pin Functions

NAME	PIN		I/O	DESCRIPTION
	HFT (22) NO.	PWP (24) NO.		
EN	1	2	I	Enable. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device. If enable functionality is not required, connect this pin to IN using a resistor divider network, see セクション 8.3.2 . Do not float this pin.
IN	2, 3, 4, 5, 6, 7	3, 4, 5, 6, 7, 8	I	Input power. An input capacitor (nominally 10 μ F) near this pin is recommended.
SS	8	9	I/O	Soft-start. A minimum 1nF capacitor is required to prevent excessive inrush currents.
GND	9, 13, 14	10, 14, 15	—	Ground
CL	10	11	I	Programmable current limit. A resistor to GND sets the over-current limit activation point. The range of resistor that can be used on the CL terminal to GND is 41.2k Ω to 442k Ω .
STAB	11	12	I/O	Stability pin. This is an output from the internal OTA (operational transconductance) error amplifier to aid in measuring or optimizing the control loop. Standard compensation networks can be applied to the STAB (see セクション 8.3.9.1); however, an output capacitance of 22 μ F to 220 μ F typically achieve high stability margins.
FB	12	13	I	The output voltage feedback input through voltage dividers. See セクション 8.3.1 .
NC	—	1, 24	—	No connect. This pin is not internally connected. It is recommended to connect these pins to GND to prevent charge buildup; however, these pins can also be left open or tied to any voltage between GND and V_{IN} .
VLDO	15	16	O	Output of internal linear regulator, requires a 470nF capacitor connected to ground.
OUT	16, 17, 18, 19, 20, 21	17, 18, 19, 20, 21, 22	O	Output power pin. The regulated output voltage. A single 47 μ F tantalum or tantalum polymer capacitor is recommended. Capacitance values between 22 μ F and 220 μ F are generally supported without additional compensation and wider ranges are supported with use of the STAB pin. See セクション 9.2.2.8 for additional information.
PG	22	23	I/O	Power good indicator. This is an open drain pin. Use a pull-up resistor or a resistor divider (to ensure pin voltage does not exceed 7V) to achieve desired logic level when tied to V_{OUT} . It is recommend to pull down PG to ground if left unused, the PG pin can be left floating if necessary. When the output reaches 95% (typ) of the set output voltage the PG pin is asserted.
Thermal pad	—	—	—	Internally grounded. It is recommended to connect this metal thermal pad to a large ground plane for effective heat dissipation.

表 5-1. Pin Functions (続き)

PIN			I/O	DESCRIPTION
NAME	HFT (22) NO.	PWP (24) NO.		
Metal lid	Lid	N/A	—	The lid is internally connected to the thermal pad and GND through the seal ring.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage	IN, STAB	-0.3	16	V
	EN, PG	-0.3	7.5	
	FB, CL	-0.3	3.3	V
Output voltage	OUT	-0.6	16	V
	VLDO	-0.3	3.6	
	SS	-0.3	3.3	V
Input current	PG	-0.001	0.01	A
Output current	OUT	-3.9	3.9	A
Junction temperature	T _J	-55	150	°C
Storage temperature	T _{stg}	-65	150	

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	IN	2.25		14	V
	EN	0		7	
	PG	0		7	
Output voltage	OUT	0.6	$V_{IN} - V_{DO}$		V
	SS	0		1.2	
Input current	PG	0		2	mA
Output current	OUT	0		2	A
Junction temperature	T_J	-55		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7H1121-SP	TPS7H1121-SP, -SEP	UNIT
		CFP HFT	PWP (HTSSOP)	
		22 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	26.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	13.3	18	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.5	7.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	5	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.3	7.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	0.9	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

Over $2.25V \leq V_{IN} \leq 14V$, $V_{OUT(set)} \leq V_{IN} - 0.5V$, $I_{OUT} = 10mA$, $C_{OUT} = 47\mu F$, over operating temperature range ($T_A = -55^\circ C$ to $125^\circ C$), typical values are at $T_A = 25^\circ C$, unless otherwise noted; includes RLAT at $T_A = 25^\circ C$ if sub-group number is present for QML RHA and SEP devices⁽²⁾

PARAMETER		Test Conditions		SUB-GROUP ⁽¹⁾	MIN	TYP	MAX	UNIT		
POWER SUPPLIES AND CURRENTS										
V_{DO}	Dropout voltage, see 7-1	$V_{OUT(set)} = 2.25V$ $V_{OUT(measured)} = 98\% \times V_{OUT(NOM)}$	$I_{OUT} = 100mA$	1,2,3		28	60	mV		
			$I_{OUT} = 250mA$	1,2,3		70	141			
			$I_{OUT} = 500mA$	1,2,3		150	280			
			$I_{OUT} = 1A$	1,2,3		300	570			
		$V_{OUT(set)} = 2.5V$ $V_{OUT(measured)} = 98\% \times V_{OUT(NOM)}$	$I_{OUT} = 1.5A$	1,2,3		525	750			
			$I_{OUT} = 2A$	1,2,3		570	900			
		$3V \leq V_{OUT(set)} \leq 13.3V$ $V_{OUT(measured)} = 98\% \times V_{OUT(NOM)}$	$I_{OUT} = 100mA$	1,2,3		20	50			
			$I_{OUT} = 250mA$	1,2,3		70	100			
			$I_{OUT} = 500mA$	1,2,3		125	180			
			$I_{OUT} = 1A$	1,2,3		300	340			
				$I_{OUT} = 1.5A$	1,2,3		325		490	
				$I_{OUT} = 2A$	1,2,3		500		700	
I_{PCL}	Programmed current limit	$V_{IN} = 3.3V$, $V_{OUT(short)} = 0.1V$	$RCL = 442k\Omega$	1,2,3	0.19	0.320	0.45	A		
			$RCL = 174k\Omega$	1,2,3	0.485	0.75	1.01			
			$RCL = 82.5k\Omega$	1,2,3	1.16	1.55	1.94			
			$RCL = 41.2k\Omega$	1,2,3	2.4	3	3.6			
I_Q	Quiescent current	$V_{EN} = 7V$, $I_{OUT} = 0A$		1,2,3		8.75	15	mA		
I_{GND} ($I_{IN} - I_{OUT}$)	Ground current	$V_{EN} = 7V$	$I_{OUT} = 1A$	1,2,3		10	18	mA		
			$I_{OUT} = 2A$	1,2,3		13	20			
V_{LDO}	Internal linear regulator output voltage	$V_{IN} = 2.25V$		1,2,3	2.05	2.2	2.25	V		
		$3V \leq V_{IN} \leq 14V$		1,2,3	2.30	2.55	2.78			
I_{SHDN}	Shutdown current	$V_{EN} = 0V$, $I_{OUT} = 0A$, $V_{OUT} = 0V$		1,2,3		380	775	μA		
I_{FB}	Feedback leakage current	$V_{FB} = 0.7V$		1,2,3		1	15	nA		
ACCURACY										
V_{ACC}	Output voltage accuracy	$10mA \leq I_{OUT} \leq 2A$, $0.6V \leq V_{OUT} \leq V_{IN} - V_{DO}$, $P_D \leq 3W$ ⁽³⁾	$3V \leq V_{IN} \leq 14V$	1,2,3	-1.5%		1.5%			
			$3V \leq V_{IN} \leq 14V$ $T_A = 25^\circ C$	1	-1.1%		1.1%			
			$2.25V \leq V_{IN} \leq 3V$	1,2,3	-1.8%		1.8%			
V_{FB}	Feedback voltage	$3V \leq V_{IN} \leq 14V$		1,2,3	0.588	0.596	0.606	V		
			$T_A = 25^\circ C$	1	0.591	0.596	0.603			
			$2.25V \leq V_{IN} \leq 3V$	1,2,3	0.586	0.596	0.608			
$\Delta V_{OUT} / \Delta V_{IN}$	Line regulation, see 7-2	$3V \leq V_{IN} \leq 14V$		1,2,3		100	650	$\mu V/V$		
			$2.25V \leq V_{IN} \leq 3V$	1,2,3		285	1800			
$\Delta V_{OUT} / \Delta I_{OUT}$	Load Regulation, see 7-3	$10mA \leq I_{OUT} \leq 2A$, $V_{IN} = 5V$, $V_{OUT} = 3.3V$		1,2,3		4	16	mV/A		
ENABLE										
$V_{EN(rising)}$	Enable rising threshold (turn-on)			1,2,3	0.565	0.605	0.625	V		
$V_{EN(falling)}$	Enable falling threshold (turn-off)			1,2,3	0.465	0.5	0.52	V		
$t_{EN(delay)}$	EN propagation delay	EN high to $V_{OUT} = 10mV$		9,10,11		50	150	μs		

6.5 Electrical Characteristics (続き)

Over $2.25V \leq V_{IN} \leq 14V$, $V_{OUT(\text{set})} \leq V_{IN} - 0.5V$, $I_{OUT} = 10\text{mA}$, $C_{OUT} = 47\mu\text{F}$, over operating temperature range ($T_A = -55^\circ\text{C}$ to 125°C), typical values are at $T_A = 25^\circ\text{C}$, unless otherwise noted; includes RLAT at $T_A = 25^\circ\text{C}$ if sub-group number is present for QML RHA and SEP devices⁽²⁾

PARAMETER		Test Conditions		SUB-GROUP ⁽¹⁾	MIN	TYP	MAX	UNIT
$I_{EN(LKG)}$	Enable leakage current	$V_{EN} = 7V$		1,2,3		1	30	nA
T_{SD}	Thermal shutdown enter temperature					160		$^\circ\text{C}$
T_{SD}	Thermal shutdown exit temperature					130		$^\circ\text{C}$
POWER GOOD								
V_{PG_RISE}	Power good rising as percent of V_{OUT}			1,2,3	93%	95%	97%	
V_{PG_FALL}	Power good falling as percent of V_{OUT}			1,2,3	88.5%	91.5%	94%	
$V_{PG(OL)}$	Power good output low	$I_{PG(SINK)} = 2\text{mA}$		1,2,3		90	190	mV
$V_{IN(MIN_PG)}$	Minimum V_{IN} for valid PG ($V_{PG} < 0.5V$)	$I_{PG(SINK)} = 0.5\text{mA}$		1,2,3		0.6	0.8	V
$I_{PG(LKG)}$	Power good leakage	$V_{PG} = 7V$, $V_{FB} = 0.7V$		1,2,3		0.05	2	μA
SOFT START								
I_{SS}	Soft-start current			1,2,3	1.4	2	2.7	μA
t_{SS}	Soft-start time	$V_{IN} = 5V$, $V_{OUT} = 3.3V$, measured from $V_{OUT} = 10\text{mV}$ to PG assert	$C_{SS} = 1\text{nF}$	9,10,11	0.22	0.35	0.48	ms
			$C_{SS} = 33\text{nF}$	9,10,11	5.5	10	14.5	
STABILITY								
GM	Gain Margin	$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $I_{OUT} = 1A$, $C_{OUT} = 47\mu\text{F}$, $T_A = 25^\circ\text{C}$, No External Compensation				24		dB
PM	Phase Margin					60°		
NOISE AND PSRR								
PSRR	Power-supply rejection ratio	$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $I_{OUT} = 1A$, $C_{SS} = 5.6\text{nF}$	$f_{\text{ripple}} = 100\text{Hz}$			68		dB
			$f_{\text{ripple}} = 1\text{kHz}$			72		
			$f_{\text{ripple}} = 10\text{kHz}$			51		
			$f_{\text{ripple}} = 100\text{kHz}$			40		
			$f_{\text{ripple}} = 1\text{MHz}$			34		
V_N	Output noise voltage (bandwidth from 10Hz to 100kHz)	$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $I_{OUT} = 1A$, $C_{SS} = 5.6\text{nF}$				35		μV_{RMS}

(1) Subgroups are applicable for QML parts. For subgroup definitions see [セクション 6.6](#).

(2) See the [5962R23203 SMD](#) for additional information on the QML RHA devices.

(3) P_D is the internal power dissipation. When P_D exceeds 3W, the current is lowered to avoid excessive local heating (due to tester limitations).

6.6 Quality Conformance Inspections

MIL-STD-883, Method 5005 - Group A

SUBGROUP	DESCRIPTION	TEMPERATURE (°C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Dynamic tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55

6.7 Typical Characteristics

$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $T_A = 25^\circ C$ and $C_{SS} = 5.6nF$, $C_{OUT} = 47\mu F$ (TBME476K025LBC0), when used, the external compensation network is applied as depicted in [セクション 8.2](#), no R_{COMP} , no C_{Comp} unless otherwise noted.

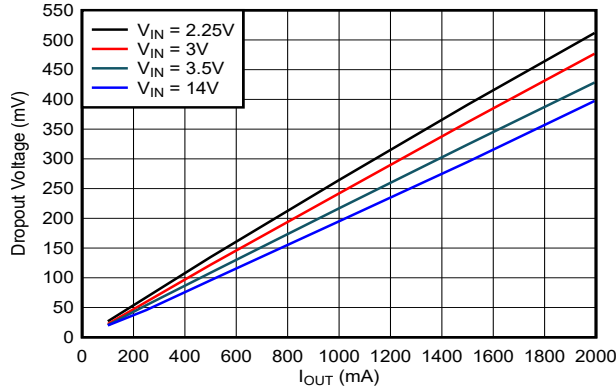
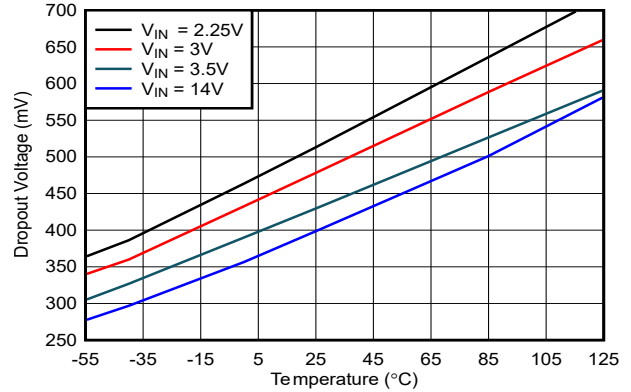
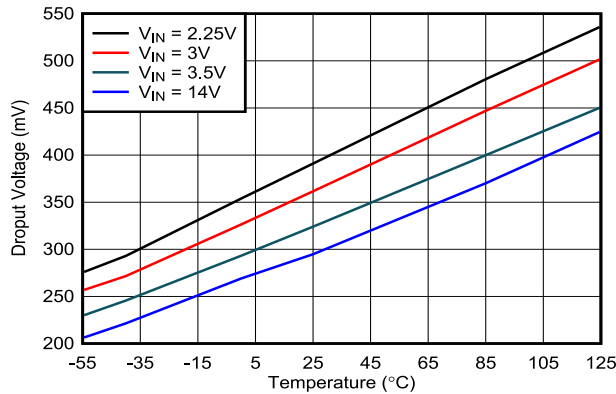


図 6-1. Dropout Voltage vs Current



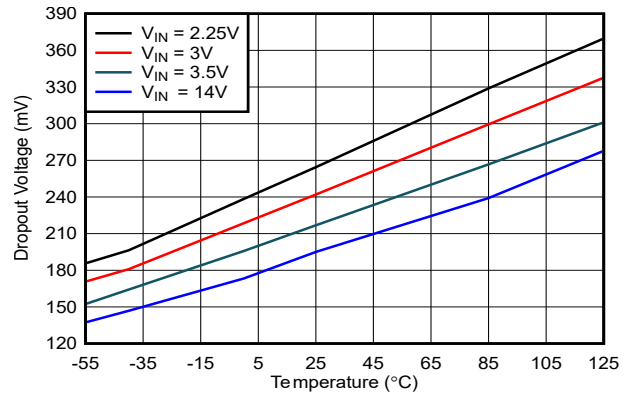
$I_{Load} = 2000mA$

図 6-2. Dropout Voltage vs Temperature



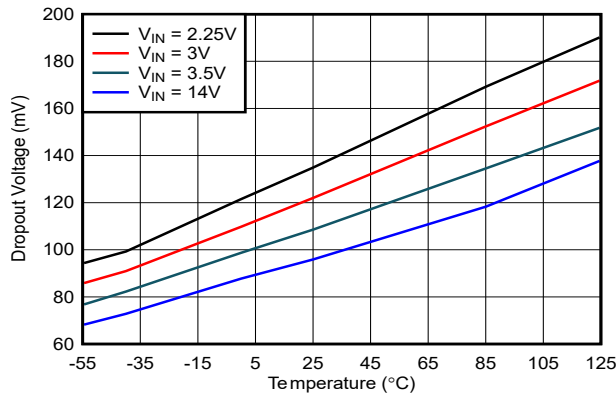
$I_{Load} = 1500mA$

図 6-3. Dropout Voltage vs Temperature



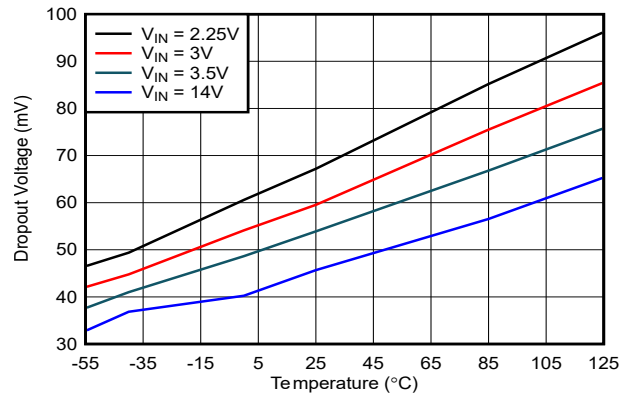
$I_{Load} = 1000mA$

図 6-4. Dropout Voltage vs Temperature



$I_{Load} = 500mA$

図 6-5. Dropout Voltage vs Temperature

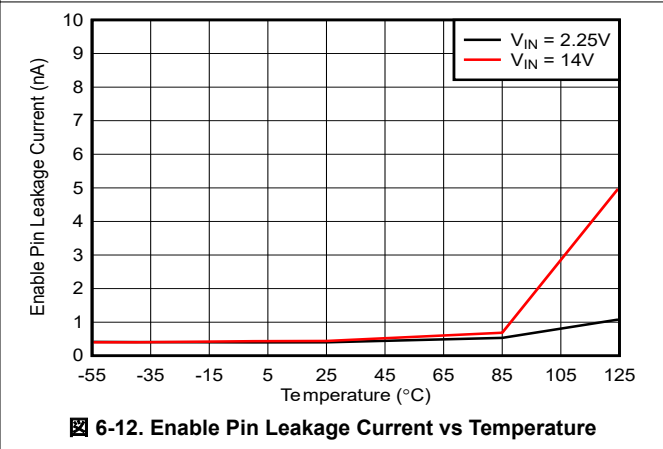
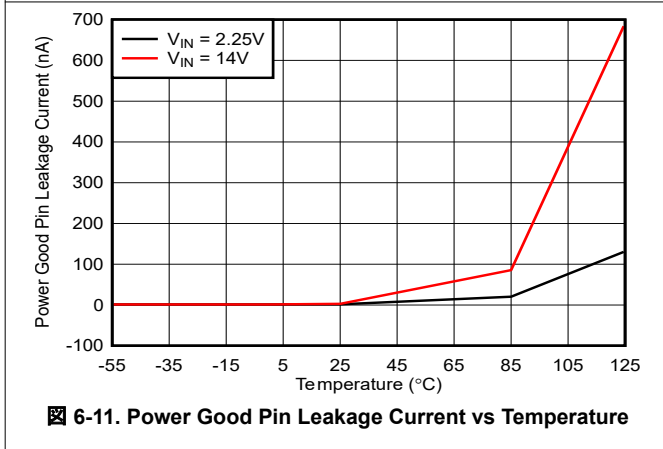
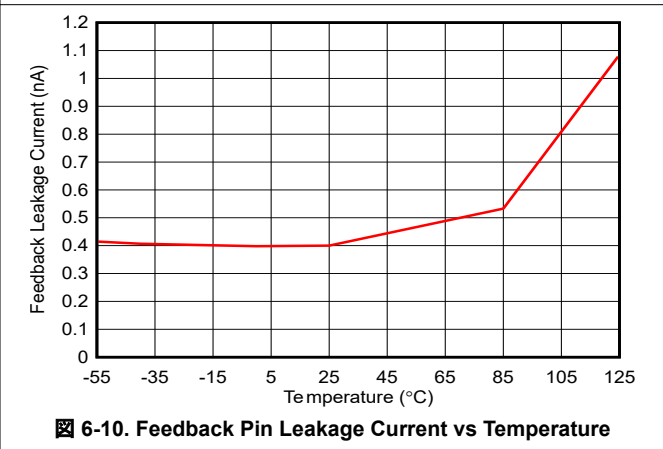
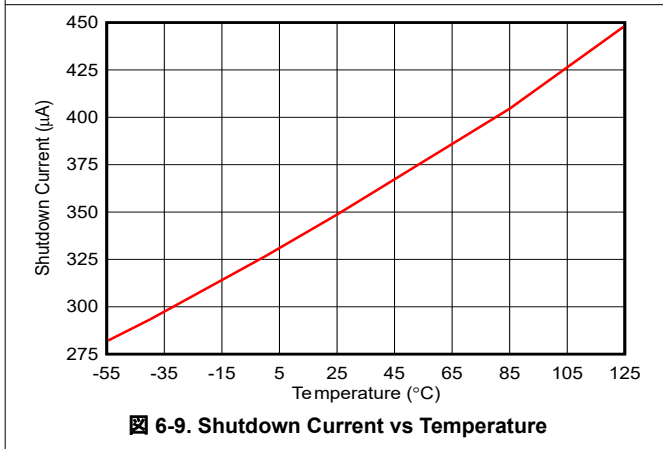
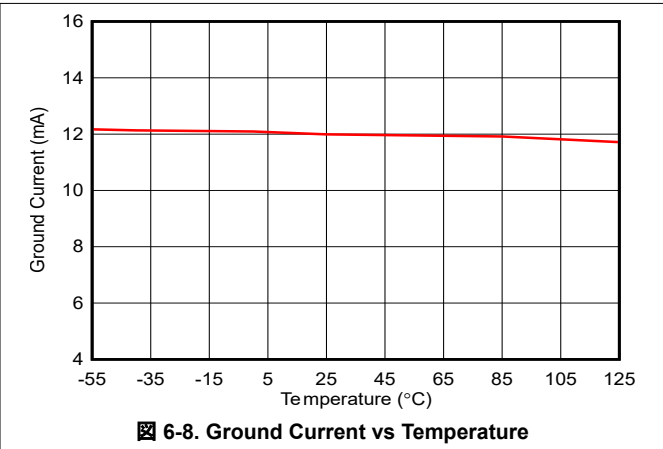
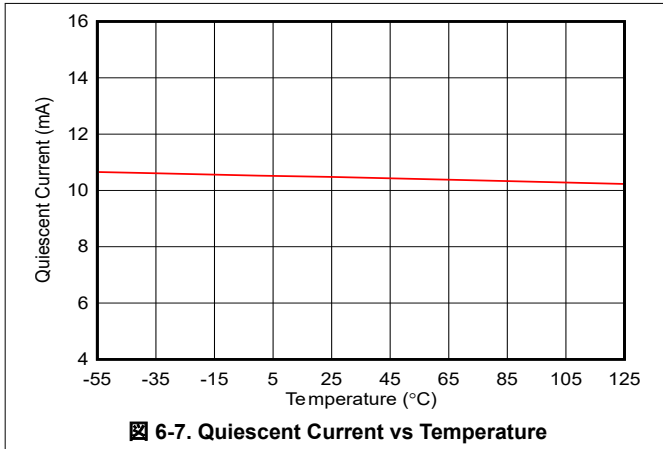


$I_{Load} = 250mA$

図 6-6. Dropout Voltage vs Temperature

6.7 Typical Characteristics (continued)

$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $T_A = 25^\circ C$ and $C_{SS} = 5.6nF$, $C_{OUT} = 47\mu F$ (TBME476K025LBC0), when used, the external compensation network is applied as depicted in [セクション 8.2](#), no R_{COMP} , no C_{Comp} unless otherwise noted.



6.7 Typical Characteristics (continued)

$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $T_A = 25^\circ C$ and $C_{SS} = 5.6nF$, $C_{OUT} = 47\mu F$ (TBME476K025LBC0), when used, the external compensation network is applied as depicted in [セクション 8.2](#), no R_{COMP} , no C_{Comp} unless otherwise noted.

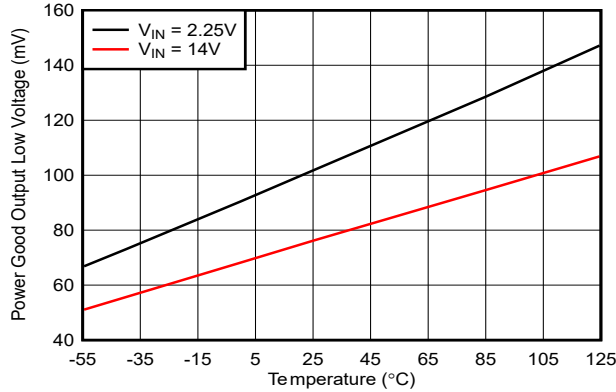


図 6-13. PG Pin Output Low vs Temperature

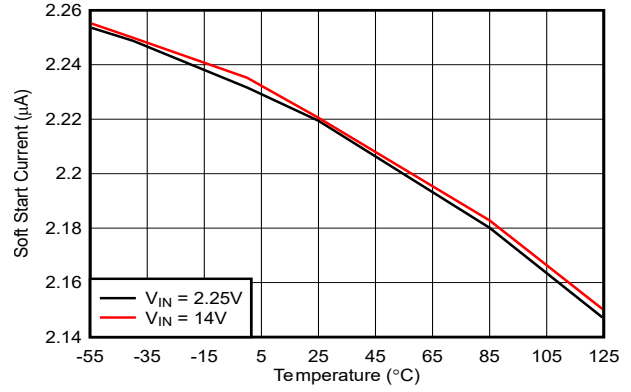
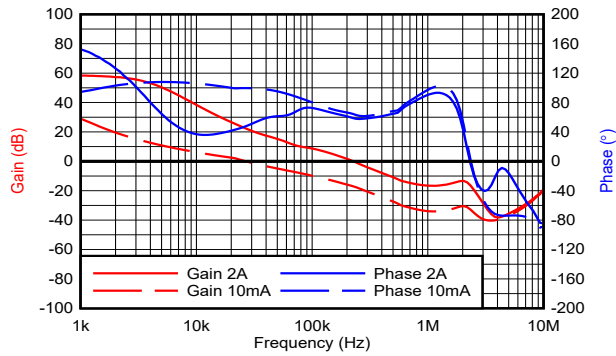
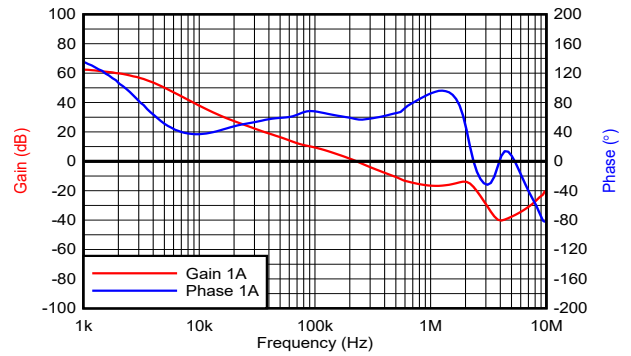


図 6-14. Soft Start Current vs Temperature



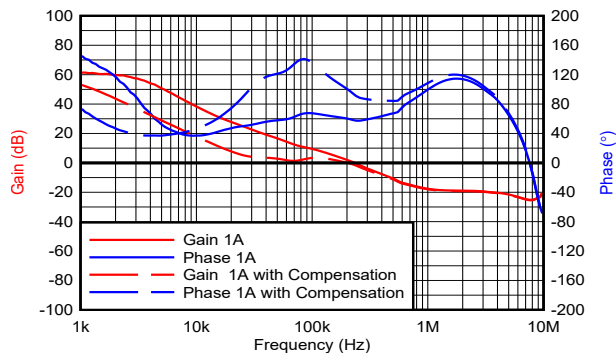
$C_{OUT1} = 47\mu F$ $C_{OUT2} = 1\mu F$ $C_{OUT3} = 0.1\mu F$
 $GM_{2A} = 17dB$ $GM_{10mA} = 32dB$
 $PM_{2A} = 58^\circ$ $PM_{10mA} = 100^\circ$

図 6-15. Gain and Phase Margin vs Frequency (Bode Plot)



$C_{OUT1} = 47\mu F$ $C_{OUT2} = 1\mu F$ $C_{OUT3} = 0.1\mu F$
 $GM_{2A} = 17dB$
 $PM_{2A} = 58^\circ$

図 6-16. Gain and Phase Margin vs Frequency (Bode Plot)



$C_{OUT} = 47\mu F$ If compensation used:
 $GM_{1A} = 24dB$ $GM_{COMP} = 25dB$ $R_{COMP} = 20k\Omega$
 $PM_{1A} = 60^\circ$ $PM_{COMP} = 101^\circ$ $C_{COMP} = 1nF$

図 6-17. Gain and Phase Margins vs Frequency (Bode Plot)

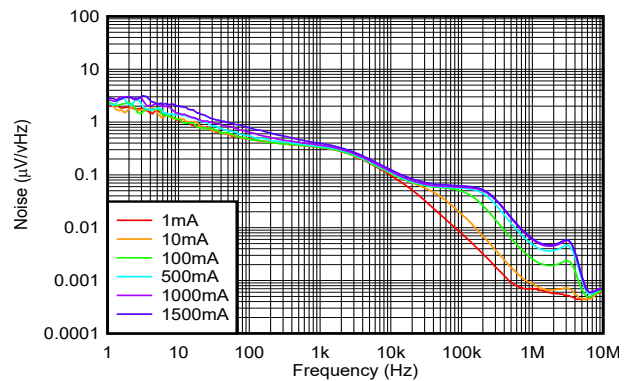
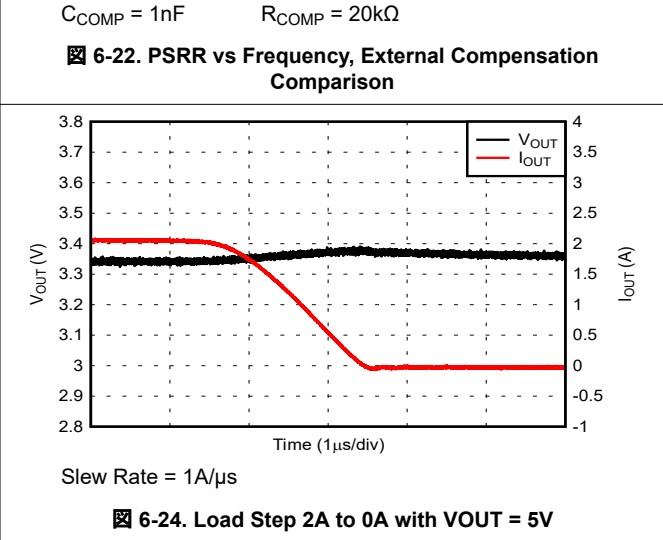
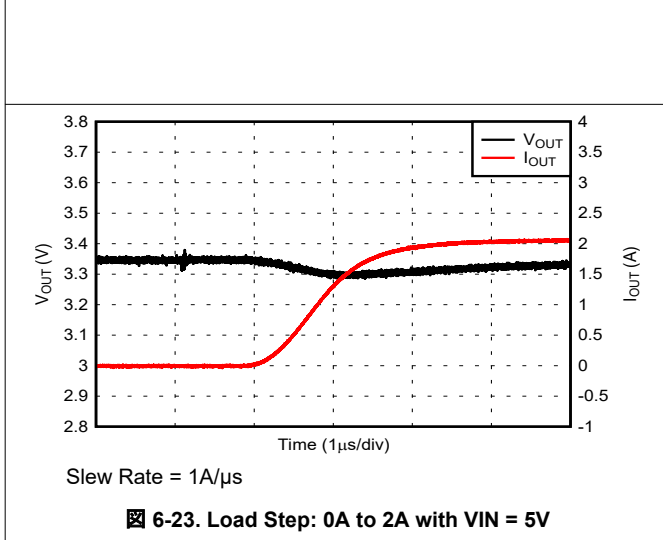
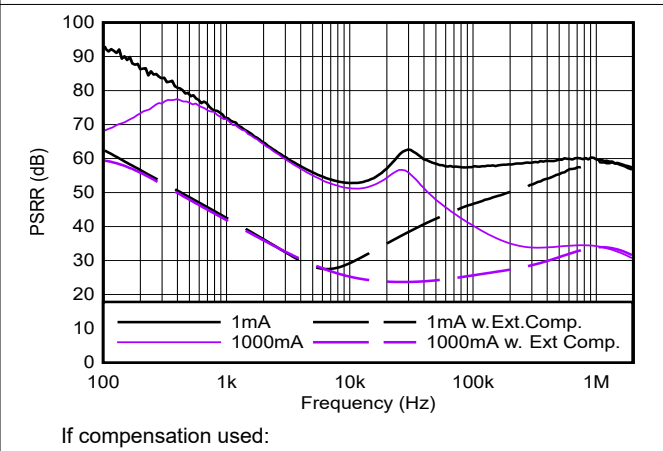
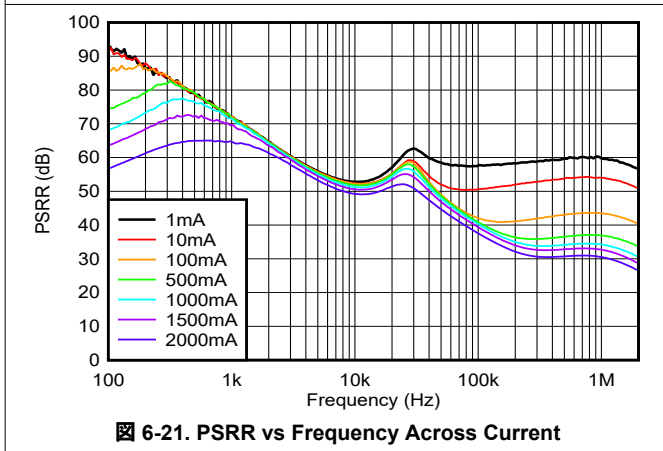
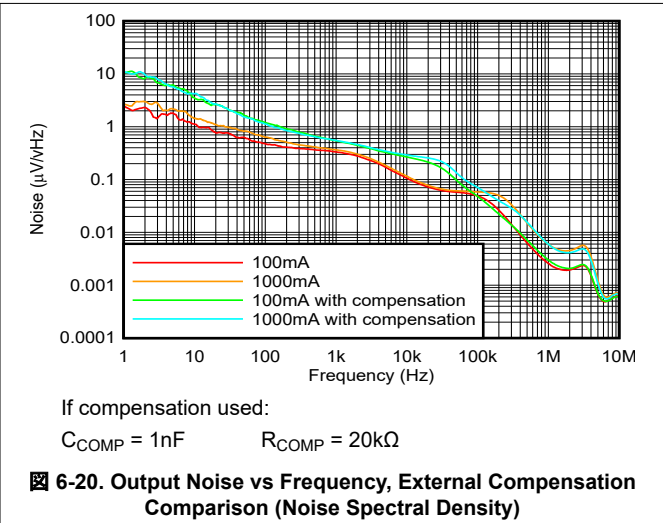
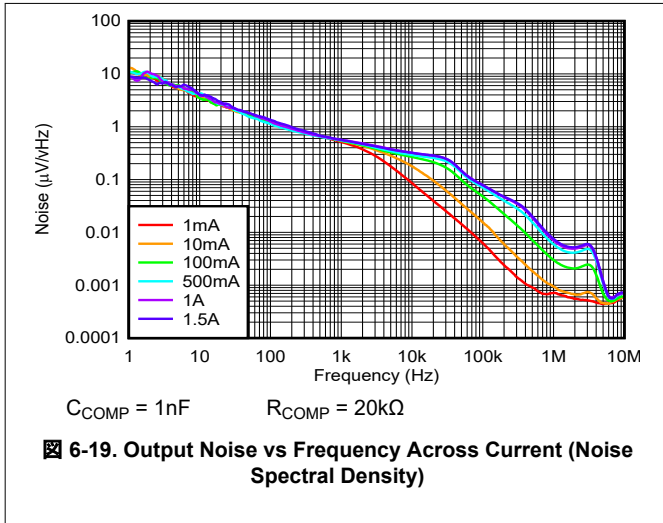


図 6-18. Output Noise vs Frequency Across Current (Noise Spectral Density)

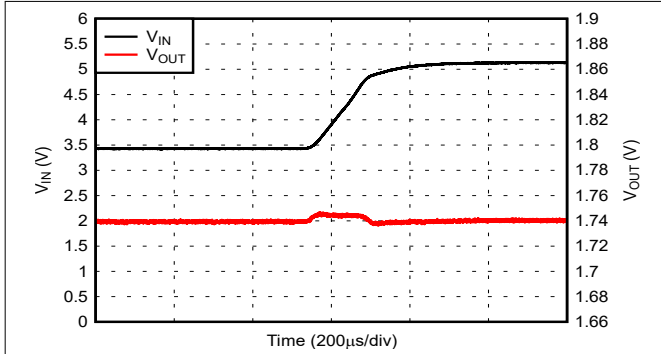
6.7 Typical Characteristics (continued)

$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $T_A = 25^\circ C$ and $C_{SS} = 5.6nF$, $C_{OUT} = 47\mu F$ (TBME476K025LBC0), when used, the external compensation network is applied as depicted in [セクション 8.2](#), no R_{COMP} , no C_{Comp} unless otherwise noted.



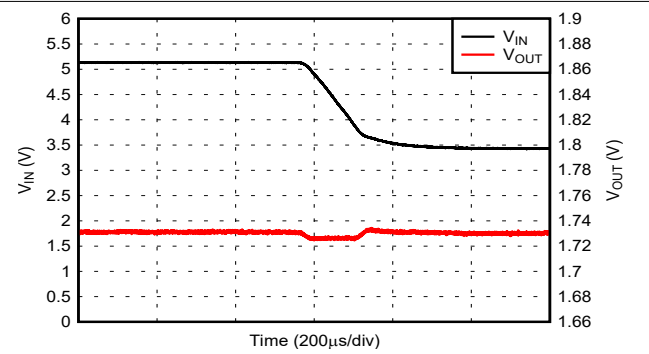
6.7 Typical Characteristics (continued)

$V_{IN} = 5V$, $V_{OUT} = 3.3V$, $T_A = 25^\circ C$ and $C_{SS} = 5.6nF$, $C_{OUT} = 47\mu F$ (TBME476K025LBC0), when used, the external compensation network is applied as depicted in [セクション 8.2](#), no R_{COMP} , no C_{Comp} unless otherwise noted.



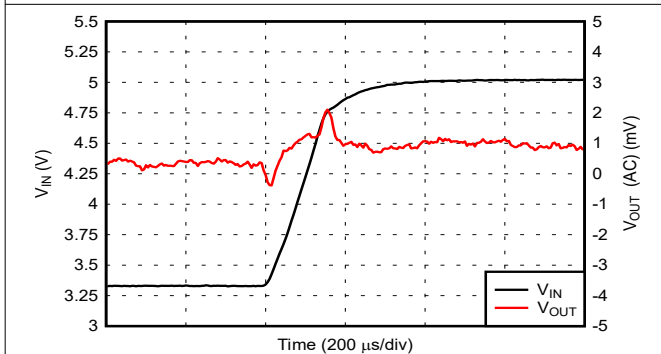
Slew Rate = 10V/ms

図 6-25. Line Step: 3.3V to 5V With $I_{OUT} = 1.8A$



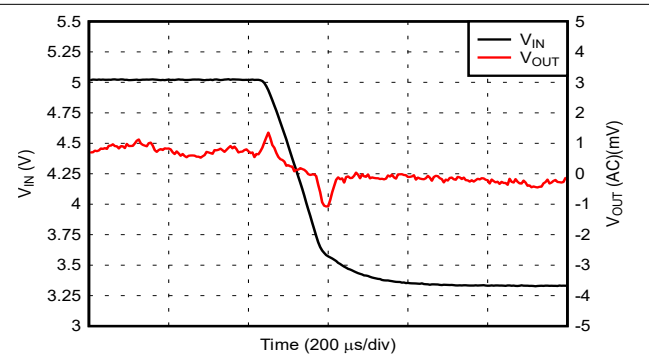
Slew Rate = 10V/ms

図 6-26. Line Step: 5V to 3.3V With $I_{OUT} = 1.8A$



Slew Rate = 10V/ms

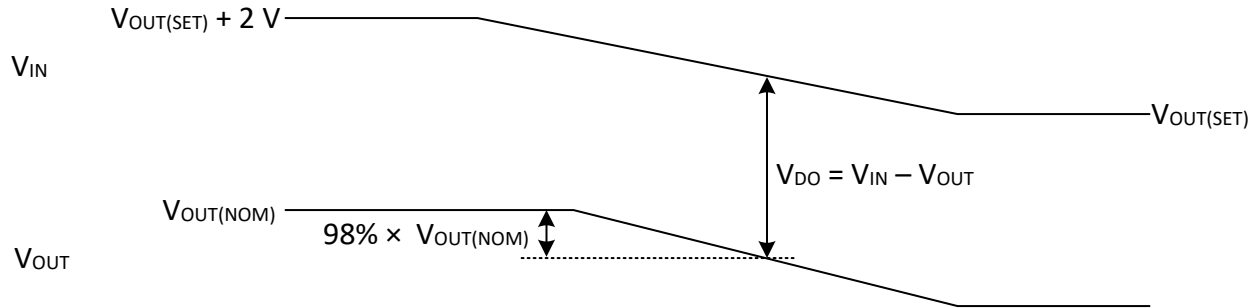
図 6-27. Line Step: 3.3V to 5V AC Coupled



Slew Rate = 10V/ms

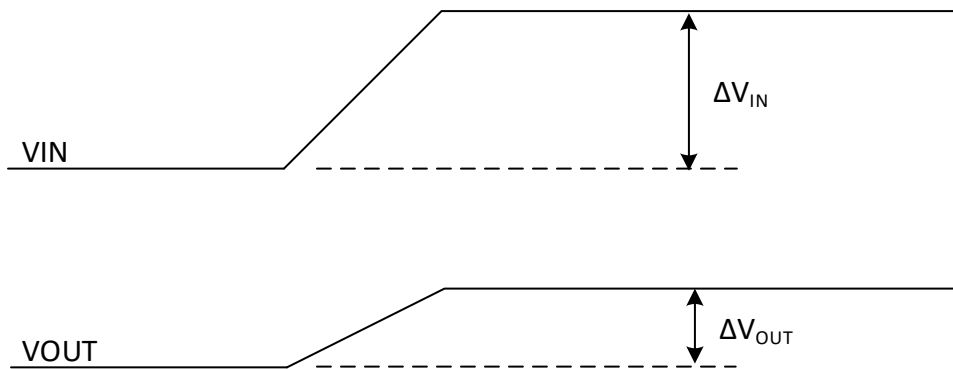
図 6-28. Line Step: 5V to 3.3V AC Coupled

7 Parameter Measurement Information



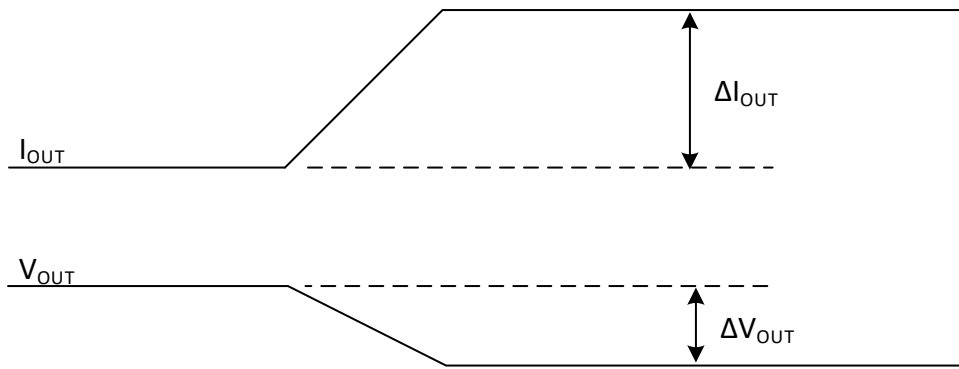
- A. $V_{OUT(SET)}$ is the configured output voltage of the regulator using the feedback resistors, $V_{OUT(NOM)}$ is the measured output voltage. V_{IN} is set 2V above the output (limited to 14V maximum) and is decreased to the output voltage set point ($V_{OUT(SET)}$). When V_{OUT} falls to 98% of the nominal value ($V_{OUT(NOM)}$), the dropout voltage is recorded.

 **7-1. Dropout**



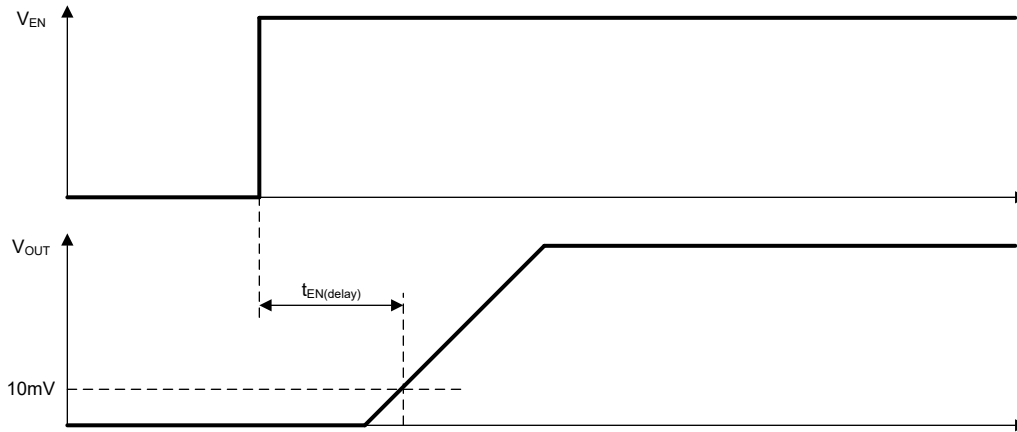
- A. $\Delta V_{OUT} / \Delta V_{IN} = 100\mu V/V$ (typ). This means for a 1V change in V_{IN} ($\Delta V_{IN} = 1V$), there will be a 100 μV change in V_{OUT} ($\Delta V_{OUT} = 100\mu V$). Line regulation is a DC parameter; therefore this waveform can only be considered valid after transients die out or for a slow V_{IN} slew rate.

 **7-2. Line Regulation**



- A. $\Delta V_{OUT} / \Delta I_{OUT} = 4\text{mV/A}$ (typ). This means for a 1A change in I_{OUT} ($\Delta I_{OUT} = 1\text{A}$), there will be a 4mV change in V_{OUT} ($\Delta V_{OUT} = 4\text{mV}$). Load regulation is a DC parameter; therefore this waveform can be considered valid after transients die out or for a slow I_{OUT} slew rate.

☒ 7-3. Load Regulation



☒ 7-4. Enable Propagation Delay

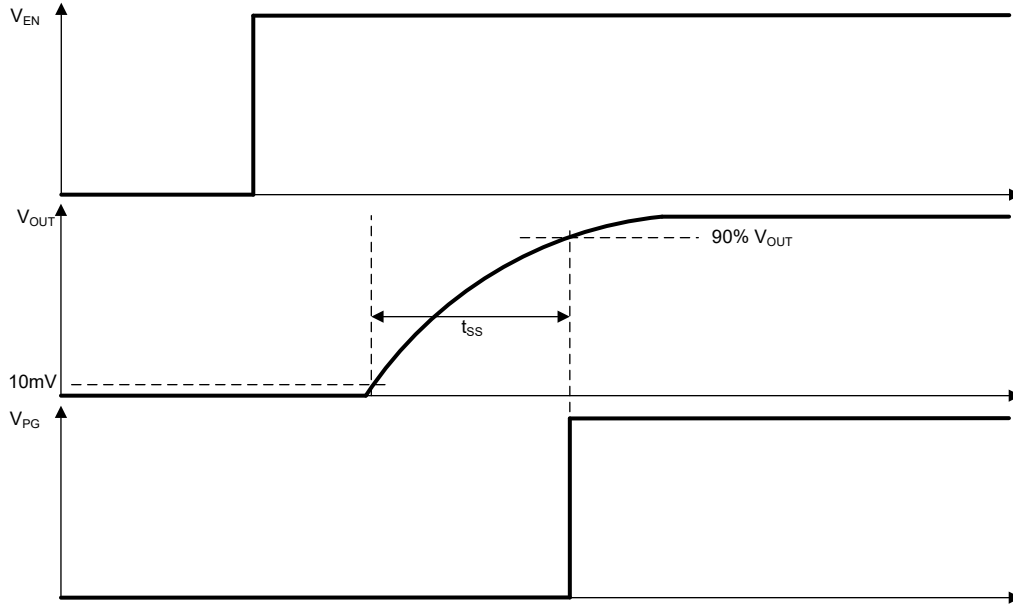


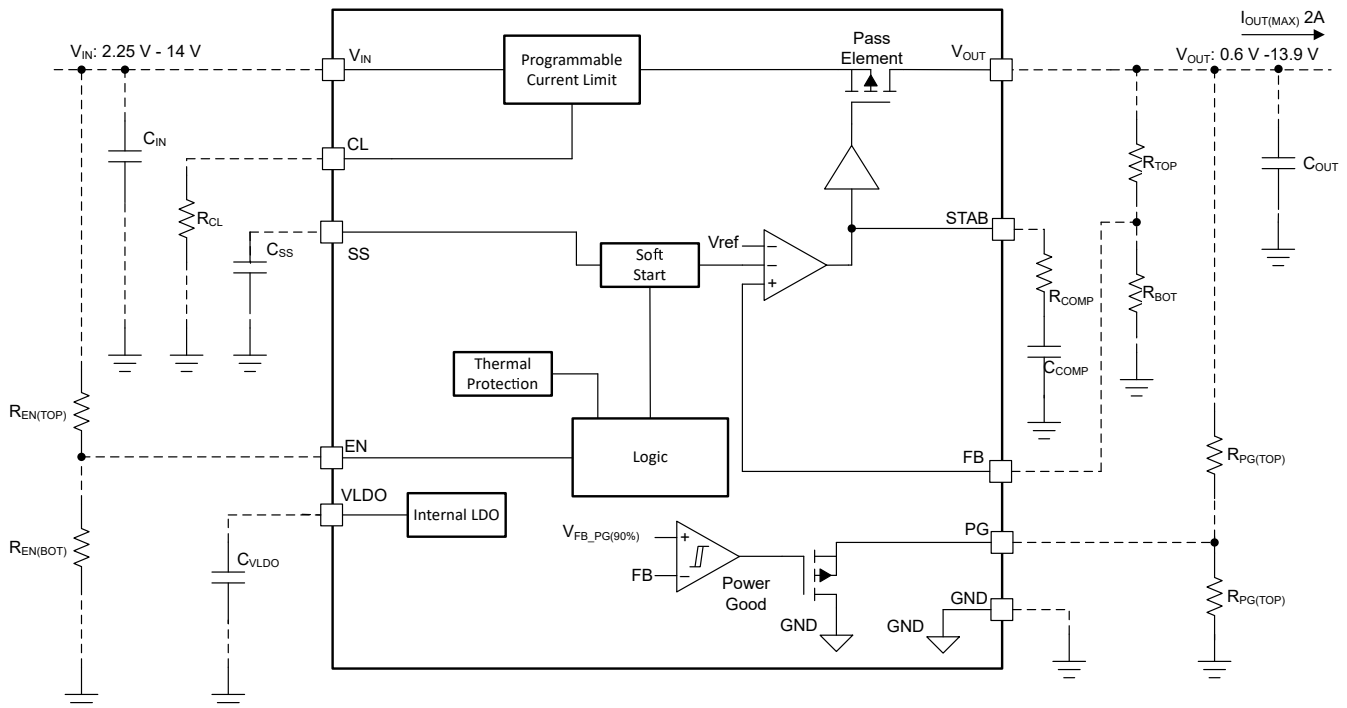
図 7-5. Soft Start Time

8 Detailed Description

8.1 Overview

The TPS7H1121 (TPS7H1121-SP and TPS7H1121-SEP) is a radiation-hardened low dropout linear regulator (LDO) which operates over a wide range of input voltages. The TPS7H1121 is optimized for powering devices in a space environment by using a PMOS pass element which is capable of sourcing up to 2A over a 2.25V to 14V input.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Adjustable Output Voltage (Feedback Circuit)

The output voltage of the TPS7H1121 can be set to a user-programmable level between 0.6V and 13.9V. Achieve this by using a resistor divider connected between V_{OUT} , FB, and GND terminals. R_{TOP} connected between V_{OUT} and V_{FB} , and R_{BOTTOM} connected between V_{FB} and GND.

Use 式 5 to determine V_{OUT} .

$$V_{OUT} = \frac{(R_{FB(TOP)} + R_{FB(BOT)}) \times V_{FB}}{R_{FB(BOT)}} \quad (1)$$

where

- $V_{FB} = 0.596V$ (typ)

8.3.2 Enable

When the enable pin is low, the device enters shutdown mode and does not regulate the output voltage. Normally, an external resistor divider from V_{IN} to GND is used to feed EN.

Connection of the Enable pin directly to V_{IN} is possible when V_{IN} is below the Recommended Operating level of 7V; if a higher voltage level is to be provided to the Enable pin, then a simple voltage divider can be applied, refer to 式 2 for resistor sizing guidance at the desired turn-on voltage.

$$V_{IN(\text{rising})} = V_{EN(\text{rising})} \times (R_{EN_TOP} + R_{EN_BOT}) / R_{EN_BOT} \quad (2)$$

Similarly, a $V_{IN(\text{falling})}$ voltage can also be calculated using 式 3. The $V_{IN(\text{rising})}$ and $V_{IN(\text{falling})}$ can be thought of as configurable UVLO (under voltage-lockout) thresholds.

$$V_{IN(\text{falling})} = V_{EN(\text{falling})} \times (R_{EN_TOP} + R_{EN_BOT}) / R_{EN_BOT} \quad (3)$$

While the TPS7H1121 will turn-on at a voltage of V_{EN} of 0.6V (typ), it is recommended that the final value is above 0.8V. This is to ensure appropriate margin above the enable threshold during normal operation to prevent SEFIs during exposure to heavy ions. This recommendation is achieved by satisfying 式 4.

$$V_{IN(\text{final})} \times R_{EN_BOT} / (R_{EN_TOP} + R_{EN_BOT}) = V_{EN(\text{final})} > 0.8V \quad (4)$$

Alternatively, the EN pin can be driven directly from a micro-controller or FPGA. The low voltage threshold of the enable pin aids in support of 1.1V, 1.8V, 2.5V, and 3.3V logic levels. Similarly a final V_{EN} above 0.8V for direct logic level driving is recommended (this is typically easily achieved with standard logic levels).

8.3.3 Dropout Voltage V_{DO}

Dropout voltage, V_{DO} , is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) where the output voltage falls to 98% of the initial value at the indicated current. See 図 7-1 for the test waveforms used to measure dropout. The dropout voltage is higher at lower values of V_{IN} ; therefore, dropout voltage is specified across different conditions in セクション 6.5.

In dropout, the pass transistor is in the ohmic or triode region of operation, and acts as a switch. The dropout voltage indirectly specifies a minimum input voltage greater than the nominal programmed output voltage at which the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage falls as well.

When V_{IN} is below 3V, the error amplifier operates with less headroom versus what is present for a V_{IN} range of 3V to 14V; the reduction in headroom causes higher dropout voltage for V_{IN} voltages less than 3V (see typical dropout performance graphs 図 6-1 through 図 6-6).

8.3.4 Output Voltage Accuracy

The TPS7H1121 features an accurate voltage reference, which is essential in minimizing the intrinsic error of the LDO.

Output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage. The accuracy specification in the セクション 6.5 table presents two operating regions, one in which the V_{IN} is above 3V and one when V_{IN} is in the "low-input" voltage region ($2.25V \leq V_{IN} \leq 3V$).

The $\pm 1.5\%$ specification applies across the complete temperature range of -55°C to 125°C , across the input voltage range of $3V \leq V_{IN} \leq 14V$, when the dissipated power is $\leq 3W$, and up to the full load ($10\text{mA} \leq I_{OUT} \leq 2A$).

When V_{IN} is below 3V ($2.25V \leq V_{IN} \leq 3V$), the output voltage accuracy is adjusted to $\pm 1.8\%$.

A few additional details to the measurement are noted:

- The range of V_{IN} , I_{OUT} and temperature mean the specification applies across all load and temperature combinations. This is accomplished by testing multiple bias conditions that cover various corners.
- Footnote 3 in セクション 6.5 specifies that the measurement is done with a power dissipation limit that is limited to a maximum 3W. This is due to tester thermal limitations.
- The test conditions specify a minimum of 10mA and not 0mA for more robust accuracy measurements. However, in a normal application the TPS7H1121 device does not have a minimum load current for stability
- TI does not recommend including the following error terms into the V_{ACC} specification as the following terms are inherently covered by the V_{ACC} parameter:
 - V_{FB} accuracy
 - $\Delta V_{OUT}/\Delta V_{IN}$ (line regulation)

- $\Delta V_{OUT}/\Delta I_{OUT}$ (load regulation)
- V_{OUT} tempco
- The error due to the feedback resistors, such as the specified tolerances can be added to the V_{ACC} specification.
- For additional information on determining accuracy see [セクション 9.2.2.2](#).

8.3.5 Output Noise

LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits. The TPS7H1121 output noise is typically $35\mu V_{RMS}$.

When an external compensation network is connected to the STAB pin, the applied network can reduce the loop bandwidth; therefore, the internal circuitry is less capable to minimize internally generated noise. [図 6-20](#) shows the noise performance difference when configured with and without an external compensation network (note: $R_{Comp} = 20k\Omega$ and $C_{Comp} = 1nF$).

8.3.6 Power Supply Rejection Ratio (PSRR)

The PSRR (power supply rejection ratio) of the TPS7H1121, is the amount of attenuation of the input noise at V_{IN} , to the output, V_{OUT} . PSRR is mathematically defined in [式 5](#).

$$PSRR = 20 \times \log_{10} \left(\frac{V_{IN(AC)}}{V_{OUT(AC)}} \right) \quad (5)$$

The input noise is generally dominated by the switching ripple of an upstream converter. This noise occurs at the switching frequency and associated harmonics.

When using an external compensation network and the loop bandwidth is reduced, then the overall PSRR diminishes as well. [図 6-22](#) illustrates the trade off in a typical application in which the applied compensation network has reduced the loop band-width, but improved system stability ($R_{Comp} = 20k\Omega$, $C_{Comp} = 1nF$).

8.3.7 Soft Start

Connecting a capacitor (C_{SS}) from the SS terminal to GND slows down the output voltage ramp rate. The soft-start capacitor charges up to 1.2V. [式 6](#) determines the required soft start capacitor value C_{SS} with a user specified soft -start time t_{SS} .

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{REF}} \quad (6)$$

where

- t_{SS} = soft-start time
- $I_{SS} = 2\mu A$ (typ)
- $V_{REF} = 1.2V$ (typ)

See Typical Graph [図 6-14](#) for Soft Start Current vs Temperature Performance.

8.3.8 Power Good (PG)

Power Good terminal is an open-drain connection and can be used to sequence multiple LDOs. The PG terminal will be pulled low until the output voltage reaches 95% (typ) of its final level. At that point, the PG pin will be pulled up through the external resistor divider. Since the PG pin is open drain, it can be pulled up to any voltage as long as it does not exceed the recommended maximum of 7V listed in [セクション 6.5](#).

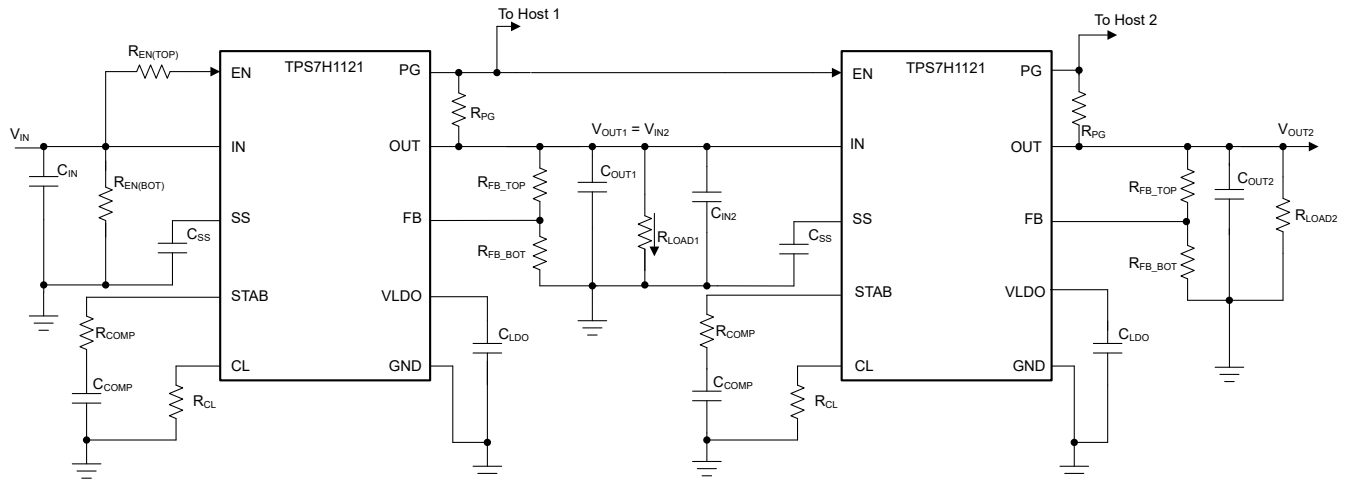


图 8-1. Sequenced Power Good

8.3.9 Stability

8.3.9.1 Stability

Traditional stability margins (such as gain margin $\geq 6\text{dB}$ and phase margin $\geq 50^\circ$) for space rated IC's are often more onerous than industrial and consumer electronics. The TPS7H1121 is designed to support a wide range of space rated output capacitors (generally $22\mu\text{F}$ to $220\mu\text{F}$) while maintaining a 6dB gain margin and 50° phase margin without utilizing the included STAB pin for external compensation.

In addition to the TPS7H1121's wide intrinsic stability, the STAB pin may be utilized to insert an external RC compensation network that ties directly to the error amplifier's output. This architecture, as depicted in 图 8-2, illustrates how an external compensation network is directly inserted prior to the pass element's buffer, which maximizes the efficacy of the inserted RC compensation circuit.

This level of efficacy for an external compensation network enables end-users of the TPS7H1121 to conduct in depth stability analysis and widen stability margins for the applied output load. Additionally, it enables utilization of output capacitors as low as $6.8\mu\text{F}$ while allowing flexibility in managing low-ESR capacitors.

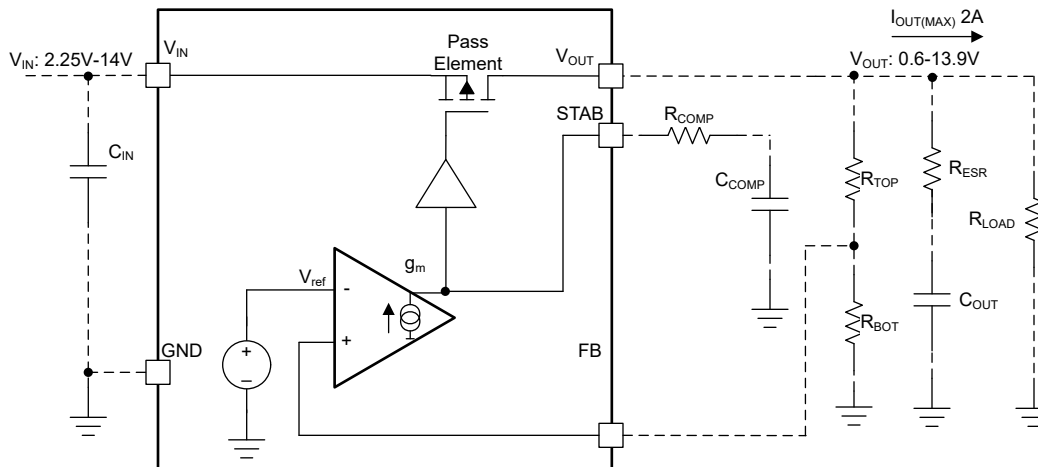


图 8-2. Simplified Compensation Schematic

8.3.9.2 STAB Pin

The STAB (stability) pin of the TPS7H1121 is designed to provide direct access to the controller's error amplifier; insertion into the LDO's control circuitry facilitates detailed stability analysis and fine tuning of the LDO's stability performance.

The TPS7H1121 has a wide envelope in which typical gain and phase margin is in excess of 6dB and 50° (with output capacitance ranging from $22\mu\text{F} \leq C_{\text{OUT}} \leq 220\mu\text{F}$). However, external compensation is provided via the STAB pin in which the R_{COMP} and C_{COMP} network can be utilized to further optimize the stability performance of the TPS7H1121 if desired. TI recommends that an external network is applied for low C_{OUT} applications or for special concerns in which maximum stability margin is necessary. For further details on how to implement Type II and III Compensation, view section セクション 9.2.2.9 or SLVA662.

8.3.10 Programmable Current Limit

Brick-wall current limit, also known as constant current limit, is shown in 図 8-3. In this mode, once I_{PCL} is reached and the current limit circuitry has time to respond, the TPS7H1121 LDO enters constant current regulation mode. In other words, the output voltage reduces to whatever value is needed to keep the output current at I_{LIM} . Once the fault is removed the device resumes regulation.

Due to the high power dissipation in brick-wall current limit, there is the possibility that the TPS7H1121 enters thermal shutdown which causes the device to stop regulation until the TPS7H1121 cools enough to exit thermal shutdown.

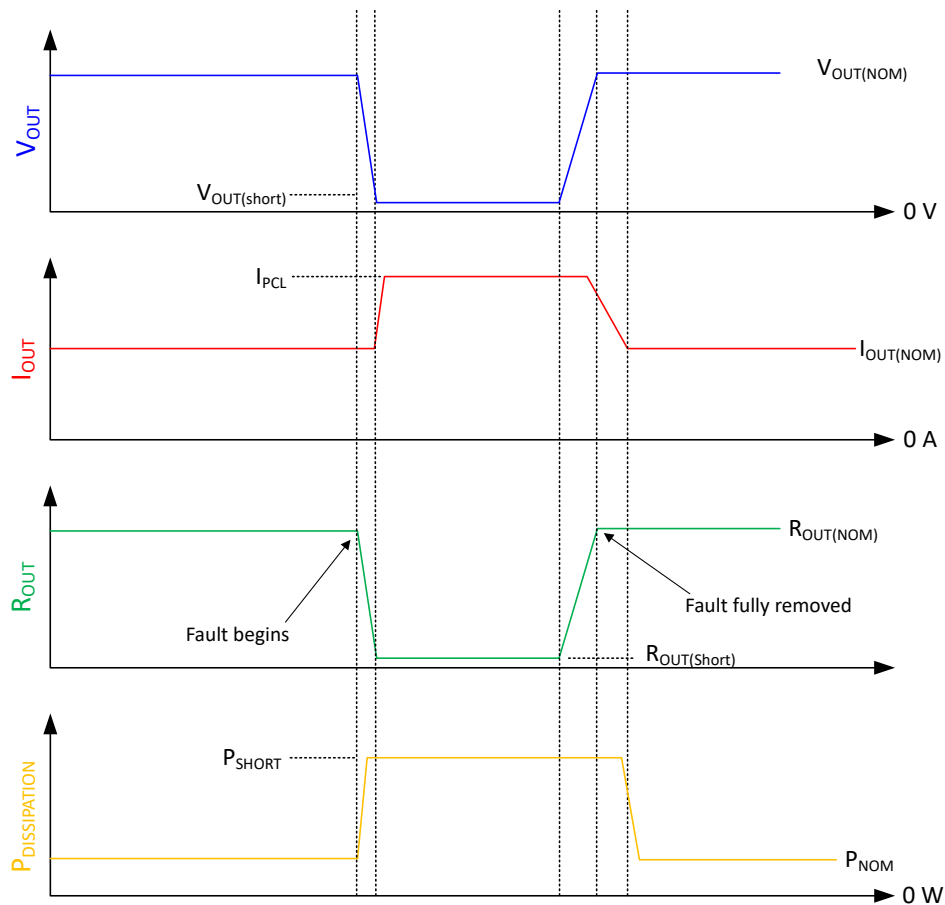


図 8-3. Simplified Brick-Wall Current Limit Waveforms

The programmable current limit's accuracy tightens with increased load current; 表 8-1 shows the recommended E96 value with a typical accuracy.

With the stipulated accuracy of the current limit, the programmable current limit resistor R_{CL} needs to be selected to accommodate the negative portion of the accuracy current limit circuitry. Additionally, a 20% headroom margin is recommended to prevent the current limit from intervening during nominal operation. For example an application with a nominal load of 1A can have a minimum programmable current limit setting of 1.4A / 97.6k Ω ; the setting for a 97.6k Ω programmable current limit has a negative accuracy of -25% which leads a minimum intervening current limit of 1.05A.

For example an application with a nominal load of 1A is recommended to have a minimum intervening current of 1.2A; which yields a nominal current limit of 1.6A. Therefore an R_{CL} setting of 80.6k Ω with a negative accuracy of -25% leads to a minimum intervening current limit of 1.2A; which complies with the recommended 20% headroom.

表 8-1. Recommended Current Limit Setting Resistor

PROGRAMMABLE CURRENT LIMIT SETTING (A)	E96 (k Ω)	ACCURACY
0.32	442	±35%
0.4	392	
0.5	332	
0.6	267	±30%
0.7	205	
0.75	174	
0.8	169	
0.9	158	
1	143	
1.1	133	±25%
1.2	121	
1.3	110	
1.4	97.6	
1.5	88.7	
1.55	82.5	
1.6	80.6	
1.7	78.6	
1.8	75	
1.9	71.5	
2	69.8	
2.1	66.5	±20%
2.2	63.4	
2.3	60.4	
2.4	57.6	
2.5	54.9	
2.6	52.3	
2.7	49.9	
2.8	46.4	
2.9	44.2	
3	41.2	

8.3.11 Thermal Shutdown

Upon exceeding the TPS7H1121 thermal shutdown temperature limit, the integrated thermal shutdown circuitry activates to turn-off the device when the die temperature exceeds $T_{SD(enter)}$. As the die cools below $T_{SD(exit)}$, the device resumes regulation. The typical $T_{SD(enter)}$ of 160°C and $T_{SD(exit)}$ of 130°C provides a large hysteresis (30°C typical). The large hysteresis is intended to allow the device to sufficiently cool before attempting to resume regulation.

8.4 Device Functional Modes

8.4.1 Enable / Disable

The table below shows the device functional modes:

表 8-2. Device Functional Modes

EN PIN	DEVICE STATUS
High	Regulation mode
Low	Shutdown mode

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS7H1121-SP LDO linear regulator is targeted space environment applications. This regulator has various features such as low dropout, soft start, output current limit, and error amplifier access via STAB pin.

9.2 Typical Application

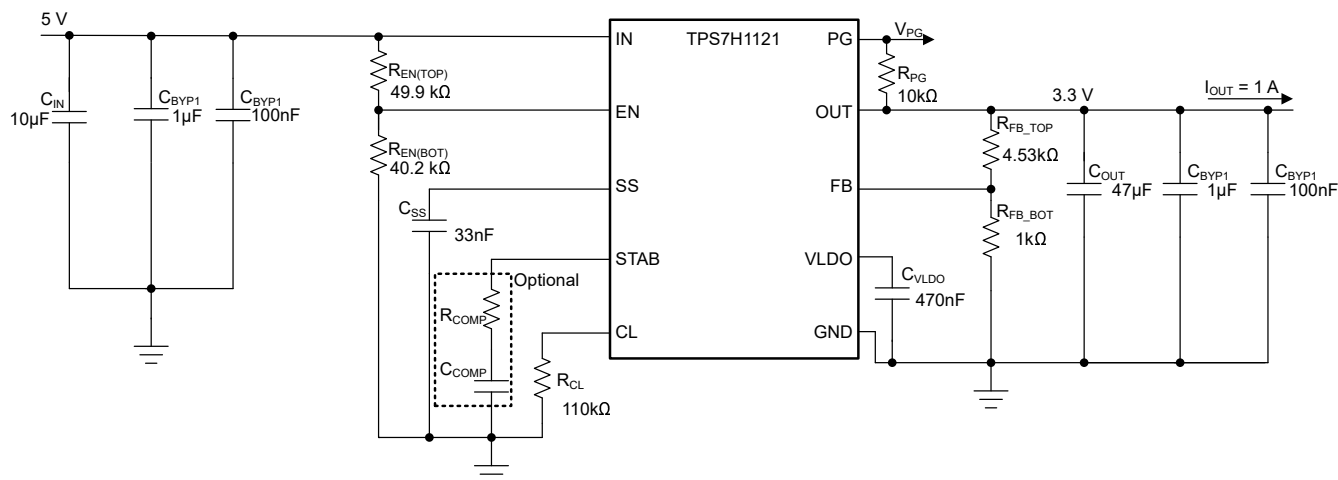


図 9-1. Application Schematic

9.2.1 Design Requirements

This example highlights a design using the TPS7H1121 based on its evaluation module. For more details, please refer to the EVM user's guide, *TPS7H1121EVM-CVAL Evaluation Module (EVM) User's Guide (SLVUCX9)*. A few parameters must be known in order to start the design process. These parameters are typically determined at the system level. For this example, we start with the following known parameters:

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	5V ± 5%
Output voltage	3.3V ± 5%
Maximum output current	1A (typ)
V _{IN} (turn-on threshold)	1.35V (typ)
V _{OUT} (PG assertion threshold)	90% of V _{OUT} (final) (typ), 2.97V
Soft start time, t _{SS}	20ms
Minimum phase margin	50°
Maximum gain margin	6dB

9.2.2 Detailed Design Procedure

9.2.2.1 Output Voltage Configuration

The output voltage is configured using 式 1.

Therefore 0.1% feedback resistors are selected with $R_{FB(TOP)} = 1.01k\Omega$ and $R_{FB(BOT)} = 4.53k\Omega$; using resistors with a 1% tolerance is acceptable, however this directly contributes a 1% error to the output voltage.

9.2.2.2 Output Voltage Accuracy

To determine the overall output voltage accuracy, refer to the device voltage accuracy V_{ACC} from the セクション 6.5, the top and bottom feedback resistors ($R_{FB(TOP)}$ and $R_{FB(BOT)}$).

$$\text{System}_{(\text{error})} = V_{ACC} + R_{(\text{error})} \quad (7)$$

When the input voltage V_{IN} is below 3V, the error amp is operating with a reduced head room such that output accuracy performance is widened to $\pm 1.8\%$; for this example V_{IN} is above 3V, therefore the standard $\pm 1.5\%$ accuracy can be applied.

For the selected 0.1% feedback resistors, the calculated error is shown in 式 8, this assumes an uncorrelated error and the errors are added as the sum of the resistors' error squared.

$$R_{(\text{error})} = \sqrt{(0.1^2 + 0.1^2)} = \pm 0.14\% \quad (8)$$

The negative and positive system error's are summed with the results for this example shown below in equations 式 9 and 式 10.

$$\text{System}_{(\text{neg_error})} = -1.5\% + -0.14\% \quad (9)$$

$$\text{System}_{(\text{pos_error})} = 1.5\% + 0.14\% \quad (10)$$

Adding the following errors together results in an accuracy of $\pm 1.64\%$.

9.2.2.3 Enable Threshold

The desired turn-on threshold is 1.35V. This means that as the V_{IN} rail is turned-on and begins rising, the TPS7H1121 commences turning-on as soon as V_{IN} reaches 1.35V. While this is not enough headroom from V_{IN} to V_{OUT} for final regulation, the regulator initiates start-up and V_{IN} progresses to the final voltage of 5V. If desired, a higher voltage turn-on threshold can be selected (for example, 3.5V), provided the desired voltage is below 7V.

Using 式 1 and selecting an $R_{EN(TOP)}$ value of 49.9k Ω , the $R_{EN(BOT)}$ can be calculated as shown in 式 11.

$$R_{EN(BOT)} = \frac{V_{EN(\text{rising})} \times R_{EN(TOP)}}{V_{IN(\text{rising})} - V_{EN(\text{rising})}} = \frac{0.605\text{ V} \times 49.9\text{ k}\Omega}{1.35\text{ V} - 0.605\text{ V}} = 40.2\text{ k}\Omega \quad (11)$$

Using E192 resistor values, $R_{EN(BOT)}$ is chosen to be 40.2k Ω .

To comply with the maximum pin voltage for Enable use 式 4. As shown in 式 12, $V_{EN(\text{final})} = 2.24\text{V}$ which is less than the recommended maximum of 7V and above the recommended minimum final value of 0.8V.

$$V_{EN(\text{final})} = V_{IN(\text{final})} \times \left(\frac{R_{EN(BOT)}}{R_{EN(BOT)} + R_{EN(TOP)}} \right) = \frac{5\text{ V} \times 40.2\text{ k}\Omega}{40.2\text{ k}\Omega + 49.9\text{ k}\Omega} = 2.24\text{V} \quad (12)$$

9.2.2.4 Soft Start Capacitor

The evaluation module is specified to have a soft start time of t_{SS} of 20ms, the soft start capacitor value can be calculated with 式 6.

$$C_{SS} = \frac{20 \text{ ms} \times 2 \text{ } \mu\text{A}}{1.2 \text{ V}} = 33.3 \text{ nF} \quad (13)$$

Therefore a 33nF ceramic capacitor is selected to configure the soft start time.

9.2.2.5 Programmable Current Limit Resistor

The evaluation module is populated with a current limit setting resistor to provide a $I_{lim} = 3\text{A}$; to configure a lower current limit see [表 8-1](#).

9.2.2.6 Characterization of Overcurrent Events that Exceed Thermal Limits

High power overcurrent events are characterized by duration, the input and output voltage they occur at, and the resulting current. In these high power overcurrent conditions, the dissipated power in the pass element becomes much greater than nominal operating conditions. Depending on the specific overcurrent conditions, the device heats up until reaching thermal shutdown. However, depending on the specific overcurrent event, the device may heat faster than the thermal shutdown circuitry can respond.

[表 8-1](#) specifies resistors values for a desired current limit setting and the anticipated accuracy of the programmable current limit at the specified setting; 3A is a recommended maximum programmable current limit setting as the 20% accuracy has a maximum current limit of 3.6A, which is below the Absolute Maximum rating of 3.9A.

The magnitude of the over-current condition intensifies as a function of the $V_{IN} - V_{OUT}$ differential and pulse width (for faults to be evaluated as DC a 1s pulse can be used). By combining the input and output voltage differential, fault pulse width, and programmable current limit setting, a recommended programmable current limit protection area is derived as shown in [図 9-2](#) which was characterized using validation hardware for the TPS7H1121 (ceramic package) under laboratory ambient conditions ($T_A = 25^\circ\text{C}$). The effective thermal resistance of the thermal pad is calculated to be $R_{TH(PCB)} = 5^\circ\text{C/W}$ (taking into account thermal via diameter, spacing, and board layers), and the programmable current limit I_{PCL} was set for the maximum allowable current of 3.6A. Applied faults of a pulse width of 10ms, 100ms and 1s were applied until the device was no longer functional; the applied voltage and programmed current were then adjusted lower on subsequent units until the curve was determined.

The depicted curve is very dependent on assumed ambient temperatures, package thermal resistance, PCB thermal resistances and nature of the applied short; the curve below is only applicable for the ceramic unit and the validation hardware utilized.

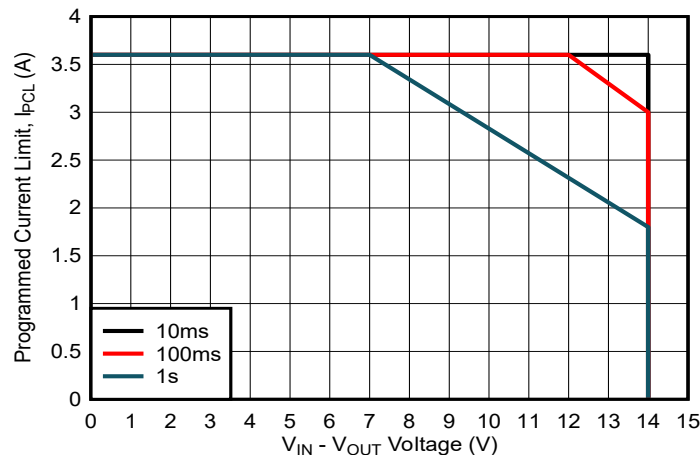


図 9-2. Programmable Current Limit Protection Area

9.2.2.7 Power Good Pull Up Resistor

TI recommends to use a pullup resistor between 10kΩ to 100kΩ; the evaluation module is configured with 10kΩ.

9.2.2.8 Capacitors

TPS7H1121 may use of a combination of tantalum and ceramic capacitors to achieve good volume to capacitance ratio. 表 9-2 highlights some of the supported capacitors. TI recommends to follow proper derating guidelines as recommended by the capacitor manufacturer based upon output voltage and operating temperature.

TI recommends to use a polymer or tantalum capacitor along with a 0.1 μ F and 1 μ F ceramic capacitors implemented as bypass capacitors. The device is stable for input and output tantalum, polymer or ceramic X7R capacitor values or networks with bulk capacitance's ranging from 6.8 μ F to 880 μ F (some values within this range may require the use of external compensation). However, the dynamic performance of the device varies based on load conditions, the capacitor values used (including ESR) and utilization of the external compensation STAB pin. Bulk output capacitance less than 22 μ F and capacitance exceeding 220 μ F, should generally use an external compensation network applied to the STAB pin to achieve robust stability margins. Thorough stability analysis should always be performed to ensure that requisite stability margins are attained across the entirety of the mission profile.

Bulk output capacitor ESR is significantly affects system stability; the TPS7H1121 was designed to achieve wide gain and phase margins with tantalum or polymer surface mount capacitors with low ESR. Ceramic capacitors are also supported, however ceramic capacitors have lower output capacitance and ESR such that an external compensation network may be necessary to achieve stability targets.

表 9-2. TPS7H1121 Capacitors

CAPACITOR PART NUMBER	CAPACITOR DETAILS (CAPACITOR, VOLTAGE, ESR @ 100kHz, Case Size)	TYPE	VENDOR
TES226K035	22 μ F, 35V, 43m Ω , 7343	Tantalum - MnO2	AVX
TBME476K025LBLC9	47 μ F, 25V, 65m Ω , 7343	Tantalum - MnO2	AVX
T540D227K010AH	220 μ F, 10V, 24m Ω , 7343	Tantalum - Polymer	Kemet

9.2.2.8.1 Hybrid Output Capacitor Network

The recommendation for the TPS7H1121 is to utilize ceramic bypass capacitors with a tantalum bulk capacitor. The combination of a tantalum and ceramic capacitor forms a hybrid network capacitor; see application report How to Calculate the Load Pole and ESR Zero When Using Hybrid Output Capacitors (SLVAE26) for how to analytically implement and assess the applied output capacitor network.

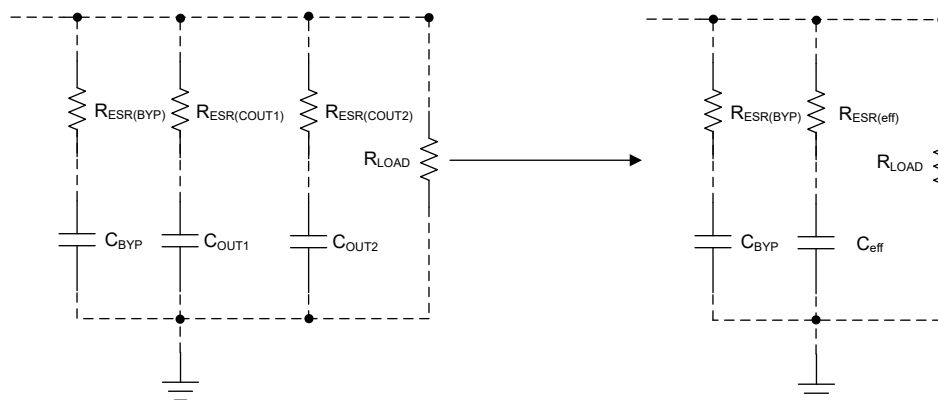


図 9-3. Recommended Hybrid Output Capacitor Network Simplification

TI recommends when conducting analytical analysis of the output capacitor network to only combine capacitors and the associated parasitic parameters which are identically specified (combine identical tantalums, keep bypass caps and tantalum caps distinct from each other in analysis). In the figure above, capacitors C_{OUT1} and C_{OUT2} are combined into effective capacitance and ESR of C_{eff} and R_{eff} with the bypass cap C_{BYP} being excluded.

9.2.2.9 Frequency Compensation

Applying a simple RC compensation network to the STAB pin as optionally depicted in [Figure 9-1](#) enables the end user to optimize the phase and gain margin of the system's stability.

The addition of this RC compensation network introduces 2 poles and 1 zero to the system. Firstly, a low frequency pole is present which can be approximated in more detailed analytical analysis.

The compensation pole frequency, $f_{p(COMP)}$, is approximated using [Equation 14](#).

$$f_{p(COMP)} = \frac{C_{COMP} + C_{OTA}}{2\pi \times R_{COMP} \times C_{COMP}} \quad (14)$$

where

- $C_{OTA} = 100\text{pF}$ (typical sim)

The compensation zero frequency, $f_{z(COMP)}$, is approximated by [Equation 15](#).

$$f_{z(COMP)} = \frac{1}{2\pi \times R_{COMP} \times C_{COMP}} \quad (15)$$

The open loop gain A_{OL} is approximated by [Equation 16](#).

$$A_{OL} = g_{m(OTA)} \times R_{OTA} \quad (16)$$

where

- $g_{m(OTA)} = 5\text{mS}$ (typical sim)
- $R_{OTA} = 220\text{k}\Omega$ (typical sim)

9.3 Power Supply Recommendations

This device is designed to operate with an input voltage supply of up to 14V. The minimum input voltage must provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

9.4 Layout

9.4.1 Layout Guidelines

- For best performance, all traces should be as short as possible.
- Use wide traces for IN, OUT, and GND to minimize the parasitic electrical effects.
- Place the bulk output capacitors (generally tantalum or tantalum polymer) near the OUT pins of the device.
 - If a ceramic output capacitor is used, place it near the point of load.

9.4.2 Layout Example

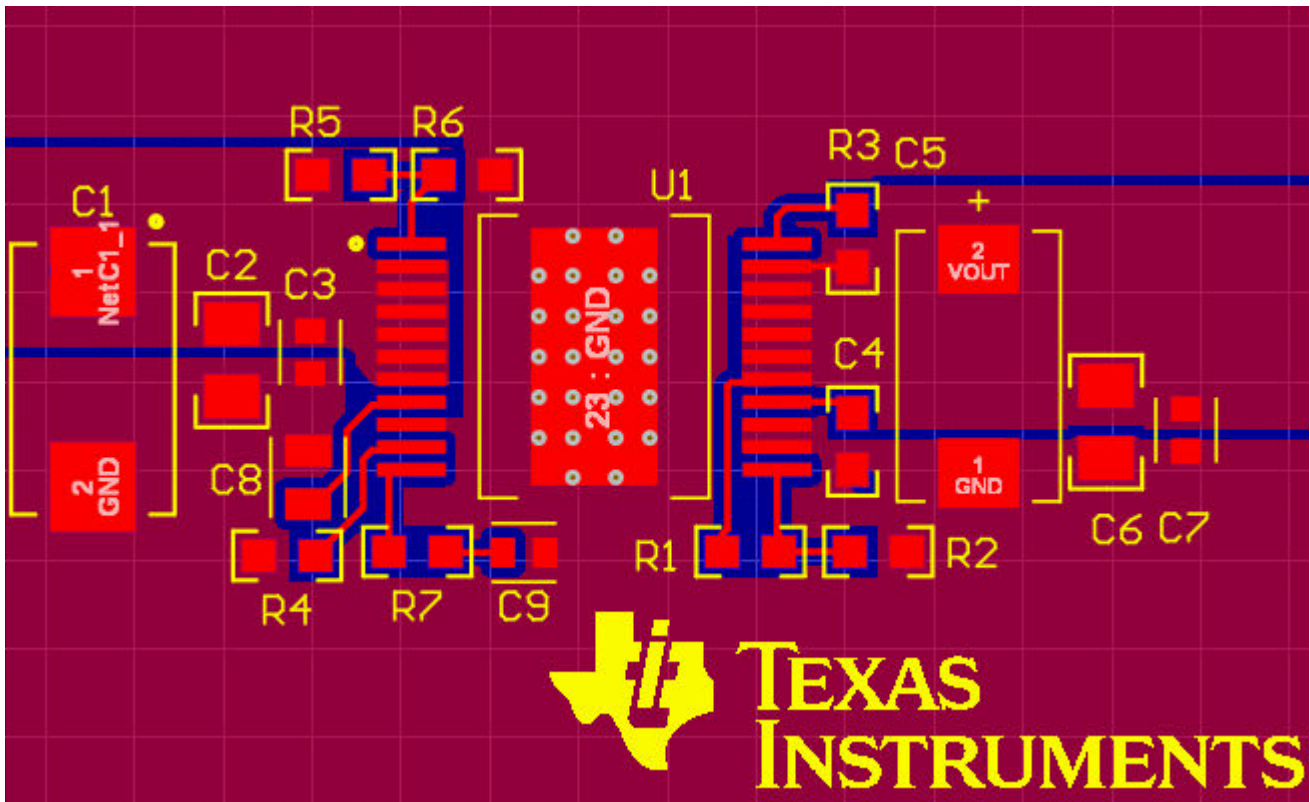
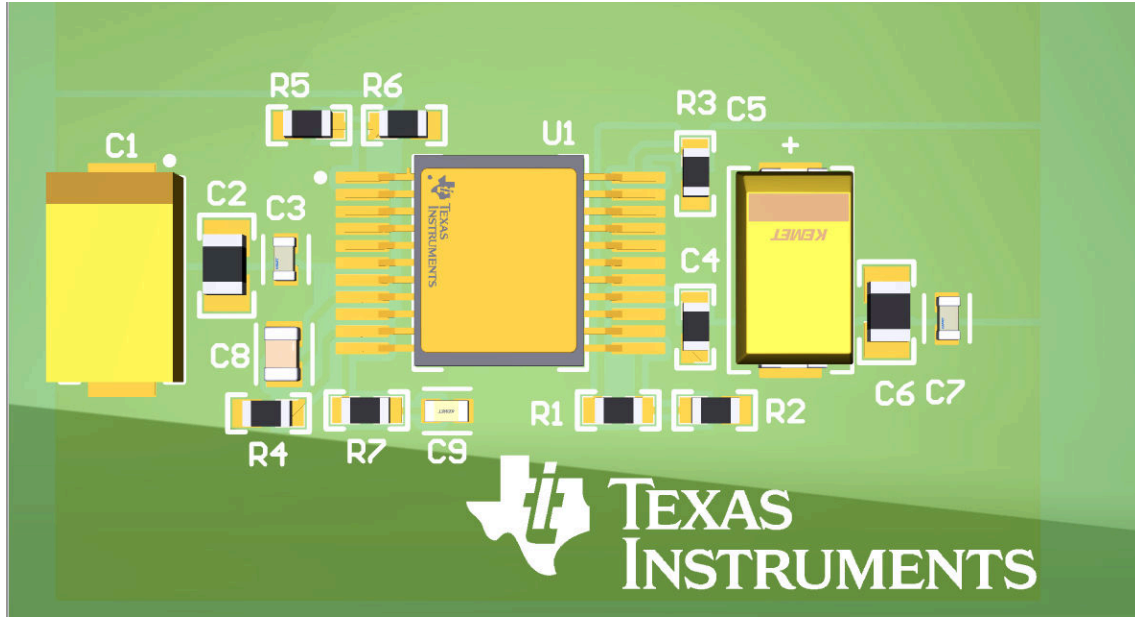


図 9-4. Printed Circuit Board Layout Example



☒ 9-5. Printed Circuit Board Layout Example: 3D View

10 Device and Documentation Support

10.1 Device Support

10.1.1 サード・パーティ製品に関する免責事項

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10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [TI Engineering Evaluation Units vs. MIL-PRF-38535 QML Class V Processing \(SLYB235\)](#)
- Texas Instruments, [Demystifying Type II and Type III Compensators Using Op-Amp and OTA for DC/DC Converters \(SLVA662\)](#)
- Texas Instruments, [TPS7H1121EVM-CVAL Evaluation Module \(EVM\) \(SLVUCX9\)](#)
- Texas Instruments, [How to Calculate the Load Pole and ESR Zero When Using Hybrid Output Capacitors \(SLVAE26\)](#)

10.3 ドキュメントの更新通知を受け取る方法

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10.7 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2024) to Revision A (September 2024)	Page
• TPS7H1121-SP の QMLV を「事前情報」から「量産データ」に変更.....	1
• 「デバイスの情報」表の部品番号 5962R2320301VXC の製品プレビューを削除。.....	1
• Removal of "Product Preview" note for Orderable Part Number 5962R2320301VXC in the Device Options Table.....	3
• Adjusted Enable threshold values and Programmable Current Limit min and max values.....	6
• Added parameter measurement diagrams for Enable Propagation Delay ($t_{EN(\text{delay})}$) and Soft Start Time (t_{SS}).	16
• Updated equation 12.....	27
• New frequency compensation application section in detailed design procedure.....	30

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R2320301VXC	ACTIVE	CFP	HFT	22	25	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R2320301VXC TPS7H1121MHFTV	Samples
TPS7H1121HFT/EM	ACTIVE	CFP	HFT	22	15	RoHS-Exempt & Green	NIAU	N / A for Pkg Type	25 to 25	TPS7H1121HFT EVAL ONLY	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962R2320301VXC	HFT	CFP	22	25	506.98	32.77	9910	NA
TPS7H1121HFT/EM	HFT	CFP	22	15	506.98	32.77	9910	NA

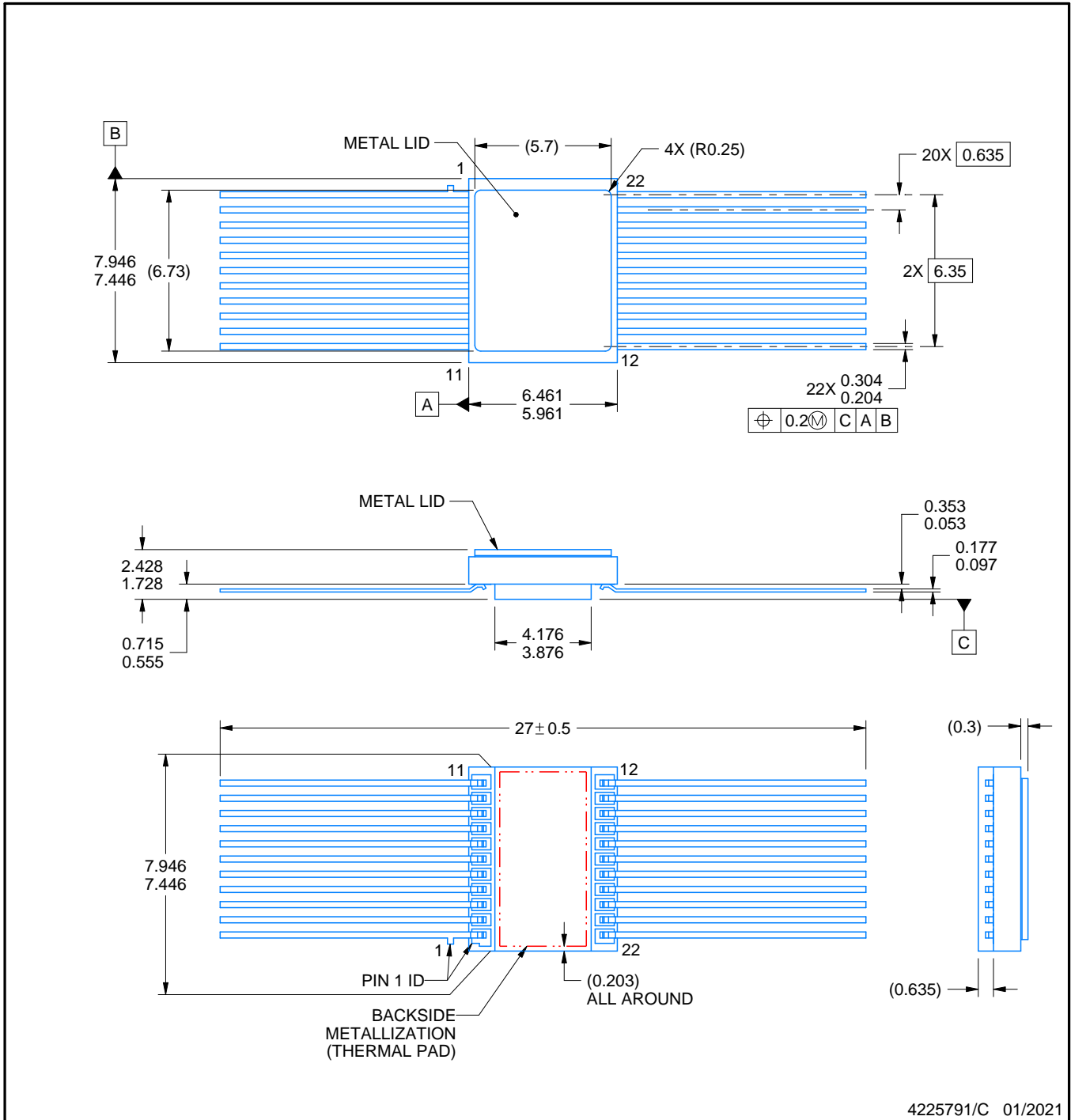
HFT0022A



PACKAGE OUTLINE

CFP - 2.428mm max height

CERAMIC FLATPACK



4225791/C 01/2021

NOTES:

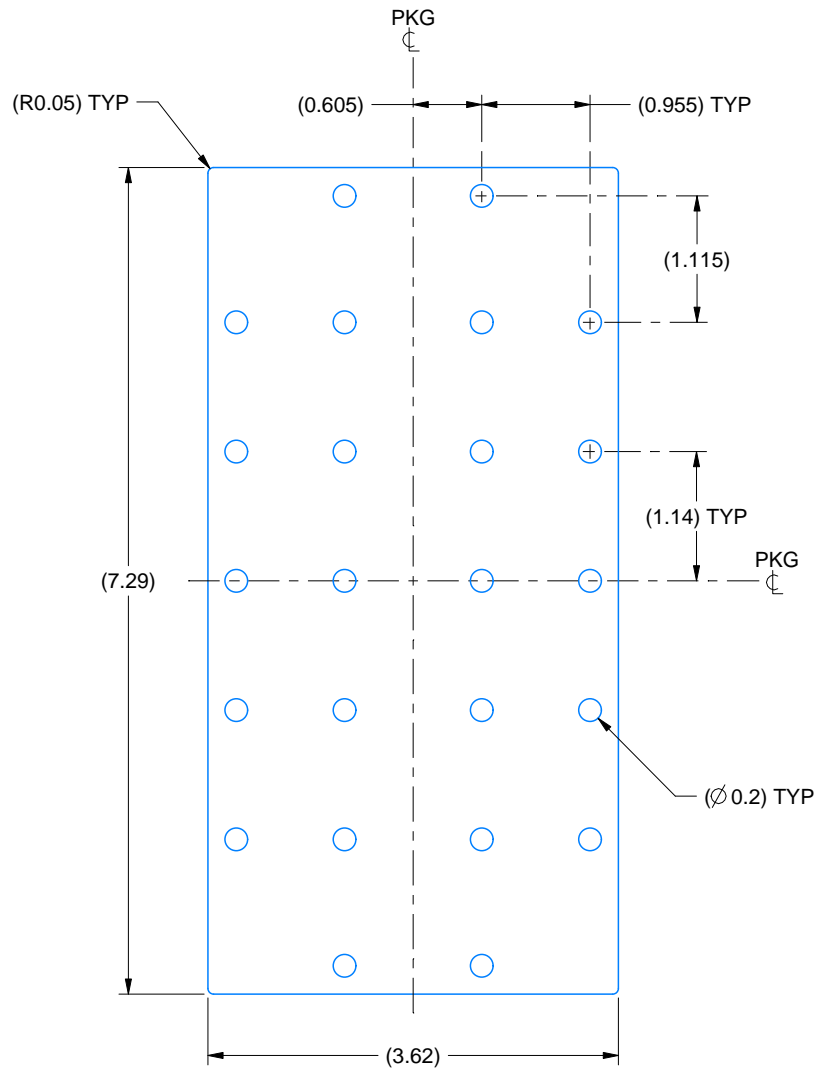
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid is not connected to any lead.
4. The leads are gold plated.
5. Metal lid is connected to backside metallization

EXAMPLE BOARD LAYOUT

HFT0022A

CFP - 2.428mm max height

CERAMIC FLATPACK



HEATSINK LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

4225791/C 01/2021

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2186323	03/13/2020	R. RAZAK / ANIS FAUZI
B	ADD LAND PATTERN VIEW / SHEET	2190485	10/22/2020	R. RAZAK / ANIS FAUZI
C	UPDATE TOTAL LEAD LENGTH TO 27 ± 0.5	2192775	01/28/2021	R. RAZAK / ANIS FAUZI

GENERIC PACKAGE VIEW

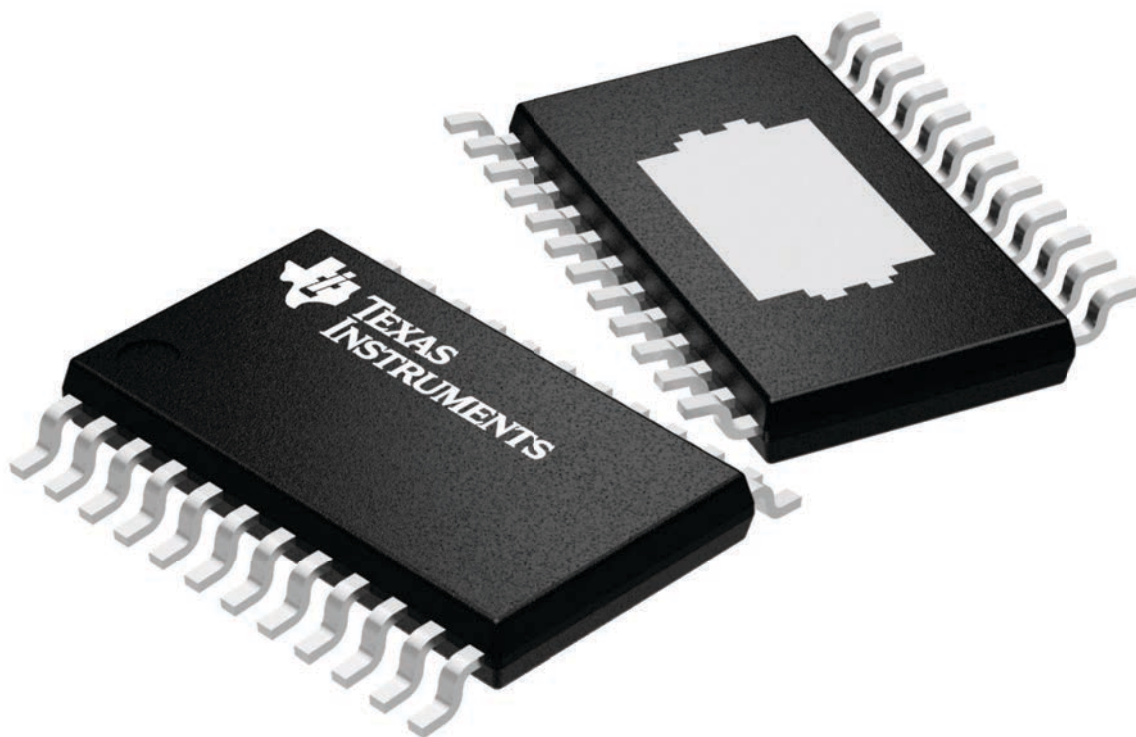
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

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