

TPS7B770x-Q1 車載用、シングルおよびデュアル・チャンネル、電流センス付きアンテナLDO

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
 - デバイス温度グレード1: 動作時周囲温度範囲 $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
 - デバイスHBM ESD分類レベル2
 - デバイスCDM ESD分類レベルC4B
- シングルおよびデュアル・チャンネルLDO、電流センスおよび可変電流制限付き
- 4.5V~40Vの広い入力電圧範囲、45Vの負荷ダンブ
- パワー・スイッチ・モード(FBをGNDに接続)
- 出力電圧は1.5V~20Vまで可変
- チャンネルごとに最大300mAの出力電流
- 外付け抵抗により電流制限を変更可能
- 高精度の電流センスにより、追加の較正を必要とせず、低電流時にアンテナのオープン状況を検出
- 高い電源除去率: 100Hzで73dB (標準値)
- 逆極性保護を内蔵、最低-40Vまで対応し、外付けダイオード不要
- 100mA負荷において最大ドロップアウト電圧 500mV
- 2.2 μF ~100 μF の範囲の出力コンデンサで安定 (ESR 1m Ω ~5 Ω)
- 保護および診断機能を内蔵
 - サーマル・シャットダウン
 - 低電圧誤動作防止(UVLO)
 - 短絡保護
 - バッテリ逆極性保護
 - 逆電流保護
 - 出力からバッテリへの短絡保護
 - 出力の誘導性負荷クランプ
 - 電流センス出力のチャンネル間およびデバイス間多重化
 - 電流センスによりすべてのフォルトを特定可能
- 16ピンHTSSOP PowerPAD™パッケージで供給

2 アプリケーション

- インフォテインメント用のアクティブ・アンテナ電源
- サラウンド・ビュー・カメラの電源
- 小電流アプリケーション用のハイサイド・パワー・スイッチ

3 概要

TPS7B770x-Q1ファミリのデバイスには、シングルおよびデュアルの高電圧で、電流センス機能付きの低ドロップアウト・レギュレータ(LDO)が搭載されており、4.5V~40Vの広い入力電圧範囲で動作するよう設計されています(負荷ダンブ保護45V)。これらのデバイスは、同軸ケーブル経由でアクティブ・アンテナの低ノイズ・アンプを駆動し、チャンネルごとに300mAの電流を供給します。また、各チャンネルの出力電圧は1.5V~20Vの範囲で調整可能です。

これらのデバイスは、電流センスおよびエラー・ピンにより診断を行えます。負荷電流を監視するため、ハイサイドの電流センス回路は、検出した負荷電流に比例したアナログ信号を出力します。正確な電流センスにより、追加の較正の必要なしに、オープン、通常、短絡の状況を検出できます。アナログ/デジタル・コンバータ(ADC)のリソースを節約するため、チャンネル間およびデバイス間で電流センスを多重化できます。各チャンネルの電流制限は、外付けの抵抗を使用して変更が可能です。

逆極性保護ダイオードが内蔵されているため、外付けのダイオードは不要です。これらのデバイスには、標準のサーマル・シャットダウン、出力からバッテリへの短絡保護、および逆電流保護機能が搭載されています。各チャンネルの出力には誘導性クランプ保護が搭載されており、誘導性スイッチのオフ時に動作します。

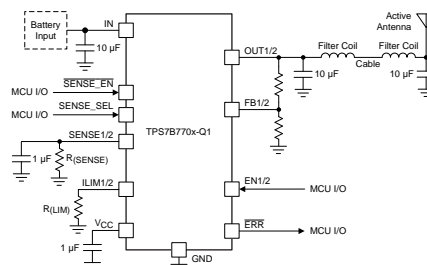
これらのデバイスは、 $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ の周囲温度範囲で動作します。

製品情報⁽¹⁾

| 型番 | パッケージ | チャンネル |
|--------------|-------------|-------|
| TPS7B7701-Q1 | HTSSOP (16) | シングル |
| TPS7B7702-Q1 | HTSSOP (16) | デュアル |

(1) 提供されているすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。

アプリケーション図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

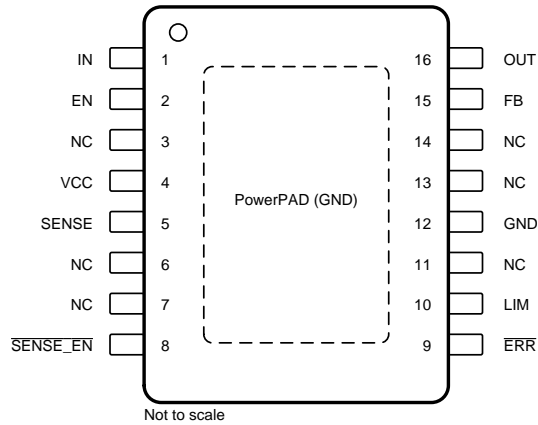
| Revision B (November 2015) から Revision C に変更 | Page |
|--|------|
| • Changed NC pin description in <i>Pin Functions</i> table to clarify which pins are internally connected | 3 |
| • Added row to <i>Recommended Operating Conditions</i> for OUT1, OUT2, and OUT regarding switched-mode operation | 4 |
| • 変更 <i>Current-Limit Resistor Selection</i> section for clarity | 17 |

| Revision A (May 2015) から Revision B に変更 | Page |
|---|------|
| • Deleted the min and max limits of –4% and 4% from the current-limit threshold voltage parameter in the <i>Electrical Characteristics</i> table | 6 |
| • Added to the current-limit accuracy table note for the programmable current-limit accuracy parameter in the <i>Electrical Characteristics</i> table | 6 |
| • 追加 graphs for the TPS7B7701-Q1 device in the <i>Typical Characteristics</i> section | 7 |
| • 削除 the channel 2 PSRR graph in the <i>Typical Characteristics</i> section | 7 |
| • 追加 additional test conditions for the 9- to 16-V <i>Line Transient</i> and <i>Power Up</i> graphs in the <i>Typical Characteristics</i> section | 9 |
| • 追加 additional test conditions of the <i>Power Up</i> graphs in the <i>Application Curves</i> section | 18 |

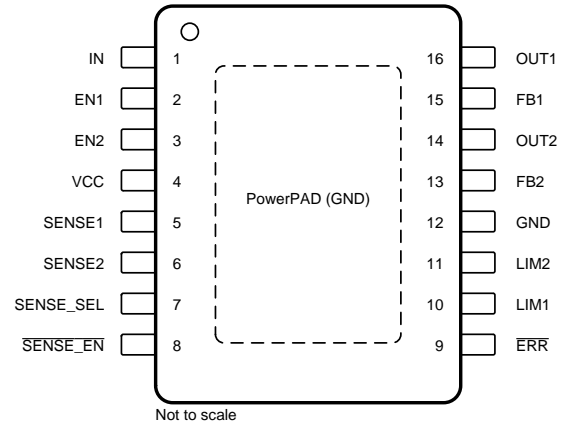
| 2015年1月発行のものから更新 | Page |
|------------------------------|------|
| • データシートのフル・バージョンをリリース | 1 |

5 Pin Configuration and Functions

Single-Channel TPS7B7701-Q1 PWP Package
16-Pin HTSSOP With PowerPAD
Top View



Dual-Channel TPS7B7702-Q1 PWP Package
16-Pin HTSSOP With PowerPAD
Top View



Pin Functions

| NAME | PIN | | TYPE | DESCRIPTION |
|-----------------|----------------|--------------|--------|--|
| | SINGLE-CHANNEL | DUAL-CHANNEL | | |
| EN | 2 | — | Input | Active-high enable input for the OUT pin with internal pulldown. |
| EN1 | — | 2 | Input | Active-high enable input for the OUT1 pin with internal pulldown. |
| EN2 | — | 3 | Input | Active-high enable input for the OUT2 pin with internal pulldown. |
| ERR | 9 | 9 | Output | This pin is an open-drain fault indicator for general faults. |
| FB | 15 | — | Input | Feedback input for setting OUT voltage. Connect FB to GND for current-limited switch operation. |
| FB1 | — | 15 | Input | Feedback input for setting OUT1 voltage. Connect FB1 to GND for current-limited switch operation. |
| FB2 | — | 13 | Input | Feedback input for setting OUT2 voltage. Connect FB2 to GND for current-limited switch operation. |
| GND | 12 | 12 | Ground | Ground reference |
| IN | 1 | 1 | Power | Input power-supply voltage |
| LIM | 10 | — | Output | Programmable current-limit pin. Connect a resistor to GND to set the current limitation level. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND. |
| LIM1 | — | 10 | Output | Programmable current-limit pin for channel 1. Connect a resistor to GND to set the current limitation level for channel 1. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND. |
| LIM2 | — | 11 | Output | Programmable current-limit pin for channel 2. Connect a resistor to GND to set the current limitation level for channel 2. This pin does not need an external capacitor. To set to internal current limit, short this pin to GND. |
| NC | 3, 13, 14 | — | — | Not connected. Connect the NC pins to ground or leave floating. |
| | 6, 7, 11 | — | — | Internally connected. These pins must either be floated or connected to GND. |
| OUT | 16 | — | Power | Output voltage |
| OUT1 | — | 16 | Power | Output voltage 1 |
| OUT2 | — | 14 | Power | Output voltage 2 |
| SENSE | 5 | — | Output | Output of current sense for sensing. To set the SENSE output voltage level, connect a resistor between this pin and GND. In addition, connect a 1- μ F capacitor from this pin to GND for frequency compensation of the current-sense loop. Short this pin to GND if not used. |
| SENSE1 | — | 5 | Output | Output of current sense for sensing. SENSE1 current is proportional to the current flow through OUT1 and SENSE 2 current is proportional to OUT2 current when SENSE_SEL and SENSE_EN are low. To set the SENSEx output voltage level, connect a resistor between this pin and GND. In addition, connect a 1- μ F capacitor from the SENSEx pin to GND for frequency compensation of the current-sense loop. Short the SENSEx pin to GND if not used. |
| SENSE2 | — | 6 | Output | |
| SENSE_EN | 8 | 8 | Input | This pin is the enable and disable of the current-sense pin for multiplexing, active-low enable. |
| SENSE_SEL | — | 7 | Input | This pin selects the current sense between channel 1 and channel 2. See Table 2 for details. |
| V _{CC} | 4 | 4 | Output | Internal 4.5-V regulator. Connect 1- μ F ceramic capacitor between V _{CC} and GND for frequency compensation. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--|--|------|-----------------------|------|
| Input voltage | Unregulated input, IN | -40 | 45 | V |
| | EN, EN1, and EN2 | -0.3 | 45 | V |
| Regulated output ⁽²⁾ | V _{CC} ⁽³⁾⁽⁴⁾ | -0.3 | 6 | V |
| | OUT1 and OUT2 | -0.3 | 45 | V |
| Low-voltage pins | SENSE, SENSE1, and SENSE2 ⁽³⁾⁽⁴⁾ | -0.3 | V _{CC} + 0.3 | V |
| | LIM, LIM1, LIM2, $\overline{\text{SENSE_EN}}$, SENSE_SEL, $\overline{\text{ERR}}$, FB, FB1, and FB2 ⁽³⁾⁽⁴⁾ | -0.3 | 7 | V |
| Operating junction temperature, T _J | | -40 | 150 | °C |
| Operating ambient temperature, T _A | | -40 | 125 | °C |
| Storage Temperature, T _{stg} | | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) There is an internal diode connects between the OUT and GND pins with 300-mA DC current capability for inductive clamp protection.
- (3) All voltage values are with respect to GND.
- (4) Absolute maximum voltage.

6.2 ESD Ratings

| | | VALUE | UNIT | |
|--|---|-------------------------------|------|------|
| V _(ESD) Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | V | |
| | Charged device model (CDM), per AEC Q100-011 | Corner pins (1, 8, 9, and 16) | | ±750 |
| | | Other pins | | ±500 |

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|-------------------------|--|-----------------------|-----|------|
| V _I | Unregulated input | 4.5 | 40 | V |
| | EN, EN1, and EN2 | 0 | 40 | V |
| Low-voltage pins | SENSE, SENSE1, SENSE2, $\overline{\text{SENSE_EN}}$, SEN_SEL, $\overline{\text{ERR}}$, FB, FB1, FB2, LIM, LIM1, LIM2, and V _{CC} | 0 | 5.3 | V |
| | OUT1, OUT2, and OUT | Normal-mode operation | 1.5 | 20 |
| Switched-mode operation | | 1.5 | 35 | |
| C _O | Output capacitor stability range | 2.2 | 100 | μF |
| C _{O(ESR)} | Output capacitor ESR stability range | 0.001 | 5 | Ω |
| T _J | Junction temperature | -40 | 150 | °C |
| T _A | Ambient temperature | -40 | 125 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TPS7B7701-Q1 | TPS7B7702-Q1 | UNIT |
|-------------------------------|---|--------------|--------------|------|
| | | PWP (HTSSOP) | PWP (HTSSOP) | |
| | | 16 PINS | 16 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance ⁽²⁾ | 45.9 | 40.3 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 29.2 | 27.7 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 24.7 | 22.3 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 1.3 | 0.8 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 24.5 | 22 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 3.7 | 2.7 | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) The thermal data is based on JEDEC standard high K profile – JESD 51-7. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated

6.5 Electrical Characteristics

at V_I = 14 V and T_J = –40°C to +150°C (unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|---|-----|-------|-----|------|
| SUPPLY VOLTAGE AND CURRENT (IN) | | | | | | |
| V _I | Input voltage | | 4.5 | | 40 | V |
| I _Q | Quiescent current | TPS7B7701-Q1: V _I = 4.5 to 40 V, V _(EN) ≥ 2 V, I _(OUT) = 0.1 mA TPS7B7702-Q1: V _I = 4.5 to 40 V, V _(EN1) and V _(EN2) ≥ 2 V, I _(OUT1) and I _(OUT2) = 0.1 mA | | 0.6 | 1 | mA |
| I _(shutdown) | Shutdown current | TPS7B7701-Q1: EN = GND TPS7B7702-Q1: EN1 = EN2 = GND | | | 5 | μA |
| I _{nom} | Operating current | TPS7B7701-Q1: V _(EN) ≥ 2 V, I _(OUT) ≤ 300 mA, GND current TPS7B7702-Q1: V _(EN1) and V _(EN2) ≥ 2 V, I _(OUT1) and I _(OUT2) ≤ 300 mA, GND current | | | 4.5 | mA |
| V _(BG) | Bandgap | Reference voltage for FB | –2% | 1.233 | 2% | V |
| V _(UVLO) | Undervoltage lockout falling | Ramp IN down until the output turns off | | | 4 | V |
| V _{hys} | Hysteresis | | | 0.4 | | V |
| INPUT CONTROL PINS (EN, EN1, EN2, SENSE_EN, AND SENSE_SEL) | | | | | | |
| V _{IL} | Logic input low level | For EN, EN1, EN2, SENSE_EN, and SENSE_SEL | 0 | | 0.7 | V |
| V _{IH} | Logic input high level | For EN, EN1, EN2, SENSE_EN, and SENSE_SEL | 2 | | | V |
| I _{I(SENSE_EN)} | SENSE_EN input current | V _(SENSE_EN) = 5 V, V _(ENx) ≥ 2 V | | | 10 | μA |
| I _{I(SENSE_SEL)} | SENSE_SEL input current | V _(SENSE_EN) = 5 V, V _(ENx) ≥ 2 V | | | 10 | μA |
| I _{I(EN)} | Enable input current | V _(ENx) ≤ 40 V | | | 10 | μA |
| REGULATED OUTPUT (OUT, OUT1, AND OUT2) | | | | | | |
| V _O | Regulated output | 40 V ≥ V _I ≥ V _O + 1.5 V and V _I ≥ 4.5 V, I _O = 1 to 300 mA ⁽¹⁾ | –2% | | 2% | |
| ΔV _{O(ΔVI)} | Line regulation | V _I = V _O + 1.5 V to 40 V and V _I ≥ 6 V, I _O = 10 mA, voltage variation on FB pin | | | 10 | mV |
| ΔV _{O(ΔIO)} | Load regulation | I _O = 1 mA to 200 mA, voltage variation on FB pin | | | 20 | mV |
| V _(DROPOUT) | Dropout voltage | Measured between IN and OUTx, I _O = 100 mA | | | 500 | mV |
| I _O | Output current | V _O in regulation | 0 | | 300 | mA |
| PSRR | Power supply ripple rejection ⁽²⁾ | I _O = 100 mA, C _O = 2.2 μF, f = 100 Hz | | 73 | | dB |
| CURRENT SENSE AND CURRENT-LIMIT | | | | | | |
| I _O /I _{SENSE} | OUTx to SENSEx current ratio (I _O / I _{SENSEx}) | V _I = 4.5 V to 40 V, 5 mA ≤ I _O ≤ 300 mA | | 198 | | |

- (1) External feedback resistor is not considered.
- (2) Design information; specified by design, not production tested.

Electrical Characteristics (continued)

 at $V_I = 14\text{ V}$ and $T_J = -40^\circ\text{C}$ to $+150^\circ\text{C}$ (unless otherwise stated)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|---------------------------------------|--|--|-----|-------|------|------------------|
| OUTx to SENSEx current ratio accuracy | $I_O = 100$ to 300 mA | -3% | | 3% | | |
| | $I_O = 50$ to 100 mA | -5% | | 5% | | |
| | $I_O = 10$ to 50 mA | -10% | | 10% | | |
| | $I_O = 5$ to 10 mA | -20% | | 20% | | |
| I_O/I_{LIM} | OUTx to LIMx current ratio (I_O / I_{LIM}) | $V_I = 4.5\text{ V}$ to 40 V , $50\text{ mA} \leq I_{(LIMx)} \leq 300\text{ mA}$ | | 198 | | |
| $I_{(LIMx)}$ | Programmable current-limit accuracy ⁽³⁾ | $V_I = 4.5\text{ V}$ to 40 V , $50\text{ mA} \leq I_{(LIMx)} \leq 300\text{ mA}$ | | -8% | 8% | |
| $I_{L(LIMx)}$ | Internal current-limit | LIMx shorted to GND | | 340 | 550 | |
| I_{lkg} | SENSE, SENSE1, SENSE2, LIM, LIM1, and LIM2 leakage current | ENx = GND, $T_A = 25^\circ\text{C}$ | | | 2 | |
| $V_{(LIMx_th)}$ | Current-limit threshold voltage | Voltage on the LIM, LIM1, and LIM2 pins when output current is limited | | 1.233 | V | |
| $V_{(SENSEx_stb)}$ | Current-sense short-to-battery fault voltage | When short-to-battery or reverse current conditions are detected | | 3.05 | 3.2 | 3.3 |
| $V_{(SENSEx_tsd)}$ | Current-sense thermal shutdown fault voltage | When thermal shutdown is detected | | 2.7 | 2.85 | 3 |
| $V_{(SENSEx_cl)}$ | Current-sense current-limit fault voltage | When current-limit conditions are detected | | 2.4 | 2.55 | 2.65 |
| $I_{(SENSEx_H)}$ | Current-sense fault condition current | When short-to-battery, reverse current, thermal shutdown, or current-limit conditions are detected | | 3.3 | | mA |
| FAULT DETECTION | | | | | | |
| $V_{(stb_th)}$ | Short-to-battery threshold | $V_{(OUTx)} - V_I$, checked during turnon sequence | | -500 | -55 | 110 |
| $I_{(REV)}$ | Reverse current detection level | Power FET on (SW or LDO mode) | | -100 | -40 | -1 |
| T_{SD} | Thermal shutdown | Junction temperature | | | 175 | $^\circ\text{C}$ |
| $T_{SD(hys)}$ | Thermal shutdown hysteresis | | | | 15 | $^\circ\text{C}$ |
| INTERFACE CIRCUITRY | | | | | | |
| V_{OL} | $\overline{\text{ERR}}$ output low | $I_{(SINK)} = 5\text{ mA}$ | | | 0.4 | V |
| I_{lkg} | $\overline{\text{ERR}}$ open-drain leakage current | $\overline{\text{ERR}}$ high impedance, 5-V external voltage is applied at $\overline{\text{ERR}}$ | | | 1 | μA |
| $R_{(OUTx_off)}$ | OUT pulldown resistor ⁽²⁾ | ENx = GND | | | 50 | k Ω |
| $I_{R(lkg)}$ | Reverse leakage current | $-40\text{ V} < V_I < 0\text{ V}$, reverse current to IN | | | 0.6 | mA |
| V_{CC} | Internal voltage regulator | $V_I = 5.5$ to 40 V , $I_{CC} = 0\text{ mA}$ | | 4.25 | 4.5 | 4.75 |
| $I_{CC(lim)}$ | Internal voltage-regulator current-limit | | | 15 | | 70 |

(3) The current-limit accuracy is maintained when the current limit is set between 50 mA and 300 mA, and it includes the deviation of the current-limit threshold voltage $V_{(LIMx_th)}$.

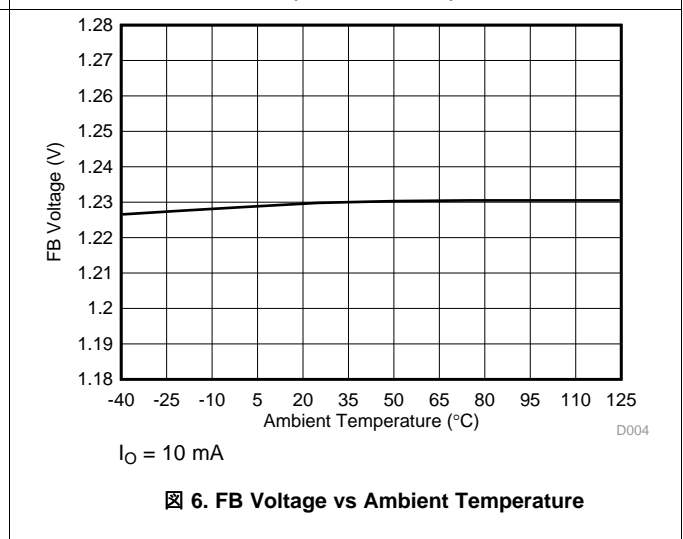
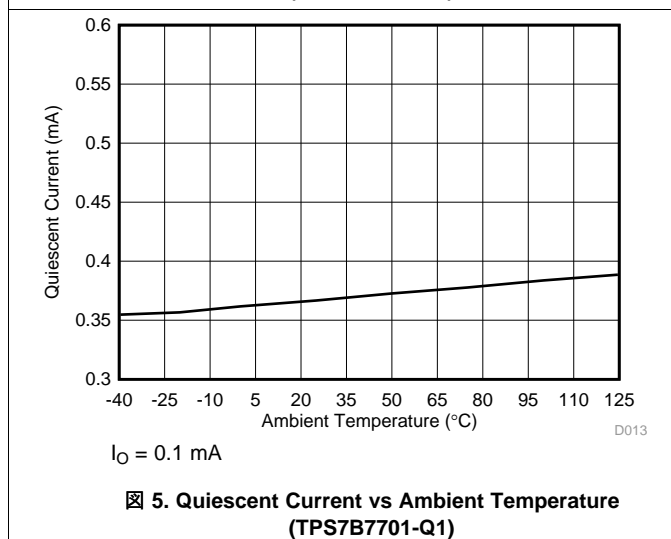
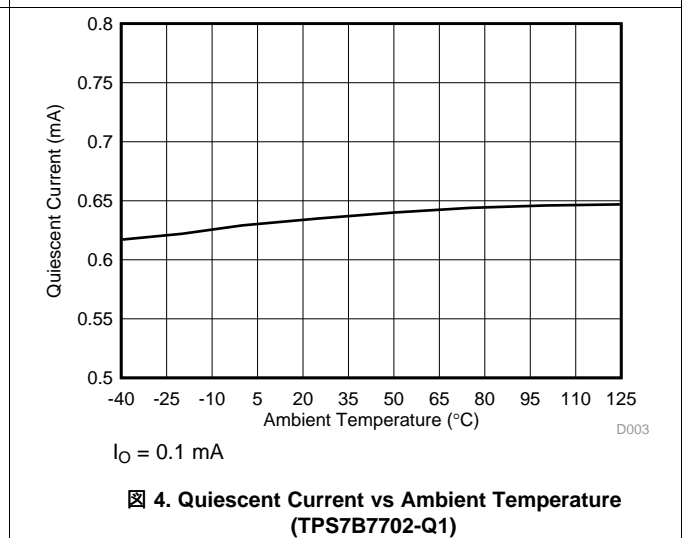
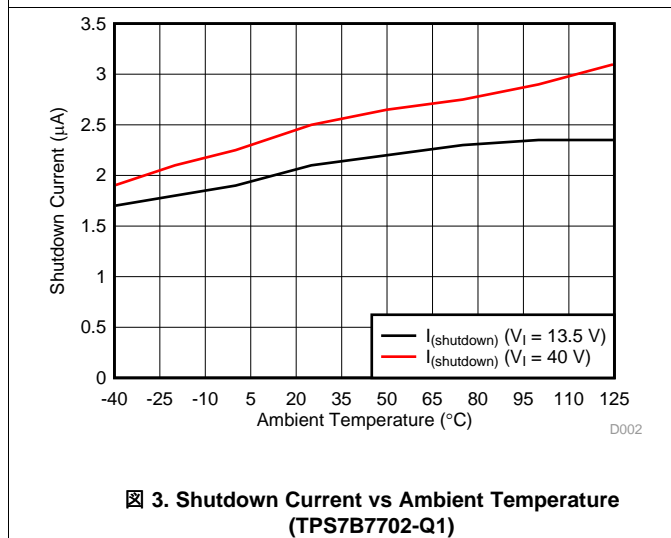
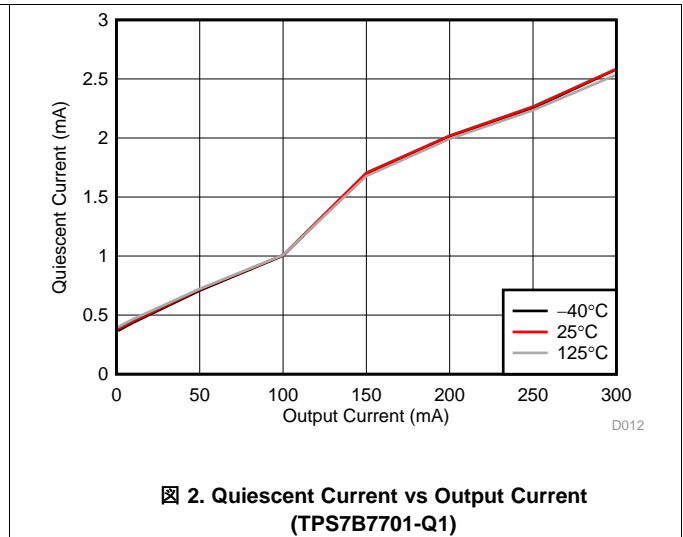
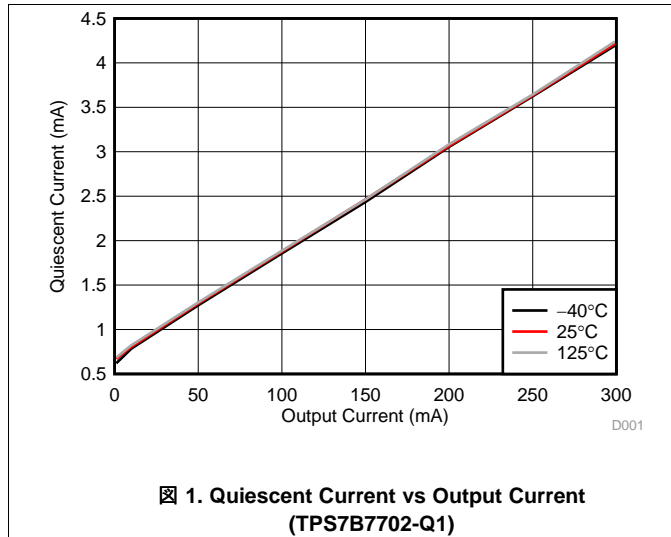
6.6 Switching Characteristics

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|--|---|-----|-----|------|---------------|
| CURRENT SENSE AND CURRENT-LIMIT | | | | | | |
| $t_{d(SENSE_SEL_r)}$ | Current-sense delay time from the rising edge of SENSE_SEL ⁽¹⁾ | $V_{(ENx)} \geq 2\text{ V}$, $\overline{\text{SENSE_EN}} = \text{GND}$, SENSE_SEL rise from 0 to 5 V | | | 10 | μs |
| $t_{d(SENSE_SEL_f)}$ | Current-sense delay time from the falling edge of SENSE_SEL ⁽¹⁾ | $V_{(ENx)} \geq 2\text{ V}$, $\overline{\text{SENSE_EN}} = \text{GND}$, SENSE_SEL fall from 5 to 0 V | | | 10 | μs |
| $t_{d(SENSE_EN_r)}$ | Current-sense delay time from rising edge of SENSE_EN ⁽¹⁾ | $V_{(ENx)} \geq 2\text{ V}$, $\overline{\text{SENSE_EN}}$ rise from 0 to 5 V | | | 10 | μs |
| $t_{d(SENSE_EN_f)}$ | Current-sense delay time from falling edge of SENSE_EN ⁽¹⁾ | $V_{(ENx)} \geq 2\text{ V}$, $\overline{\text{SENSE_EN}}$ fall from 5 to 0 V | | | 10 | μs |
| FAULT DETECTION | | | | | | |
| $t_{(PD_RC)}$ | Reverse current (Short-to-BAT) shutdown deglitch time | Delay to shut down the switch or LDO after a drop over r_{on} becomes negative, $I_{(OUTx)} = -200\text{ mA}$ (typical), $T_A = 25^\circ\text{C}$ | | | 5 | 20 |
| $t_{(BLK_RC)}$ | Reverse current blanking time | Blanking time for reverse-current detection after power up, the rising edge of the ENx pin, or the current limiting event is over | | | 16 | ms |

(1) Design information; specified by design; not production tested.

6.7 Typical Characteristics

at $V_I = 14\text{ V}$ (unless otherwise specified)



Typical Characteristics (continued)

at $V_I = 14\text{ V}$ (unless otherwise specified)

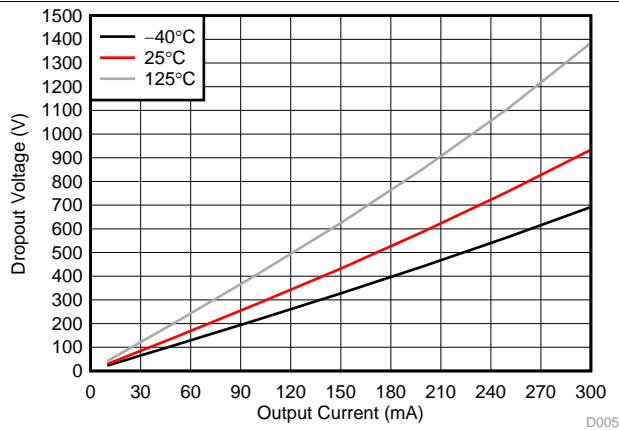
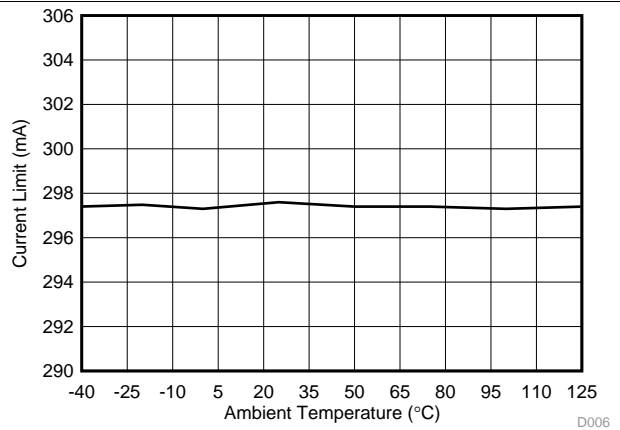


图 7. Dropout Voltage vs Output Current



$I_{LIM} = 300\text{ mA}$

图 8. Current Limit vs Ambient Temperature

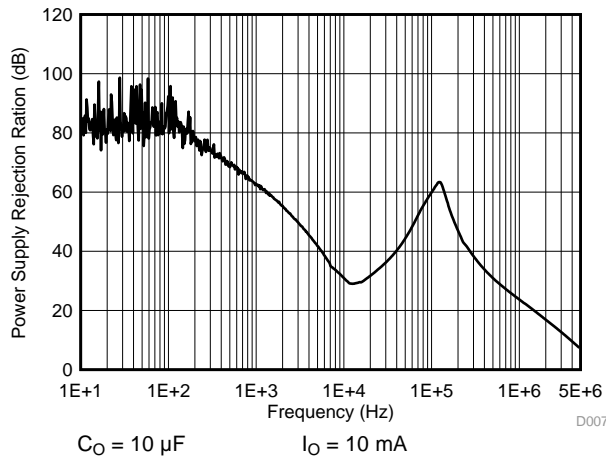


图 9. PSRR TPS7B770x-Q1

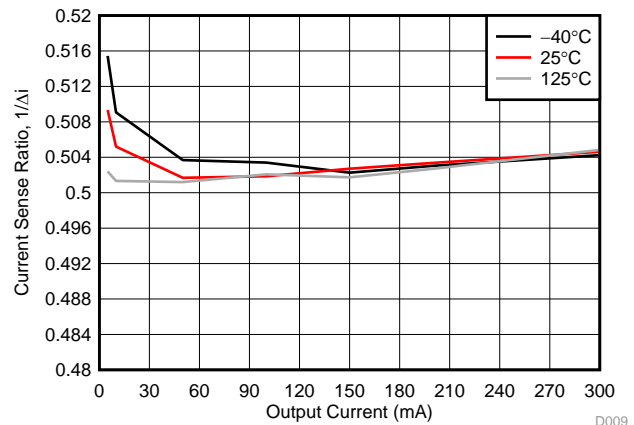


图 10. Current Sense Ratio vs Output Current, TPS7B7702-Q1 Channel 1

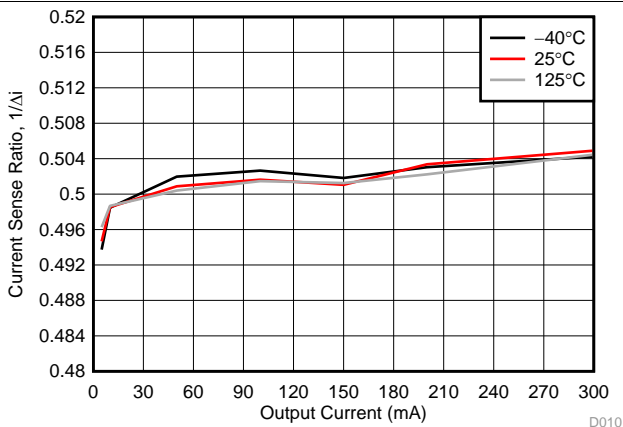


图 11. Current Sense Ratio vs Output Current, TPS7B7702-Q1 Channel 2

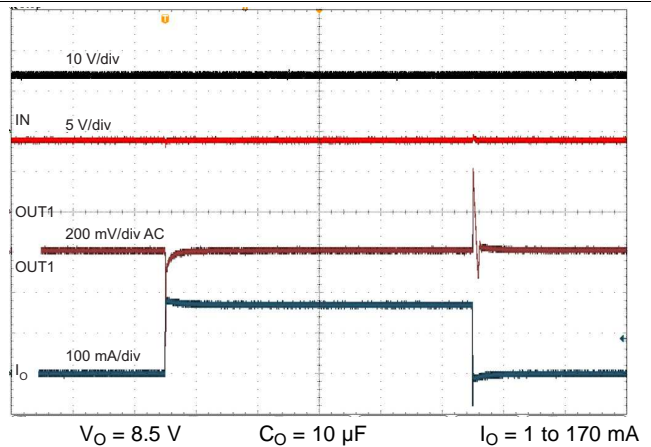
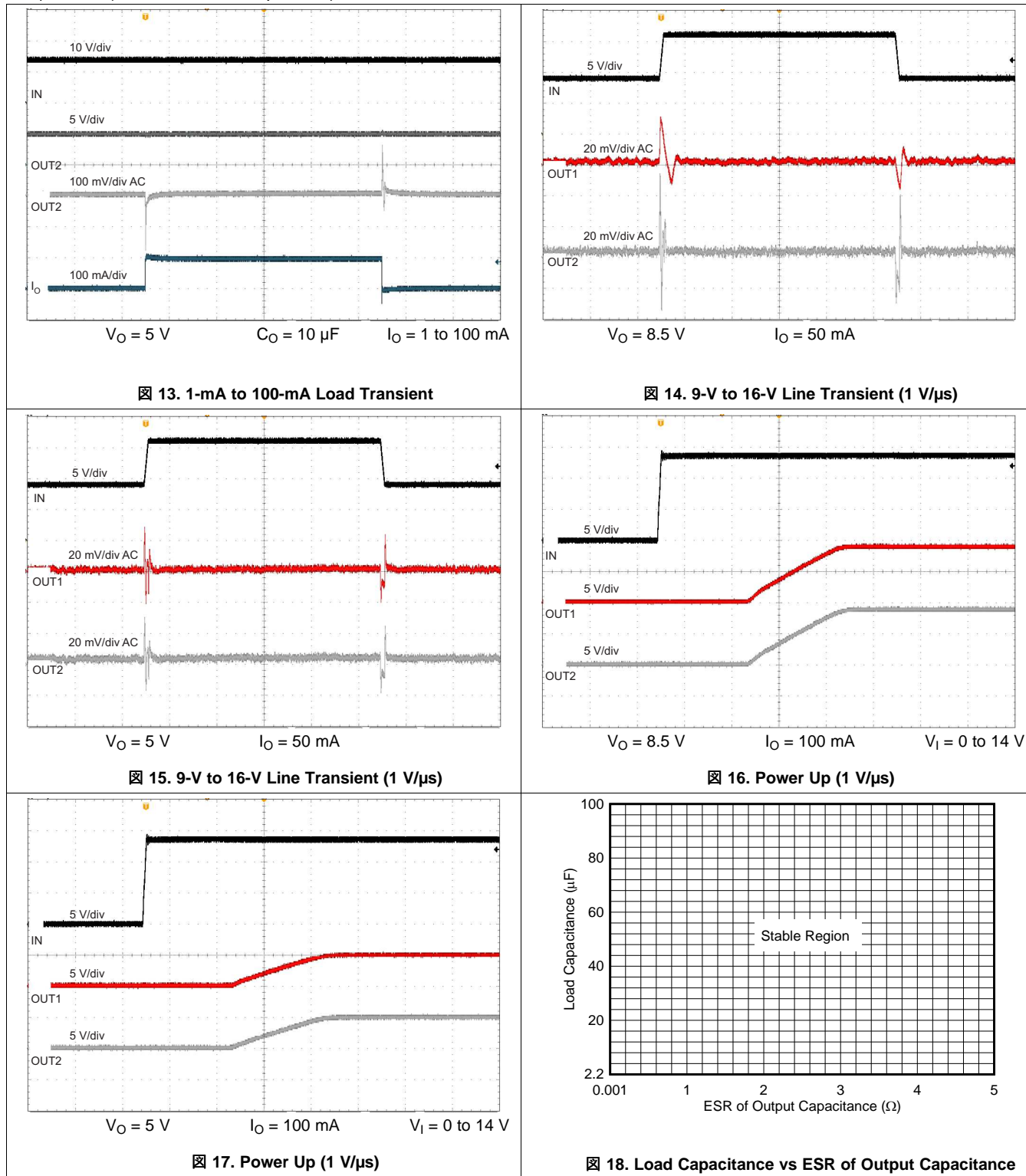


图 12. 1-mA to 170-mA Load Transient

Typical Characteristics (continued)

at $V_I = 14\text{ V}$ (unless otherwise specified)



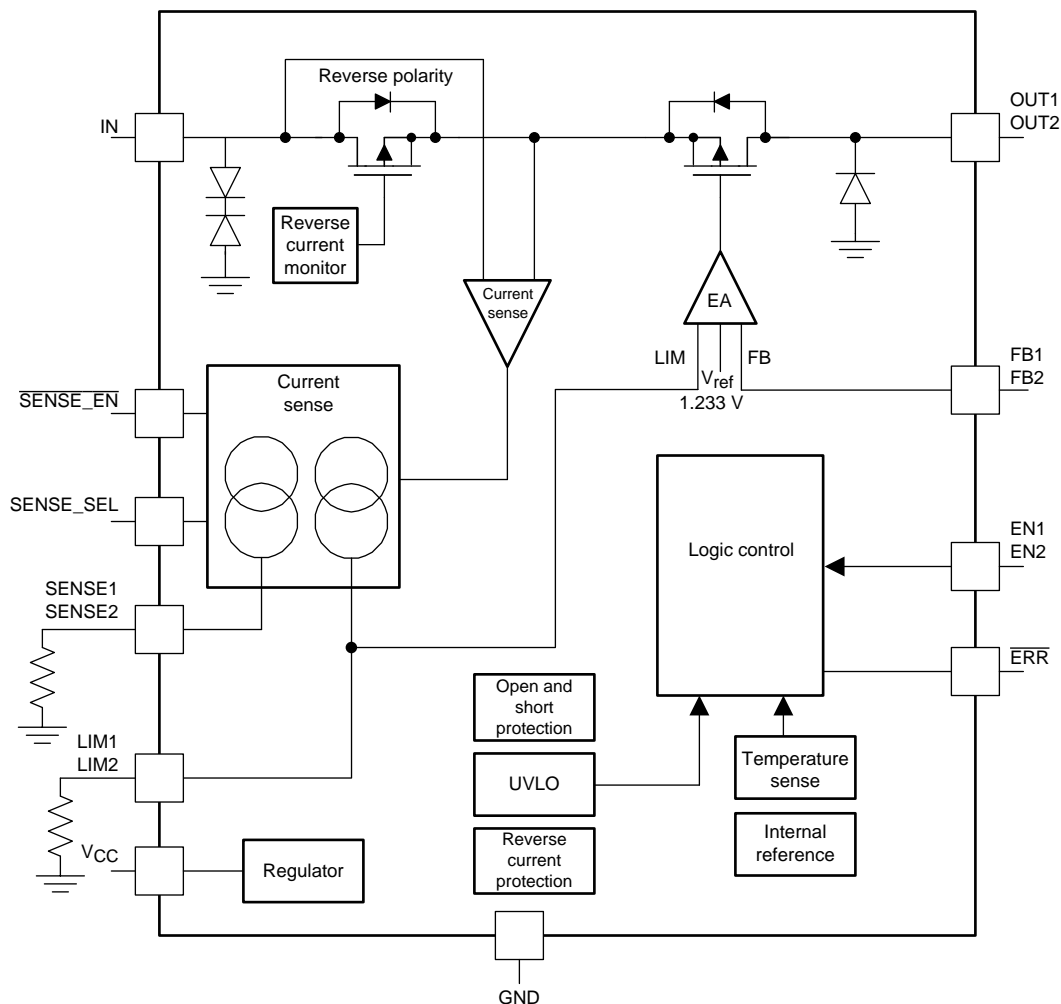
7 Detailed Description

7.1 Overview

The TPS7B770x-Q1 family of devices feature a single- or dual-channel, high voltage LDO with a current-sense function. These devices operate with a wide input-voltage range of 4.5 V to 40 V (45-V load dump protection). These devices also offers protection of antenna lines against electrostatic discharge (ESD) and from short-to-ground, short-to-battery, and thermal overstress. Device output voltage is adjustable from 1.5 V to 20 V through an external resistor divider. Alternatively, each channel can be configured as a switch.

These devices monitor the load. Accurate current sense allows for detection of open, normal, and short-circuit conditions without the need of further calibration. The current sense can also be multiplexed between channels and devices to save ADC resources. Each channel also provides an adjustable current limit with external resistor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fault Detection and Protection

The device includes both analog current sense and digital fault pins for full diagnostics of different fault conditions.

The current-sense voltage scale is selected based on the output-current range of interest. [Figure 19](#) shows a recommended setting that allows for full diagnostics of each fault. Before the device goes into current-limit mode, the output current-sense voltage is linearly proportional to the actual load current. During a thermal-shutdown (TSD) and short-to-battery (STB) condition, the current-sense voltage is set to the fault voltage level that is specified in the [Electrical Characteristics](#) table.

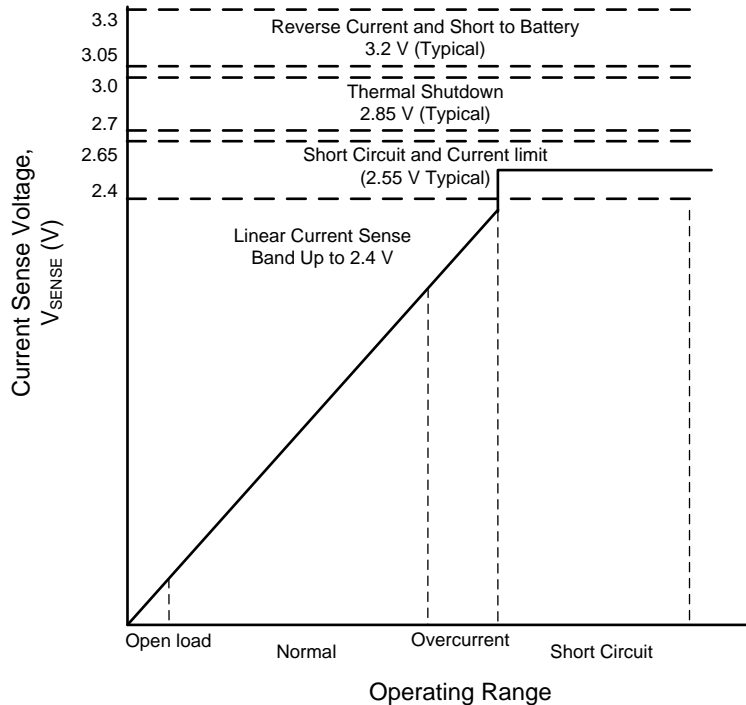


Figure 19. Functionality of the Current-Sense Output

7.3.2 Short-Circuit and Overcurrent Protection

The current limit on each channel is programmed by selecting the external resistor. The voltage on LIMx pin is compared with an internal voltage reference. When the threshold is exceeded, the current limit is triggered. The output of the current limited channel continues to remain on and the current is limited.

Under current-limit status, the \overline{ERR} pin asserts low and the SENSE voltage of the fault channel is internally pulled up to a voltage rail between 2.4 V and 2.65 V as shown in [Figure 19](#). At this moment, the output voltage is not disabled. The microcontroller (MCU) should monitor the voltage at the SENSEx pin or \overline{ERR} pin to disable the faulted channel by pulling the \overline{ENx} pin low. If a current-limit condition exists for a long period of time, thermal shutdown can be triggered and shutdown the output.

7.3.3 Short-to-Battery and Reverse Current Detection

Shorting the OUT pin to the battery because of a fault in the system is possible. Each channel detects this failure by comparing the voltage at the OUT and IN pins before the switch turns on. Each time the LDO switch is enabled on the rising edge of the EN pin or during the exiting of the thermal shutdown, the short-to-battery detection occurs. At this moment, if the device detects the short-to-battery fault, the LDO switch is latched off, the \overline{ERR} pin is asserted low, and the fault-channel SENSE voltage is pulled up internally to a voltage rail between 3.05 V and 3.3 V. The device operates normally when the short-to-battery is removed and the EN pin is toggled.

Feature Description (continued)

During normal operation if a short-to-battery fault results in reverse current for more than 5 μs (typical), the LDO switch is latched off and the $\overline{\text{ERR}}$ pin is asserted low. To remove the latched condition after a short-to-battery (reverse current) fault, the condition must first be removed and then the EN pin must be toggled.

Series inductance and the output capacitor can produce ringing during power up or recovery from current limit, resulting in an output voltage that temporarily exceeds the input voltage. The 16-ms (typical) reverse-current blanking can help filter this ringing.

For the dual-channel antenna LDO application, if both channels are enabled and one channel is shorted to ground after power up, the current drawn from the input capacitor can result in a temporary dip in the input voltage, which can trigger the reverse-current detection fault. To avoid this false trigger event, care must be taken when selecting the input capacitor; an increase of the input capacitor value is recommended.

7.3.4 Thermal Shutdown

The device incorporates a TSD circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output is turned off. When the junction temperature decreases by 15°C (typical) than the TSD trip point, the output is turned on again. The SENSE voltage is internally pulled up to a voltage rail between 2.7 V and 3 V during TSD status.

注

The purpose of the design of the internal protection circuitry of the TPS7B770x-Q1 family of devices is to protect against overload conditions and is not intended as a replacement for proper heat-sinking. Continuously running the device into thermal shutdown degrades device reliability.

7.3.5 Integrated Reverse-Polarity Protection

The device integrates a reverse-connected PMOS to block the reverse current during reverse polarity at the input and output short-to-battery condition. A special ESD structure at the input is specified to withstand -40 V .

7.3.6 Integrated Inductive Clamp

During output turnoff, the cable inductance continues to source the current from the output of the device. The device integrates an inductive clamp to help dissipate the inductive energy stored in the cable. An internal diode is connected between OUT and GND pins with a DC-current capability of 300 mA for inductive clamp protection.

7.3.7 Undervoltage Lockout

The device includes an undervoltage lockout (UVLO) threshold that is internally fixed. The undervoltage lockout activates when the input voltage on the IN pin drops below $V_{(\text{UVLO})}$. The UVLO makes sure that the regulator is not latched into an unknown state during low input-supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and then recovers, the regulator shuts down and powers up with a normal power-up sequence when the input voltage is above the required levels.

表 1. Fault Table

| FAILURE MODE | $V_{(\text{SENSE})}$ | $\overline{\text{ERR}}$ | LDO SWITCH OUTPUT | LATCHED |
|--------------------------------|---|-------------------------|-------------------|---------|
| Open load | $I_{\text{O}} \times R_{(\text{SENSE})}$ 198 | HIGH | Enabled | No |
| Normal | | HIGH | Enabled | No |
| Overcurrent | | HIGH | Enabled | No |
| Short-circuit or current limit | 2.4 to 2.65 V | LOW | Enabled | No |
| Thermal shutdown | 2.7 to 3 V | LOW | Disabled | No |
| Output short-to-battery | 3.05 to 3.3 V | LOW | Disabled | Yes |
| Reverse current | 3.05 to 3.3 V | LOW | Disabled | Yes |

7.3.8 Enable (EN, EN1, and EN2)

The TPS7B7702-Q1 device features two active-high enable inputs, EN1 and EN2. The EN1 pin controls output voltage 1, OUT1, and the EN2 pin controls output voltage 2, OUT2. The device consumes a maximum of shutdown current 5- μ A when the ENx pins are low. Both the EN1 and EN2 pins have a maximum internal pulldown of 10 μ A.

The TPS7B7701-Q1 device features one active-high enable input. The device consumes a maximum shutdown current of 5 μ A when the EN pin is low. The EN pin has a maximum internal pull down of 10 μ A.

7.3.9 Internal Voltage Regulator (V_{CC})

The device features an internal regulator that regulates the input voltage to 4.5 V to power all internal circuitry. Bypass a 1- μ F ceramic capacitor from the V_{CC} pin to the GND pin for frequency compensation. The V_{CC} pin can be used as a power supply for external circuitry with up to 15-mA current capability.

7.3.10 Current Sense Multiplexing

The two, independent current sense pins (one for each channel) provide flexibility in the system design. When the ADC resource is limited, the device allows the multiplexing of the current sense pins by only using one current sense pin and one ADC to monitor all the antenna outputs.

The SENSE_SEL pin (TPS7B7702-Q1 only) selects the channels to monitor the current. The $\overline{\text{SENSE_EN}}$ pin enables and disables the SENSE pin, allowing multiplexing between chips. Therefore, only one ADC and one resistor is needed for current-sense diagnostics of multiple outputs. When the SENSE1 pin is connected to an ADC, the current flow through both channels can be sensed by changing the electrical level at the SENSE_SEL pin.

表 2 lists the selection logic for the current sense.

表 2. $\overline{\text{SENSE_EN}}$ and SEN_SEL Logic Table

| $\overline{\text{SENSE_EN}}$ | SEN_SEL | SENSE1 Status | SENSE2 Status |
|-------------------------------|---------|----------------|----------------|
| LOW | LOW | CH1 current | CH2 current |
| LOW | HIGH | CH2 current | HIGH impedance |
| HIGH | — | HIGH impedance | HIGH impedance |

图 20 shows the application of four antenna channels sharing one ADC resource.

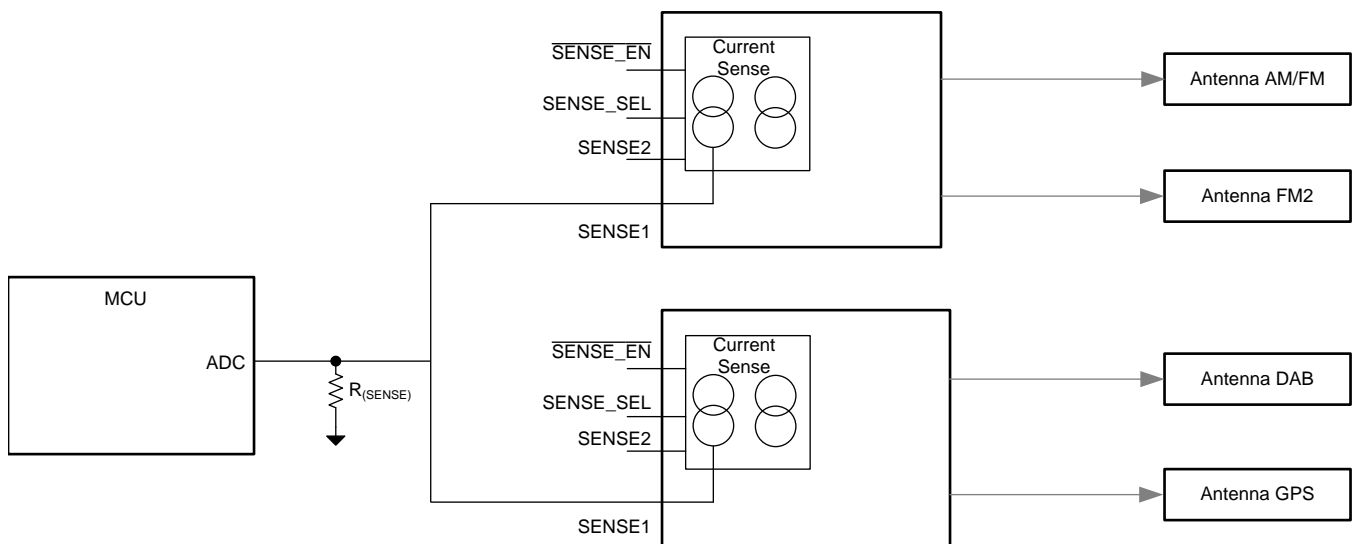


图 20. Current Multiplexing Application Block

7.3.11 Adjustable Output Voltage (FB, FB1, and FB2)

Using an external resistor divider selects an output voltage between 1.5 V and 20 V. Use 表 2 to calculate the output voltage (V_O). The recommended value for both R1 and R2 is less than 100 k Ω .

$$V_O = \frac{V_{(FB)} \times (R1 + R2)}{R2}$$

where

- $V_{(FB)} = 1.233 \text{ V}$

(1)

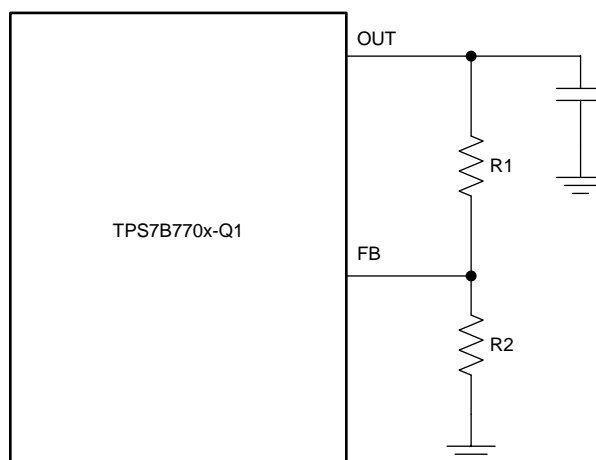


图 21. TPS7B770x-Q1 Output Voltage Setting Connection

The TPS7B770x-Q1 family of devices can also be used as a current-limited switch by connecting the FB pin to the GND pin.

7.4 Device Functional Modes

7.4.1 Operation With $I_N < 4.5 \text{ V}$

The maximum UVLO voltage is 4 V and the device operates at an input voltage above 4.5V. The device can also operate at lower input voltage. No minimum UVLO voltage is specified. At an input voltage below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With EN Control

The threshold of EN rising edge is 2 V (maximum). With the EN pin held above that voltage and the input voltage above 4.5 V, the device becomes active. The EN falling edge is 0.7 V (minimum). Holding the EN pin below that voltage disables the device which therefore reduces the quiescent current of the device.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B770x-Q1 family of devices is a single- or dual-channel 300-mA LDO regulator with high, accurate current sense and a programmable current-limit function. Use the PSPICE transient model to evaluate the base function of the devices. Go to www.ti.com to download the PSPICE model and user's guide for the devices.

8.2 Typical Application

Figure 22 shows the typical application circuit for the TPS7B770x-Q1 family of devices. Different values of external components can be used depending on the end application. An application can require a larger output capacitor during fast load steps to prevent large drops on output voltage. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R.

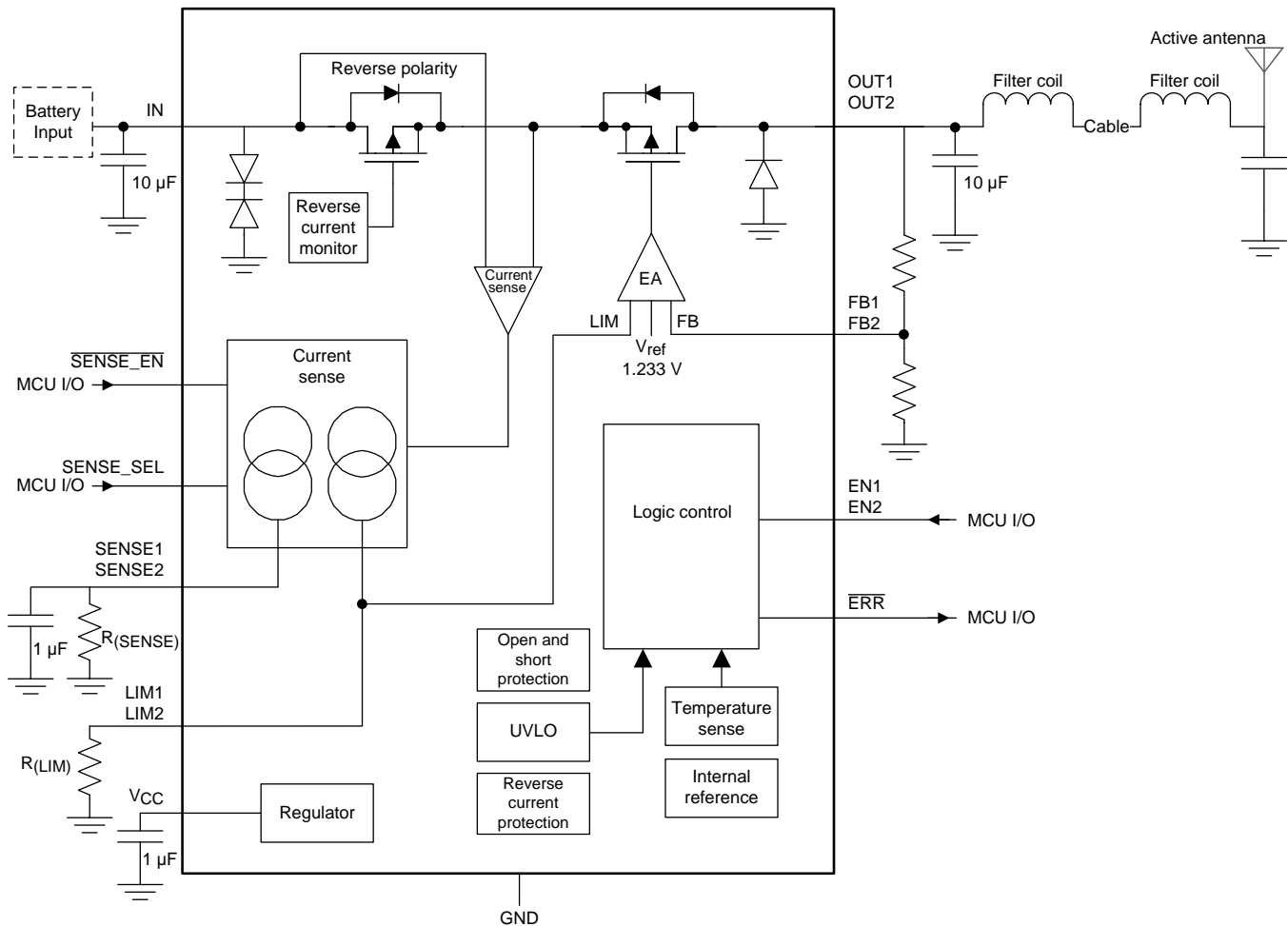


Figure 22. TPS7B770x-Q1 Typical Application

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in [表 3](#) as the design parameters.

表 3. Design Parameters

| DESIGN PARAMETER | EXAMPLE VALUE |
|----------------------------|--|
| Input voltage range | 4.5 to 40 V |
| Output voltage | 1.5 to 20 V |
| Output capacitor range | 2.2 to 100 μ F |
| Output Capacitor ESR range | 0.001 to 5 Ω |
| SENSE resistor | See the Current Sense Resistor Selection section |
| Programmable current limit | 50 to 300 mA |

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage
- Output voltage
- Output current
- Current limit
- ADC voltage rating

8.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommended value for the decoupling capacitor is 10 μ F. The voltage rating must be greater than the maximum input voltage.

8.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The capacitor value should be between 2.2 μ F and 100 μ F. The ESR range should be between 1 m Ω and 5 Ω . TI recommends selecting a ceramic capacitor with low ESR to improve the load transient response.

8.2.2.3 Current Sense Resistor Selection

The current-sense outputs, SENSE_x (SENSE, SENSE1, and SENSE2), are proportional to the output current at the OUT, OUT1, and OUT2 pins with a factor of 1/198. An output resistor, R_(SENSE_x), must be connected between the SENSE_x pin and ground to generate a current sense voltage to be sampled by ADC. Use [式 2](#) to calculate the voltage at SENSE_x pin ($V_{(SENSE_x)}$).

$$V_{(SENSE_x)} = I_{(SENSE_x)} \times R_{(SENSE_x)}$$

where

$$I_{(SENSE_x)} = \frac{I_{(OUT_x)}}{198} \quad (2)$$

For this example, select 1.5 k Ω as a value for R_(SENSE_x). Do not consider the resistor and current-sense accuracy.

For a load current of 198 mA, use [式 3](#) to calculate the value of $V_{(SENSE_x)}$.

$$I_{(SENSE_x)} = \frac{198 \text{ mA}}{198} = 1 \text{ mA} \rightarrow V_{(SENSE_x)} = 1 \text{ mA} \times 1.5 \text{ k}\Omega = 1.5 \text{ V} \quad (3)$$

To avoid any overlap between normal operation and current-limit or short-to-ground phase, using 式 4 to select the value of the SENSE resistor is recommended.

$$R_{(\text{SENSE}x)} \leq \frac{198 \times 2.4 \text{ V}}{I_{\text{Omax}}}$$

where

- 198 is the output current to current-sense ratio
- 2.4 V is the minimum possible voltage at the SENSE_x pin under a short-circuit fault case
- I_{Omax} is the maximum possible output current under normal operation (4)

To stabilize the current-sense loop, connecting a 1-μF ceramic capacitor at the SENSE, SENSE1, or SENSE2 pin is required. 表 4 lists the current sense accuracy across temperature.

表 4. Current Sense Accuracy

| OUTPUT CURRENT | CURRENT SENSE ACCURACY |
|------------------|------------------------|
| 5 mA to 10 mA | 20% |
| 10 mA to 50 mA | 10% |
| 50 mA to 100 mA | 5% |
| 100 mA to 300 mA | 3% |

8.2.2.4 Current-Limit Resistor Selection

The current at the LIM_x pins (LIM, LIM1, and LIM2) is proportional to the load current at the OUT_x (OUT, OUT1, and OUT2) pins and is internally connected to a current-limit comparator referenced to 1.233 V. The current limit is programmable through the external resistor connected at LIM_x pin. Use 式 5 to calculate the value of the external resistor, $R_{(\text{LIM}x)}$. The programmable current limit accuracy is 8% maximum across all conditions. The internal current limit of the device is set by shorting the LIM pin to ground. Because the current limit varies by 8%, 式 6 shows how to calculate the minimum current limit value, and 式 7 shows how to calculate the maximum current limit value.

$$R_{(\text{LIM}x)} = \frac{1.233 \text{ V}}{I_{(\text{LIM}x)}} \times 198$$

where

- $I_{(\text{LIM}x)(\text{typ})} = \frac{1.233 \text{ V}}{R_{(\text{LIM}x)}} \times 198$ (5)

$$I_{(\text{LIM}x)(\text{min})} = I_{(\text{LIM}x)(\text{typ})} \times 0.92 = (0.92) \left(\frac{1.233 \text{ V}}{R_{(\text{LIM}x)}} \times 198 \right) \quad (6)$$

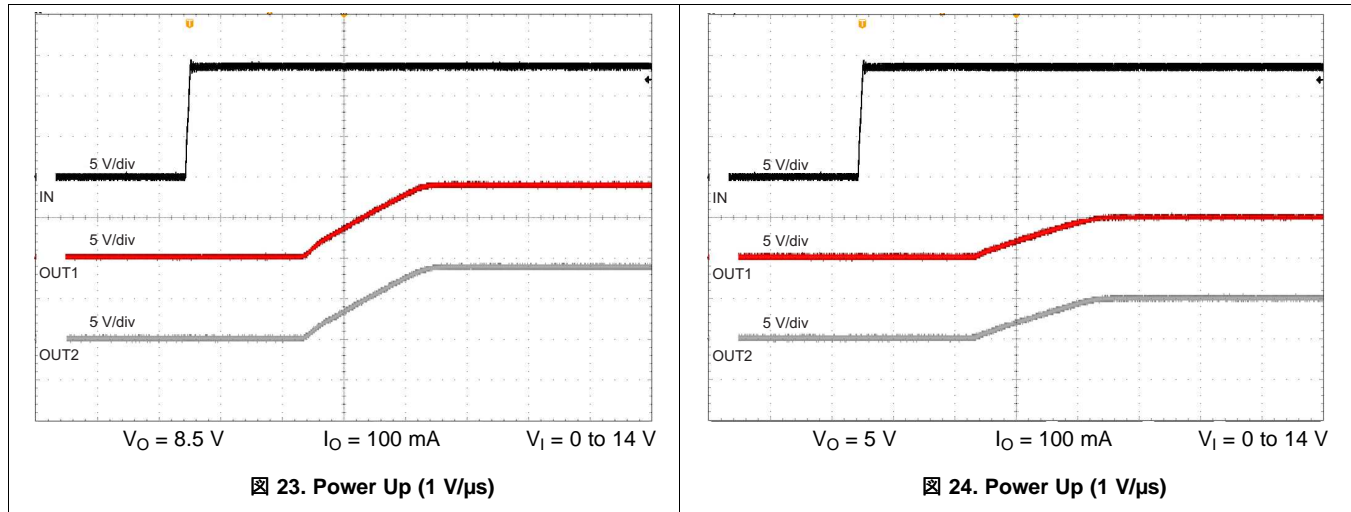
$$I_{(\text{LIM}x)(\text{max})} = I_{(\text{LIM}x)(\text{typ})} \times 1.08 = (1.08) \left(\frac{1.233 \text{ V}}{R_{(\text{LIM}x)}} \times 198 \right) \quad (7)$$

Select a maximum current-limit value of 200 mA and use 式 8 to calculate the value of $R_{(\text{LIM}x)}$.

$$R_{(\text{LIM}x)} = \frac{1.08 \times 198 \times 1.233 \text{ V}}{I_{(\text{LIM}x)(\text{max})}} \quad (8)$$

Using 式 8 yields a $R_{\text{LIM}x}$ value of 1.318 kΩ. The closest 1% resistor that can be selected is 1.33 kΩ. Now using 式 7 and plugging in 1.33 kΩ for $R_{\text{LIM}x}$ yields a maximum current of 198.2 mA. Keep in mind this result does not include resistor tolerance in the calculation. To make sure that the current does not exceed the set amount, resistor tolerance must also be included in the equation.

8.2.3 Application Curves



9 Power Supply Recommendations

The device is designed to operate from an input voltage supply with a range between 4.5 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B770x-Q1 device, TI recommends adding an 10- μF electrolytic capacitor and a ceramic bypass capacitor at the input.

10 Layout

10.1 Layout Guidelines

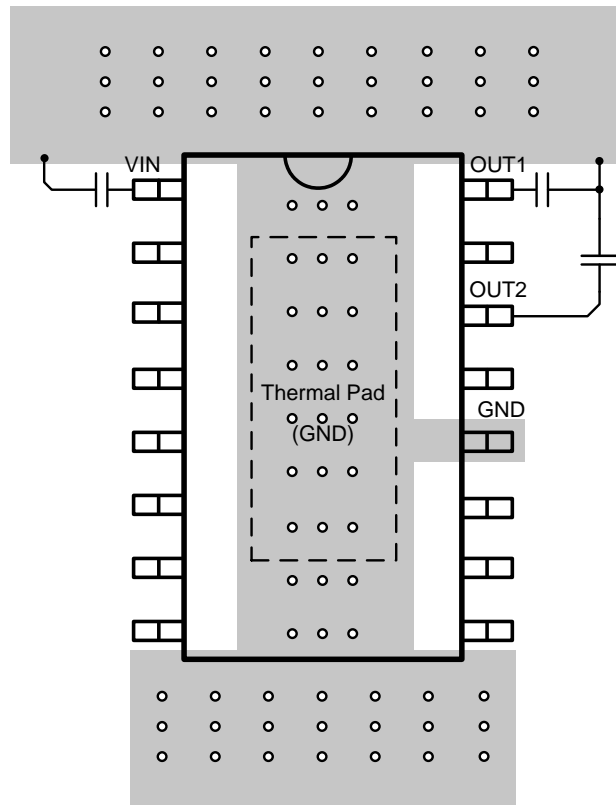
For the layout of TPS7B770x-Q1 device, place the input and output capacitors close to the device as shown in [Figure 25](#). To enhance the thermal performance, TI recommends surrounding the device with some vias.

Minimize equivalent-series inductance (ESL) and ESR to maximize performance and provide stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use long traces because they can negatively impact system performance and cause instability.

If possible, and to maintain the maximum performance specified in this device data sheet, use the same layout pattern used for the TPS7B770x-Q1 evaluation board, available online at www.ti.com/tool/TPS7B7702EVM.

10.2 Layout Example



☒ 25. TPS7B770x-Q1 Layout Example

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

[『TPS7B7702-Q1評価モジュール ユーザー・ガイド』](#)

11.2 関連リンク

表 5 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 5. 関連リンク

| 製品 | プロダクト・フォルダ | サンプルとご購入 | 技術資料 | ツールとソフトウェア | サポートとコミュニティ |
|--------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| TPS7B7701-Q1 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |
| TPS7B7702-Q1 | ここをクリック | ここをクリック | ここをクリック | ここをクリック | ここをクリック |

11.3 ドキュメントの更新通知を受け取る方法

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11.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™オンライン・コミュニティ TIのE2E (*Engineer-to-Engineer*) コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

設計サポート TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

11.5 商標

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All other trademarks are the property of their respective owners.

11.6 静電気放電に関する注意事項



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11.7 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS7B7701QPWPRQ1 | ACTIVE | HTSSOP | PWP | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 7B7701 | Samples |
| TPS7B7702QPWPRQ1 | ACTIVE | HTSSOP | PWP | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 7B7702 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS7B7701QPWPRQ1 | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| TPS7B7702QPWPRQ1 | HTSSOP | PWP | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

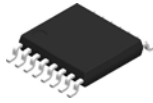

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS7B7701QPWRQ1 | HTSSOP | PWP | 16 | 2000 | 350.0 | 350.0 | 43.0 |
| TPS7B7702QPWRQ1 | HTSSOP | PWP | 16 | 2000 | 350.0 | 350.0 | 43.0 |



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

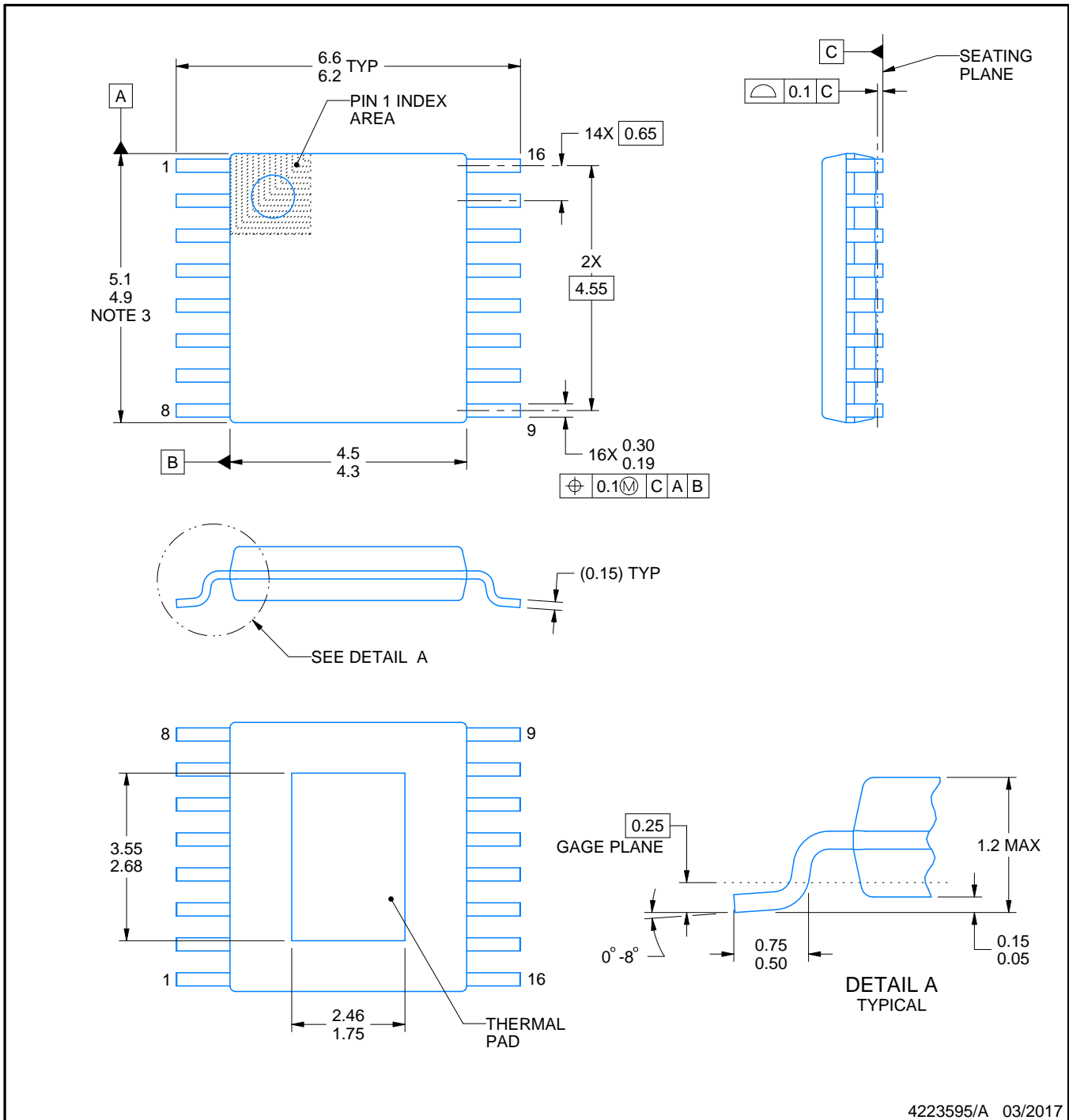
PWP0016J



PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

PowerPAD is a trademark of Texas Instruments.

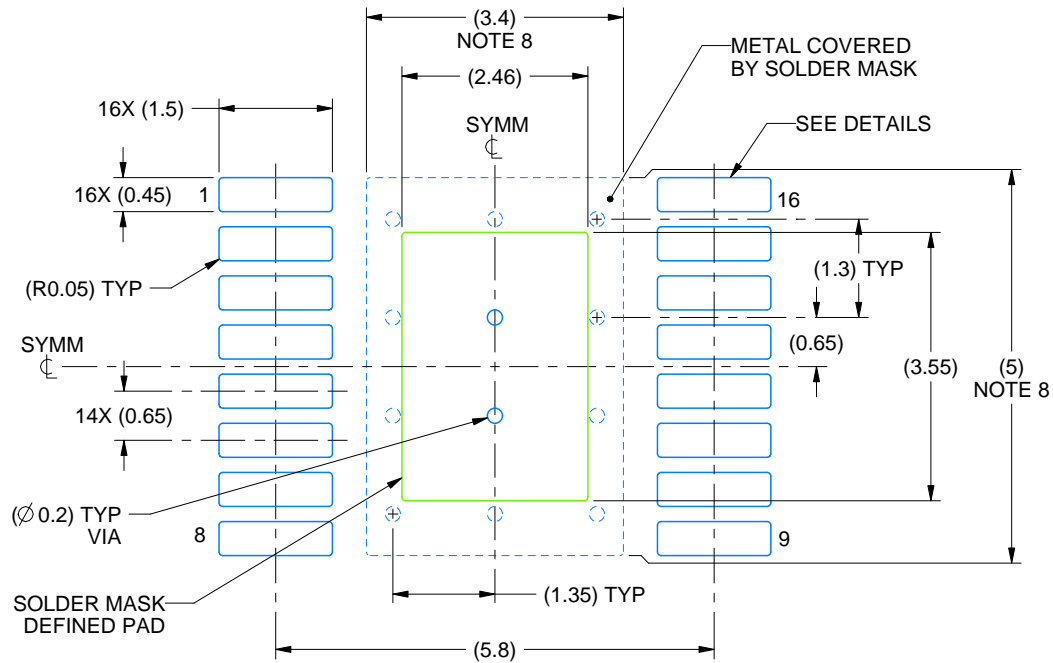
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

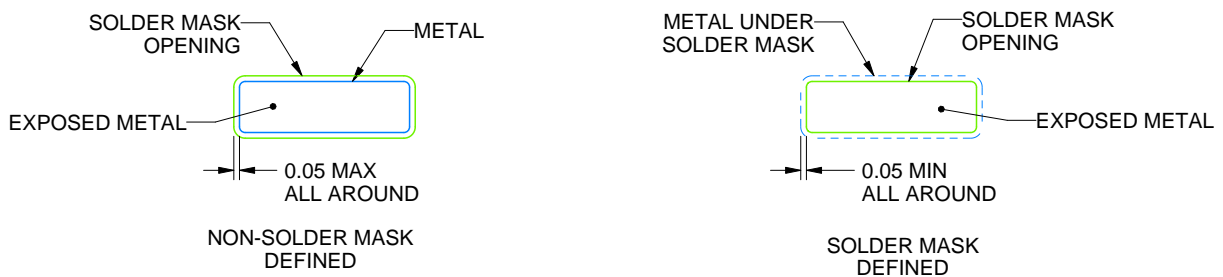
PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

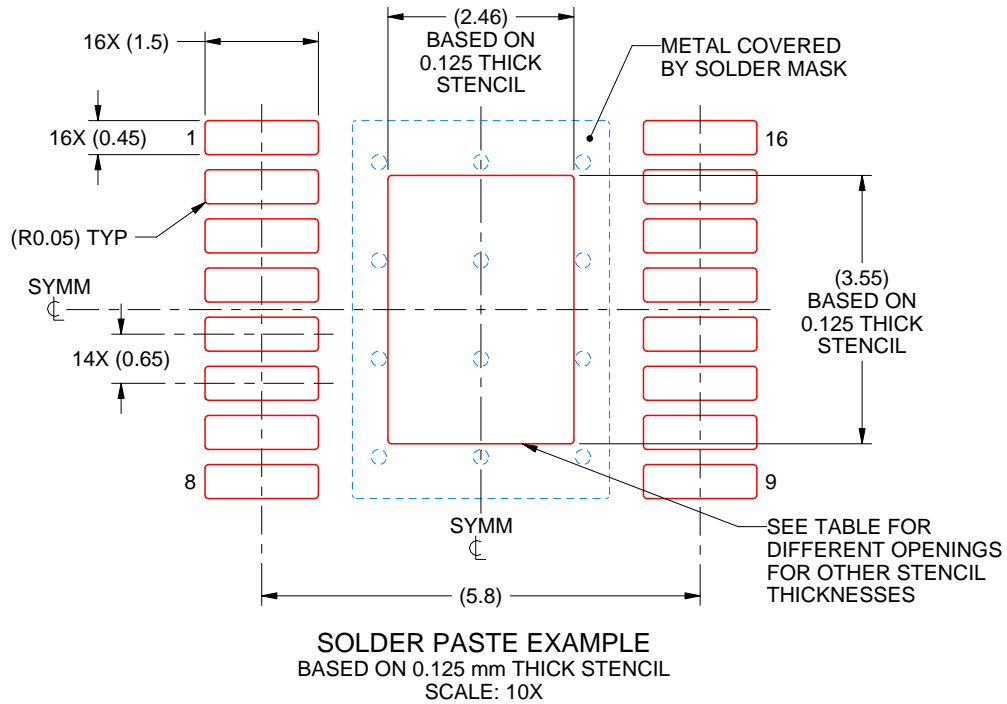
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1 | 2.75 X 3.97 |
| 0.125 | 2.46 X 3.55 (SHOWN) |
| 0.15 | 2.25 X 3.24 |
| 0.175 | 2.08 X 3.00 |

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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