

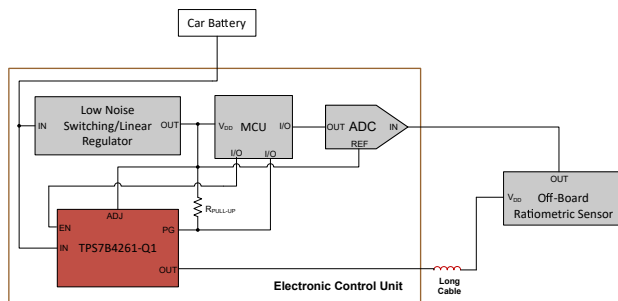
TPS7B4261-Q1 車載、300mA、40V、PG を搭載する電圧トラッキング LDO

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 1: $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$, T_A
 - 接合部温度: $-40^{\circ}\text{C} \sim +150^{\circ}\text{C}$, T_J
- 幅広い入力電圧範囲:
 - 絶対最大入力範囲: $-40\text{V} \sim 45\text{V}$
 - 動作範囲: $3.3\text{V} \sim 40\text{V}$
- 広い出力電圧範囲: $2\text{V} \sim 40\text{V}$
- 最大出力電流: 300mA
- 非常に厳格な出力トラッキング許容誤差: 6mV (最大値)
- Low ドロップアウト電圧: 200mA 時に 330mV
- 個別のイネーブルピンの機能
- パワーグッド機能は、低電圧および過電圧状態を検出することです
- 低い静止電流 (軽負荷時): $55\mu\text{A}$
- 幅広いセラミック出力コンデンサの値全体で安定:
 - C_{OUT} 範囲: $1\mu\text{F} \sim 100\mu\text{F}$
 - ESR 範囲: $1\text{m}\Omega \sim 2\Omega$
- 内蔵保護機能:
 - 逆電流保護
 - 逆極性保護
 - 過熱保護
 - グラウンド / 電源への出力短絡に対する保護
- 熱抵抗の小さい 8 ピンのパッケージで利用可能:
 - HSOIC (DDA), $R_{\theta\text{JA}} = 48^{\circ}\text{C/W}$

2 アプリケーション

- パワートレインの圧力センサ
- パワートレインの温度センサ
- パワートレインの排気ガスセンサ
- パワートレインの液体濃度センサ
- 車体制御モジュール (BCM)
- ゾーン制御モジュール (ZCM)
- HVAC 制御モジュール



代表的なアプリケーション

3 概要

TPS7B4261-Q1 は、モノリシックの統合型低ドロップアウト電圧トラッカーです。このデバイスは、8 ピン HSOIC パッケージで供給されます。TPS7B4261-Q1 は、車載環境でオフボードセンサに電源を供給するように設計されています。デバイスは 300mA 電流定格が高いため、単一の TPS7B4261-Q1 で複数のオフボードセンサに同時に電源を供給できる可能性があります。オフボード電力を供給するケーブル上で障害が発生するリスクが高いため、このデバイスには、逆電流 (バッテリーへの短絡)、逆極性、出力からグラウンドへの短絡 (電流制限)、過熱 (サーマルシャットダウン) などのフォルト条件に対する保護機能が内蔵されています。このデバイスは、金属酸化膜半導体電界効果トランジスタ (PMOS) トポロジを逆並列に採用しています。このトポロジにより、逆電流の原因となるフォルト条件から保護するための外部ダイオードが不要になります。このデバイスは、 45V (絶対最大定格) までの入力電圧に対応し、車載向けの負荷ダンプ過渡条件に耐えられるように設計されています。

可変入力ピン (ADJ) に印加される基準電圧は、OUT ピンのライン、負荷、そして温度にわたって 6mV (最大値) の非常に厳しい公差でトラッキングされます。この厳しいトラッキングにより、TPS7B4261-Q1 は、最大 300mA の負荷に対して高精度で電源電圧を供給できます。TPS7B4261-Q1 には、低電圧および過電圧フォルト状態を検出する独立したイネーブルピン (EN) およびパワーグッド機能があります。

EN 入力ピンを Low に設定することで、TPS7B4261-Q1 はスタンバイモードに切り替わり、低ドロップアウトレギュレータ (LDO) の静止電流消費を $3.8\mu\text{A}$ 未満 (最大値) までに低減できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)
TPS7B4261-Q1	DDA (HSOIC, 8)	6mm × 4.9mm

- 詳細については、[メカニカル](#)、[パッケージ](#)、および[注文情報](#)を参照してください。
- パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



TPS7B4261-Q1 は、ADC の基準電圧に対する効果的なバッファとして機能し、この電圧 (またはそのスケールされた電圧) を長いケーブルで安全に送信して、オフボード センサに電力を供給します。センサがレシオメトリックで、出力が ADC によってサンプリングされる場合、TPS7B4261-Q1 の説明した機能により、センサ測定の信頼性と精度の大幅な向上が可能になります。

ADVANCE INFORMATION

Table of Contents

1 特長	1	7.1 Application Information.....	15
2 アプリケーション	1	7.2 Typical Application.....	16
3 概要	1	7.3 Power Supply Recommendations.....	17
4 Pin Configuration and Functions	4	7.4 Layout.....	18
5 Specifications	5	8 Device and Documentation Support	21
5.1 Absolute Maximum Ratings.....	5	8.1 Device Support.....	21
5.2 ESD Ratings.....	5	8.2 Documentation Support.....	21
5.3 Recommended Operating Conditions.....	5	8.3 ドキュメントの更新通知を受け取る方法.....	21
5.4 Thermal Information	6	8.4 サポート・リソース.....	21
5.5 Electrical Characteristics.....	6	8.5 Trademarks.....	21
5.6 Typical Characteristics.....	8	8.6 静電気放電に関する注意事項.....	21
6 Detailed Description	9	8.7 用語集.....	21
6.1 Overview.....	9	9 Revision History	21
6.2 Functional Block Diagram.....	9	10 Mechanical, Packaging, and Orderable Information	22
6.3 Feature Description.....	9	10.1 Mechanical Data.....	23
6.4 Device Functional Modes.....	14		
7 Application and Implementation	15		

4 Pin Configuration and Functions

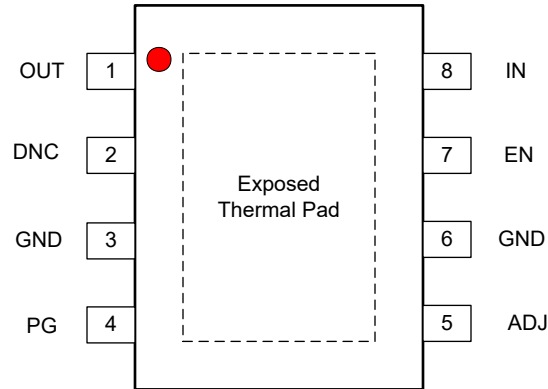


図 4-1. DDA Package, 8-Pin HSOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DDA		
ADJ	5	I	Adjustable input pin. Connect the external reference voltage to this pin, either directly or with a voltage divider for lower output voltages. This pin connects to the inverting input of the error amplifier internally. To compensate for line influences, place a 0.1μF capacitor close to this pin.
DNC	2	—	Do not connect a voltage source to this pin. Leave this pin floating or connect to GND to improve thermal performance.
EN	7	I	Enable pin. A low signal below V_{IL} disables the device, and a high signal above V_{IH} enables the device. Do not leave this pin floating.
GND	3, 6	G	GND pin. Connect this pin to a low impedance path to ground.
IN	8	I	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND. See the Recommended Operating Conditions table. Place the input capacitor as close to the input pin of the device as possible to compensate for line influences. See the Input and Output Capacitor Selection section for more details.
OUT	1	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, select a ceramic capacitor within the range of C_{OUT} values provided in the Recommended Operating Conditions table. Place this capacitor as close to output of the device as possible. See the Input and Output Capacitor Selection section for more details.
PG	4	O	Active-high, open-drain based power-good pin. Connect this pin to a positive voltage via a pullup resistor. After device start-up, the pin assumes a logic low level only if the tracker output voltage fall below or exceeds the nominal V_{OUT} value by the under- or overvoltage threshold, respectively. This feature helps identify possible fault conditions on the tracker output. See the Power Good section for more details.
Thermal Pad	—		Thermal pad. Connect the pad to GND for best possible thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{IN}	Unregulated input pin voltage	-40	45	V
V _{OUT}	Regulated output pin voltage	-5	45	V
V _{EN}	Enable pin voltage	-40	45	V
V _{PG}	Power-good pin voltage	-0.3	45	V
V _{ADJ}	Adjustable reference input pin voltage	-40	45	V
T _J	Operating junction temperature	-40	150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may effect the device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾		±2500
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000
			Corner pins	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V _{IN}	Input voltage	3.3		40	V
V _{OUT}	Output voltage	2		40	V
I _{OUT}	Output current	0		300	mA
V _{EN}	Enable pin voltage	0		40	V
V _{ADJ}	Adjustable reference pin voltage	2		40	V
V _{PG}	Power-good pin voltage	0		40	V
C _{IN}	Input capacitor ⁽¹⁾		1		µF
C _{OUT}	Output capacitor ⁽²⁾	1		100	µF
ESR	Output capacitor ESR requirements	0.001		2	Ω
T _J	Operating junction temperature	-40		150	°C

- (1) For robust EMI performance the minimum input capacitance recommended is 500nF.
 (2) Effective output capacitance of 500nF minimum is required for stability.

5.4 Thermal Information

THERMAL METRIC ^{(1) (2)}		TPS7B4261-Q1	
		DDA (HSOIC)	UNIT
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	48	°C/W
R _{θJCTop}	Junction-to-case (top) thermal resistance	71.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	23.5	°C/W
ψ _{JT}	Junction-to-top characterization parameter	9.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	23.3	°C/W
R _{θJCbott}	Junction-to-case (bottom) thermal resistance	11.5	°C/W

- (1) The thermal data is based on the JEDEC standard high-K board layout, JESD 51-7. This is a two-signal, two-plane, four-layer board with 2-oz. copper on the external layers. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.
- (2) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

specified at T_J = -40°C to +150°C, V_{IN} = 13.5V, I_{OUT} = 100µA, C_{OUT} = 1µF, C_{IN} = 1µF, V_{EN} = 2V and V_{ADJ} = 5V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
I _Q	Quiescent current	V _{IN} = 5.4V to 40V, I _{OUT} = 100µA, T _J = 25°C			75	µA
		V _{IN} = 5.4V to 40V, I _{OUT} = 100µA, -40°C < T _J < 85°C			80	
		V _{IN} = 5.4V to 40V, I _{OUT} = 100µA			85	
I _{GND}	Ground current	V _{IN} = 5.4V to 40V, I _{OUT} = 300mA			3.2	mA
I _{SHUTDOWN}	Shutdown supply current	V _{ADJ/EN} = 0V			3.8	µA
I _{ADJ}	ADJ pin current	I _{OUT} = 100µA			0.9	µA
V _{UVLO (RISING)}	Rising input supply UVLO	V _{IN} rising, I _{OUT} = 5mA	2.6	2.7	2.85	V
V _{UVLO (FALLING)}	Falling input supply UVLO	V _{IN} falling, I _{OUT} = 5mA	2.3	2.4	2.5	V
V _{UVLO (HYST)}	V _{UVLO(IN)} hysteresis			300		mV
ΔV _{OUT}	Output voltage tracking accuracy	V _{IN} = V _{OUT} + 1.2V to 40V, I _{OUT} = 100µA to 300mA ⁽¹⁾	-6		6	mV
ΔV _{OUT (ΔVIN)}	Line regulation	V _{IN} = V _{OUT} + 1.2V to 40V, I _{OUT} = 100µA	-0.4		0.4	mV
ΔV _{OUT (ΔIOUT)}	Load regulation	V _{IN} = V _{OUT} + 1.2V, I _{OUT} = 100µA to 300mA ⁽¹⁾			2.1	mV
V _{DO}	Dropout voltage	I _{OUT} = 200mA, V _{ADJ} ≥ 3.3V, V _{IN} = V _{ADJ}		330	700	mV
I _{CL}	Output current limit	V _{IN} = V _{OUT} + 1.2V, V _{OUT} short to 90% x V _{ADJ}	301	430	560	mA
V _{PG UV-TH}	Power-good undervoltage threshold, V _{ADJ} - V _{OUT}	V _{OUT} decreasing, V _{IN} = V _{ADJ} = 0.5V, V _{IN} reducing	40	80	120	mV
V _{PG OV-TH}	Power-good overvoltage threshold, V _{OUT} - V _{ADJ}	V _{OUT} increasing, V _{IN} ≥ V _{ADJ/REF} + 0.5V	40	80	120	mV
V _{PG-HYST}	Power-good hysteresis			25		mV
t _{PG}	Power-good reaction time		20	50	80	µS
V _{PG, LOW}	Power-good output low voltage	I _{PG} = 1.8mA			0.4	V
I _{PG, LEAKAGE}	Power-good pin leakage current	V _{PG} = 5V			2	µA
V _{EN, OFF}	Device disable voltage range				0.8	V
V _{EN, ON}	Device enable voltage range		1.8			V
I _{EN}	Enable pin leakage current	V _{EN} = 5V			1	µA
PSRR	Power-supply ripple rejection	V _{RIPPLE} = 1V _{PP} , frequency = 100Hz, I _{OUT} ≥ 5mA		80		dB
V _n	Output noise voltage	V _{OUT} = 3.3V, I _{OUT} = 1mA, BW = 10Hz to 100KHz, a 5µV _{RMS} reference is used for this measurement		150		µV _{RMS}
I _{REV}	Reverse current at V _{IN}	V _{IN} = 0V, V _{OUT} = 32V	-0.6		0.6	µA
I _{REV-N1}	Reverse current at negative V _{IN}	V _{IN} = -20V, V _{OUT} = 20V	-1.2		1.2	µA

5.5 Electrical Characteristics (続き)

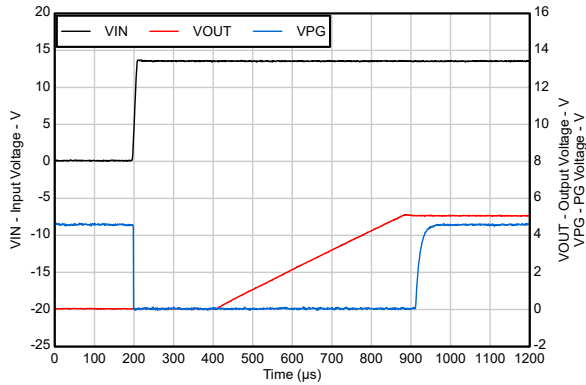
specified at $T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$, $V_{IN} = 13.5\text{V}$, $I_{OUT} = 100\mu\text{A}$, $C_{OUT} = 1\mu\text{F}$, $C_{IN} = 1\mu\text{F}$, $V_{EN} = 2\text{V}$ and $V_{ADJ} = 5\text{V}$ (unless otherwise noted); typical values are at $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		$^{\circ}\text{C}$
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			15		$^{\circ}\text{C}$

- (1) Because the power dissipation is potentially large, this specification is measured using pulse testing with a low duty cycle. See the thermal information table for more information on how much power the device dissipates while maintaining a junction temperature below 150°C .

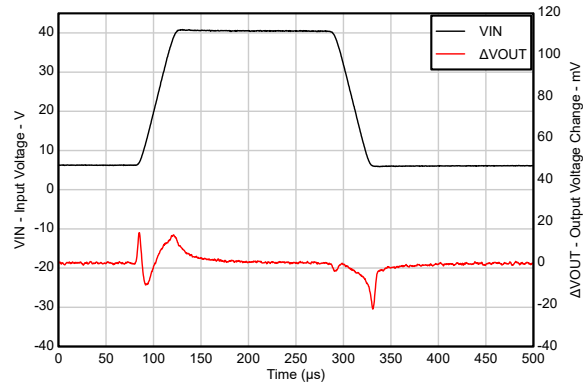
5.6 Typical Characteristics

ADVANCE INFORMATION



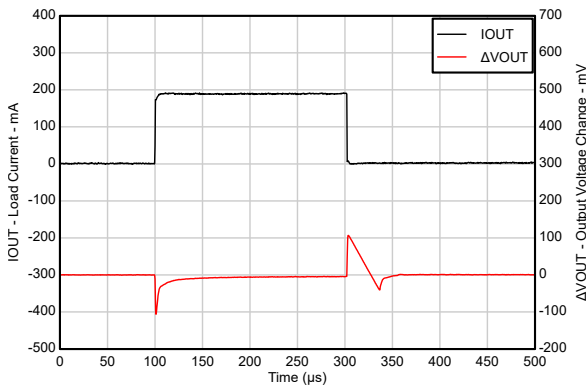
$V_{IN} = 0V$ to $13.5V$ at a rate of $1V/\mu s$, $V_{ADJ} = 5V$, $V_{EN} = 2V$,
 $C_{OUT} = 1\mu F$, $I_{OUT} = 200mA$

Figure 5-1. Start-Up Profile



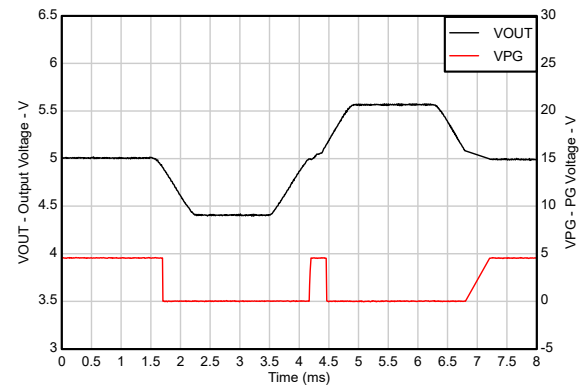
$V_{IN} = 6V$ to $40V$ at a rate of $1V/\mu s$, $V_{ADJ} = 5V$, $V_{EN} = 2V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 200mA$

Figure 5-2. Line Transient



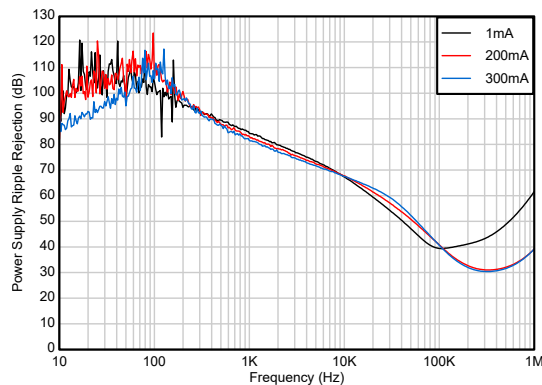
$V_{IN} = 13.5V$, $V_{ADJ} = 5V$, $V_{EN} = 2V$, $C_{OUT} = 1\mu F$, $I_{OUT} = 1mA$ to
 $200mA$ at $1A/\mu s$

Figure 5-3. Load Transient



$V_{ADJ} = 5V$, $V_{EN} = 2V$, $C_{OUT} = 1\mu F$, V_{OUT} ramped down to $4.4V$
 from nominal value of $5V$ and then ramped up to $5.6V$

Figure 5-4. Power-Good Functionality



$V_{IN} = 13.5V$, $V_{ADJ} = 5V$, $V_{EN} = 2V$, $C_{OUT} = 1\mu F$

Figure 5-5. PSRR vs Frequency

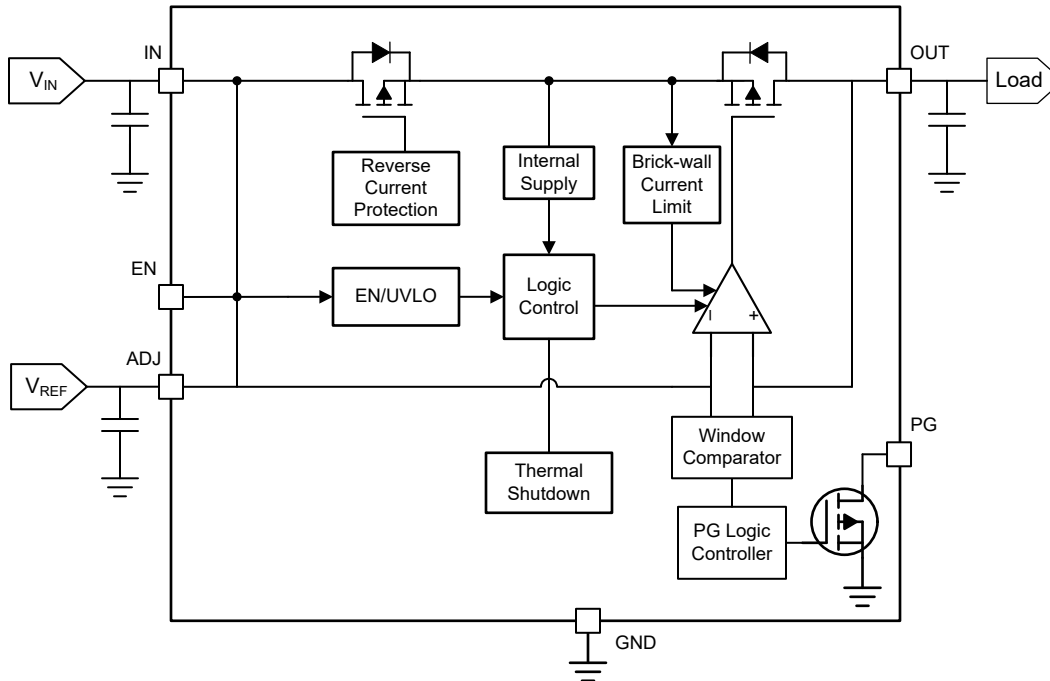
6 Detailed Description

6.1 Overview

The TPS7B4261-Q1 is an integrated, low-dropout (LDO) voltage tracker with ultra-low tracking tolerance. Because of the high risk of cable shorts when powering off-board sensors, multiple features are built into the LDO. These features protect against fault conditions resulting in short to battery, short to GND, and reverse current flow.

In addition, this device also features thermal shutdown protection, brick-wall current limiting, undervoltage lockout (UVLO), reverse polarity protection, and under- and overvoltage detection.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Tracker Output Voltage (V_{OUT})

Because this device is a tracking LDO, the output voltage is equal to the voltage provided to the ADJ pin, so long as sufficient voltage is provided to the ADJ pin ($\geq 2V$) and EN pin ($\geq 1.8V$). The LDO remains enabled as long as both V_{EN} and V_{ADJ} exceed $V_{EN, ON}$ and is disabled when either of V_{EN} or V_{ADJ} become less than $V_{EN, OFF}$. The values of $V_{EN, ON}$ and $V_{EN, OFF}$ can be found in the [Electrical Characteristics](#) table. The device has a soft-start feature incorporated, which allows the output voltage to rise linearly and limits the in-rush current at start-up. After start-up and upon attaining steady state, the output voltage V_{OUT} remains within $\pm 6mV$ from the voltage set on the ADJ pin V_{ADJ} over all specified operating conditions.

6.3.1.1 Output Voltage Equal to Reference Voltage

Figure 6-1 shows the external reference voltage applied directly to the ADJ pin. Under these conditions, the LDO output voltage is equal to the reference voltage, as given in Equation 1.

$$V_{OUT} = V_{REF} \tag{1}$$

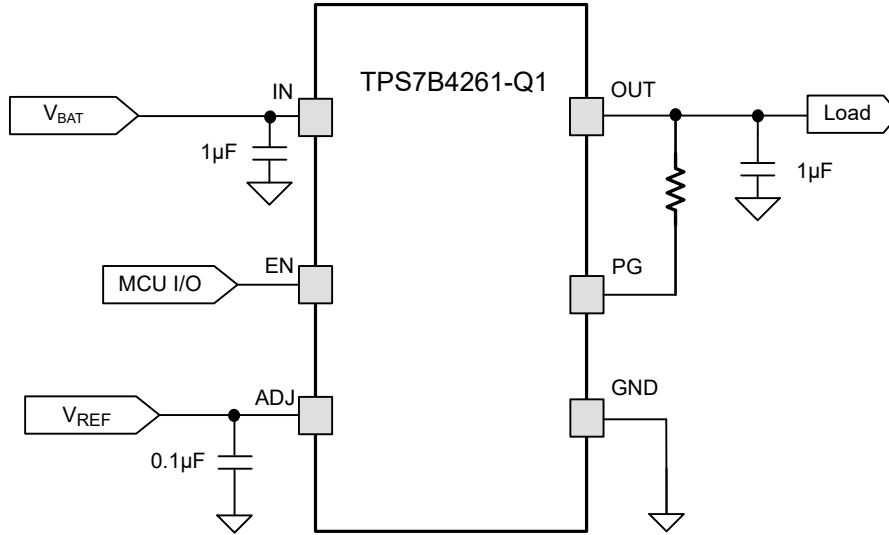


Figure 6-1. Tracker Output Voltage Equal to Reference Voltage

6.3.1.2 Output Voltage Less Than the Reference Voltage

Connecting an external resistor divider at the ADJ pin, as shown in Figure 6-2, helps generate an output voltage that is lower than the reference voltage. Both R_1 and R_2 must be less than 100kΩ to minimize the error in voltage caused by the ADJ pin leakage current, I_{ADJ} . Equation 2 calculates V_{OUT} .

$$V_{OUT} = \frac{(V_{REF} \times R_2)}{R_1 + R_2} \tag{2}$$

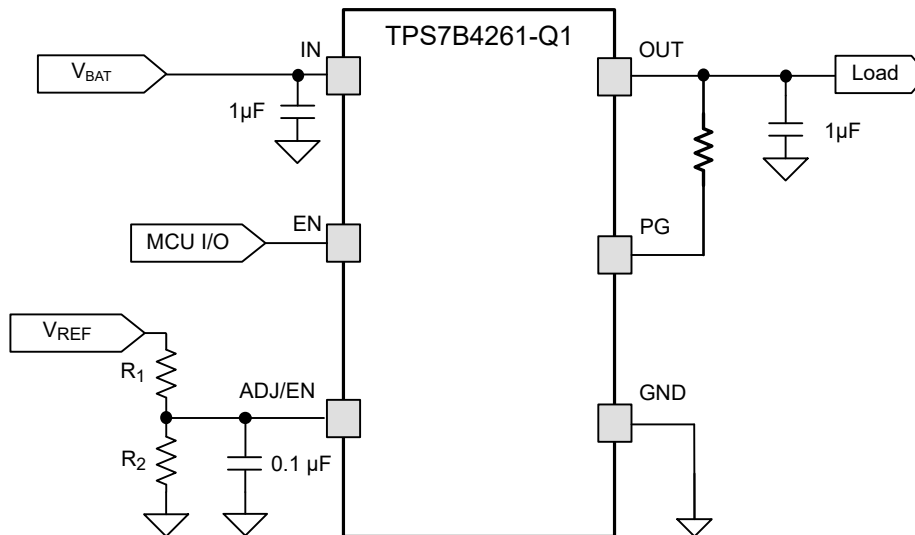


Figure 6-2. Tracker Output Voltage Less Than the Reference Voltage

6.3.2 Reverse Current Protection

The TPS7B4261-Q1 incorporates a back-to-back PMOS topology that protects the device from damage against a fault condition, resulting in V_{OUT} being higher than V_{IN} and the subsequent flow of reverse current. No damage occurs to the device if this fault condition occurs, provided the [Absolute Maximum Ratings](#) are not violated. This integrated protection feature eliminates the need for an external diode. The reverse current comparator typically responds to a reverse voltage condition in 10 μ s, and along with the body diode of the blocking PMOS transistor, limits the reverse current to I_{REV} , as specified in the [Electrical Characteristics](#) table.

6.3.3 Power Good

The TPS7B4261-Q1 has an open-drain based power-good pin, that can help detect undervoltage and overvoltage fault conditions at the tracker output. This pin can be pulled up to a regulated rail via a pullup resistor, and the maximum value of this $V_{PULL-UP}$ rail can be inferred from the V_{PG} range of values listed in the [Recommended Operating Conditions](#). The input voltage V_{IN} must be higher than $V_{UVLO(RISING)}$, for V_{PG} to have a valid value.

So long as the device is enabled ($V_{EN} > V_{EN, ON}$) and sufficient V_{IN} & V_{ADJ} are provided ($V_{IN} \geq V_{IN MIN}$, $V_{ADJ} \geq V_{ADJ MIN}$), the PG pin assumes a high-impedance state when the tracker output voltage remains within the $V_{PG UV-TH}$ and $V_{PG OV-TH}$ values of V_{ADJ} and is pulled up to $V_{PULL-UP}$.

Variations in tracker output voltage beyond the power-good switching thresholds, that also last longer than t_{PG} , takes the PG pin low, to a voltage $V_{PG} < V_{PG, LOW}$. Transients in V_{OUT} that last less than t_{PG} are not flagged as errors by the PG pin. The PG pin remains low when the device is disabled ($V_{EN} < V_{EN, OFF}$), even if sufficient V_{IN} and V_{ADJ} are provided. The values of $V_{PG UV-TH}$, $V_{PG OV-TH}$, t_{PG} , and $V_{PG, LOW}$ are specified in the [Electrical Characteristics](#) table.

6.3.4 Undervoltage Lockout

The device has an internally fixed undervoltage lockout (UVLO) threshold. Undervoltage lockout activates when the input voltage V_{IN} drops below the undervoltage lockout level (see the $V_{UVLO(FALLING)}$ parameter in the [Electrical Characteristics](#) table). This activation makes sure the regulator is not latched into an unknown state during a low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up in the standard power-up sequence when the input voltage recovers to the required level (see the $V_{UVLO(RISING)}$ parameter in the [Electrical Characteristics](#) table).

6.3.5 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C, which allows the device to cool. When the junction temperature cools to approximately 160°C, the output circuitry enables. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle off and on until the condition that causes excessive power dissipation is removed. This cycling limits the dissipation of the regulator, thus protecting the regulator from damage as a result of overheating.

The internal protection circuitry of the TPS7B4261-Q1 is designed to protect against overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7B4261-Q1 into thermal shutdown degrades device reliability.

6.3.6 Current Limit

The device has an internal current limit circuit that protects the device during overcurrent or shorting conditions. The current-limit circuit, as shown in [Figure 6-3](#), is a brick-wall scheme. When the device is in current limit, the device sources I_{CL} and the output voltage is not regulated. In this scenario, the output voltage depends on the load impedance.

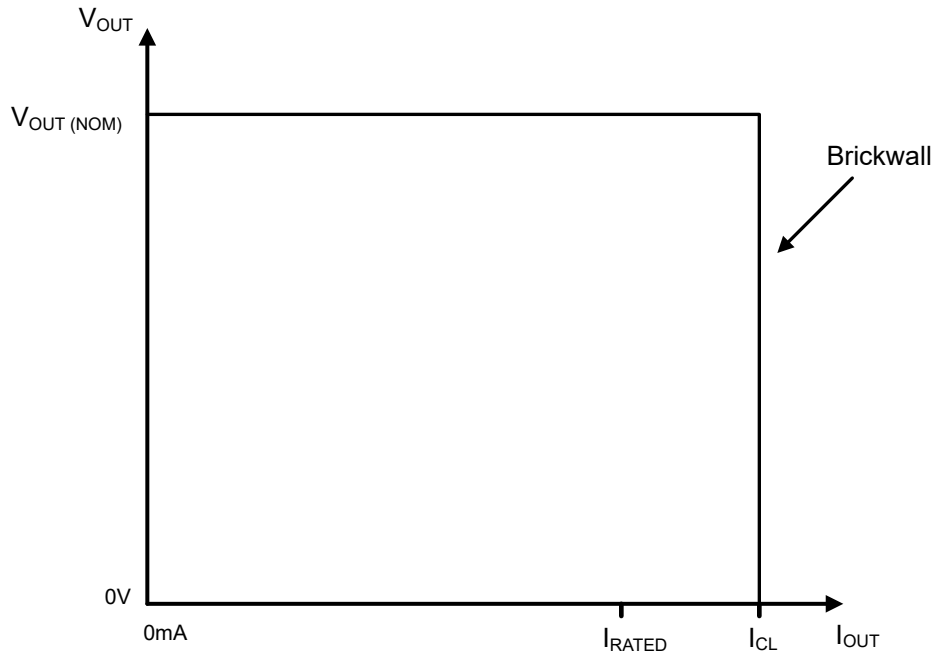


Figure 6-3. Brickwall Current Limit Scheme

During current-limit events, the potential for high power dissipation exists because of the elevated current level and the increased input-to-output differential voltage ($V_{IN} - V_{OUT}$). If the heat dissipation is substantial, the device enters thermal shutdown. If the current-limit condition is not removed when the device turns back on after cooling, the device enters thermal shutdown again. This cycle continues until the current-limit condition is removed. The device survives this fault, but repeatedly operating in this mode degrades long-term reliability.

6.3.7 Output Short to Battery

When the output is shorted to the battery (see [Figure 6-4](#)), the TPS7B4261-Q1 survives and no damage occurs to the device. A short to the battery also occurs when the device is powered by an isolated supply (see [Figure 6-5](#)) at a lower voltage. In this example, the TPS7B4261-Q1 supply input voltage is set at 7V when a short to battery (14V typical) occurs on V_{OUT} , which typically runs at 5V. The back-to-back PMOS topology helps limit the continuous reverse current flowing through V_{IN} to I_{REV} , as provided in the [Electrical Characteristics](#) table.

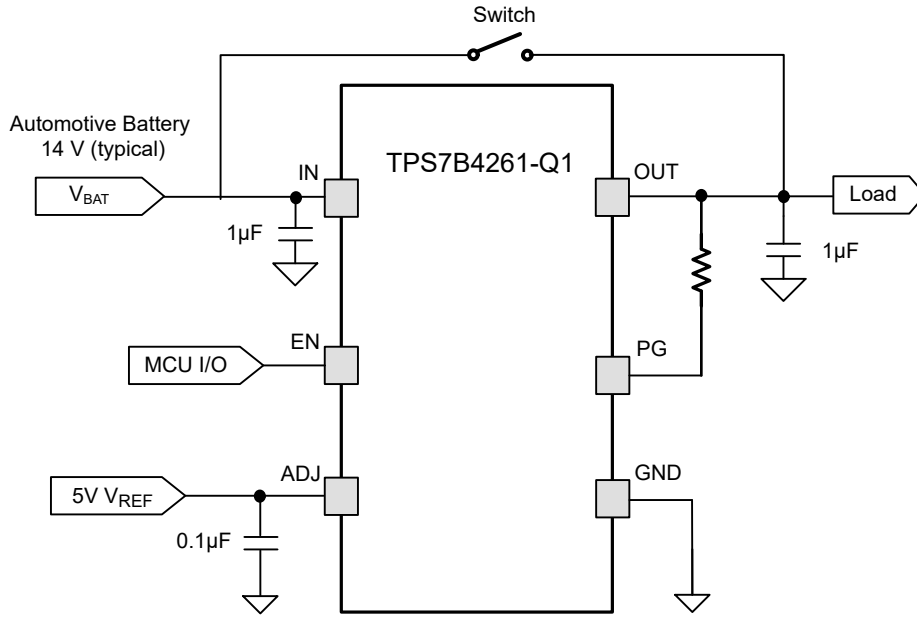


図 6-4. Tracker Output Short to Battery

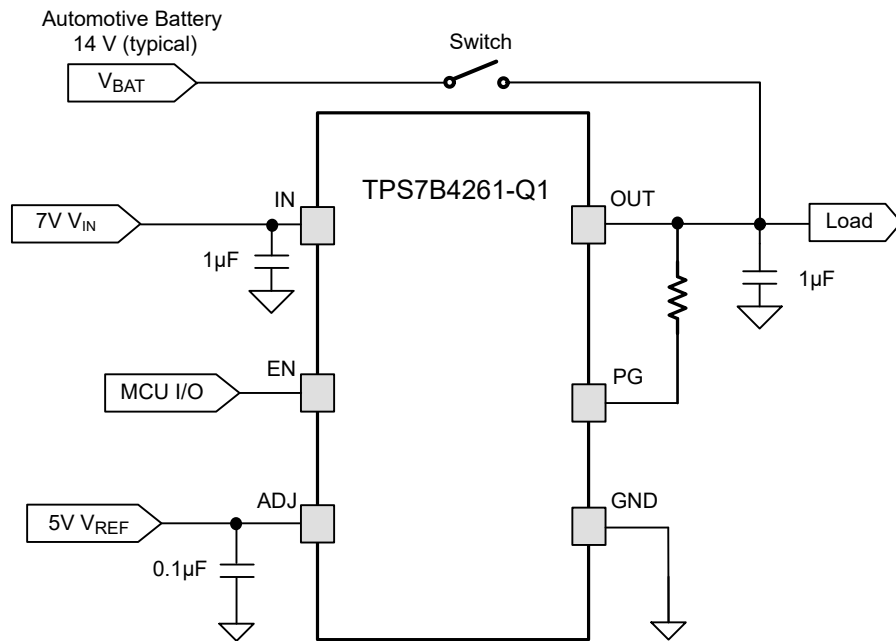


図 6-5. Tracker Output Voltage Higher Than Input Voltage

6.4 Device Functional Modes

表 6-1 shows the conditions that lead to the different modes of operation. See the [Electrical Characteristics](#) table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER ⁽¹⁾				
	V _{IN}	V _{ADJ}	V _{EN}	I _{OUT}	T _J
Normal operation	$V_{IN} > V_{OUT(Nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{ADJ} > V_{EN, ON}$	$V_{EN} > V_{EN, ON}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J \leq 150^\circ\text{C}$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ADJ} > V_{EN, ON}$	$V_{EN} > V_{EN, ON}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ADJ} < V_{EN, OFF}$	$V_{EN} < V_{EN, OFF}$	Not applicable	$T_J > T_{SD(shutdown)}$

(1) The device turns on when V_{IN} is greater than V_{UVLO(RISING)} and both V_{ADJ} and V_{EN} are greater than the enable rising threshold V_{EN, ON}.

6.4.1 Normal Operation

The device output voltage V_{OUT(Nom)} tracks the reference voltage at the ADJ pin when the following conditions are met:

- The input voltage is at least 3.3V (V_{IN(min)}) and greater than the nominal output voltage plus the dropout voltage (V_{OUT(nom)} + V_{DO}).
- The reference voltage at the ADJ pin and the enable pin voltage V_{EN} are both greater than the enable rising threshold V_{EN, ON}. The voltage on the ADJ pin stays stable at the appropriate V_{REF} value.
- The output current is less than I_{OUT(max)} (I_{OUT} ≤ 300mA).
- The device junction temperature is less than the thermal shutdown temperature (T_J < T_{SD}).

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, V_{IN} < V_{OUT(NOM)} + V_{DO}, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage (V_{OUT(NOM)} + V_{DO}), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the saturation region.

6.4.3 Operation With V_{IN} < 3.3V

For input voltages below 3.3V and above V_{UVLO(FALLING)}, the LDO continues to operate but certain circuits potentially do not have proper headroom to operate within specification. When the input voltage drops below V_{UVLO(FALLING)} the device shuts off.

6.4.4 Disable With ADJ and EN Controls

Both the ADJ and EN pins are independently able to disable the device. Shutdown the output of the device by forcing either V_{ADJ} or V_{EN} to less than V_{EN, OFF}. When disabled, the pass transistor is turned off, the internal circuits are shutdown, and the LDO is in a low-power mode.

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as the input voltage minus the output voltage ($V_{IN} - V_{OUT}$) when the pass transistor is fully on. This condition arises when the input voltage falls to the point where the error amplifier drives the gate of the pass transistor to the rail. During this condition, there is no remaining headroom for the control loop to operate. The pass transistor is in the ohmic or triode region of operation, and acts as a switch. Dropout voltage directly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage follows, minus the dropout voltage (V_{DO}).

In dropout mode, the output voltage is no longer regulated, and transient performance is severely degraded. The device loses PSRR, and load transients potentially cause large output voltage deviation.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated output current (I_{RATED} , see the [Recommended Operating Conditions](#) table), the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (3)$$

7.1.2 Reverse Current

The TPS7B4261-Q1 incorporates reverse current protection that prevents damage from a fault condition, resulting in V_{OUT} being higher than V_{IN} . During such a fault condition, where the V_{IN} and V_{OUT} absolute maximum ratings are not violated and $V_{OUT} - V_{IN}$ is less than 40V, no damage occurs and less than 1.2 μ A (max) of reverse current flows through the LDO. The reverse current comparator typically responds to a reverse voltage condition and, along with the body diode of the blocking PMOS transistor, limits the reverse current in 10 μ s.

7.2 Typical Application

Figure 7-1 shows a typical application circuit for the TPS7B4261-Q1.

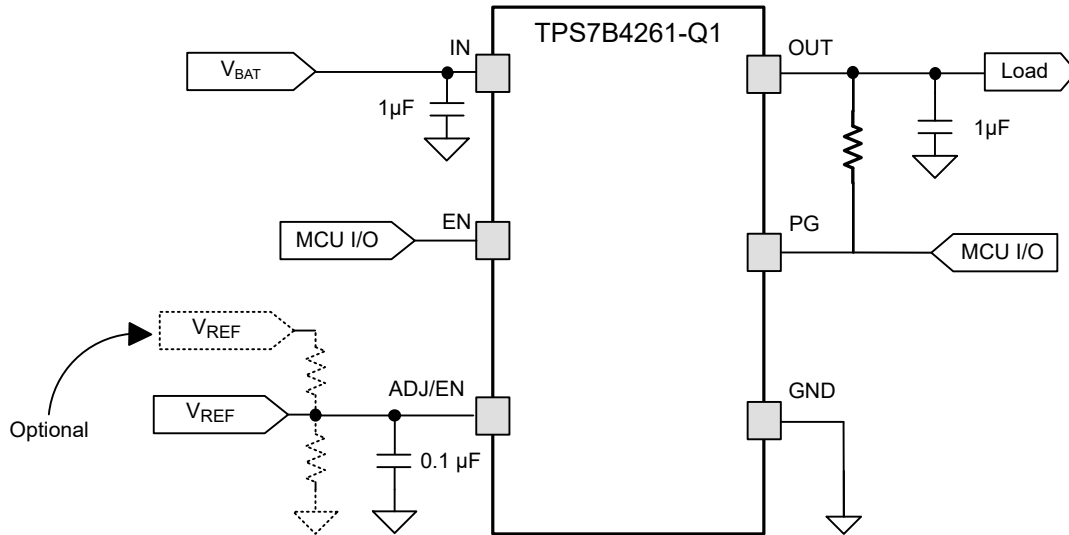


Figure 7-1. Typical Application Schematic

7.2.1 Design Requirements

Use the parameters listed in Table 7-1 for this design example.

Table 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage	3.3V to 40V
Adjustable reference voltage	2V to 40V
Enable Voltage	1.8V to 40V
Output voltage	2V to 40V
Output current rating	300mA
Output capacitor range	1µF to 100µF
Output capacitor ESR range	1mΩ to 2Ω

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Selection

Depending on the end-application, different values of external components can be used. Some applications require a larger output capacitor during fast load steps to prevent a reset from occurring. Use a low equivalent series resistance (ESR) ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

The TPS7B4261-Q1 requires an output capacitor of at least 1 μ F (500nF or larger capacitance) for stability and an ESR between 0.001 Ω and 2 Ω . Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For most applications, a low ESR, 10 μ F ceramic capacitor on the OUT pin is sufficient to provide excellent transient performance.

Use a minimum 100nF input capacitor for the TPS7B4261-Q1. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce the input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.2.3 Application Curves

The following images illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness for the HSOIC-8 (DDA) package. These plots are generated with a 101.6mm \times 101.6mm \times 1.6mm printed circuit board (PCB) of two and four layers. For the 2-layer board, the bottom layer is a ground plane of constant size, and the top layer copper is connected to GND and varied. For the 4-layer board, the second layer is a ground plane of constant size and the third layer is a power plane of constant size. The top and bottom layers copper fills are connected to GND and varied at the same rate. For the 4-layer board, inner planes use 1oz copper thickness. Outer layers are simulated with both 1oz and 2oz copper thickness. A 3 \times 3 array of thermal vias with a 300 μ m drill diameter and 25 μ m copper plating is located underneath the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. [PowerPAD™ Thermally Enhanced Package application note](#) discusses the impact that thermal vias have on thermal performance.

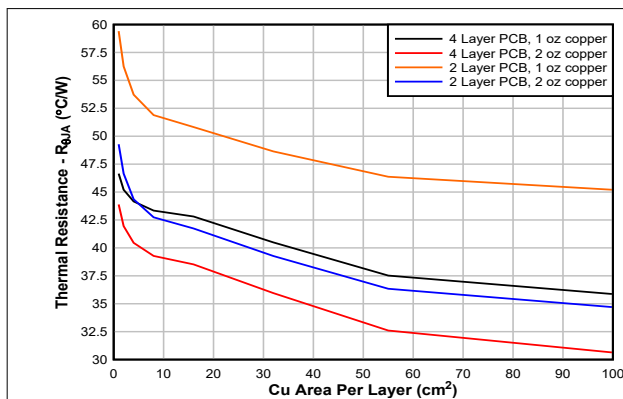


Figure 7-2. $R_{\theta JA}$ vs Copper Area (HSOIC-8 Package)

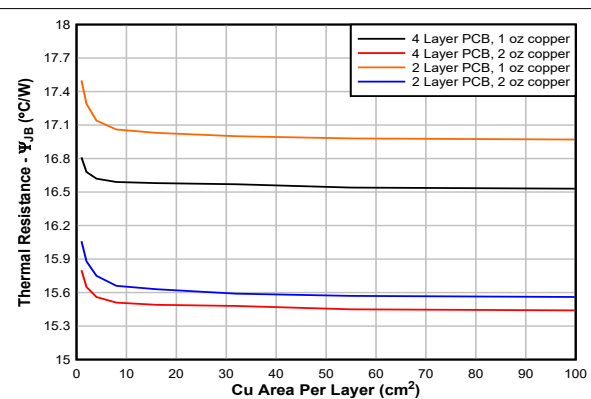


Figure 7-3. ψ_{JB} vs Copper Area (HSOIC-8 Package)

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3.3V to 40V.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board. Place these components as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other. Use a wide, component-side, copper surface to make these connections. Using vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. Use a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage and shields noise. This reference plane also behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4261-Q1 are available at the end of this document and at www.ti.com.

7.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT} . Connect each ground plane only at the GND pin of the device. In addition, directly connect the ground connection for the output capacitor to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR to maximize performance and provide stability. Place each capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any capacitors on the opposite side of the PCB from where the regulator is installed. Using vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces potentially cause instability.

If possible, and to provide the maximum performance denoted in this document, use the same layout pattern used for the TPS7B4261-Q1 evaluation board. This evaluation board is available at www.ti.com.

7.4.1.3 Power Dissipation and Thermal Considerations

式 4 calculates the device power dissipation.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \quad (4)$$

where:

- P_D = Continuous power dissipation
- I_{OUT} = Output current
- V_{IN} = Input voltage
- V_{OUT} = Output voltage
- I_Q = Quiescent current

Because I_Q is much less than I_{OUT} , the term $I_Q \times V_{IN}$ in 式 4 can be ignored.

Calculate the junction temperature (T_J) with 式 5 for a device under operation at a given ambient air temperature (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (5)$$

where:

- $R_{\theta JA}$ = Junction-to-junction-ambient air thermal impedance

式 6 calculates a rise in junction temperature because of power dissipation.

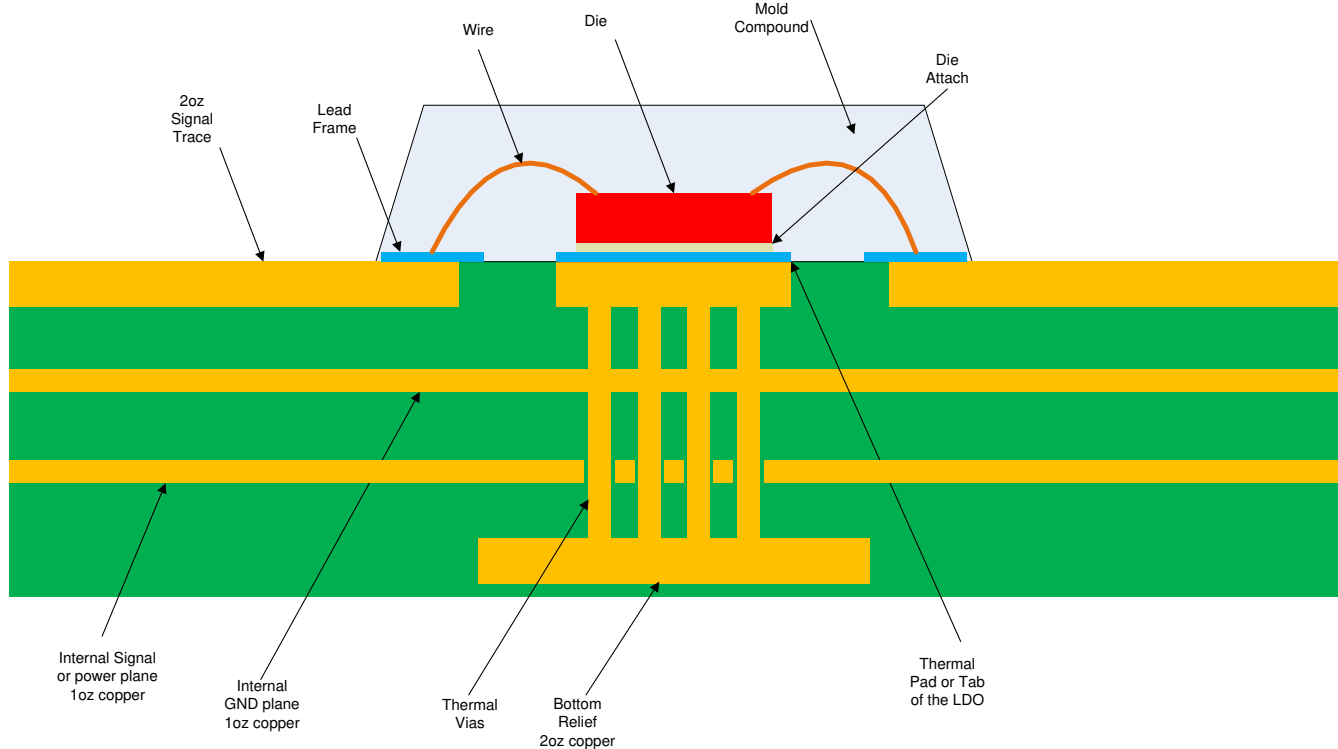
$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (6)$$

The maximum ambient air temperature (T_{AMAX}) at which the device operates is calculated with 式 7 for a given maximum junction temperature (T_{JMAX}).

$$T_{AMAX} = T_{JMAX} - (R_{\theta JA} \times P_D) \quad (7)$$

7.4.1.4 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design. $R_{\theta JA}$ therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard (☒ 7-4), PCB, and copper-spreading area. This parameter is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of $R_{\theta JCbot}$ plus the thermal resistance contribution by the PCB copper. $R_{\theta JCbot}$ is the package junction-to-case (bottom) thermal resistance, as given in the *Thermal Information* table.



☒ 7-4. JEDEC Standard 2s2p PCB

ADVANCE INFORMATION

7.4.2 Layout Example

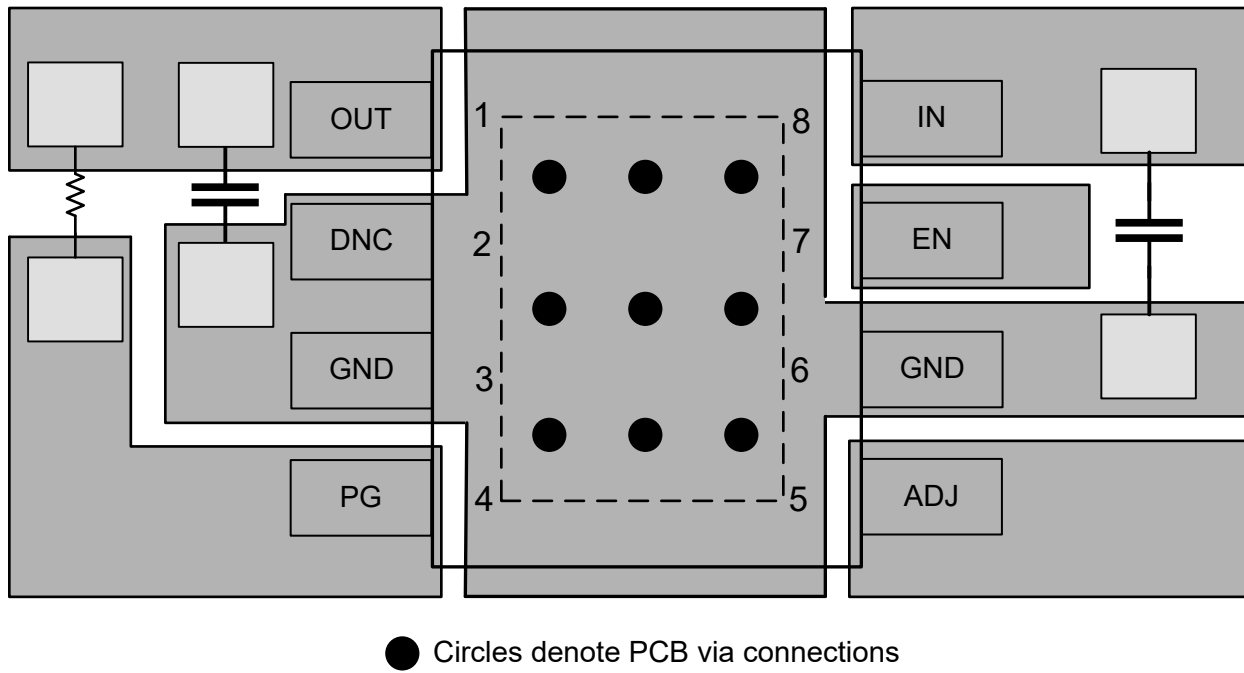


図 7-5. Layout Example

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT ⁽¹⁾	V _{OUT}
TPS7B4261QDDARQ1	In the HSOIC (DDA) package: Q indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. R is the packaging quantity. Q1 indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [PowerPAD™ Thermally Enhanced Package application note](#)

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

テキサス・インスツルメンツ [E2E™ サポート・フォーラム](#) は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの [使用条件](#) を参照してください。

8.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History


資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

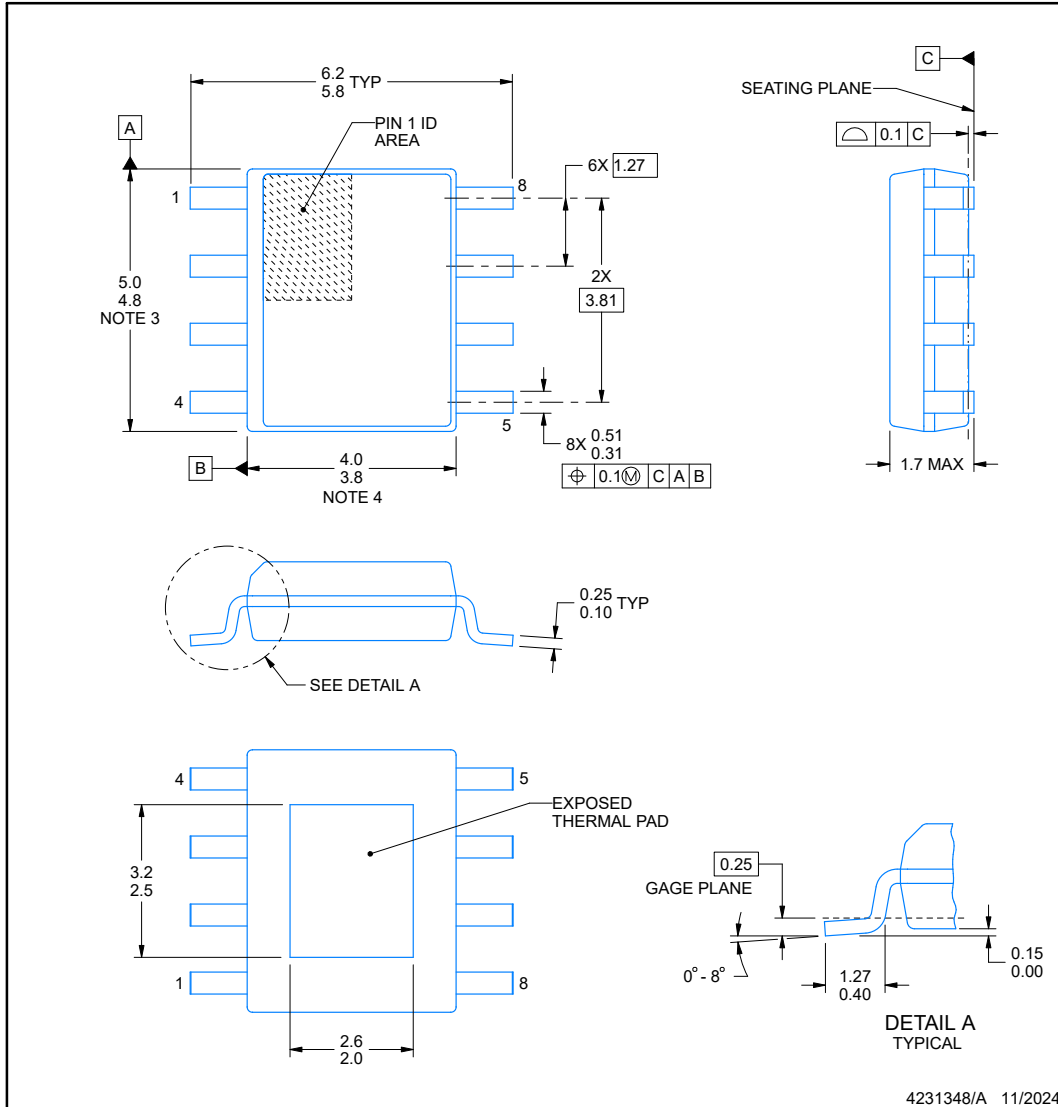
DATE	REVISION	NOTES
January 2025	*	Initial Release

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Mechanical Data

DDA0008J-C02

PACKAGE OUTLINE
PowerPAD™ SOIC - 1.7 mm max height
 PLASTIC SMALL OUTLINE



4231348/A 11/2024

PowerPAD is a trademark of Texas Instruments.

NOTES:

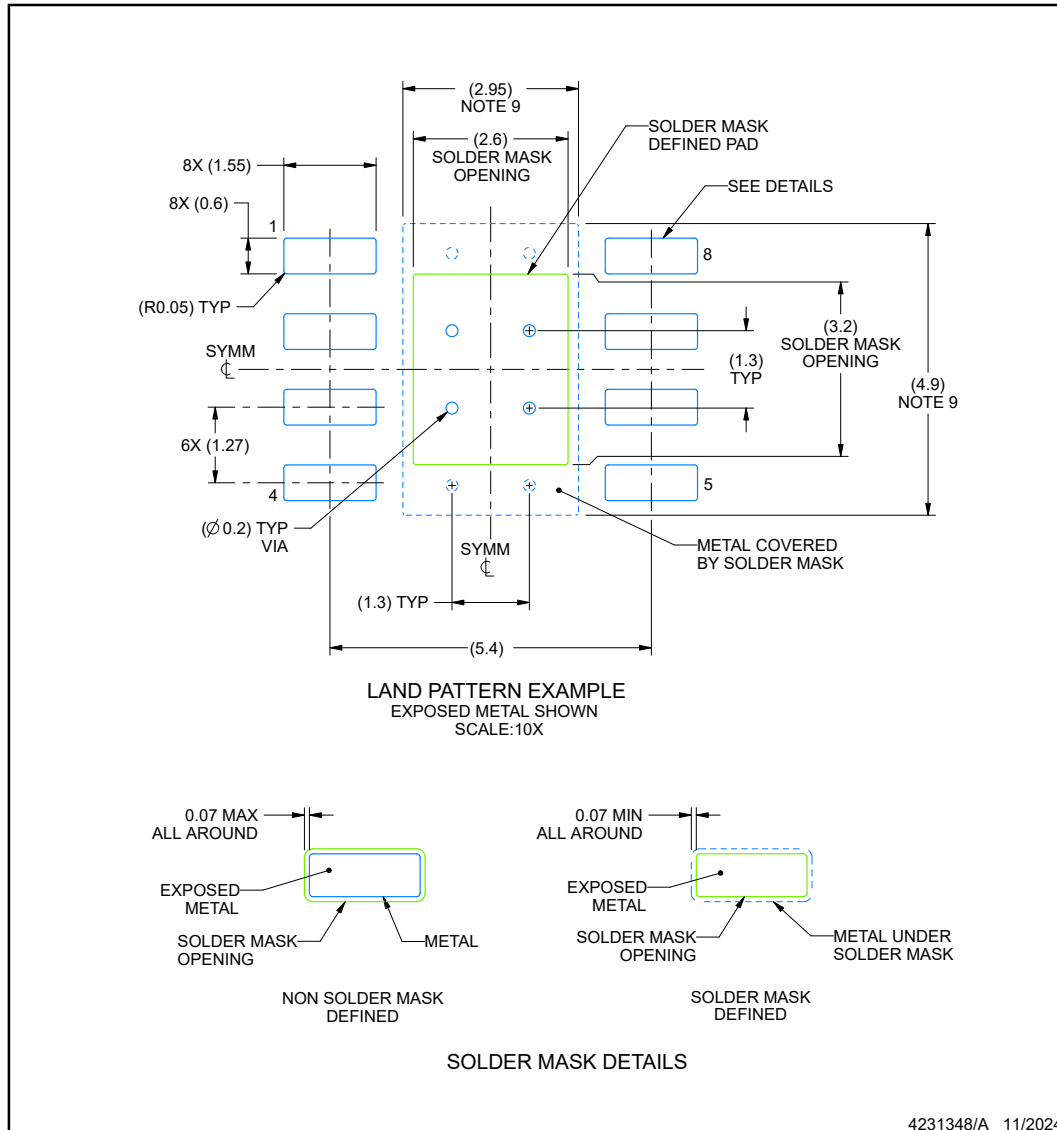
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

EXAMPLE BOARD LAYOUT

DDA0008J-C02

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

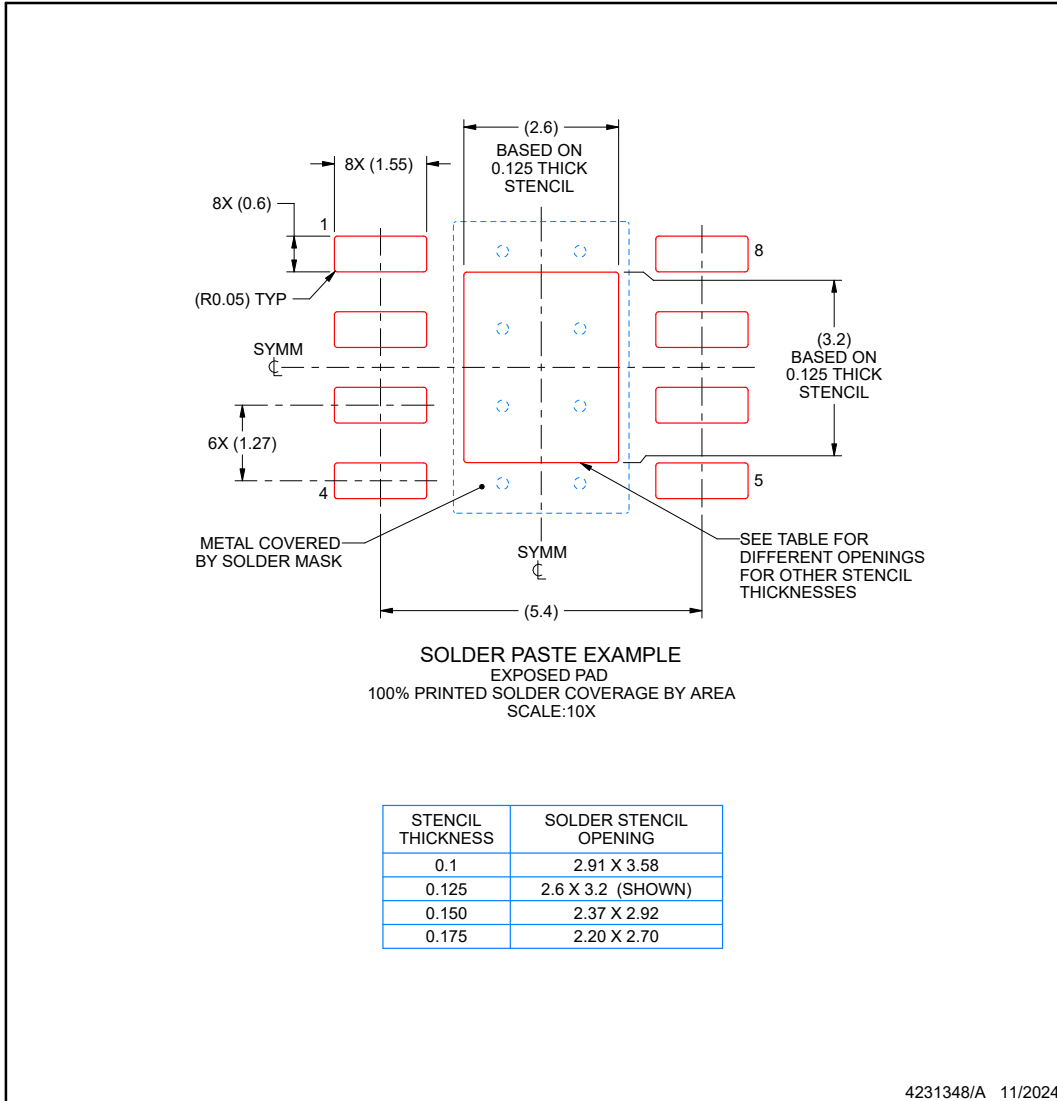
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DDA0008J-C02

PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS7B4261QDDARQ1	ACTIVE	SO PowerPAD	DDA	8	2500	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

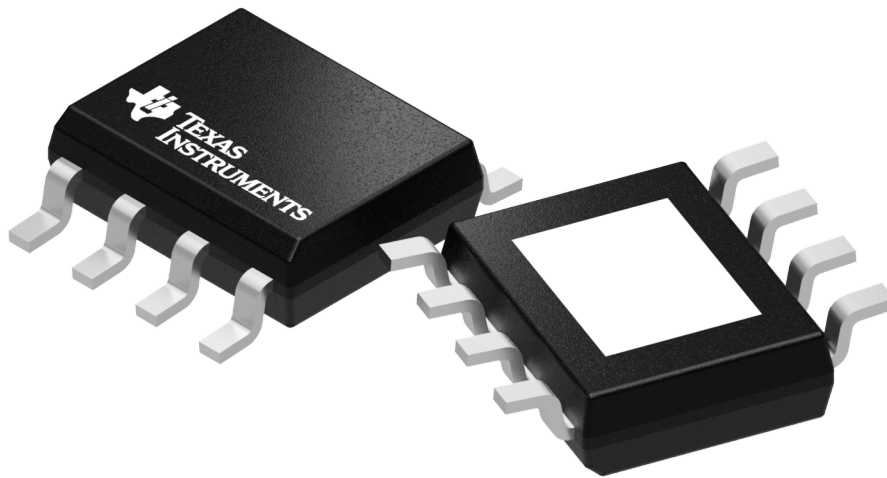
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ(データシートを含みます)、設計リソース(リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適したテキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されているテキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、[テキサス・インスツルメンツの販売条件](#)、または [ti.com](https://www.ti.com) やかかるテキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2025, Texas Instruments Incorporated