TPS7B4260-Q1 トラッキング許容誤差 6mV、車載用、300mA、40V、電圧トラッキング LDO

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
  - 接合部温度:–40℃～+150℃、T_J
- 幅広い入力電圧範囲:
  - 絶対最大入力範囲:-40V～+45V
  - 動作範囲:3.3V～40V
- 出力電圧:
  - 広い動作範囲:2V～40V
  - 出力電圧の柔軟性:分圧器構成で外付け抵抗を使用して、V_{OUT} を基準電圧より高い値または低い値にスケーリング可能
- 最大出力電流:300mA
- 非常に厳格な出力トラッキング許容誤差:6mV (最大値)
- Low ドロップアウト電圧:200 mA 時に 330 mV
- イネーブル機能と基準電圧機能の組み合わせ
- 低い静止電流 (軽負荷時):55µA
- 幅広いセラミック出力コンデンサの値全体で安定:
  - C_{OUT} 範囲:1µF～100µF
  - ESR 範囲:1mΩ～2Ω
- 内蔵保護機能:
  - 逆電流保護
  - 逆極性保護
  - 過熱保護
  - グランド / 電源への出力短絡に対する保護
- HSOIC (DDA) の低熱抵抗 ($R_{\theta JA}$ = 48°C /W) 8 ピンパッケージで利用可能

2 アプリケーション

- パワートレインの圧力センサ
- パワートレインの温度センサ
- パワートレインの排気ガス センサ
- パワートレインの液体濃度センサ
- 車体制御モジュール (BCM)
- ゾーン制御モジュール
- HVAC 制御モジュール

3 概要

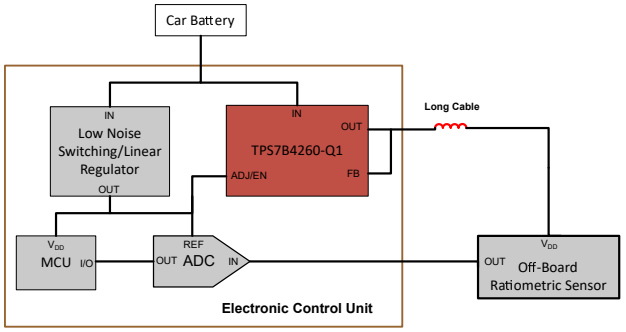
TPS7B4260-Q1 は、モノリシックの統合型低ドロップアウト (LDO) 電圧トラッカーです。このデバイスは、8 ピン HSOIC パッケージで供給されます。TPS7B4260-Q1 は、車載環境でオフボード センサに電源を供給するよう設計されています。デバイスの電流定格が 300mA と高いため、単一のデバイスで複数のオフボード センサに同時に電源を供給できる可能性があります。オフボード電力を供給するケーブルで故障が発生するリスクが高いため、このデバイスには、バッテリへの短絡、逆極性、出力からグランドへの短絡、過熱などの故障状態に対する保護機能が内蔵されています。このデバイスは、2 つの双方向 P チャネル金属酸化膜半導体電界効果トランジスタ (MOSFET) を実装するトポロジを採用しています。この PMOS トポロジにより、逆電流の原因となる故障状態から保護するために必要な外付けダイオードが不要になります。このデバイスは、45V (絶対最大定格) までの入力電圧に対応し、車載向けの負荷ダンプ過渡条件に耐えられるように設計されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS7B4260-Q1	DDA (HSOIC、8)	6mm × 4.9mm

(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。

(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション

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可変入力ピン (ADJ/EN) に印加される基準電圧は、FB ピンのライン、負荷、および温度範囲全体にわたって 6mV (最大値) の非常に厳しい公差でトラッキングされます。この厳しいトラッキングにより、TPS7B4260-Q1 は、最大 300mA の負荷に対して高精度で電源電圧を供給できます。リファレンス電圧は、ADJ/EN ピンに直接接続するか、ADJ/EN ピンの外付け抵抗デバイダを使用して最低 2V まで降圧できます。出力電圧は、FB ピンを OUT ピンに直接接続することで、ADJ/EN ピンの電圧 (± トラッキング許容誤差) と等しくするか、FB と OUT ピンとの間に抵抗分圧器を使用してより高い値に昇圧できます。

TPS7B4260-Q1 は、ADC の基準電圧に対する効果的なバッファとして機能し、この電圧 (またはそのスケーリングされた電圧) を長いケーブルで安全に送信して、オフボード センサに電力を供給します。センサがレシオメトリックで、出力が ADC によってサンプリングされる場合、TPS7B4260-Q1 の説明した機能により、センサ測定の信頼性と精度の大幅な向上が可能になります。

ADJ/EN 入力ピンを Low に設定することで、TPS7B4260-Q1 はスタンバイ モードに切り替わり、LDO の静止電流消費を 3.8µA 未満に低減できます。

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4 Pin Configuration and Functions

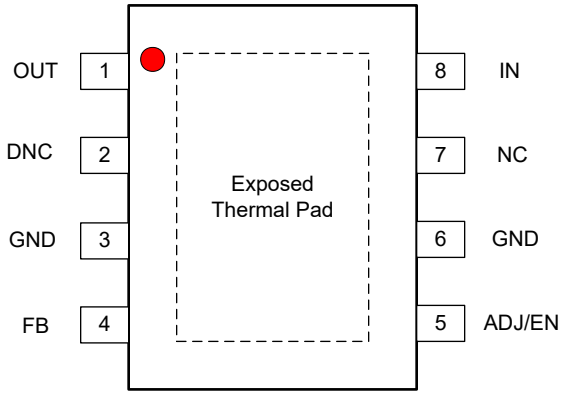

図 4-1. DDA Package, 8-Pin HSOIC (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DDA		
ADJ/EN	5	I	Adjustable/enable input pin. Connect the external reference voltage to this pin. This pin connects to the inverting input of the error amplifier internally. A low signal below V_{IL} disables the device, and a high signal above V_{IH} enables the device. Connect the voltage reference directly, or with a voltage divider to attain output voltages lower than the reference. To compensate for line influences, place a 0.1µF capacitor close to this pin.
DNC	2	—	Do not connect a voltage source to this pin. Either leave the pin floating or connect to GND to improve thermal performance.
FB	4	I	Feedback pin. This pin is connected to the noninverting input of the error amplifier internally and controls the output voltage. For output voltages equal to or less than the external reference voltage, connect this pin directly to the output pin. To attain output voltage values higher than the reference, use a voltage divider with external feedback resistors.
GND	6, 3	G	GND pin. Connect this pin to a low impedance path to ground.
IN	8	I	Input power-supply voltage pin. For best transient response and to minimize input impedance, use the recommended value or larger ceramic capacitor from IN to GND. See the *Recommended Operating Conditions* table. Place the input capacitor as close to the input pin of the device as possible to compensate for line influences. See the *Input and Output Capacitor Selection* section for more details.
NC	7	—	Not internally connected. For best thermal performance, connect these pins to GND.
OUT	1	O	Regulated output voltage pin. A capacitor is required from OUT to GND for stability. For best transient response, select a ceramic capacitor within the range of C_{OUT} values provided in the *Recommended Operating Conditions* table. Place this capacitor as close to output of the device as possible. See the *Input and Output Capacitor Selection* section for more details.
Thermal Pad	Pad		Thermal pad. Connect the pad to GND for best possible thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Unregulated input pin voltage	–40	45	V
V_{OUT}	Regulated output pin voltage	–5	45	V
V_{FB}	Feedback pin voltage	–5	45	V
$V_{ADJ/EN}$	Adjustable reference and enable pin voltage	–40	45	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may effect the device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2500	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±1000	
			Corner pins		

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	3.3		40	V
V_{OUT}	Output voltage	2		40	V
$V_{ADJ/EN}$	Adjust pin voltage	2		40	V
V_{FB}	Feedback pin voltage	0		40	V
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor(1)		1		µF
C_{OUT}	Output capacitor(2)	1		100	µF
ESR	Output capacitor ESR requirements	0.001		2	Ω
T_J	Operating junction temperature	–40		150	°C

(1) For robust EMI performance the minimum input capacitance recommended is 500nF.
(2) Effective output capacitance of 500nF minimum is required for stability.

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5.4 Thermal Information

THERMAL METRIC(1) (2)		TPS7B4260-Q1	
		DDA (HSOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	71.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.3	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	11.5	°C/W

(1) The thermal data is based on the JEDEC standard high-K board layout, JESD 51-7. This is a two-signal, two-plane, four-layer board with 2-oz. copper on the external layers. The copper pad is soldered to the thermal land pattern. Also, correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

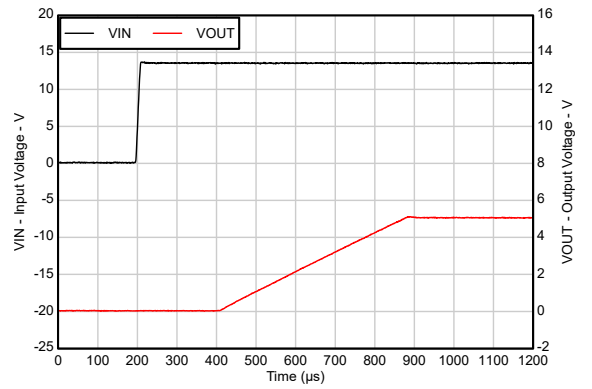
5.5 Electrical Characteristics

specified at T_J = –40°C to +150°C, V_{IN} = 13.5V, V_{OUT} = V_{FB}, I_{OUT} = 100µA, C_{OUT} = 1µF, C_{IN} = 1µF and $V_{ADJ/EN}$ = 5V (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_Q	Quiescent current	V_{IN} = 5.4V to 40V, I_{OUT} = 100µA, T_J = 25ºC		55	70	µA
		V_{IN} = 5.4V to 40V, I_{OUT} = 100µA, –40ºC < T_J < 85ºC			75	
		V_{IN} = 5.4V to 40V, I_{OUT} = 100µA			80	
I_{GND}	Ground current	V_{IN} = 5.4V to 40V, $V_{ADJ/EN}$ = 5V, I_{OUT} = 300mA			3.2	mA
$I_{SHUTDOWN}$	Shutdown supply current	$V_{ADJ/EN}$ = 0V			3.8	µA
$I_{ADJ/EN}$	ADJ/EN pin current	I_{OUT} = 100µA			1.2	µA
$V_{UVLO\ (RISING)}$	Rising input supply UVLO	V_{IN} rising, I_{OUT} = 5mA	2.6	2.7	2.85	V
$V_{UVLO\ (FALLING)}$	Falling input supply UVLO	V_{IN} falling, I_{OUT} = 5mA	2.3	2.4	2.5	V
$V_{UVLO\ (HYST)}$	$V_{UVLO(IN)}$ hysteresis			300		mV
V_{IL}	Enable logic input low level				0.8	V
V_{IH}	Enable logic input high level		1.8			V
ΔV_{OUT}	Output voltage tracking accuracy	V_{IN} = V_{OUT} + 1.2V to 40V, I_{OUT} = 100µA to 300mA (1)	–6		6	mV
$\Delta V_{OUT\ (\Delta VIN)}$	Line regulation	V_{IN} = V_{OUT} + 1.2V to 40V, I_{OUT} = 100µA	–0.4		0.4	mV
$\Delta V_{OUT\ (\Delta IOUT)}$	Load regulation	V_{IN} = V_{OUT} + 1.2V, I_{OUT} = 100µA to 300mA (1)			2.1	mV
V_{DO}	Dropout voltage	I_{OUT} = 200mA, $V_{ADJ/EN}$ ≥ 3.3V, V_{IN} = $V_{ADJ/EN}$		330	700	mV
I_{CL}	Output current limit	V_{IN} = V_{OUT} + 1.2V, V_{OUT} short to 90% x $V_{ADJ/EN}$	301	430	560	mA
PSRR	Power-supply ripple rejection	V_{RIPPLE} = 1V_{PP}, frequency = 100Hz, I_{OUT} ≥ 5mA		80		dB
V_n	Output noise voltage	V_{OUT} = 3.3V, I_{OUT} = 1mA, BW = 10Hz to 100KHz, a 5µV_{RMS} reference is used for this measurement		150		µV_{RMS}
I_{REV}	Reverse current at V_{IN}	V_{IN} = 0V, V_{OUT} = 32V	–0.6		0.6	µA
I_{REV-N1}	Reverse current at negative V_{IN}	V_{IN} = –20V, V_{OUT} = 20V	–1.2		1.2	µA
I_{FB}	Feedback pin current			0.1	0.25	µA
$T_{SD(SHUTDOWN)}$	Junction shutdown temperature			175		°C
$T_{SD(HYST)}$	Hysteresis of thermal shutdown			15		°C

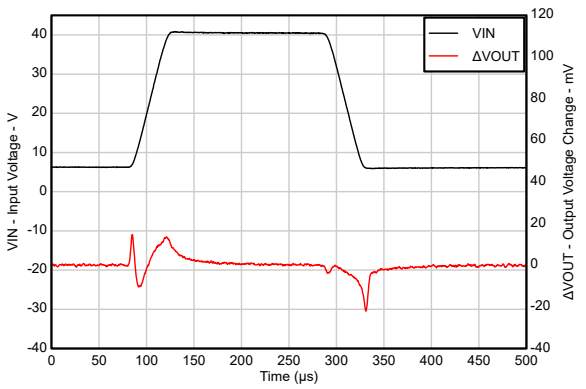
(1) Because the power dissipation is potentially large, this specification is measured using pulse testing with a low duty cycle. See the thermal information table for more information on how much power the device dissipates while maintaining a junction temperature below 150°C.

5.6 Typical Characteristics



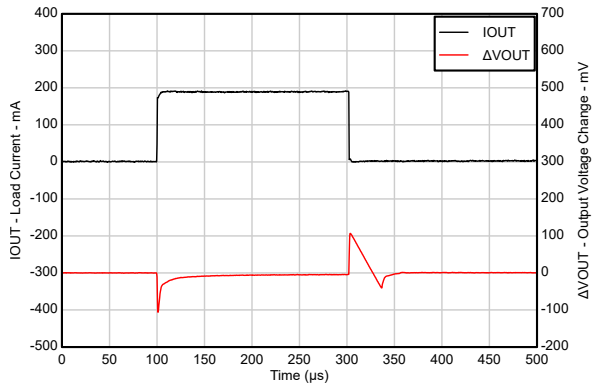
V_{IN} = 0V to 13.5V at a rate of 1V/µs , $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, C_{OUT} = 1µF, I_{OUT} = 200mA

図 5-1. Start-Up Profile



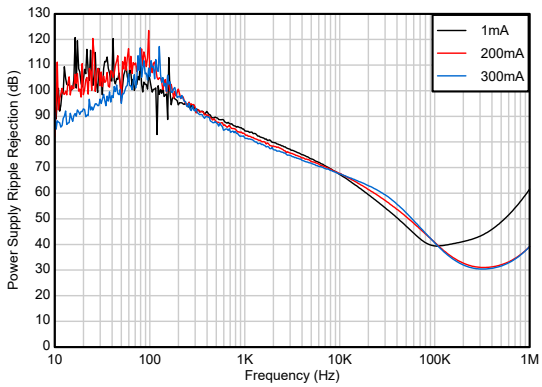
V_{IN} = 6V to 40V at a rate of 1V/µs , $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, C_{OUT} = 1µF, I_{OUT} = 200mA

図 5-2. Line Transient



V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, C_{OUT} = 1µF, I_{OUT} = 1mA to 200mA at 1A/µs

図 5-3. Load Transient



V_{IN} = 13.5V, $V_{ADJ/EN}$ = 5V, V_{FB} = V_{OUT}, C_{OUT} = 1µF

図 5-4. PSRR vs Frequency

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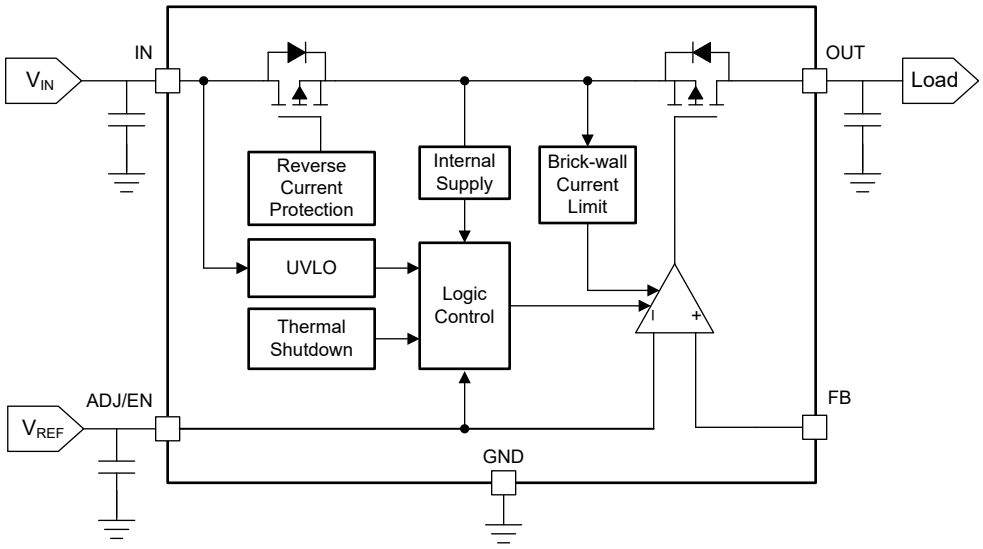
6 Detailed Description

6.1 Overview

The TPS7B4260-Q1 is an integrated, low-dropout (LDO) voltage tracker with ultra-low tracking tolerance. Because of the high risk of cable shorts when powering off-board sensors, multiple features are built into the LDO. These features protect against fault conditions resulting in short to battery, short to GND, and reverse current flow.

In addition, this device also features thermal shutdown protection, brick-wall current limiting, undervoltage lockout (UVLO), and reverse polarity protection.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Tracker Output Voltage (V_{OUT})

Because this device is a tracking LDO, the output voltage is determined by the voltage provided to the ADJ/EN pin. The LDO remains disabled as long as $V_{ADJ/EN}$ is less than V_{IL}. When $V_{ADJ/EN}$ exceeds V_{IH}, the output voltage V_{OUT} begins to rise. The device has a soft-start feature incorporated, which allows the output voltage to rise linearly and limits the in-rush current at start-up. After start-up and attaining steady state, V_{FB} remains within ±6mV from the voltage set on the ADJ/EN pin over all specified operating conditions. V_{FB} is the feedback pin voltage.

6.3.1.1 Output Voltage Equal to Reference Voltage

図 6-1 shows the external reference voltage applied directly to the ADJ/EN pin and the FB pin connected to the OUT pin. Under these conditions, the LDO output voltage is equal to the reference voltage, as given in 式 1.

$$V_{OUT} = V_{REF} \quad (1)$$

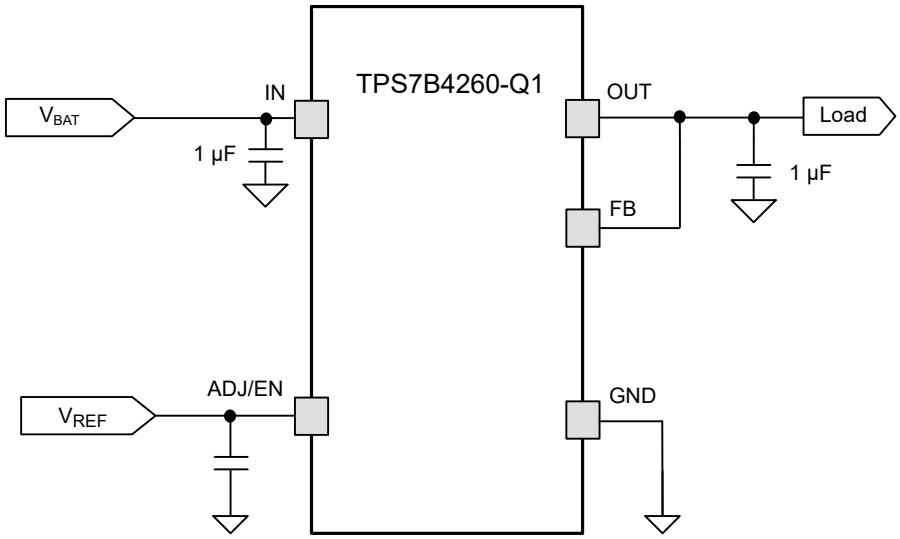


図 6-1. Tracker Output Voltage Equal to Reference Voltage

6.3.1.2 Output Voltage Less Than the Reference Voltage

Connecting an external resistor divider at the ADJ/EN pin, as shown in 図 6-2, helps generate an output voltage lower than the reference voltage. Both R_1 and R_2 must be less than 100kΩ to minimize the error in voltage caused by the ADJ/EN pin leakage current, $I_{ADJ/EN}$. 式 2 calculates V_{OUT}.

$$V_{OUT} = \frac{(V_{REF} \times R_2)}{R_1 + R_2} \quad (2)$$

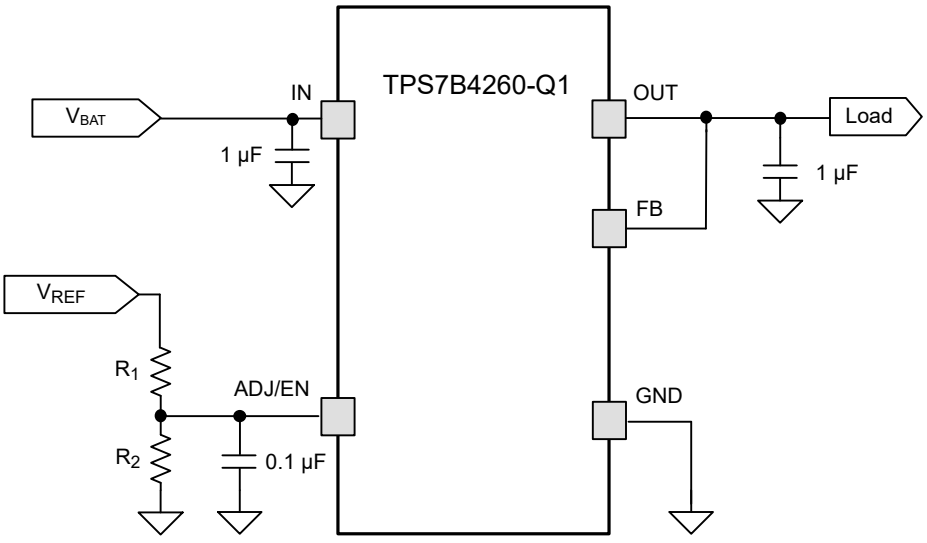


図 6-2. Tracker Output Voltage Less Than the Reference Voltage

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6.3.1.3 Output Voltage Larger than the Reference Voltage

Connecting an external resistor divider between the OUT and FB pin, as shown in 図 6-3, helps generate an output voltage higher than the reference voltage. Both R_1 and R_2 must be less than 100kΩ to minimize the error in voltage caused by the FB pin leakage current, I_{FB}. 式 3 calculates V_{OUT}.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

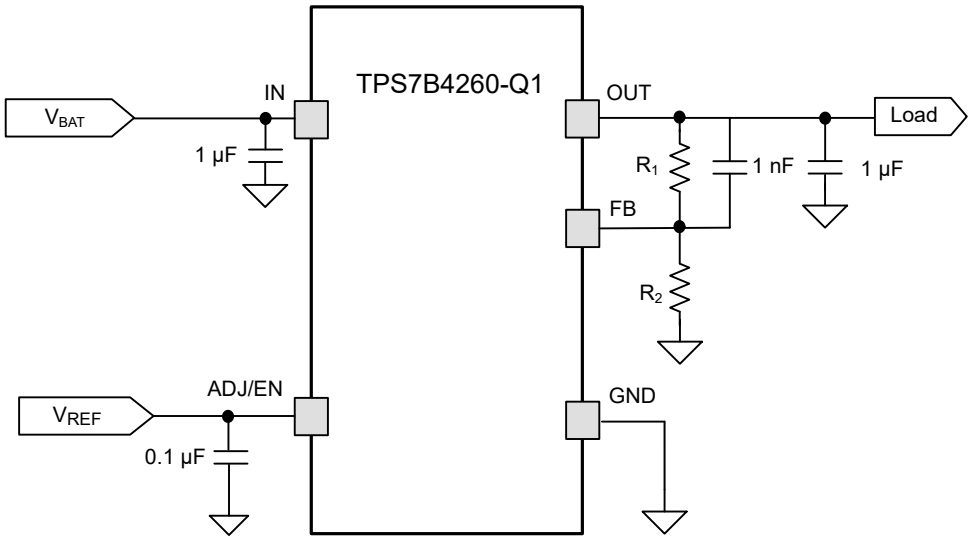

図 6-3. Tracker Voltage Larger Than the Reference Voltage

6.3.2 Reverse Current Protection

The TPS7B4260-Q1 incorporates a back-to-back PMOS topology that protects the device from damage against a fault condition, resulting in V_{OUT} being higher than V_{IN} and the subsequent flow of reverse current. No damage occurs to the device if this fault condition occurs, provided the *Absolute Maximum Ratings* are not violated. This integrated protection feature eliminates the need for an external diode. The reverse current comparator typically responds to a reverse voltage condition in 10µs, and along with the body diode of the blocking PMOS transistor, limits the reverse current to I_{REV} specified in the *Electrical Characteristics* table.

6.3.3 Undervoltage Lockout

The device has an internally fixed undervoltage lockout (UVLO) threshold. Undervoltage lockout activates when the input voltage V_{IN} drops below the undervoltage lockout level (see the $V_{UVLO(FALLING)}$ parameter in the *Electrical Characteristics* table). This activation makes sure the regulator is not latched into an unknown state during a low input supply voltage. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up in the standard power-up sequence when the input voltage recovers to the required level (see the $V_{UVLO(RISING)}$ parameter in the table).

6.3.4 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 175°C, which allows the device to cool. When the junction temperature cools to approximately 160°C, the output circuitry enables. Although the device can be enabled at such high temperatures, the device parameters and performance are specified up to a junction temperature of 150°C. Based on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit can cycle off and on until the condition that causes excessive power dissipation is removed. This cycling limits the thermal dissipation within the regulator, thus protecting the regulator from damage as a result of overheating.

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The internal protection circuitry of the TPS7B4260-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS7B4260-Q1 into thermal shutdown degrades device reliability.

6.3.5 Current Limit

The device has an internal current limit circuit that protects the device during overcurrent or shorting conditions. The current-limit circuit, as shown in 図 6-4, is a brick-wall scheme. When the device is in current limit, the device sources I_{CL} and the output voltage is not regulated. In this scenario, the output voltage depends on the load impedance.

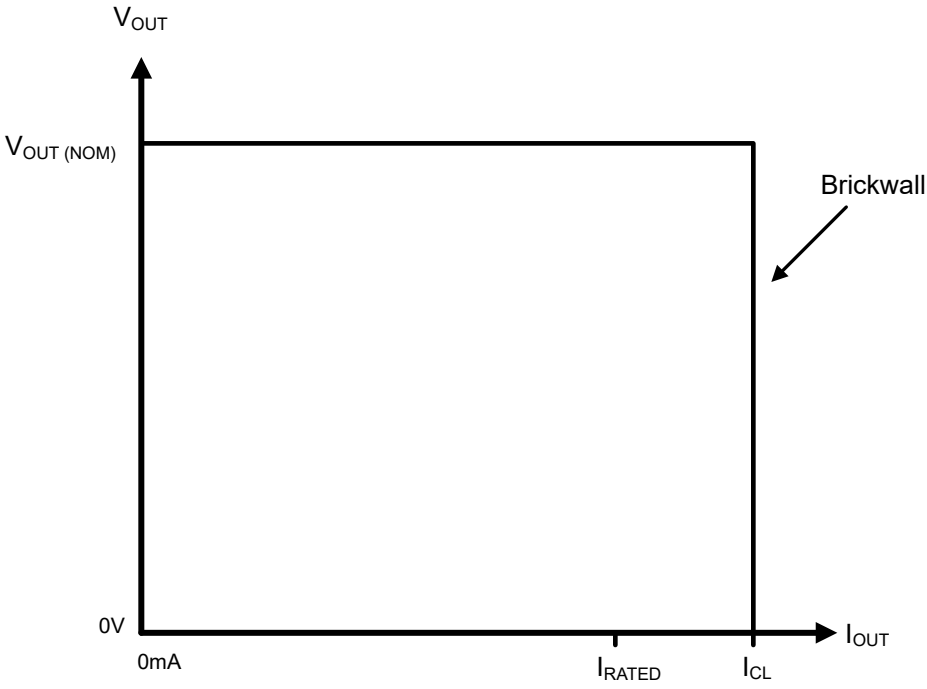

図 6-4. Brickwall Current Limit Scheme

During current-limit events, the potential for high power dissipation exists because of the elevated current level and the increased input-to-output differential voltage (V_{IN} – V_{OUT}). If the heat dissipation is substantial, the device enters thermal shutdown. If the current-limit condition is not removed when the device turns back on after cooling, the device enters thermal shutdown again. This cycle continues until the current-limit condition is removed. The device survives this fault, but repeatedly operating in this mode degrades long-term reliability.

6.3.6 Output Short to Battery

When the output is shorted to the battery (see 図 6-5), the TPS7B4260-Q1 survives and no damage occurs to the device. A short to the battery can also occur when the device is powered by a voltage source that is lower than the battery voltage (see 図 6-6). In this example case, the TPS7B4260-Q1 supply input voltage is set at 7V when a short to battery (14V typical) occurs on V_{OUT}, which typically runs at 5V. The back-to-back PMOS FETs topology helps limit the continuous reverse current flowing through V_{IN} to I_{REV}, as provided in the *Electrical Characteristics* table.

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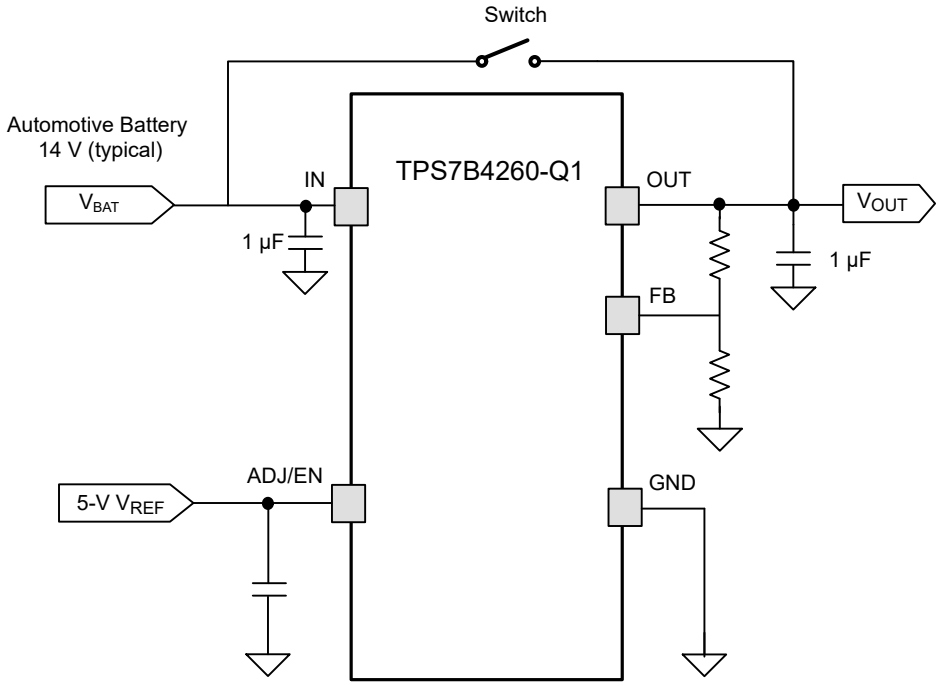

図 6-5. Tracker Output Short to Battery

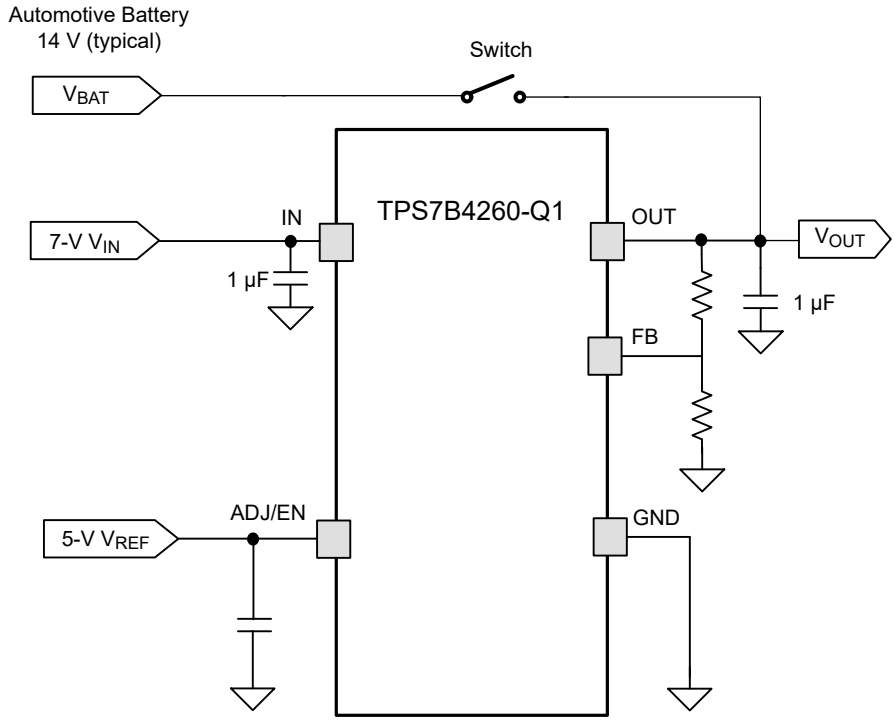

図 6-6. Tracker Output Voltage Higher Than Input Voltage

6.3.7 Tracking Regulator With an Enable Circuit

By pulling the reference voltage below V_{IL}, the device disables and enters a sleep state where the device draws 3.8µA (max) from the power supply. In a typical application, the reference voltage is generally sourced from another LDO voltage rail. A scenario where the device must be disabled without a shutdown of the reference voltage can occur. The device can be configured as shown in 図 6-7 in this case. The TPS7B84-Q1 is a 150mA LDO with ultra-low quiescent current that provides the reference voltage to both the TPS7B4260-Q1 and the ADC. The operational status of the device is controlled by a microcontroller (MCU) input or output (I/O).

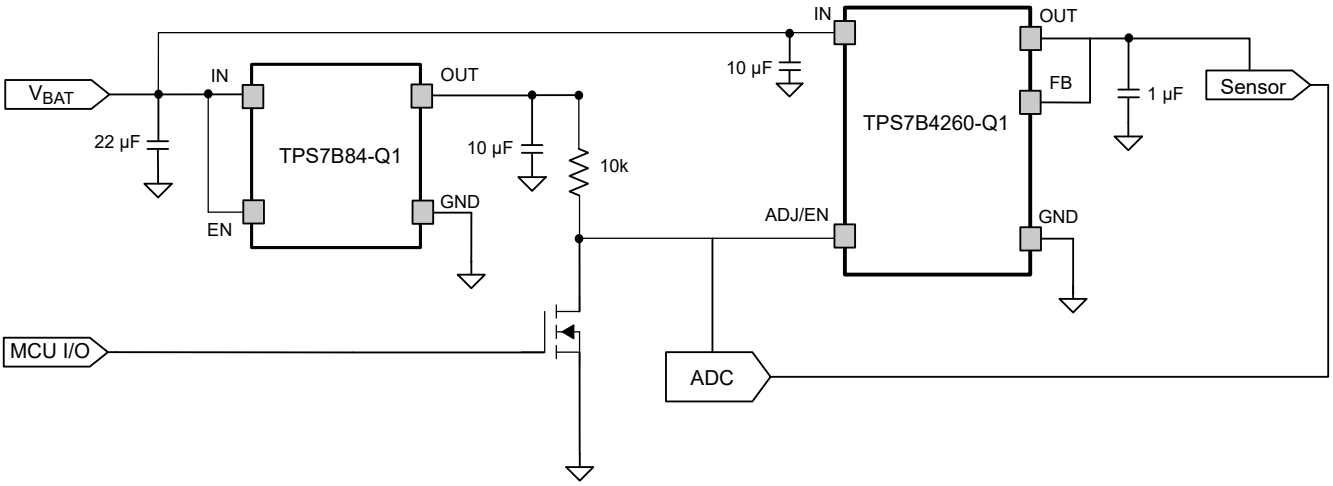

図 6-7. Tracking LDO With an Enable Circuit

ADVANCE INFORMATION

6.4 Device Functional Modes

表 6-1 shows the conditions that lead to the different modes of operation. See the *Electrical Characteristics* table for parameter values.

表 6-1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER(1)			
	V_{IN}	$V_{ADJ/EN}$	I_{OUT}	T_J
Normal operation	$V_{IN} > V_{OUT(Nom)} + V_{DO}$ and $V_{IN} \geq V_{IN(min)}$	$V_{ADJ/EN} > V_{IH}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J \leq 150℃$
Dropout operation	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{ADJ/EN} > V_{IH}$	$I_{OUT} \leq I_{OUT(max)}$	$T_J < T_{SD(shutdown)}$
Disabled (any true condition disables the device)	$V_{IN} < V_{UVLO}$	$V_{ADJ/EN} < V_{IL}$	Not applicable	$T_J > T_{SD(shutdown)}$

(1) The device turns on when V_{IN} is greater than $V_{UVLO(RISING)}$ and $V_{ADJ/EN}$ is greater than the enable rising threshold V_{IH}.

6.4.1 Normal Operation

The device output voltage $V_{OUT(Nom)}$ tracks the reference voltage at the ADJ/EN pin when the following conditions are met:

- The input voltage is at least 3.3V ($V_{IN(min)}$) and greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$)
- The reference voltage at the ADJ/EN pin is greater than the enable rising threshold V_{IH} and stays stable at the appropriate V_{REF} value
- The output current is less than $I_{OUT(max)}$ ($I_{OUT} \leq 300mA$)
- The device junction temperature is less than 150℃ ($T_J \leq 150℃$)

6.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In this mode, the transient performance of the device becomes significantly degraded. During this mode, the pass transistor is driven fully on. Line or load transients in dropout potentially result in large output voltage deviations.

When the device is in a steady dropout state (defined as when the device is in dropout, $V_{IN} < V_{OUT(NOM)} + V_{DO}$, directly after being in a normal regulation state, but *not* during start up), the pass transistor is driven into the ohmic or triode region. When the input voltage returns to a value greater than or equal to the nominal output voltage plus the dropout voltage ($V_{OUT(NOM)} + V_{DO}$), the output voltage can overshoot for a short period of time while the device pulls the pass transistor back into the saturation region.

6.4.3 Operation With V_{IN} < 3.3V

For input voltages below 3.3V and above $V_{UVLO\ (FALLING)}$, the LDO continues to operate. However, certain internal circuits potentially do not have proper headroom to operate within specification. When the input voltage drops below $V_{UVLO\ (FALLING)}$, the device shuts off.

6.4.4 Disable With ADJ/EN Control

The ADJ/EN pin operates as both the reference and the enable pin to the LDO. The output of the device can be shutdown by forcing $V_{ADJ/EN}$ less than V_{IL}. When disabled, the pass transistor is turned off, the internal circuits are shutdown, and the LDO is in a low-power mode.

ADVANCE INFORMATION

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

7.1.1 Dropout Voltage

Dropout voltage (V_{DO}) is defined as $V_{IN} – V_{OUT}$ when the pass transistor is fully on. V_{IN} is the input voltage and V_{OUT} is the output voltage. This condition arises when the input voltage falls to the point where the error amplifier drives the gate of the pass transistor to the rail. During this condition, there is no remaining headroom for the control loop to operate. At this operating point, the pass transistor is driven fully on. Dropout voltage directly specifies a minimum input voltage greater than the nominal programmed output voltage where the output voltage is expected to stay in regulation. If the input voltage falls to less than the nominal output regulation, then the output voltage follows, minus the dropout voltage (V_{DO}).

In dropout mode, the output voltage is no longer regulated, and transient performance is severely degraded. The device loses PSRR, and load transients potentially cause large output voltage deviation.

For a CMOS regulator, the dropout voltage is determined by the drain-source on-state resistance ($R_{DS(ON)}$) of the pass transistor. Therefore, if the linear regulator operates at less than the rated output current (I_{RATED}, see the *Recommended Operating Conditions* table), the dropout voltage for that current scales accordingly. The following equation calculates the $R_{DS(ON)}$ of the device.

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (4)$$

7.1.2 Reverse Current

The TPS7B4260-Q1 incorporates reverse current protection that prevents damage from a fault condition, resulting in V_{OUT} being higher than V_{IN}. During such a fault condition, where the V_{IN} and V_{OUT} absolute maximum ratings are not violated and $V_{OUT} – V_{IN}$ is less than 40V, no damage occurs and less than 1.1µA of reverse current flows through the LDO. The reverse current comparator typically responds to a reverse voltage condition and, along with the body diode of the blocking PMOS transistor, limits the reverse current in 10µs.

ADVANCE INFORMATION

7.2 Typical Application

図 7-1 shows a typical application circuit for the TPS7B4260-Q1.

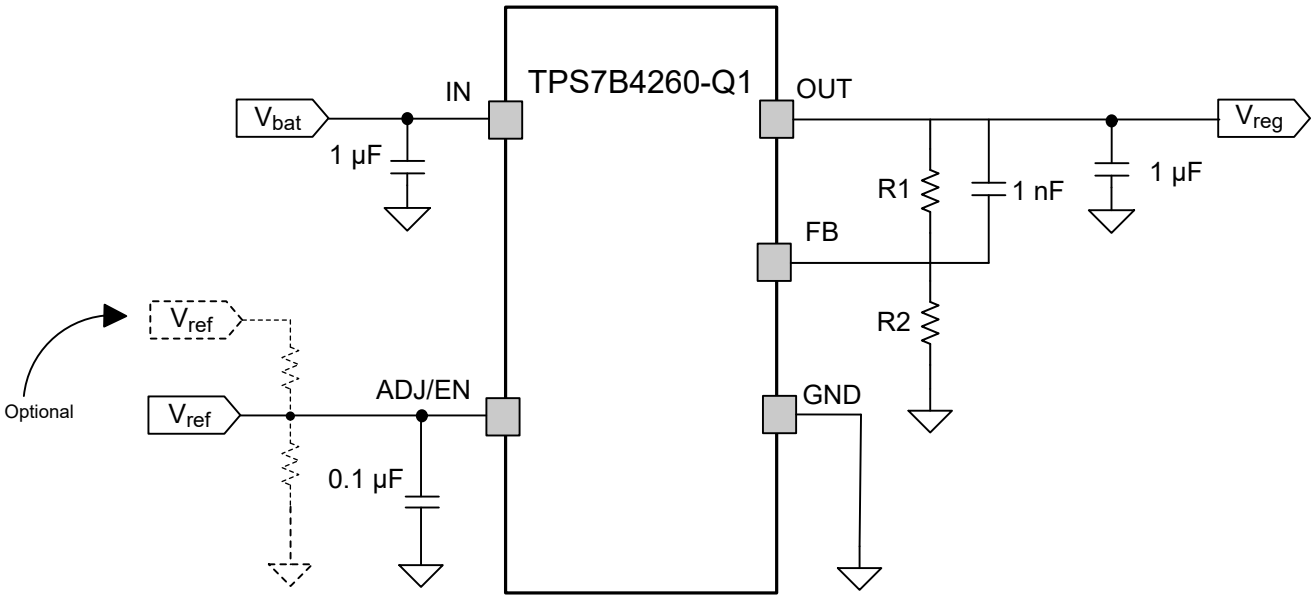

図 7-1. Typical Application Schematic

7.2.1 Design Requirements

Use the parameters listed in 表 7-1 for this design example.

表 7-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage	3.3V to 40V
ADJ/EN reference voltage	2V to 40V
Output voltage	2V to 40V
Output current rating	300mA
Output capacitor range	1µF to 100µF
Output capacitor ESR range	1mΩ to 2Ω

7.2.2 Detailed Design Procedure

7.2.2.1 Input and Output Capacitor Selection

Depending on the end application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to prevent a significant droop in output voltage and reset of downstream component from occurring. Use a low equivalent series resistance (ESR) ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

The TPS7B4260-Q1 requires an output capacitor of at least 1µF (500nF or larger capacitance) for stability and an ESR between 0.001Ω and 2Ω. Without the output capacitor, the regulator oscillates. For best transient performance, use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and ESR over temperature. When choosing a capacitor for a specific application, be mindful of the DC bias characteristics for the capacitor. Higher output voltages cause a significant derating of the capacitor. For most applications, a low ESR, 10µF ceramic capacitor on the OUT pin is sufficient to provide excellent transient performance.

ADVANCE INFORMATION

An input capacitor is not required for stability. However, a good analog practice is to connect a capacitor (500nF or higher) between the GND and IN pin of the TPS7B4260-Q1. Some input supplies have a high impedance, thus placing the input capacitor on the input supply helps reduce input impedance. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. If the input supply has high impedance over a large range of frequencies, use several input capacitors in parallel to lower the impedance over frequency. Use a higher-value capacitor if large, fast rise-time load transients are anticipated, or if the device is located several inches from the input power source.

7.2.2.2 Feedback Resistor Selection

V_{OUT} is set by the voltage at the ADJ/EN pin and the external feedback resistors R_1 and R_2 according to the following equation:

$$V_{OUT} = V_{ADJ/EN} \times \left(1 + \frac{R_1}{R_2}\right) \quad (5)$$

To ignore the FB pin current error term in the V_{OUT} equation, set the feedback divider current to 100 times the FB pin current listed in the *Electrical Characteristics* table. This setting provides the maximum feedback divider series resistance, as shown in the following equation:

$$R_1 + R_2 \leq \frac{V_{OUT}}{(I_{FB} \times 100)} \quad (6)$$

7.2.2.3 Feedforward Capacitor

A feedforward capacitor (C_{FF}) is recommended to be connected between the OUT pin and the FB pin. C_{FF} improves transient, noise, and PSRR performance. A higher capacitance C_{FF} can be used; however, the start-up time increases. For a detailed description of C_{FF} tradeoffs, see the *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note.

As shown in 図 7-2, poor layout practices and using long traces at the FB pin result in the formation of a parasitic capacitor (C_{FB}).

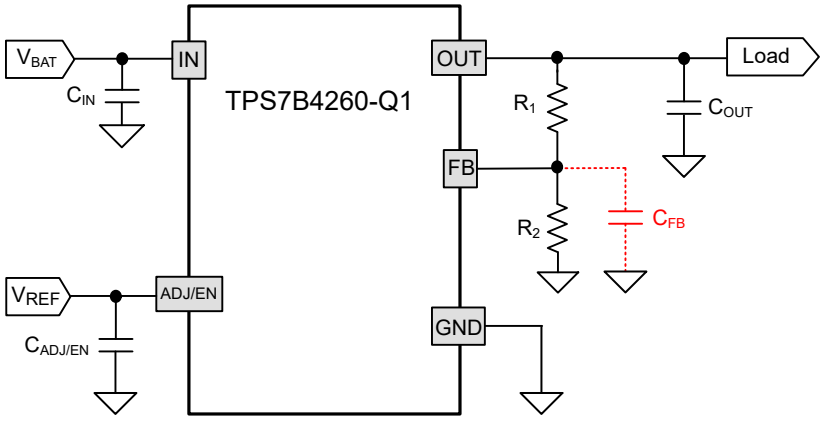

図 7-2. Parasitic Capacitor on the FB Pin

C_{FB}, along with the feedback resistors R_1 and R_2 can result in the formation of an uncompensated pole in the transfer function of the loop gain. A C_{FB} value as small as 20pF can cause the parasitic pole frequency, given by 式 7, to fall within the bandwidth of the LDO and result in instability.

$$f_P = \frac{1}{(2 \times \pi \times C_{FB} \times (R_1 \parallel R_2))} \quad (7)$$

ADVANCE INFORMATION

Adding a feedforward capacitor (C_{FF}), as shown in 図 7-3, creates a zero in the loop gain transfer function that can compensate for the parasitic pole created by C_{FB}. 式 8 and 式 9 calculate the pole and zero frequencies.

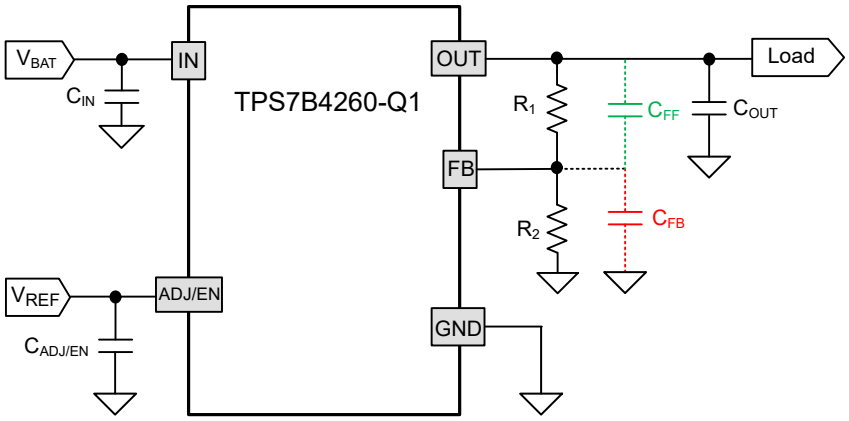

図 7-3. Feedforward Capacitor Helps Mitigate Impact of the Parasitic Feedback Capacitor

$$f_P = \frac{1}{(2 \times \pi \times (R_1 \parallel R_2) \times (C_{FF} + C_{FB}))} \quad (8)$$

$$f_Z = \frac{1}{(2 \times \pi \times C_{FF} \times R_1)} \quad (9)$$

The C_{FF} value that makes f_P equal to f_Z, and result in a pole-zero cancellation, depends on the values of C_{FB} and the feedback resistors used in the application. Alternatively, if the feedforward capacitor is selected so that $C_{FF} \gg C_{FB}$, then the pole and zero frequencies given by 式 8 and 式 9 are related as:

$$\frac{f_p}{f_z} \approx \left(1 + \frac{R_1}{R_2}\right) = \frac{V_{OUT}}{V_{ADJ/EN}} \quad (10)$$

In most applications, particularly where a 3.3V or 5V V_{OUT} is generated, this ratio is not very large, implying that the frequencies are located close to each other and therefore the parasitic pole is compensated. Even for large V_{OUT} values, where this ratio can be as large as 20, a C_{FF} value in the range 100pF ≤ C_{FF} ≤ 10nF typically helps prevent instability caused by the parasitic capacitance on the feedback node.

Following good layout practices, as described in the *Layout Guidelines* section and in the *TRKRLDOEVM-119 General-Purpose Tracker LDO Evaluation Module* user guide, helps minimize the parasitic feedback pin capacitance to values that prevent the resulting parasitic pole from causing instability.

ADVANCE INFORMATION

7.2.3 Application Curves

The following images illustrate the functions of $R_{\theta JA}$ and ψ_{JB} versus copper area and thickness for the HSOIC-8 (DDA) package. These plots are generated with a 101.6mm × 101.6mm × 1.6mm printed circuit board (PCB) of two and four layers. For the 2-layer board, the bottom layer is a ground plane of constant size, and the top layer copper is connected to GND and varied. For the 4-layer board, the second layer is a ground plane of constant size, the third layer is a power plane of constant size. The top and bottom layers copper fills are connected to GND and varied at the same rate. For the 4-layer board, inner planes use 1oz copper thickness. Outer layers are simulated with both 1oz and 2oz copper thickness. A 3 × 3 array of thermal vias with a 300µm drill diameter and 25µm copper plating is located underneath the device. The thermal vias connect the top layer, the bottom layer and, in the case of the 4-layer board, the first inner GND plane. *PowerPAD™ Thermally Enhanced Package* application note discusses the impact that thermal vias have on thermal performance.

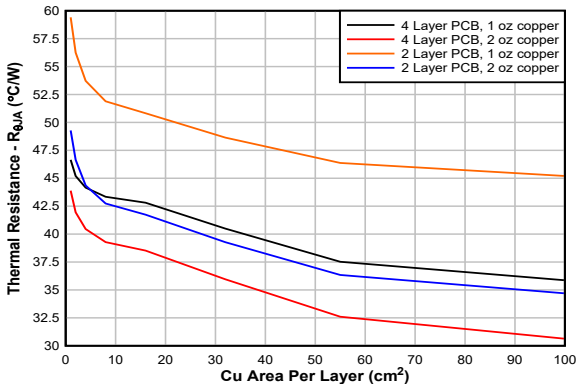

図 7-4. $R_{\theta JA}$ vs Copper Area (HSOIC-8 Package)

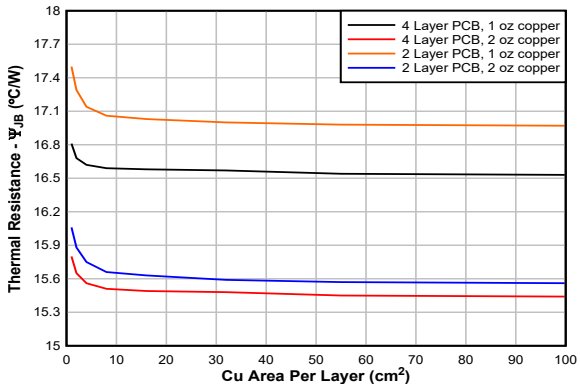

図 7-5. ψ_{JB} vs Copper Area (HSOIC-8 Package)

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 3V to 40V.

7.4 Layout

7.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close as possible to each other, connected by a wide, component-side, copper surface. Using vias and long traces to the input and output capacitors is strongly discouraged and negatively affects system performance. Use a ground reference plane either embedded in the PCB or located on the bottom side of the PCB opposite the components. This reference plane serves to provide accuracy of the output voltage, shield noise, and behaves similarly to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

7.4.1.1 Package Mounting

Solder-pad footprint recommendations for the TPS7B4260-Q1 are available at the end of this document and at www.ti.com.

7.4.1.2 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), design the board with separate ground planes for V_{IN} and V_{OUT}. Connect each ground plane only at the GND pin of the device. In addition, directly connect the ground connection for the output capacitor to the GND pin of the device.

Minimize equivalent series inductance (ESL) and ESR to maximize performance and provide stability. Place each capacitor as close as possible to the device and on the same side of the PCB as the regulator.

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Do not place any capacitors on the opposite side of the PCB from where the regulator is installed. Using vias and long traces is strongly discouraged because of the negative impact on system performance. Vias and long traces potentially also cause instability.

If possible, and to provide the maximum performance denoted in this document, use the same layout pattern used for the TPS7B4260-Q1 evaluation board. This evaluation board is available at www.ti.com.

7.4.1.3 Power Dissipation and Thermal Considerations

式 11 calculates the device power dissipation.

$$P_D = I_{OUT} \times (V_{IN} - V_{OUT}) + I_Q \times V_{IN} \quad (11)$$

where:

- P_D = Continuous power dissipation
- I_{OUT} = Output current
- V_{IN} = Input voltage
- V_{OUT} = Output voltage
- I_Q = Quiescent current

Because I_Q is much less than I_{OUT}, the term $I_Q \times V_{IN}$ in 式 11 can be ignored.

Calculate the junction temperature (T_J) with 式 12 for a device under operation at a given ambient air temperature (T_A).

$$T_J = T_A + (R_{\theta JA} \times P_D) \quad (12)$$

where:

- $R_{\theta JA}$ = Junction-to-junction-ambient air thermal impedance

式 13 calculates a rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (R_{\theta JA} \times P_D) \quad (13)$$

The maximum ambient air temperature (T_{AMAX}) at which the device can operate can be calculated with 式 14 for a given maximum junction temperature (T_{JMAX}).

$$T_{AMAX} = T_{JMAX} - (R_{\theta JA} \times P_D) \quad (14)$$

7.4.1.4 Thermal Performance Versus Copper Area

The most used thermal resistance parameter $R_{\theta JA}$ is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard (図 7-6), PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

ADVANCE INFORMATION

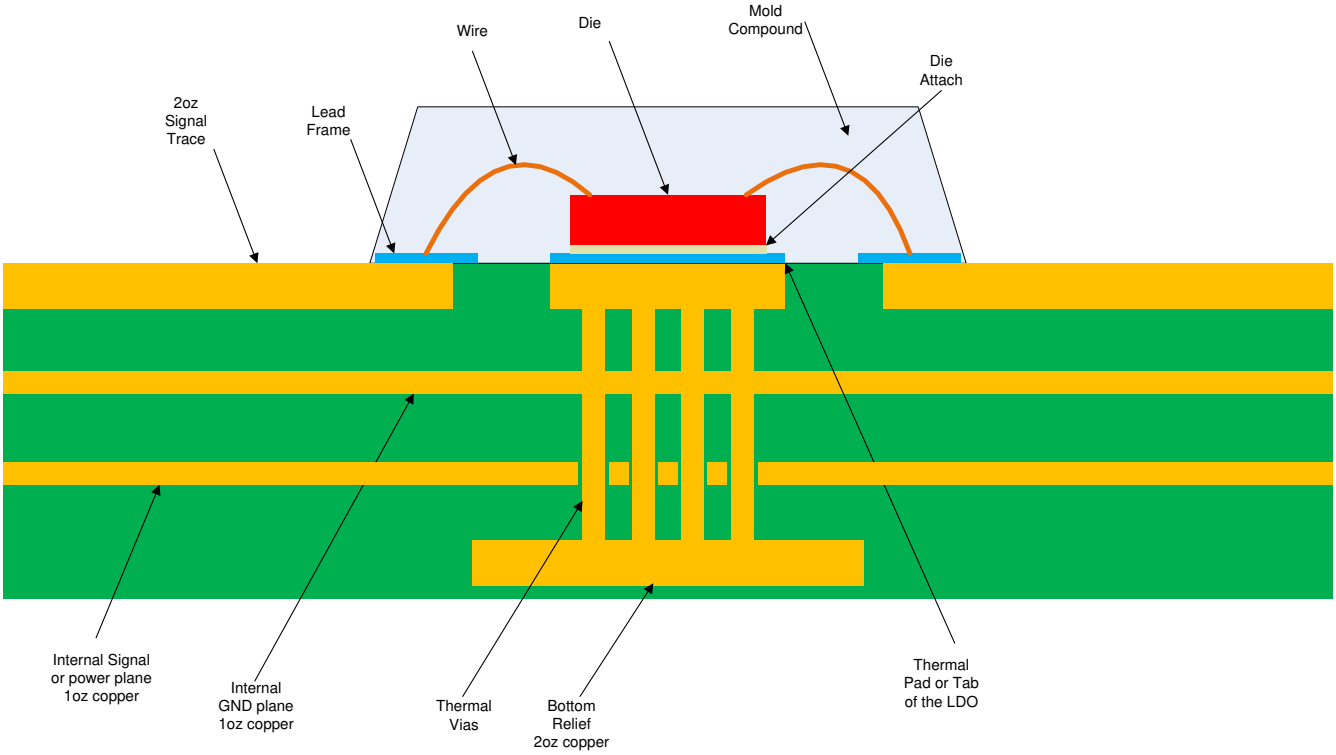

図 7-6. JEDEC Standard 2s2p PCB

7.4.2 Layout Example

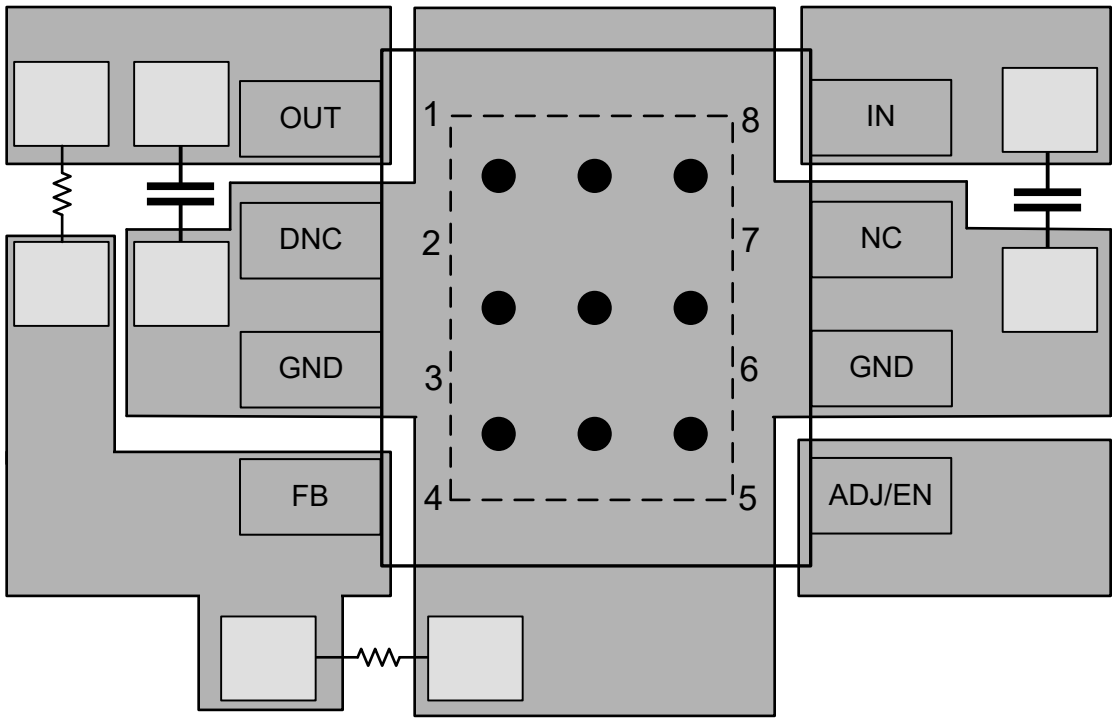

図 7-7. Layout Example

ADVANCE INFORMATION

8 Device and Documentation Support

8.1 Device Support

8.1.1 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT(1)	V_{OUT}
TPS7B4260**QDDARQ1**	In the HSOIC (DDA) package: **Q** indicates that this device is a grade-1 device in accordance with the AEC-Q100 standard. **R** is the packaging quantity. **Q1** indicates that this device is an automotive grade (AEC-Q100) device.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *TPS7B84-Q1 150mA, 40V, Adjustable, Low-Dropout Regulator* data sheet
- Texas Instruments, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* application note
- Texas Instruments, *TRKRLDOEVM-119 General-Purpose Tracker LDO Evaluation Module* user guide

8.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.5 Trademarks

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8.6 静電気放電に関する注意事項

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

ADVANCE INFORMATION

DATE	REVISION	NOTES
January 2025	*	Initial release.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

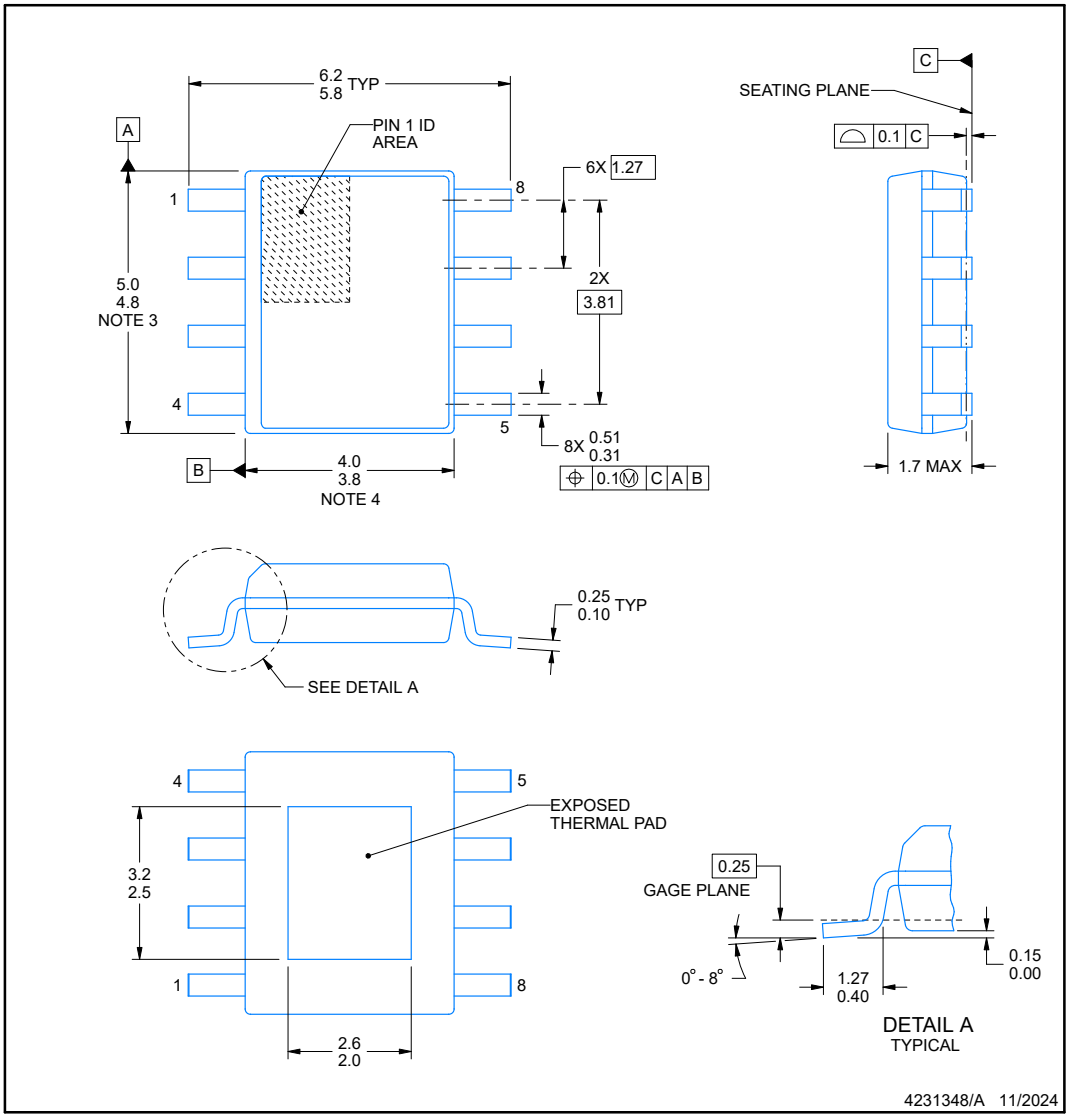
ADVANCE INFORMATION

10.1 Mechanical Data

PACKAGE OUTLINE

DDA0008J-C02 **PowerPAD™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

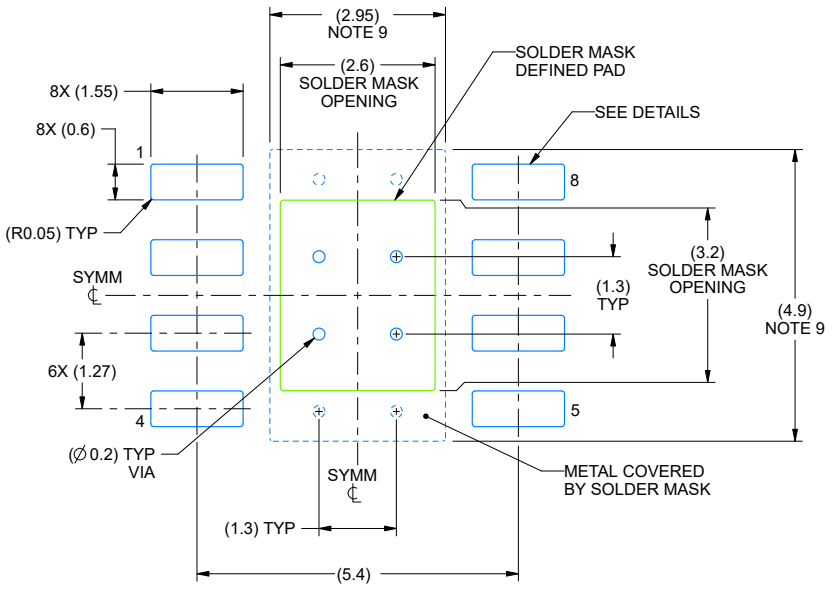
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.

TEXAS INSTRUMENTS
www.ti.com

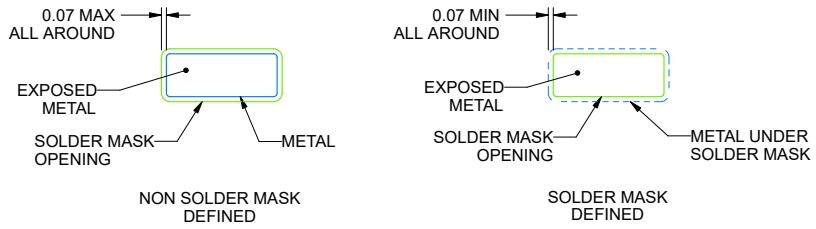
EXAMPLE BOARD LAYOUT

DDA0008J-C02 — **PowerPAD ™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:10X



SOLDER MASK DETAILS

4231348/A 11/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.

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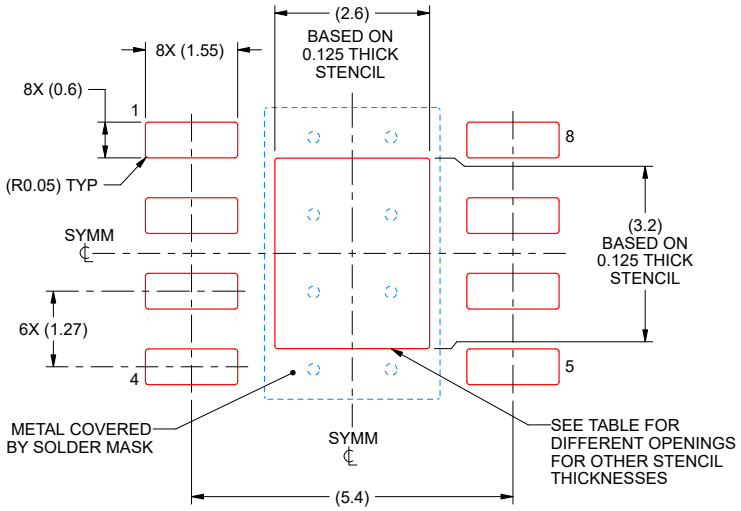
ADVANCE INFORMATION

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

DDA0008J-C02 — **PowerPAD ™ SOIC - 1.7 mm max height**

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 3.58
0.125	2.6 X 3.2 (SHOWN)
0.150	2.37 X 2.92
0.175	2.20 X 2.70

4231348/A 11/2024

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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