

TPS7A47-Q1 35V、1A、4.2μV_{RMS}、RF LDO電圧レギュレータ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み:
 - デバイス温度グレード1: 動作時周囲温度範囲 –40°C~125°C
 - デバイスHBM ESD分類レベル2
 - デバイスCDM ESD分類レベルC4A
- 入力電圧範囲: 3V~35V
- 動作時の接合部温度範囲: –40°C~+145°C
- 出力電圧ノイズ: 4.2μV_{RMS} (10Hz~100kHz)
- 電源除去率:
 - 82dB (100Hz)
 - 55dB以上 (10Hz~10MHz)
- 2つの出力電圧モード:
 - ANY-OUT™バージョン(ユーザーがPCBレイアウトにより出力をプログラム可能)
 - 出力電圧範囲: 1.4V~20.5V
 - 可変動作:
 - 出力電圧範囲: 1.4V~34V
- 出力電流: 1A
- 熱抵抗: $\theta_{JA} = 31.1^{\circ}\text{C}/\text{W}$
- ドロップアウト電圧: 1Aで307mV
- CMOSロジック・レベル互換のインエーブル・ピン
- 固定の電流制限とサーマル・シャットダウンを内蔵

2 アプリケーション

- 電圧制御の発振器(VCO)
- Rx、Tx、PA回路
- 車載用インフォテインメントおよびクラスタ
- オペアンプ、DAC、ADC、および他の高精度アナログ回路の電源レール

3 概要

TPS7A47-Q1デバイスは、正電圧(35V)、超低ノイズ(4.2μV_{RMS})の低ドロップアウト・リニア・レギュレータ(LDO)で、1Aの負荷に電力を供給できます。

TPS7A47-Q1の出力電圧は、ユーザーがプログラム可能なプリント基板(PCB)レイアウト(最高20.5V)、または外付けの帰還抵抗(最高34V)により設定できます。

TPS7A47-Q1は、システム性能を最大化するためにクリーンな電源レールが決定的に重要な、高精度、高分解能の計測機器アプリケーションを主な対象として、バイポーラ・テクノロジーで設計されています。この特長から、このデバイスはオペアンプ、アナログ/デジタル・コンバータ(ADC)、デジタル/アナログ・コンバータ(DAC)、その他の高性能アナログ回路への電源供給に最適です。

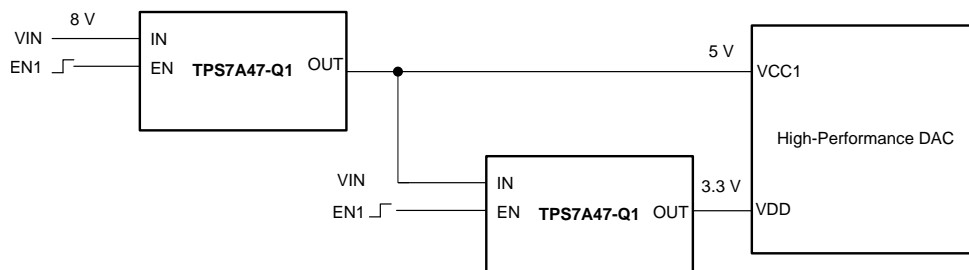
さらに、TPS7A47-Q1はDC/DCコンバータのポスト・レギュレーションにも理想的です。DC/DCスイッチング変換に本質的に付随する出力電圧リップルをフィルタ処理で取り除き、感受性の高い計測機器、オーディオ、RFアプリケーションにおいて、最大のシステム性能が保証されます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPS7A47-Q1	VQFN (20)	5.00mm×5.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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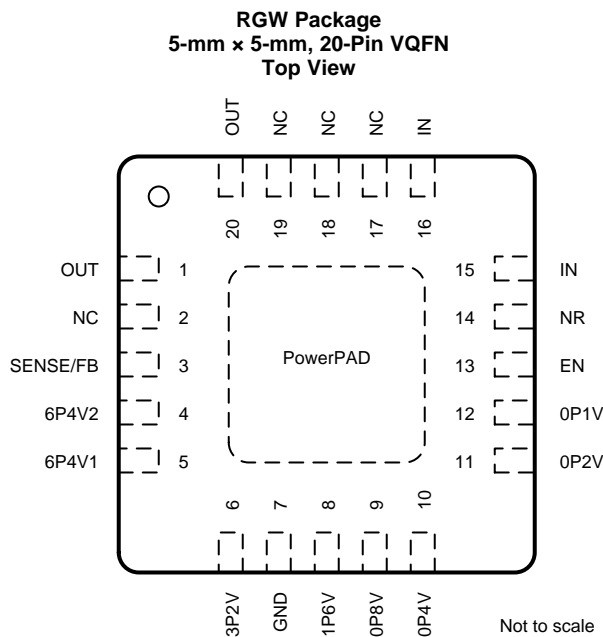
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4 改訂履歴

日付	改訂内容	注
2017年8月	*	初版

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
0P1V	12	I	When connected to GND, this pin adds 0.1 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P2V	11	I	When connected to GND, this pin adds 0.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P4V	10	I	When connected to GND, this pin adds 0.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
0P8V	9	I	When connected to GND, this pin adds 0.8 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
1P6V	8	I	When connected to GND, this pin adds 1.6 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
3P2V	6	I	When connected to GND, this pin adds 3.2 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V1	5	I	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
6P4V2	4	I	When connected to GND, this pin adds 6.4 V to the nominal output voltage of the regulator. Do not connect any voltage other than GND to this pin. If not used, leave this pin floating.
EN	13	I	Enable pin. The device is enabled when the voltage on this pin exceeds the maximum enable voltage, $V_{EN(HI)}$. If enable is not required, tie EN to IN.
GND	7	—	Ground
IN	15, 16	I	Input supply. A capacitor greater than or equal to 1 μ F must be tied from this pin to ground to assure stability. A 10- μ F capacitor is recommended to be connected from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedances are encountered.
NC	2, 17-19	—	This pin can be left open or tied to any voltage between GND and IN.
NR	14	—	Noise-reduction pin. When a capacitor is connected from this pin to GND, RMS noise can be reduced to very low levels. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. A 1- μ F capacitor is recommended to be connected from NR to GND (as close to the device as possible) to maximize ac performance and minimize noise.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1, 20	O	Regulator output. A capacitor greater than or equal to 10 μ F must be tied from this pin to ground to assure stability. A 47- μ F ceramic output capacitor is highly recommended to be connected from OUT to GND (as close to the device as possible) to maximize ac performance.
SENSE/FB	3	I	Control-loop error amplifier input. This pin is the SENSE pin if the device output voltage is programmed using ANY-OUT (no external feedback resistors). This pin must be connected to OUT. Connect this pin to the point of load to maximize accuracy. This pin is the FB pin if the device output voltage is set using external resistors. See the Adjustable Operation section for more details.
PowerPAD	Pad	—	Connect the PowerPAD to a large-area ground plane. The PowerPAD™ is internally connected to GND.

6 Specifications

6.1 Absolute Maximum Ratings

 over junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	IN pin to GND pin	−0.4	36	V
	EN pin to GND pin	−0.4	36	
	EN pin to IN pin	−36	0.4	
	OUT pin to GND pin	−0.4	36	
	NR pin to GND pin	−0.4	36	
	SENSE/FB pin to GND pin	−0.4	36	
	0P1V pin to GND pin	−0.4	36	
	0P2V pin to GND pin	−0.4	36	
	0P4V pin to GND pin	−0.4	36	
	0P8V pin to GND pin	−0.4	36	
	1P6V pin to GND pin	−0.4	36	
	3P2V pin to GND pin	−0.4	36	
	6P4V1 pin to GND pin	−0.4	36	
	6P4V2 pin to GND pin	−0.4	36	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T _J	−40	145	°C
	Storage, T _{stg}	−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the network ground terminal.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2500	V
	Charged-device model (CDM), per AEC Q100-011	±500	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_I	Input voltage	3.0		35.0	V
V_O	Output voltage	1.4		34.0	V
C_{OUT}	Output capacitor	10			μ F
V_{EN}	Enable pin voltage	0		V_{IN}	V
I_O	Output current	0		1.0	A

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A47-Q1	UNIT
		RGW (VQFN)	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.1	$^{\circ}$ C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	21.1	$^{\circ}$ C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.2	$^{\circ}$ C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	$^{\circ}$ C/W
ψ_{JB}	Junction-to-board characterization parameter	10.2	$^{\circ}$ C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.9	$^{\circ}$ C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

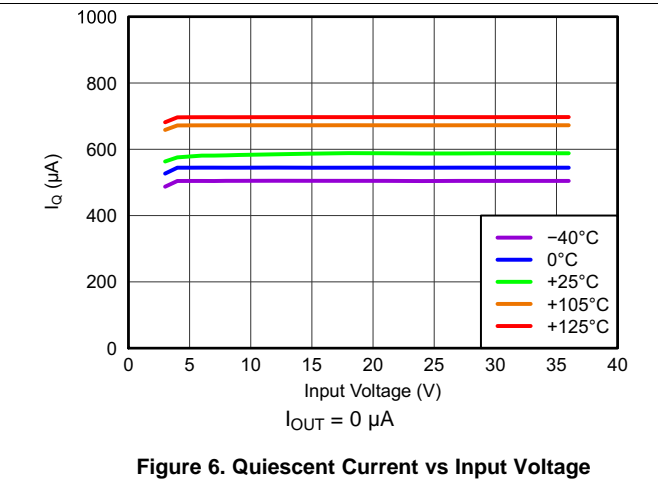
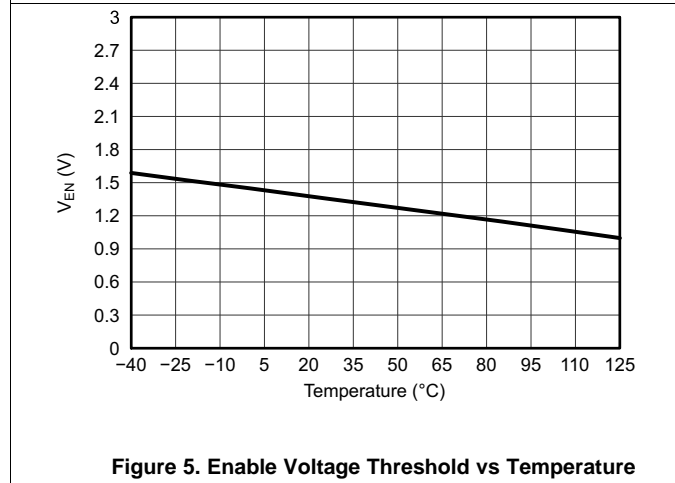
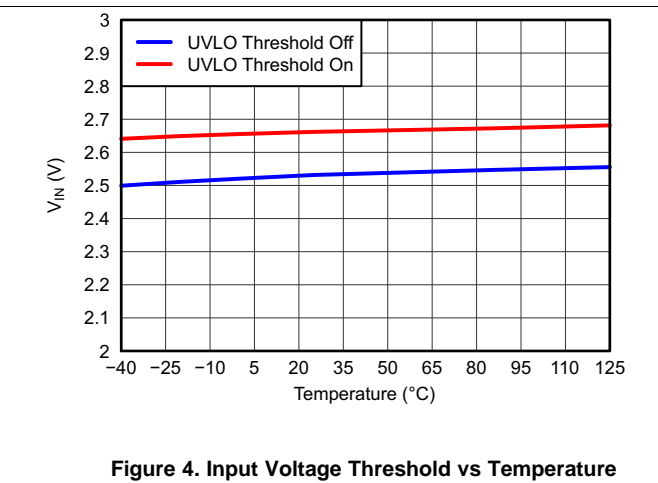
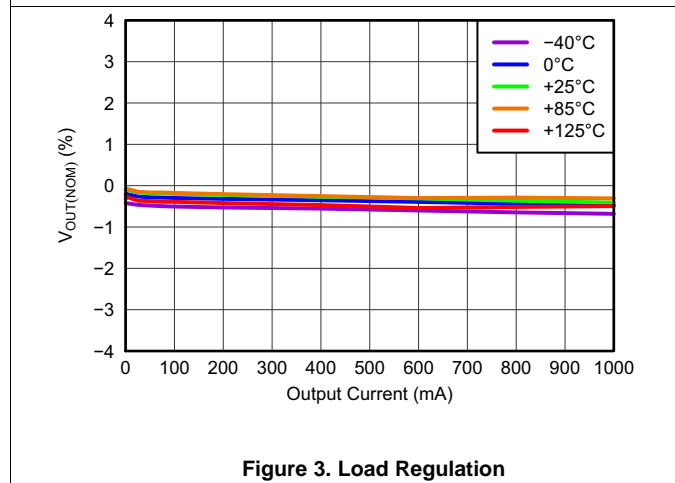
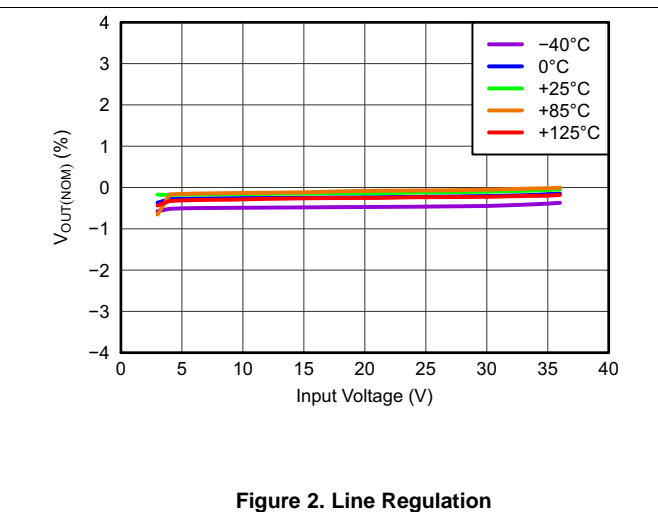
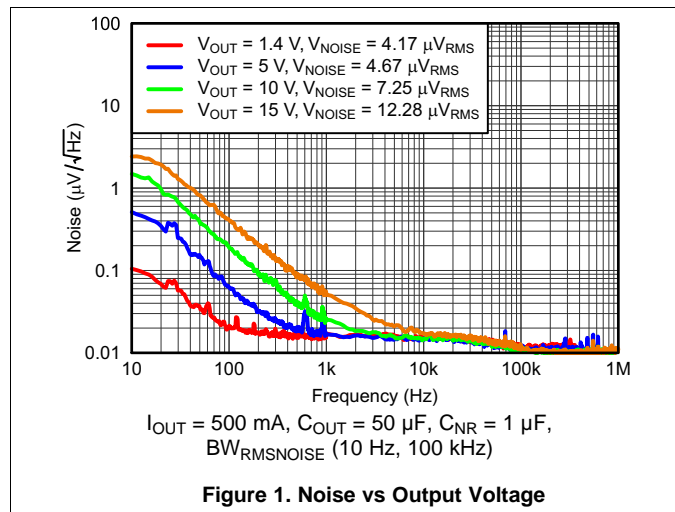
6.5 Electrical Characteristics

at $-40^{\circ}\text{C} \leq T_J \leq 145^{\circ}\text{C}$; $V_I = V_{O(\text{nom})} + 1.0\text{ V}$ or $V_I = 3.0\text{ V}$ (whichever is greater); $V_{\text{EN}} = V_I$; $I_O = 0\text{ mA}$; $C_{\text{IN}} = 10\text{ }\mu\text{F}$; $C_{\text{OUT}} = 10\text{ }\mu\text{F}$; $C_{\text{NR}} = 10\text{ nF}$; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins open (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_I	Input voltage range	3		35	V
V_{UVLO}	Undervoltage lockout threshold	V_I rising	2.67		V
		V_I falling	2.5		
$V_{(\text{REF})}$	Reference voltage	$V_{(\text{REF})} = V_{(\text{FB})}$			V
$V_{\text{UVLO}(\text{HYS})}$	Under-voltage lockout hysteresis		177		mV
V_{NR}	Noise reduction pin voltage	Using ANY-OUT option	V_{OUT}		V
		In adjustable mode only	1.4		
V_O	Output voltage range	$C_{\text{OUT}} = 20\text{ }\mu\text{F}$, using ANY-OUT option	1.4	20.5	V
		$C_{\text{OUT}} = 20\text{ }\mu\text{F}$, using adjustable option	1.4	34	
	Nominal V_O accuracy	$T_J = 25^{\circ}\text{C}$, $C_{\text{OUT}} = 20\text{ }\mu\text{F}$		1.0	$\%V_O$
	Overall V_O accuracy	$V_{O(\text{nom})} + 1.0\text{ V} \leq V_I \leq 35\text{ V}$, $0\text{ mA} \leq I_O \leq 1\text{ A}$, $C_{\text{OUT}} = 20\text{ }\mu\text{F}$		2.5	$\%V_O$
$\Delta V_{O(\Delta V_I)}$	Line regulation	$V_{O(\text{nom})} + 1.0\text{ V} \leq V_I \leq 35\text{ V}$		0.092	$\%V_O$
$\Delta V_{O(\Delta I_O)}$	Load regulation	$0\text{ mA} \leq I_O \leq 1\text{ A}$		0.3	$\%V_O$
$V_{(\text{DO})}$	Dropout voltage	$V_I = 95\% V_{O(\text{nom})}$, $I_O = 0.5\text{ A}$		216	mV
		$V_I = 95\% V_{O(\text{nom})}$, $I_O = 1\text{ A}$		307	
$I_{(\text{CL})}$	Current limit	$V_O = 90\% V_{O(\text{nom})}$		1	A
$I_{(\text{GND})}$	Ground pin current	$I_O = 0\text{ mA}$		0.58	mA
		$I_O = 1\text{ A}$		6.1	
$I_{(\text{EN})}$	Enable pin current	$V_{\text{EN}} = V_I$		0.78	μA
		$V_I = V_{\text{EN}} = 35\text{ V}$		0.81	
$I_{(\text{SHDN})}$	Shutdown supply current	$V_{\text{EN}} = 0.4\text{ V}$		2.55	μA
		$V_{\text{EN}} = 0.4\text{ V}$, $V_I = 35\text{ V}$		3.04	
$V_{+\text{EN}(\text{HI})}$	Enable high-level voltage	2.0		V_I	V
$V_{+\text{EN}(\text{LO})}$	Enable low-level voltage	0		0.4	V
$I_{(\text{FB})}$	Feedback pin current		350		nA
PSRR	Power-supply rejection ratio	$V_I = 16\text{ V}$, $V_{O(\text{nom})} = 15\text{ V}$, $C_{\text{OUT}} = 50\text{ }\mu\text{F}$, $I_O = 500\text{ mA}$, $C_{\text{NR}} = 1\text{ }\mu\text{F}$, $f = 1\text{ kHz}$		78	dB
V_n	Output noise voltage	$V_I = 3\text{ V}$, $V_{O(\text{nom})} = 1.4\text{ V}$, $C_{\text{OUT}} = 50\text{ }\mu\text{F}$, $C_{\text{NR}} = 1\text{ }\mu\text{F}$, $\text{BW} = 10\text{ Hz to }100\text{ kHz}$		4.17	μV_{RMS}
		$V_{\text{IN}} = 6\text{ V}$, $V_{O(\text{nom})} = 5\text{ V}$, $C_{\text{OUT}} = 50\text{ }\mu\text{F}$, $C_{\text{NR}} = 1\text{ }\mu\text{F}$, $\text{BW} = 10\text{ Hz to }100\text{ kHz}$		4.67	
T_{sd}	Thermal shutdown temperature	Shutdown, temperature increasing		170	$^{\circ}\text{C}$
		Reset, temperature decreasing		150	
T_J	Operating junction temperature	-40		145	$^{\circ}\text{C}$

6.6 Typical Characteristics

at $T_J = 25^\circ\text{C}$; $V_I = V_{O(\text{nom})} + 1.0\text{ V}$ or $V_I = 3.0\text{ V}$ (whichever is greater); $V_{\text{EN}} = V_I$; $I_O = 0\text{ mA}$; $C_{\text{IN}} = 10\text{ }\mu\text{F}$; $C_{\text{OUT}} = 10\text{ }\mu\text{F}$; $C_{\text{NR}} = 1\text{ }\mu\text{F}$; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins open (unless otherwise noted)



Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$; $V_I = V_{O(\text{nom})} + 1.0\text{ V}$ or $V_I = 3.0\text{ V}$ (whichever is greater); $V_{\text{EN}} = V_I$; $I_O = 0\text{ mA}$; $C_{\text{IN}} = 10\text{ }\mu\text{F}$; $C_{\text{OUT}} = 10\text{ }\mu\text{F}$; $C_{\text{NR}} = 1\text{ }\mu\text{F}$; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins open (unless otherwise noted)

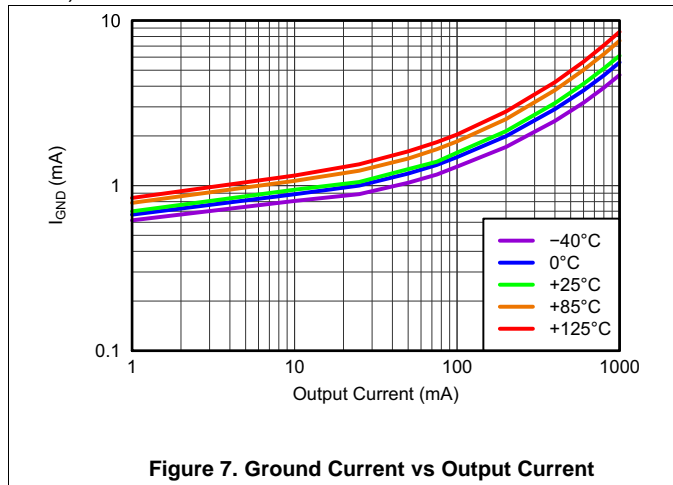


Figure 7. Ground Current vs Output Current

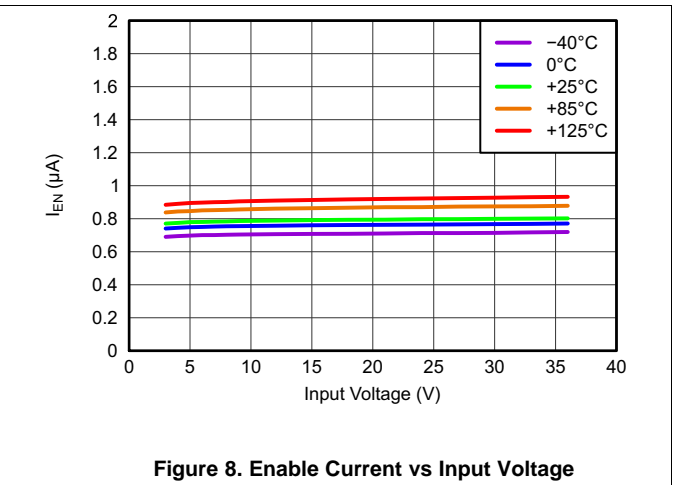


Figure 8. Enable Current vs Input Voltage

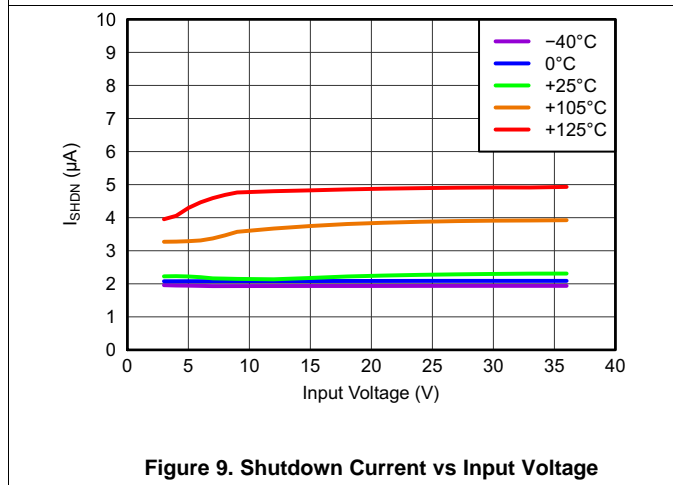


Figure 9. Shutdown Current vs Input Voltage

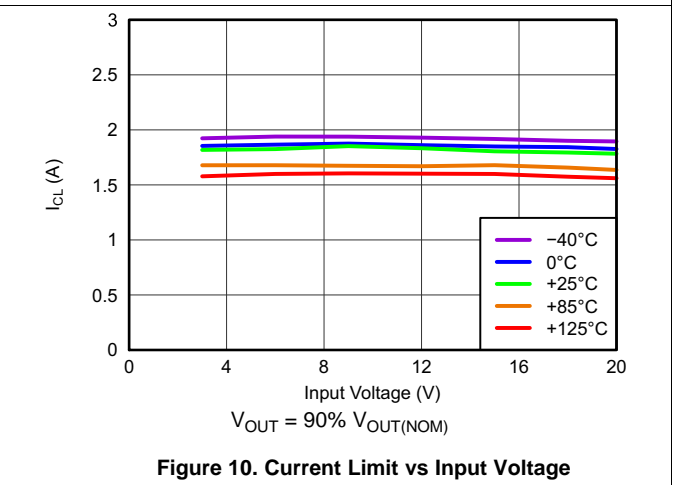


Figure 10. Current Limit vs Input Voltage

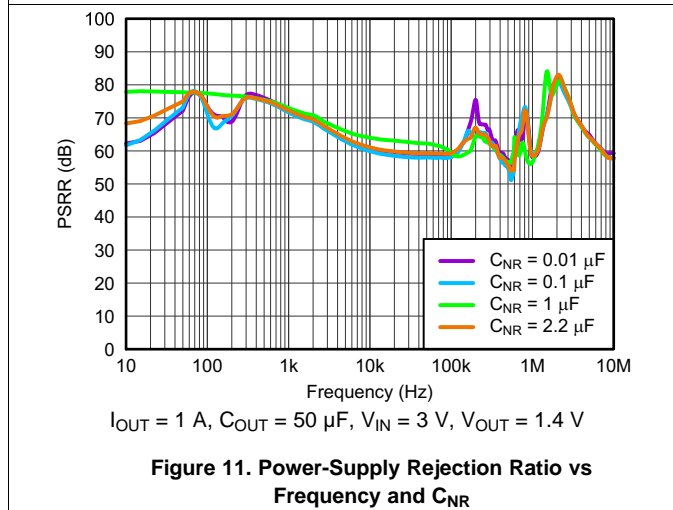


Figure 11. Power-Supply Rejection Ratio vs Frequency and C_{NR}

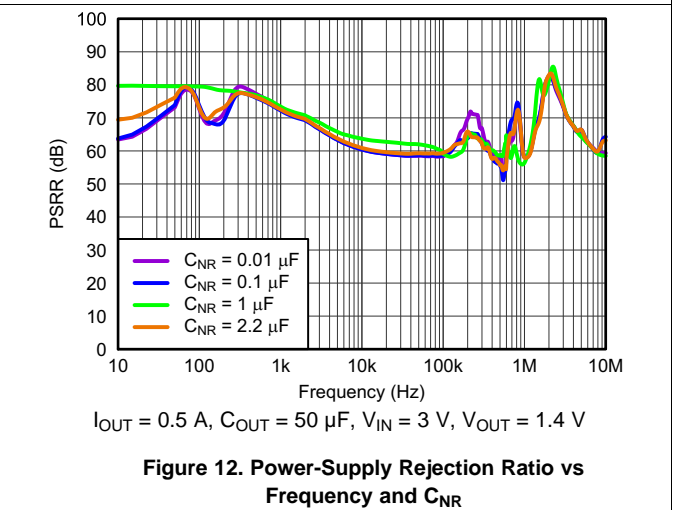
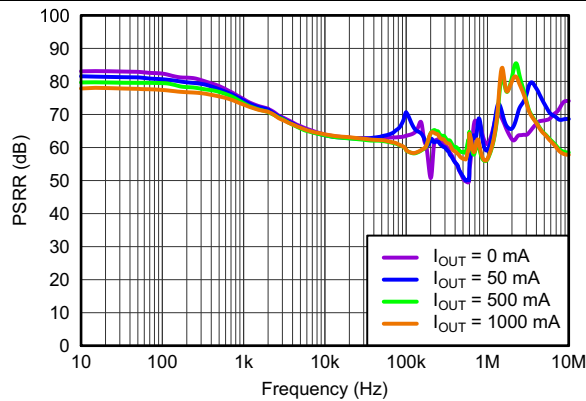


Figure 12. Power-Supply Rejection Ratio vs Frequency and C_{NR}

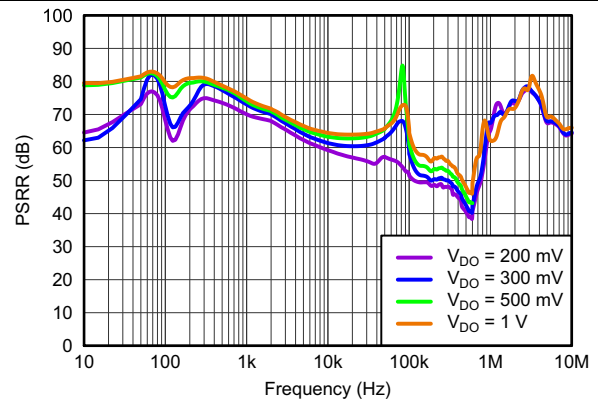
Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$; $V_I = V_{O(nom)} + 1.0\text{ V}$ or $V_I = 3.0\text{ V}$ (whichever is greater); $V_{EN} = V_I$; $I_O = 0\text{ mA}$; $C_{IN} = 10\text{ }\mu\text{F}$; $C_{OUT} = 10\text{ }\mu\text{F}$; $C_{NR} = 1\text{ }\mu\text{F}$; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins open (unless otherwise noted)



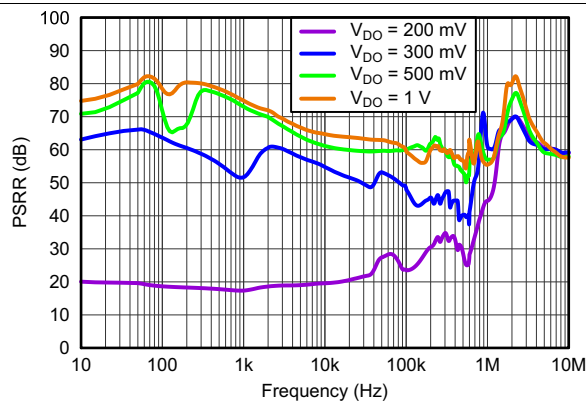
$C_{NR} = 1\text{ }\mu\text{F}$, $C_{OUT} = 50\text{ }\mu\text{F}$, $V_{IN} = 3\text{ V}$, $V_{OUT} = 1.4\text{ V}$

Figure 13. Power-Supply Rejection Ratio vs Frequency and I_O



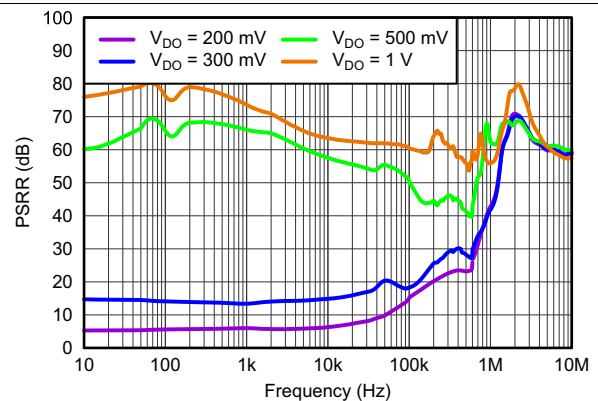
$V_{OUT} = 3.3\text{ V}$, $C_{NR} = 1\text{ }\mu\text{F}$, $C_{OUT} = 50\text{ }\mu\text{F}$, $I_{OUT} = 50\text{ mA}$

Figure 14. Power-Supply Rejection Ratio vs Frequency and V_{DO}



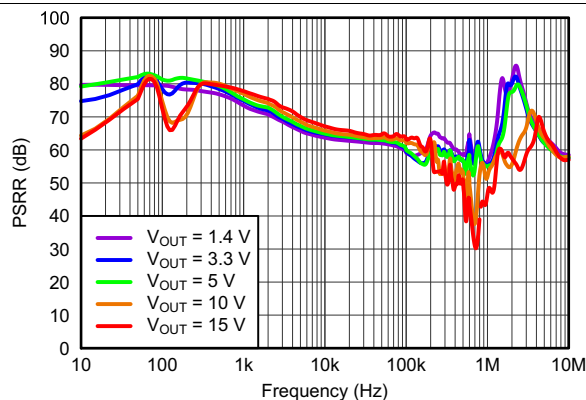
$V_{OUT} = 3.3\text{ V}$, $C_{NR} = 1\text{ }\mu\text{F}$, $C_{OUT} = 50\text{ }\mu\text{F}$, $I_{OUT} = 500\text{ mA}$

Figure 15. Power-Supply Rejection Ratio vs Frequency and V_{DO}



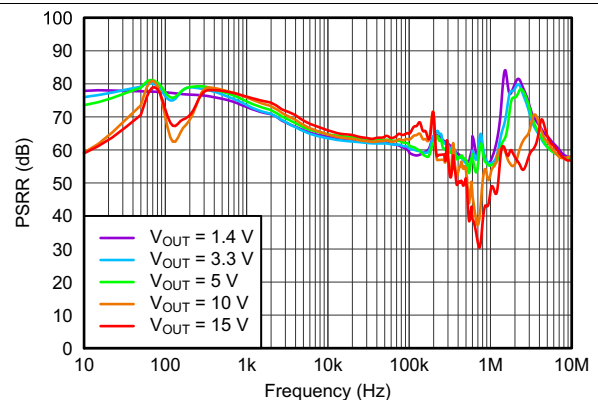
$V_{OUT} = 3.3\text{ V}$, $C_{NR} = 1\text{ }\mu\text{F}$, $C_{OUT} = 50\text{ }\mu\text{F}$, $I_{OUT} = 1\text{ A}$

Figure 16. Power-Supply Rejection Ratio vs Frequency and V_{DO}



$C_{NR} = 1\text{ }\mu\text{F}$, $C_{OUT} = 50\text{ }\mu\text{F}$, $I_{OUT} = 500\text{ mA}$

Figure 17. Power-Supply Rejection Ratio vs Frequency and V_{OUT}



$C_{NR} = 1\text{ }\mu\text{F}$, $C_{OUT} = 50\text{ }\mu\text{F}$, $I_{OUT} = 1000\text{ mA}$

Figure 18. Power-Supply Rejection Ratio vs Frequency and V_{OUT}

Typical Characteristics (continued)

at $T_J = 25^\circ\text{C}$; $V_I = V_{O(\text{nom})} + 1.0\text{ V}$ or $V_I = 3.0\text{ V}$ (whichever is greater); $V_{\text{EN}} = V_I$; $I_O = 0\text{ mA}$; $C_{\text{IN}} = 10\text{ }\mu\text{F}$; $C_{\text{OUT}} = 10\text{ }\mu\text{F}$; $C_{\text{NR}} = 1\text{ }\mu\text{F}$; SENSE/FB tied to OUT; and 0P1V, 0P2V, 0P4V, 0P8V, 1P6V, 3P2V, 6P4V1, 6P4V2 pins open (unless otherwise noted)

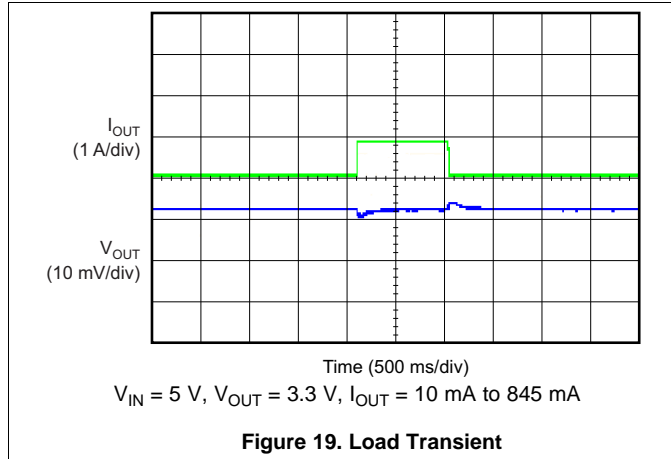


Figure 19. Load Transient

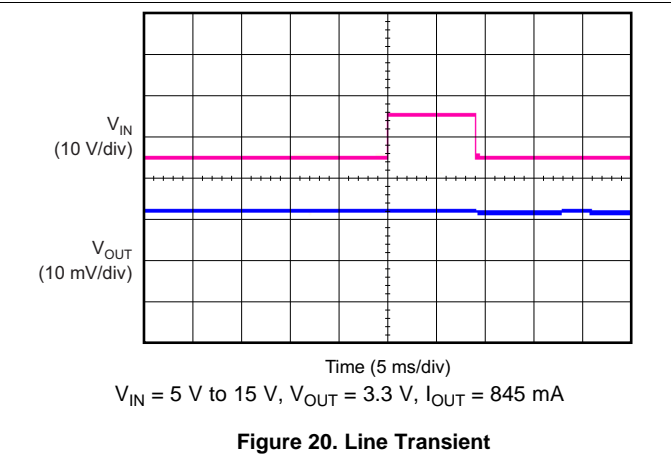


Figure 20. Line Transient

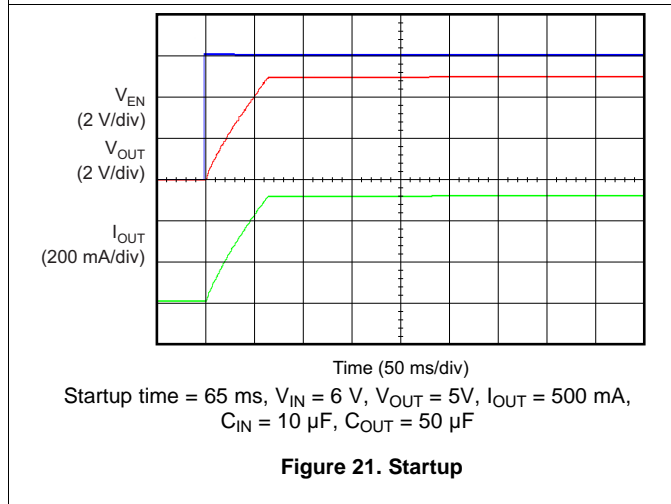


Figure 21. Startup

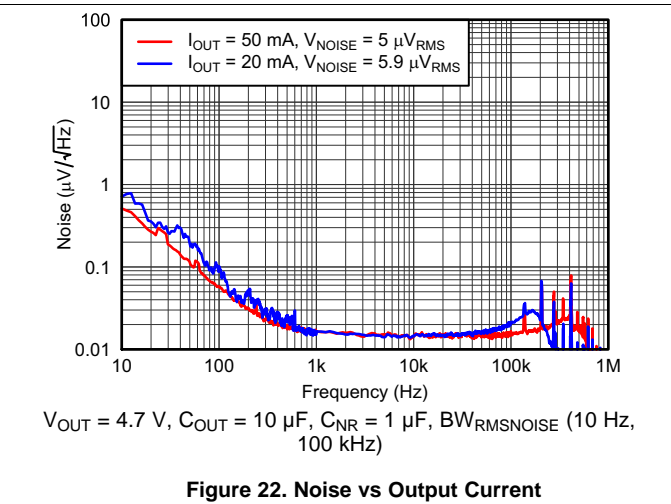


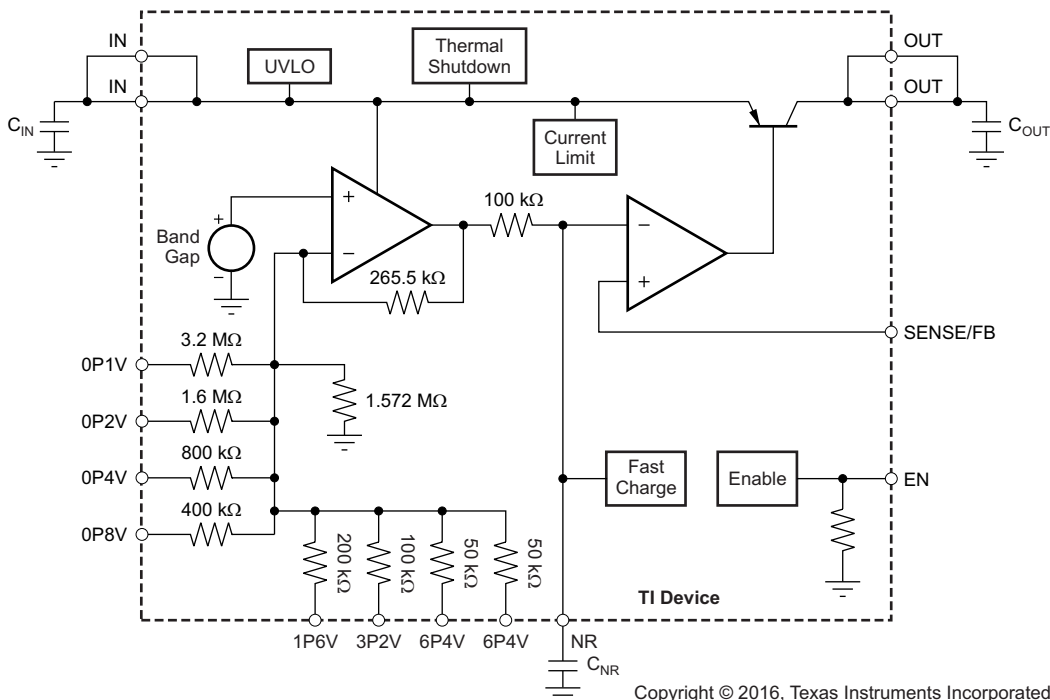
Figure 22. Noise vs Output Current

7 Detailed Description

7.1 Overview

The TPS7A47-Q1 is a positive voltage (35 V), ultralow-noise ($4.2 \mu\text{V}_{\text{RMS}}$) LDO capable of sourcing a 1-A load. The TPS7A47-Q1 is designed with bipolar technology primarily for high-accuracy, high-precision instrumentation applications where clean voltage rails are critical to maximize system performance. This feature makes the device ideal for powering operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other high-performance analog circuitry.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit (I_{CL})

The internal current limit circuit is used to protect the LDO against high-load current faults or shorting events. The LDO is not designed to operate at a steady-state current limit. During a current-limit event, the LDO sources constant current. Therefore, the output voltage falls when load impedance decreases. Also, when a current limit occurs while the resulting output voltage is low, excessive power is dissipated across the LDO, which results in a thermal shutdown of the output.

7.3.2 Enable (EN) And Undervoltage Lockout (UVLO)

The TPS7A47-Q1 only turns on when both EN and UVLO are above the respective voltage thresholds. The UVLO circuit monitors input voltage (V_I) to prevent device turn-on before V_I rises above the lockout voltage. The UVLO circuit also causes a shutdown when V_I falls below lockout. The EN signal allows independent logic-level turn-on and shutdown of the LDO when the input voltage is present. EN can be connected directly to V_I if independent turn-on is not needed.

Feature Description (continued)

7.3.3 Soft-Start And Inrush Current

Soft-start refers to the ramp-up characteristic of the output voltage during LDO turn-on after EN and UVLO have achieved the threshold voltage. The noise-reduction capacitor serves a dual purpose of both governing output noise reduction and programming the soft-start ramp during turn-on.

Inrush current is defined as the current through the LDO from IN to OUT during the time of the turn-on ramp up. Inrush current then consists primarily of the sum of load and charge current to the output capacitor. Use [Equation 1](#) to estimate in-rush current:

$$I_{OUT(t)} = \left[\frac{C_{OUT} \times dV_{OUT}(t)}{dt} \right] + \left[\frac{V_{OUT}(t)}{R_{LOAD}} \right]$$

where:

- $V_{OUT}(t)$ is the instantaneous output voltage of the turn-on ramp
 - $dV_{OUT}(t) / dt$ is the slope of the V_O ramp
 - R_{LOAD} is the resistive load impedance
- (1)

7.4 Device Functional Modes

The TPS7A47-Q1 has the following functional modes:

1. **Enabled:** when EN goes above $V_{+EN(HI)}$, the device is enabled.
2. **Disabled:** when EN goes below $V_{+EN(LO)}$, the device is disabled. During this time, OUT is high impedance, and the current into IN does not exceed $I_{(SHDN)}$.

7.5 Programming

7.5.1 ANY-OUT Programmable Output Voltage

For ANY-OUT operation, do not use external resistors to set the output voltage, but use device pins 4, 5, 6, 8, 9, 10, 11, and 12 to program the regulated output voltage. Each pin is either connected to ground (active) or is left open (floating). The ANY-OUT programming is set by [Equation 2](#) as the sum of the internal reference voltage ($V_{REF} = 1.4$ V) plus the accumulated sum of the respective voltages assigned to each active pin; that is, 100 mV (pin 12), 200 mV (pin 11), 400 mV (pin 10), 800 mV (pin 9), 1.6 V (pin 8), 3.2 V (pin 6), 6.4 V (pin 5), or 6.4 V (pin 4). [Table 1](#) summarizes these voltage values associated with each active pin setting for reference. By leaving all program pins open, or floating, the output is thereby programmed to the minimum possible output voltage equal to V_{REF} .

$$V_{OUT} = V_{REF} + (\Sigma \text{ ANY-OUT Pins to Ground})$$
(2)

Table 1. ANY-OUT Programmable Output Voltage

ANY-OUT PROGRAM PINS (Active Low)	ADDITIVE OUTPUT VOLTAGE LEVEL
Pin 4 (6P4V2)	6.4 V
Pin 5 (6P4V1)	6.4 V
Pin 6 (3P2)	3.2 V
Pin 8 (1P6)	1.6 V
Pin 9 (0P8)	800 mV
Pin 10 (0P4)	400 mV
Pin 11 (0P2)	200 mV
Pin 12 (0P1)	100 mV

Table 2 shows a list of the most common output voltages and the corresponding pin settings. The voltage setting pins have a binary weight; therefore, the output voltage can be programmed to any value from 1.4 V to 20.5 V in 100-mV steps.

Table 2. Common Output Voltages and Corresponding Pin Settings

V _O (V)	PIN NAMES AND VOLTAGE PER PIN							
	0P1V (100 mV)	0P2V (200 mV)	0P4V (400 mV)	0P8V (800 mV)	1P6V (1.6 V)	3P2V (3.2 V)	6P4V1 (6.4 V)	6P4V2 (6.4 V)
1.4	Open	Open	Open	Open	Open	Open	Open	Open
1.5	GND	Open	Open	Open	Open	Open	Open	Open
1.8	Open	Open	GND	Open	Open	Open	Open	Open
2.5	GND	GND	Open	GND	Open	Open	Open	Open
3	Open	Open	Open	Open	GND	Open	Open	Open
3.3	GND	GND	Open	Open	GND	Open	Open	Open
4.5	GND	GND	GND	GND	GND	Open	Open	Open
5	Open	Open	GND	Open	Open	GND	Open	Open
10	Open	GND	GND	Open	GND	Open	GND	Open
12	Open	GND	Open	GND	Open	GND	GND	Open
15	Open	Open	Open	GND	Open	Open	GND	GND
18	Open	GND	GND	Open	Open	GND	GND	GND
20.5	GND	GND	GND	GND	GND	GND	GND	GND

7.5.2 Adjustable Operation

The TPS7A47-Q1 has an output voltage range of 1.4 V to 34 V. For adjustable operation, set the nominal output voltage of the device (as shown in Figure 23) using two external resistors.

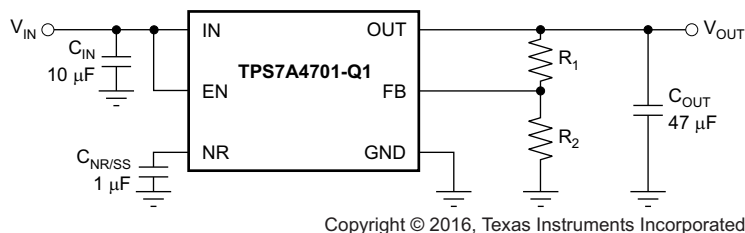


Figure 23. Adjustable Operation for Maximum AC Performance

R₁ and R₂ can be calculated for any output voltage within the operational range. The current through feedback resistor R₂ must be at least 5 µA to ensure stability. Additionally, the current into the FB pin (I_(FB), typically 350 nA) creates an additional output voltage offset that depends on the resistance of R₁. For high-accuracy applications, select R₂ such that the current through R₂ is at least 35 µA to minimize any effects of I_(FB) variation on the output voltage; 10 kΩ is recommended. Equation 3 calculates R₁.

$$R_1 = \frac{V_{OUT} - V_{REF}}{I_{FB} + \frac{V_{REF}}{R_2}}$$

where

- V_{REF} = 1.4 V
- I_{FB} = 350 nA

(3)

Use 0.1% tolerance resistors to minimize the effects of resistor inaccuracy on the output voltage.

Table 3 shows the resistor combinations to achieve some standard rail voltages with commercially available 1% tolerance resistors. The resulting output voltages yield a nominal error of < 0.5%.

Table 3. Suggested Resistors for Common Voltage Rails

V _{OUT}	R ₁ , CALCULATED	R ₁ , CLOSEST 1% VALUE	R ₂
1.4 V	0 Ω	0 Ω	∞
1.8 V	2.782 kΩ	2.8 kΩ	9.76 kΩ
3.3 V	13.213 kΩ	13.3 kΩ	9.76 kΩ
5 V	25.650 kΩ	25.5 kΩ	10 kΩ
12 V	77.032 kΩ	76.8 kΩ	10.2 kΩ
15 V	101.733 kΩ	102 kΩ	10.5 kΩ
18 V	118.276 kΩ	118 kΩ	10 kΩ
24 V	164.238 kΩ	165 kΩ	10.2 kΩ

To achieve higher nominal accuracy, two resistors can be used in the place of R₁. Select the two resistor values such that the sum results in a value as close as possible to the calculated R₁ value.

There are several alternative ways to set the output voltage. The program pins can be pulled low using external general-purpose input/output pins (GPIOs), or can be hardwired by the given layout of the printed circuit board (PCB) to set the ANY-OUT voltage. The [TPS7A4701 evaluation module \(EVM\)](#), available for purchase from [the TI eStore](#), allows the output voltage to be programmed using jumpers.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A47-Q1 is a high-voltage, low-noise, 1-A LDO. Low-noise performance makes this LDO ideal for providing rail voltages to noise-sensitive loads, such as PLLs, oscillators, and high-speed ADCs.

8.2 Typical Application

As shown in Figure 24, output voltage is set by grounding the appropriate control pins. When grounded, all control pins add a specific voltage on top of the internal reference voltage ($V_{REF} = 1.4\text{ V}$). For example, when grounding pins 0P1V, 0P2V, and 1P6V, the voltage values 0.1 V, 0.2 V, and 1.6 V are added to the 1.4-V internal reference voltage for $V_{O(nom)}$ equal to 3.3 V, as described in the [Programming](#) section.

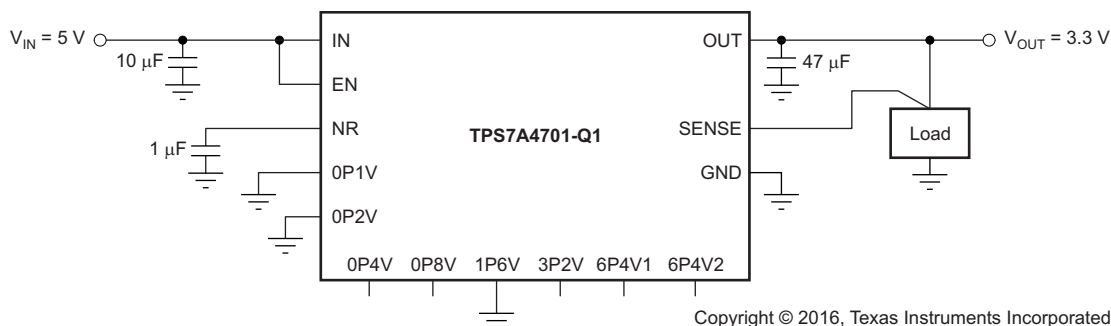


Figure 24. Typical Application, $V_{OUT} = 3.3\text{ V}$

8.2.1 Design Requirements

PARAMETER	DESIGN REQUIREMENT
Input voltage	5.0 V, $\pm 10\%$
Output voltage	3.3 V, $\pm 3\%$
Output current	500 mA
Peak-to-peak noise, 10 Hz to 100 kHz	50 μV_{PP}

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitor Recommendations

This LDO is designed to be stable using low equivalent series resistance (ESR), ceramic capacitors at the input, output, and at the noise-reduction pin (NR, pin 14). Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended here, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature, but the use of Y5V-rated capacitors is discouraged precisely because the capacitance varies so widely. In all cases, ceramic capacitance varies a great deal with operating voltage and the design engineer must be aware of these characteristics. TI recommends applying a 50% derating of the nominal capacitance in the design.

Attention must be given to the input capacitance to minimize transient input droop during load current steps because the TPS7A47-Q1 has a very fast load transient response. Large input capacitors are necessary for good transient load response, and have no detrimental influence on the stability of the device. However, using large ceramic input capacitances can also cause unwanted ringing at the output if the input capacitor, in combination with the wire lead inductance, creates a high-Q peaking effect during transients. For example, a 5-nH lead inductance and a 10- μ F input capacitor form an LC filter with a resonance frequency of 712 kHz at the edge of the control loop bandwidth. Short, well-designed interconnect leads to the up-stream supply minimize this effect without adding damping. Damping of unwanted ringing can be accomplished by using a tantalum capacitor, with a few hundred milliohms of ESR, in parallel with the ceramic input capacitor.

8.2.2.1.1 Input and Output Capacitor Requirements

The TPS7A47-Q1 is designed and characterized for operation with ceramic capacitors of 10 μ F or greater at the input and output. Optimal noise performance is characterized using a total output capacitor value of 50 μ F. Input and output capacitances must be located as near as practical to the respective input and output pins.

8.2.2.1.2 Noise-Reduction Capacitor (C_{NR})

The noise-reduction capacitor, connected to the NR pin of the LDO, forms an RC filter for filtering out noise that might ordinarily be amplified by the control loop and appear on the output voltage. Larger capacitances, up to 1 μ F, affect noise reduction at lower frequencies and also tend to further reduce noise at higher frequencies. C_{NR} also serves a secondary purpose in programming the turn-on rise time of the output voltage and thereby controls the turn-on surge current.

8.2.2.2 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the voltage difference between the input and output voltage ($V_{(DO)} = V_I - V_O$). However, in the [Electrical Characteristics](#) $V_{(DO)}$ is defined as the $V_I - V_O$ voltage at the rated current ($I_{(RATED)}$), where the main current pass-FET is fully on in the Ohmic region of operation and is characterized by the classic $R_{DS(on)}$ of the FET. $V_{(DO)}$ indirectly specifies a minimum input voltage above the nominal programmed output voltage at which the output voltage is expected to remain within its accuracy boundary. If the input falls below this $V_{(DO)}$ limit ($V_I < V_O + V_{(DO)}$), then the output voltage decreases in order to follow the input voltage.

Dropout voltage is always determined by the $R_{DS(on)}$ of the main pass-FET. Therefore, if the LDO operates below the rated current, then $V_{(DO)}$ is directly proportional to the output current and can be reduced by the same factor. Use [Equation 4](#) to calculate $R_{DS(on)}$ for the TPS7A47-Q1:

$$R_{DS(ON)} = \frac{V_{DO}}{I_{RATED}} \quad (4)$$

8.2.2.3 Output Voltage Accuracy

The output voltage accuracy specifies minimum and maximum output voltage error, relative to the expected nominal output voltage stated as a percent. This accuracy error typically includes the errors introduced by the internal reference and the load and line regulation across the full range of rated load and line operating conditions over temperature, unless otherwise specified by the [Electrical Characteristics](#). Output voltage accuracy also accounts for all variations between manufacturing lots.

8.2.2.4 Startup

The startup time for the TPS7A47-Q1 depends on the output voltage and the capacitance of the C_{NR} capacitor. [Equation 5](#) calculates the startup time for a typical device.

$$t_{SS} = 100,000 \cdot C_{NR} \cdot \ln\left(\frac{V_R + 5}{5}\right)$$

where

- C_{NR} = capacitance of the C_{NR} capacitor
 - $V_R = V_O$ voltage if using the ANY-OUT configuration, or 1.4 V if using the adjustable configuration
- (5)

8.2.2.5 AC Performance

AC performance of the LDO is typically understood to include power-supply rejection ratio, load step transient response, and output noise. These metrics are primarily a function of open-loop gain and bandwidth, phase margin, and reference noise.

8.2.2.5.1 Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of how well the LDO control loop rejects ripple noise from the input source to make the dc output voltage as noise-free as possible across the frequency spectrum (usually 10 Hz to 10 MHz). Equation 6 gives the PSRR calculation as a function of frequency where input noise voltage $[V_{S(IN)}(f)]$ and output noise voltage $[V_{S(OUT)}(f)]$ are understood to be purely ac signals.

$$\text{PSRR (dB)} = 20 \text{ Log}_{10} \left[\frac{V_{S(IN)}(f)}{V_{S(OUT)}(f)} \right] \quad (6)$$

Noise that couples from the input to the internal reference voltage for the control loop is also a primary contributor to reduced PSRR magnitude and bandwidth. This reference noise is greatly filtered by the noise-reduction capacitor at the NR pin of the LDO in combination with an internal filter resistor (R_{SS}) for optimal PSRR.

The LDO is often employed not only as a dc/dc regulator, but also to provide exceptionally clean power-supply voltages that are free of noise and ripple to power-sensitive system components. This usage is especially true for the TPS7A47-Q1.

8.2.2.5.2 Load Step Transient Response

The load step transient response is the output voltage response by the LDO to a step change in load current whereby output voltage regulation is maintained. The worst-case response is characterized for a load step of 10 mA to 1 A (at 1 A per microsecond) and shows a classic, critically-damped response of a very stable system. The voltage response shows a small dip in the output voltage when charge is initially depleted from the output capacitor and then the output recovers as the control loop adjusts itself. The depth of the charge depletion immediately after the load step is directly proportional to the amount of output capacitance. However, to some extent, the speed of recovery is inversely proportional to that same output capacitance. In other words, larger output capacitances act to decrease any voltage dip or peak occurring during a load step but also decrease the control-loop bandwidth, thereby slowing response.

The worst-case, off-loading step characterization occurs when the current step transitions from 1 A to 0 mA. Initially, the LDO loop cannot respond fast enough to prevent a small increase in output voltage charge on the output capacitor. Because the LDO cannot sink charge current, the control loop must turn off the main pass-FET to wait for the charge to deplete, thus giving the off-load step its typical monotonic decay (which appears triangular in shape).

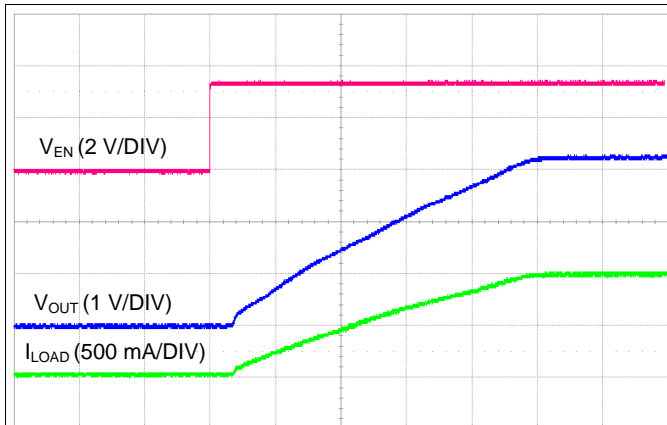
8.2.2.5.3 Noise

The TPS7A47-Q1 is designed, in particular, for system applications where minimizing noise on the power-supply rail is critical to system performance. This scenario is the case for phase-locked loop (PLL)-based clocking circuits for instance, where minimum phase noise is all important, or in-test and measurement systems where even small power-supply noise fluctuations can distort instantaneous measurement accuracy. Because the TPS7A47-Q1 is also designed for higher voltage industrial applications, the noise characteristic is well designed to minimize any increase as a function of the output voltage.

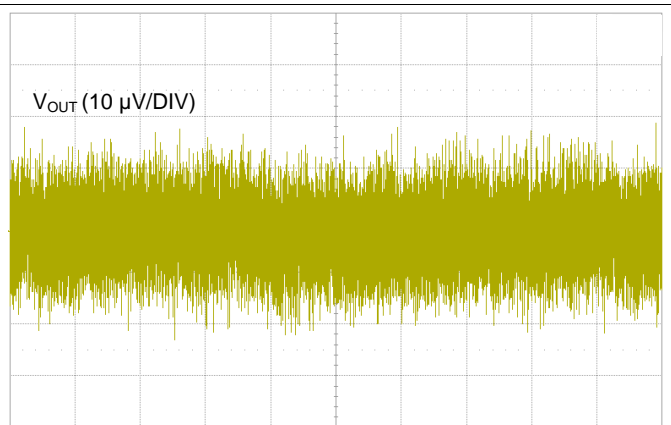
LDO noise is defined as the internally-generated intrinsic noise created by the semiconductor circuits alone. This noise is the sum of various types of noise (such as shot noise associated with current-through-pin junctions, thermal noise caused by thermal agitation of charge carriers, flicker or 1/f noise that is a property of resistors and dominates at lower frequencies as a function of 1/f, burst noise, and avalanche noise).

To calculate the LDO RMS output noise, a spectrum analyzer must first measure the spectral noise across the bandwidth of choice (typically 10 Hz to 100 kHz in units of $\mu\text{V}/\sqrt{\text{Hz}}$). The RMS noise is then calculated in the usual manner as the integrated square root of the squared spectral noise over the band, then averaged by the bandwidth.

8.2.3 Application Curves



**Figure 25. Startup With EN Pin Rising
(10 ms per Division)**



**Figure 26. Output Noise Voltage, 10 Hz to 100 kHz
(10 ms per Division)**

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range of 3 V to 35 V. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

9.1 Power Dissipation (P_D)

Power dissipation must be considered in the PCB design. In order to minimize risk of device operation above 145°C, use as much copper area as available for thermal dissipation. Do not locate other power-dissipating devices near the LDO.

Power dissipation in the regulator depends on the input to output voltage difference and load conditions. Equation 7 calculates P_D :

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \quad (7)$$

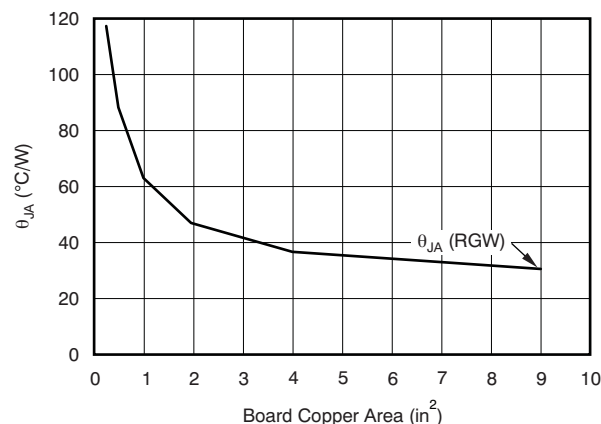
Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input voltage necessary for output regulation to be obtained.

The primary heat conduction path for the VQFN (RGW) package is through the PowerPAD to the PCB. The PowerPAD must be soldered to a copper pad area under the device. Thermal vias are recommended to improve the thermal conduction to other layers of the PCB.

The maximum power dissipation determines the maximum allowable junction temperature (T_J) for the device. According to Equation 8, power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance (θ_{JA}) of the combined PCB and device package and the temperature of the ambient air (T_A).

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (8)$$

Unfortunately, this thermal resistance (θ_{JA}) depends primarily on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the spreading planes. The θ_{JA} recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout, θ_{JA} is actually the sum of the VQFN package junction-to-case (bottom) thermal resistance (θ_{JCbot}) plus the thermal resistance contribution by the PCB copper. By knowing θ_{JCbot} , the minimum amount of appropriate heat sinking can be used with Figure 27 to estimate θ_{JA} . θ_{JCbot} can be found in the *Thermal Information* table.



NOTE: θ_{JA} value at a board size of 9-in² (that is, 3-in x 3-in) is a JEDEC standard.

Figure 27. θ_{JA} vs Board Size

10 Layout

10.1 Layout Guidelines

For best overall performance, all circuit components are recommended to be located on the same side of the circuit board and as near as practical to the respective LDO pin connections. Ground return connections to the input and output capacitor, and to the LDO ground pin, must also be as close to each other as possible and connected by a wide, component-side, copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes inductive parasitics and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

A ground reference plane is also recommended. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the PowerPAD. In most applications, this ground plane is necessary to meet thermal requirements.

Use the [TPS7A4701 evaluation module \(EVM\)](#), available for purchase from [the TI eStore](#), as a reference for layout and application design.

10.2 Layout Example

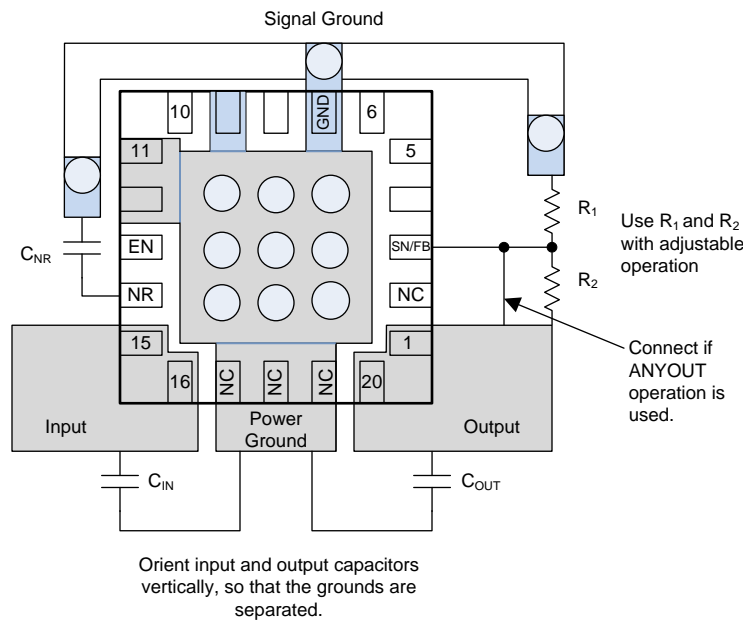


Figure 28. Layout Example

10.3 Thermal Protection

The TPS7A47-Q1 contains a thermal shutdown protection circuit to turn off the output current when excessive heat is dissipated in the LDO. Thermal shutdown occurs when the thermal junction temperature (T_J) of the main pass-FET exceeds 170°C (typical). Thermal shutdown hysteresis assures that the LDO again resets (turns on) when the temperature falls to 145°C (typical). Because the TPS7A47-Q1 is capable of supporting high input voltages, a great deal of power can be expected to be dissipated across the device at low output voltages, which causes a thermal shutdown. The thermal time-constant of the semiconductor die is fairly short, and thus the output oscillates on and off at a high rate when thermal shutdown is reached until power dissipation is reduced.

For reliable operation, the junction temperature must be limited to a maximum of 145°C. To estimate the thermal margin in a given layout, increase the ambient temperature until the thermal protection shutdown is triggered using worst-case load and highest input voltage conditions. For good reliability, thermal shutdown must be designed to occur at least 45°C above the maximum expected ambient temperature condition for the application. This configuration produces a worst-case junction temperature of 145°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A47-Q1 is designed to protect against thermal overload conditions. The circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A47-Q1 into thermal shutdown degrades device reliability.

10.4 Estimating Junction Temperature

JEDEC standards recommend the use of PSI thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These PSI metrics are determined to be significantly independent of copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are given in the [Thermal Information](#) table and are used in accordance with [Equation 9](#).

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- P_D is the power dissipated as explained in [Equation 7](#)
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge (9)

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『TPS7A33 -36V, 1A, 超低ノイズの負の電圧レギュレータ』
- 『TPS7A47XXEVM-094 評価モジュール・ユーザー・ガイド』
- 『低ドロップアウト・レギュレータでフィードフォワード・コンデンサを使用することの長所と短所』

11.2 ドキュメントの更新通知を受け取る方法

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11.3 コミュニティ・リソース

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11.4 商標

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11.5 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4701QRGWRQ1	ACTIVE	VQFN	RGW	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A4701Q	Samples
TPS7A4701QRGWTQ1	ACTIVE	VQFN	RGW	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A4701Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4701QRGWRQ1	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TPS7A4701QRGWTQ1	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4701QRGWRQ1	VQFN	RGW	20	3000	346.0	346.0	33.0
TPS7A4701QRGWTQ1	VQFN	RGW	20	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

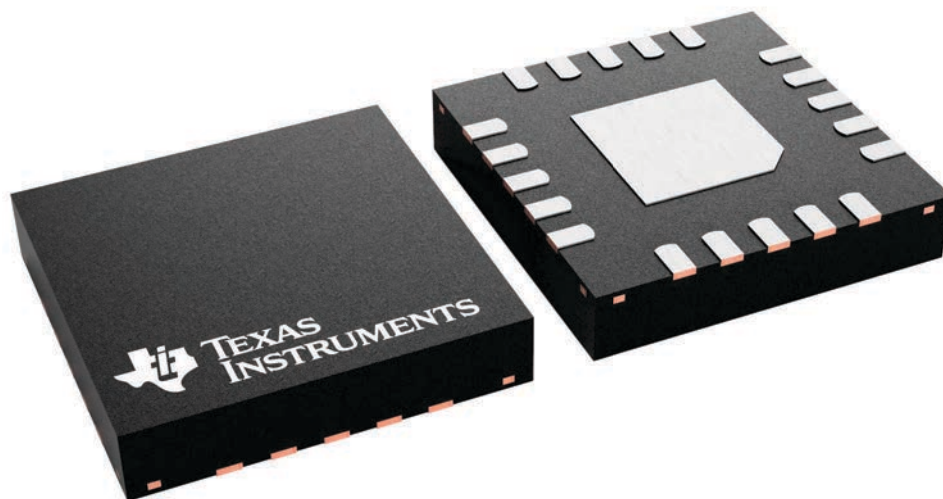
RGW 20

VQFN - 1 mm max height

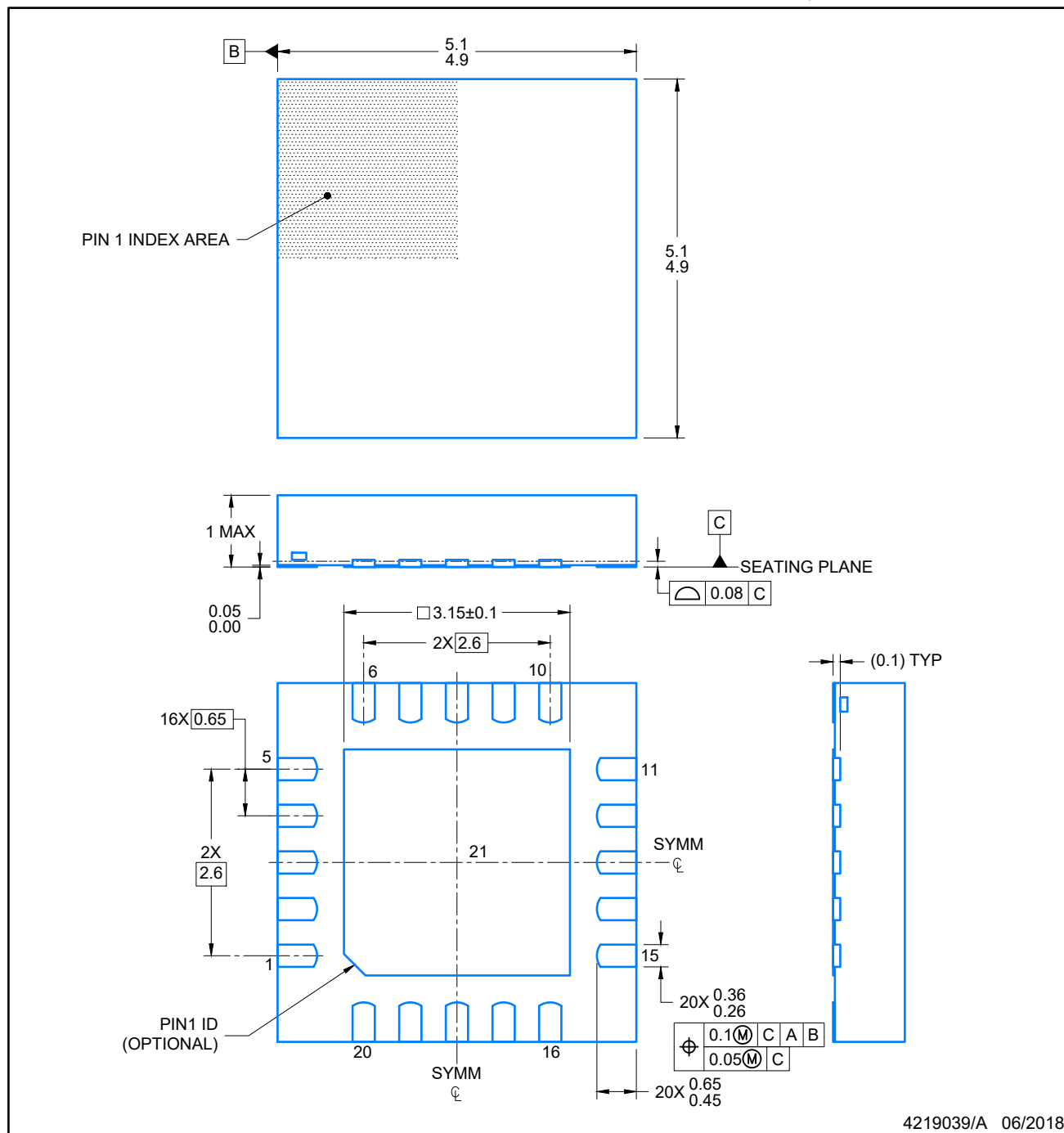
5 x 5, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

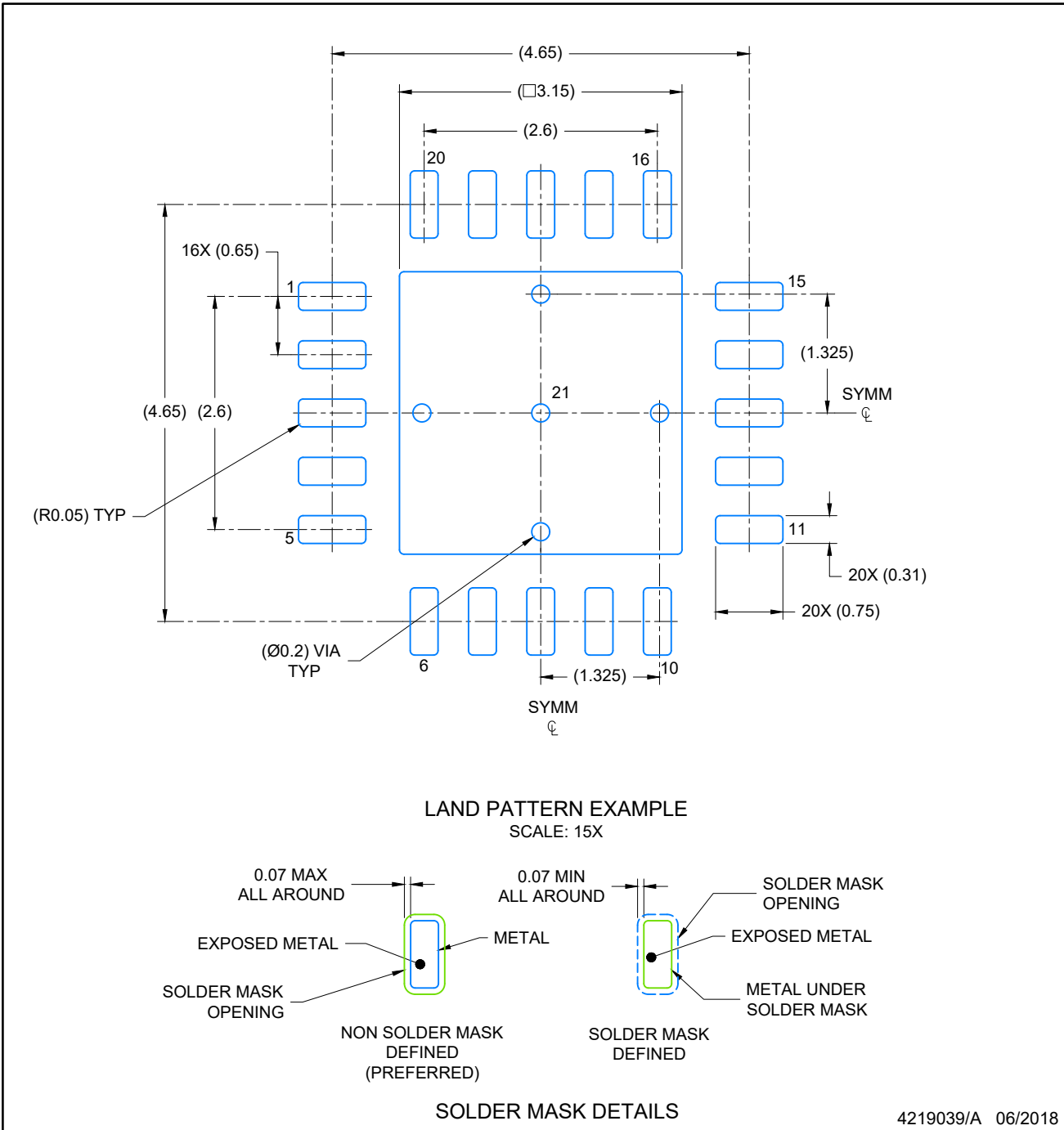


4227157/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



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NOTES: (continued)

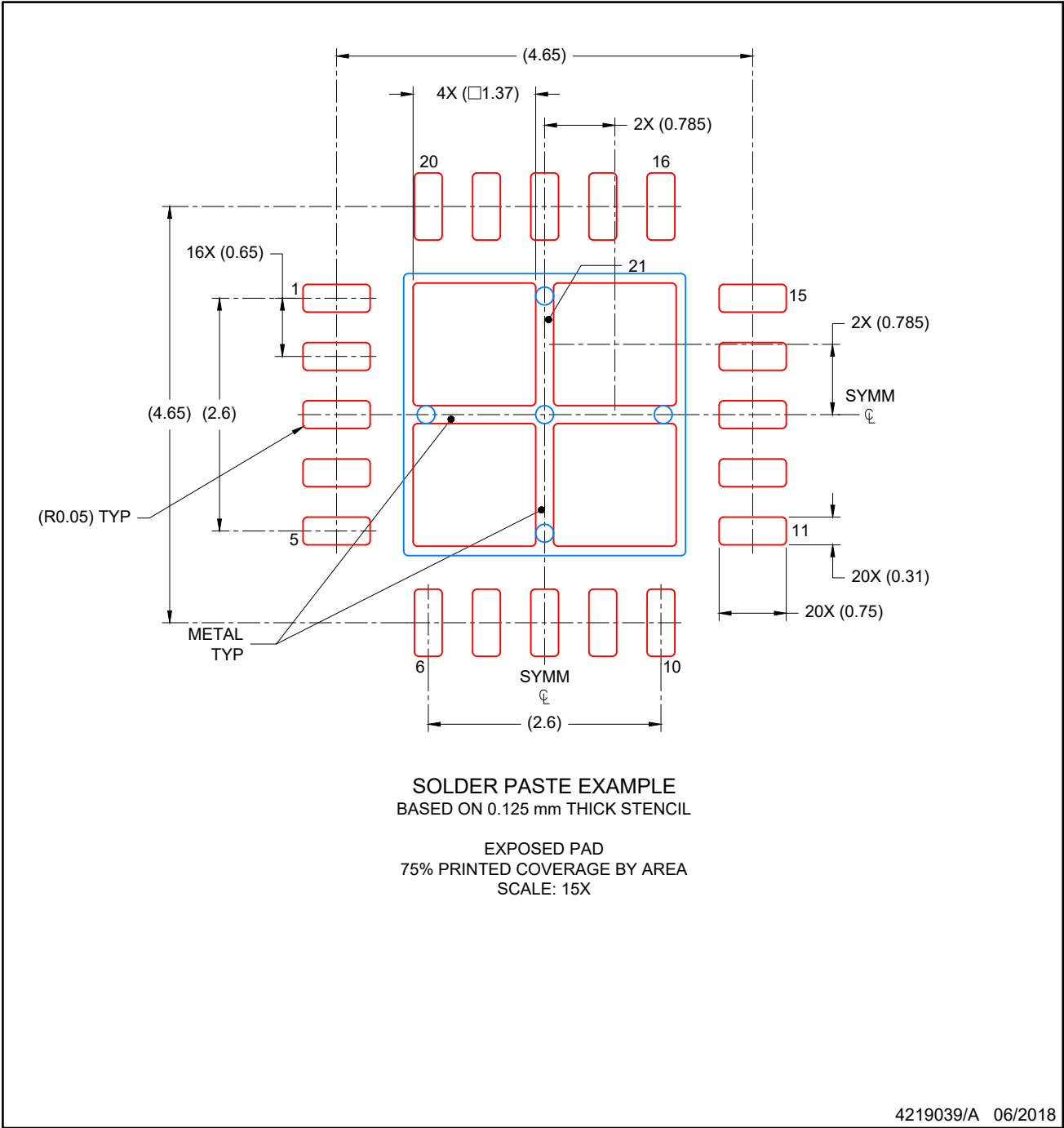
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGW0020A

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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