

## TPS65919-Q1 プロセッサ用電力管理ユニット(PMU)

### 1 デバイスの概要

#### 1.1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み:
  - デバイス温度グレード 2: 動作時周囲温度範囲  
–40°C~+105°C
  - デバイスHBM分類レベル2
  - デバイスCDM分類レベルC4B
- システム電圧範囲: 3.135V~5.25V
- 低消費電力
  - オフ・モードで20µA
  - 2つのSMPSがアクティブなスリープ・モードで90µA
- 4つの降圧型スイッチ・モード電源(SMPS)レギュレータ
  - 出力範囲0.7~3.3V、10または20mVステップ
  - 3.5Aの能力を持つ2つのSMPSレギュレータ、デュアル・フェーズ構成での組み合わせにより7Aを出力可能、差動リモート・センシング付き(出力およびグラウンド)
  - 3Aおよび1.5Aの能力を持つ、他の2つのSMPSレギュレータ
  - 3.5Aおよび3AのSMPSレギュレータでの、動的電圧スケールリング(DVS)制御および出力電流測定
  - ハードウェアおよびソフトウェア制御の Eco-mode™により最大5mAを供給
  - 短絡保護
  - パワー・グッド通知(電圧および過電流の通知)
  - 内部ソフトスタートによる突入電流の制限
  - 1.7MHz~2.7MHzの外部クロックと同期可能
- 4つの低ドロップアウト(LDO)リニア・レギュレータ
  - 50mVステップで0.9~3.3Vの出力範囲
  - 2つは300mVの能力とバイパス・モード付き
  - 1つは100mAの能力を持ち、50mAまでの低ノイズ性能
  - 他の1つのLDOは200mAの電流能力
  - 短絡保護
- 8つの入力チャンネル(外部2つ)を持つ12ビットのシグマ・デルタ汎用ADC (GPADC)
- 温度監視と高温警告およびサーマル・シャットダウン
- 電力シーケンス制御:
  - パワーアップおよびパワーダウンのシーケンスを構成可能(OTP)
  - SLEEPとACTIVEの間の状態遷移シーケンスを構成可能(OTP)
  - 3つのデジタル出力信号をスタートアップ・シーケンスに含めることが可能
- 制御インターフェイスを選択可能:
  - リソース構成およびDVS制御用の1つのSPI
  - 2つのI<sup>2</sup>Cインターフェイス:
    - DVS制御専用x1
    - リソース構成およびDVS制御用の汎用I<sup>2</sup>Cインターフェイスx1
- OTPビット整合性エラー検出、電源オン・シーケンスおよびRESET\_OUT解除の続行/保留オプション付き
- パッケージ・オプション
  - 7mmx7mmの48ピン、0.5mmピッチ

#### 1.2 アプリケーション

- 車載用デジタル・クラスタ
- 車載用ナビゲーション・システム
- 車載用先進運転支援システム(ADAS)

#### 1.3 概要

TPS65919-Q1 PMICには4つの構成可能な降圧型コンバータが内蔵され、プロセッサ・コア、メモリ、I/O、LDOのプリレギュレーションに最大3.5Aの出力電流を供給できます。このデバイスはAEC-Q100認定済みです。降圧型コンバータは内部の2.2MHzクロックに同期しているため、デバイスのEMC性能が向上しています。GPIO\_3ピンにより、降圧型コンバータは外部クロックと同期でき、複数のデバイスを同じクロックと同期させることで、システム・レベルのEMC性能が向上します。このデバイスには、低電流または低ノイズのドメインに電力を供給する、4つのLDOも搭載されています。

電源シーケンス・コントローラは1回プログラム可能(OTP)メモリを使用して電源シーケンスを制御し、出力電圧やGPIO構成などのデフォルトの構成も制御します。OTPは出荷時に、ソフトウェアの必要なしにスタートアップを行うようプログラムされます。ほとんどの静的な設定はSPIまたはI<sup>2</sup>Cによりデフォルトから変更でき、多くの種類のシステムで要求に応じてデバイスを構成できます。たとえば、電圧スケールリング・レジスタはプロセッサの動的な電圧スケールリング要件をサポートするため使用されます。OTPにはビット整合性エラー検出機能も含まれており、エラーが検出された場合には電源オン・シーケンスを停止し、システムが不明な状態で起動することを防止できます。



TPS65919-Q1デバイスには、システムの状態を監視するためのアナログ/デジタル・コンバータ(ADC)も含まれています。GPADCには2つの外部チャンネルがあり、任意の外部電圧を監視できるほか、内部チャンネルで電源電圧、出力電流、ダイの温度を測定でき、プロセッサがシステムの健全性を監視できます。このデバイスにはウォッチドッグ機能があり、ソフトウェアのロックアップを監視できます。また、短絡保護、温度監視、シャットダウン、および電圧が事前定義されたスレッショルドを下回るかどうかを検出するための自動ADC変換などの保護および診断機構が内蔵されています。PMICはこれらのイベントを割り込みハンドラでプロセッサへ通知でき、プロセッサはそれに対する応答動作を実行できます。

#### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
TPS65919-Q1	VQFN (48)	7.00mm×7.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

1.4 チャネル 1 の機能図

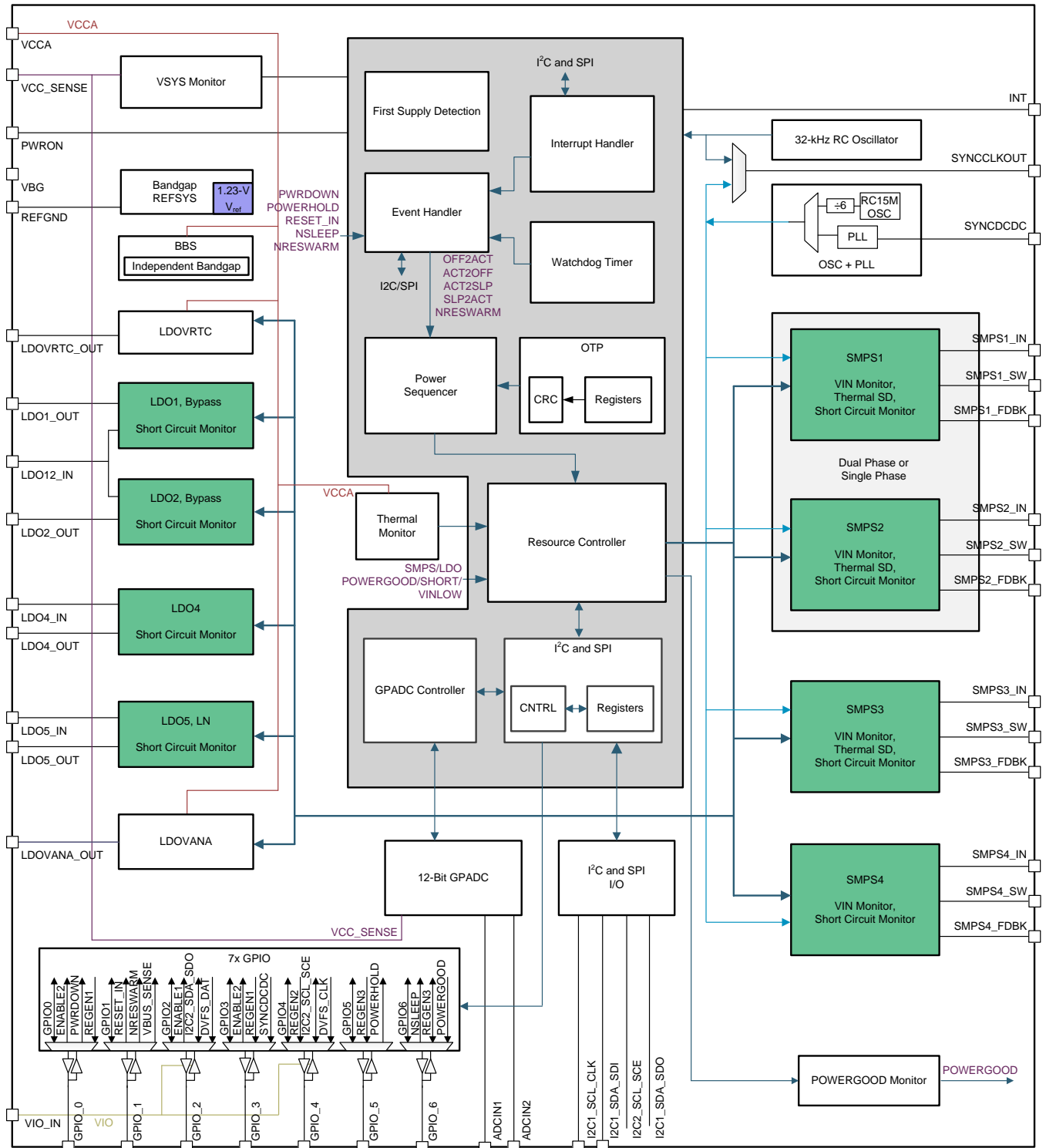


図 1-1. 機能図

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## 2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

### 2017年8月発行のものから更新

Page

- Clarified that LDO1 and LDO2 input pins are not included in this minimum recommended operating voltage. See *Electrical Characteristics: LDO Regulators* for more information. .... [12](#)
- Added LDO and SMPS output capacitance footnote .....
- Added SMPS Output voltage slew rate description .....
- 変更 the comparison condition from VCCA to VCC\_SENSE in the *Embedded Power Controller* section .....

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• Added typical debounce time from POWERHOLD to the enable of the first rail in the power sequence. ....	<a href="#">32</a>
• Changed discharge resistance to match electrical characteristics table section .....	<a href="#">41</a>
• Changed description of clock dithering from internal to external only .....	<a href="#">43</a>
• Added information about shutdown timing during short circuit detection .....	<a href="#">44</a>
• Updated POWERGOOD block diagram and description to clarify dual phase operation. ....	<a href="#">44</a>
• 追加 notes to the <i>SMPS Controls for DVS</i> image.....	<a href="#">46</a>
• 追加 the equation to convert GPADC code to internal die temperature in the <i>12-Bit Sigma-Delta General-Purpose ADC (GPADC)</i> section.....	<a href="#">50</a>
• Additional description of VSYS_LO functionality .....	<a href="#">64</a>
• Added details on identifying device version. ....	<a href="#">67</a>
• SMPS and LDO output capacitance specification further explained .....	<a href="#">72</a>
• Added design considerations for VCCA capacitance to support loss of power .....	<a href="#">72</a>
• Corrected 9-V <sub>pp</sub> with 7V absolute maximum specification in the <i>Layout Guidelines</i> section .....	<a href="#">77</a>
• Updated requirements relating to measurement of high-side and low-side FETs in the <i>Layout Guidelines</i> section...	<a href="#">78</a>
• Updated images and description on differential measurements across high-side and low-side FETs .....	<a href="#">79</a>

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### 3 Pin Configuration and Functions

Figure 3-1 shows the 48-pin RGZ plastic quad-flatpack no-lead (VQFN) pin assignments and thermal pad.

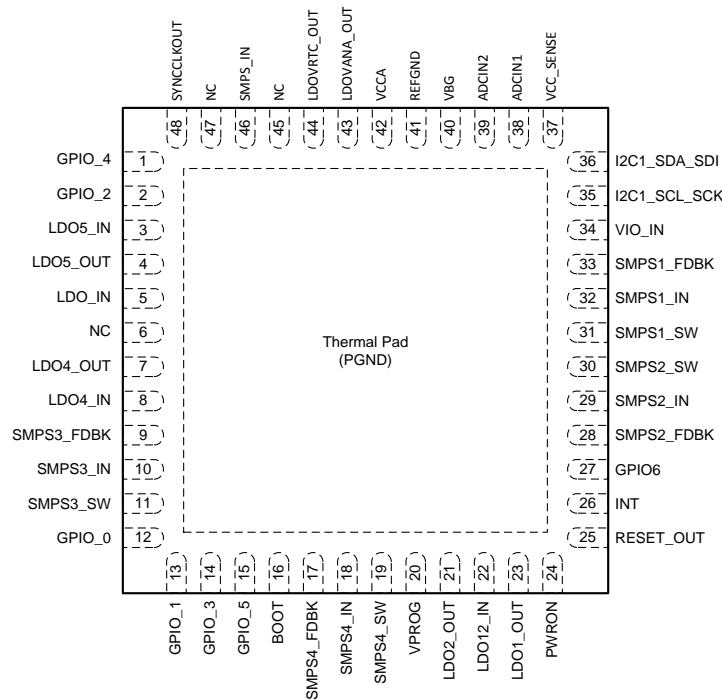


Figure 3-1. 48-Pin RGZ (VQFN) Package, 0.5-mm Pitch, With Thermal Pad (Top View)

#### 3.1 Pin Attributes

##### Pin Attributes

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED	PU/PD <sup>(1)</sup>
NAME	NO.				
<b>REFERENCE</b>					
REFGND	41	—	System reference ground	Ground	—
VBG	40	O	Bandgap reference voltage	—	—
<b>STEP-DOWN CONVERTERS (SMPSs)</b>					
SMPS1_IN	32	I	Power input for SMPS1	System supply	—
SMPS1_FDBK	33	I	Output voltage-sense (feedback) input for SMPS1 or differential voltage-sense (feedback) positive input for SMPS12 in dual-phase configuration	Ground	—
SMPS1_SW	31	O	Switch node of SMPS1; connect output inductor	Floating	—
SMPS2_IN	29	I	Power input for SMPS2	System supply	—
SMPS2_FDBK	28	I	Output voltage-sense (feedback) input for SMPS2 or differential voltage-sense (feedback) negative input for SMPS12 in dual-phase configuration	Ground	—
SMPS2_SW	30	O	Switch node of SMPS2; connect output inductor	Floating	—
SMPS3_IN	10	I	Power input for SMPS3	System supply	—
SMPS3_FDBK	9	I	Output voltage-sense (feedback) input for SMPS3	Ground	—
SMPS3_SW	11	O	Switch node of SMPS3; connect output inductor	Floating	—
SMPS4_IN	18	I	Power input for SMPS4	System supply	—

(1) The PU/PD column shows the pullup and pulldown resistors on the digital input lines. Pullup and pulldown resistors: PU = Pullup, PD = Pulldown, PPU = Software-programmable pullup, PPD = Software-programmable pulldown.

**Pin Attributes (continued)**

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED	PU/PD <sup>(1)</sup>
NAME	NO.				
SMPS4_FDBK	17	I	Output voltage-sense (feedback) input for SMPS4	Ground	—
SMPS4_SW	19	O	Switch node of SMPS4; connect output inductor	Floating	—
SMPS_IN	46	I	Power input for SMPS	System supply	—
NC	45	—	No Connection	Floating	—
NC	47	—	No Connection	Floating	—
<b>LOW DROPOUT REGULATORS</b>					
LDO12_IN	22	I	Power input voltage for LDO1 and LDO2 regulators	System supply	—
LDO1_OUT	23	O	LDO1 output voltage	Floating	—
LDO2_OUT	21	O	LDO2 output voltage	Floating	—
LDO_IN	5	I	Power input voltage for LDO regulator	System supply	—
NC	6	—	No Connection	Floating	—
LDO4_IN	8	I	Power input voltage for LDO4 regulator	System supply	—
LDO4_OUT	7	O	LDO4 output voltage	Floating	—
LDO5_IN	3	I	Power input voltage for LDO5 regulator	System supply	—
LDO5_OUT	4	O	LDO5 output voltage	Floating	—
<b>LOW-DROPOUT REGULATORS (INTERNAL)</b>					
LDOVRTC_OUT	44	O	LDOVRTC output voltage. To support rapid power off and on, connect a pulldown resistor on the LDOVRTC_OUT pin. See 5.15 for more details.	—	—
LDOVANA_OUT	43	O	LDOVANA output voltage	—	—
<b>GPADC</b>					
ADCIN1	38	I	GPADC input 1	Ground	—
ADCIN2	39	I	GPADC input 2	Ground	—
<b>CLOCKING</b>					
SYNCLKOUT	48	O	Primary function: 2.2-MHz fallback switching frequency for SMPS Secondary function: 32-kHz digital-gated output clock when VIO_IN input supply is present	Floating	—
<b>SYSTEM CONTROL</b>					
BOOT	16	I	Boot ball for power-up sequence selection	Ground or VRTC	—
GPIO_0	12	I/O	Primary function: General-purpose input <sup>(2)</sup> and output	Ground or VRTC	PPD
		I	Secondary function: ENABLE2 which is the peripheral power request input 2	Floating	PPD <sup>(2)</sup>
			Secondary function: PWRDOWN input	Ground or VIO	PPD
		O	Secondary function: REGEN1 which is the external regulator enable output 1	Floating	—
GPIO_1	13	I/O	Primary function: General-purpose input <sup>(2)</sup> and output	Floating	PPD
			Secondary function: RESET_IN which is the reset input	Floating	PPD
		I	Secondary function: VBUS_SENSE input	Ground or VIO	—
			Secondary function: NRESWARM which is the warm reset input	VRTC	PPD
GPIO_2	2	I/O	Primary function: General-purpose input <sup>(2)</sup> and output	Floating	PPU PPD
		I	Secondary function: ENABLE1 which is the peripheral power request input 1	Floating	PPU PPD <sup>(2)</sup>
		I/O	Secondary function: I2C2_SDA_SDO which is the DVS I <sup>2</sup> C serial bidirectional data (external pullup) and the SPI output data signal	Floating	—

(2) Default option.

## Pin Attributes (continued)

PIN		I/O	DESCRIPTION	CONNECTION IF NOT USED	PU/PD <sup>(1)</sup>
NAME	NO.				
GPIO_3	14	I/O	Primary function: General-purpose input <sup>(2)</sup> and output	Floating	PPD
		O	Secondary function: REGEN1 which is the external regulator enable output 1	Floating	—
		I	Secondary function: ENABLE2 which is the peripheral power request input 2		PPD <sup>(2)</sup>
		I	Secondary function: SYNCDCDC which is the synchronization signal for SMPS switching	Floating	PPD <sup>(2)</sup>
GPIO_4	1	I/O	Primary function: General-purpose input <sup>(2)</sup> and output	Floating	PPU PPD
		O	Secondary function: REGEN2 which is the external regulator enable output 2	Floating	—
		I	Secondary function: I2C2_SCL_SCE which is the DVS I <sup>2</sup> C serial clock (external pullup) and the SPI chip enable signal	Floating	—
GPIO_5	15	I/O	Primary function: General-purpose input <sup>(2)</sup> and output	Ground	PPD
		I	Secondary function: POWERHOLD input	Ground or VIO	PPD
		O	Secondary function: REGEN3 which is the external regulator enable output 3	Floating	—
GPIO_6	27	I/O	Primary function: General-purpose input <sup>(2)</sup> and output	Ground	PPD
		I	Secondary function: NSLEEP request signal	Floating	PPU <sup>(2)</sup> PPD
		O	Secondary function: POWERGOOD which is the indication signal for valid regulator output voltages	Floating	—
		O	Secondary function: REGEN3 which is the external regulator enable output 3	Floating	—
I2C1_SCL_SCK	35	I	Control I <sup>2</sup> C serial clock (external pullup) and SPI clock signal	—	—
I2C1_SDA_SDI	36	I/O	Control I <sup>2</sup> C serial bidirectional data (external pullup) and SPI input data signal	—	—
INT	26	O	Maskable interrupt output request to the host processor	—	—
PWRON	24	I	External power-on event (on-button switch-on event)	Floating	PU
RESET_OUT	25	O	System reset or power on output (low = reset, high = active or sleep)	Floating	—
<b>PROGRAMMING, TESTING</b>					
VPROG	20	I	Primary function: OTP programming voltage	Ground or floating	—
		O	Secondary function: TESTV	Floating	—
<b>POWER SUPPLIES</b>					
VCCA	42	I	Analog input voltage for internal LDOs	System supply	—
VCC_SENSE	37	I	System supply sense line	System supply	—
VIO_IN	34	I	Digital supply input for GPIOs and I/O supply voltage	N/A	—



### 3.2 Signal Descriptions

**Table 3-1. Signal Descriptions**

SIGNAL NAME	LEVEL	I/O <sup>(1)</sup>	INPUT PU/PD <sup>(2)</sup>	PU/PD SELECTION	OUTPUT TYPE SELECTION	ACTIVITY	OTP POLARITY SELECTION
PWRON	VSYS (VCCA)	Input	PU fixed	N/A (fixed)	N/A (input)	Low	No
BOOT	VRTC	Tri-level input	N/A (input)	N/A (input)	N/A (input)	Boot conf.	No
GPIO_0 (primary function)	VRTC, fail-safe (5.25-V tolerance)	Input <sup>(1)</sup> /output	PPD	OTP/SW	Open-drain	Low or high	Yes
GPIO_0 secondary function: PWRDOWN		Input	PPD (Opt. Ext. PU)	OTP/SW	N/A (input)	High	Yes
GPIO_0 secondary function: ENABLE2		Input	PPD <sup>(1)</sup>	SW	N/A (input)	High	No, but software possible
GPIO_0 secondary function: REGEN1		Output	N/A (output)	N/A (output)	Open-drain	High	No
GPIO_1 (primary function)	VRTC, fail-safe (5.25-V tolerance)	Input <sup>(1)</sup> /output	PPD	OTP/SW	Open-drain	Low or high	Yes
GPIO_1 secondary function: RESET_IN		Input	PPD	OTP/SW	N/A (input)	Low	Yes
GPIO_1 secondary function: NRESWARM		Input	PPD	SW	N/A (input)	Low or high	Yes
GPIO_1 secondary function: VBUS_SENSE		Input	No	No	N/A (input)	High	No

(1) Default option.

(2) Pullup and pulldown resistors: PU = Pullup, PD = Pulldown, PPU = Software-programmable pullup, PPD = Software-programmable pulldown.

**Table 3-1. Signal Descriptions (continued)**

SIGNAL NAME	LEVEL	I/O <sup>(1)</sup>	INPUT PU/PD <sup>(2)</sup>	PU/PD SELECTION	OUTPUT TYPE SELECTION	ACTIVITY	OTP POLARITY SELECTION
GPIO_2 (primary function)	VIO (VIO_IN)	Input <sup>(1)</sup> /output	PPU/PPD	OTP/SW	Push-pull <sup>(1)</sup> or open-drain	Low or high	Yes
GPIO_2 secondary function: ENABLE1		Input	PPU/PPD <sup>(1)</sup>	SW	N/A (input)	High	No, but software possible
GPIO_2 secondary function: I2C2_SDA_SDO		Input/output	No	No	Open-drain	High	No
GPIO_3 (primary function)	VRTC, fail-safe (5.25-V tolerance)	Input <sup>(1)</sup> /output	PPD	OTP/SW	Open-drain	Low or high	Yes
GPIO_3 secondary function: ENABLE2		Input	PPD <sup>(1)</sup>	SW	N/A (input)	High	No, but software possible
GPIO_3 secondary function: REGEN1		Output	N/A (output)	N/A (output)	Open-drain	High	No
GPIO_3 secondary function: SYNCD CDC		Input	PPD <sup>(1)</sup>	SW	N/A (input)	Toggling	No
GPIO_4 (primary function)	VIO (VIO_IN)	Input <sup>(1)</sup> /output	PPU/PPD	OTP/SW	Push-pull <sup>(1)</sup> or open-drain	Low or high	Yes
GPIO_4 secondary function: REGEN2		Output	N/A (output)	N/A (output)	Push-pull <sup>(1)</sup> or open-drain	High	No
GPIO_4 secondary function: I2C2_SCL_SCE		Input	No	No	N/A (input)	High	No
GPIO_5 (primary function)	VRTC, fail-safe (5.25-V tolerance)	Input <sup>(1)</sup> /output	PPD	OTP/SW	Open-drain	Low or high	Yes
GPIO_5 secondary function: POWERHOLD		Input	PPD <sup>(1)</sup>	SW	N/A (input)	High	Yes
GPIO_5 secondary function: REGEN3		Output	N/A (output)	N/A (output)	Open-drain	High	No

**Table 3-1. Signal Descriptions (continued)**

SIGNAL NAME	LEVEL	I/O <sup>(1)</sup>	INPUT PU/PD <sup>(2)</sup>	PU/PD SELECTION	OUTPUT TYPE SELECTION	ACTIVITY	OTP POLARITY SELECTION
GPIO_6 (primary function)	VRTC	Input <sup>(1)</sup> /output	PPD	OTP/SW	Open-drain	Low or high	Yes
GPIO_6 secondary function: NSLEEP		Input	PPU <sup>(1)</sup> /PPD	SW	N/A (input)	Low	Yes
GPIO_6 secondary function: POWERGOOD		Output	N/A (output)	N/A (output)	Open-drain	Low or high	Yes
GPIO_6 secondary function: REGEN3		Output	N/A (output)	N/A (output)	Open-drain	High	No
RESET_OUT	VIO (VIO_IN)	Output	N/A (output)	N/A (output)	Push-pull <sup>(1)</sup> or open-drain	Low	No
INT	VIO (VIO_IN)	Output	N/A (output)	N/A (output)	Push-pull <sup>(1)</sup> or open-drain	Low	No, but software possible
SYNCLKOUT	VRTC	Output	N/A (output)	N/A (output)	Push-pull	Toggling	No
I2C1_SDA_SDI	VIO (VIO_IN)	Input/output	No	No	Open-drain	High	No
I2C1_SCL_CLK	VIO (VIO_IN)	Input	No	No	N/A (input)	High	No
VCC_SENSE	VSYS (VCCA)	Input	No	No	N/A (analog)	Analog	No

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	VCCA	-0.3	6	V
	VCC_SENSE	-0.3	7	
	All LDOs and SMPS supply voltage input pins	-0.3	6	
	SMPSx_SW pins, 10-ns transient	-2	7	
	All SMPS-related input pins _FDBK	-0.3	3.6	
	I/O digital supply voltage (VIO_IN with respect to VIO_GND)	-0.3 VIO <sub>max</sub> + 0.3	VIO <sub>max</sub> + 0.3	
	VBUS	-0.3	6	
	GPADC pins: ADCIN1 and ADCIN2	-0.3	2.4	
	OTP supply voltage VPROG	-0.3	7	
	VRTC digital input pins, without fail-safe	-0.3	2.15	
	VRTC digital input pins, with fail-Safe	-0.3	5.25	
	VIO digital input pins (VIO_IN pin reference)	-0.3	VIO <sub>max</sub> + 0.3	
	VSYS digital input pins (VCCA pin reference)	-0.3	6	
Current	Peak output current on all pins other than power resources	-5	5	mA
	Buck SMPS, SMPSx_IN, SMPSx_SW, and SMPSx_OUT total per phase		4	A
	LDOs		1	
Junction temperature, T <sub>J</sub>		-45	150	°C
Storage temperature, T <sub>stg</sub>		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 4.2 ESD Ratings

			VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V	
		Charged-device model (CDM), per AEC Q100-011	All pins		±500
			Corner pins (1, 12, 13, 24, 25, 36, 37, and 48)		±750

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 4.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
<b>ELECTRICAL</b>					
System voltage input pin VCCA (named VSYS in the specification)		3.135	3.8	5.25	V
VCC_SENSE, HIGH_VCC_SENSE = 0 (if measured with GPADC, see also 表 5-9)		3.135		VCCA	V
VCC_SENSE, HIGH_VCC_SENSE = 1 (if measured with GPADC, see also 表 5-9)		3.135		VCCA - 1	V
All LDO-related input pins _IN <sup>(1)</sup>		1.75	3.8	5.25	V
All SMPS-related input pins _IN		3.135	3.8	5.25	V
All SMPS-related input pins _FDBK		0		V <sub>OUTmax</sub> + 0.3	V
All SMPS-related input pins _FDBK_GND		-0.3		0.3	V
I/O digital supply voltage VIO_IN	VIO = 1.8 V	1.71	1.8	1.89	V
	VIO = 3.3 V	3.135	3.3	3.465	

(1) Does not include LDO1 and LDO2 minimum input voltages.

## Recommended Operating Conditions (continued)

Over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
Voltage on the GPADC pins ADCIN1 (channel 0) and ADCIN2 (channel 1)		0		1.25	V
OTP supply voltage VPROG		0	6		V
Voltage on VRTC digital input pins	without fail-safe	0	LDOVRTC	1.85	V
	with fail-safe	0	LDOVRTC	5.25	
Voltage on VIO digital input pin (VIO_IN pin reference)		0	VIO	VIO <sub>max</sub>	V
Voltage on VSYS digital input pins (VCCA pin reference)		0	3.8	5.25	V
<b>TEMPERATURE</b>					
Operating free-air temperature range <sup>(2)</sup>		-40	27	105	°C
Junction temperature, T <sub>J</sub>	Operational	-40	27	150	°C
	Parametric compliance	-40	27	125	
Storage temperature, T <sub>stg</sub>		-65	27	150	°C
Lead temperature (soldering, 10 s)			260		°C

(2) Additional cooling strategies may be necessary to maintain junction temperature at recommended limits.

## 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS65919-Q1	UNIT
		RGZ (VQFN)	
		48 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	24.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	5.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	3.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.1	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	3.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	0.1	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 4.5 Electrical Characteristics — LDO Regulators

Over operating free-air temperature range, typical values are at T<sub>A</sub> = 27°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Input filtering capacitance (C18, C19)	Connected from LDOx_IN to GND Shared input tank capacitance (depending on platform requirements)	0.6	2.2		μF	
Output filtering capacitance (C20, C21, C22, C23, C24) <sup>(1)</sup>	Connected from LDOx_OUT to GND	0.6	2.2	2.7	μF	
C <sub>ESR</sub>	Filtering capacitor ESR	< 100 kHz	20	100	600	mΩ
		1 to 10 MHz	1	10	20	
V <sub>IN(LDOx)</sub>	LDO1, LDO2 from LDO12_IN, Normal Mode	0.9 V ≤ V <sub>OUT</sub> < 2.2 V	1.2		VCCA	V
		2.2 V ≤ V <sub>OUT</sub> ≤ 3.3 V	1.2		5.25	
	LDO1, LDO2 from LDO12_IN, Bypass Mode	V <sub>OUT</sub> = V <sub>IN</sub>	1.2		3.6	
	LDO4, LDO5 from LDO4_IN and LDO5_IN	0.9 V ≤ V <sub>OUT</sub> < 2.2 V	1.75		VCCA	
2.2 V ≤ V <sub>OUT</sub> ≤ 3.3 V		1.75		5.25		
V <sub>OUT(LDOx)</sub>	LDO output voltage programmable <sup>(2)</sup> (except LDOVRTC and LDOVANA)	Range			3.3	V
	Step size		50			mV
T <sub>DCOV(LDOx)</sub>	Total DC output voltage accuracy, including voltage references, DC load and line regulations, process and temperature	All LDOs except LDOVANA and LDOVRTC V <sub>IN(LDOx)</sub> ≥ 2.5 V	0.99 × V <sub>OUT(LDOx)</sub> - 0.014		1.006 × V <sub>OUT(LDOx)</sub> + 0.014	V
		All LDOs except LDOVANA and LDOVRTC V <sub>IN(LDOx)</sub> < 2.5 V and V <sub>OUT(LDOx)</sub> < 1.5 V	0.99 × V <sub>OUT(LDOx)</sub> - 0.014		1.006 × V <sub>OUT(LDOx)</sub> + 0.014	

(1) Additional information about how this parameter is specified is located in 6.2.2.

(2) LDO output voltages are programmed separately.

## Electrical Characteristics — LDO Regulators (continued)

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$T_{\text{DCOV(LDOx)}}$	Total DC output voltage accuracy, including voltage references, DC load and line regulations, process and temperature	LDOVRTC_OUT	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	1.726	1.8	1.85	V
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$	1.726	1.8	1.85	
$T_{\text{DCOV(LDOx)}}$	Total DC output voltage accuracy, including voltage references, DC load and line regulations, process and temperature	LDOVANA_OUT	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	2.002	2.093	2.14	V
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$	2.002	2.093	2.14	
$D_{\text{V(LDOx)}}$	Dropout voltage $D_{\text{V(LDOx)}} = V_{\text{IN}} - V_{\text{OUT}}$ where $V_{\text{OUT}} = V_{\text{OUTnom}} - 2\%$	LDO1, LDO2: $I_{\text{OUT}} = I_{\text{OUTmax}}$				150	mV
		LDO4: $I_{\text{OUT}} = I_{\text{OUTmax}}$				290	
		LDO5: $I_{\text{OUT}} = 50\text{ mA}$				150	
		LDO5: $I_{\text{OUT}} = I_{\text{OUTmax}}$ (not low-noise performance)				290	
$I_{\text{OUT(LDOx)}}$	Output current	LDO1, LDO2				300	mA
		LDO4				200	
		LDO5				100	
$I_{\text{OUT(LDOx)}}$	Output current, internal LDOs	LDOVANA in Active Mode				10	mA
$I_{\text{OUT(LDOx)}}$	Output current, internal LDOs	LDOVRTC in Active Mode				25	mA
$I_{\text{SHORT(LDOx)}}$	LDO current limitation	LDO1, LDO2		380	600	1800	mA
		LDO4		340	650	1300	
		LDO5		135	325	740	
	LDO inrush current	LDO1, LDO2				500	mA
$\text{DC}_{\text{LDR}}$	DC load regulation, $\Delta V_{\text{OUT}}$	$I_{\text{OUT}} = 0$ to $I_{\text{OUTmax}}$ at pin, LDO1, LDO2	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		4	16	mV
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$		4	16	
		$I_{\text{OUT}} = 0$ to $I_{\text{OUTmax}}$ at pin, all other LDOs	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		4	14	
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$		4	14	
$\text{DC}_{\text{LNR}}$	DC line regulation, $\Delta V_{\text{OUT}} / V_{\text{OUT}}$	$V_{\text{IN}} = V_{\text{INmin}}$ to $V_{\text{INmax}}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.1%	0.2%		
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$	0.1%	0.2%		
		$V_{\text{SYS}} = V_{\text{SYSmin}}$ to $V_{\text{SYSmax}}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$ , $V_{\text{IN}}$ constant (LDO preregulated), $V_{\text{OUT}} \leq 2.2\text{ V}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	0.3%	0.75%		
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$	0.3%	0.75%		
$R_{\text{DIS}}$	Pulldown discharge resistance at LDO output, except LDOVRTC	Off mode, pulldown enabled and LDO disabled. Applies to bypass mode also.		30		125	$\Omega$
	Power supply ripple rejection (PSRR), LDO1, LDO2	$f = 217\text{ Hz}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$		55	90		
		$f = 50\text{ kHz}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$		35	45		
		$f = 1\text{ MHz}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$		25	35		
	Power supply ripple rejection (PSRR), LDO4	$f = 217\text{ Hz}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$		55	90	dB	
		$f = 50\text{ kHz}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$		25	45		
		$f = 1\text{ MHz}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$		20	35		
	Power supply ripple rejection (PSRR), LDO5	$f = 217\text{ Hz}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$		55	90		
		$f = 50\text{ kHz}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$		25	45		
		$f = 1\text{ MHz}$ , $I_{\text{OUT}} = I_{\text{OUTmax}}$		25	35		
$I_{\text{Qoff}}$	Quiescent current – off mode	For all LDOs, $V_{\text{CCA}} = V_{\text{IN(LDOx)}} = 3.8\text{ V}$ , $T_A = 27^\circ\text{C}$		0.1	0.4	$\mu\text{A}$	
		For all LDOs, $V_{\text{CCA}} = V_{\text{IN(LDOx)}} = 3.8\text{ V}$ , $T_A = 85^\circ\text{C}$		0.2	1.3		
		For all LDOs, $V_{\text{CCA}} = V_{\text{IN(LDOx)}} = 3.8\text{ V}$ , $T_A = 105^\circ\text{C}$		0.2	1.3		
$I_{\text{Qon(LDO)}}$	Quiescent current – LDO on mode	$I_{\text{LOAD}} = 0\text{ mA}$ (LDO1, LDO2), $V_{\text{IN(LDOx)}} > V_{\text{OUT(LDOx)}} + D_{\text{V(LDOx)}}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	46	70	$\mu\text{A}$	
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$	46	70		
		$I_{\text{LOAD}} = 0\text{ mA}$ (LDO4), $V_{\text{IN(LDOx)}} > V_{\text{OUT(LDOx)}} + D_{\text{V(LDOx)}}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	36	47		
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$	36	47		
		$I_{\text{LOAD}} = 0\text{ mA}$ (LDO5), $V_{\text{OUT}} \leq 1.8\text{ V}$ , $V_{\text{IN(LDOx)}} > V_{\text{OUT(LDOx)}} + D_{\text{V(LDOx)}}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	140	190		
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$	140	190		
		$I_{\text{LOAD}} = 0\text{ mA}$ (LDO5), $V_{\text{OUT}} > 1.8\text{ V}$ , $V_{\text{IN(LDOx)}} > V_{\text{OUT(LDOx)}} + D_{\text{V(LDOx)}}$	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$	180	210		
			$85^\circ\text{C} < T_A \leq 105^\circ\text{C}$	180	210		
$\alpha\text{Q}$	Quiescent current coefficient LDO on mode, $I_{\text{Qout}} = I_{\text{Qon}} + \alpha\text{Q} \times I_{\text{OUT}}$	$I_{\text{OUT}} < 100\ \mu\text{A}$		4%			
		$100\ \mu\text{A} \leq I_{\text{OUT}} < 1\text{ mA}$		2%			
		$I_{\text{OUT}} \geq 1\text{ mA}$		1%			
$T_{\text{LDR}}$	Transient load regulation, $\Delta V_{\text{OUT}}$	On mode, $I_{\text{OUT}} = 10\text{ mA}$ to $I_{\text{OUTmax}} / 2$ , $T_R = T_F = 1\ \mu\text{s}$ . All LDOs except LDO5		-25	25	mV	
		On mode, $I_{\text{OUT}} = 1\text{ mA}$ to $I_{\text{OUTmax}} / 2$ , $T_R = T_F = 1\ \mu\text{s}$ . LDO5		-25	25		
		On mode, $I_{\text{OUT}} = 100\ \mu\text{A}$ to $I_{\text{OUTmax}} / 2$ , $T_R = T_F = 1\ \mu\text{s}$		-50	33		

## Electrical Characteristics — LDO Regulators (continued)

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$T_{LNR}$	Transient line regulation, $\Delta V_{OUT} / V_{OUT}$	$V_{IN}$ step = 600 mVpp, $T_R = T_F = 10 \mu\text{s}$		0.25%	0.5%		
		$V_{SYS}$ step = 600 mVpp, $T_R = T_F = 10 \mu\text{s}$ . $V_{IN}$ constant (LDO preregulated), $V_{OUT} \leq 2.2 \text{ V}$		0.8%	1.6%		
Noise (except LDO5)		100 Hz < f ≤ 10 kHz		5000	8000	nV/√Hz	
		10 kHz < f ≤ 100 kHz		1250	2500		
		100 kHz < f ≤ 1 MHz		150	300		
		f > 1 MHz		250	500		
Noise (LDO5)		100 Hz < f ≤ 5 kHz, $I_{OUT} = 50 \text{ mA}$ , $V_{OUT} \leq 1.8 \text{ V}$		400	500	nV/√Hz	
		5 kHz < f ≤ 400 kHz, $I_{OUT} = 50 \text{ mA}$ , $V_{OUT} \leq 1.8 \text{ V}$		62	125		
		400 kHz < f ≤ 10 MHz, $I_{OUT} = 50 \text{ mA}$ , $V_{OUT} \leq 1.8 \text{ V}$		25	50		
Ripple		LDO1, LDO2, ripple at 32 kHz (from the internal charge pump of 300 mA LDO)			5	mV <sub>pp</sub>	
<b>LDO BYPASS MODE LDO1, LDO2</b>							
	Bypass resistance of 300 mA LDO	2.9 V ≤ $V_{IN}$ ≤ 3.3 V, $V_{SYS} \geq 3.4 \text{ V}$ , $I_{OUT} = 250 \text{ mA}$ , programmed to BYPASS				0.22	Ω
	Bypass resistance of 300 mA LDO	1.75 V ≤ $V_{IN}$ ≤ 1.9 V, $I_{OUT} = 75 \text{ mA}$ , programmed to BYPASS				0.24	Ω
	Bypass resistance of 300 mA LDO	1.75 V ≤ $V_{IN}$ ≤ 1.9 V, $I_{OUT} = 200 \text{ mA}$ , programmed to BYPASS				0.24	Ω
	Bypass mode inrush current	Maximum 50 μF load connected to LDOx_OUT				1100	mA
$I_{Oon(bypass)}$	Quiescent current – bypass mode					60	μA
	Slew-rate					60	mV/μs

## 4.6 Electrical Characteristics — SMPS1&2 in Dual-Phase Configuration

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input capacitance (C8, C9)			4.7		μF
	Output capacitance (C13, C14) <sup>(2)</sup>	SMPS1&2 input dual phase operation, per phase	33	47	57	μF
$C_{ESR}$	Filtering capacitor ESR	1 to 10 MHz		2	10	mΩ
	Output filter inductance (L1, L2)	SMPSx_SW	0.7	1	1.3	μH
$DCR_L$	Filter inductor DC resistance			50	100	mΩ
$V_{IN}$ (SMPSx)	Input voltage range, SMPSx_IN	$V_{SYS}$ (VCCA)	3.135		5.25	V
$V_{OUT}$ (SMPSx)	Output voltage, programmable, SMPSx	RANGE = 0 (value for RANGE must not be changed when SMPS is active). In ECO mode the output voltage values are fixed (defined before ECO mode is enabled). RANGE = 1 is not supported in Multi-phase configuration.	0.7		1.65	V
		Step size, $0.7 \text{ V} \leq V_{OUT} \leq 1.65 \text{ V}$ (RANGE = 0)		10		mV
	DC output voltage accuracy, includes voltage references, DC load and line regulation, process and temperature	ECO mode	-3%		4%	
		PWM mode	-1%		2%	
	Ripple, dual phase	Max load, $V_{IN} = 3.8 \text{ V}$ , $V_{OUT} = 1.2 \text{ V}$ , $ESR_{COUT} = 2 \text{ m}\Omega$ , measure with 20-MHz LPF		4		mV <sub>pp</sub>
$DC_{LNR}$	DC line regulation, $\Delta V_{OUT} / V_{OUT}$	$V_{IN} = V_{INmin}$ to $V_{INmax}$		0.1		%/V
$DC_{LDR}$	DC load regulation, $\Delta V_{OUT} / V_{OUT}$	$I_{OUT} = 0$ to $I_{OUTmax}$		0.1		%/A
$T_{LDSR}$	Transient load step response, dual phase	$I_{OUT} = 0.8$ to $2 \text{ A}$ , $T_R = T_F = 400 \text{ ns}$ , $C_{OUT} = 47 \mu\text{F}$ , $L = 1 \mu\text{H}$		3%		
		$I_{OUT} = 0.5$ to $500 \text{ mA}$ , $T_R = T_F = 100 \text{ ns}$ , $C_{OUT} = 47 \mu\text{F}$ , $L = 1 \mu\text{H}$		3%		
$I_{OUTmax}$	Rated output current, SMPS1&2	Advance thermal design is required to avoid thermal shut down			7	A
	Maximum output current, ECO mode				5	mA
$I_{LIM HS FET}$	High-side MOSFET forward current limit	SMPS1&2, each phase	4.2	4.5		A
$I_{LIM LS FET}$	Low-side MOSFET forward current limit	SMPS1&2, each phase		4.2		A
$R_{DS(ON) HS FET}$	N-channel MOSFET on-resistance, high-side FET	SMPS1&2, each phase		50		mΩ
$R_{DS(ON) LS FET}$	N-channel MOSFET on-resistance, low-side FET	SMPS1&2, each phase		39		mΩ
	Output voltage slew rate <sup>(3)</sup>	RANGE = 1		2.5		mV/μs

(1) SMPS1 and SMPS2 can be used in parallel in dual-phase mode to be able to multiply the output current by 2, and the converter is named SMPS1&2. The naming SMPS1 and SMPS2 is used when the bucks are configured as a separate buck converters.

(2) Additional information about how this parameter is specified is located in 6.2.2.

(3) This slew rate refers to the rate at which the output voltage changes from one voltage level to another voltage after startup is complete.

## Electrical Characteristics — SMPS1&2 in Dual-Phase Configuration (continued)

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).<sup>(1)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>DIS</sub>	Pull-down discharge resistance output	SMPS <sub>x</sub> _FDBK, SMPS turned off		375		Ω
		SMPS <sub>x</sub> _SW, SMPS turned off. Pull-down is at master phase output.		9	22	
R <sub>SENSE</sub>	Input resistance for remote sense (sense line)	Between SMPS1_FDBK and SMPS2_FDBK	260		2200	kΩ
I <sub>Qoff</sub>	Quiescent current – Off mode	I <sub>LOAD</sub> = 0 mA		0.1	2.5	μA
I <sub>Qon(ON)</sub>	Quiescent current – On mode, dual phase	ECO mode, device not switching, $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		15	25	μA
		ECO mode, device not switching, $85^\circ\text{C} < T_A \leq 105^\circ\text{C}$		18	25.5	
		PWM mode, I <sub>LOAD</sub> = 0 mA, V <sub>IN</sub> = 3.8 V, V <sub>OUT</sub> = 1 V, device switching, 1-phase operation			11	
V <sub>SMPSPG</sub>	Powergood threshold SMPS1, SMPS2	SMPS output voltage rising, referenced to programmed output voltage		-4%		
		SMPS output voltage falling, referenced to programmed output voltage		-16%		
I <sub>L_AVG_COMP</sub>	Powergood: GPADC monitoring SMPS1&2	IL_AVG_COMP_rising		6		A
		IL_AVG_COMP_falling				

## 4.7 Electrical Characteristics — SMPS1, SMPS2, SMPS3, and SMPS4 Stand-Alone Regulators

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input capacitance (C8, C9, C10, C11, C12)			4.7		μF
	Output capacitance (C13, C14, C15, C16, C17) <sup>(1)</sup>		33	47	57	μF
C <sub>ESR</sub>	Filtering capacitor DC ESR	1 to 10 MHz		2	10	mΩ
	Output filter inductance (L1, L2, L3, L4, L5)	SMPS <sub>x</sub> _SW	0.7	1	1.3	μH
DCR <sub>L</sub>	Filter inductor DC resistance			50	100	mΩ
V <sub>IN</sub> (SMPS <sub>x</sub> )	Input voltage range, SMPS <sub>x</sub> _IN	VSYS (VCCA)	3.135		5.25	V
V <sub>OUT</sub> (SMPS <sub>x</sub> )	Output voltage, programmable, SMPS <sub>x</sub>	RANGE = 0 (value for RANGE must not be changed when SMPS is active). In ECO mode the output voltage value is fixed (defined before ECO mode is enabled).	0.7		1.65	V
		RANGE = 1 (value for RANGE must not be changed when SMPS is active). In ECO mode the output voltage value is fixed (defined before ECO mode is enabled).	1.0		3.3	
		Step size, $0.7\text{ V} \leq V_{OUT} \leq 1.65\text{ V}$		10		mV
		Step size, $1\text{ V} \leq V_{OUT} \leq 3.3\text{ V}$		20		
	DC output voltage accuracy, includes voltage references, DC load and line regulation, process and temperature	ECO mode	-3%		4%	
		PWM mode	-1%		2%	
	Ripple	Max load, V <sub>IN</sub> = 3.8 V, V <sub>OUT</sub> = 1.2 V, ESR <sub>COUT</sub> = 2 mΩ, measured with 20-MHz LPF		8		mV <sub>pp</sub>
DC <sub>LNR</sub>	DC line regulation, $\Delta V_{OUT} / V_{OUT}$	V <sub>IN</sub> = V <sub>INmin</sub> to V <sub>INmax</sub>		0.1		%/V
DC <sub>LDR</sub>	DC load regulation, $\Delta V_{OUT} / V_{OUT}$	I <sub>OUT</sub> = 0 to I <sub>OUTmax</sub>		0.1		%/A
T <sub>LDSR</sub>	Transient load step response	SMPS1, SMPS2, SMPS3, I <sub>OUT</sub> = 0.5 to 500 mA, T <sub>R</sub> = T <sub>F</sub> = 100 ns, C <sub>OUT</sub> = 47 μF, L = 1 μH		3%		
T <sub>LDSR</sub>	Transient load step response	SMPS4, I <sub>OUT</sub> = 0.5 to 500 mA, T <sub>R</sub> = T <sub>F</sub> = 1 μs, C <sub>OUT</sub> = 47 μF, L = 1 μH		3%		
I <sub>OUTmax</sub> (SMPS1,2)	Rated output current, SMPS1, SMPS2	Advance thermal design is required to avoid thermal shut down			3.5	A
I <sub>OUTmax</sub> (SMPS3)	Rated output current, SMPS3	Advance thermal design is required to avoid thermal shut down			3	A
I <sub>OUTmax</sub> (SMPS4)	Rated output current, SMPS4	Advance thermal design is required to avoid thermal shut down			1.5	A
I <sub>OUTmax</sub> (ECO)	Maximum output current, ECO mode	Advance thermal design is required to avoid thermal shut down			5	mA
I <sub>LIM HS FET</sub>	High-side MOSFET forward current limit	SMPS1, SMPS2, SMPS3	4.2	4.5		A
		SMPS4	2.2	2.5		
I <sub>LIM LS FET</sub>	Low-side MOSFET forward current limit	SMPS1, SMPS2, SMPS3		4.2		A
		SMPS4		2.2		
R <sub>DS(ON) HS FET</sub>	N-channel MOSFET on-resistance (high-side FET)	SMPS1, SMPS2, SMPS3		50		mΩ
		SMPS4		110		
R <sub>DS(ON) LS FET</sub>	N-channel MOSFET on-resistance (low-side FET)	SMPS1, SMPS2, SMPS3		39		mΩ
		SMPS4		79		
	Overshoot during turn-on				5%	

(1) Additional information about how this parameter is specified is located in 6.2.2.



## Electrical Characteristics — SMPS1, SMPS2, SMPS3, and SMPS4 Stand-Alone Regulators (continued)

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage slew rate <sup>(2)</sup>			2.5		mV/ $\mu\text{s}$
$R_{DIS}$ Pulldown discharge resistance at SMPSx output	SMPSx_FDBK, SMPS turned off		375		$\Omega$
	SMPSx_SW, SMPS turned off		9	22	
$I_{Qoff}$ Quiescent current – Off mode	$I_{LOAD} = 0\text{ mA}$		0.1	2.5	$\mu\text{A}$
$I_{Qon(SMPS1,2,3)}$ Quiescent current – On mode - SMPS1, SMPS2, SMPS3	ECO mode, device not switching, $V_{OUT} < 1.8\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		15	25	$\mu\text{A}$
	ECO mode, device not switching, $V_{OUT} < 1.8\text{ V}$ , $85^\circ\text{C} < T_A \leq 105^\circ\text{C}$		18	25.5	
	ECO mode, device not switching, $V_{OUT} \geq 1.8\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		16.5	25	
	ECO mode, device not switching, $V_{OUT} \geq 1.8\text{ V}$ , $85^\circ\text{C} < T_A \leq 105^\circ\text{C}$		19.5	25.5	
	FORCED_PWM mode, $I_{LOAD} = 0\text{ mA}$ , $V_{IN} = 3.8\text{ V}$ , $V_{OUT} = 1\text{ V}$ , device switching			11	
$I_{Qon(SMPS4)}$ Quiescent current – On mode - SMPS4	ECO mode, device not switching, $V_{OUT} < 1.8\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		15	24	$\mu\text{A}$
	ECO mode, device not switching, $V_{OUT} < 1.8\text{ V}$ , $85^\circ\text{C} < T_A \leq 105^\circ\text{C}$		18	25	
	ECO mode, device not switching, $V_{OUT} \geq 1.8\text{ V}$ , $-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		16.5	24	
	ECO mode, device not switching, $V_{OUT} \geq 1.8\text{ V}$ , $85^\circ\text{C} < T_A \leq 105^\circ\text{C}$		19.5	25	
	FORCED_PWM mode, $I_{LOAD} = 0\text{ mA}$ , $V_{IN} = 3.8\text{ V}$ , $V_{OUT} = 1\text{ V}$ , device switching			7	
$V_{SMPSPG}$ Powergood threshold	SMPS output voltage rising, referenced to programmed output voltage		-4%		
	SMPS output voltage falling, referenced to programmed output voltage		-16%		
IL_AVG_COMP Powergood: GPADC monitoring	IL_AVG_COMP_rising - SMPS1, SMPS2		3		A
	IL_AVG_COMP_rising - SMPS3		3		
	IL_AVG_COMP_falling - SMPS1, SMPS2, SMPS3			$I_{L\_AVG\_COM}$ $P_{rising} - 5\%$	

(2) This slew rate refers to the rate at which the output voltage changes from one voltage level to another voltage after startup is complete.

## 4.8 Electrical Characteristics — Reference Generator (Bandgap)

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filtering capacitor	Connected from VBG to REFGND	30	100	150	nF
Output voltage			0.85		V
Ground current			20	40	$\mu\text{A}$

## 4.9 Electrical Characteristics — 32-kHz RC Oscillators and SYNCCLKOUT Output Buffers

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>32-kHz RC OSCILLATOR</b>					
Active current consumption			4	8	$\mu\text{A}$
Power down current				30	nA
<b>SYNCCLKOUT OUTPUT BUFFER</b>					
Logic output external load		5	35	50	pF

## 4.10 Electrical Characteristics — 12-Bit Sigma-Delta ADC

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{OON}$ Current consumption	During conversion		1500	1600	$\mu\text{A}$
$I_{OOFF}$ Off mode current	GPADC is not enabled (no conversion)			1	$\mu\text{A}$
Gain error	Without calibration (inputs without scaler)	-3.5%		3.5%	
	Without calibration (inputs with scaler)	-4.5%		4.5%	
	With calibration, $T_A = 27^\circ\text{C}$ , $V_{CCA} = 5.25\text{V}$	-0.95%		0.95%	
Offset	Without calibration	-65		65	LSB
	With calibration, $T_A = 27^\circ\text{C}$ , $V_{CCA} = 5.25\text{V}$	-17		17	
Gain error drift (after trimming, including reference voltage)	Temperature and supply	-0.6%		0.6%	
Offset drift after trimming	Temperature and supply	-2		2	LSB
INL Integral nonlinearity	Best fitting	-3.5		3.5	LSB
DNL Differential nonlinearity		-1		3.5	LSB
Input capacitance	ADCIN1, ADCIN2		0.5		pF
Source input impedance	Source resistance without capacitance			20	k $\Omega$
	Source capacitance with > 20-k $\Omega$ source resistance	100			nF
Input range (sigma-delta ADC)	Typical range	0		1.25	V
	Assured range without saturation	0.01		1.215	
<b>SMPS CURRENT MONITORING (GPADC CHANNEL 4)<sup>(1)</sup></b>					
Channel 4 SMPS output current measurement gain factor, $I_{FS0}$			3.958		A
Channel 4 SMPS output current measurement current offset, $I_{OS0}$			0.652		A
Channel 4 SMPS output current measurement temperature coefficient, $TC_{R0}$			-1090		ppm/ $^\circ\text{C}$
SMPS output current measurement accuracy, $I_{err}$ (%), GPADC trimmed	$I_{LOAD\_error} (\%) = I_{LOAD\_meas} / I_{LOAD} \times 100$ . $I_{LOAD} = 3\text{ A}$ for SMPS1/SMPS2/SMPS3. $25^\circ\text{C}$	-8%		8%	
SMPS output current measurement accuracy, $I_{err}$ (%), GPADC trimmed	$I_{LOAD\_error} (\%) = I_{LOAD\_meas} / I_{LOAD} \times 100$ .	-10%		10%	

- (1) **Basic equation for result:**  $I_{LOAD} = I_{FS} \times \text{GPADC code} / (2^{12} - 1) - I_{OS}$ , where K is the number of SMPS active phases,  $I_{FS} = I_{FS0} \times K$  and  $I_{OS} = I_{OS0} \times K$   
**Temperature compensated result:**  $I_{LOAD} = I_{FS} \times \text{GPADC code} / ((2^{12} - 1) \times (1 + TC_{R0} \times (TEMP - 25))) - I_{OS}$

## 4.11 Electrical Characteristics — Thermal Monitoring and Shutdown

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Hot-die temperature threshold	HDSEL[1:0] = 00	Rising threshold	104	117	127	$^\circ\text{C}$
		Falling threshold	95	108	119	
	HDSEL[1:0] = 01	Rising threshold	109	121	132	
		Falling threshold	99	112	123	
	HDSEL[1:0] = 10	Rising threshold	113	125	136	
		Falling threshold	104	116	128	
	HDSEL[1:0] = 11	Rising threshold	117	130	143	
		Falling threshold	108	120	132	
Thermal shutdown threshold	Rising threshold	133	148	163	$^\circ\text{C}$	
	Falling threshold	111	123	135		
$I_{OOFF}$ Off ground current (two sensors on the die, specification for one sensor)	Device in OFF state, $V_{CCA} = 3.8\text{ V}$ , $T = 25^\circ\text{C}$			0.1	$\mu\text{A}$	
	Device in OFF state			0.5		
$I_{OON}$ On ground current (two sensors on the die, specification for one sensor)	Device in ACTIVE state, $V_{CCA} = 3.8\text{ V}$ , $T = 25^\circ\text{C}$		7	15	$\mu\text{A}$	
	Device in ACTIVE state, GPADC measurement		25	40		

## 4.12 Electrical Characteristics — System Control Thresholds

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POR (power-on reset) rising-edge threshold	Measured on VCCA pin	2.0	2.15	2.5	V
POR falling-edge threshold	Measured on VCCA pin	1.7	2	2.46	V
POR hysteresis	Rising edge to falling edge	40		300	mV
VSYS_LO, falling threshold, measured on VCCA pin	Voltage range, 50-mV steps	2.75		3.1	V
	Voltage accuracy	-50		95	mV
VSYS_LO hysteresis	Falling edge to rising edge	75		460	mV
VSYS_HI, measured on VCC_SENSE pin	Voltage range, 50-mV steps	2.9		3.85	V
	Voltage accuracy	-70		140	mV
VSYS_MON, measured on VCC_SENSE pin	Voltage range, 50-mV steps	2.75		4.6	V
	Voltage accuracy	-70		140	mV
VBUS detection (VBUS wake-up comparator threshold [plug detect])	Rising threshold	2.9		3.6	V
	Falling threshold	2.8		3.3	V

## 4.13 Electrical Characteristics — Current Consumption

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>OFF MODE</b>					
$I_{\text{OFF}}$ Device Off Mode Current Consumption	VCCA = 3.8 V, Device in OFF mode.		20	55	$\mu\text{A}$
<b>SLEEP MODE</b>					
$I_{\text{SLEEP}}$ Device Sleep Mode Current Consumption	VCCA = 3.8 V, PLL disabled, Device in Sleep mode. SMPS4 enabled in ECO mode, no load, all other external supply rails are disabled		90	150	$\mu\text{A}$

## 4.14 Electrical Characteristics — Digital Input Signal Parameters

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted). (VIO to refers to VIO\_IN pin, VSYS to refers to VCCA pin)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>PWRON</b>					
$V_{\text{IL(VSYS)}}$ Low-level input voltage related to VSYS (VCCA pin reference)		-0.3	0	$0.35 \times \text{VSYS}$	V
$V_{\text{IH(VSYS)}}$ High-level input voltage related to VSYS (VCCA pin reference)		$0.65 \times \text{VSYS}$	VSYS	$\text{VSYS} + 0.3 \leq 5.25$	V
Hysteresis related to VSYS		$0.025 \times \text{VSYS}$			V
<b>GPIO_2, GPIO_4, ENABLE1, I2C2_SCL_SCE, I2C2_SDA_SDO, I2C1_SCL_SCK, I2C1_SDA_SDI</b>					
$V_{\text{IL(VIO)}}$ Low-level input voltage related to VIO (VIO_IN pin reference)		-0.3	0	$0.3 \times \text{VIO}$	V
$V_{\text{IH(VIO)}}$ High-level input voltage related to VIO (VIO_IN pin reference)		$0.7 \times \text{VIO}$	VIO	$\text{VIO} + 0.3$	V
Hysteresis related to VIO		$0.045 \times \text{VIO}$			V
<b>BOOT, SYNCDCDC, ENABLE2, GPIO_0, GPIO_1, GPIO_3, GPIO_5, GPIO_6, NRESWARM, POWERHOLD, PWRDOWN, RESET_IN, NSLEEP</b>					
$V_{\text{IL(VRTC)}}$ Low-level input voltage related to VRTC		-0.3	0	$0.3 \times \text{VRTC}$	V
$V_{\text{IH(VRTC)}}$ High-level input voltage related to VRTC		$0.7 \times \text{VRTC}$	VRTC	$\text{VRTC} + 0.3$	V
Hysteresis related to VRTC		$0.05 \times \text{VRTC}$			V

## 4.15 Electrical Characteristics — Digital Output Signal Parameters

$T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , typical values are at  $T_A = 27^{\circ}\text{C}$  (unless otherwise noted). (VIO to refers to VIO\_IN pin, VSYS to refers to VCCA pin)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>GPIO_2, GPIO_4, REGEN2, INT, RESET_OUT</b>					
Low-level output voltage, push-pull and open-drain	$I_{OL} = 2\text{ mA}$			0.45	V
	$I_{OL} = 100\ \mu\text{A}$			0.2	
High-level output voltage, push-pull (VIO_IN pin reference)	$I_{OH} = 2\text{ mA}$	VIO – 0.45		VIO	V
	$I_{OH} = 100\ \mu\text{A}$	VIO – 0.2		VIO	
Supply for external pullup resistor, open drain				VIO	V
<b>SYNCLKOUT</b>					
$V_{OL(\text{SYNCLKOUT})}$ Low-level output voltage, push-pull	$I_{OL} = 1\text{ mA}$			0.45	V
	$I_{OL} = 100\ \mu\text{A}$			0.2	
$V_{OH(\text{SYNCLKOUT})}$ High-level output voltage, push-pull	$I_{OH} = 1\text{ mA}$	VRTC – 0.45		VRTC	V
	$I_{OH} = 100\ \mu\text{A}$	VRTC – 0.2		VRTC	
<b>GPIO_0, GPIO_1, GPIO_3, GPIO_5, REGEN1</b>					
Low-level output voltage, open-drain	External pullup to VRTC, $I_{OL} = 2\text{ mA}$			0.45	V
	External pullup to VRTC, $I_{OL} = 100\ \mu\text{A}$			0.2	
Supply for external pullup resistor, open-drain				5.25	V
<b>GPIO_6, POWERGOOD, REGEN3</b>					
Low-level output voltage, open-drain	External pullup to VRTC, $I_{OL} = 2\text{ mA}$			0.45	V
	External pullup to VRTC, $I_{OL} = 100\ \mu\text{A}$			0.2	
Supply for external pullup resistor, open-drain				VRTC	V
<b>I2C1_SDA_SDI, I2C2_SDA_SDO</b>					
$V_{OL(\text{VIO})}$ Low-level output voltage related to VIO (VIO_IN pin reference)	3-mA sink current		0.1 x VIO	0.2 x VIO	V
$C_B$ Capacitive load for I2C2_SDA_SDO	SPI Interface mode is selected			20	pF

## 4.16 I/O Pullup and Pulldown Characteristics

Over operating free-air temperature range (unless otherwise noted). (VIO to refers to VIO\_IN pin, VSYS to refers to VCCA pin)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
PWRON signal, fixed pullup	VSYS pullup supply	PULL UP	55	120	370	k $\Omega$
GPIO_0, GPIO_1, GPIO3, and GPIO5 signals	VRTC pullup supply	PULL DOWN	180	400	900	k $\Omega$
GPIO_2 and GPIO_4 signals	VIO pullup supply	PULL UP	170	400	1200	k $\Omega$
		PULL DOWN	170	400	950	
GPIO_6 signal	VRTC pullup supply	PULL UP	170	400	1200	k $\Omega$
		PULL DOWN	180	400	900	

## 4.17 Electrical Characteristics — I<sup>2</sup>C Interface

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_B$ Capacitive load for SDA and SCL				400	pF

## 4.18 Timing Requirements — I<sup>2</sup>C Interface

Over operating free-air temperature range, typical values are at T<sub>A</sub> = 27°C (unless otherwise noted). <sup>(1)(2)(3)(4)</sup>

		MIN	MAX	UNIT	
f <sub>(SCL)</sub>	SCL clock frequency	Standard mode	100	kHz	
		Fast mode	400	kHz	
		High-speed mode (write operation), C <sub>B</sub> – 100 pF max	3.4	MHz	
		High-speed mode (read operation), C <sub>B</sub> – 100 pF max	3.4	MHz	
		High-speed mode (write operation), C <sub>B</sub> – 400 pF max	1.7	MHz	
		High-speed mode (read operation), C <sub>B</sub> – 400 pF max	1.7	MHz	
t <sub>BUF</sub>	Bus free time between a stop (P) and start (S) condition	Standard mode	4.7	μs	
		Fast mode	1.3	μs	
t <sub>HD(STA)</sub>	Hold time (Repeated) start condition	Standard mode	4	μs	
		Fast mode	600	ns	
		High-speed mode	160	ns	
t <sub>LOW</sub>	Low period of the SCL clock	Standard mode	4.7	μs	
		Fast mode	1.3	μs	
		High-speed mode, C <sub>B</sub> – 100 pF max	160	ns	
		High-speed mode, C <sub>B</sub> – 400 pF max	320	ns	
t <sub>HIGH</sub>	High period of the SCL clock	Standard mode	4	μs	
		Fast mode	600	ns	
		High-speed mode, C <sub>B</sub> – 100 pF max	60	ns	
		High-speed mode, C <sub>B</sub> – 400 pF max	120	ns	
t <sub>SU(STA)</sub>	Setup time for a repeated start (Sr) condition	Standard mode	4.7	μs	
		Fast mode	600	ns	
		High-speed mode	160	ns	
t <sub>SU(DAT)</sub>	Data setup time	Standard mode	250	ns	
		Fast mode	100	ns	
		High-speed mode	10	ns	
t <sub>HD(DAT)</sub>	Data hold time	Standard mode	0	3.45	μs
		Fast mode	0	0.9	μs
		High-speed mode, C <sub>B</sub> – 100 pF max	0	70	ns
		High-speed mode, C <sub>B</sub> – 400 pF max	0	150	ns
t <sub>RCL</sub>	Rise time of the SCL signal	Standard mode	20 + 0.1 C <sub>B</sub>	1000	ns
		Fast mode	20 + 0.1 C <sub>B</sub>	300	ns
		High-speed mode, C <sub>B</sub> – 100 pF max	10	40	ns
		High-speed mode, C <sub>B</sub> – 400 pF max	20	80	ns
t <sub>RCL1</sub>	Rise time of the SCL signal after a Repeated Start condition and after an acknowledge bit	Standard mode	20 + 0.1 C <sub>B</sub>	1000	ns
		Fast mode	20 + 0.1 C <sub>B</sub>	300	ns
		High-speed mode, C <sub>B</sub> – 100 pF max	10	80	ns
		High-speed mode, C <sub>B</sub> – 400 pF max	20	160	ns

(1) Specified by design. Not tested in production.

(2) All values referred to V<sub>IHmin</sub> and V<sub>IHmax</sub> levels.

(3) For bus line loads C<sub>B</sub> between 100 and 400 pF, the timing parameters must be linearly interpolated.

(4) A device must internally provide a data hold time to bridge the undefined part between V<sub>IH</sub> and V<sub>IL</sub> of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

## Timing Requirements — I<sup>2</sup>C Interface (continued)

Over operating free-air temperature range, typical values are at T<sub>A</sub> = 27°C (unless otherwise noted). (1)(2)(3)(4)

		MIN	MAX	UNIT	
t <sub>FCL</sub>	Fall time of the SCL signal	Standard mode	20 + 0.1 C <sub>B</sub>	300	ns
		Fast mode	20 + 0.1 C <sub>B</sub>	300	ns
		High-speed mode, C <sub>B</sub> – 100 pF max	10	40	ns
		High-speed mode, C <sub>B</sub> – 400 pF max	20	80	ns
t <sub>RDA</sub>	Rise time of the SDA signal	Standard mode	20 + 0.1 C <sub>B</sub>	1000	ns
		Fast mode	20 + 0.1 C <sub>B</sub>	300	ns
		High-speed mode, C <sub>B</sub> – 100 pF max	10	80	ns
		High-speed mode, C <sub>B</sub> – 400 pF max	20	160	ns
t <sub>FDA</sub>	Fall time of the SDA signal	Standard mode	20 + 0.1 C <sub>B</sub>	300	ns
		Fast mode	20 + 0.1 C <sub>B</sub>	300	ns
		High-speed mode, C <sub>B</sub> – 100 pF max	10	80	ns
		High-speed mode, C <sub>B</sub> – 400 pF max	20	160	ns
t <sub>SU(STO)</sub>	Setup time for a stop condition	Standard mode	4		μs
		Fast mode	600		ns
		High-speed mode	160		ns

## 4.19 Timing Requirements — SPI

See [4-3](#) for the SPI timing diagram.

		MIN	MAX	UNIT
t <sub>cesu</sub>	Chip-select set up time	30		ns
t <sub>cehld</sub>	Chip-select hold time	30		ns
t <sub>ckper</sub>	Clock cycle time	67	100	ns
t <sub>ckhigh</sub>	Clock high typical pulse duration	20		ns
t <sub>cklow</sub>	Clock low typical pulse duration	20		ns
t <sub>sisu</sub>	Input data set up time, before clock active edge	5		ns
t <sub>sihld</sub>	Input data hold time, after clock active edge	5		ns
t <sub>dr</sub>			15	ns
t <sub>CE</sub>	Time from CE going low to CE going high	67		ns
	Capacitive load on pin SDO		30	pF

## 4.20 Switching Characteristics — LDO Regulators

Over operating free-air temperature range, typical values are at T<sub>A</sub> = 27°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T <sub>on</sub>	Turn-on time	I <sub>OUT</sub> = 0, V <sub>OUT</sub> = 0.1 V up to V <sub>OUTmin</sub>	100	500	μs
T <sub>off</sub>	Turn-off time (except VRTC)	I <sub>OUT</sub> = 0, V <sub>OUT</sub> down to 10% × V <sub>OUT</sub>	250	500	μs

## 4.21 Switching Characteristics — SMPS1&2 in Dual-Phase Configuration

Over operating free-air temperature range, typical values are at T<sub>A</sub> = 27°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
f <sub>SW</sub>	Switching frequency	PWM mode	1.7	2.2	2.7	MHz
T <sub>start</sub>	Time from enable to the start of the ramp		240		μs	
T <sub>ramp</sub>	Time from enable to 80% of V <sub>OUT</sub>	C <sub>OUT</sub> < 57 μF per phase, no load	400	1000	μs	

#### 4.22 Switching Characteristics — SMPS1, SMPS2, SMPS3, and SMPS4 Stand-Alone Regulators

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{\text{SW}}$	Switching frequency	In PWM mode	1.7	2.2	2.7	MHz
$T_{\text{start}}$	Time from enable to the start of the ramp			150		$\mu\text{s}$
$T_{\text{ramp}}$	Time from enable to 80% of $V_{\text{OUT}}$	$C_{\text{OUT}} < 57 \mu\text{F}$ per phase, no load		400	1000	$\mu\text{s}$

#### 4.23 Switching Characteristics — Reference Generator (Bandgap)

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time			1	3	ms

#### 4.24 Switching Characteristics — PLL for SMPS Clock Generation

Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
$f_{\text{SYNC}}$	Synchronization range of SYNCDCDC clock	1.7	2.2	2.7	MHz	
$A_{\text{DITHER}}$	Dither amplitude of SYNCDCDC clock			128	kHz	
$M_{\text{DITHER}}$	Dither slope of SYNCDCDC clock			1.35	kHz/ $\mu\text{s}$	
$f_{\text{FALLBACK}}$	Fallback frequency	$V_{\text{CCA}} = 5.25 \text{ V}$	1.98	2.2	2.42	MHz
		$V_{\text{CCA}} = 3.8 \text{ V}$	1.9	2.2	2.42	
		$V_{\text{CCA}} = 3.135 \text{ V}$	1.9	2.2	2.42	
$f_{\text{SAT,LO}}$	The low saturation frequency of the PLL	1.35		1.68	MHz	
$f_{\text{SAT,HI}}$	The high saturation frequency of the PLL	2.8		3.8	MHz	
$t_{\text{SETTLE}}$	Settling time	Time from initial application or removal of sync clock until PLL output has settled to 1% of the final value			100	$\mu\text{s}$
$f_{\text{ERROR}}$	Frequency error	The steady-state percent of difference between $f_{\text{SYNC}}$ and the switching frequency			-1%	1%

#### 4.25 Switching Characteristics — 32-kHz RC Oscillators and SYNCCLKOUT Output Buffers

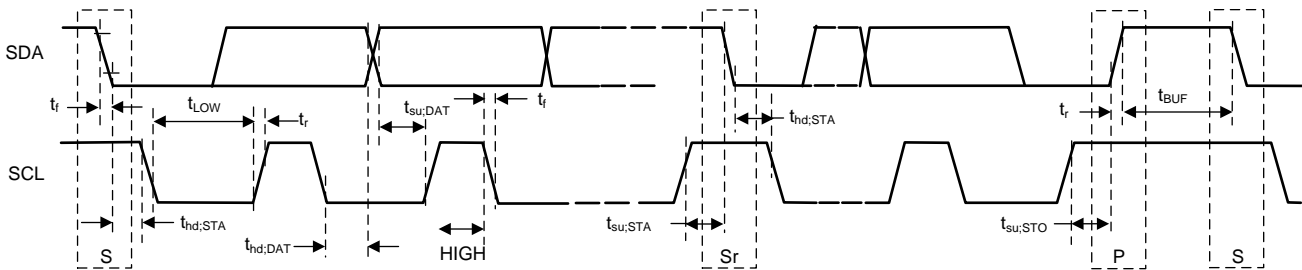
Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>32-kHz RC OSCILLATOR</b>					
Output frequency low-level output voltage			32768		Hz
Output frequency accuracy	After trimming at $27^\circ\text{C}$	-10%	0%	10%	
Cycle jitter (RMS)				10%	
Output duty cycle		40%	50%	60%	
Settling time				150	$\mu\text{s}$
<b>SYNCCLKOUT OUTPUT BUFFER</b>					
Rise and fall time	$C_L = 35 \text{ pF}$ , 10% to 90%	5	20	100	ns
Duty cycle	Logic output signal	40%	50%	60%	

### 4.26 Switching Characteristics — 12-Bit Sigma-Delta ADC

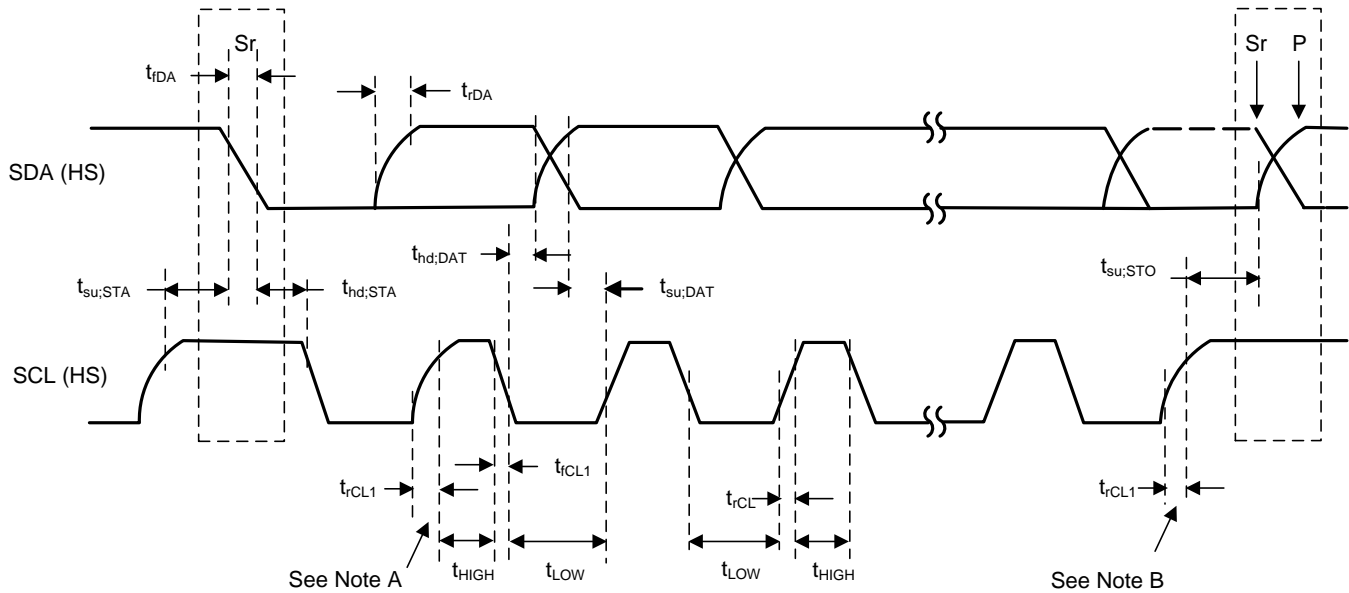
Over operating free-air temperature range, typical values are at  $T_A = 27^\circ\text{C}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Turn-on time	Active or sleep with VANA ON and RC15MHZ_ON_IN_SLEEP = 1 or sleep with GPADC_FORCE = 1		0		$\mu\text{s}$
	Sleep or OFF		794		
	Sleep with VANA enabled		282		
Conversion time	1 channel, EXTEND_DELAY = 0		113		$\mu\text{s}$
	1 channel, EXTEND_DELAY = 1		563		
	2 channels		223		



Note: S = Start; Sr = Repeated start; P = Stop

4-1. Serial Interface Timing Diagram For F/S Mode



See Note A

See Note B

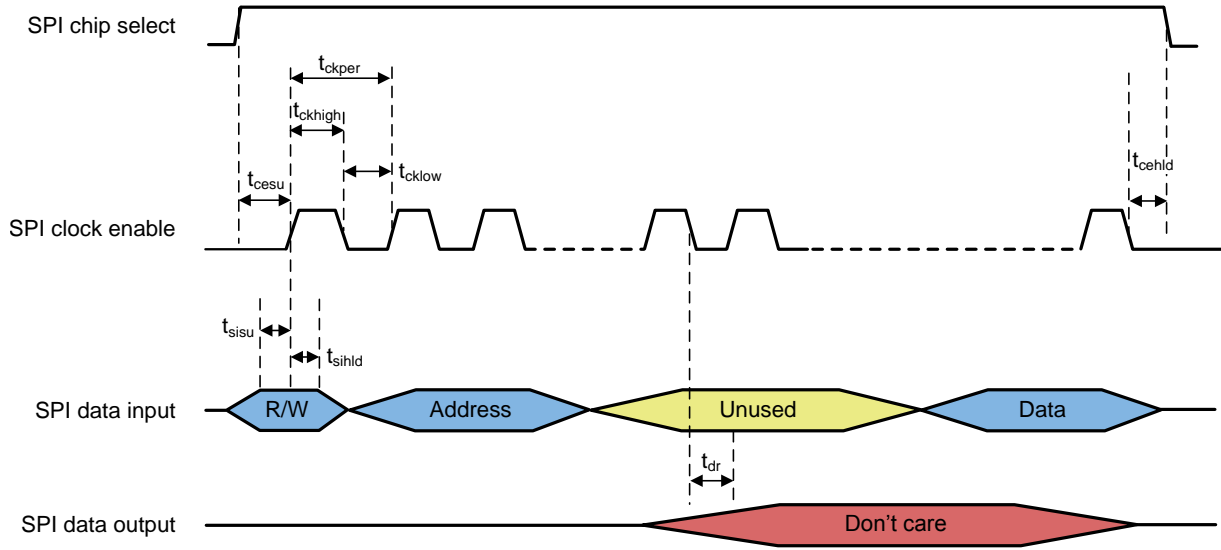
= MCS Current Source Pullup

=  $R_{(P)}$  Resistor Pullup

- A. First rising edge of the SCL (HS) signal after Sr and after each acknowledge bit.
- B. Sr = Repeated start; P = Stop

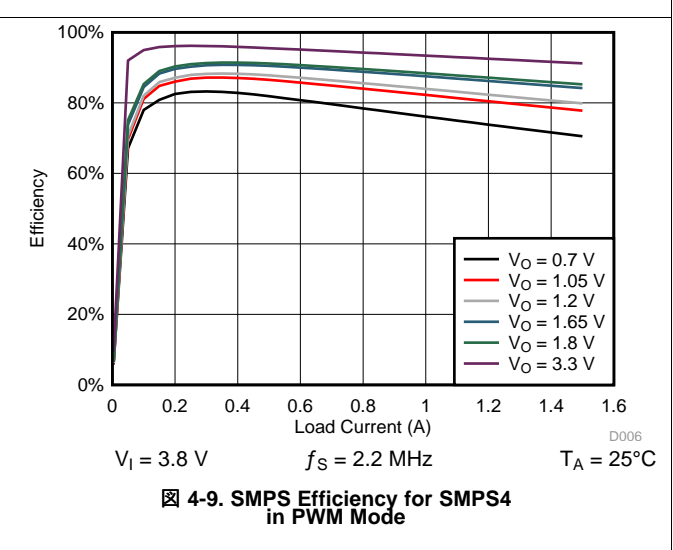
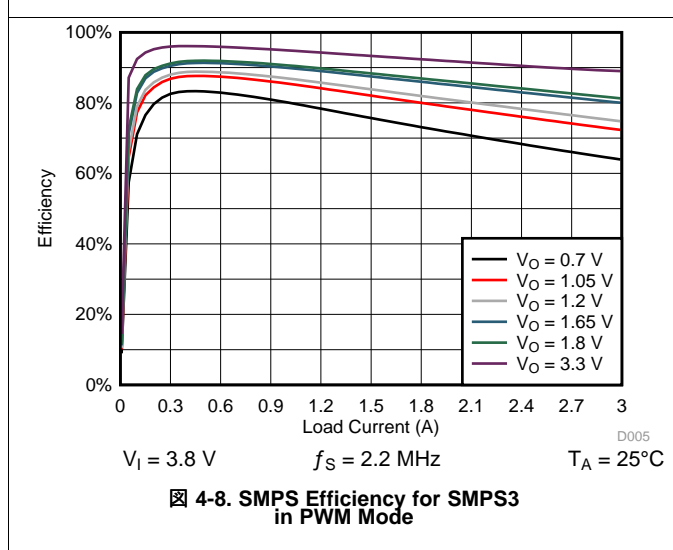
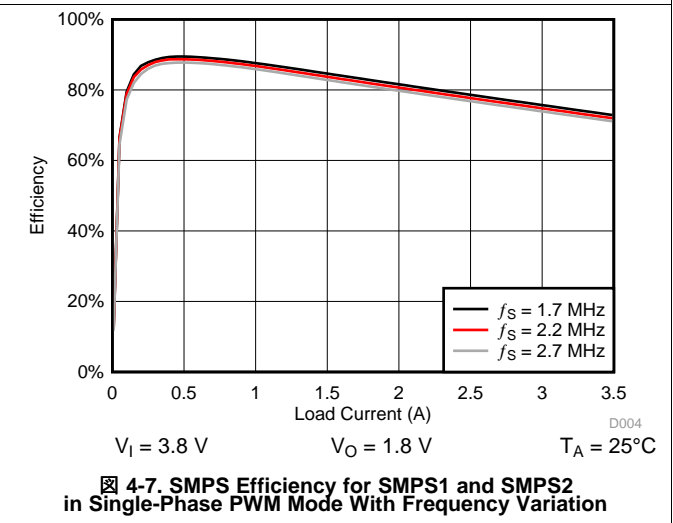
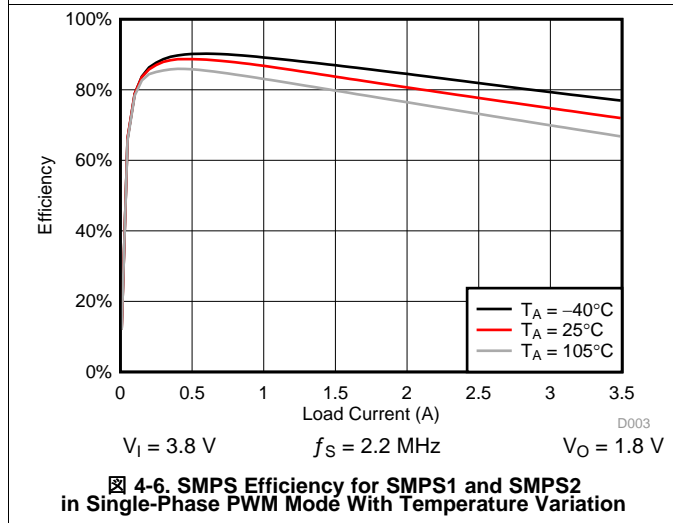
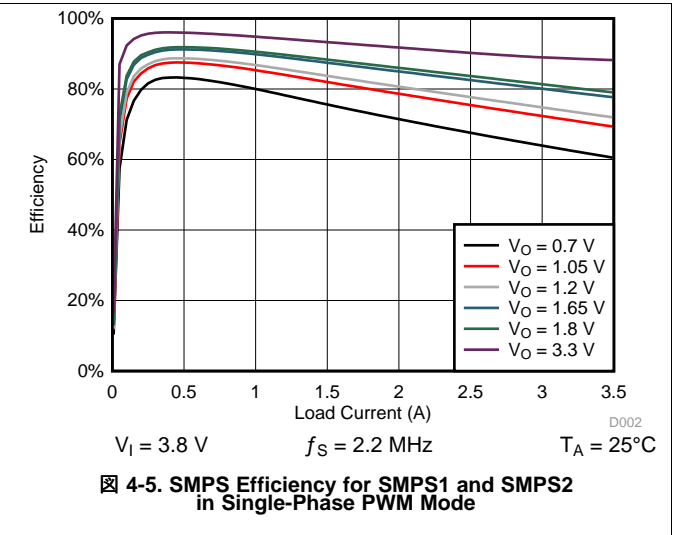
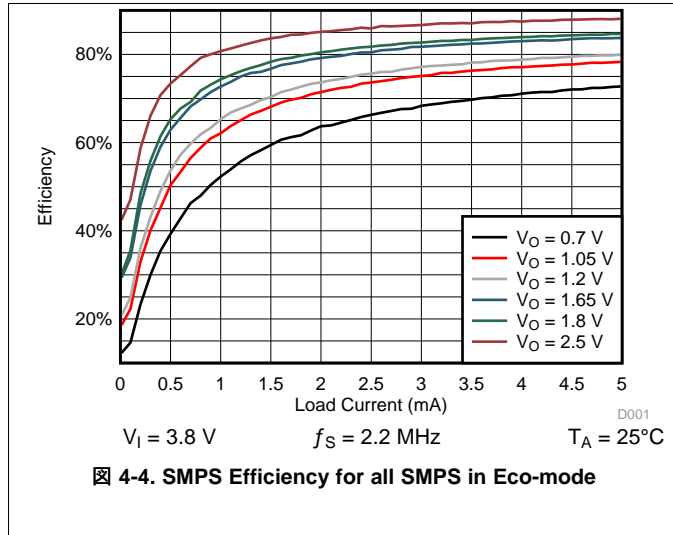
4-2. Serial Interface Timing Diagram For HS Mode



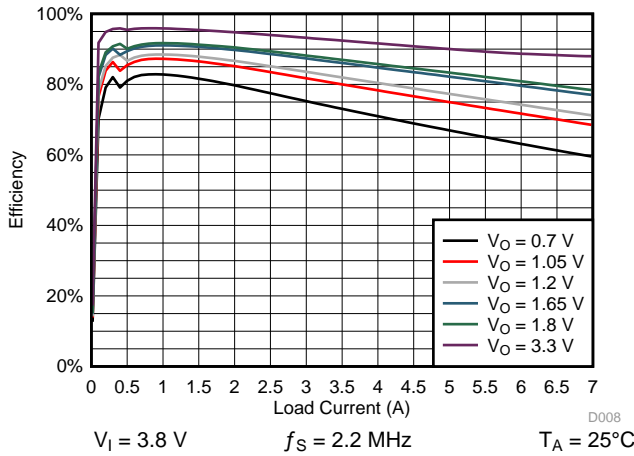


4-3. SPI Timings  
See Section 4.19 for the Timing Parameters

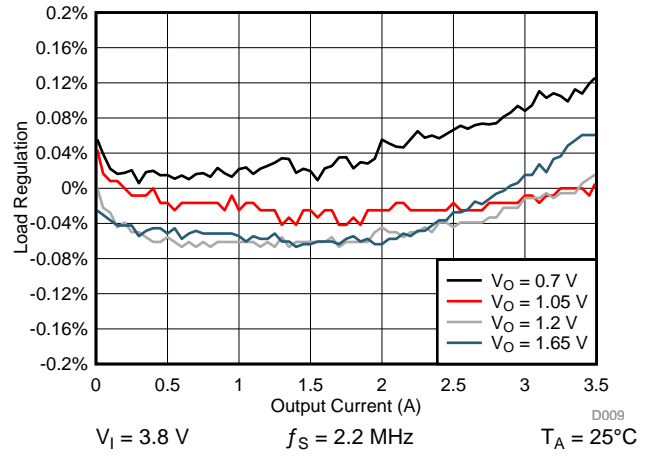
### 4.27 Typical Characteristics



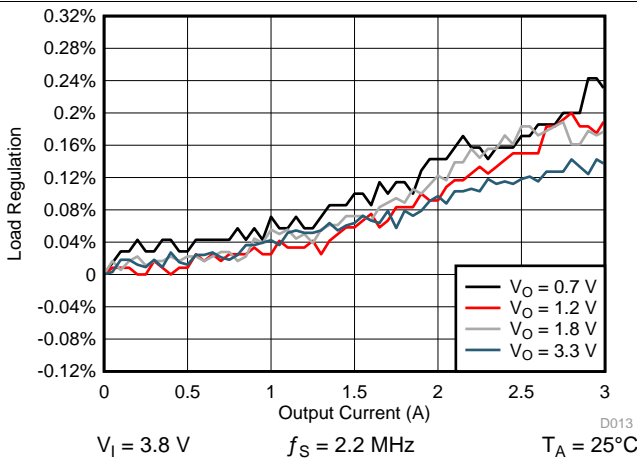
Typical Characteristics (continued)



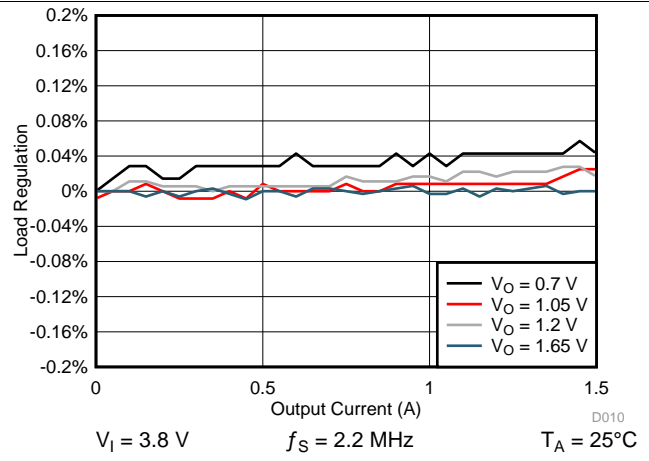
4-10. SMPS Efficiency for SMPS12 in Dual-Phase PWM Mode



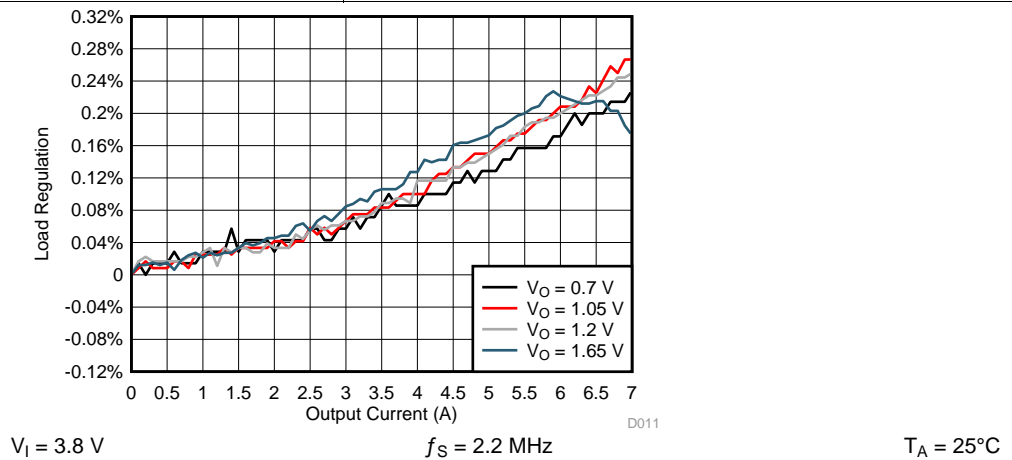
4-11. SMPS Load Regulation for SMPS1 and SMPS2 Single-Phase PWM Mode



4-12. SMPS Load Regulation for SMPS3, PWM Mode



4-13. SMPS Load Regulation for SMPS4 in PWM Mode



4-14. SMPS Load Regulation for SMPS12 in Dual-Phase PWM Mode

## 5 Detailed Description

### 5.1 Overview

The TPS65919-Q1 device is an integrated power-management integrated circuit (PMIC), available in a 48-pin, 0.5-mm pitch, 7-mm × 7-mm QFN package. It provides five configurable step-down converter rails, with two of the rails having the ability to combine power rails and supply up to 7A of output current in multi-phase mode. The TPS65919-Q1 device also provides five external LDO rails. It also comes with a 12-bit GPADC with two external channels, seven configurable GPIOs, two I<sup>2</sup>C interface channels or one SPI interface channel, PLL for external clock sync and phase delay capability, and programmable power sequencer and control for supporting different processors and applications.

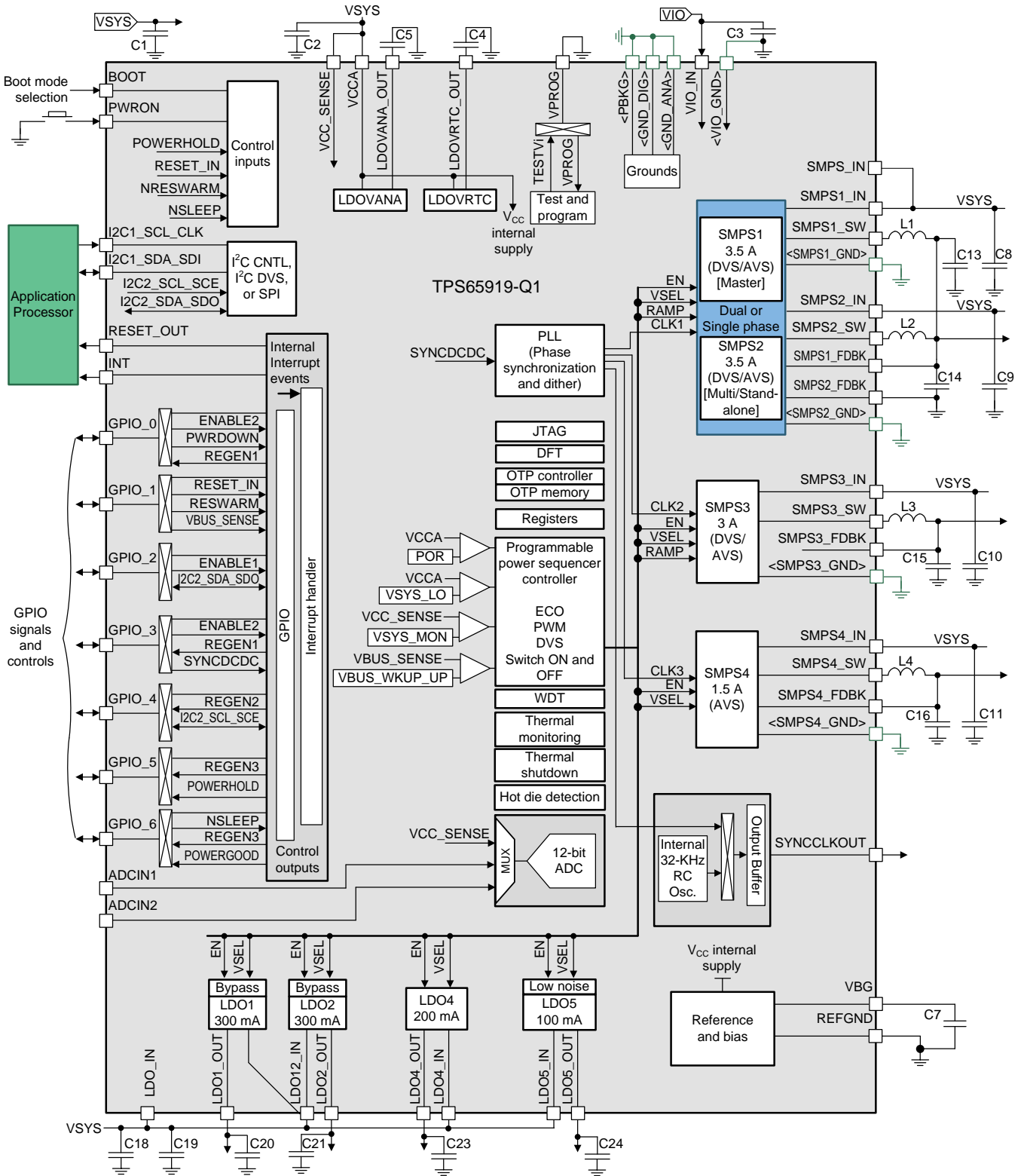
The five step-down converter rails are consisting of five high frequency switch mode converters with integrated FETs. They are capable of synchronizing to an external clock input and supports switching frequency between 1.7 MHz and 2.7 MHz. The SMPS1 and SMPS2 can combine in dual phase configuration to supply up to 7 A. In addition, SMPS1, SMPS2, and SMPS3 support dynamic voltage scaling by a dedicated I<sup>2</sup>C interface for optimum power savings.

The five LDOs support 0.9 V to 3.3 V output with 50-mV step. The LDOs can be supplied from either a system supply or a pre-regulated supply. All LDOs and step-down converters can be controlled by the SPI or I<sup>2</sup>C interface, or by power request signals. In addition, voltage scaling registers allow transitioning the SMPS to different voltages by SPI, I<sup>2</sup>C, or roof and floor control.

The power-up and power-down controller is configurable and programmable through OTP. The TPS65919-Q1 device includes a 32-kHz RC oscillator to sequence all resources during power up and power down. An internal LDOVRTC generates the supply for the entire digital circuitry of the device as soon as the VSYS supply is available through the VCCA input.

Configurable GPIOs with multiplexed feature are available on the TPS65919-Q1 device. The GPIOs can be configured and used as enable signals for external resources, which can be included into the power-up and power-down sequence. The general-purpose (GP) sigma-delta analog-to-digital converter (ADC) with two external input channels included in this device can be used as thermal or voltage and current monitors.

## 5.2 Functional Block Diagram



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### 5.3 Device State Machine

The TPS65919-Q1 device integrates an embedded power controller (EPC) that fully manages the state of the device during power transitions. According to the four defined types of requests (ON, OFF, WAKE, and SLEEP), the EPC executes one of the five predefined power sequences (OFF2ACT, ACT2OFF, SLP2OFF, ACT2SLP, and SLP2ACT) to control the state of the device resources. Any resource can be included in any power sequence. When a resource is not controlled or configured through a power sequence, the resource is left in the default state as pre-programmed by the OTP.

Each resource is only configured through register bits. Therefore, the user can statically control the resource through the control interfaces (I<sup>2</sup>C or SPI), or the EPC can automatically control the resource during power transitions which are predefined sequences of registers accesses.

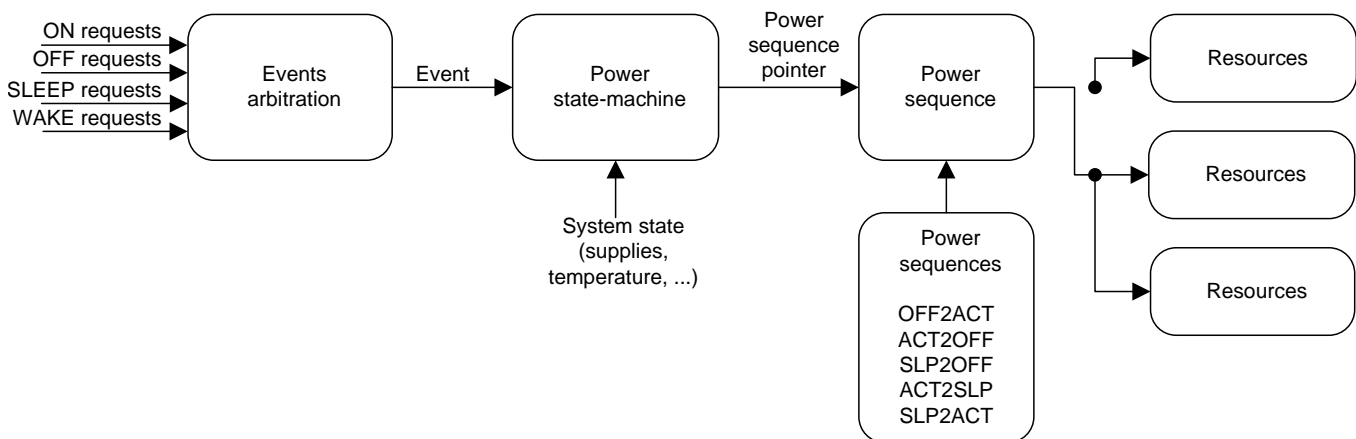
The EPC is powered by an internal LDO which is automatically enabled when VSYS is available to the device. Ensuring that the VSYS pin (which is connected to VCCA, VCC\_SENSE, SMPSx\_In and LDOx\_IN as suggested in the device block diagram) is the first supply available to the device is important to ensure proper operation of all the power resources provided by the device. Ensuring that the VSYS pin is stable prior to the VIO supply becoming available is important to ensure proper operation of the control interface and device IOs.

#### 5.3.1 Embedded Power Controller

The EPC is composed of the following three main modules:

- An event arbitration module that is used to prioritize ON, OFF, WAKE, and SLEEP requests.
- A power state-machine that is used to determine which power sequence to execute based on the system state (supplies, temperature, and so forth) and requested transition (from the event arbitration module).
- A power sequencer that fetches the selected power sequence from OTP and executes the sequence. The power sequencer sets up and controls all resources accordingly, based on the definition of each sequence.

✎ 5-1 shows the EPC block diagram.



✎ 5-1. EPC Block Diagram

The power state-machine is defined through the following states:

**NO SUPPLY** The device is not powered by a valid energy source on the system power rail ( $V_{CCA} < POR$ ).

**BACKUP** The device is powered by a valid supply on the system power rail which is above power-on reset (POR) threshold but below the system low threshold ( $POR < V_{CCA} < V_{SYS\_LO}$ ).

**OFF** The device is powered by a valid supply on the system power rail ( $V_{CCA} > V_{SYS\_LO}$ ) and is waiting for a start-up event or condition. All device resources, except VRTC, are in the

OFF state.

**ACTIVE** The device is powered by a valid supply on the system power rail ( $VCC\_SENSE > VSYS\_HI$ ) and has received a start-up event. The device has switched to the ACTIVE state and has full capacity to supply the processor and other platform modules.

**SLEEP** The device is powered by a valid supply on the system power rail ( $VCCA > VSYS\_LO$ ) and is in low-power mode. All configured resources are set to the low-power mode, which can be ON, SLEEP, or OFF depending on the specific resource setting. If a given resource is maintained active (ON) during low-power mode, then all linked subsystems are automatically maintained active.

Figure 5-2 shows the state diagram for the power control state-machine.

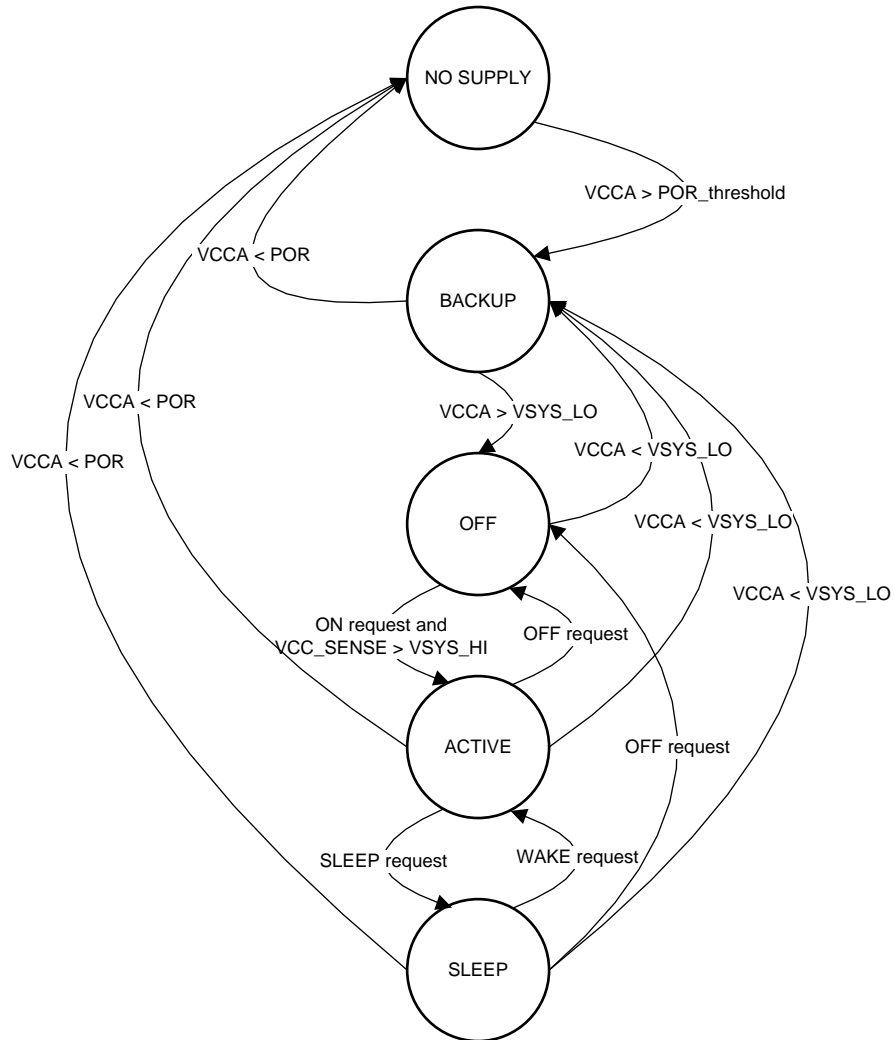


Figure 5-2. State Diagram for the Power Control State-Machine

Power sequences define how a resource state switches between the OFF, ACTIVE, and SLEEP states, but these sequences have no effect during the NO SUPPLY or BACKUP states. When the device is brought into the OFF state from a NO SUPPLY or BACKUP state, internal hardware manages the state transition automatically before the EPC takes control of the device power sequencing as the device arrives the OFF state.

The allowed power transitions include the following:

- OFF to ACTIVE (OFF2ACT)
- ACTIVE to OFF (ACT2OFF)

- ACTIVE to SLEEP (ACT2SLP)
- SLEEP to ACTIVE (SLP2ACT)
- SLEEP to OFF (SLP2OFF)

Each power transition consists of a sequence of one or several register accesses that controls the resources according to the EPC supervision. Because these sequences are stored in nonvolatile memory (OTP), these sequences cannot be altered.

An error detection routine of the OTP bit integrity is available with this device. If enabled, this routine is executed to compare the current OTP values with the preprogrammed values at the beginning of every OFF2ACT power sequence. When an OTP bit integrity error is detected, the OTP register, CRC\_CONTROL, can be preprogrammed to select the following options:

- *Skip Error Detection* and execute all power sequence
- *Execute Error Detection* and execute all power-up sequence, even if an error is detected
- *Execute Error Detection*. If an error is detected, execute power-up sequence until the VIO supply rail is up
- *Execute Error Detection*. If an error is detected, stop power-up sequence altogether

When an error is detected, an interrupt (INT2.OTP\_ERROR) is sent to the host processor regardless of the CRC\_CONTROL setting.

## 5.3.2 State Transition Requests

### 5.3.2.1 ON Requests

ON requests are used to switch on the device, which transitions the device from the OFF to the ACTIVE state. 表 5-1 lists the ON requests.

表 5-1. ON Requests

EVENT	MASKABLE	POLARITY	COMMENT	DEBOUNCE
PWRON (pin)	No	Low	Level sensitive	N/A
Part of interrupts (event)	Yes (INTx_MASK register. Default: Masked)	Event	Edge sensitive	N/A
POWERHOLD (pin)	No	High	Level sensitive	3 - 5 ms typical

If one of the events listed in 表 5-1 occurs, the event powers on the device unless one of the gating conditions listed in 表 5-2 is present. 表 5-12 lists interrupt sources that can be configured as ON requests.

表 5-2. ON Requests Gating Conditions

EVENT	MASKABLE	POLARITY	COMMENT
VSYS_HI (event)	No	Low	VCC_SENSE < VSYS_HI
HOTDIE (event)	No	High	Device temperature exceeds the HOTDIE level
PWRDOWN (pin)	No	OTP configurable	—
RESET_IN (pin)	No	OTP configurable	—

### 5.3.2.2 OFF Requests

OFF requests are used to switch off the device, meaning a transition from SLEEP or ACTIVE to OFF state. 表 5-3 lists the OFF requests. OFF requests have the highest priority, which means these requests have no gating conditions. Any OFF request is executed even though a valid SLEEP or ON request is present. The device goes to the OFF state and then, when the OFF request is cleared, the device reacts to an ON request, if one occurs.



**表 5-3. OFF Requests**

EVENT	MASKABLE	POLARITY	DEBOUNCE	SWITCH OFF DELAY <sup>(1)</sup>	RESET LEVEL <sup>(2)</sup>	RESET SEQUENCE <sup>(3)</sup>
PWRON (pin) (long press key)	No	Low	LPK_TIME (OTP)	SWOFF_DLY	OTP configurable	OTP configurable
PWRDOWN (pin)	No	OTP configurable		SWOFF_DLY	OTP configurable	OTP configurable
WATCHDOG TIMEOUT <sup>(4)</sup> (internal event)	N/A	N/A	N/A	SWOFF_DLY	OTP configurable	OTP configurable
THERMAL SHUTDOWN (internal event)	No	N/A	N/A	0	OTP configurable	OTP configurable
RESET_IN (pin)	No	OTP configurable	1 ms for ACT2OFF 26 ms for OFF2ACT	SWOFF_DLY	OTP configurable	OTP configurable
SW_RST (register bit)	No	N/A	N/A	0	OTP configurable	OTP configurable
DEV_ON <sup>(5)</sup> (register bit)	No	N/A	N/A	0	SWORST	SD
VSYS_LO (internal event)	No	N/A		0	OTP configurable	OTP configurable
POWERHOLD <sup>(6)</sup> (pin)	No	Low		0	SWORST	SD
GPADC_SHUTDOWN	Yes	N/A	N/A	SWOFF_DLY	OTP configurable	OTP configurable

- (1) SWOFF\_DLY is the same for all requests. When configured (in the PMU\_CONFIG register) to a specific value (0, 1, 2, or 4 s), the value is applied to all OFF requests.
- (2) The reset level is selectable as HWRST (a wide set of registers is reset to default values) or SWORTS (a more limited set of registers is reset). See 5.3.7.
- (3) The OFF requests in the reset sequence are configured to force the EPC to execute either a shutdown (SD) or a cold restart (CR). Configuration occurs in the SWOFF\_COLDTRST register.
  - When configured to generate a shutdown, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and remains in the OFF state.
  - When configured to generate a cold restart, the EPC executes a transition to the OFF state (SLP2OFF or ACT2OFF power sequence) and restarts, transitioning to the ACTIVE state (OFF2ACT power sequence) if none of the ON request gating conditions are present.
- (4) The watchdog is disabled by default. Software can enable watchdog and lock (write protect) watchdog register (WATCHDOG).
- (5) The DEV\_ON event has a lower priority than other ON events, meaning that DEV\_ON forces the device to go to the OFF state only if no other ON conditions keep the device active (POWERHOLD).
- (6) The POWERHOLD event has a lower priority than other ON events, meaning that POWERHOLD forces the device to go to the OFF state only if no other ON conditions keep the device active (DEV\_ON).

### 5.3.2.3 SLEEP and WAKE Requests

The device transitions from the ACTIVE to the SLEEP state after receiving a SLEEP request. Upon this request, internal resources as well as user-defined resources will enter the low-power mode as predefined by the user. The states of the resources during ACTIVE and SLEEP states are defined in the LDO\*\_CTRL and SMPSx\_CTRL registers.

表 5-4 lists the SLEEP requests. Any of these events trigger the ACT2SLP sequence unless pending interrupts (unmasked) are present. Once the device enters the SLEEP state, only an interrupt or an NSLEEP signal can generate a WAKE request to wake up the device (exit from the SLEEP state). A WAKE request (only during the SLEEP state) wakes up the device and triggers a SLP2ACT or a SLP2OFF power sequence.

**表 5-4. SLEEP Requests**

EVENT	MASKABLE	POLARITY	COMMENT
NSLEEP (pin)	Yes (Default: Masked)	Low	Level sensitive

For each resource, a transition from the ACTIVE state to the SLEEP state or from the SLEEP state to the ACTIVE state is controlled in two different ways which are described as follows:

- Through EPC sequencing (ACT2SLP or SLP2ACT power sequence) when the resource is associated to the NSLEEP signal.

- Through direct control of the resource power mode (ACTIVE or SLEEP) in which case the user can bypass SLEEP and WAKE sequencing by having resources assigned to two external control signals (ENABLE1 and ENABLE2). These signals have a direct control on the power modes (ACTIVE or SLEEP) of any resources associated to them and they trigger an immediate switch from one mode to the other, regardless of the EPC sequencing.

Therefore, all resources can be associated to three external pins (NSLEEP, ENABLE1, and ENABLE2) and can switch between the SLEEP and ACTIVE states. 表 5-5 outlines the type of state transition each resource undergoes according to the logic combination of the NSLEEP, ENABLE1 and ENABLE2 assignments.

表 5-5. Resources SLEEP and ACTIVE Assignments<sup>(1)</sup>

ENABLE1 ASSIGNMENT	ENABLE2 ASSIGNMENT	NSLEEP ASSIGNMENT	ENABLE1 PIN STATE	ENABLE2 PIN STATE	NSLEEP PIN STATE	STATE	TRANSITION
0	0	0	Don't care	Don't care	Don't care	ACTIVE	None
0	0	1	Don't care	Don't care	0 ↔ 1	SLEEP ↔ ACTIVE	Sequenced
0	1	0	Don't care	0 ↔ 1	Don't care	SLEEP ↔ ACTIVE	Immediate
0	1	1	Don't care	0	0 ↔ 1	SLEEP ↔ ACTIVE	Sequenced
				1	0 ↔ 1	ACTIVE	None
				0 ↔ 1	0	SLEEP ↔ ACTIVE	Immediate
				0 ↔ 1	1	ACTIVE	None
1	0	0	0 ↔ 1	Don't care	Don't care	SLEEP ↔ ACTIVE	Immediate
1	0	1	Don't care	0	0 ↔ 1	SLEEP ↔ ACTIVE	Sequenced
				1	0 ↔ 1	ACTIVE	None
				0 ↔ 1	0	SLEEP ↔ ACTIVE	Immediate
				0 ↔ 1	1	ACTIVE	None
1	1	0	Don't care	0	0 ↔ 1	SLEEP ↔ ACTIVE	Immediate
				1	0 ↔ 1	ACTIVE	None
				0 ↔ 1	0	SLEEP ↔ ACTIVE	Immediate
				0 ↔ 1	1	ACTIVE	None
1	1	1	0	0	0 ↔ 1	SLEEP ↔ ACTIVE	Sequenced
			0	1	0 ↔ 1	ACTIVE	None
			1	0	0 ↔ 1	ACTIVE	None
			1	1	0 ↔ 1	ACTIVE	None
			0	0 ↔ 1	0	SLEEP ↔ ACTIVE	Immediate
			0	0 ↔ 1	1	ACTIVE	None
			1	0 ↔ 1	0	ACTIVE	None
			1	0 ↔ 1	1	ACTIVE	None
			0 ↔ 1	0	0	SLEEP ↔ ACTIVE	Immediate
			0 ↔ 1	0	1	ACTIVE	None
			0 ↔ 1	1	0	ACTIVE	None
			0 ↔ 1	1	1	ACTIVE	None

(1) Notes:

- The polarity of the NSLEEP, ENABLE1, and ENABLE2 signals is configurable through the POLARITY\_CTRL register. By default:
  - ENABLE1 and ENABLE2 are active high, meaning a transition from 0 to 1 requests a transition from SLEEP state to ACTIVE state.
  - NSLEEP is active low, meaning a transition from 1 to 0 requests a transition from ACTIVE state to SLEEP state.
- Resource assignments to the NSLEEP, ENABLE1, and ENABLE2 signals are configured in the ENABLEx\_YYY\_ASSIGN and NSLEEP\_YYY\_ASSIGN registers (where x = 1 or 2 and YYY = RES, SMPS, or LDO).
- Several resources can be assigned to the same ENABLE signal (ENABLE1 or ENABLE2) and therefore, when triggered, they all switch their power mode at the same time.
- When resources are assigned only to the NSLEEP signal, the respective switching order is controlled and defined in the power sequence.
- When a resource is not assigned to any signal (NSLEEP, ENABLE1, or ENABLE2), it never switches from the ACTIVE state to the SLEEP state. The resource always remains in ACTIVE mode.

### 5.3.3 Power Sequences

A power sequence is an automatic preprogrammed sequence the TPS65919-Q1 device configures its resources, which include the states of the SMPSs, LDOs, 32-kHz clock, and part of the GPIOs (REGEN signals). For a detailed description of the GPIOs signals, please refer to 5.9.

Figure 5-3 shows an example of an OFF2ACT transition followed by an ACT2OFF transition. The sequence is triggered through PWRON pin and the resources controlled (for this example) are: SMPS3 (VIO), LDO1, SMPS2, LDO2, REGEN1, and LDO5. The time between each resource enable and disable (TinstX) is also part of the preprogrammed sequence definition.

When a resource is not assigned to any power sequence, it remains in off mode. The user (through software) can enable and configure this resource independently when the power sequence completes.

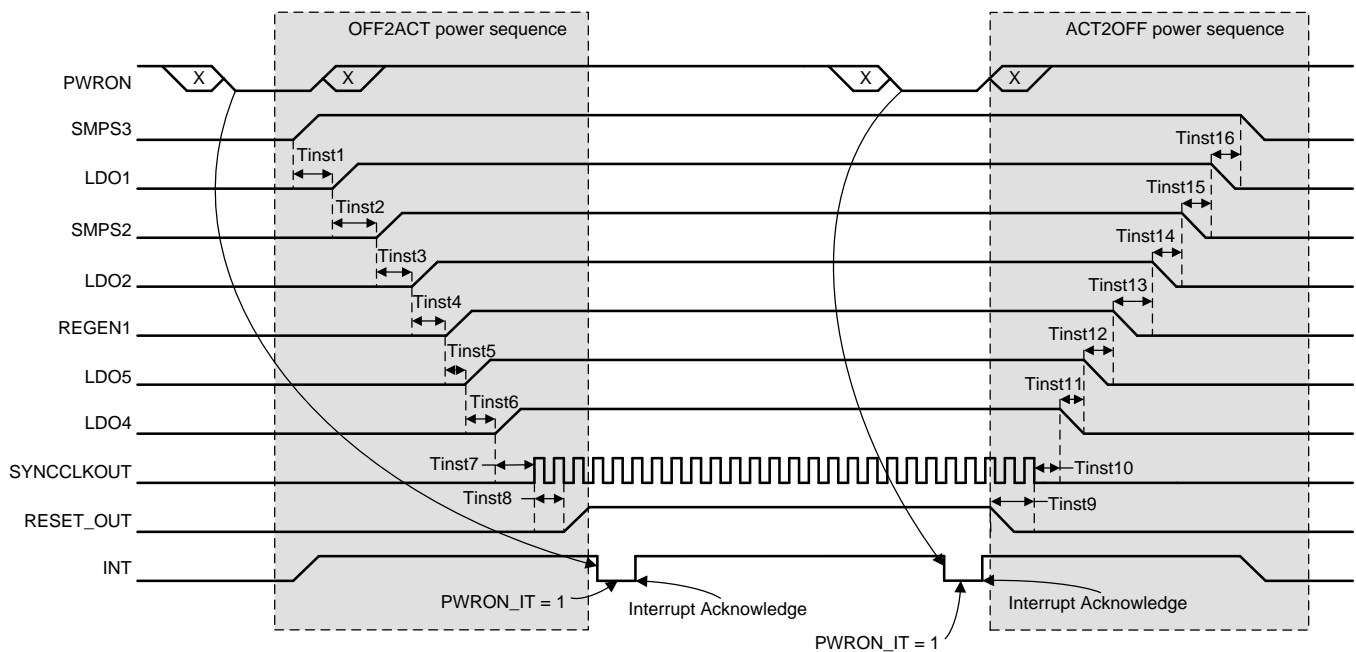


Figure 5-3. Power Sequence Example

As the power sequences of the TPS65919-Q1 device are defined according to the processor requirements, the total time for the completion of the power sequence will vary across various system definitions.

### 5.3.4 Device Power Up Timing

Figure 5-4 shows the timing diagram of the TPS65919-Q1 after the first supply detection.

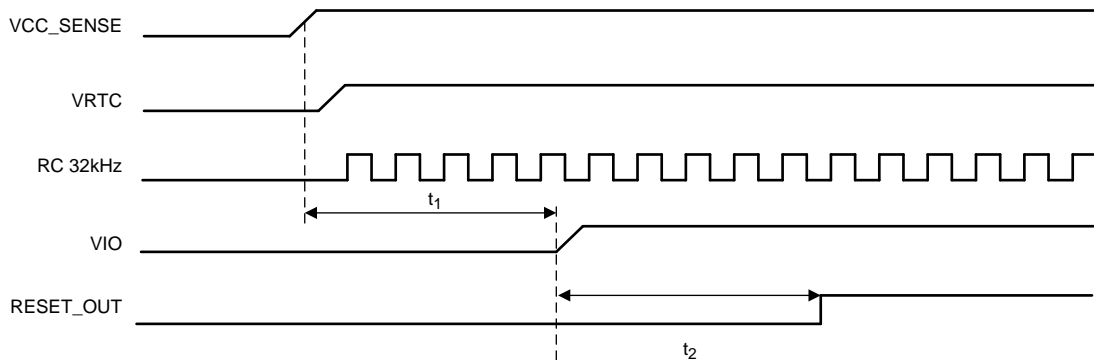


Figure 5-4. TPS65919-Q1 Power-Up Sequence After FSD

The time  $t_1$  is the delay from VCC crossing the POR threshold to VIO rising up. The time  $t_1$  must be at least 6 ms. If the time from VCC to VIO is less than 6 ms, the VIO buffers will be supplied while the OTP is still being initialized, which could cause glitches on any VIO output buffer. Supplying VIO at least 6 ms after supplying VCC ensures that the OTP is initialized and output buffers are held low when VIO is supplied.

The time  $t_2$  is the delay between the start of the power-up sequence and the RESET\_OUT release. The RESET\_OUT resource is released when the power-up sequence is complete. The duration of the power-up sequence depends on OTP programming.

### 5.3.5 Power-On Acknowledge

The PMIC is designed to support the following power-on acknowledge modes: POWERHOLD mode and AUTODEVON mode.

#### 5.3.5.1 POWERHOLD Mode

In POWERHOLD mode, the power-on acknowledge is received through a dedicated pin, POWERHOLD. When an ON request is received, the device initiates the power-up sequence and asserts the RESET\_OUT pin high while the device is in the ACTIVE state (reset released). The device remains in ACTIVE state for a fixed delay of 8 seconds and then automatically shuts down. During this timeframe, to keep the device active, the host processor must assert and keep the POWERHOLD pin high. The device interprets a the high to low transition of the POWERHOLD pin as an OFF request.

Figure 5-5 shows the POWERHOLD mode timing diagram.

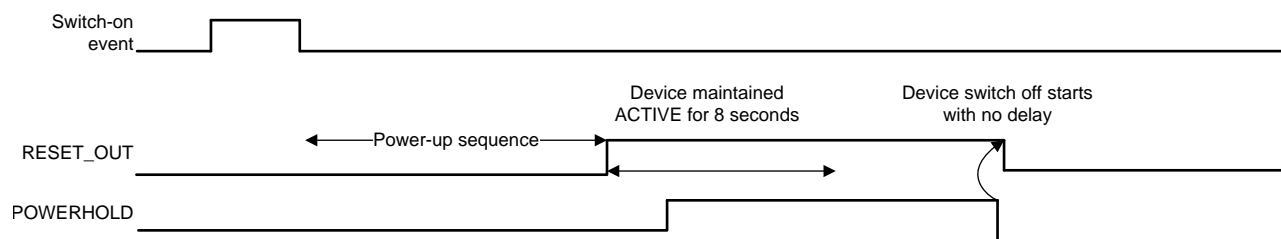


Figure 5-5. POWERHOLD Mode Timing Diagram

### 5.3.5.2 AUTODEVON Mode

In AUTODEVON mode, at the end of the power-up sequence, the DEV\_CTRL.DEV\_ON register bit is automatically set to 1 and the device remains in the ACTIVE state until the host processor clears this bit. No dedicated signal from processor is required to maintain the PMIC in the ACTIVE state.

Figure 5-6 and Figure 5-7 show the AUTODEVON mode timing diagrams.

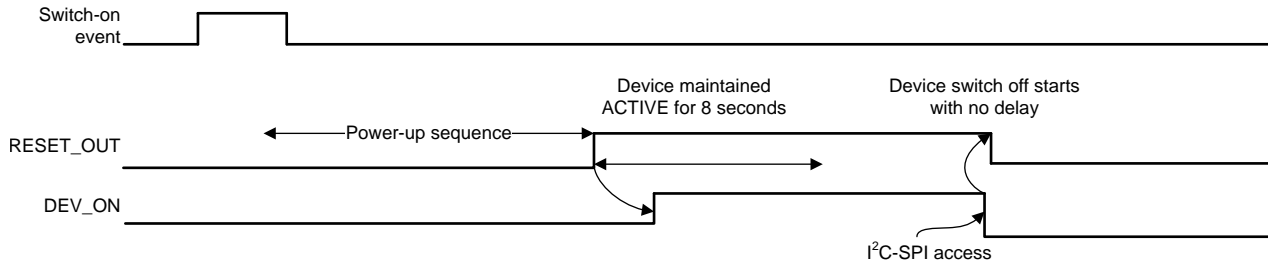


Figure 5-6. AUTODEVON Mode Timing Diagram

The DEV\_ON bit can also be configured so that it is not auto-updated (set to 1) at the end of the power-up sequence. In this case, the device functions similarly to when it is in the POWERHOLD mode, except that the host has control over the device using the DEV\_CTRL.DEV\_ON register bit instead of the POWERHOLD pin. Therefore, to maintain the device in the ACTIVE state, the host must set and keep this bit at 1.

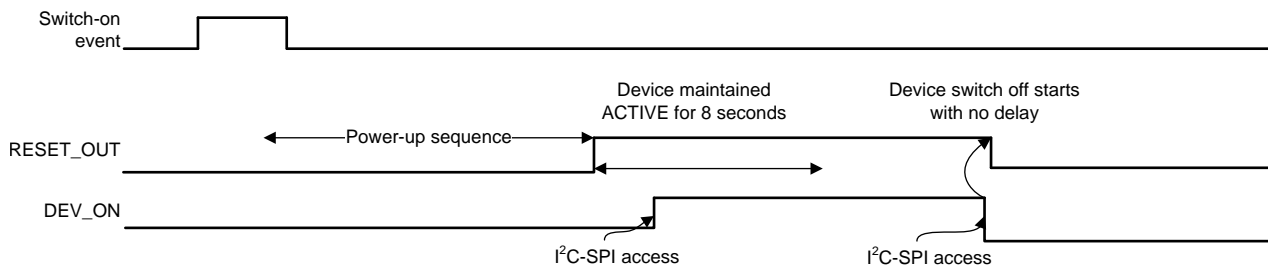


Figure 5-7. DEV\_ON Mode Timing Diagram

### 5.3.6 BOOT Configuration

All TPS65919-Q1 resource settings are stored in registers. Therefore, any platform-related settings are linked to an action which alters these registers. This action is either a static update (register initialization value) or a dynamic update of the register (from the user or a power sequence).

Resources and platform settings are stored in nonvolatile memory (OTP). These settings are defined as follows:

**Static platform settings** These settings define, for example, the SMPS and LDO default voltages, GPIO functionality, and TPS65919-Q1 switch-on events.

**Sequence platform settings** These settings define TPS65919-Q1 power sequences between state transitions. An example includes the OFF2ACT sequence when transitioning from OFF state to ACTIVE state. Each power sequence is composed of several register accesses that define the resources (and the corresponding registers) that must be updated during the respective state transition. Small modifications from the main sequence can be defined with the BOOT pin as long as the OTP memory size constraint is respected. The user can overwrite these settings when the power sequence completes.

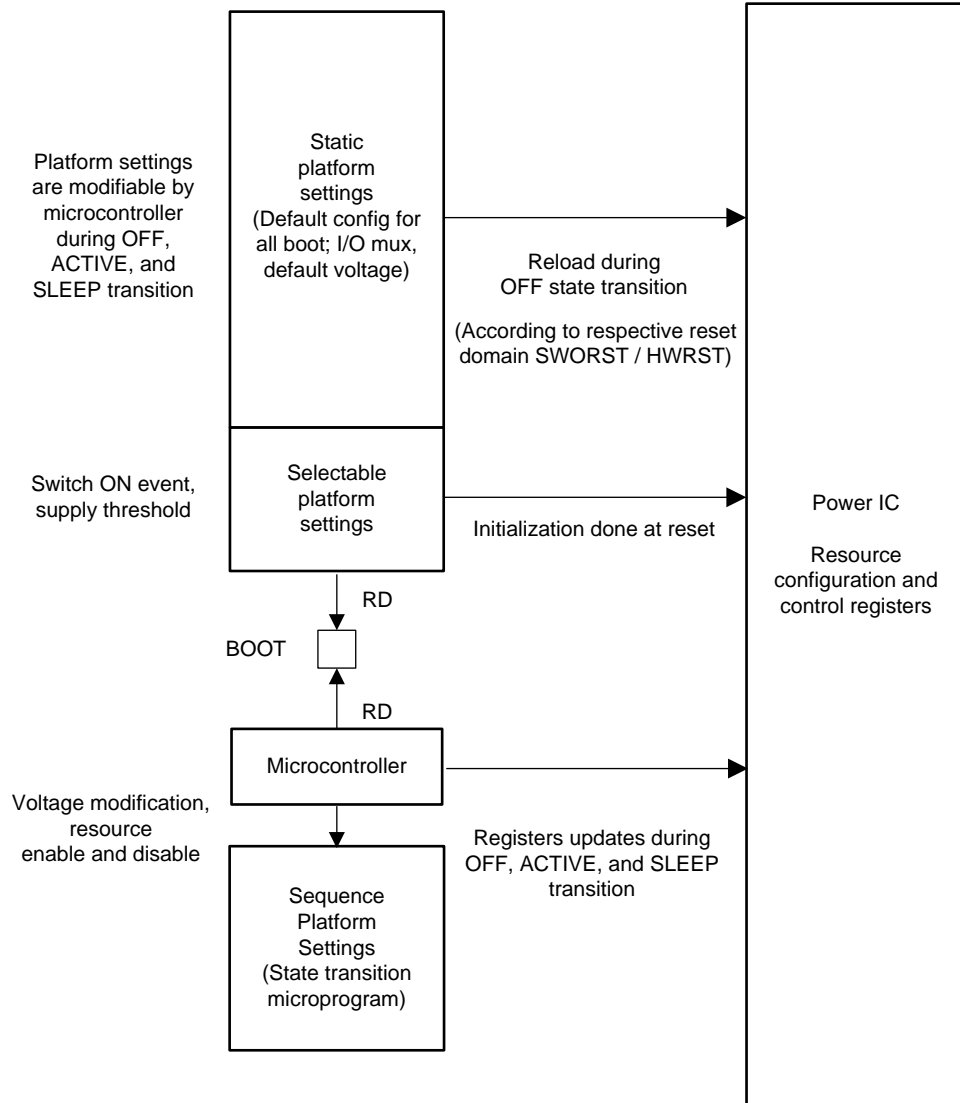


图 5-8. Boot Pins Control

### 5.3.6.1 Boot Pin Usage and Connection

表 5-6 lists the associated configurations of the boot pins.

表 5-6. Boot Pins Associated Configurations

BOOT	OTP CONFIGURATION	POWER SEQUENCE SELECTOR
0	OTP5 (0x00~0x2F)	Sel_0
1	OTP5 (0x30~0x5F)	Sel_1

The BOOT pin must be grounded or pulled up.

The status of the BOOT pin is latched at the end of the transition from OFF to ACTIVE mode and stored in the BOOT\_STATUS register.

The BOOT pin can also be used as static selectors during execution of the power sequence. This static selection provides from within a static power sequence, to branch to different instructions. This static selection allows the selection of power sequences (or subpart of power sequences) without altering the power sequences themselves in OTP.

### 5.3.7 Reset Levels

The TPS65919-Q1 resource control registers are defined by the following three categories:

- Power-on request (POR) registers
- Hardware (HW) registers
- Switchoff (SWO) registers

These registers are associated to three levels of reset which are described as follows

**Power-on reset (POR)** A POR occurs when the device receives supplies and transition from the NO SUPPLY state to the BACKUP state. The POR is the global device reset which resets all registers.

The values of the registers in this domain will retain their value under HWRST and SWORST event. This ensures the information which contains the cause of the switch off event is retained when the device is reset to its default operating state.

The following registers are reset only during POR event:

- SMPS\_THERMAL\_STATUS
- SMPS\_SHORT\_STATUS
- SMPS\_POWERGOOD\_MASK
- LDO\_SHORT\_STATUS
- SWOFF\_STATUS

This list is indicative only; a full list and bit details can be found in the *TPS65919-Q1 Register Map*.

**Hardware reset (HWRST)** A HWRST occurs when any OFF request is configured to generate a hardware reset. Configuration of the reset level is programmed in the SWOFF\_HWRST register. This reset triggers a transition to the OFF state from either the ACTIVE or SLEEP state, and therefore executes the ACT2OFF or SLP2OFF sequence.

A HWRST will reset all registers in the HWRST and the SWORST domain, but leave the registers in the POR domain unchanged.

The following registers are in the HWRST domain:

- SMPS control registers expect MODE\_ACTIVE and MODE\_SLEEP bits
- LDO control registers expect MODE\_ACTIVE and MODE\_SLEEP bits
- VSYS\_LO Threshold
- PMU\_CONFIG & PMU\_CTRL
- NSLEEP, ENABLE1, and ENABLE2 resource assignment registers
- Input and Output, including the GPIO pins, Configuration and Control registers
- Interrupt Control, Status and Mask Registers
- OTP CRC results register
- GPADC Configuration and Results registers

This list is indicative only; a full list and bit details can be found in the *TPS65919-Q1 Register Map*.

**Switch-off reset (SWORST)** A SWORST occurs when any OFF request is configured to not generate a hardware reset. Configuration is done in the SWOFF\_HWRST register. This reset acts like the HWRST, except only the SWO registers are reset. The TPS65919-Q1 goes into the OFF state, from either ACTIVE or SLEEP, and therefore executes the ACT2OFF or SLP2OFF sequence.

A SWORST only resets registers in the SWORST domain, but leave the registers in the HWRST and POR domains unchanged.

The following registers are in the SWORST domain:

- SMPS control registers for voltage levels and operating mode control
- LDO control registers for voltage levels and operating mode control
- DEV\_CTRL & POWER\_CTRL registers
- VSYS\_MON enable and result register
- WATCHDOG configuration register
- PLL and REGEN Control registers

This list is indicative only; a full list and bit details can be found in the *TPS65919-Q1 Register*

Map.

表 5-7 lists the reset levels, and 图 5-9 shows the reset levels versus registers.

表 5-7. Reset Levels

LEVEL	RESET TAG	REGISTERS AFFECTED	COMMENT
0	POR	POR, HW, SWO	This reset level is the lowest level, for which all registers are reset.
1	HWRST	HW, SWO	During hardware reset (HWRST), all registers are reset except the POR registers.
2	SWORST	SWO	Only the SWO registers are reset.

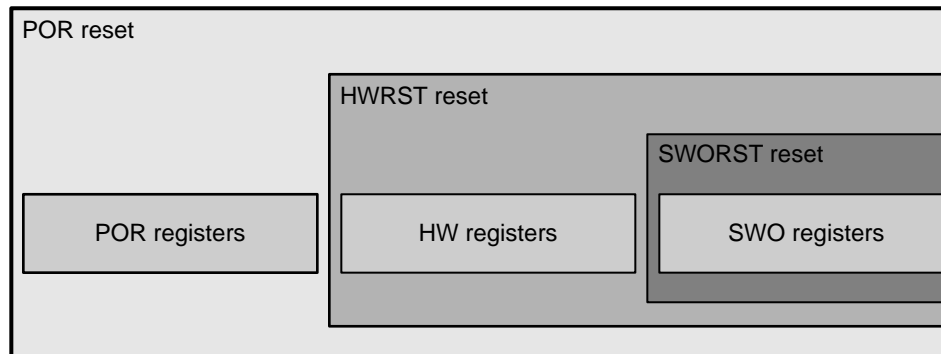


图 5-9. Reset Levels versus Registers

### 5.3.8 INT

The INT output is the interrupt request to the processor. By default, the INT pin is push-pull output and active low (when interrupt is pending, output is driven low). By default, the line is masked when the PMIC is in sleep state (configurable by setting the INT\_MASK\_IN\_SLEEP bit). Individual interrupt sources can be masked according to 表 5-12 .

### 5.3.9 Warm Reset

The TPS65919-Q1 device can execute a warm reset. The main purpose of this reset is to recover the device from a locked or unknown state by reloading default configuration. The warm reset is triggered by the NRESWARM pin. During a warm reset, the OFF2ACT sequence is executed regardless of the state (ACTIVE or SLEEP) and the device returns to or remains in the ACTIVE state. Resources that are not part of the OFF2ACT sequence are not impacted by a warm reset and retain the previous state. Resources that are part of power-up sequence go to active mode, and output voltage level is reloaded from OTP or kept in the previous value depending on the WR\_S bit in the SMPSx\_CTRL or LDOx\_CTRL register.

### 5.3.10 RESET\_IN

The RESET\_IN function causes a switch-off event (either a cold reset or shutdown). 表 5-3 shows that the RESET\_IN behavior is programmable. The RESET\_IN input has a 1-ms debounce that is independent of the selected polarity. In addition, after the device goes into the OFF state, a 25-ms masking period occurs before a new RESET\_IN event is accepted, which is equivalent to a 26-ms debounce for an OFF2ACT request.

## 5.4 Power Resources (Step-Down and Step-Up SMPS Regulators, LDOs)

The power resources provided by the TPS65919-Q1 device include inductor-based SMPSs and linear LDOs. These supply resources provide the required power to the external processor cores, external components, and to modules embedded in the TPS65919-Q1 device. 表 5-8 lists the power resources provided by the TPS65919-Q1 device.



**表 5-8. Power Resources**

RESOURCE	TYPE	VOLTAGE	CURRENT	COMMENTS
SMPS1, SMPS2	SMPS	0.7 to 1.65 V, 10-mV steps 1 to 3.3 V, 20-mV steps	7 A	Can be used as 1 dual-phase (7 A) or 2 single-phase (3.5 A) regulators
SMPS3	SMPS	0.7 to 1.65 V, 10-mV steps 1 to 3.3 V, 20-mV steps	3 A	
SMPS4	SMPS	0.7 to 1.65 V, 10-mV steps 1 to 3.3 V, 20-mV steps	1.5 A	
LDO1, LDO2	LDO	0.9 to 3.3 V, 50-mV steps	300 mA	
LDO4	LDO	0.9 to 3.3 V, 50-mV steps	200 mA	
LDO5	LDO	0.9 to 3.3 V, 50-mV steps	100 mA	Low-noise LDO

### 5.4.1 Step-Down Regulators

The synchronous step-down converter used in the power-management core has high efficiency while enabling operation with cost-competitive and small external components. The SMPSx\_IN supply pins of all the converters should be individually connected to the VSYS supply (VCCA pin). Two of these configurable step-down converters can be multiphased to create up to a 7-A rail. All of the step-down converters can synchronize to an external clock source between 1.7 MHz and 2.7 MHz, or an internal fallback clock at 2.2 MHz.

The step-down converter supports two operating modes, which can be selected independently. These two operating modes are defined as follows:

**Forced PWM mode:** In forced PWM mode, the device avoids pulse skipping and allows easy filtering of the switch noise by external filter components. The drawback is the higher  $I_{DDQ}$  at low-output current levels.

**Eco-mode (lowest quiescent-current mode):** Each step-down converter can be individually controlled to enter a low quiescent-current mode. In ECO-mode, the quiescent current is reduced and the output voltage is supervised by a comparator while most of the control circuitry disabled to save power. The regulators should not be enabled under ECO-mode to ensure the stability of the output. ECO-mode should only be enabled when a converter has less than 5 mA of load current and  $V_O$  can remain constant. In addition, ECO-mode should be disabled before a load-transient step to allow the converter to respond in a timely manner to the excess current draw.

To ensure proper operation of the converter while it is in ECO-mode, the output voltage level must be less than 70% of the input supply voltage level. If the  $V_O$  of the converter is greater than 2.8 V, the device monitors the supply voltage of the converter and automatically switch off the converter if the input voltage falls below 4 V. The purpose of this mechanism is to prevent damage to the converter because of design limitation while the converter is in ECO mode.

In addition to the operating modes, the following parameters can be selected for the regulators:

- Powergood: See [5.4.1.3](#).
- Output discharge: Each switching regulator is equipped with an output discharge enable bit. When this bit is set to 1, the output of the regulator is discharged to ground with the equivalent of a 9- $\Omega$  resistor when the regulator is disabled. If the regulator enable bit is set, the discharge bit of the regulator is ignored.
- Output-current monitoring: The GPADC can monitor the SMPS output current. One SMPS at a time can be selected for measurement from the following: SMPS1, SMPS2, SMPS1&2, and SMPS3. Selection is controlled through the GPADC\_SMPS\_ILMONITOR\_EN register.
- Enable control of the Step-down converters: The step-down converter enable and disable is part of the flexible power-up and power-down state-machine. Each converter can be programmed such that it is powered up automatically to a preselected voltage in one of the time slots after a power-on condition occurs. Alternatively, each SMPS can be controlled by a dedicated pin. The NSLEEP, ENABLE1, and ENABLE2 pins can be mapped to any resource (LDOs, SMPS converter, 32-kHz clock output, or GPIO) to enable or disable the pin. Each SMPS can also be enabled and disabled through access to the I<sup>2</sup>C registers.

### 5.4.1.1 Output Voltage and Mode Selection

One-time programmable (OTP) bits define the default output voltage and enabling of the regulator during the start-up sequence.

After start up, while the SMPS is in forced PWM mode, software can change the output voltage by setting the RANGE and VSEL bits in the SMPSx\_VOLTAGE register. When the SMPS enters ECO mode, the output voltage cannot be changed. Setting the SMPSx\_VOLTAGE.VSEL register to 0x0 disables the SMPS (turns off). The value for the RANGE bit cannot be changed when the SMPS is active. To change the operating voltage range, the SMPS must be disabled.

The operating mode (ECO, forced PWM, or off) of an SMPS when the TPS65919-Q1 device is in ACTIVE state can be selected in the SMPSx\_CTRL register by setting the MODE\_ACTIVE[1:0] bit field.

The operating mode of an SMPSx when the TPS65919-Q1 device is in the SLEEP state is controlled by the MODE\_SLEEP[1:0] bit field, depending on the SMPS assignment to the NSLEEP, ENABLE1, and ENABLE2 pins (see [Table 5-5](#)).

The soft-start slew rate ( $t_{\text{ramp}}$ ) is fixed.

The pulldown discharge resistance for off mode is enabled and disabled in the SMPS\_PD\_CTRL register. By default, discharge is enabled. Two pulldown resistors, one at SMPSx\_SW and one at SMPS\_FDBK node, are enabled or disabled together. For multiphase SMPS, pulldown is in the master phase.

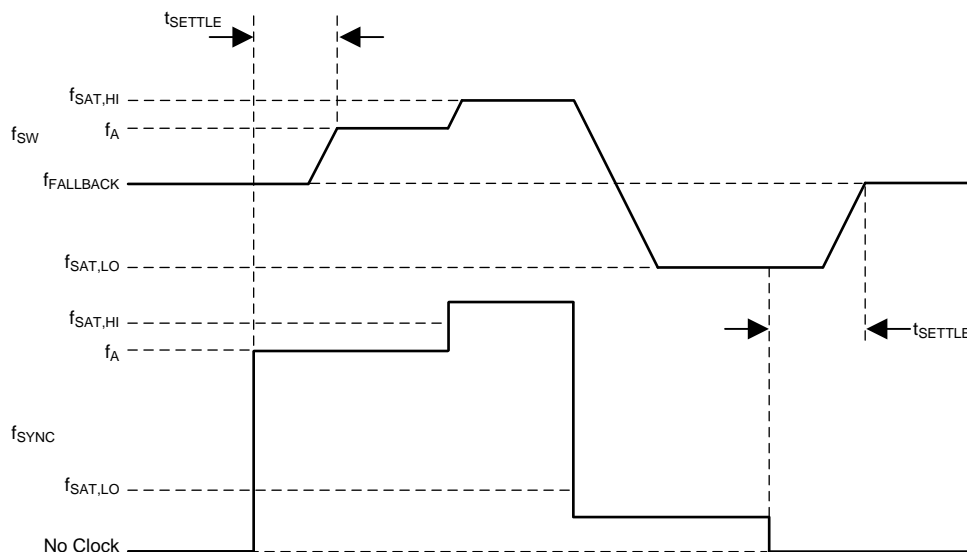
SMPS behavior for warm reset (reload default values or keep current values) is defined by the SMPSx\_CTRL.WR\_S bit.

### 5.4.1.2 Clock Generation for SMPS

In PWM mode, the SMPSs are synchronized on an external input clock, SYNCDCDC (muxed with GPIO\_3), whereas in ECO mode, the switching frequency is based on an internal RC oscillator.

For PWM mode, a PLL is present to buffer the external clock input from SYNCDCDC pin, and to create 5 clock signals for the 5 SMPSs with different phases.

[Figure 5-10](#) shows the frequency of SYNCDCDC input clock ( $f_{\text{SYNC}}$ ) and the frequency of PLL output signal ( $f_{\text{SW}}$ ).



**Figure 5-10. Synchronized Clock Frequency**

When no clock is present on the SYNCDCDC pin, the PLL generates a clock with a frequency equal to the fallback frequency ( $f_{\text{FALLBACK}}$ ).

When a clock is present on the SYNCDCDC pin with a frequency between the low and high PLL saturation frequencies ( $f_{SAT,LO}$  and  $f_{SAT,HI}$ ), then the PLL is synchronized on the SYNCDCDC clock and generates a clock with frequency equal to  $f_{SYNC}$ .

If  $f_{SYNC}$  is higher than  $f_{SAT,HI}$ , then the PLL generates a clock with a frequency equal to  $f_{SAT,HI}$ .

If  $f_{SYNC}$  is smaller than  $f_{SAT,LO}$ , then the PLL generates a clock with a frequency equal to  $f_{SAT,LO}$ .

Dithering can be achieved by changing the frequency of the clock provided on the SYNCDCDC pin. The sync clock dither specification parameters are based on a triangular dither pattern, but other patterns that comply with the minimum and maximum sync frequency range and the maximum dither slope can also be used, as seen in [Figure 5-11](#).

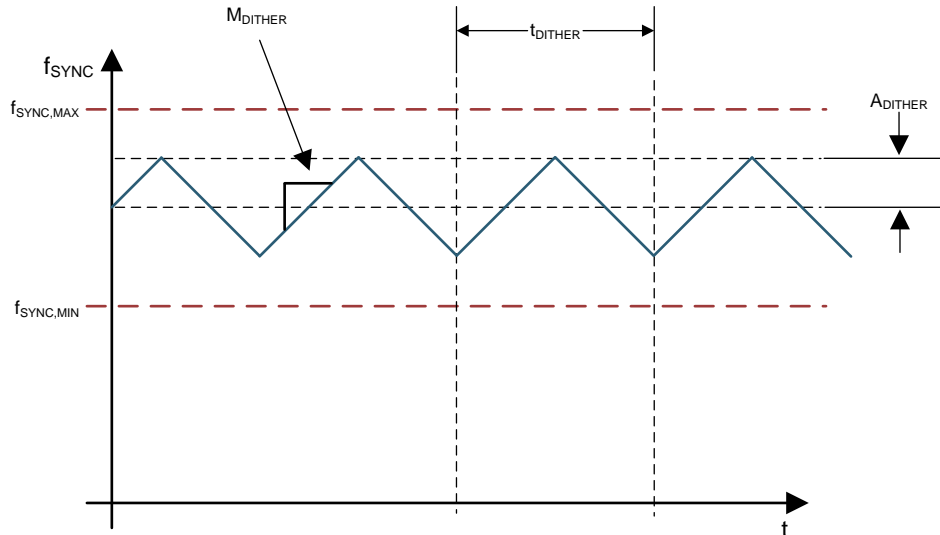


Figure 5-11. Synchronized Clock Frequency Range and Dither

#### 5.4.1.3 Current Monitoring and Short Circuit Detection

SMPS1, SMPS2, SMPS1&2, and SMPS3 include several other features.

The SMPS sink current limitation is controlled with the SMPS\_NEGATIVE\_CURRENT\_LIMIT\_EN register. The limitation is enabled by default.

Channel 4 of the GPADC can be used to monitor the output current of SMPS1, SMPS2, SMPS1&2, or SMPS3. Load current monitoring is enabled for a given SMPS in the SMPS\_ILMONITOR\_EN register. SMPS output-power monitoring is intended to be used during the steady state of the output voltage, and is supported in PWM mode only.

Use [Equation 1](#) to calculate the SMPS output-current result.

$$I_{LOAD} = I_{FS} \times \text{GPADC code} / (2^{12} - 1) - I_{OS} \quad (1)$$

where

- $I_{FS} = I_{FS0} \times K$
- $I_{OS} = I_{OS0} \times K$
- $K$  is the number of SMPS active phases

Use [Equation 2](#) to calculate the temperature compensated result.

$$I_{LOAD} = I_{FS} \times \text{GPADC code} / ((2^{12} - 1) \times [1 + TC\_R0 \times (TEMP - 25)]) - I_{OS} \quad (2)$$

For the values of  $I_{FS0}$  and  $I_{OS0}$ , see [Section 4.10](#).

The SMPS thermal monitoring is enabled (default) and disabled with the SMPS\_THERMAL\_EN register. When enabled, the SMPS thermal status is available in the SMPS\_THERMAL\_STATUS register. SMPS12 and SMPS3 have thermal protection. A unique thermal sensor is shared and protecting both SMPS1 and SMPS2. SMPS4 has no dedicated thermal protection.

Each SMPS has a detection for load current above  $I_{LIM}$ , indicating overcurrent or a shorted SMPS output. The SMPS\_SHORT\_STATUS register indicates any SMPS short condition. Depending on the setting of the INT2\_MASK.SHORT register, an interrupt is generated upon any shorted SMPS. If a short occurs on any enabled SMPSs, the corresponding short status bit is set in the SMPS\_SHORT\_STATUS register. A switch-off signal is then sent to the corresponding SMPS, and it remains off until the corresponding bit in the SMPS\_SHORT\_STATUS register is cleared. This register is cleared on read, or by issuing a POR. The same behavior applies to LDO shorts using the LDO\_SHORT\_STATUS registers.

A short must occur on any enabled SMPS or LDO for at least 155 us to 185 us for the short detection to shut off the rail. During startup of the device, there is a 2 ms counter that masks any short-circuit shutdown. This counter starts when the device is enabled and the counter is reset when any SMPSx or LDOx rail becomes ACTIVE. When no rail has been enabled for 2 ms, the counter reaches its threshold and the short-circuit shutdown is no longer masked for the enabled SMPSs and LDOs.

#### 5.4.1.4 POWERGOOD

The TPS65919-Q1 device includes an external POWERGOOD pin which indicates if the outputs of the SMPS are within the acceptable range of the programmed output voltage, and if the current loading for the SMPS is within the range of the current limit. Users can select whether POWERGOOD reports the result of both voltage and current monitoring or only current monitoring. This selection applies to all SMPSs in the SMPS\_POWERGOOD\_MASK2 register. POWERGOOD\_TYPE\_SELECT register. When both the voltage and current are monitored, the POWERGOOD signal indicates whether or not all SMPS outputs are within a certain percentage, as specified by the  $V_{SMSPG}$  parameter, of the programmed value while the load current is below  $I_{LIM}$ .

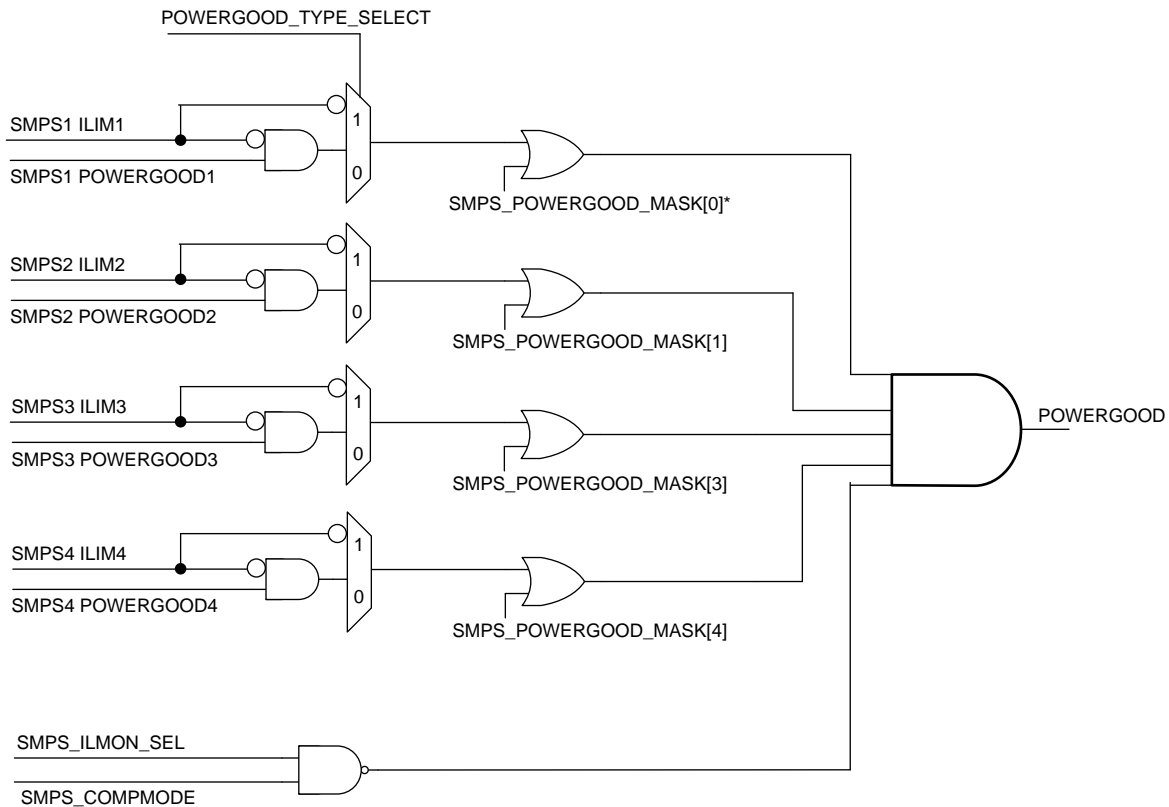
All POWERGOOD sources can be masked in the SMPS\_POWERGOOD\_MASK1 and SMPS\_POWERGOOD\_MASK2 registers. By default, only the SMPS1 rail (or SMPS12 rail if in dual phase) is monitored. When an SMPS is disabled, it should be masked in the SMPS\_POWERGOOD\_MASKx registers to prevent the SMPS from forcing the POWERGOOD pin to go inactive. When the SMPS voltage is transitioning from one target voltage to another because of a DVS command, voltage monitoring is internally masked and POWERGOOD is not impacted.

The GPADC result for SMPS output current monitoring can be included in POWERGOOD by setting the SMPS\_COMPMODE bit to 1. The GPADC can monitor only one SMPS.

✎ 5-12 is the block diagram of the circuitry which constructs the logic output of the POWERGOOD pin.

#### 注意

When operating in dual phase, the SMPS12 current monitor may cause POWERGOOD to change to a low level (with default polarity) when transitioning from dual phase operation to single phase operation. TI recommends masking SMPS12 as a POWERGOOD source, using SMPS\_POWERGOOD\_MASK1, or debouncing the POWERGOOD signal if this POWERGOOD toggle is not desired in the application design.



\*When operating in dual phase, SMPS\_POWERGOOD\_MASK[0] controls the monitoring of SMPS12. SMPS\_POWERGOOD\_MASK[1] is masked internally with dual phase operation.

5-12. POWERGOOD Block Diagram

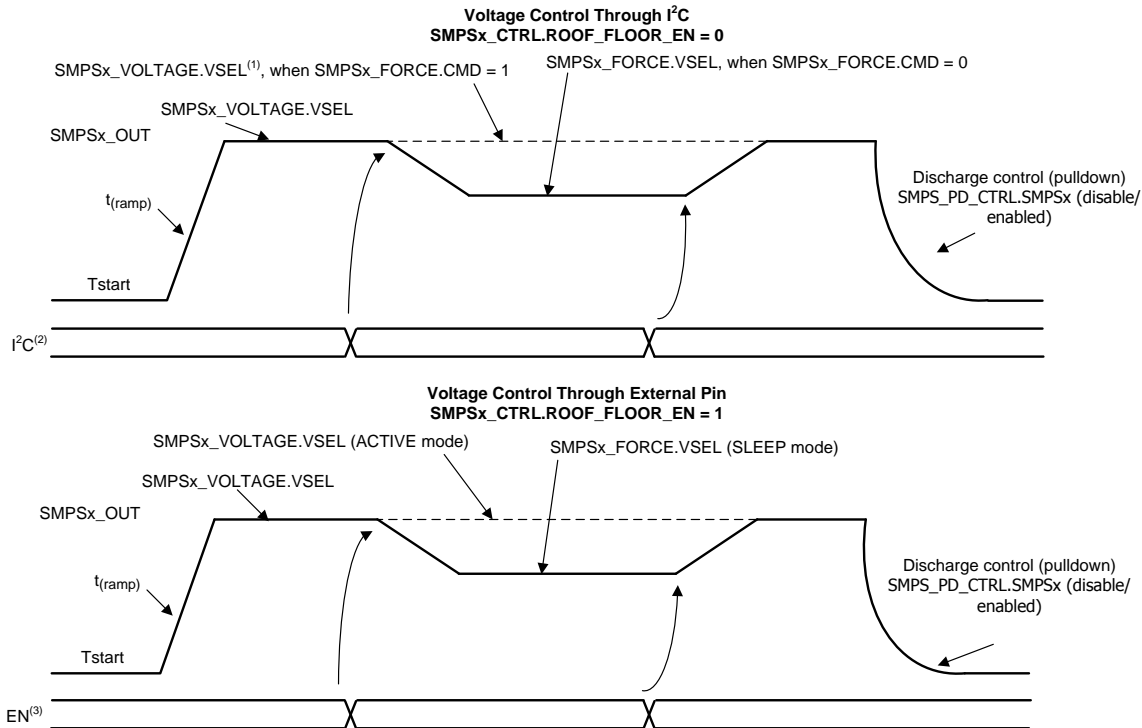
#### 5.4.1.5 DVS-Capable Regulators

The Step-down converters, SMPS1, SMPS2, or SMPS1&2 and SMPS3, are DVS-capable and have some additional parameters for control. The slew rate of the output voltage during a voltage level change is fixed at 2.5 mV/ $\mu$ s. The control for two different voltage levels (roof and floor) with the NSLEEP, ENABLE1, and ENABLE2 signals is available. When the roof-floor control is not used (ROOF\_FLOOR\_EN = 0), the CMD bit in the SMPSx\_FORCE register can select two different voltage levels.

Below are the steps for programming two difference output voltage levels (roof and floor) for the DVS-capable step-down converters:

- The NSLEEP, ENABLE1, or ENABLE2 pins can be used for roof-floor control of SMPS. For roof-floor operation, set the SMPSx\_CTRL.ROOF\_FLOOR\_EN register, and assign SMPS to NSLEEP, ENABLE1, and ENABLE2 in the NSLEEP\_SMPS\_ASSIGN, ENABLE1\_SMPS\_ASSIGN, and ENABLE2\_SMPS\_ASSIGN registers, respectively. When the controlling pin is active, the value for the SMPS output is defined by the SMPSx\_VOLTAGE register. When the controlling pin is not active, the value for the SMPS output is defined by the SMPSx\_FORCE register.
- Set the second value for the output voltage with the SMPSx\_FORCE.VSEL register. Setting this register to 0x0 turns off the SMPS.
- Select which register, SMPSx\_VOLTAGE or SMPSx\_FORCE, to use with the SMPSx\_FORCE.CMD bit. The default is the voltage setting of SMPSx\_VOLTAGE. For the CMD bit to work, ensure that the SMPSx\_CTRL.ROOF\_FLOOR\_EN bit is set to 0.

5-13 shows the SMPS controls for DVS.



- (1) **VSEL[6:0] (voltage selection):**  
SMPSx\_VOLTAGE.RANGE = 0: OFF, 0.5 V to 1.65 V in 10-mV steps  
SMPSx\_VOLTAGE.RANGE = 1: 1 to 3.3 V in 20-mV steps
- (2) **I<sup>2</sup>C:** Control through access to SMPSx\_VOLTAGE, SMPSx\_FORCE registers
- (3) **EN:** Control through NSLEEP, ENABLE1, and ENABLE2 pins (see 表 5-5)

图 5-13. SMPS Controls for DVS

#### 5.4.1.5.1 Non DVS-Capable Regulators

SMPS4 is a non-DVS-capable regulator. The slew rate of the output voltage is not controlled internally, and the converter achieves the new output voltage in JUMP mode. When changes to the output voltage are required, programming the changes to the output voltage of SMPS4 at a rate slower than 2.5 mV/μs is recommended to avoid voltage overshoot or undershoot.

#### 5.4.1.6 Step-Down Converters SMPS1, SMPS2 or SMPS1&2

The step-down converters, SMPS1 and SMPS2, can be used in two different configurations which are described as follows:

- SMPS1 and SMPS2 in single-phase configuration with each SMPS supporting a 3.5-A load current
- SMPS1&2 in dual-phase configuration supporting 7-A load current

SMPS1 and SMPS2 can be used as separate converters. In dual-phase configuration the two interleaved synchronous buck-regulator phases with built-in current sharing operate in opposite phases. For light loads, the converter automatically changes to single-phase operation.

图 5-14 shows the connections for dual-phase configurations.

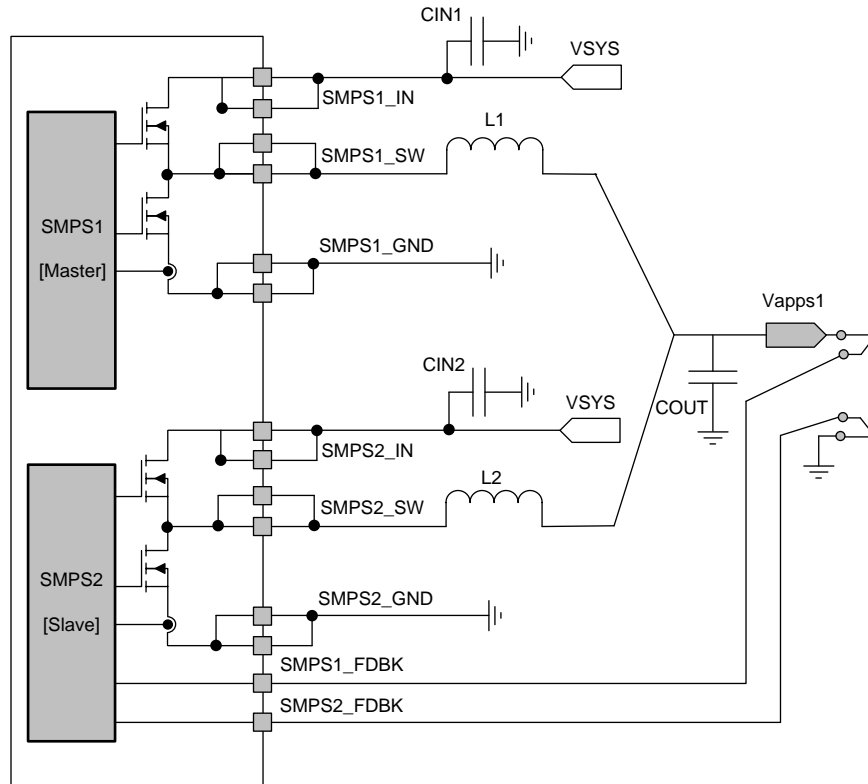


图 5-14. SMPS1&2 Dual-Phase Configuration

Below are the steps to program the SMPS1 and SMPS2 for single-phase or dual-phase operation:

- The OTP bit defines single-phase (SMPS1 and SMPS2) or dual-phase (SMPS1&2) operation. If dual-phase mode is selected, the SMPS12 registers control SMPS1&2.
- By default, SMPS1&2 operates in dual-phase mode for higher load currents and switches automatically to single-phase mode for low load currents. Forcing multiphase operation or single-phase operation is possible by setting the SMPS\_CTRL.SMPS12\_PHASE\_CTRL[1:0] bits when the SMPS1&2 are loaded. Under no-load condition, do not force the multiphase operation because it causes SMPS12 to exhibit instability.

#### 5.4.1.7 Step-Down Converters SMPS3, and SMPS4

SMPS3 is a buck converter supporting up to 3-A load current. SMPS4 is also a buck converter that supports up to 1.5-A load current. SMPS3 is DVS-capable.

#### 5.4.2 Low Dropout Regulators (LDOs)

All LDOs are integrated. They can be connected to the system supply, to an external buck boost SMPS, or to another preregulated voltage source. The output voltages of all LDOs can be selected, regardless of the LDO input voltage level,  $V_{IN}$ . No hardware protection is available to prevent software from selecting an improper output voltage if the  $V_{IN}$  minimum level is lower than the total DC-output voltage ( $T_{DCOV(LDOx)}$ ) plus the dropout voltage ( $D_{V(LDOx)}$ ). In such conditions, the output voltage is lower and nearly equal to the input supply. The output voltage of the regulator cannot be modified while the LDO is enabled from one voltage range (0.9 to 2.1 V) to the other voltage range (2.2 to 3.3 V). The regulator must be restarted in these cases. If an LDO is not needed, the external components do not need to be mounted. The TPS65919-Q1 device is not damaged by such configuration. The other functions do not depend on the unused LDOs and work properly.

### 5.4.2.1 LDOVANA

The LDOVANA voltage regulator is dedicated to supply the analog functions of the TPS65919-Q1 device, such as the GPADC and other analog circuitry. The LDOVANA regulator is automatically enabled and disabled as needed. The automatic control optimizes the overall current consumption if the SLEEP state.

### 5.4.2.2 LDOVRTC

The LDOVRTC regulator supplies always-on functions, such as wake-up functions. This power resource is active as soon as a valid energy source is present.

This resource has two modes which are Normal mode and backup mode. The LDOVRTC regulator functions in normal mode when supplied from the main system power rail and is able to supply all digital components of the TPS65919-Q1 device. The LDOVRTC regulator functions backup mode when supplied from system power rail that is above the power-on reset threshold but below the system low threshold and is only able to supply always-on components.

The LDOVRTC regulator supplies the digital components of the TPS65919-Q1 device. In the BACKUP state, the digital activity is reduced to maintaining the wake up functions only. In the OFF state, the turn-on events and detection mechanism are added to the previous current load in the BACKUP state. In the BACKUP and OFF states, the external load on the LDOVRTC pin should not exceed 0.5 mA. In the ACTIVE state, the LDOVRTC switches automatically into active mode. The reset is released and the clocks are available. In SLEEP state, the LDOVRTC is kept active. The reset is released and only the 32-kHz clock is available. To reduce power consumption, the user is still able to select low-power mode through the software.

---

#### 注

If  $V_{CC}$  is discharged rapidly and then resupplied, a POR may not be reliably generated. In this case a pull-down resistor can be added on the LDOVRTC output. See [5.15](#) for details.

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### 5.4.2.3 LDO1 and LDO2

The LDO1 and LDO2 regulators have bypass capability to connect the input voltage to the output. This ability is useful, for example, as an input-output (I/O) supply of an SD card and preregulated with a 2.7 to 3.3 V supply. This ability allows switching between 1.8 V (normal LDO mode) and the preregulated supply (bypass mode).

### 5.4.2.4 Low-Noise LDO (LDO5)

LDO5 is specifically designed to supply noise sensitive circuits. This supply can be used to power circuits such as PLLs, oscillators, or other analog modules that require low noise on the supply.

### 5.4.2.5 Other LDOs

All other LDOs have the same output voltage capability which is from 0.9 to 3.3 V in 50-mV steps.

## 5.5 SMPS and LDO Input Supply Connections

To avoid leakage, all SMPS<sub>x</sub>\_IN supply pins and the VCCA pin must be externally connected together.

The LDO preregulation from a boosted supply (voltage at LDO<sub>x</sub>\_IN > voltage at VCCA) is supported if the output voltage of the LDO is 2.2 V (minimum).

## 5.6 First Supply Detection

The TPS65919-Q1 device can be configured to detect and wake up from a first supply-detection (FSD) event.



When an automatic start from an FSD event is enabled, the PMIC powers up automatically when a supply is inserted, without waiting for a PWRON button press or other start-up event. An FSD event is detected when the VCCA pin voltage increases above the VSYS\_LO threshold. Transition to ACTIVE state requires that the VCC\_SENSE voltage increases above the VSYS\_HI voltage.

The FSD feature is enabled through unmasking the corresponding interrupt. This event triggers the interrupt, FSD, to the interrupt (INT) line. When an FSD interrupt occurs, the source can be determined using the FSD\_STATUS bit in the PMU\_SECONDARY\_INT register. An interrupt from an FSD event, if not masked, is a wake-up event. Interrupt masking is pre-programmed in the one time programmable memory (OTP) of the device. Any HWRST event sets the interrupt mask bits to the default (OTP) value. The FSD event can also be masked through the PMU\_SECONDARY\_INT register by setting the FSD\_MASK bit.

## 5.7 Long-Press Key Detection

The TPS65919-Q1 device can detect a long press on a key (or pin), PWRON. Upon detection, the device generates a LONG\_PRESS\_KEY interrupt and then switches the system off. The key-press duration is configured through the LONG\_PRESS\_KEY.LPK\_TIME bits.

## 5.8 12-Bit Sigma-Delta General-Purpose ADC (GPADC)

The features of the GPADC include the following:

The GPADC consists of a 12-bit sigma-delta ADC combined with a 8-input analog multiplexer. The running frequency of the GPADC is 2.5MHz. The GPADC lets the host processor monitor analog signals using analog-to-digital conversion on the input source. After the conversion is complete, an interrupt is generated to signal the host processor that the result of the conversion is ready to be accessed through the I<sup>2</sup>C interface.

The GPADC supports 8 analog inputs. Two of these inputs are available on external pins and the remaining inputs are dedicated to VSYS supply voltage monitoring and internal resource monitoring.

 [5-15](#) shows the block diagram of the GPADC.

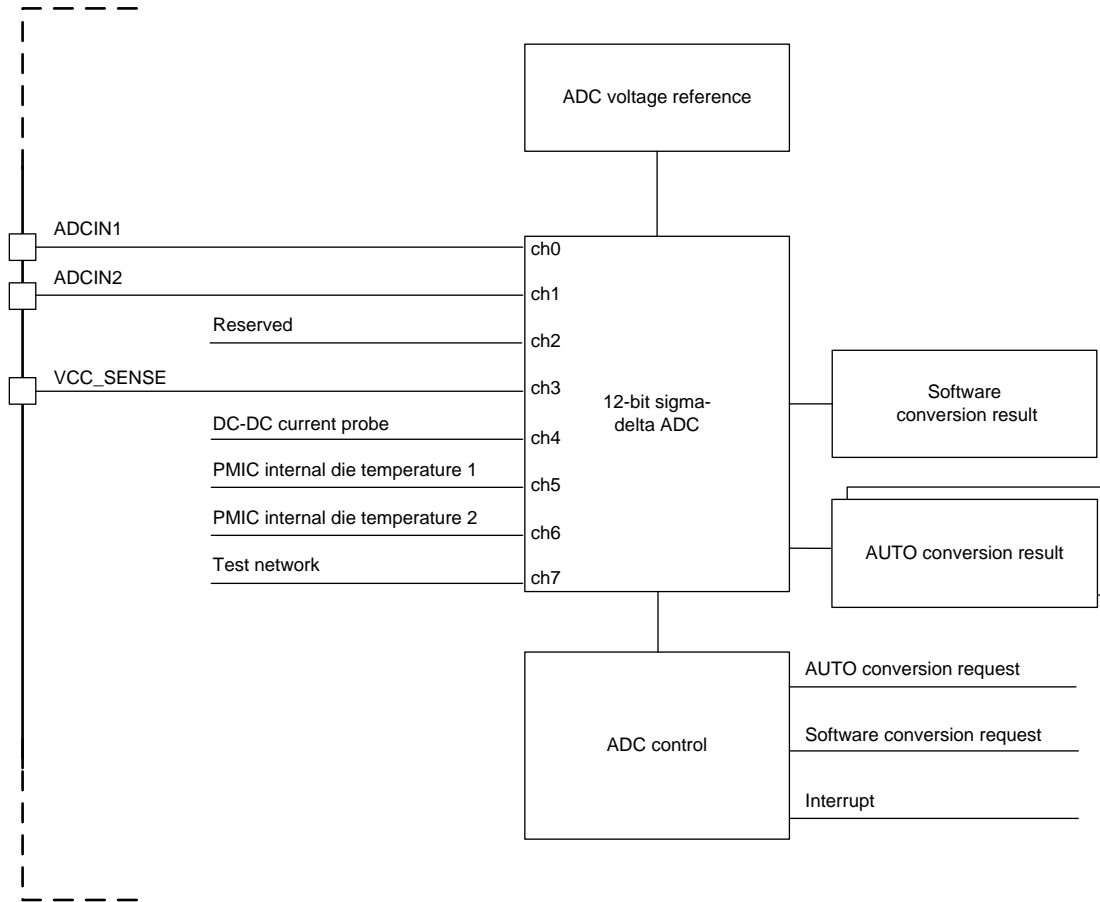


图 5-15. Block Diagram of the GPADC

The conversion requests are initiated by the host processor either by software through the I<sup>2</sup>C or by periodical measurements.

Two kinds of conversion requests occur with the following priority:

1. Asynchronous conversion request (SW), see 5.8.1
2. Periodic conversion (AUTO), see 5.8.2

表 5-9 lists the GPADC channel assignments.

Use 式 3 to convert from the GPADC code to the internal die temperature using GPADC channels 5 and 6.

$$\text{Die Temperature (}^\circ\text{C)} = \frac{\left( \left[ \frac{\text{GPADC Code}}{2^{12}} \right] \times 1.25 \right) - 0.753 \text{ V}}{2.64 \text{ mV}} \quad (3)$$

表 5-9. GPADC Channel Assignments

CHANNEL	TYPE	INPUT VOLTAGE FULL RANGE <sup>(1)</sup>	INPUT VOLTAGE PERFORMANCE RANGE <sup>(2)</sup>	SCALER	OPERATION
0 (ADCIN1)	External <sup>(3)</sup>	0 to 1.25 V	0.01 to 1.215 V	No	General purpose
1 (ADCIN2)	External <sup>(3)</sup>	0 to 1.25 V	0.01 to 1.215 V	No	General purpose
2	Reserved				

(1) The minimum and maximum voltage full range corresponds to typical minimum and maximum output codes (0 and 4095).  
 (2) The performance voltage is a range where gain error drift, offset drift, INL and DNL parameters are ensured.  
 (3) If VANALDO is off, maximum current to draw from GPADC\_INx is 1 mA for reliability. For current higher than 1 mA, LDOVANA must be in the SLEEP or ACTIVE state.

**表 5-9. GPADC Channel Assignments (continued)**

CHANNEL	TYPE	INPUT VOLTAGE FULL RANGE <sup>(1)</sup>	INPUT VOLTAGE PERFORMANCE RANGE <sup>(2)</sup>	SCALER	OPERATION
3 (VCC_SENSE)	Internal	2.5 to 5 V when HIGH_VCC_SENSE = 0 2.3 V to (VCCA – 1 V) when HIGH_VCC_SENSE = 1	2.5 to 4.86 V when HIGH_VCC_SENSE = 0 2.3 V to (VCCA – 1 V) when HIGH_VCC_SENSE = 1	4	System supply voltage (VCC_SENSE)
4	Internal	0 to 1.25 V		No	DC-DC current probe
5	Internal	0 to 1.25 V	0 to 1.215 V	No	PMIC internal die temperature 1
6	Internal	0 to 1.25 V	0 to 1.215 V	No	PMIC internal die temperature 2
7	Internal	0 to VCCA V	0.055 to VCCA V	5	Test network

### 5.8.1 Asynchronous Conversion Request (SW)

The user can request an asynchronous conversion. This conversion is not critical for start-of-conversion positioning.

The user must select the channel to be converted through the software and then request the conversion through the GPADC\_SW\_SELECT register. An GPADC\_EOC\_SW interrupt is generated when the conversion result is ready, and the result is stored in the GPADC\_SW\_CONV0\_LSB and GPADC\_SW\_CONV0\_MSB registers.

#### 注意

A defect in the digital controller of TPS65919-Q1 device may cause an unreliable result from the first asynchronous conversion request after the device exit from a warm reset. Texas Instruments recommends that user rely on subsequent requests to obtain accurate result from the asynchronous conversion after a device warm reset.

For detailed information regarding this issue, see *Guide to Using the GPADC in TPS65903x and TPS6591x Devices* [SLIA087](#).

### 5.8.2 Periodic Conversion (AUTO)

The user can enable periodic conversions to compare one or two channels with a predefined threshold level. One or two channels can be selected by programming the GPADC\_AUTO\_SELECT register. The thresholds and polarity of the conversion can be programmable through the GPADC\_THRES\_CONV0\_LSB, GPADC\_THRES\_CONV0\_MSB, GPADC\_THRES\_CONV1\_LSB, and GPADC\_THRES\_CONV1\_MSB registers. In addition, software must select the conversion interval with the GPADC\_AUTO\_CTRL register and enable the periodic conversion with the AUTO\_CONV0\_EN and AUTO\_CONV1\_EN bits.

The GPADC does not need to be enabled separately. The control logic enables and disables the GPADC automatically to save power. The latest conversion result is always stored in the GPADC\_AUTO\_CONV0\_LSB, GPADC\_AUTO\_CONV0\_MSB, GPADC\_AUTO\_CONV1\_LSB, and GPADC\_AUTO\_CONV1\_MSB registers. All selected channels are queued and converted from channel 0 to 7. The first (lower) converted channel result is placed in the GPADC\_AUTO\_CONV0 register and the second result is placed in the GPADC\_AUTO\_CONV1 register. Therefore, it is recommended to place the lower channel for conversion in the AUTO\_CONV0\_SEL bit field of the GPADC\_AUTO\_SELECT register, and the higher channel for conversion in the AUTO\_CONV1\_SEL bit field.

If the conversion result triggers the threshold level, an INT interrupt is generated and the conversion result is stored. If the interrupt is not cleared or the results are not read before another auto-conversion is complete, then the registers store only the latest results, discarding the previous ones. The auto-conversion is never stopped by an uncleared interrupt or unread registers.

Programming the triggering of the threshold level can also generate shutdown. This programming is available independently for the CONV0 and CONV1 channels and is enabled by setting the SHUTDOWN bits in the GPADC\_AUTO\_CTRL register. During sleep and off modes, only channels 0 to 4 can be converted. For channels 5 and 6, conversion is possible in sleep state if the thermal sensor is not disabled.

### 5.8.3 Calibration

The GPADC channels are calibrated in the production line using a 2-point calibration method. The channels are measured with two known values (X1 and X2) and the difference (D1 and D2) to the ideal values (Y1 and Y2) are stored in the OTP memory. 5-16 shows the principle of the calibration.

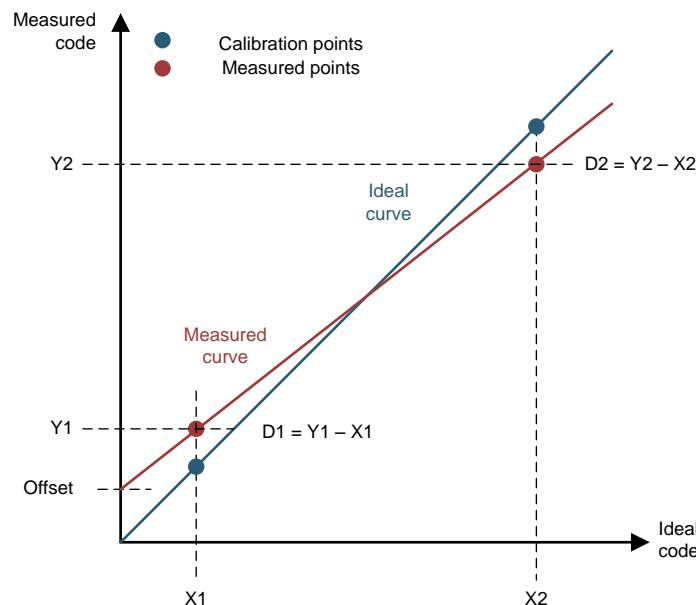


图 5-16. ADC Calibration Scheme

Some of the GPADC channels can use the same calibration data. Use 式 4 and 式 5 to calculate the corrected result.

$$\text{Gain: } k = 1 + \frac{(D2 - D1)}{(X2 - X1)} \tag{4}$$

$$\text{Offset: } b = D1 - (k - 1) \times X1 \tag{5}$$

If the measured code is *a*, the corrected code *a'* is calculated using 式 6.

$$a' = \frac{(a - b)}{k} \tag{6}$$

表 5-10 lists the parameters, X1 and X2, and the register for D1 and D2 required in the calculation for all the channels.

表 5-10. GPADC Calibration Parameters

CHANNEL	X1	X2	D1	D2	COMMENTS
0, 1	2064 (0.63 V)	3112 (0.95 V)	GPADC_TRIM1	GPADC_TRIM2	

**表 5-10. GPADC Calibration Parameters (continued)**

CHANNEL	X1	X2	D1	D2	COMMENTS
3	2064 (2.52 V)	3112 (3.8 V)	GPADC_TRIM3	GPADC_TRIM4	When HIGH_VCC_SENSE = 0
3	2064 (2.52 V)	3112 (3.8 V)	GPADC_TRIM5	GPADC_TRIM6	When HIGH_VCC_SENSE = 1

## 5.9 General-Purpose I/Os (GPIO Pins)

The TPS65919-Q1 device integrates seven configurable general-purpose I/Os that are multiplexed with alternative features as listed in [表 5-11](#)

**表 5-11. General Purpose I/Os Multiplexed Functions**

PIN	PRIMARY FUNCTION	SECONDARY FUNCTION
GPIO_0	General-purpose I/O Port 0	Input: PWRDOWN (Power down signal)
		Input: ENABLE2 (Peripheral power request input 2)
		Output: REGEN1 (External regulator enable output 4)
GPIO_1	General-purpose I/O Port 1	Input: RESET_IN (Reset input)
		Input: NRESWARM (Warm reset input)
		Input: VBUS_SENSE (VBUS input)
GPIO_2	General-purpose I/O Port 2	Input: ENABLE1 (Peripheral power request input 1) Input/Output: I2C2_SDA_SDO (DVS control I <sup>2</sup> C serial bidirectional data) or SPI output data signal
GPIO_3	General-purpose I/O Port 3	Input: ENABLE2 (Peripheral power request input 2)
		Output: REGEN1 (External regulator enable output 1)
		Input: SYNCDCDC (SMPS clock synchronization input)
GPIO_4	General-purpose I/O Port 4	Output: REGEN2 (External regulator enable output 2)
		Input/Output: I2C2_SCL_SCE (DVS control I <sup>2</sup> C serial clock) or SPI chip-select signal
GPIO_5	General-purpose I/O Port 5	Input: POWERHOLD (Power hold input)
		Output: REGEN3 (External regulator enable output 3)
GPIO_6	General-purpose I/O Port 6	Input: NSLEEP (Sleep mode request signal)
		Output: POWERGOOD (Indicator signal for valid regulator output voltages)
		Output: REGEN3 (External regulator enable output 3)

For GPIOs characteristics, refer to:

- Pin description,
- Electrical characteristics, [Section 4.14](#) and [Section 4.15](#)
- Pullup and pulldown characteristics, [Section 4.16](#)

Each GPIO event can generate an interrupt on a rising edge, falling edge, or both; each line is individually maskable (as described in [5.11](#)). A GPIO-interrupt applies only when the primary function (general-purpose I/O) has been selected.

All GPIOs can be used as wake-up events.

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### 注

GPIO\_2 and GPIO\_4 are in the VIO domain (only the I/O supply is required to be available) and therefore these GPIOs cannot be used as ON requests from the OFF mode.

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The REGEN1 output is muxed in GPIO\_0 and GPIO\_3, the REGEN2 output is muxed in GPIO\_4, and the REGEN3 output is muxed in GPIO\_5 and GPIO\_6. When the GPIO\_0, GPIO\_3, GPIO\_4, GPIO\_5, and GPIO\_6 pins are configured as REGEN1, REGEN2, or REGEN3, these pins can be programmed as part of the power-up sequence to enable external devices such as external SMPSs. The REGEN1 and REGEN3 signals are at the VRTC voltage level and the REGEN2 signal is at the VIO voltage level.

The PRIMARY\_SECONDARY\_PAD1 and PRIMARY\_SECONDARY\_PAD2 registers control selection between primary and secondary functions.

When configured as primary functions, all GPIOs are controlled through the following set of registers:

- GPIO\_DAT\_DIR: Configures individually each GPIO direction (read and write)
- GPIO\_DATA\_IN: Data line-in when configured as an input (read only)
- GPIO\_DATA\_OUT: Data line-out when configured as an output (read and write)
- GPIO\_DEBOUNCE\_EN: Enables individually each GPIO debouncing (read and write)
- GPIO\_CTRL: Global GPIO control to enable and disable all GPIOs (read and write)
- GPIO\_CLEAR\_DATA\_OUT: Clears individually each GPIO data out (write only)
- GPIO\_SET\_DATA\_OUT: Sets individually each GPIO data out (write only)
- PU\_PD\_GPIO\_CTRL1, PU\_PD\_GPIO\_CTRL2: Configures each line pullup and pulldown (read and write)
- OD\_OUTPUT\_GPIO\_CTRL: Enables individual output open drain (read and write)

When configured as secondary functions, none of the GPIO control registers (see [表 5-11](#)) affect GPIO lines. The line configurations (pullup, pulldown, or open drain) for secondary functions are held in a separate register set as well as specific function settings.

## 5.10 Thermal Monitoring

The TPS65919-Q1 device includes several thermal monitoring functions for internal thermal protection of the PMIC.

The TPS65919-Q1 device integrates two thermal detection modules to monitor the temperature of the die. These modules are placed on opposite sides of the device and close to the LDO and SMPS modules. An over-temperature condition at either module first generates a warning to the system and then, if the temperature continues to rise, a switch-off of the PMIC device can occur before damage to the die.

Two thermal protection levels are available. One of these protections is a hot-die (HD) function which sends an interrupt to software. Software is expected to close any noncritical running tasks to reduce power. The second protection is a thermal shutdown (TS) function which immediately begins device switch-off.

By default, thermal protection is always enabled except in the BACKUP or OFF state. Disabling thermal protection in sleep state is possible for minimum power consumption.

To use thermal monitoring in the system do the following:

- Set the value for the hot-die temperature threshold with the OSC\_THERM\_CTRL.THERM\_HD\_SEL[1:0] bits.
- Disable thermal shutdown in sleep state by setting the THERM\_OFF\_IN\_SLEEP bit to 1 in the OSC\_THERM\_CTRL register.

During operation, if the die temperature increases beyond HD\_THR\_SEL, an interrupt (INT1.HOTDIE) is sent to the host processor. Immediate action to reduce the PMIC power dissipation by shutting down some functions must occur.

If the die temperature of the PMIC device rises further (above 148°C), an immediate shutdown occurs. Indication of a thermal shutdown event indication is written to the status register, INT1\_STATUS\_HOTDIE. The system cannot restart until the temperature falls below the HD\_THR\_SEL threshold.

### 5.10.1 Hot-Die Function (HD)

The HD detector monitors the temperature of the die and provides a warning to the host processor through the interrupt system when the temperature reaches a critical value. The threshold value must be set to less than the thermal shutdown threshold. Hysteresis is added to the HD detection to avoid generating multiple interrupts.

The integrated HD function provides the host PM software with an early warning overtemperature condition. This monitoring system is connected to the interrupt controller (INTC) and can send an interrupt when the temperature is higher than the programmed threshold. The TPS65919-Q1 device allows the programming of four junction-temperature thresholds to increase the flexibility of the system: in nominal conditions, the threshold triggering of the interrupt can be set from 117°C to 130°C. The HD hysteresis is 10°C in typical conditions.

When the power-management software triggers an interrupt, immediate action must be taken to reduce the amount of power drawn from the PMIC device (for example, noncritical applications must be closed).

### 5.10.2 Thermal Shutdown

The thermal shutdown detector monitors the temperature on the die. If the junction reaches a temperature at which damage can occur, a switch-off transition is initiated and a thermal shutdown event is written into a status register.

The system cannot restart until the die temperature falls below the HD threshold.

## 5.11 Interrupts

[表 5-12](#) lists the TPS65919-Q1 interrupts.

These interrupts are split into four register groups (INT1, INT2, INT3, and INT4) and each group has three associated control registers which are defined as follows:

**INTx\_STATUS** Reflects which interrupt source has triggered an interrupt event

**INTx\_MASK** Used to mask any source of interrupt, to avoid generating an interrupt on a specified source

**INTx\_LINE\_STATE** Reflects the real-time state of each line associated to each source of interrupt

The INT4 register group has two additional registers, INT4\_EDGE\_DETECT1 and INT4\_EDGE\_DETECT2, to independently configure rising and falling edge detection (respectively).

All interrupts are logically combined on a single output line, INT (default is active low). The INT line is used as an external interrupt line to warn the host processor of any interrupt event that has occurred within the device. The host processor must read the interrupt status registers (INTx\_STATUS) through the control interface (I<sup>2</sup>C) to identify the interrupt source. Any interrupt source can be masked by programming the corresponding mask register, INTx\_MASK. When an interrupt is masked, the associated event-detection mechanism is disabled. Therefore the corresponding STATUS bit is not updated and the INT line is not triggered if the masked event occurs. If an event occurs while the corresponding interrupt is masked, that event is not recorded. If an interrupt is masked after it has been triggered (the event has occurred and has not been cleared), the STATUS bit would reflect the event until the bit is cleared. While the event is masked, the STATUS bit will not be over-written when a new event occurs.

Because some interrupts are sources of ON requests (see [表 5-12](#)), source masking can mask a specific device switch-on event. Because an active interrupt line, INT, is treated as an ON request, any interrupt that is not masked must be cleared to allow the execution of a sleep sequence of the device, when requested.

The polarity of the INT line and clearing method of interrupts can be configured using the INT\_CTRL register.

An INT line can be triggered in either SLEEP or ACTIVE state, depending on the setting of the OSC\_THERM\_CTRL.INT\_MASK\_IN\_SLEEP bit.

When a new interrupt occurs while the INT line is still active (not all interrupts are cleared), then the following occurs:

- If the new interrupt source is the same as the one that has already triggered the INT line, the interrupt can be discarded or stored as a pending interrupt depending on the setting of the INT\_CTRL.INT\_PENDING bit.
  - When the INT\_CTRL.INT\_PENDING bit is active, then any new interrupt event occurring on the same source (while the INT line is still active) is stored as a pending interrupt. Because only one level of pending interrupts can be stored for a given source, when more than two events occur on the same source, only the last event is stored. While an interrupt is pending, two accesses are required (either read or write) to clear the STATUS bit: one access for the actual interrupt and the other for the pending interrupt. Two consecutive read-write (R/W) operations to the same register clear only one interrupt. Another register must be accessed between the two R/W clear operations. For example, for a clear-on-read operation, when the INT signal is active, read all four INTx\_STATUS registers in sequence to collect the status of all potential interrupt sources. The read access clears the full register for the active or actual interrupt. If the INT line is still active, repeat the read sequence to check and clear pending interrupts.
  - When the INT\_CTRL.INT\_PENDING bit is inactive (default), then any new interrupt event occurring on the same source (while the INT line is still active) is discarded. Two consecutive R/W operations to the same register only clear one interrupt. Another register must be accessed between the two R/W-to-clear operations.
- If the new interrupt source is different from the one that already triggered the INT line, then the interrupt is stored immediately in the corresponding STATUS bit.

To clear the interrupt line, all status registers must be cleared. The clearing of all status registers occurs by using a clear-on-read or a clear-on-write method. The clearing method is selectable through the INT\_CTRL.INT\_CLEAR bit. When this bit is set, the clearing method applies to all bits for all interrupts.

The two different clear operations are defined as follows:

**Clear-on-read** Read operation on a single status register clears all bits for only this specific register (8 bits). Therefore, a read operation of all the four status registers is required to clear all the interrupt requests. When the four read operations are complete, if the INT line is still active then another interrupt event has occurred during the read process. Therefore, the read sequence must be repeated.

**Clear-on-write** This method is bit-based; setting a specific bit to 1 clears only the written bit. Therefore, to clear a complete status register, write 0xFF. Writing 0xFF to all four status registers is required to clear all the interrupt requests. When the four write operations are complete, if the INT line is still active then another interrupt event has occurred during the write process. Therefore the write sequence must be repeated.



表 5-12. Interrupt Sources

INTERRUPT	ASSOCIATED EVENT	EDGES DETECTION	ON REQUEST	REG. GROUP	REG. BIT	DESCRIPTION
VSYS_MON	Internal event	Rising and falling	Never	INT1	6	System voltage monitoring interrupt Triggered when the system voltage crosses the configured threshold in the VSYS_MON register.
HOTDIE	Internal event	Rising and Falling	Never		5	Hot-die temperature interrupt The embedded thermal monitoring module has detected a die temperature above the hot-die detection threshold. An interrupt is generated in ACTIVE and SLEEP states, not in OFF state.
PWRDOWN	PWRDOWN (pin)	Rising and falling	Never		4	Power-down interrupt Triggered when event is detected on the PWRDOWN pin.
LONG_PRESS_KEY	PWRON (pin)	Falling	Never		2	Power-on long key-press interrupt Triggered when PWRON is low during more than the long-press delay, LONG_PRESS_KEY.LPK_TIME.
PWRON	PWRON (pin)	Falling	Always (INT mask, don't care)		1	Power-on interrupt Triggered when the PWRON button is pressed (low) while the device is on. An interrupt is generated in ACTIVE and SLEEP states, not in OFF state.
SHORT	Internal event	Rising	Yes (if INT not masked)	INT2	6	Short interrupt Triggered when at least one of the power resources (SMPS or LDO) outputs is shorted.
FSD	Internal event	Rising	Yes (if INT not masked)		5	First supply detection interrupt Triggered when a first supply detection is detected. This functions is selected by PMU_SECONDARY_INT.FSD_MASK.
RESET_IN	RESET_IN (pin)	Rising	Never		4	RESET_IN interrupt Triggered when event is detected on the RESET_IN pin.
WDT	Internal event	Rising	Never		2	Watchdog time-out interrupt Triggered when watchdog time-out expires.
OTP_ERROR	Internal event	Rising	Never		1	OTP bit error detection interrupt Triggered when an OTP bit error is detected.
VBUS	VBUS (pin)	Rising and falling	Yes (if INT not masked)	INT3	7	VBUS wake-up comparator interrupt Active in OFF state. Triggered when VBUS present.
GPADC_EOC_SW	Internal event	N/A	Yes (if INT not masked)		2	GPADC software end-of-conversion interrupt Triggered when the conversion result is available.
GPADC_AUTO_1	Internal event	N/A	Yes (if INT not masked)		1	GPADC automatic periodic conversion 1 Triggered when the result of a conversion is either above or below (depending on configuration) reference threshold GPADC_AUTO_CONV1_LSB and GPADC_AUTO_CONV1_MSB.
GPADC_AUTO_0	Internal event	N/A	Yes (if INT not masked)		0	GPADC automatic periodic conversion 0 Triggered when the result of a conversion is either above or below (depending on configuration) reference threshold GPADC_AUTO_CONV0_LSB and GPADC_AUTO_CONV0_MSB.
GPIO_6	GPIO_6 (pin)	Rising, falling, or both	Yes (if INT not masked)	INT4	6	GPIO_6 rising-edge detection interrupt, falling-edge detection interrupt, or detection interrupt for both edges
GPIO_5	GPIO_5 (pin)	Rising, falling, or both	Yes (if INT not masked)		5	GPIO_5 rising-edge detection interrupt, falling-edge detection interrupt, or detection interrupt for both edges
GPIO_4	GPIO_4 (pin)	Rising, falling, or both	Yes (if INT not masked)		4	GPIO_4 rising-edge detection interrupt, falling-edge detection interrupt, or detection interrupt for both edges
GPIO_3	GPIO_3 (pin)	Rising, falling, or both	Yes (if INT not masked)		3	GPIO_3 rising-edge detection interrupt, falling-edge detection interrupt, or detection interrupt for both edges
GPIO_2	GPIO_2 (pin)	Rising, falling, or both	Yes (if INT not masked)		2	GPIO_2 rising-edge detection interrupt, falling-edge detection interrupt, or detection interrupt for both edges
GPIO_1	GPIO_1 (pin)	Rising, falling, or both	Yes (if INT not masked)		1	GPIO_1 rising-edge detection interrupt, falling-edge detection interrupt, or detection interrupt for both edges
GPIO_0	GPIO_0 (pin)	Rising, falling, or both	Yes (if INT not masked)		0	GPIO_0 rising-edge detection interrupt, falling-edge detection interrupt, or detection interrupt for both edges

## 5.12 Control Interfaces

The TPS65919-Q1 device has two, exclusive selectable (from factory settings) interfaces; 2 high-speed I<sup>2</sup>C interfaces (I2C1\_SCL\_SCK or I2C1\_SDA\_SDI and I2C2\_SCL\_SCE or I2C2\_SDA\_SDO) or 1 SPI (I2C1\_SCL\_SCK, I2C1\_SDA\_SDI, I2C2\_SDA\_SDO, or I2C2\_SCL\_SCE). Both are used to fully control and configure the device and have access to all the registers. When the I<sup>2</sup>C configuration is selected (either I2C1\_SCL\_SCK or I2C1\_SDA\_SDI) a general purpose control (GPC) interface is dedicated to configure the device and the I2C2\_SCL\_SCE or I2C2\_SDA\_SDO interface, dynamic voltage scaling (DVS) is dedicated to dynamically change the output voltage of the SMPS converters. The DVS I<sup>2</sup>C interface has access only to the voltage scaling registers of the SMPS converters (R/W mode).

### 5.12.1 I<sup>2</sup>C Interfaces

The GPC I<sup>2</sup>C interface (I2C1\_SCL\_SCK and I2C1\_SDA\_SDI) is dedicated to access the configuration registers of all the resources of the system.

The DVS I<sup>2</sup>C interface (I2C2\_SCL\_SCE and I2C2\_SDA\_SDO) is dedicated to access the DVS registers independently from the GPC I<sup>2</sup>C.

The control interfaces comply with the HS-I<sup>2</sup>C specification and support the following features:

- Mode: Slave only (receiver and transmitter)
- Speed:
  - Standard mode (100 kbps)
  - Fast mode (400 kbps)
  - High-speed mode (3.4 Mbps)
- Addressing: 7-bit mode addressing device

The following features are not supported:

- 10-bit addressing
- General call
- Master mode (bus arbitration and clock generation)

I<sup>2</sup>C is a 2-wire serial interface developed by NXP (formerly Philips Semiconductor) (see *I<sup>2</sup>C-Bus Specification and user manual, Rev 03, June 2007*). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, the SDA and SCL lines are pulled high. All the I<sup>2</sup>C-compatible devices connect to the I<sup>2</sup>C bus through open-drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the start and stop of data transfers. A slave device receives data, transmits data, or both on the bus under control of the master device. The data transfer protocol for standard and fast modes is exactly the same. In this data sheet, these modes are referred to as F/S mode. The protocol for high-speed (HS) mode is different from F/S mode.

#### 5.12.1.1 I<sup>2</sup>C Implementation

The TPS65919-Q1 standard I<sup>2</sup>C 7-bit slave device address is set to 010010xx (binary) where the two least-significant bits are used for page selection.

The device is organized in five internal pages of 256 bytes (registers) as follows:

- Slave device address 0x48: Power registers
- Slave device address 0x49: Interfaces and auxiliaries
- Slave device address 0x4A: Trimming and test
- Slave device address 0x4B: OTP
- Slave device address 0x12: DVS

The device address for the DVS I<sup>2</sup>C interface is set to 0x12.

If one of the addresses conflicts with another device I<sup>2</sup>C address, remapping each address to a fixed alternative address is possible as listed in [表 5-13](#). The I<sup>2</sup>C for DVS is fixed because it is a dedicated interface.

**表 5-13. I<sup>2</sup>C Address Configuration**

REGISTER	BIT	PAGE	ADDRESSES
I2C_SPI	ID_I2C1[0]	Power registers	ID_I2C1[0] = 0: 0x48
			ID_I2C1[0] = 1: 0x58
	ID_I2C1[1]	Interfaces and auxiliaries	ID_I2C1[1] = 0: 0x49
			ID_I2C1[1] = 1: 0x59
	ID_I2C1[2]	Trimming and test	ID_I2C1[2] = 0: 0x4A
			ID_I2C1[2] = 1: 0x5A
	ID_I2C1[3]	OTP	ID_I2C1[3] = 0: 0x4B
			ID_I2C1[3] = 1: 0x5B
ID_IDC2	DVS	ID_I2C2 = 0: 0x12	

### 5.12.1.2 F/S Mode Protocol

The master initiates a data transfer by generating a START condition. The START condition is when a high-to-low transition occurs on the SDA line while SCL is high (see [图 5-17](#)). All I<sup>2</sup>C-compatible devices should recognize a START condition.

The master then generates SCL pulses and transmits the 7-bit address and the read or write direction bit (R/W) on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see [图 5-18](#)). All devices recognize the address sent by the master and compare it to the internal fixed addresses of the respective device. Only the slave device with a matching address generates an acknowledge signal (see [图 5-19](#)) by pulling the SDA line low during the entire high period of the ninth SCL cycle. When this acknowledge signal is detected, the communication link between the master and the slave device has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit 1) or receive data from the slave (R/W bit 0). In either case, the receiver must acknowledge the data sent by the transmitter. An acknowledge signal can be generated by the master or the slave, depending on which device is the receiver. Nine-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue for as long as required.

To signal the end of the data transfer, the master generates a STOP condition by pulling the SDA line from low to high while the SCL line is high (see [图 5-17](#)). Pulling the line from low to high while SCL is high releases the bus and stops the communication link with the addressed slave. All I<sup>2</sup>C-compatible devices must recognize the STOP condition. Upon the receipt of a STOP condition, the slave device must wait for a START condition followed by a matching address.

Attempting to read data from the register addresses not listed in this section results in a read out of 0xFF.

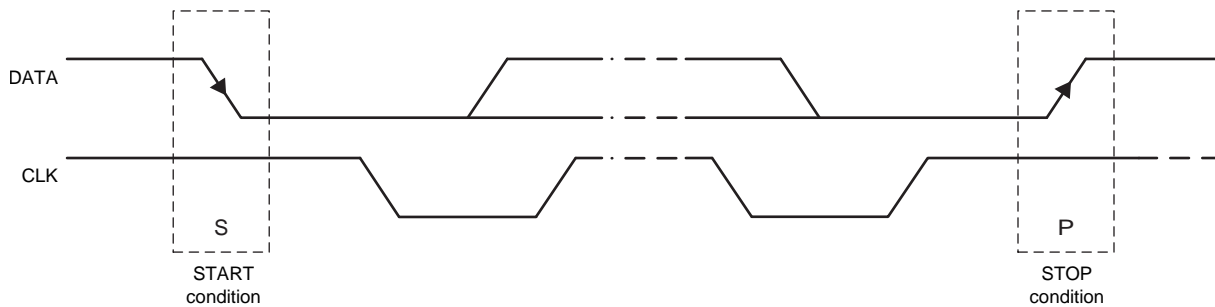
### 5.12.1.3 HS Mode Protocol

When the bus is idle, the SDA and SCL lines are pulled high by the pullup devices.

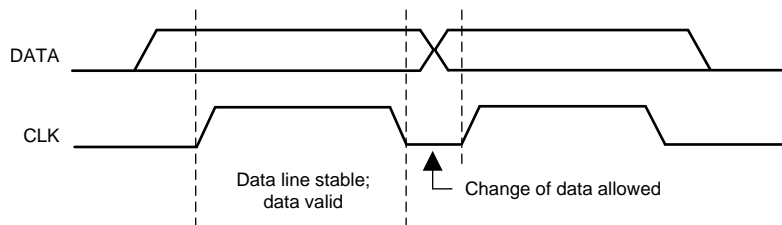
The master generates a START condition followed by a valid serial byte containing the HS master code, 00001XXX. This transmission is made in F/S mode at no more than 400 kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch the internal setting to support 3.4-Mbps operation.

The master then generates a REPEATED START condition (a REPEATED START condition has the same timing as the START condition). After the REPEATED START condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 Mbps are allowed. A STOP condition ends the HS mode and switches all the internal settings of the slave devices to support F/S mode. Instead of using a STOP condition, REPEATED START conditions are used to secure the bus in HS mode.

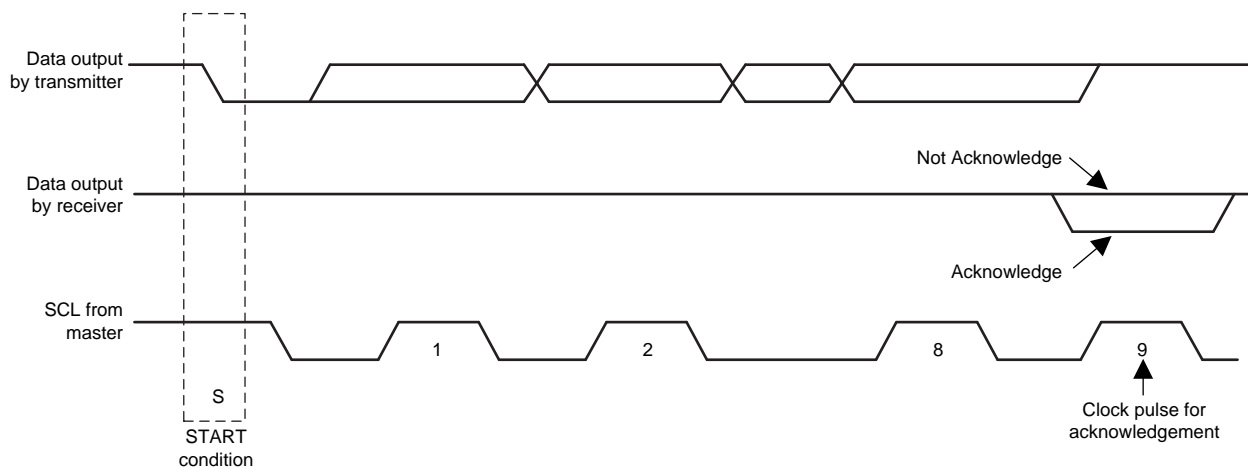
Attempting to read data from register addresses not listed in this section results in a read out of 0xFF.



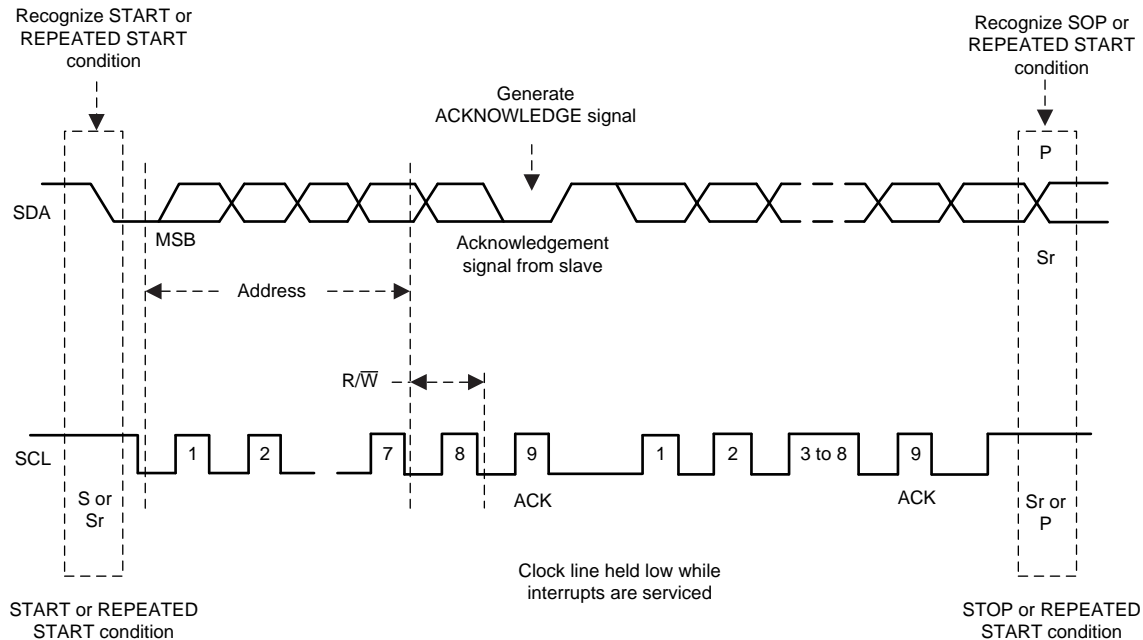
5-17. START and STOP Conditions



5-18. Bit Transfer on the Serial Interface



5-19. Acknowledge on the I<sup>2</sup>C Bus



✎ 5-20. Bus Protocol

### 5.12.2 Serial Peripheral Interface (SPI)

The SPI is a 4-wire slave interface used to access and configure the device. The SPI allows read-and-write access to the configuration registers of all resources of the system.

The SPI uses the following signals:

- SCE (I2C2\_SCL\_SCE): Chip enable which is the input driven by host master. This signal is used to initiate and terminate a transaction
- SCK (I2C1\_SCL\_SCK): Clock which is the input driven by host master. This signal is as master clock for data transaction
- SDI (I2C1\_SDA\_SDI): Data input which is the input driven by host master. This signal is as data line from master to slave
- SDO (I2C2\_SDA\_SDO): Data output which is the output driven by TPS65919-Q1. This signal is as data line from slave to master and defaults to high impedance

#### 5.12.2.1 SPI Modes

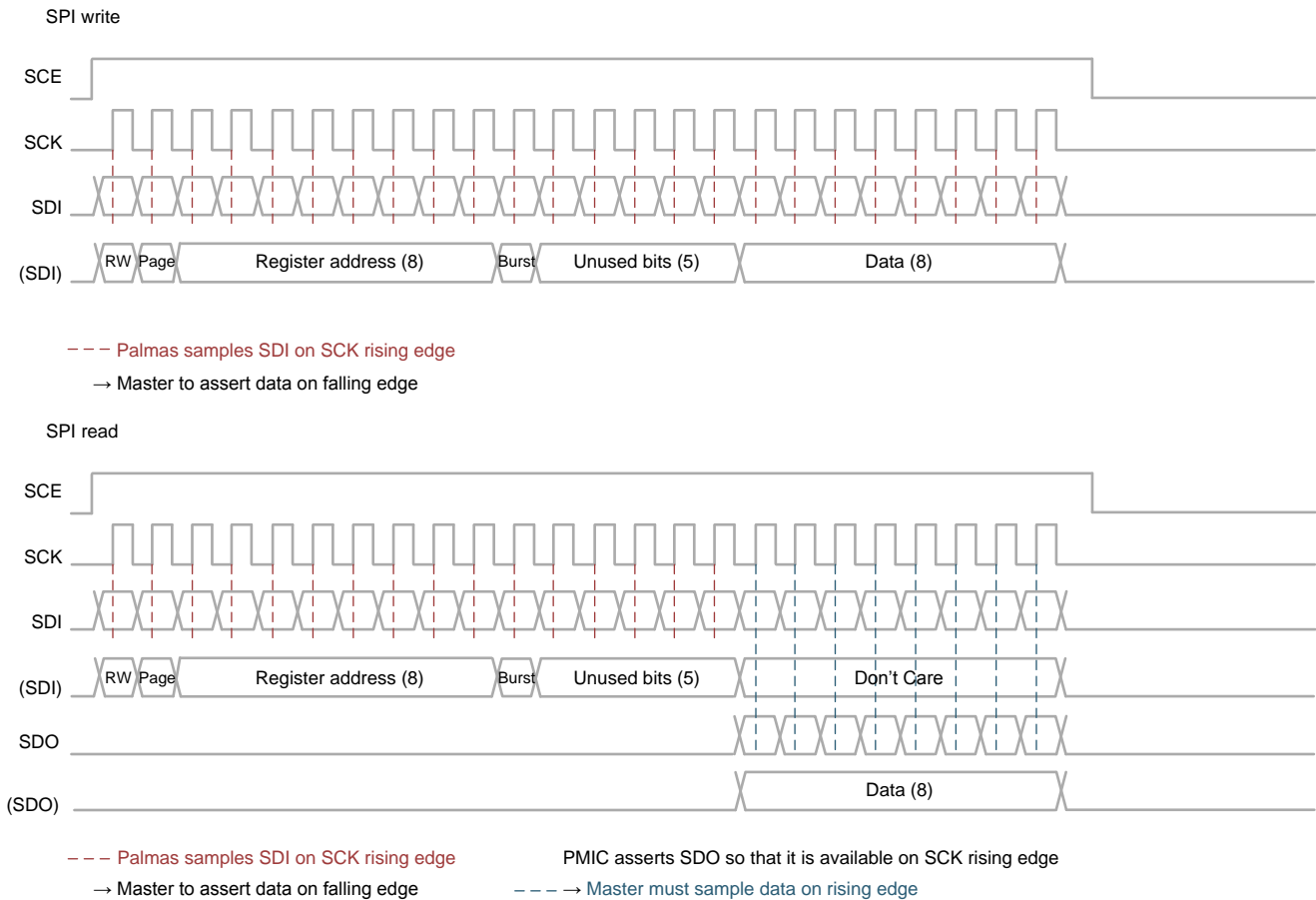
This SPI supports two access modes which are single access and burst access. All shifts occur with the most significant bit (MSB) first (data, address, page). These two access modes have the following features:

- Single access (read or write)
  - This mode consists of fetching and storing one single data location. The protocol is shown in ✎ 5-21.
  - The R/W bit is always provided first, followed by page address and register address fields. When the R/W bit = 0, a read access is performed. When the R/W bit = 1, a write access is performed.
  - One burst bit indicates if the following transfer is a single access (BURST = 0) or a burst access (BURST = 1).
  - Four unused bits follow the burst bit and the 8-bit data is finally either shifted in (write) or out (read).
  - For a write access, the data output line SDO is invalid (useless) during the whole transaction.
  - For a read access, the data output line SDO is invalid during the unused bits (time slot used for data fetch) and then becomes active or valid after the unused bits.

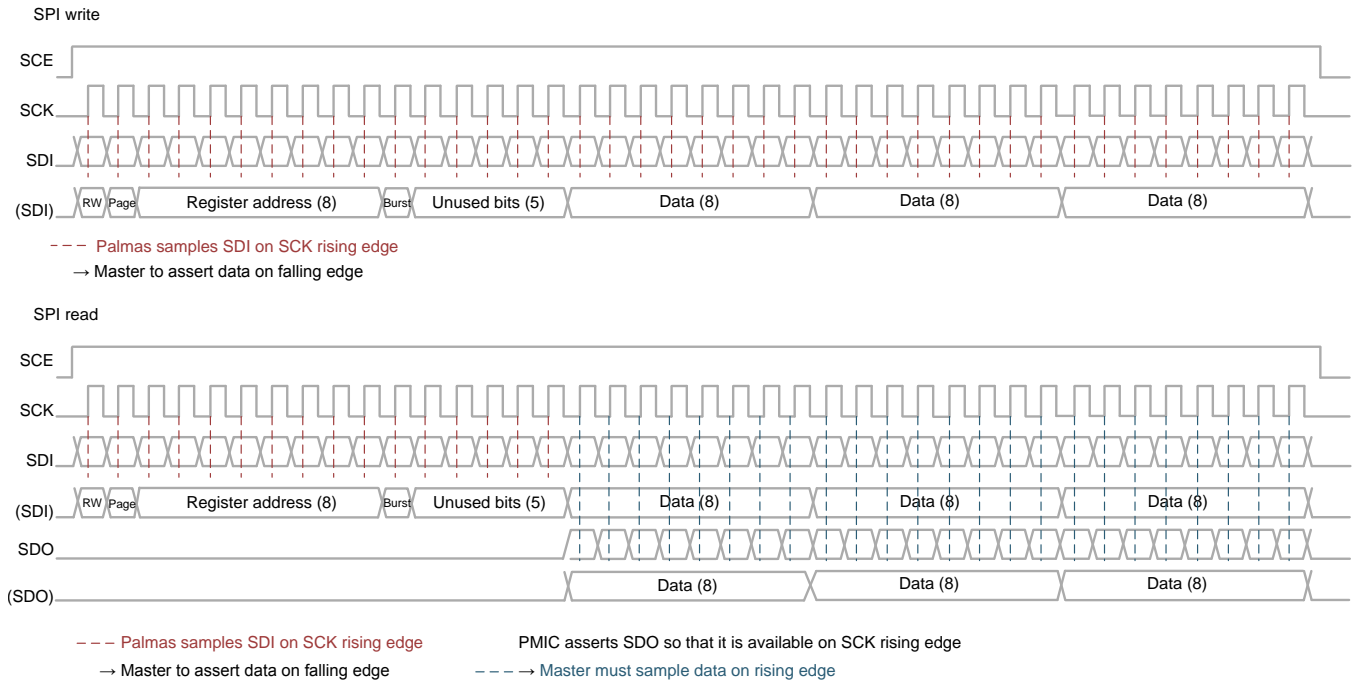
- Burst access (read or write)
  - This mode consists of fetching and storing several data at contiguous locations. The protocol is shown in [Figure 5-22](#).
  - The R/W bit is always provided first, followed by page address and register address fields. When the R/W bit 0, a read access is performed. When the R/W bit 1, a write access is performed.
  - One burst bit indicates if the following transfer is a single access (BURST = 0) or a burst access (BURST = 1).
  - Four unused bits follow the burst bit and packets of 8-bit data are finally either shifted in (write) or out (read).
  - The transaction remains active as long as the SCE signal is maintained high by the host.
  - The address is automatically incremented internally for each new 8-bit packet received.
  - The host must pull the SCE signal low after a complete 8-bit data is transferred, otherwise the last transaction is discarded.
  - For a write access, the data output line SDO is invalid (useless) during the whole transaction.
  - For a read access, the data output line SDO is invalid during the unused bits (time slot used for data fetch) and then becomes active or valid after the unused bits.

### 5.12.2.2 SPI Protocol

[Figure 5-21](#) shows the SPI protocol for a single read and write access. [Figure 5-22](#) shows the SPI protocol for a burst read and write access.



**Figure 5-21. SPI Single Read and Write Access**



**Figure 5-22. SPI Burst Read and Write Access**

### 5.13 OTP Configuration Memory

The register mapping for the device describes the OTP configuration bits. These bits are highlighted as the value X during reset in the register mapping (the value of the bit is the copy of the OTP configuration memory).

### 5.14 Watchdog Timer (WDT)

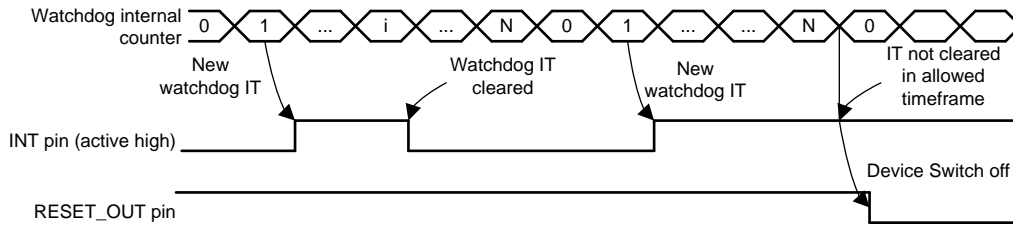
The watchdog timer has two modes of operation: periodic mode and interrupt mode.

In periodic mode, an interrupt is generated with a regular period  $N$ , defined by the setting of WATCHDOG.TIMER. This interrupt is generated at the beginning of the period (when the watchdog internal counter equals 1). The IC initiates a shutdown at the end of the period (when the internal counter reaches  $N$ ) only if the interrupt is not cleared within the defined time frame (0 to  $N$ ). In this mode, when the interrupt is cleared, the internal counter is not reset. The counter continues counting until it reaches the maximum value (defined by the TIMER setting) and automatically rolls over to 0 to start a new counting period. Regardless of when the interrupt is cleared within a given period ( $N$ ), the next interrupt is generated only when the ongoing period completes (reaches  $N$ ). The internal watchdog counter is initialized and kept at 0 as long as the RESET\_OUT pin is low. The watchdog counter begins counting when the RESET\_OUT pin is released.

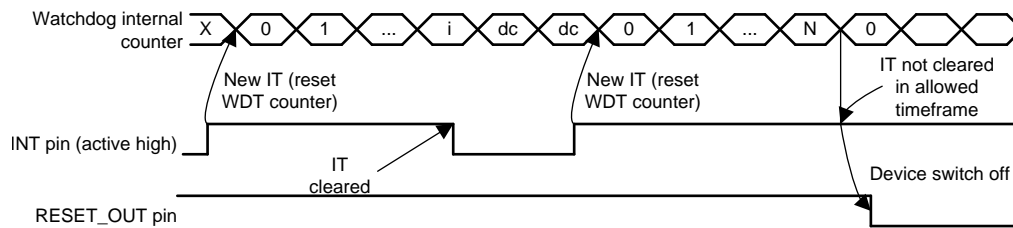
In interrupt mode, any interrupt source resets the watchdog counter and starts the counting. If the sources of the interrupts are not cleared (meaning the INT line is released) before the end of the predefined period,  $N$  (set by WATCHDOG.TIMER setting), then the device initiates a shutdown. If the sources of the interrupts are cleared within the predefined period, then the watchdog counter is discarded (dc) and no shutdown sequence is initiated.

By default, the watchdog is disabled. The watchdog can be enabled by setting the ENABLE bit of the WATCHDOG register to 1, and this selection is write protected by setting the LOCK bit to 1. Reset of the device returns these bits to default values.

Figure 5-23 and Figure 5-24 show the watchdog timings.



5-23. Watchdog Timings—Periodic Mode



5-24. Watchdog Timings—Interrupt Mode

### 5.15 System Voltage Monitoring

Comparators that monitor the voltage on the VCC\_SENSE, and VCCA pins control the power state machine of the TPS65919-Q1 device. For electrical parameters, see [Section 4.12](#).

**POR** When the supply at the VCCA pin is below the POR threshold, the TPS65919-Q1 device is in the NO SUPPLY state. All functionality is off. The device moves from the NO SUPPLY state to the BACKUP state when the voltage in VCCA rises above the POR threshold.

**VSYS\_LO** When the voltage on the VCCA pin rises above VSYS\_LO, the device enters from the BACKUP state to the OFF state. When the device is in an ACTIVE, SLEEP, or OFF state and the voltage on VCCA decreases below the VSYS\_LO level, the device enters backup mode. When the device transitions from the ACTIVE state to the BACKUP state, all active SMPS and LDO regulators, except LDOVRTC, are disabled simultaneously. There is a 180-µs deglitch time after VCCA becomes less than VSYS\_LO and before the regulators are disabled. The level of VSYS\_LO is OTP programmable.

**VSYS\_MON** During power up, the value of VSYS\_HI OTP is used as a threshold for the VSYS\_MON comparator which is gating PMIC start-up (that is, as a threshold for transition from the OFF state to the ACTIVE state). The VSYS\_MON comparator monitors the VCC\_SENSE pin. After power up, software can configure the comparator threshold in the VSYS\_MON register.

5-25 shows a block diagram of the system comparators and 5-26 shows the state transitions.



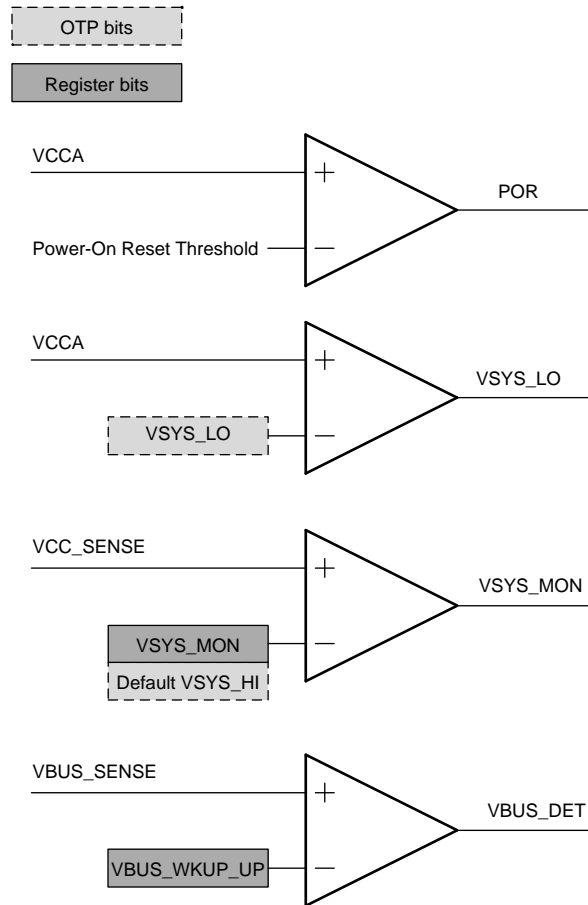


图 5-25. System Comparators

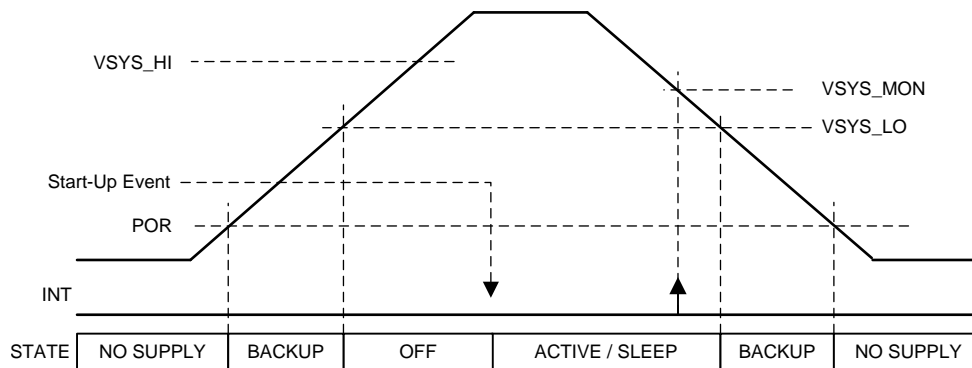


图 5-26. State Transitions

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To generate a POR from a falling  $V_{CC}$ ,  $V_{CC}$  is sampled every 1 ms and compared to the POR threshold. In case  $V_{CC}$  is discharged and resupplied quickly, a POR may not be reliably generated if  $V_{CC}$  crosses the POR threshold between samples. Another way to generate POR is to discharge the LDOVRTC regulator to 0 V after  $V_{CC}$  is removed. With no external load, this could take seconds for the LDOVRTC output to discharge to 0 V. The PMIC should not be restarted after  $V_{CC}$  is removed but before LDOVRTC is discharged to 0 V. If necessary, TI recommends adding a pulldown resistor from the LDOVRTC output to GND with a minimum of 3.9 k $\Omega$  to speed up the LDOVRTC discharge time.

The value of the pulldown resistor should be chosen based on the desired discharge time and acceptable current draw in the OFF state, but no greater than 0.5 mA. Use 式 7 to calculate the pulldown resistor based on the desired discharge time.

$$R_{PD} \text{ (k}\Omega\text{)} = \frac{t_{\text{discharge}} \text{ (ms)}}{C_O \text{ (}\mu\text{F)} \times 3}$$

where

- $t_{\text{discharge}}$  = discharge time of the VRTC output
  - $R_{PD}$  = pulldown resistance from the VRTC output to GND
  - $C_O$  = output capacitance on the VRTC line (typically 2.2  $\mu\text{F}$ )
- (7)

Because LDOVRTC is always on when VCC is supplied, additional current is drawn through the pulldown resistor. The output current of LDOVRTC while the PMIC is in OFF state should not exceed 0.5 mA. Use 式 8 to calculate the pulldown current.

$$I_{PD} = \frac{1.8 \text{ V}}{R_{PD}}$$

where

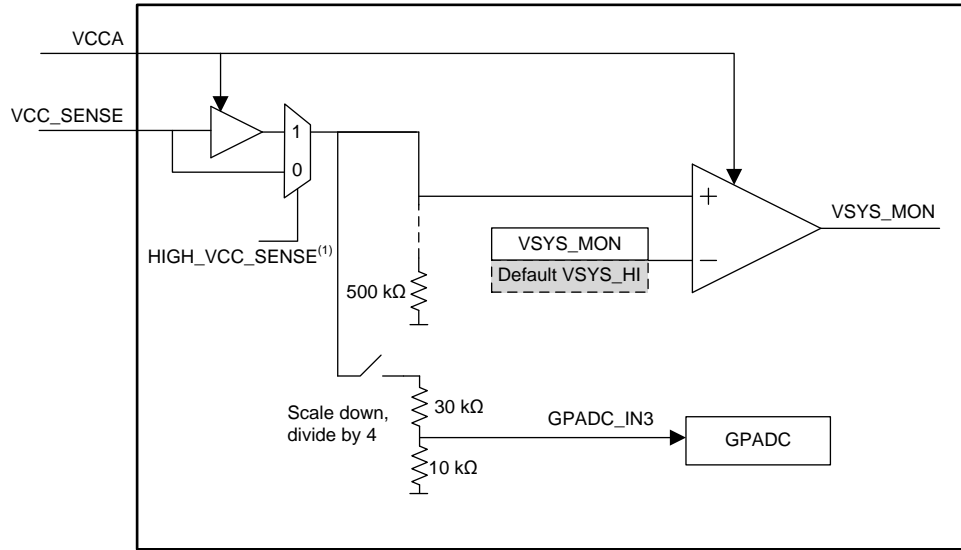
- $I_{PD}$  = current through the pulldown resistor
  - $R_{PD}$  = pulldown resistance from the VRTC regulator
- (8)

To use comparators in the system:

- The VSYS\_HI and VSYS\_LO thresholds are defined in the OTP. Software cannot change these levels.
- After startup, the VSYS\_MON comparator is automatically disabled. Software can select new threshold levels using the VSYS\_MON register and then enable the comparators.
- To have the same coding for rising and falling edge, the VSYS\_MON comparator does not include hysteresis and thus can generate multiple interrupts when the voltage level is at threshold level. New interrupt generation has a 125- $\mu\text{s}$  debounce time. This time lets software mask the interrupt and update the threshold level or disable the comparator before receiving a new interrupt.

☒ 5-27 shows more details on VSYS\_MON comparator. When the VSYS\_MON comparator is enabled, and the internal buffer is bypassed, the input impedance at VCC\_SENSE pin is 500 k $\Omega$  (typical). When the comparator is disabled, the VCC\_SENSE pin is in the high-impedance state. If GPADC is enabled to measure channel 2 or channel 3, 40 k $\Omega$  is added in parallel to the corresponding comparator. See 表 5-9 for GPADC input range.

To enable system voltage sensing above 5.25 V, an external resistive divider can be used. Internal buffers can be enabled by setting the OTP bit HIGH\_VCC\_SENSE to 1 to provide high impedance for the external resistive dividers. The maximum input level for the internal buffer is VCCA – 1 V.



(1) **HIGH\_VCC\_SENSE = 0:** buffer bypassed (not enabled). **HIGH\_VCC\_SENSE = 1:** buffer enabled, bypass disabled (Hi-Z at SENSE input)

5-27. VSYS\_MON Comparator Details

## 5.16 Register Map

### 5.16.1 Functional Register Mapping

For the register descriptions, refer to the [TPS65919-Q1 Register Map](#).

## 5.17 Device Identification

The following registers can differentiate the TPS65919-Q1 device being used.

表 5-14. TPS65919-Q1 Device ID

REGISTER NAME	REGISTER DESCRIPTION	VALUE
PRODUCT_ID_MSB	For all TPS65919-Q1 devices, this register will have the same value.	0x09
PRODUCT_ID_LSB	For all TPS65919-Q1 devices, this register will have the same value.	0x17
DESIGNREV	This register distinguishes which silicon version is used.	Revision 1.0
		Revision 1.1
SW_REVISION	This register will be representative of the OTP version programmed on the device.	OTP dependent - See User's Guide

## 6 Applications, Implementation, and Layout

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### 注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

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### 6.1 Application Information

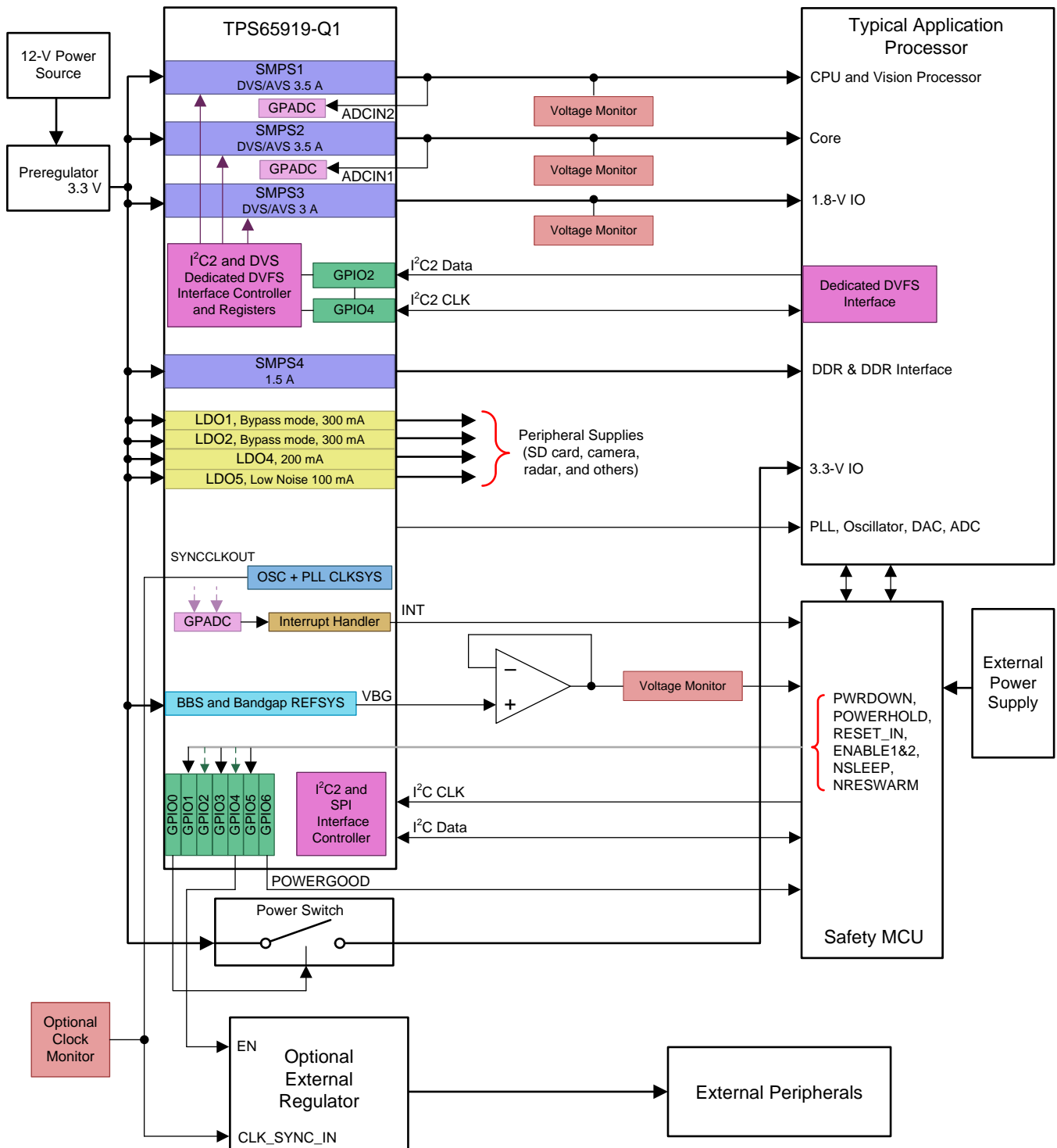
The TPS65919-Q1 device is an integrated power management integrated circuits (PMIC), available in a 48-pin, 0.5-mm pitch, 7-mm × 7-mm QFN package. It has four configurable step-down converter rails, with two of these SMPSs capable of combining power rails and supply up to 7 A of output current in multi-phase mode. These step-down converters can be synchronized to an external clock between 1.7 MHz to 2.7 MHz, or an internal fallback clock at 2.2 MHz. The TPS65919-Q1 device also has four external LDOs which can be supplied from the system supply or a pre-regulated supply. Two of these LDOs can be configured in bypass mode. One of the five LDOs also provides low noise output.

The TPS65919-Q1 device also come with a 12-bit GPADC with two external channels, seven configurable GPIOs, two I<sup>2</sup>C interface channels or one SPI interface channel, a PLL for external clock sync and phase delay capability, and a programmable power sequencer and control for supporting different processors and applications.

As TPS65919-Q1 device is a highly integrated PMIC device, it is very important that customers should take necessary actions to ensure the PMIC is operating under the recommended operating conditions to ensure desired performance from the device. Additional cooling strategies may be necessary to maintain the junction temperature below maximum limit allowed for the device. To minimize the interferences when turning on a power rail while the device is in operation, optimal PCB layout and grounding strategy are essential and are recommended in 6.3. In addition, customer may take steps such as turning on additional rails only when the systems is operating in light load condition.

Details on how to use this device as a power management device for a application processor are described throughout this device specification. The following sections provides the typical application use case with the recommended external components and layout guidelines. A design checklist for the TPS65919-Q1 device is also available on which provides application design guidance and cross checks.

## 6.2 Typical Application



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Figure 6-1. Application Diagram in a Typical ADAS System

### 6.2.1 Design Requirements

For a typical ADAS application shown in [图 6-1](#), [表 6-1](#) lists the key design parameters of the power resources.

**表 6-1. Design Parameters**

DESIGN PARAMETER	VALUE
Supply voltage	3.3 V to 5 V
Switching frequency	2.2 MHz
SMPS1 voltage	1.15 V
SMPS1 current	Up to 3.5 A
SMPS2 voltage	1.15 V
SMPS2 current	Up to 3.5 A
SMPS3 voltage	1.8 V
SMPS3 current	Up to 3 A
SMPS4 voltage	1.35 V or 1.5 V
SMPS4 current	Up to 1.5 A
LDO1 voltage	1.8 V or 3.3 V
LDO1 current	Up to 300 mA
LDO2 voltage	1.8 V
LDO2 current	Up to 300 mA
LDO4 voltage	3.3 V
LDO4 current	Up to 200 mA
LDO5 voltage	1.8 V
LDO5 current	Up to 100 mA

## 6.2.2 Detailed Design Procedure

lists the recommended external components.

**表 6-2. Recommended External Components**

REFERENCE COMPONENTS	COMPONENT <sup>(1)</sup>	MANUFACTURER	PART NUMBER	VALUE	EIA size code <sup>(2)</sup>	SIZE (mm)	MASS PRODUCTION <sup>(3)</sup>
<b>INPUT POWER SUPPLIES EXTERNAL COMPONENTS</b>							
C1, C2	VSYS and VCCA tank capacitor <sup>(4)</sup>	Murata	GCM21BR70J106KE22	10 $\mu$ F, 6V3	0805	2 x 1.25 x 1.25	Available <sup>(5)</sup>
C3	Decoupling capacitor	Murata	GCM155R71C104KA55	100 nF, 16 V	0402	1 x 0.5 x 0.5	Available <sup>(5)</sup>
<b>BANDGAP EXTERNAL COMPONENTS</b>							
C7	Capacitor	Murata	GCM155R71C104KA55	100 nF, 16 V	0402	1 x 0.5 x 0.5	Available <sup>(5)</sup>
<b>SMPS EXTERNAL COMPONENTS</b>							
C8, C9, C10, C11	Input capacitor	Murata	GCM21BC71A475MA735	4.7 $\mu$ F 10 V	0805	2 x 1.25 x 1.25	Available <sup>(5)</sup>
C13, C14, C15, C16	Output capacitor	Murata	GCM32ER70J476KE19	47 $\mu$ F 10 V	1210	3.2 x 2.5 x 2.5	Available <sup>(5)</sup>
L1, L2, L3, L4	Inductor	VISHAY	IHLP1616ABER1R0M11	1 $\mu$ H		4.45 x 4.1 x 1.2	Available <sup>(5)</sup>
<b>LDO EXTERNAL COMPONENTS</b>							
C18, C19	Input capacitor	Murata	GCM188R70J225KE22	2.2 $\mu$ F 6V3	0603	1.6 x 0.8 x 0.8	Available <sup>(5)</sup>
C4, C5, C20, C21, C23, C24	Output capacitor	Murata	GCM188R70J225KE22	2.2 $\mu$ F 6V3	0603	1.6 x 0.8 x 0.8	Available <sup>(5)</sup>

- (1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.
- (2) The PACK column describes the external component package type.
- (3) This column refers to the criteria.
- (4) The tank capacitors filter the VSYS and VCCA input voltage of the LDO and SMPS core architectures.
- (5) Component used on the validation boards.

### 6.2.2.1 SMPS Input Capacitors

All SMPS inputs require an input decoupling capacitor to minimize input ripple voltage. Using a 10-V, 4.7- $\mu$ F capacitor for each SMPS is recommended. Depending on the input voltage of the SMPS, a 6.3-V or 10-V capacitor can be used.

For optimal performance, the input capacitors should be placed as close to the SMPS input pins as possible. See the [6.3.1](#) section for more information about component placement.

### 6.2.2.2 SMPS Output Capacitors

All SMPS outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. To ensure stability across the entire switching frequency range, the TPS65919-Q1 device requires an output capacitance value between 33  $\mu$ F and 57  $\mu$ F. To meet this requirement across temperature and DC bias voltage, using a 47- $\mu$ F capacitor for each SMPS is recommended. Remember that each SMPS requires an output capacitor, not just each output rail. For example, SMPS12 is a dual-phase regulator and an output capacitor is required for the SMPS1 output and the SMPS2 output. Note, this requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. Additional capacitance placed near the load can be supported, but the end application or system should be evaluated for stability.

### 6.2.2.3 SMPS Inductors

Again, to ensure stability across the entire switching frequency range, using a 1- $\mu$ H inductor on each SMPS is recommended. Remember that each SMPS requires an inductor, not just each output rail. For example, SMPS12 is a dual-phase regulator and an inductor is required for the SMPS1\_SW pins and the SMPS2\_SW pins.

### 6.2.2.4 LDO Input Capacitors

All LDO inputs require an input decoupling capacitor to minimize input ripple voltage. Using a 2.2- $\mu$ F capacitor for each LDO is recommended. Depending on the input voltage of the LDO, a 6.3-V or 10-V capacitor can be used.

For optimal performance, the input capacitors should be placed as close to the LDO input pins as possible. See the [6.3.1](#) section for more information about component placement.

### 6.2.2.5 LDO Output Capacitors

All LDO outputs require an output capacitor to hold up the output voltage during a load step or changes to the input voltage. Using a 2.2- $\mu$ F capacitor for each LDO output is recommended. Note, this requirement excludes any capacitance seen at the load and only refers to the capacitance seen close to the device. Additional capacitance placed near the load can be supported, but the end application or system should be evaluated for stability.

### 6.2.2.6 VCCA

VCCA is the supply for the analog input voltage of the device. This pin requires a 10- $\mu$ F decoupling capacitor.

Texas Instruments recommends to always power down the TPS65919-Q1 before removing power from VCCA. If the input voltage to the device is removed while the device is ACTIVE, the device will shut off when VCCA reaches the VSYS\_LO threshold. As mentioned in the [5.15](#) section, once VCCA reaches VSYS\_LO, there is about 180 us delay before all the output rails are disabled simultaneously.

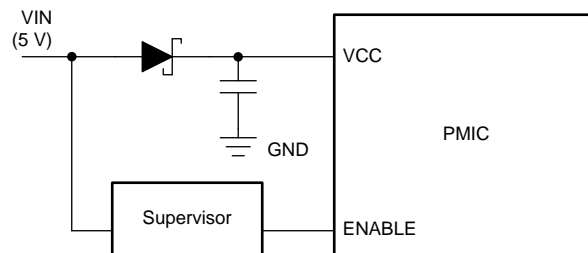
There are two scenarios to consider in the system-level design in the event of unexpected loss of power.



### 6.2.2.6.1 Meeting the Power-Down Sequence

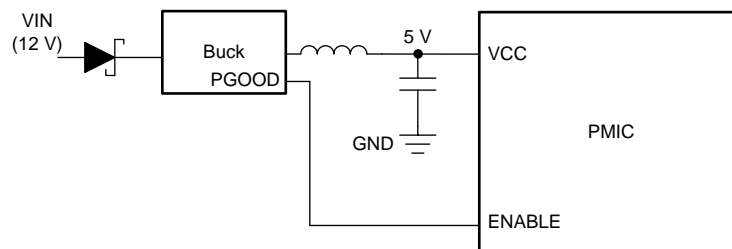
To prevent a sequencing violation, it is important to block reverse current and implement a disable signal to the PMIC. A Schottky diode can block reverse current when the input is removed. Additionally, capacitors can help maintain the input voltage level while the power-down sequence occurs. Depending on the system design, there are a couple ways to implement a disable signal.

For a system where the TPS65919-Q1 is powered by the system input voltage, a supervisor can be used to create a logic signal, indicating if the power is at a good level. An example of this solution is shown in [Figure 6-2](#).



**Figure 6-2. Supporting Uncontrolled Power Down When the PMIC is Supplied by the System Input Voltage**

An alternative solution is possible when a pre-regulator is present. In the case of the pre-regulator, the pre-regulator output capacitance can also act as the energy storage to maintain VCCA for the necessary time. The total supply capacitance should be calculated to support the worst-case leakage current during power down so that the voltage is maintained until the power-down sequence completes. [Figure 6-3](#) shows an example of this configuration.



**Figure 6-3. Supporting Uncontrolled Power Down when the PMIC is Supplied by a Preregulator**

To determine the capacitance needed at the output of the pre-regulator, use [Equation 9](#). This equation is used to ensure that the power down sequence is complete before the device is disabled.

$$C = I \times \Delta T / (V_{CCA} - V_{SYS\_LO})$$

where

- C is total capacitance on VCCA, including preregulator output capacitance and PMIC input capacitance
- I is the total current on the PMIC input supply
- $\Delta T$  is the time it takes the power-down sequence to complete
- VCCA is the voltage at the VCCA pin
- VSYS\_LO is the threshold where the device is disabled

(9)

### 6.2.2.6.2 Maintaining Sufficient Input Voltage

In the event of high loading during loss of input voltage, there is a risk to go below the voltage level necessary for the internal logic of the device to work properly before the device is disabled. This means that when the VCCA voltage supply level becomes lower than the VSYS\_LO threshold, the input voltage may continue dropping to very low voltages during the 180 us  $\pm 10\%$  delay before the device is disabled.

If a large input voltage drop occurs before the device is disabled, the internal logic can no longer properly drive the FETs of the SMPS, and it is possible that the high-side FET and low-side FET of the SMPS are on at the same time. In the event that the high-side and low-side FETs for an SMPS are on at the same time, there is a direct path from SMPSx\_IN to GND, allowing cross-conduction and possible damage of the device.

In order to prevent damage or irregular switching behavior, it is important that the voltage at the SMPSx\_IN pin stays above 1.8 V, including negative transients, before the device is disabled. The minimum voltage seen at the SMPSx\_IN pin is dependent on VCCA and the PCB inductance between the SMPSx\_IN pin and the input capacitor. Use 式 10 to determine the minimum capacitance needed on VCCA to ensure that the device continues switching properly before it is disabled.

$$C = I \times \Delta T / (V_{SYS\_LO} - V_{CCA\_MIN})$$

where

- C is total capacitance on VCCA, including preregulator output capacitance and PMIC input capacitance
- I is the total current on the PMIC input supply
- $\Delta T$  is the maximum debounce time after VCCA = VSYS\_LO before the device switches off (198us)
- VSYS\_LO is the threshold where the device is disabled
- VCCA\_MIN is the minimum VCCA voltage to keep the SMPSx\_IN transients above 1.8 V (10)

When measuring the SMPSx\_IN and VCCA during power down, use active differential probes and a high resolution oscilloscope (4GS/sec or more). VCCA can be measured over the 10uF input capacitor. However, SMPSx\_IN must be measured at the pin in order to measure the transients on this rail accurately. To measure SMPSx\_IN, place the negative lead of the differential probe at a nearby GND, such as the GND of the SMPSx\_IN input capacitor. Place the positive lead of the differential probe directly on the exposed metal of the SMPSx\_IN pin. With this set up, verify that SMPSx\_IN, including the ripple on this signal, does not drop below 1.8V before the SMPS stops switching. See 图 6-4 for an example of how to take this measurement. For ways to decrease the amplitude of the transient spikes, see 表 6-3 for recommended parasitic inductance requirements.

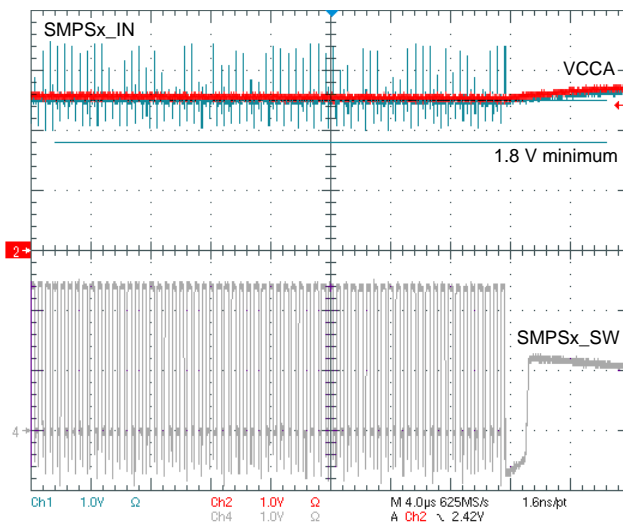


图 6-4. Waveform of SMPSx\_IN Transients

### 6.2.2.7 VIO\_IN

VIO\_IN is the supply for the interface IO circuits inside the device. This pin requires a 0.1- $\mu$ F decoupling capacitor.

### 6.2.2.8 GPADC

To perform a software conversion with the GPADC, use the following steps:

1. Enable software conversion mode – GPADC\_SW\_SELECT.SW\_CONV\_EN
2. Select the channel to convert – GPADC\_SW\_SELECT.SW\_CONV0\_SEL
  - For channel 0, set up the current source in the GPADC\_CTRL1 register if needed.
3. For minimum latency, the GPADC can be set to always on (instead of default enabled from conversion request) by GPADC\_CTRL1.GPADC\_FORCE.
4. Unmask software conversion interrupt – INT3\_MASK.GPADC\_EOC\_SW
5. Start conversion – GPADC\_SW\_SELECT.SW\_START\_CONV0.
6. An interrupt is generated at the end of the conversion INT3\_STATUS.GPADC\_EOC\_SW.
7. Read conversion result – GPADC\_SW\_CONV0\_MSB and GPADC\_SW\_CONV0\_LSB
8. Expected result =  $\text{dec}(\text{GPADC\_SW\_CONV0\_MSB}[3:0].\text{GPADC\_SW\_CONV0\_LSB}[7:0]) / 4096 \times 1.25 \times \text{scaler}$

To perform an auto conversion with the GPADC, use the following steps:

1. Select the channel to convert – GPADC\_AUTO\_SELECT.AUTO\_CONV0\_SEL
2. Configure auto conversion frequency – GPADC\_AUTO\_CTRL.COUNTER\_CONV
3. Set the threshold level for comparison – GPADC\_THRESH\_CONV0\_MSB.THRESH\_CONV0\_MSB, GPADC\_THRESH\_CONV0\_LSB.THRESH\_CONV0\_LSB
  - Level = expected voltage threshold / (1.25 × scaler) × 4096 (in hexadecimal)
4. Set if the interrupt is triggered when conversion is above or below threshold – GPADC\_THRESH\_CONV0\_MSB.THRESH\_CONV0\_POL
5. Triggering the threshold level can also be programmed to generate shutdown – GPADC\_AUTO\_CTRL.SHUTDOWN\_CONV0
6. Unmask AUTO\_CONV\_0 interrupt – INT3\_MASK.GPADC\_AUTO\_0
7. Enable AUTO\_CONV0 – GPADC\_AUTO\_CTRL.AUTO\_CONV0\_EN
8. When selected channel crosses programmed threshold, interrupt is generated – INT3\_STATUS.GPADC\_AUTO\_0
9. Conversion results are available – GPADC\_AUTO\_CONV0\_MSB, GPADC\_AUTO\_CONV0\_LSB
10. If shutdown was enabled, chip switches off after SWOFF\_DLY, unless interrupt is cleared

Both examples above are for CONV0; a similar procedure applies to CONV1.

### 6.2.3 Application Curves

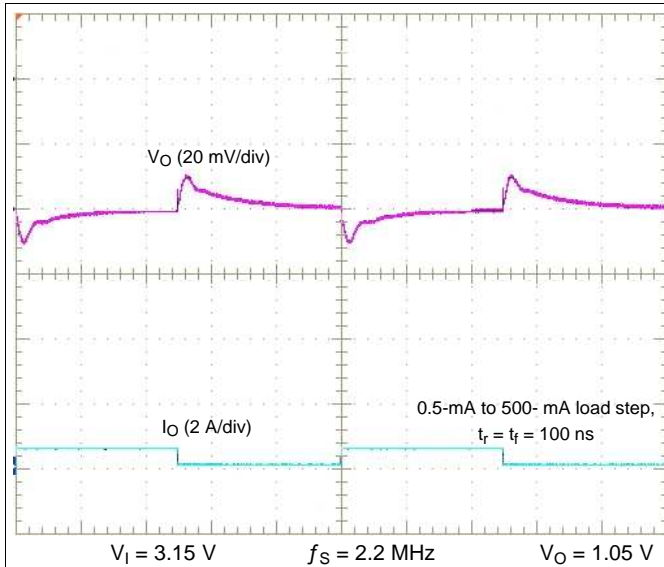


图 6-5. Typical SMPS Load Transient Response for SMPS12 in Dual Phase Mode

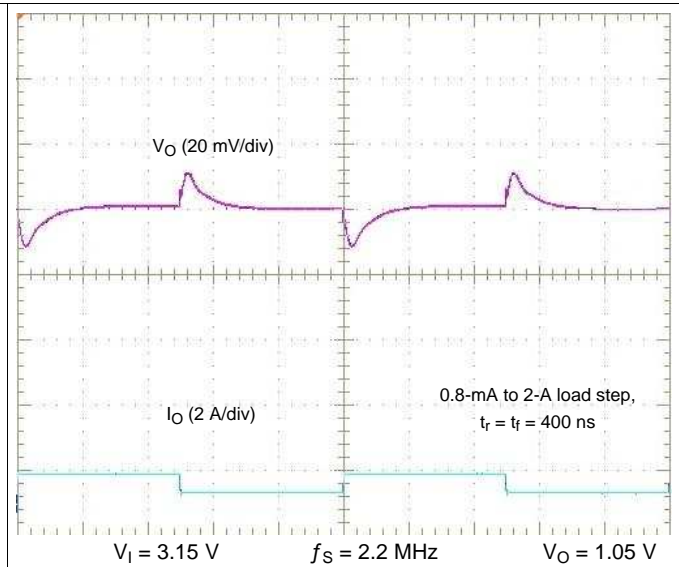


图 6-6. Typical SMPS Load Transient Response for SMPS12 in Dual Phase Mode

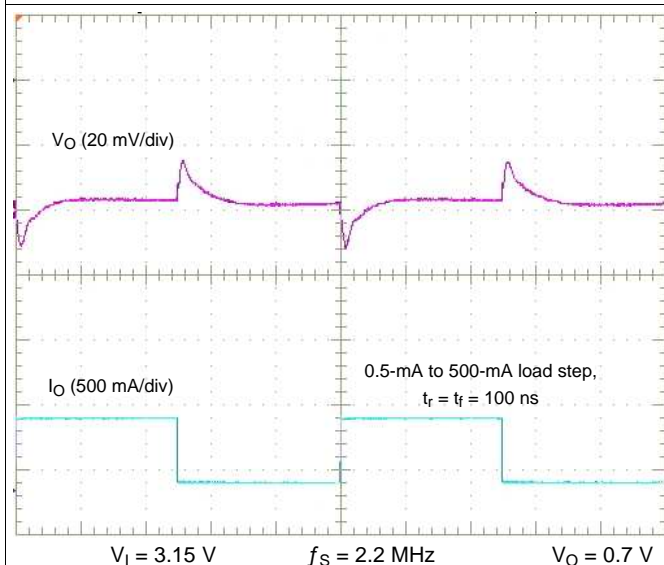


图 6-7. Typical SMPS Load Transient Response for SMPS1, SMPS2, SMPS3

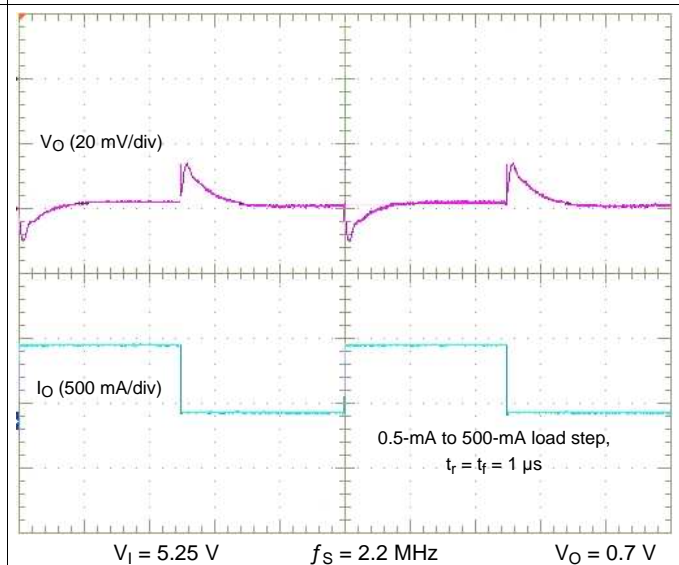


图 6-8. Typical SMPS Load Transient Response for SMPS4

## 6.3 Layout

### 6.3.1 Layout Guidelines

As in every switch-mode-supply design, general layout rules apply:

- Use a solid ground-plane for the power ground (PGND)
- Connect those grounds at a star-point that is located ideally underneath the device.
- Place input capacitors as close as possible to the input pins of the device. This placement is paramount and more important than the output-loop.
- Place the inductor and output capacitor as close as possible to the phase node (or switch-node) of the device.
- Keep the loop-area formed by the phase-node, inductor, output-capacitor, and PGND as small as possible.
- For traces and vias on power-lines, keep inductance and resistance as small as possible by using wide traces. Avoid switching layers but, if needed, use plenty of vias.

The goal of these guidelines is a layout that minimizes emissions, maximizes EMI immunity, and maintains a safe operating area (SOA) for the device.

To minimize the spiking at the phase-node for both the high-side (VIN to SWx) and low-side (SWx to PGND), the decoupling of VIN is the most important guideline. Appropriate decoupling and thorough layout should ensure that the spikes never exceed 7V across the high-side and low-side FETs.

Figure 6-9 shows a set of guidelines regarding parasitic inductance and resistance that are recommended.

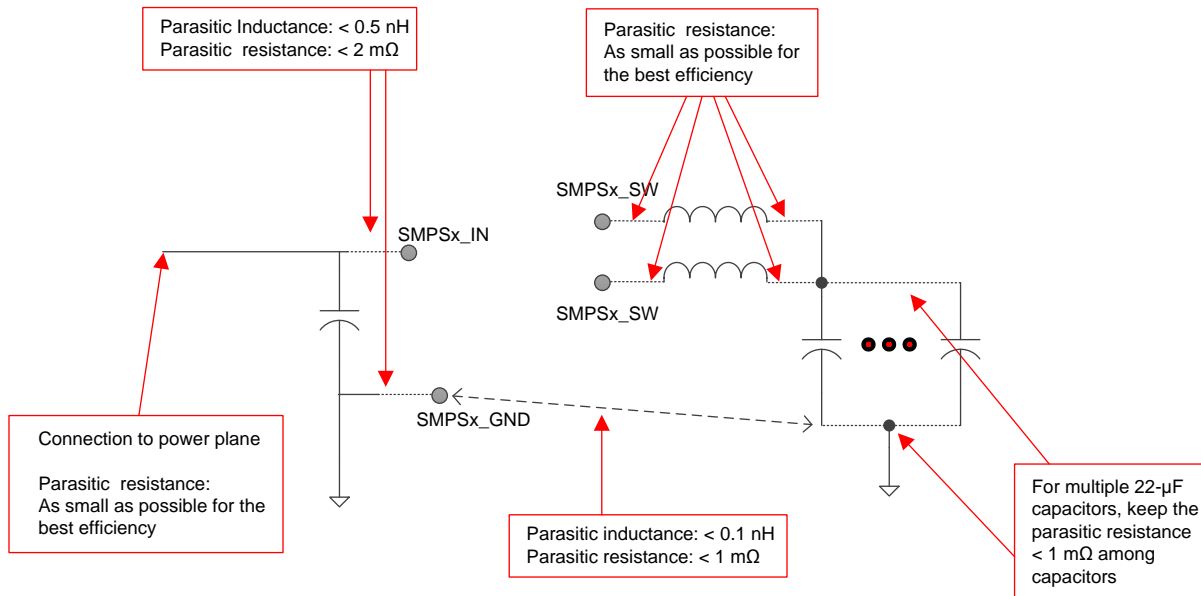


Figure 6-9. Parasitic Inductance and Resistance

Table 6-3 lists the maximum allowable parasitic (inductance measured at 100 MHz) and the achievable values in an optimized layout.

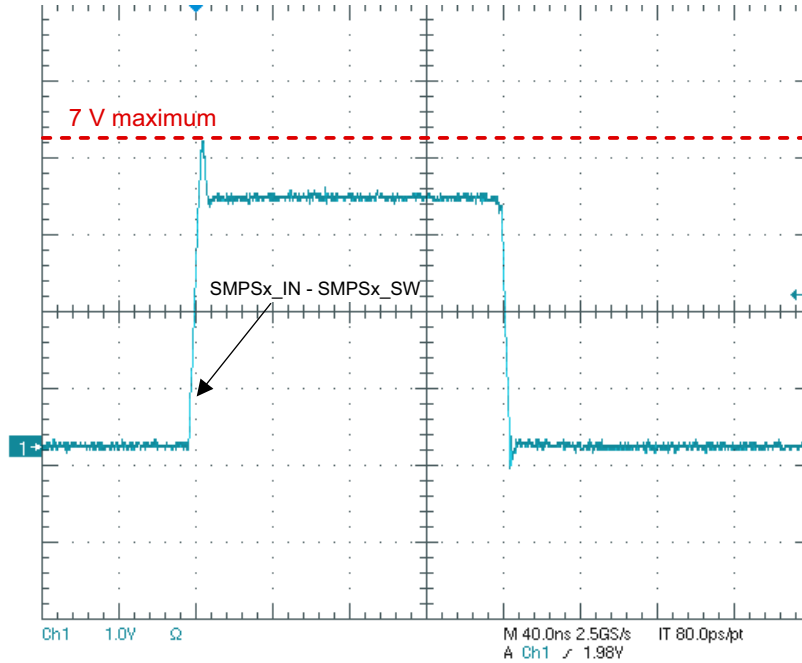
表 6-3. Maximum Allowable Parasitic

CONNECTION	MAXIMUM ALLOWABLE INDUCTANCE	MAXIMUM ALLOWABLE RESISTANCE	OPTIMIZED LAYOUT (EVM) INDUCTANCE		OPTIMIZED LAYOUT (EVM) RESISTANCE	
PowerPlane to C <sub>IN</sub>	N/A	N/A for SOA Maintain a low resistance value for efficiency	N/A		N/A for SOA Maintain a low resistance value for efficiency	
C <sub>IN</sub> to SMPS <sub>x</sub> _IN	0.5 nH	2 mΩ	SMPS1	0.2 nH	SMPS1	1.1 mΩ
			SMPS2	0.2 nH	SMPS2	1.6 mΩ
			SMPS3	0.2 nH	SMPS3	1.5 mΩ
			SMPS4	0.2 nH	SMPS4	1.8 mΩ
C <sub>IN</sub> to PGND	0.5 nH	2 mΩ	SMPS1	0.3 nH	SMPS1	0.4 mΩ
			SMPS2	0.3 nH	SMPS2	0.4 mΩ
			SMPS3	0.4 nH	SMPS3	0.5 mΩ
			SMPS4	0.3 nH	SMPS4	0.6 mΩ
SMPS <sub>x</sub> _SW to inductor	N/A	N/A for SOA Maintain a low resistance value for efficiency	N/A		SMPS1	1 mΩ
			N/A		SMPS2	0.7 mΩ
			N/A		SMPS3	1 mΩ
			N/A		SMPS4	0.7 mΩ
Inductor to C <sub>OUT</sub>	N/A	N/A for SOA Maintain a low resistance value for efficiency	N/A		N/A for SOA Maintain a low resistance value for efficiency	
C <sub>OUT</sub> to GND	Use dedicated GND plane to keep inductance low	1 mΩ	SMPS1	0.8 nH	SMPS1	0.7 mΩ
			SMPS2	0.6 nH	SMPS2	0.8 mΩ
			SMPS3	0.5 nH	SMPS3	0.6 mΩ
			SMPS4	0.4 nH	SMPS4	0.6 mΩ
GND (C <sub>IN</sub> ) to GND (C <sub>OUT</sub> )	Use dedicated GND plane to keep inductance low	1 mΩ	Use dedicated GND plane to keep inductance low		mΩ	

Texas Instruments recommends measuring the voltages across the high-side FET (voltage at SMPS<sub>x</sub>\_IN versus SMPS<sub>x</sub>\_SW) and the low-side FET (SMPS<sub>x</sub>\_SW versus PGND) with a high bandwidth, high sampling-rate scope with a low-capacitance probe (ideally a differential probe). Measure the voltages as close as possible to the device pins and verify the amplitude of the spikes. A small-loop ground connection to PGND is essential.

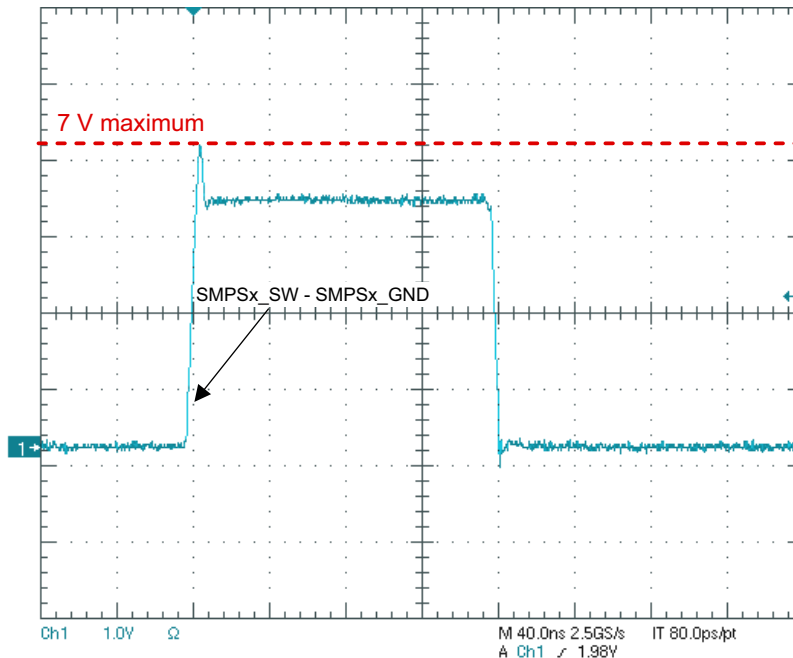
When measuring the voltage difference between the SMPS<sub>x</sub>\_IN and SMPS<sub>x</sub>\_SW pins, there should be a maximum of 7 V when measuring at the pins. Similarly, when measuring the voltage difference between the SMPS<sub>x</sub>\_SW and PGND pins, there should be a maximum of 7 V when measuring at the pins.

For more information on cursor-positioning, see [6-10](#) and [6-11](#).



Measure across the high-side FET (SMPSx\_IN – SMPSx\_SW) as close to the IC as possible. The preferred measurement is with a differential probe. The negative side of the probe should be at SMPSx\_SW and the positive side of the probe should measure SMPSx\_IN. As shown in this image, the voltage across the high-side FET should not exceed 7 V. Repeat the measurement for all SMPSs in use.

图 6-10. Measuring the High-Side FET (Differentially)

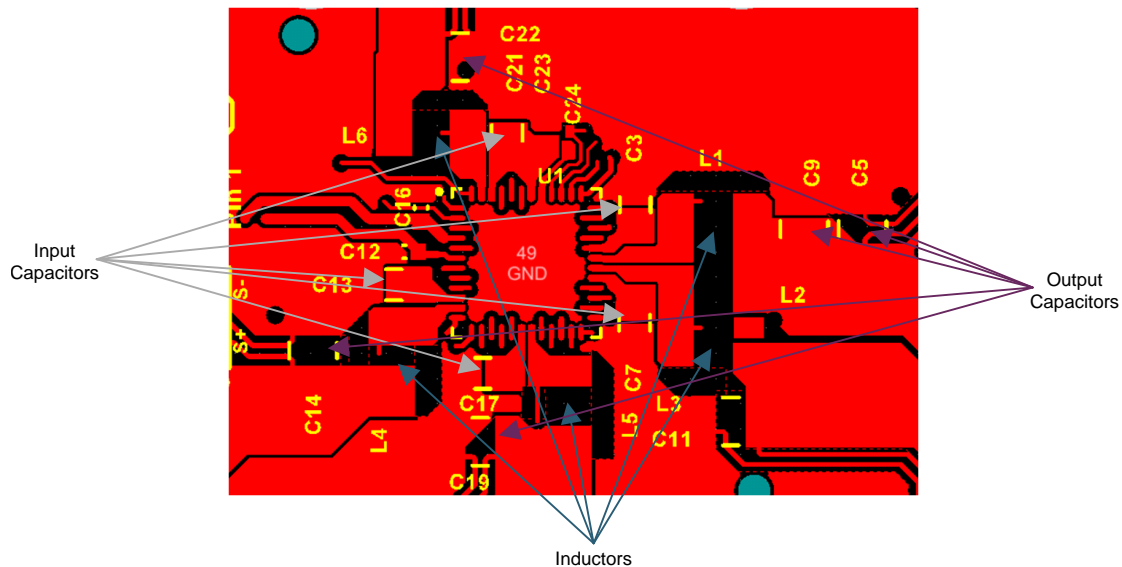


Measure across the low-side FET (SMPSx\_SW – GND) as close to the IC as possible. The preferred measurement is with a differential probe. The negative side of the probe should be at GND and the positive side of the probe should measure SMPSx\_SW. As shown in this image, the voltage across the low-side FET should not exceed 7 V. Repeat the measurement for all SMPSs in use.

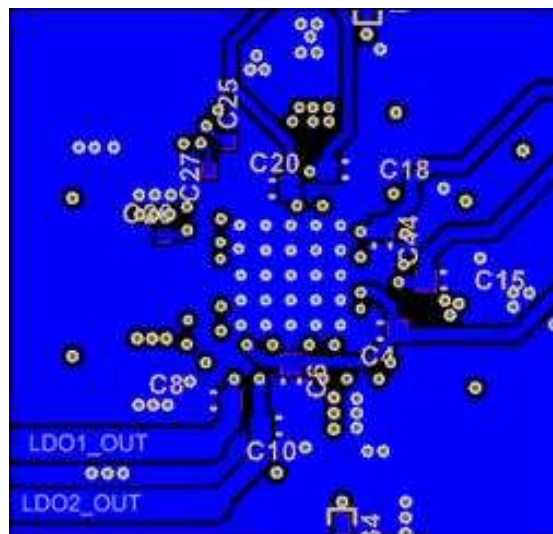
图 6-11. Measuring the Low-Side FET (Differentially)

### 6.3.2 Layout Example

See [Figure 6-12](#) and [Figure 6-13](#) for the actual placement and routing on the EVM.



**Figure 6-12. Top Layer Overview of Inductor and Capacitor Placement and Routing of SMPSs**



**Figure 6-13. Bottom Layer Overview of Capacitor Placement and Routing of LDOs**

## 6.4 Power Supply Coupling and Bulk Capacitors

The TPS65919-Q1 device is designed to work with an analog supply-voltage range of 3.135 V to 5.25 V. The input supply should be well regulated and connected to the VCCA pin, as well as SMPS and LDO input pins with appropriate bypass capacitors as recommended in . If the input supply is located more than a few inches from the TPS65919-Q1 device, additional capacitance may be required in addition to the recommended input capacitors at the VCCA pin and the SMPS and LDO input pins.



## 7 デバイスおよびドキュメントのサポート

### 7.1 デバイス・サポート

#### 7.1.1 *Third-Party Products Disclaimer*

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#### 7.1.2 デバイスの項目表記

このデータシートでは、以下の頭字語および用語が使用されています。用語、頭字語、定義の詳細な一覧については、[TI用語集](#)を参照してください。

<b>ADC</b>	アナログ/デジタル・コンバータ
<b>APE</b>	アプリケーション・プロセッサ・エンジン
<b>DVS</b>	デジタル電圧スケーリング
<b>GPIO</b>	汎用入出力
<b>LDO</b>	低ドロップアウト電圧リニア・レギュレータ
<b>PM</b>	パワー・マネージメント
<b>PMIC</b>	パワー・マネージメントIC
<b>PSRR</b>	電源電圧除去比
<b>RTC</b>	リアルタイム・クロック
<b>SMPS</b>	スイッチ・モード電源
<b>NA</b>	該当なし
<b>OTP</b>	ワンタイム・プログラマブル
<b>ESR</b>	等価直列抵抗
<b>PMU</b>	パワー・マネージメント・ユニット
<b>PFM</b>	パルス周波数
<b>PWM</b>	パルス幅変調
<b>SPI</b>	シリアル・ペリフェラル・インターフェイス
<b>EPC</b>	組み込み電源コントローラ
<b>FSD</b>	最初の電源検出

### 7.2 ドキュメントのサポート

#### 7.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、[『TPS65903xおよびTPS6591xデバイスのGPADC使用法ガイド』](#)
- テキサス・インスツルメンツ、[『TPS65919-Q1 電源管理ユニット\(PMU\)安全性マニュアル』](#)
- テキサス・インスツルメンツ、[『TPS65919-Q1レジスタ・マップ』](#)
- テキサス・インスツルメンツ、[『TPS65919-Q1およびTPS65917-Q1 DRA71x、DRA79x、TDA2E-17用電源ユーザー・ガイド』](#)
- テキサス・インスツルメンツ、[『TPS65919-Q1およびTPS65917-Q1 TDA3x用電源ユーザー・ガイド』](#)

### 7.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

### 7.7 Glossary

**TI Glossary** This glossary lists and explains terms, acronyms, and definitions.

## 8 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
O919A14CTRGZRQ1	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS65919 OTP 4C 1.1	<a href="#">Samples</a>
O919A14CTRGZTQ1	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS65919 OTP 4C 1.1	<a href="#">Samples</a>
O919A14ETRGZRQ1	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS65919 OTP 4E 1.1	<a href="#">Samples</a>
O919A14ETRGZTQ1	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS65919 OTP 4E 1.1	<a href="#">Samples</a>
O919A152TRGZRQ1	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS65919 OTP 52 1.1	<a href="#">Samples</a>
O919A152TRGZTQ1	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	TPS65919 OTP 52 1.1	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
O919A14CTRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
O919A14CTRGZTQ1	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
O919A14ETRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
O919A14ETRGZTQ1	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
O919A152TRGZRQ1	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
O919A152TRGZTQ1	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
O919A14CTRGZRQ1	VQFN	RGZ	48	2500	367.0	367.0	38.0
O919A14CTRGZTQ1	VQFN	RGZ	48	250	210.0	185.0	35.0
O919A14ETRGZRQ1	VQFN	RGZ	48	2500	367.0	367.0	38.0
O919A14ETRGZTQ1	VQFN	RGZ	48	250	210.0	185.0	35.0
O919A152TRGZRQ1	VQFN	RGZ	48	2500	367.0	367.0	38.0
O919A152TRGZTQ1	VQFN	RGZ	48	250	210.0	185.0	35.0

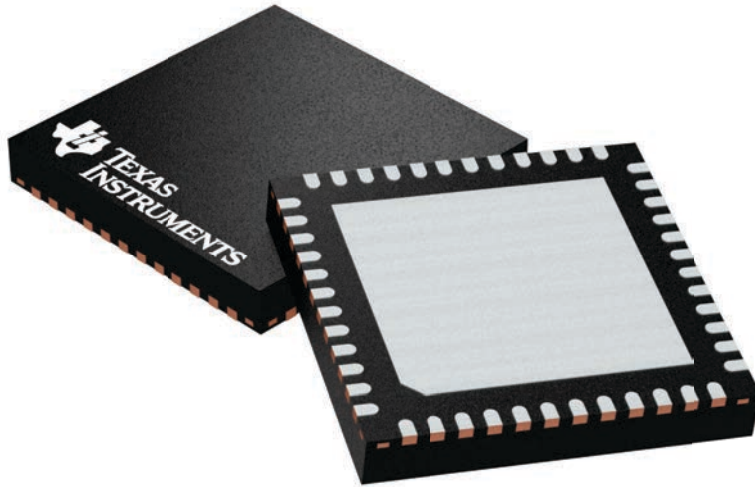
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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