

TPS6291x-Q1 3V~17V、4.5A/6A/8A、車載用、低ノイズ、低リップルの降圧コンバータ、フェライトビーズフィルタ補償機能内蔵

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
 - 温度グレード 1: -40°C ~ +125°C, T_A
- 機能安全対応
 - 機能安全システムの設計に役立つ資料を利用可能
- 小さい出力 1/f ノイズ: 20μV_{RMS} 未満 (100Hz ~ 100kHz)
- 小さい出力電圧リップル: 10μV_{RMS} 未満 (フェライトビーズの後)
- 優れた PSRR: 65dB 超 (最大 100kHz)
- 2.2MHz、1.4MHz、または 1.0MHz の固定周波数ピーク電流モード制御
- 外部クロックと同期可能 (オプション)
- 2 段階 L-C フィルタとしてフェライトビーズ (オプション) を使用できる内蔵ループ補償機能 (30dB 減衰)
- スペクトラム拡散変調 (オプション)
- 入力電圧範囲: 3.0V ~ 17V
- 出力電圧範囲: 0.8V ~ 5.5V
- 25mΩ/7mΩ の R_{DSon}
- ±1% の出力電圧精度 (全温度範囲)
- 高精度のイネーブル入力により以下を実現
 - ユーザー定義の低電圧誤動作防止機能
 - 正確なシーケンシング
- 可変ソフトスタート
- パワーグッド出力
- 出力放電 (オプション)
- 40°C ~ 150°C の接合部温度範囲
- 2.0mm × 3.0mm QFN、0.5mm ピッチ
- WEBENCH® Power Designer により、TPS6291x-Q1 を使用するカスタム設計を作成

2 アプリケーション

- 先進運転支援システム (ADAS)
- ゾーンアーキテクチャ

3 概要

車載認定済み TPS6291x-Q1 デバイスは、高効率、低ノイズ、低リップルの電流モード同期整流降圧コンバータのファミリです。これらのデバイスは、通常はポストレギュレーションに LDO を使用するような、ノイズの影響を受けやすいアプリケーション (たとえば、高速 ADC、クロックおよびジッタ クリーナ、シリアライザ、デシリアライザ、レーダー) 向けに設計されています。

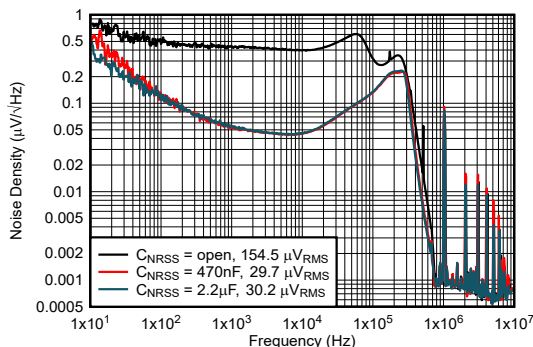
出力電圧リップルを低減するため、本デバイスのループ補償は、オプションの 2 段階フェライトビーズ L-C フィルタを使用して動作するように設計されています。NR/SS ピンに接続されたコンデンサで内部基準電圧をフィルタ処理することで、低ノイズ LDO と同様の低い周波数ノイズレベルをさらに達成しています。これらの機能を組み合わせることで、出力電圧リップルを 10μV_{RMS} 未満に抑えることができます。

本デバイスは 2.2MHz、1.4MHz または 1MHz の固定スイッチング周波数で動作し、外部クロックにも同期できます。オプションのスペクトラム拡散変調方式を使用すると、DC/DC スwitching 周波数をより広い範囲にわたって拡散できるため、ミキシング スプリアスを低減できます。

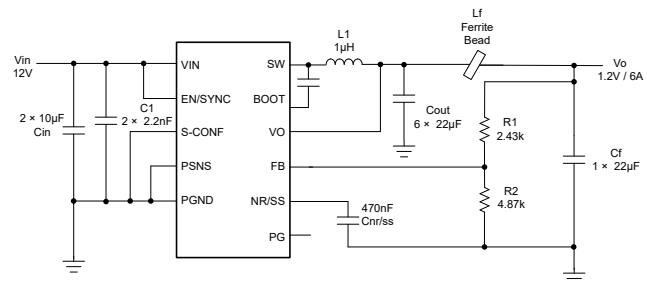
製品情報

型番	出力電流	パッケージ ⁽¹⁾	パッケージサイズ ⁽²⁾
TPS62916-Q1	6A	RPY (VQFN-HR, 14)	2.5mm × 3.0mm
TPS62914-Q1	4.5A		
TPS62918-Q1	8A		

- 詳細については、[セクション 10](#) を参照してください。
- パッケージサイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



出力ノイズと周波数との関係



代表的なアプリケーション



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4 Pin Configuration and Functions

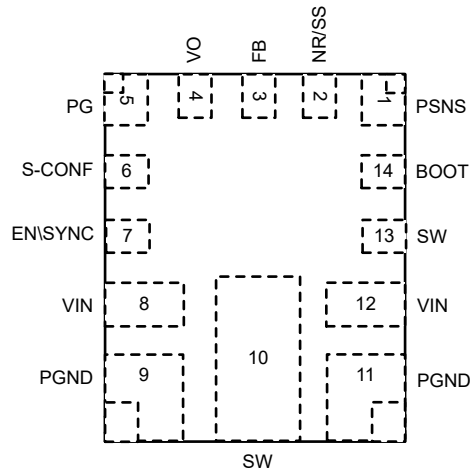


図 4-1. 14-Pin VQFN-HR, RPY Package (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
NR/SS	2	O	A capacitor connected to this pin sets the soft-start time and low frequency noise level of the device.
VO	4	I	Output voltage sense pin. This pin must be connected directly after the first inductor.
VIN	8, 12	I	Power supply input voltage pin
PGND	9, 11	—	Power ground connection
SW	10	O	Switch pin of the power stage. Connect this pin to the start winding of the output inductor .
SW	13	O	Switch pin. Connect a capacitor from this pin to the BOOT pin.
EN/SYNC	7	I	Enable, Disable pin including threshold-comparator. Connect to logic low to disable the device. Pull high to enable the device. This pin has an internal pulldown resistor of typically 500kΩ when the device is disabled. Apply a clock to this pin to synchronize the device
BOOT	14	I	Supply for the internal high-side MOSFET gate driver. Connect a capacitor from this pin to SW.
PSNS	1	—	Power sense ground, connect directly to GND plane
FB	3	O	Feedback pin of the device
PG	5	O	Open-drain power-good output. This pin is pulled to GND when V_{OUT} is below the power-good threshold. this pin requires a pullup resistor to output a logic high. This pin can be left open or tied to GND if not used.
S-CONF	6	O	Smart Configuration pin. This pin configures the operation modes of the device. See 表 6-1.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage ⁽²⁾	VIN, EN/SYNC, PG, S-CONF	-0.3	18	V
	SW (DC)	-0.3	V _{IN} + 0.3	V
	SW (AC, less than 10ns) ⁽³⁾	-2.5	21	V
	BOOT	-0.3	V _{IN} + 6	
	BOOT to SW	-0.3	6	
	VO, FB, NR/SS	-0.3	6	V
	VSNS-	-0.3	0.3	V
Sink current	PG		10	mA
T _J	Junction temperature	-40	150	°C
T _{stg}	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to the network ground terminal.
- (3) While switching.

5.2 ESD Ratings

			VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V	
	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	All pins	±500	V
			Corner pins (1, 5, 9, 11)	±750	V

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{IN}	Input voltage	3.0		17	V
V _{OUT}	Output voltage	0.8		5.5	V
C _{IN}	Effective input capacitance	5	10		μF
C _{OUT}	Effective output capacitance	80	120	200	μF
L _f	Effective filter inductance	0	10	50	nH
C _f	Effective filter capacitance	20	40	160	μF
C _{OUT} + C _f	Effective total output capacitance, including first and second L-C filter	80		400	μF
I _{OUT}	Output current for TPS62914-Q1	0		4.5	A
I _{OUT}	Output current for TPS62916-Q1	0		6	A
I _{OUT}	Output current for TPS62918-Q1	0		8	A
f _{SYNC}	Synchronization Range (2.2MHz setting)	1.9	2.2	2.4	MHz
f _{SYNC}	Synchronization Range (1.4MHz setting)	1.2	1.4	1.6	MHz
f _{SYNC}	Synchronization Range (1.0MHz setting)	0.8	1.0	1.2	MHz
T _J ⁽¹⁾	Junction temperature	-40		150	°C

- (1) Operating lifetime is derated at junction temperatures above 125°C.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS62916x-Q1		UNIT
		RPY 14-pin QFN		
		JEDEC 51-7 PCB	TPS6291x EVM	
R _{θJA}	Junction-to-ambient thermal resistance	58.9	29.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	37.8	n/a ⁽²⁾	°C/W
R _{θJB}	Junction-to-board thermal resistance	7.3	n/a ⁽²⁾	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	0.9	1.8	°C/W
Y _{JB}	Junction-to-board characterization parameter	7.2	13.4	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

(2) Not applicable to an EVM.

5.5 Electrical Characteristics

Over recommended input voltage range, T_J = –40°C to 150°C. Typical values are at V_{in} = 12V and T_J = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I _Q	Quiescent current	EN = High, no load, device switching, f _{sw} = 1MHz		5		mA
I _{SD}	Shutdown current	EN = GND, T _J = –40°C to 125°C		0.7	70	μA
V _{UVLO}	Undervoltage lockout	V _{IN} rising, T _J = –40°C to 125°C	2.85	2.92	3.0	V
V _{HYS}	Undervoltage lockout hysteresis			200		mV
T _{JSD}	Thermal shutdown threshold	T _J rising		170		°C
	Thermal shutdown hysteresis	T _J falling		20		°C
CONTROL and INTERFACE						
V _{H_EN}	High-level input-threshold voltage at EN/ SYNC		0.97	1.01	1.04	V
V _{L_EN}	Low-level input-threshold voltage at EN/ SYNC		0.87	0.9	0.93	V
I _{EN,LKG}	Input leakage current into EN/SYNC	EN/SYNC = GND or V _{IN} , –40°C ≤ T _J ≤ 125 °C		5	160	nA
R _{PD}	Pulldown resistor on EN/SYNC	EN/SYNC = Low	330	500		kΩ
t _{delay}	Enable delay time	Time from EN/SYNC high to device starts switching, R _{S-CONF} = 80.6kΩ		1		ms
I _{NR/SS}	NR/SS source current		67.5	75	82.5	μA
R _{S-CONF}	S-CONF resistor step range accuracy	R _{S-CONF} tolerance for all settings according to S-CONF Table	–4		+4	%
V _{PG}	Power-good threshold	V _{FB} rising, referenced to V _{FB} nominal	93	95	98	%
V _{PG}	Power-good threshold	V _{FB} falling, referenced to V _{FB} nominal	88	90	93	%
V _{PG,OL}	Low-level output voltage at PG pin	I _{SINK} = 1mA			0.4	V
I _{PG,LKG}	Input leakage current into PG pin	V _{PG} = 5V; –40°C ≤ T _J ≤ 125°C		5	500	nA
t _{PG,DLY}	Power-good delay time	V _{FB} falling		9		μs
OUTPUT						
t _{on}	Minimum on-time	V _{IN} ≥ 5V, I _{out} = 1A		35		ns
t _{off}	Minimum off-time	V _{IN} ≥ 5V, I _{out} = 1A		50		ns
V _{FB}	Feedback regulation accuracy	–40°C ≤ T _J ≤ 150°C	0.792	0.8	0.808	V
I _{FB,LKG}	Input leakage current into FB	V _{FB} = 0.8V, –40°C ≤ T _J ≤ 125°C		1	70	nA
I _{VO,LKG}	Input leakage current into VO	V _{VO} = 1.2V, –40°C ≤ T _J ≤ 125°C		0.01	30	μA

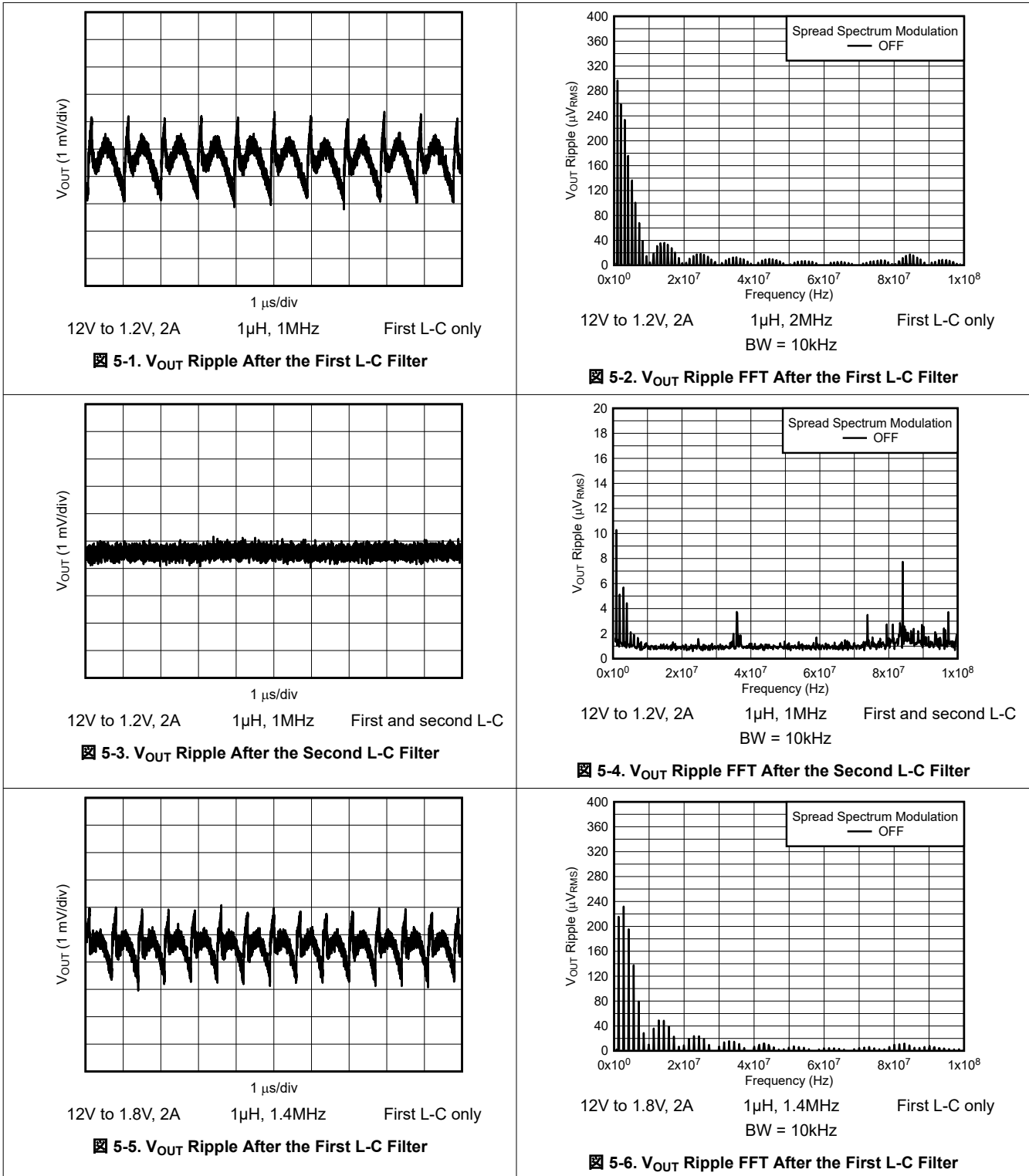
5.5 Electrical Characteristics (続き)

Over recommended input voltage range, $T_J = -40^\circ\text{C}$ to 150°C . Typical values are at $V_{IN} = 12\text{V}$ and $T_J = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PSRR	Power supply rejection ratio	$V_{IN} = 12\text{V}$, $1.2V_{OUT}$, 1A , $C_{NR/SS} = 470\text{nF}$, $f_{SW} = 1\text{MHz}$, $C_{FF} = \text{open}$, $L_1 = 1\mu\text{H}$, $C_{OUT} = 4 \times 22\mu\text{F}$, $f \leq 100\text{kHz}$		65		dB
PSRR	Power supply rejection ratio	$V_{IN} = 5\text{V}$, $1.2V_{OUT}$, 1A , $C_{NR/SS} = 470\text{nF}$, $f_{SW} = 2.2\text{MHz}$, $C_{FF} = \text{open}$, $L_1 = 1\mu\text{H}$, $C_{OUT} = 4 \times 22\mu\text{F}$, $f \leq 100\text{kHz}$		70		dB
V_{NRMS}	Output voltage RMS noise	$V_{IN} = 12\text{V}$, $BW = 100\text{Hz}$ to 100kHz , $C_{NR/SS} = 470\text{nF}$, $f_{SW} = 1\text{MHz}$, $V_{OUT} = 1.2\text{V}$, $C_{FF} = \text{open}$, $L_1 = 1\mu\text{H}$, $C_{OUT} = 4 \times 22\mu\text{F}$		24.4		μV_{RMS}
V_{NRMS}	Output voltage RMS noise	$V_{IN} = 5\text{V}$, $BW = 100\text{Hz}$ to 100kHz , $C_{NR/SS} = 470\text{nF}$, $f_{SW} = 2.2\text{MHz}$, $V_{OUT} = 1.2\text{V}$, $C_{FF} = \text{open}$, $L_1 = 1\mu\text{H}$, $C_{OUT} = 4 \times 22\mu\text{F}$		16.5		μV_{RMS}
V_{opp}	Output ripple voltage at f_{SW}	$V_{IN} = 12\text{V}$, $f_{SW} = 1\text{MHz}$, $V_{OUT} = 1.2\text{V}$, $L_1 = 1\mu\text{H}$, $C_{OUT} = 4 \times 22\mu\text{F}$, $L_f = 10\text{nH}$, $C_f = 22\mu\text{F}$		36		μV_{RMS}
V_{opp}	Output ripple voltage at f_{SW}	$V_{IN} = 5\text{V}$, $f_{SW} = 2.2\text{MHz}$, $V_{OUT} = 1.2\text{V}$, $L_1 = 2.2\mu\text{H}$, $C_{OUT} = 3 \times 22\mu\text{F}$, $L_f = 10\text{nH}$, $C_f = 22\mu\text{F}$		13		μV_{RMS}
R_{DIS}	Output discharge resistance	$EN/SYNC = \text{GND}$, $V_{OUT} = 1.2\text{V}$, $V_{IN} \geq 5\text{V}$.		4		Ω
R_{DIS}	Output discharge resistance	$EN/SYNC = \text{GND}$, $V_{OUT} = 5\text{V}$, $V_{IN} \geq 5\text{V}$.		16		Ω
f_{SW}	Switching frequency	2.2MHz setting	1.98	2.2	2.42	MHz
f_{SW}	Switching frequency	1.4MHz setting	1.26	1.4	1.54	MHz
f_{SW}	Switching frequency	1MHz setting	0.9	1	1.18	MHz
D_{SYNC}	Synchronization duty cycle		45		55	%
t_{sync_elay}	Synchronization phase delay	Phase delay from EN/SYNC rising edge to SW rising edge		90		ns
I_{SWpeak}	Peak switch current limit	TPS62914-Q1	6.3	7.3	8.9	A
$I_{SWvalley}$	Valley switch current limit	TPS62914-Q1		7.1		A
I_{SWpeak}	Peak switch current limit	TPS62916-Q1	8.34	9	10.2	A
$I_{SWvalley}$	Valley switch current limit	TPS62916-Q1		8.8		A
I_{SWpeak}	Peak switch current limit	TPS62918-Q1	9.3	11	12.8	A
$I_{SWvalley}$	Valley switch current limit	TPS62918-Q1		10.8		A
$I_{negvalley}$	Negative valley current limit			-2.9	-1.6	A
$R_{DS(ON)}$	High-side FET on-resistance	$V_{IN} \geq 5\text{V}$		25		m Ω
	Low-side FET on-resistance	$V_{IN} \geq 5\text{V}$		7		m Ω

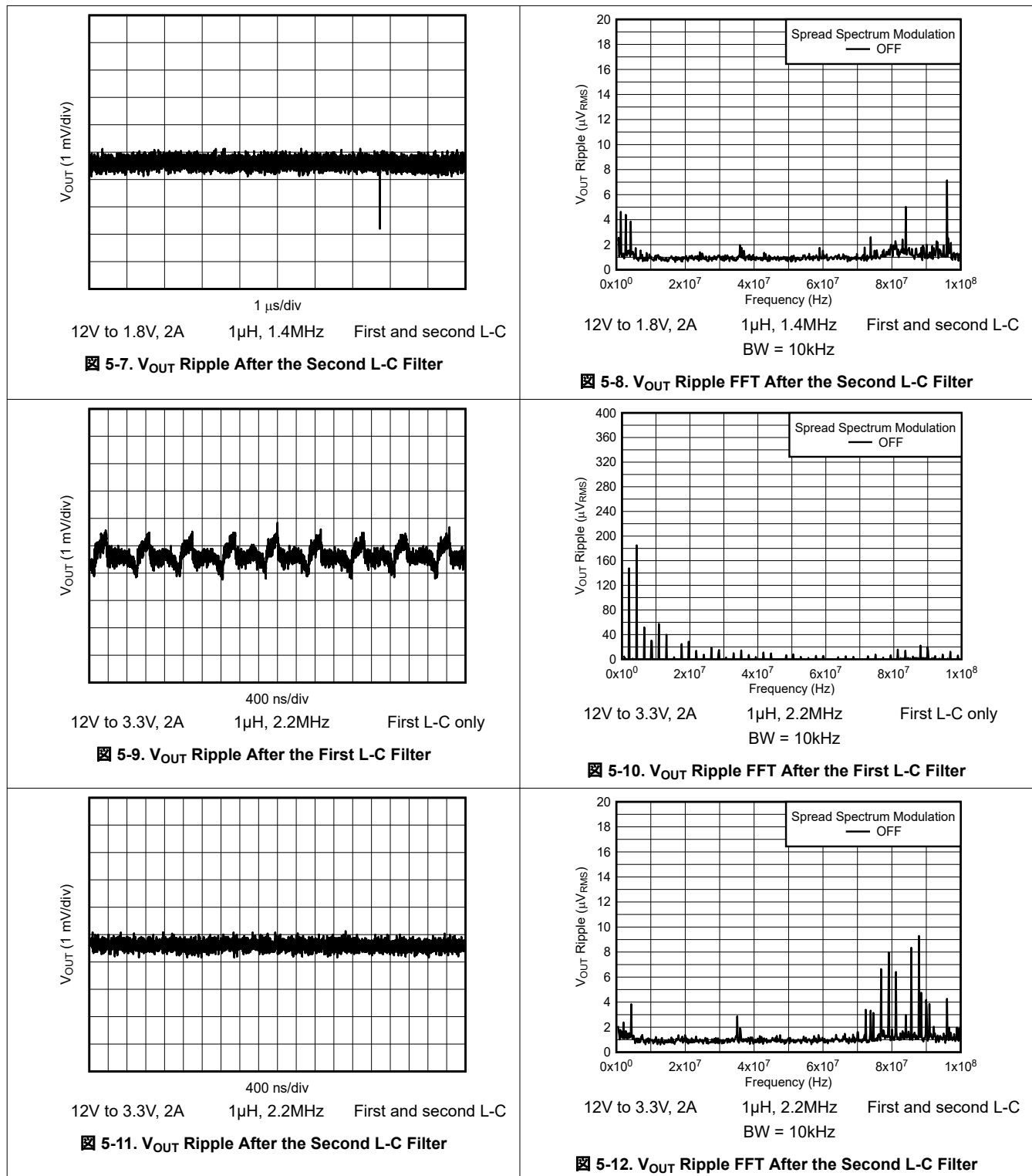
5.6 Typical Characteristics

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $T_A = 25^\circ C$, BOM = 表 7-1, (unless otherwise noted)



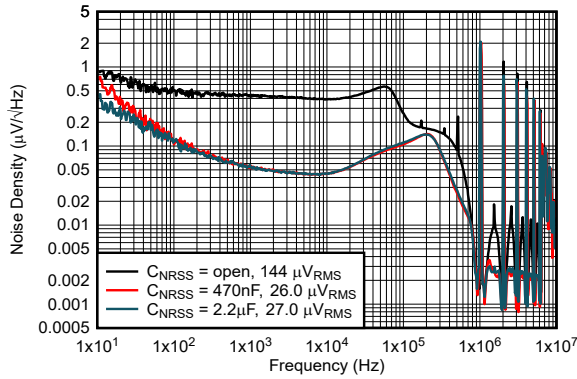
5.6 Typical Characteristics (continued)

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $T_A = 25^\circ C$, BOM = 表 7-1, (unless otherwise noted)



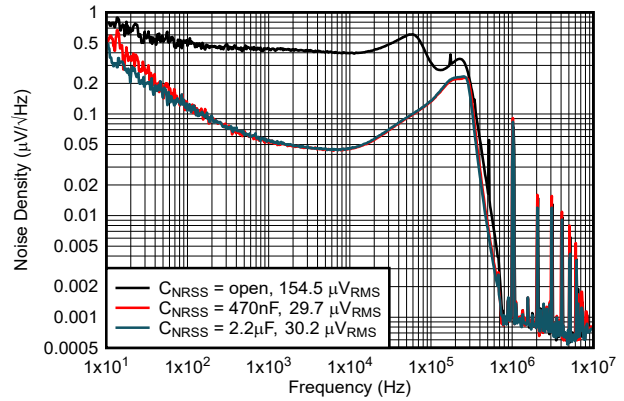
5.6 Typical Characteristics (continued)

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $T_A = 25^\circ C$, BOM = 表 7-1, (unless otherwise noted)



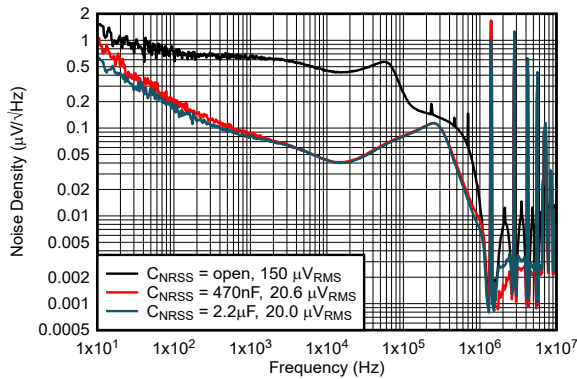
12V to 1.2V 1µH, 1MHz First L-C only
NR/SS = Open, 470nF, 2.2µF, BW = 100Hz to 100kHz

5-13. Output Noise Density vs Frequency



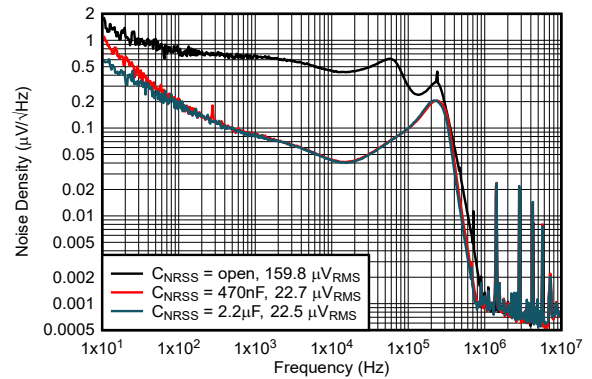
12V to 1.2V 1µH, 1MHz After ferrite bead filter
NR/SS = Open, 470nF, 2.2µF, BW = 100Hz to 100kHz

5-14. Output Noise Density vs Frequency



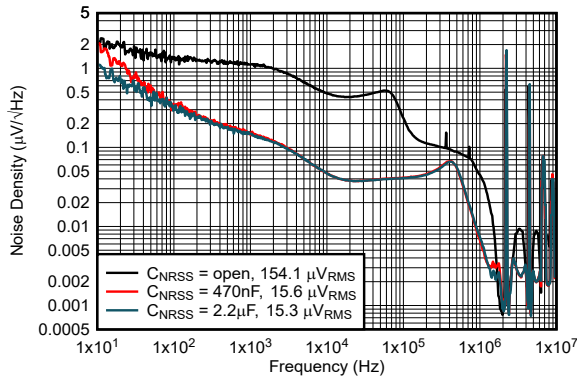
12V to 1.8V 1µH, 1.4MHz First L-C only
NR/SS = Open, 470nF, 2.2µF, BW = 100Hz to 100kHz

5-15. Output Noise Density vs Frequency



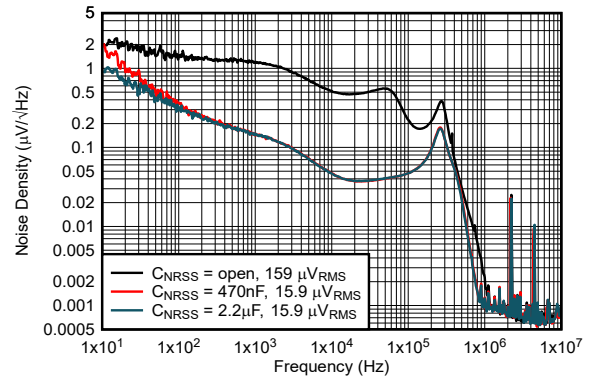
12V to 1.8V 1µH, 1.4MHz After ferrite bead filter
NR/SS = Open, 470nF, 2.2µF, BW = 100Hz to 100kHz

5-16. Output Noise Density vs Frequency



12V to 3.3V 1µH, 2.2MHz First L-C only
NR/SS = Open, 470nF, 2.2µF, BW = 100Hz to 100kHz

5-17. Output Noise Density vs Frequency



12V to 3.3V 1µH, 2.2MHz After ferrite bead filter
NR/SS = Open, 470nF, 2.2µF, BW = 100Hz to 100kHz

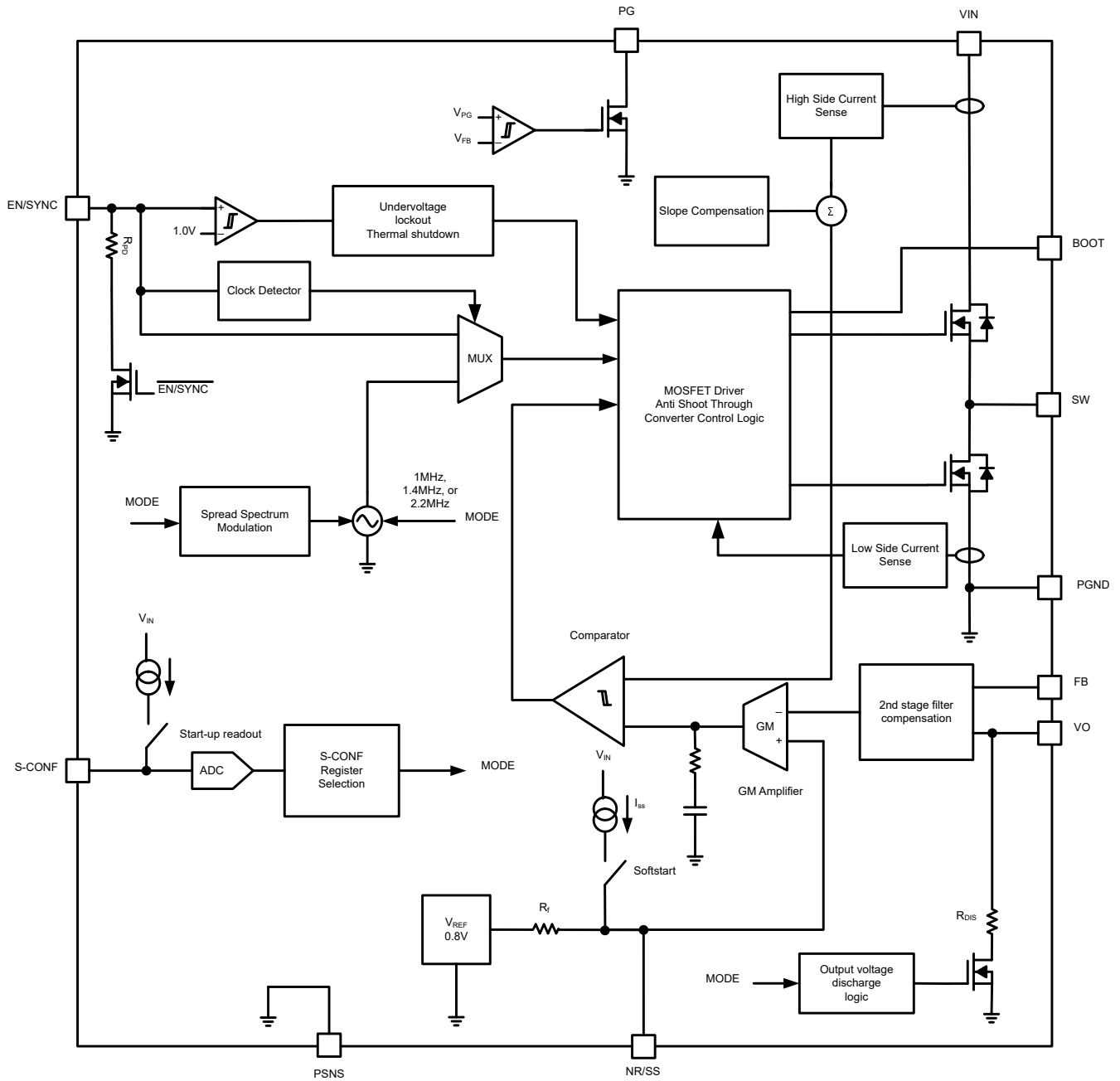
5-18. Output Noise Density vs Frequency

6 Detailed Description

6.1 Overview

The TPS6291x-Q1 low-noise, low-ripple, synchronous buck converter is a fixed frequency current mode converter. The converter has a filtered internal reference to achieve a low-noise output similar to low noise LDOs. The converter achieves lower output voltage ripple by using a switching frequency of either 2.2MHz, 1.4MHz, or 1MHz and a larger inductance. The output voltage ripple can be further reduced by adding a small second stage L-C filter to the output. This can be a ferrite bead or a small inductor, followed by an output capacitor. Internal compensation maintains stability with an external filter inductor up to 50nH. To avoid voltage drops across this second stage filter, the device regulates the output voltage after the filter. The TPS6291x-Q1 family supports an optional spread spectrum modulation. When powering ADCs, for example, spread spectrum modulation reduces the mixing spurs. Switching frequency, spread spectrum modulation, and output discharge are set using the S-CONF pin.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Smart Config (S-CONF)

This S-CONF pin configures the device based on the resistor value. This pin is read after EN/SYNC goes high. The device configuration cannot be changed during operation. The S-CONF value is re-read if EN is pulled below 200mV or if VIN falls below UVLO. 表 6-1 shows the configuration options of switching frequency, spread spectrum modulation, output discharge, and synchronization.

To make sure the internal circuit detects the resistor value correctly, minimize the distance between the resistor and the S-CONF pin and do not place any capacitors on the S-CONF pin.

表 6-1. S-CONF Device Configuration Modes

S-CONF	SWITCHING FREQUENCY	SPREAD SPECTRUM	OUTPUT DISCHARGE	SYNC
VIN	2.2MHz	OFF	OFF	No
GND	1MHz	OFF	OFF	No
4.87kΩ	1.4MHz	OFF	OFF	No
6.04kΩ	1.4MHz	OFF	OFF	1.2MHz to 1.6MHz
7.5kΩ	2.2MHz	OFF	OFF	1.9MHz to 2.42MHz
9.31 kΩ	1MHz	OFF	OFF	0.9MHz to 1.2MHz
11.5kΩ	1MHz	Random	OFF	No
14.3kΩ	1.4MHz	Random	OFF	No
18.2kΩ	2.2MHz	Random	OFF	No
22.1kΩ	1MHz	OFF	ON	No
27.4kΩ	1.4MHz	OFF	ON	No
34kΩ	2.2MHz	OFF	ON	No
42.2kΩ	1MHz	OFF	ON	0.9MHz to 1.2MHz
52.3kΩ	1.4MHz	OFF	ON	1.2MHz to 1.6MHz
64.9kΩ	2.2MHz	OFF	ON	1.9MHz to 2.42MHz
80.6kΩ	1MHz	Random	ON	No
100kΩ	1.4MHz	Random	ON	No
124kΩ	2.2MHz	Random	ON	No

6.3.2 Device Enable (EN/SYNC)

The device is enabled by pulling the EN/SYNC pin high, and has an accurate rising threshold voltage of typically 1.01V. After the device is enabled, the operation mode is set by the configuration of the S-CONF pin. This action occurs during the device start-up delay time t_{delay} . After t_{delay} expires, the internal soft-start circuitry ramps up the output voltage over the soft-start time set by the $C_{\text{NR/SS}}$ capacitor. The start-up delay time t_{delay} varies depending on the selected S-CONF value. The start-up delay time is shortest with smaller S-CONF resistors.

The EN/SYNC pin has an active pulldown resistor R_{PD} . This resistor prevents an uncontrolled start-up of the device, in case the EN/SYNC pin cannot be driven to a low level. The pulldown resistor is disconnected after start-up. With EN set to a low level, the device enters shutdown and the pulldown resistor is activated again.

6.3.3 Device Synchronization (EN/SYNC)

The EN/SYNC pin is also used for device synchronization. After a clock signal is applied to this pin, the device is enabled and reads the configuration of the S-CONF pin. The external clock frequency must be within the clock synchronization frequency range set by the S-CONF pin. When the clock signal changes from a clock to a static high, then the device switches from external clock to internal clock. To shutdown the device when using an external clock, EN/SYNC must go low for at least 10 μ s.

The clock signal can be a logic signal with a logic level as specified in the electrical table, and can be applied directly to the EN/SYNC pin. External logic, such as an AND gate, can be used to combine separate enable and clock inputs, as shown in [Figure 6-1](#).

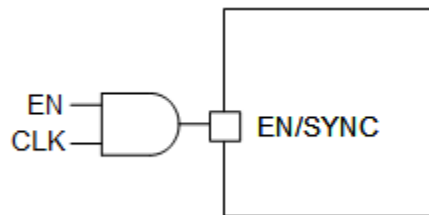


Figure 6-1. Synchronization With Separate Enable Signal (Optional)

6.3.4 Spread Spectrum Modulation

Using the S-CONF pin enables or disables spread spectrum modulation. The DC/DC converter generates an output voltage ripple at the switching frequency. When powering ADCs or an analog front-end (AFE), the switching frequency generates high frequency mixing spurs as well as a low frequency spur in the output frequency spectrum. Using the optional second stage L-C filter reduces the ripple of the converter and spurs by up to 30dB.

The device has an integrated random spread spectrum modulation (SSM) scheme, selected by the resistor connected to the S-CONF pin according to [Table 6-1](#). Selecting random modulation to spread the switching frequency over a larger frequency range is possible. The modulation spread is $\pm 10\%$ of the device switching frequency. This SSM provides high attenuation when the receiver bandwidth is \leq the modulation frequency, typically the case for systems using Fast Fourier Transforms (FFT) post processing as in high speed ADC applications. For applications sensitive to noise at the modulation frequency, random SSM is used. Using a random spread spectrum modulation also reduces the spurs in the output spectrum as shown in [Figure 5-2](#). The randomized modulation uses a Fibonacci Linear-Feedback Shift Register (LFSR) so that every tone is generated once during the pseudo-random generation period. The frequency spreading is shown in [Figure 6-2](#).

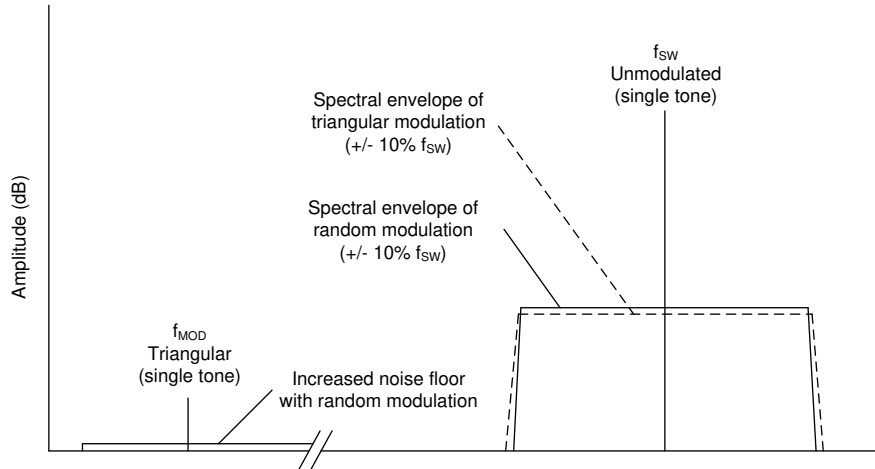


図 6-2. Spread Spectrum Modulation

6.3.5 Output Discharge

Output discharge is enabled or disabled, depending on the S-CONF setting. With output discharge enabled, the output voltage is pulled low by a discharge resistor R_{DIS} of typically 7Ω . The output discharge function is enabled during thermal shutdown, UVLO, or when EN/SYNC is pulled low.

6.3.6 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, the device is enabled after the input voltage is above the undervoltage lockout threshold. The device is disabled after the input voltage falls below the undervoltage threshold.

6.3.7 Power-Good Output

The device has a power-good output. The PG pin goes high impedance after the FB pin voltage is above 95% of the nominal voltage, and is driven low after the voltage falls below typically 90% of the nominal voltage. 表 6-2 shows the typical PG pin logic. The PG pin is an open-drain output and is specified to sink up to 10mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 18V. The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other s. If not used, the PG pin can be left floating or connected to GND. PG has a deglitch time of typically $8\mu s$ before going low.

表 6-2. Power-Good Pin Logic

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enabled (EN/SYNC = High)	$V_{FB} \geq V_{PG}$	√	
	$V_{FB} < V_{PG}$ after t_{PG}		√
Shutdown (EN/SYNC = Low)			√
UVLO	$0.7V < V_{IN} < V_{UVLO}$		√
Thermal shutdown	$T_J > T_{JSD}$		√
Power supply removal	$V_{IN} < 0.7V$	√	

6.3.8 Noise Reduction and Soft-Start Capacitor (NR/SS)

A capacitor connected to this pin reduces the low frequency noise of the converter and sets the soft-start time. The larger the capacitor, the lower the noise and the longer the start-up time of the converter. A 470nF capacitor is typically connected to this pin for a start-up time of 5ms, although longer and shorter start-up times can be used. During soft start with a light load, the device skips switching pulses as needed to not discharge the output voltage. The device can start into a prebiased output voltage.

The device achieves low noise by adding an R-C filter to the reference voltage, as shown in [セクション 6.2](#). During start-up, the NR/SS capacitor is charged with a constant current of 75µA (typical) to 0.8V. Larger NR/SS capacitors provide for lower low frequency noise. The maximum NR/SS cap is 3.3µF for a start-up time of 35ms. The minimum start-up time is set internally to 0.7ms, which occurs when there is a small NR/SS capacitor or no NR/SS capacitor.

6.3.9 Current Limit and Short-Circuit Protection

The device is protected against short circuits and overcurrent. The switch current limit prevents the device from high inductor current and from drawing excessive current from the input voltage rail. Excessive current can occur with a shorted, saturated inductor or a heavy load, shorted output circuit condition. If the inductor current reaches the threshold I_{SWpeak} , the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET is turned on again only when the low-side current is below the low-side sourcing current limit $I_{SWvalley}$.

Due to internal propagation delay, the actual current can exceed the static current limit, especially if the input voltage is high and very small inductances are used. The dynamic current limit is calculated as follows in [式 1](#):

$$I_{PEAK(typ)} = I_{SWpeak} + \left(\frac{V_L}{L}\right) \times t_{PD} \quad (1)$$

where

- I_{SWpeak} is the static current limit, specified in .
- L is the inductance.
- V_L is the voltage across the inductor ($V_{IN} - V_{OUT}$).
- t_{PD} is the internal propagation delay, typically 50ns.

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle.

6.3.10 Thermal Shutdown

The device goes into thermal shutdown after the junction temperature exceeds typically 170°C with a 20°C hysteresis.

6.4 Device Functional Modes

6.4.1 Fixed Frequency Pulse Width Modulation

To minimize output voltage ripple, the device operates in fixed frequency PWM operation down to no load. The switching frequency of 1MHz, 1.4MHz, or 2.2MHz is selected using the S-CONF pin.

6.4.2 Low Duty Cycle Operation

For high input voltages or low output voltages, the 70ns minimum on-time limits the maximum input to output voltage difference and the switching frequency selected. When the minimum on-time is reached, the output voltage rises above the regulation point. Refer to [表 7-2](#) for detailed design recommendations.

6.4.3 High Duty Cycle Operation (100% Duty Cycle)

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times (R_{DS(ON)} + R_L) \quad (2)$$

where

- $V_{OUT(min)}$ is the minimum output voltage the load can accept.

- I_{OUT} is the output current.
- $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the high-side MOSFET.
- R_L is the DC resistance of the inductor used.

To maintain fixed frequency switching, the device requires a minimum off-time of 50ns (typical), 60ns (maximum). If this limit is reached during a switching pulse, the device skips switching pulses to maintain output voltage regulation. If the input voltage decreases further, the device enters 100% mode.

6.4.4 Second Stage L-C Filter Compensation (Optional)

Most low-noise and low-ripple applications use a ferrite bead and bypass capacitor before the load. Using a second L-C filter is especially useful for low-noise and low-ripple applications with constant load current such as ADCs, DACs, and Jitter Cleaner. The second stage L-C filter is optional, and the device can be used without this filter. Without the filter, the device has a low output voltage noise of typically $16.9\mu V_{RMS}$ with an output voltage ripple of $280\mu V_{RMS}$ shown in [Figure 5-10](#). The second stage L-C filter attenuates the output voltage ripple by another approximately 30dB shown in [Figure 5-12](#). To improve load regulation, the device can remote sense the output voltage after the second stage L-C filter and is internally compensated for the additional double pole generated by the L-C filter.

To keep the second stage L-C filter as small as possible, the internal compensation is optimized for a 10nH to 50nH inductance. A small ferrite bead or even a PCB trace provides sufficient inductance for output voltage ripple filtering. For details, see [Section 7.2.2.2.4](#).

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The TPS6291x-Q1 family of devices are designed for low noise and low output voltage ripple.

7.2 Typical Applications

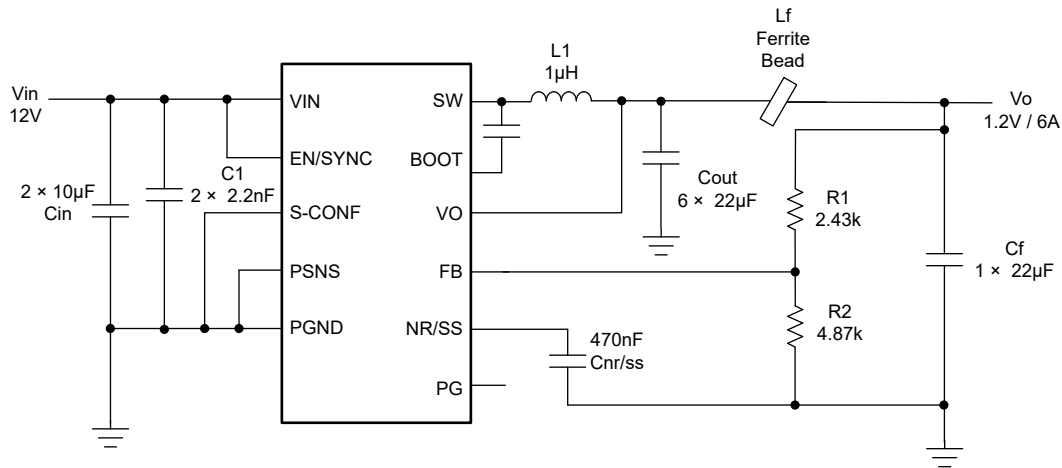


図 7-1. Typical Schematic

The following table shows the list of recommended components for most applications.

表 7-1. List of Components

REFERENCE	PART NUMBER	DESCRIPTION	MANUFACTURER
L ₁	XGL4030-102MEC or XGL5030-102MEC	Inductor: 1.0µH	Coilcraft
C _{IN}	C2012X7S1E106K125AC	Ceramic capacitors: 2 × 10µF ±10% 25V Ceramic Capacitor X7S 0805	TDK
C _{OUT}	C2012X7S1A226M125AC	Ceramic capacitors: 6 × 22µF, 10V, ±20%, X7S, 0805	TDK
L _f	BLE32SN120SN1L	Ferrite Bead	MuRata
C _f	C2012X7S1A226M125AC	Ceramic capacitor: 1 × 22µF, 10V, ±20%, X7S, 0805 × 22µF, 10V, ±20%, X7S, 0805	TDK
C _{NR/SS} , C _{FF}		Ceramic capacitor	Standard
R1, R2, R3, R4		Resistor	Standard

7.2.1 Design Requirements

The external components have to fulfill the needs of the application, but also meet the stability criteria of the control loop of the device. The device is designed to work within a range of external components, and can be optimized for efficiency, output ripple, component count, or lowest 1/f noise.

Typical applications that have input voltages of $\leq 6V$ use a $1\mu H$ inductor with a 2.2MHz switching frequency. Applications that have input voltages $> 6V$ can be optimized for efficiency using a $1\mu H$ inductor with a 1MHz or 1.4MHz switching frequency depending on the output voltage. Optimization for powering clock and PLL circuits that need a 3.3V output use a $1\mu H$ inductor with 2.2MHz switching frequency, minimizing output voltage ripple and low frequency noise.

For the application cases that are not found in the following table, there are two methods to design the TPS6291x-Q1 circuit. [セクション 7.2.2.1](#) uses WEBENCH to design the circuit automatically or the calculations in [セクション 7.2.2.2](#) can be used instead.

表 7-2. Typical Single L-C Filter Design Recommendations

DESIGN GOAL	V_{IN}	V_{OUT}	F_{sw}	INDUCTOR ⁽²⁾	OUTPUT CAPACITORS ⁽³⁾
Typical	12V ⁽¹⁾	$\leq 1.4V$ ⁽¹⁾	1MHz	$1\mu H$	6 × 22 μF , 10V, 0805
Typical	12V	$1.4V < V_{OUT} \leq 2.2V$	1.4MHz	$1\mu H$	6 × 22 μF , 10V, 0805
Typical	12V	$> 2.2V$	2.2MHz	$1\mu H$	8 × 22 μF , 10V, 0805
Typical	5V	$\leq 3.3V$	2.2MHz	$1\mu H$	6 × 22 μF , 10V, 0805
Typical	5V	$> 3.3V$	2.2MHz	$1\mu H$	8 × 22 μF , 10V, 0805

- (1) The maximum input to output voltage difference is limited by the device maximum minimum on-time of 70ns. This limit is especially important for input voltages above 12V or output voltages below 1V. See [セクション 7.2.2.2.1](#).
- (2) For inductor part numbers, see [表 7-4](#).
- (3) For output capacitor part numbers, see [表 7-5](#).

The second stage L-C filter is optional, as the device can be used without this filter to achieve below 20 μV_{RMS} noise typically. A second stage filter is added to provide additional attenuation of the output ripple voltage. The output voltage is sensed after the second L-C filter by connecting the FB resistors to the second stage L-C filter capacitor. This action provides remote sense, minimizing output voltage drop due to the ferrite bead. Refer to the following table for second stage L-C filter recommendations based on the output voltage.

表 7-3. Second Stage L-C (Ferrite Bead) Filter Design Recommendations

VOUT (V)	FERRITE BEAD IMPEDANCE (AT 100MHZ) ⁽²⁾	OUTPUT CAPACITORS ⁽¹⁾
$\leq 2.2V$	8 to 20 Ω	1 × 22 μF , 10V, 0805
$> 2.2V$	8 to 20 Ω	2 × 22 μF , 10V, 0805

- (1) For output capacitor part numbers, see [表 7-5](#).
- (2) For second stage L-C filter part numbers, see [表 7-6](#).

7.2.2 Detailed Design Procedure

If the specific design is not found in [表 7-2](#), TI recommends WEBENCH to generate the design. Alternatively, follow the manual design procedure in [セクション 7.2.2.2](#).

7.2.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS6291x-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Open the advanced tab to optimize for output voltage ripple.
4. After in a TPS6291x-Q1 design, you can enable the second stage L-C filter and change other settings from the drop-down on the left.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

7.2.2.2 External Component Selection

7.2.2.2.1 Switching Frequency Selection

The switching frequency can be chosen to optimize efficiency (lower) or ripple noise (higher). Using the higher 1.4MHz or 2.2MHz setting increases the gain of the feedback loop and can result in lower output noise. However, additional considerations for minimum on-time and duty cycle must also be considered. First, calculate the duty cycle using 式 3. Higher efficiency results in a shorter on-time, so a conservative approach is to use a higher efficiency than expected in the application.

$$D = \frac{V_{OUT}}{V_{IN} \times \eta} \quad (3)$$

where:

- η = estimated efficiency (use the value from the efficiency curves or 0.9 as an conservative assumption)

Then, calculate the on-time with 1MHz, 1.4MHz, and 2.2MHz using 式 4. The on-time must always remain above the minimum on-time of 70ns. Use the maximum input voltage and maximum efficiency to determine the minimum duty cycle, D_{min} . Use the maximum switching frequency for f_{SW} .

$$T_{ON} = \frac{D_{min}}{f_{SW_min}} \quad (4)$$

then

- If t_{ON_min} minimum < 70ns with 2.2MHz, use 1.4MHz.
- If t_{ON_min} minimum < 70ns with 1.4MHz, use 1MHz
- If t_{ON_min} minimum < 70ns with 1MHz, reduce the maximum input voltage.
- If t_{ON_min} minimum \geq 70ns, use a lower frequency for highest efficiency, or the highest frequency for the lowest noise and ripple.

7.2.2.2.2 Inductor Selection for the First L-C Filter

The inductor must be rated for the appropriate saturation current. 式 5 and 式 6 calculate the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The calculation must be done for the maximum input voltage where the peak switch current is highest.

$$\Delta I_L = \frac{\frac{V_{OUT}}{\eta} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \eta}\right)}{f_{SW} \times L} \quad (5)$$

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (6)$$

where:

- f_{SW} is the switching frequency (1MHz, 1.4MHz, or 2.2MHz).
- L = inductance.
- η = estimated efficiency (use the value from the efficiency curves or 0.9 as an conservative assumption).

注

The calculation must be done for the maximum input voltage of the application.

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. TI recommends a margin of 20% be added to cover for load transients during operation.

See 表 7-4 for typical inductors.

表 7-4. Inductor Selection

INDUCTOR VALUE	MANUFACTURER	PART NUMBER	SIZE (L × W × H IN mm)	ISAT/DCR (30% DROP)
1μH	Coilcraft	XGL4020-102	4 × 4 × 2.1	8.8A / 8.2mΩ
1μH	Coilcraft	XGL4030-102	4 × 4 × 3.1	10.3A / 6.5mΩ
1μH	Würth Elektronik	74438356010	4.1 × 4.1 × 2.1	9A / 12mΩ
1μH	Würth Elektronik	74438357010	4.1 × 4.1 × 3.1	9.6A / 11.6mΩ
1μH	Coilcraft	XGL5020-102	5 × 5 × 2.1	11.4A / 7.5mΩ
1μH	Coilcraft	XGL5030-102	5 × 5 × 3.1	14A / 4.8mΩ

7.2.2.2.3 Output Capacitor Selection

The effective output capacitance can range from 80μF (minimum) up to 400μF (maximum) for a single L-C system design. When using a second L-C filter, the first L-C filter must have output capacitance between 80μF and 160μF, the second stage L-C filter (if used) must have at least 20μF of capacitance, and the total capacitance for both L-C filters must be less than 400μF. Load transient testing and measuring the bode plot are good ways to verify stability.

注

For designs requiring cold temperature (< -10°C) operation, TI recommends to use a minimum effective output capacitance of 120μF for a single L-C system design or within the first L-C filter when using a second L-C filter design.

TI recommends ceramic capacitors (X5R or X7R). Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating. The ESR and ESL of the output capacitor are also important considerations in selecting the output capacitors for low noise applications. Smaller package sizes typically have lower ESL and ESR. TI recommends 0805 or smaller packages, as long as the packages provide the required capacitance and voltage rating for stable operation. 表 7-5 lists recommended output capacitors.

表 7-5. Recommended Output Capacitors

CAPACITOR TYPE	CAPACITOR VALUE	MANUFACTURER	VOLTAGE (V)	PACKAGE
Bulk Capacitor	22μF, X7S	TDK C2012X7S1A226M125AC	10	0805
Bulk Capacitor	47μF, X7R	Murata GRM32ER71A476ME15L	10	1210

7.2.2.2.4 Ferrite Bead Selection for Second L-C Filter

Using a ferrite bead for the second stage L-C filter minimizes the external component count because most of the noise sensitive circuits use a RF bead for high frequency attenuation as a default component at the inputs.

Make sure to select a ferrite bead with sufficiently high inductance at full load, and with low DC resistance (below 10mΩ) to keep the converter efficiency as high as possible. The ferrite bead inductance decreases with increased load current. Therefore, the ferrite bead must have a current rating much higher than the desired load current.

The recommendation is to choose a ferrite bead with an impedance of 8Ω to 20Ω at 100MHz. Ferrite beads can be used in parallel if higher current is needed, however this can halve the inductance and filtering. Refer to 表 7-6 for possible ferrite beads.

表 7-6. Recommended Ferrite Beads

PART NUMBER	MANUFACTURER	SIZE	IMPEDANCE AT 100MHZ	INDUCTANCE AT 100MHZ (CALCULATED)	DC RESISTANCE	CURRENT RATING
BLE18PS080SN1	MuRata	0603	8.5Ω	13.5 nH	4mΩ	5A
BLE32SN120SN1L	MuRata	1210	12Ω	18 nH	0.78mΩ	20A
74279221100	Würth Elektronik	1206	10Ω	15.9 nH	3mΩ	10.5A
7427922808	Würth Electronik	0603	8Ω	12.7 nH	5mΩ	9.5A

The internal compensation has been designed to be stable with up to 50nH of inductance in the second stage filter. To achieve low ripple, the second L-C filter requires only 5nH to 10nH inductance. The inductance can be estimated from the ferrite bead impedance specification at 100MHz, with the assumption that the inductance is similar at the selected converter switching frequency of 1MHz, 1.4MHz, or 2.2MHz, and can be verified through tools available on some manufacturer websites. Use 式 7 to calculate the inductance of a ferrite bead:

$$L = \frac{Z}{2\pi \times f} \quad (7)$$

where

- Z is the impedance of the ferrite bead in ohms at the specified frequency (usually 100MHz).
- f is the specified frequency (usually 100MHz).

7.2.2.2.5 Input Capacitor Selection

For the best output and input voltage filtering, TI recommends X5R or X7R ceramic capacitors. The input bulk capacitor minimizes input voltage ripple, suppresses input voltage spikes, and provides a stable system rail for the device. TI recommends a 10μF or larger input capacitor. Having two in parallel further improves the input voltage ripple filtering, minimizing noise coupling into adjacent circuits. The voltage rating of the cap must also be taken into consideration, and must provide the required 5μF minimum effective capacitance after DC bias derating.

In addition to the bulk input cap, a smaller cap must be placed directly from the VIN pin to the PGND pin to minimize input loop parasitic inductance, thereby minimizing the high frequency noise of the device. The input cap placement affects the output noise, so care needs to be taken in placing both the bulk cap and bypass caps as shown in [セクション 7.4.2](#). [表 7-7](#) lists recommended input capacitors.

表 7-7. Recommended Input Capacitors

INPUT CAP TYPE	CAPACITOR VALUE	MANUFACTURER	VOLTAGE RATING (V)	PACKAGE SIZE
Bulk Cap	10μF, X7S	TDK C2012X7S1E106K125AC	25	0805
Bypass Cap	2.2nF, X7R	Murata GRM155R71E222KA01D	25	0402

7.2.2.2.6 Setting the Output Voltage

Choose resistors R1 and R2 to set the output voltage within a range of 0.8V to 5.5V, according to 式 8. To keep the feedback network robust from noise, and to reduce the self-generated noise of resistors, set R2 equal to or lower than 5kΩ. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the [Design Considerations for a Resistive Feedback Divider in a DC/DC Converter analog design journal](#).

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R_2 \times \left(\frac{V_{OUT}}{0.8V} - 1 \right) \quad (8)$$

VOUT (V)	R1	R2
0.9	604Ω	4.87kΩ

VOUT (V)	R1	R2
1.0	1.21kΩ	4.87kΩ
1.2	2.43kΩ	4.87kΩ
1.8	6.04kΩ	4.87kΩ
2.5	10.4kΩ	4.87kΩ
3.3	15.2kΩ	4.87kΩ
5	25.5kΩ	4.87kΩ

A feedforward capacitor (C_{FF}) is not required for proper operation, but can further improve output noise. However, care must be taken in choosing the C_{FF} because the power-good (PG) function can not be valid with a large C_{FF} during start-up, and can cause spurious triggering of the PG pin during a large load transient. Refer to the [Pros and Cons Using a Feedforward Capacitor with a Low Dropout Regulator application report](#) for a discussion of the pros and cons of using a feedforward capacitor.

7.2.2.2.7 Bootstrap Capacitor Selection

A 0.1μF ceramic capacitor must be connected between the BOOT and SW pins for proper operation. The capacitor must be rated for at least 10V to minimize DC bias derating.

A resistor must be added in series with the BOOT capacitor to slow down the turn-on of the high-side MOSFET and rising edge overshoot on the SW pin, which comes with the trade off of more power loss and lower efficiency. The recommended BOOT resistor value to decrease the SW pin overshoot is 2.2Ω.

7.2.2.2.8 NR/SS Capacitor Selection

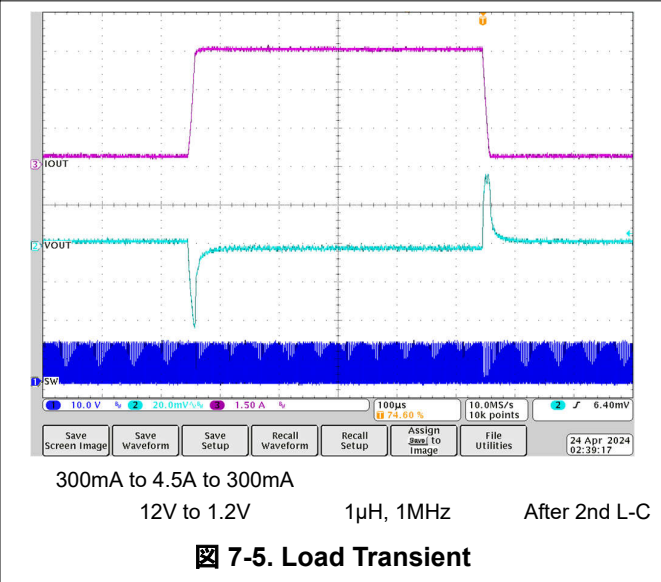
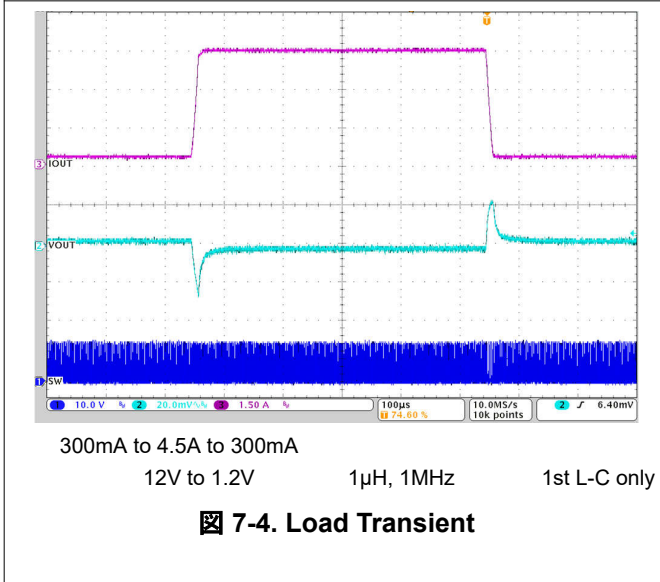
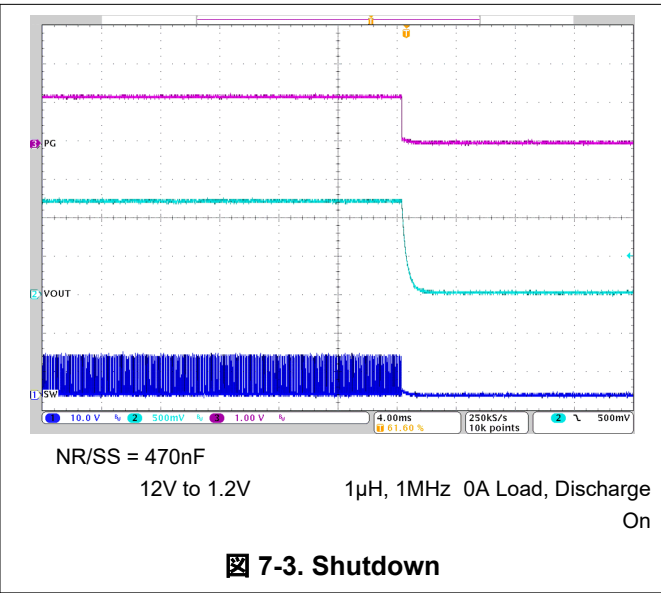
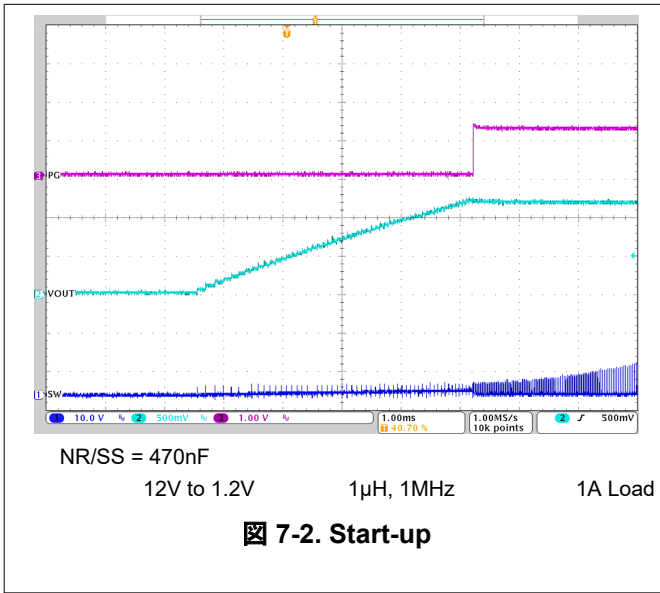
As described in [セクション 6.3.8](#), the NR/SS cap affects both the total noise and the soft-start time. The recommended value for a 5ms soft-start time and good noise performance is 470nF. The maximum NR/SS cap is 3.3μF for a start-up time of 35ms. Values greater than 1μF have minimal improvement in noise performance. Use the following equations to calculate the soft-start time based on desired soft-start time or the chosen capacitor value.

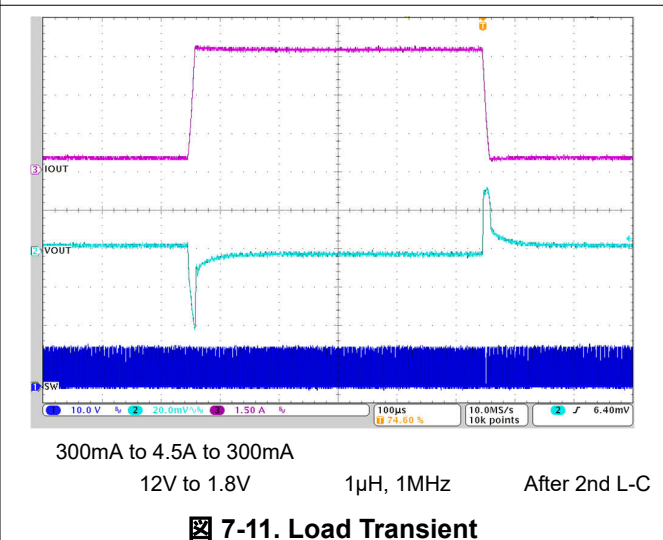
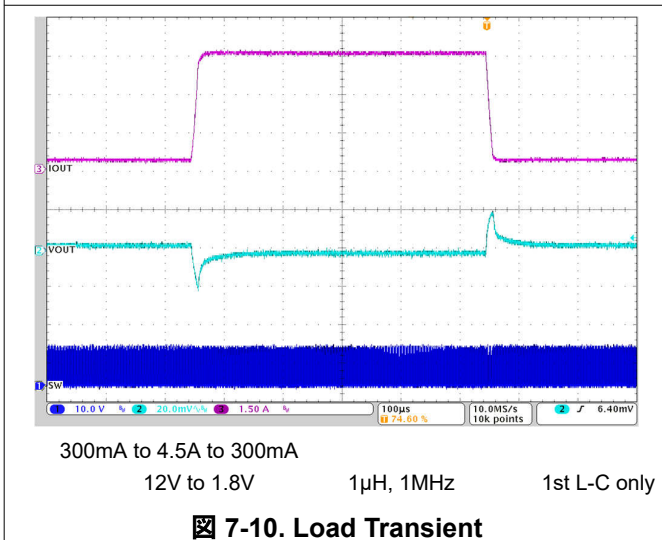
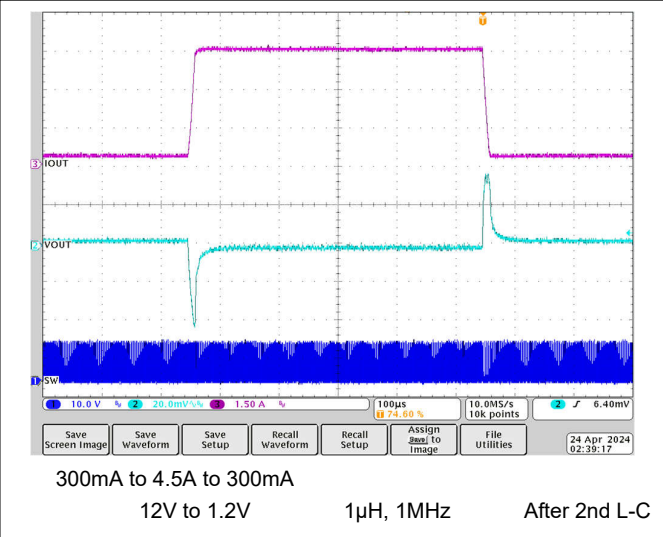
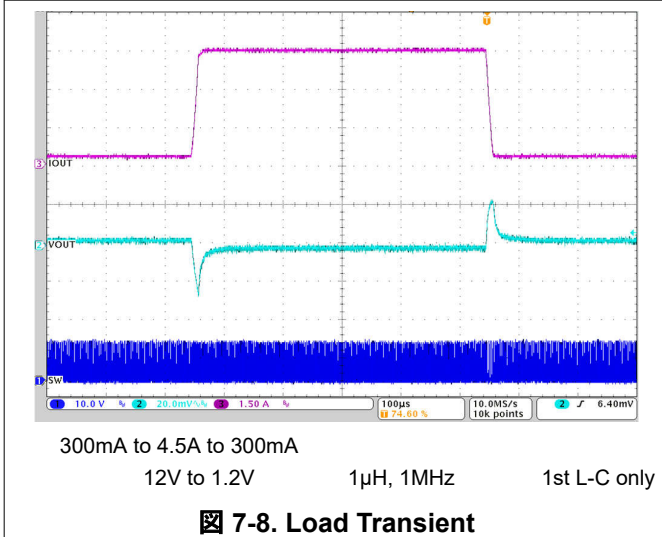
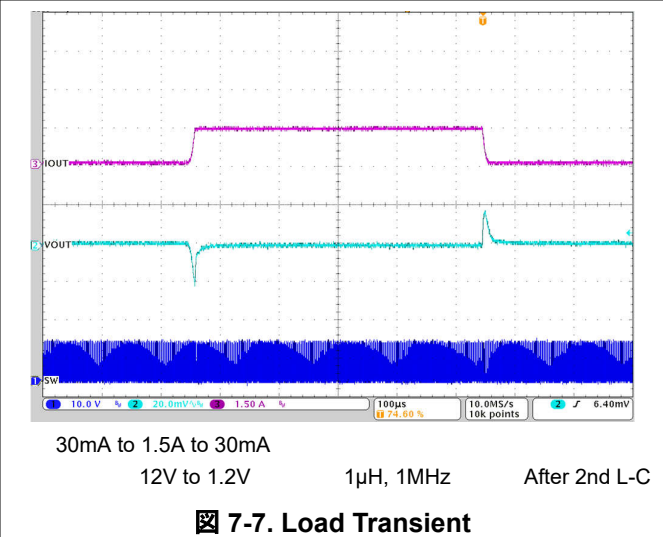
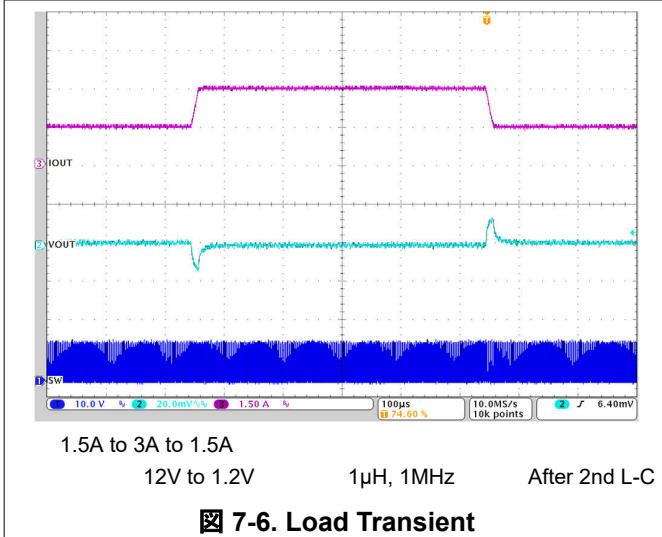
$$t_{ss} (s) = \frac{C_{NRSS} \times 0.8V}{I_{NRSS}} \quad (9)$$

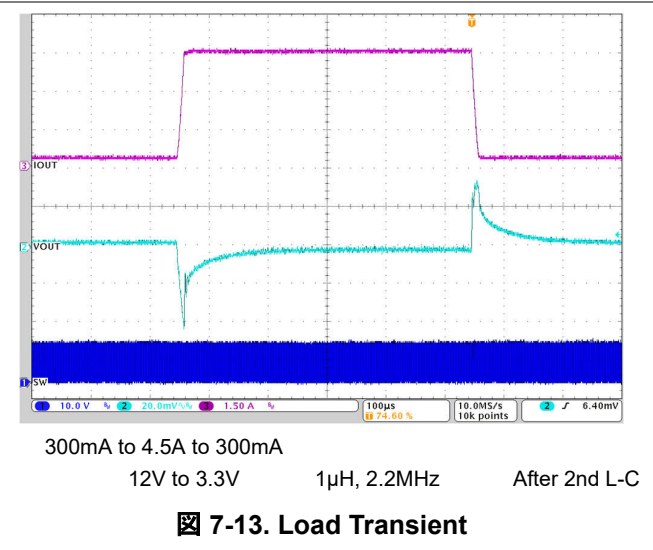
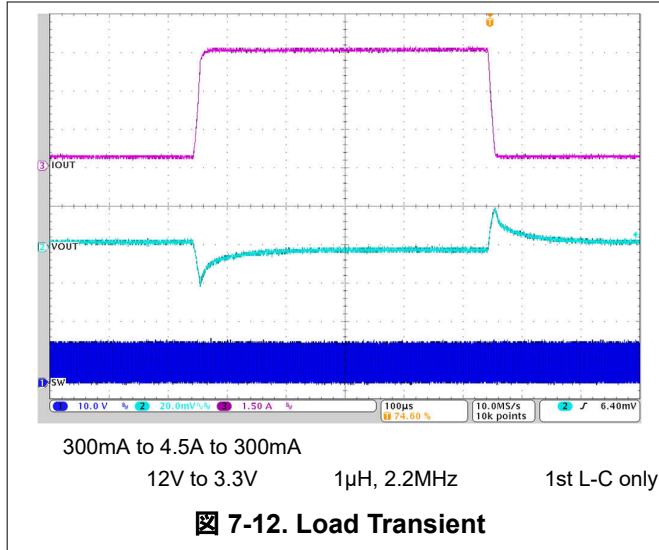
$$C_{NRSS} (F) = \frac{I_{NRSS} \times t_{SS}}{0.8V} \quad (10)$$

7.2.3 Application Curves

$V_{IN} = 12V$, $V_{OUT} = 1.2V$, $T_A = 25^\circ C$, BOM = 表 7-1







7.3 Power Supply Recommendations

The power supply to the TPS6291x-Q1 must have a current rating according to the supply voltage, output voltage, and output current of the TPS6291x-Q1.

7.4 Layout

7.4.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPS6291x-Q1 demands careful attention to make sure of best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the [Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal](#) for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- Place the input capacitor or capacitors as close as possible to the VIN and PGND pins of the device. This placement is the most critical component placement. Route the input capacitors directly to the VIN and PGND pins avoiding vias.
- Place the inductor close to the SW pin. Minimize the copper area at the switch node.
- Place the output capacitor ground close to the PGND pin and route directly avoiding vias. Minimize the length of the connection from the inductor to the output capacitor.
- Connect the VO pin directly to the first output capacitor, C_{OUT} .
- Connect sensitive traces, such as the connections to the NR/SS, VO, and FB pins with short traces and be routed away from any noise source, such as the SW pin.
- Connect the PSNS pin directly to the system GND plane with a via.
- Place the second L-C filter, L_f and C_f , near the load to reduce any radiated coupling around the second L-C filter
- Avoid placing the ferrite bead in the keep out region as shown in [7-15](#)
- Place the FB resistors, R1 and R2, close to the FB pin and route the VOUT connection from R1 to the load as a remote sense trace. If a second L-C filter is used, this connection must be made after L_f .
- See the recommended layout implemented on the EVM and shown in the EVM user's guide, [TPS62968 Step-Down Converter Evaluation Module User's Guide](#), as well as in [7-15](#).

7.4.2 Layout Example

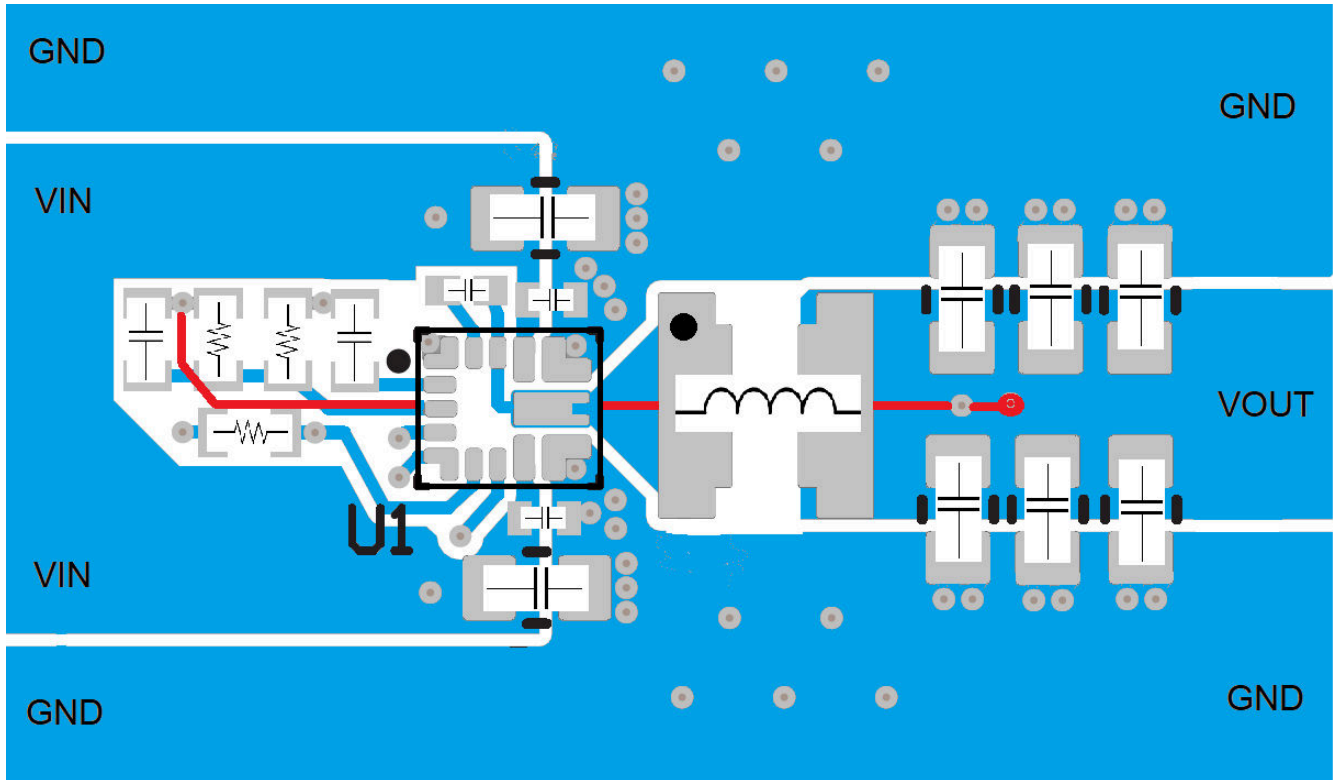


図 7-14. Recommended Layout for Single L-C Filter

注

The start winding of the inductor, as shown in the figures as a black dot, must be connected to the DC/DC converter switch pin, SW, to minimize capacitive coupling to the surrounding area.

注

The red dot indicates where the feedback sense must be placed for the best DC regulation. For a single L-C configuration, the feedback sense is placed near the VOUT capacitors. For a second L-C filter design, the feedback sense is placed near the load after the VOUT_FILTER capacitors.

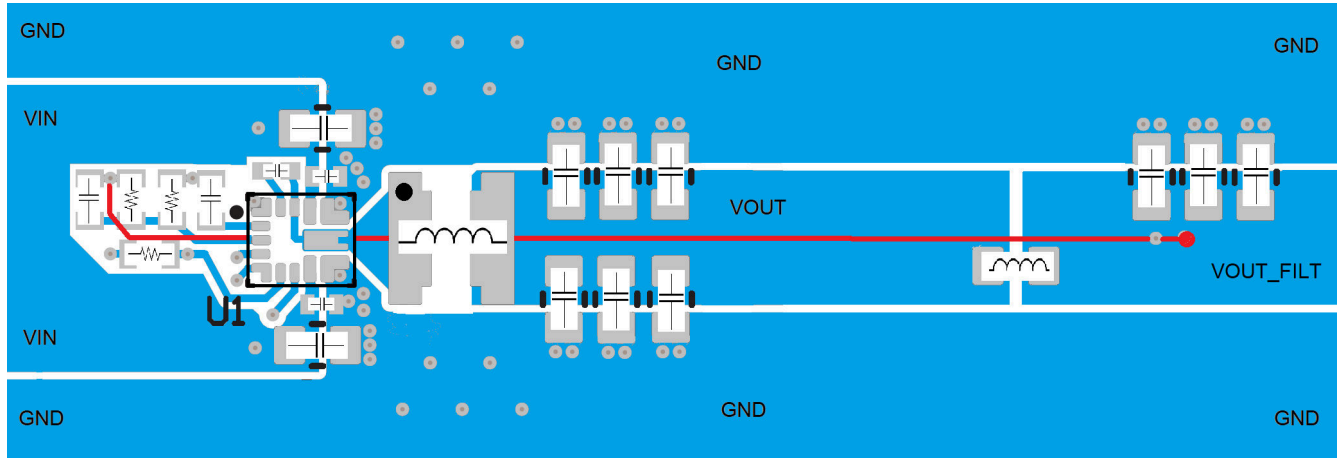


図 7-15. Recommended Layout for Design with Second L-C Filter

注

The ferrite bead can be placed closer to the device as long as the ferrite bead is *not* placed between the inductor and output capacitors. Placing the ferrite bead further away avoids capacitive and electromagnetic coupling to the output of the ferrite bead. If the ferrite bead is placed in the keep out area, the filtering effect of the ferrite bead is greatly reduced. If the ferrite bead is routed through a via to the back side of the board, make sure adequate ground plane between the layers if the ferrite bead are in this area.

8 Device and Documentation Support

8.1 Device Support

8.1.1 サード・パーティ製品に関する免責事項

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8.1.2 Development Support

8.1.2.1 Custom Design With WEBENCH® Tools

[Click here](#) to create a custom design using the TPS6291x-Q1 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Open the advanced tab to optimize for output voltage ripple.
4. After in a TPS6291x-Q1 design, you can enable the second stage L-C filter and change other settings from the drop-down on the left.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Pros and Cons Using a Feedforward Capacitor with a Low Dropout Regulator application report](#)
- Texas Instruments, [TPS62916 Step-Down Converter Evaluation Module User's Guide EVM user's guide](#)
- Texas Instruments, [Five Steps to a Great PCB Layout for a Step-Down Converter analog design journal](#)
- Texas Instruments, [Design Considerations for a Resistive Feedback Divider in a DC/DC Converter analog design journal](#)

8.3 ドキュメントの更新通知を受け取る方法

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[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (November 2024) to Revision B (January 2025)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更.....	1

Changes from Revision * (August 2024) to Revision A (November 2024)	Page
• 動作時の接合部温度の最低値を -55°C から -40°C に変更.....	1
• Added the <i>Thermal Information</i> table.....	4

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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