

# TPS6287x-Q1 2.7V~6V 入力、6A、9A、12A、15A、高速過渡応答付きスタックブル同期整流降圧コンバータ

## 1 特長

- 車載アプリケーション向けに AEC-Q100 認定済み
  - 温度グレード 1: -40°C~+125°C、T<sub>A</sub>
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
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- 2.7V~6V の入力電圧範囲
- ピン互換性のあるデバイス・ファミリー: 6A、9A、12A、15A
- 4 つの出力電圧範囲:
  - 1.25mV 刻みで 0.4V~0.71875V
  - 2.5mV 刻みで 0.4V~1.0375V
  - 5mV 刻みで 0.4V~1.675V
  - 10mV 刻みで 0.8V~3.35V
- ±1% の出力電圧精度
- 7mΩ および 4.5mΩ のパワー MOSFET を内蔵
- 可変外部補償
- スタートアップ時の出力電圧を抵抗によって選択可能
- スイッチング周波数を抵抗によって選択可能
- パワー・セーブまたは強制 PWM 動作
- I<sup>2</sup>C 互換インターフェイス: 最高 1MHz
- 差動リモート・センシング
- オプションのスタック動作により、出力電流能力を向上
- サーマル警告およびサーマル・シャットダウン
- 高精度イネーブル入力
- アクティブ出力放電
- オプションのスペクトラム拡散クロッキング
- ウィンドウ・コンパレータによるパワー・グッド出力
- ウェットプル・フランク付き 2.55mm × 3.55mm × 1mm の VQFN パッケージ
- 40°C~150°C の接合部温度範囲 (T<sub>J</sub>)

## 2 アプリケーション

- インフォテインメントおよびクラスタ
- 先進運転支援システム (ADAS)
- FPGA、ASIC、デジタル・コア電源
- DDR メモリ電源

## 3 概要

TPS6287x-Q1 は、差動リモート・センシング機能を搭載したピン互換の 6A、9A、12A、15A 同期整流降圧 DC/DC コンバータのファミリーです。各電流定格に、I<sup>2</sup>C インターフェイス付きのフル機能のデバイス・バリエーションと I<sup>2</sup>C インターフェイスなしの制限機能付きデバイス・バリエーションがあります。すべてのデバイスは、高い効率と使いやすさを特長としています。低抵抗の電源スイッチにより、高い周囲温度でも最大 15A の連続出力電流を供給できます。

これらのデバイスをスタック・モードで動作させることで、大きな出力電流を供給することや、消費電力を複数のデバイスに分散することが可能です。

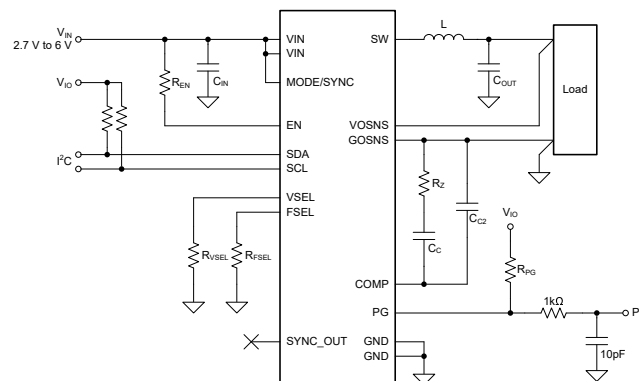
TPS6287x-Q1 ファミリーは、固定周波数動作で高速過渡応答をサポートする拡張 DCS 制御方式を実装しています。デバイスは、最大効率を達成するパワー・セーブ・モード、または最高の過渡性能と最小の出力電圧リップルを実現する強制 PWM モードで動作できます。

オプションのリモート・センシング機能は、POL (ポイント・オブ・ロード) での電圧レギュレーションを最大化し、あらゆる動作条件において ±1% 以内の DC 電圧精度を実現します。

### 製品情報

部品番号 <sup>(2)</sup>	電流定格	パッケージ <sup>(1)</sup>
TPS62870-Q1	6A	RXS (VQFN-FCRLF, 16)
TPS62871-Q1	9A	
TPS62872-Q1	12A	
TPS62873-Q1	15A	

- 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
- 「デバイスのオプション」表を参照してください。



TPS6287x-Q1 の概略回路図



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

<b>Changes from Revision B (January 2023) to Revision C (October 2023)</b>	<b>Page</b>
• Updated the <i>Device Options</i> Table.....	3
• Updated <a href="#">図 9-5</a> to add inductor value.....	16
• Updated <a href="#">表 9-5</a> to reflect new available Orderable Part Number.....	22
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• Updated <a href="#">図 10-18</a> to show device performance up to 20 MHz.....	48
<b>Changes from Revision A (July 2022) to Revision B (January 2023)</b>	<b>Page</b>
• Updated the <i>Device Options</i> Table.....	3
• Modified MODE/SYNC pin Description in <a href="#">Pin Functions</a> .....	5
• Changed the title of <a href="#">図 8-5</a> .....	12
• Added approximate minimum on time value.....	16
• Added behavior of device when EN is toggled and input voltage is applied.....	18
• Updated <a href="#">表 9-5</a> to reflect new available Orderable Part Number.....	22
• Added a comment on how to connect secondary devices SYNC_OUT pin.....	29
• Added a footnote to <a href="#">表 9-10</a> .....	33
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• Added Number of phases N $\phi$ and adapted passive component selection equations in <a href="#">Typical Application</a> ...	43
<b>Changes from Revision * (May 2022) to Revision A (July 2022)</b>	<b>Page</b>
• ドキュメントのステータスを「事前情報」から「量産データ」に変更.....	1

## 5 概要 (続き)

スイッチング周波数は、FSEL ピンに接続した抵抗により選択できます。スイッチング周波数は 1.5MHz、2.25MHz、2.5MHz、3.0MHz のいずれかに設定できます。または、同じ周波数範囲の外部クロックに同期させることができます。

I<sup>2</sup>C 互換インターフェイスを使うと、各種の制御、監視、警告機能 (電圧の監視、温度に関連する警告など) を実現できます。出力電圧は、アプリケーションの性能要求に負荷の消費電力が適合するように、I<sup>2</sup>C 互換インターフェイスを使って素早く調整できます。デフォルトの起動電圧は、VSEL ピンに接続した抵抗により選択できます。

## 6 Device Options

表 6-1. Devices With I<sup>2</sup>C Interface

Device Number	Output Current	Start-Up Voltage, I <sup>2</sup> C Address <sup>(1) (2)</sup>	VSEL Settings	Spread Spectrum Clocking	Soft-Start Time
TPS62870QWRXSRQ1	6 A	0.850 V, 0x40	6.2 kΩ to GND	Default setting = off	Default setting = 1 ms
TPS62871QWRXSRQ1	9 A	0.750 V, 0x41	Short to GND		
TPS62872QWRXSRQ1	12 A	0.875 V, 0x42	Short to VIN		
TPS62873QWRXSRQ1	15 A	1.000 V, 0x43	47 kΩ to VIN		
TPS62870Y1QWRXSRQ1	6 A	0.800 V, 0x40	6.2 kΩ to GND	Default setting = off	Default setting = 1 ms
TPS62871Y1QWRXSRQ1	9 A	0.750 V, 0x41	Short to GND		
TPS62872Y1QWRXSRQ1	12 A	0.875 V, 0x42	Short to VIN		
TPS62873Y1QWRXSRQ1	15 A	0.800 V, 0x43	47 kΩ to VIN		
TPS62870Y0QWRXSRQ1	6 A	0.500 V, 0x40	6.2 kΩ to GND	Default setting = off	Default setting = 1 ms
		0.750 V, 0x41	Short to GND		
		0.875 V, 0x42	Short to VIN		
		1.050 V, 0x43	47 kΩ to VIN		
TPS62870Y2QWRXSRQ1	6 A	1.800 V, 0x30	6.2kΩ to GND	Default setting = off	Default setting = 1 ms
TPS62872Y2QWRXSRQ1	12 A	1.500 V, 0x31	Short to GND		
		1.750 V, 0x32	Short to VIN		
		3.300 V, 0x33	47 kΩ to VIN		
TPS62870Y3QWRXSRQ1	6 A	0.810 V, 0x40	6.2 kΩ to GND	Default setting = off	Default setting = 1 ms
		0.750 V, 0x41	Short to GND		
		0.875 V, 0x42	Short to VIN		
		1.000 V, 0x43	47 kΩ to VIN		
TPS62872Y4QWRXSRQ1	12 A	0.850 V, 0x40	6.2 kΩ to GND	Default setting = off	Default setting = 1 ms
		0.750 V, 0x41	Short to GND		
		0.875 V, 0x42	Short to VIN		
		0.850 V, 0x43	47 kΩ to VIN		
TPS62871Y5QWRXSRQ1	9 A	1.100 V, 0x10	6.2 kΩ to GND	Default setting = off	Default setting = 1 ms
		1.500 V, 0x11	Short to GND		
		1.750 V, 0x12	Short to VIN		
		3.300 V, 0x13	47 kΩ to VIN		
TPS62871Y6QWRXSRQ1	9 A	1.200 V, 0x20	6.2 kΩ to GND	Default setting = off	Default setting = 1 ms
TPS62872Y6QWRXSRQ1	12 A	1.500 V, 0x21	Short to GND		
		1.750 V, 0x22	Short to VIN		
		2.500 V, 0x23	47 kΩ to VIN		

(1) The I<sup>2</sup>C address is linked to the selected start-up voltage. The user cannot select the start-up voltage and I<sup>2</sup>C address independently.

(2) The user can use the VSEL pin to select which of the four start-up voltages the device uses. For more information, see 表 9-5 and 表 9-10.

**表 6-2. Devices Without I<sup>2</sup>C Interface**

Device Number	Output Current	Start-Up Voltage <sup>(2)</sup>	VSEL Settings	Spread Spectrum Clocking	Soft-Start Time
TPS62870N0QWRXSRQ1	6 A	0.500 V	6.2 kΩ to GND	On	0.5 ms
TPS62871N0QWRXSRQ1	9 A	0.750 V	Short to GND		
TPS62872N0QWRXSRQ1	12 A	0.875 V	Short to VIN		
TPS62873N0QWRXSRQ1	15 A	1.050 V	47 kΩ to VIN		
TPS62870N1QWRXSRQ1	6 A	0.800 V	6.2kΩ to GND	On	1 ms
TPS62871N1QWRXSRQ1	9 A	0.750 V	Short to GND		
TPS62872N1QWRXSRQ1	12 A	0.875 V	Short to VIN		
TPS62873N1QWRXSRQ1	15 A	0.840 V	47 kΩ to VIN		
TPS62872N2QWRXSRQ1	12 A	1.800 V	6.2 kΩ to GND	Off	
		1.500 V	Short to GND		
		1.750 V	Short to VIN		
		3.300 V	47kΩ to VIN		
TPS62872N3QWRXSRQ1	12 A	1.000 V	6.2 kΩ to GND	On	0.5 ms
		0.750 V	Short to GND		
		0.875 V	Short to VIN		
		1.100 V	47kΩ to VIN		

Unless otherwise noted, device variants without I<sup>2</sup>C operate with the same default settings as device variants with I<sup>2</sup>C.

## 7 Pin Configuration and Functions

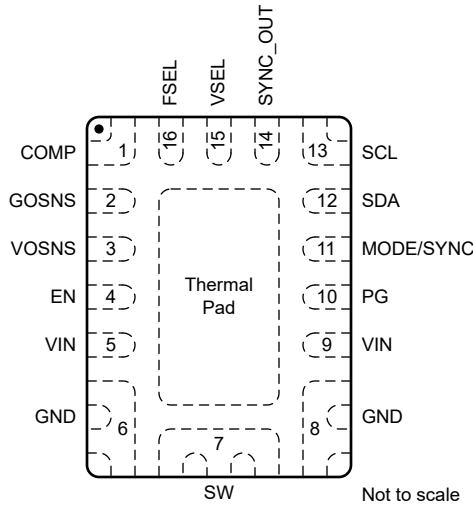


図 7-1. 16-Pin RXS VQFN Package (Top View)

表 7-1. Pin Functions

Pin		Type <sup>(1)</sup>	Description
Name	No.		
COMP	1	—	Device compensation input. A resistor and capacitor from this pin to GOSNS define the compensation of the control loop. In stacked operation, connect the COMP pins of all stacked devices together and connect a resistor and capacitor between the common COMP node and GOSNS.
GOSNS	2	I	Output ground sense (differential output voltage sensing)
VOSNS	3	I	Output voltage sense (differential output voltage sensing)
EN	4	I	This is the enable pin of the device. The user must connect to this pin using a series resistor of at least 15 kΩ. A low logic level on this pin disables the device and a high logic level on this pin enables the device. Do not leave this pin unconnected. For stacked operation, interconnect EN pins of all stacked devices with a resistor to the supply voltage or a GPIO of a processor. See <a href="#">セクション 9.3.17</a> for a detailed description.
VIN	5, 9	P	Power supply input. Connect the input capacitor as close as possible between VIN and GND.
GND	6, 8	GND	Ground pin
SW	7	O	This pin is the switch pin of the converter and is connected to the internal power MOSFETs.
PG	10	I/O	Open-drain power-good output. Low impedance when not "power good," high impedance when "power good." This pin can be left open or be tied to GND when not used in single device operation. In stacked operation, interconnect the PG pins of all stacked devices. Only the PG pin of the primary converter in stacked operation is an open-drain output. For devices that are defined as secondary converters in stacked mode, this pin is an input pin. See <a href="#">セクション 9.3.17</a> for a detailed description.
MODE/SYNC	11	I	The device runs in power save mode when this pin is pulled low. If the pin is pulled high, the device runs in forced-PWM mode. If unused, this pin can be left floating and an internal pulldown resistor will pull it low. The mode pin can also be used to synchronize the device to an external clock.
SDA	12	I/O	I <sup>2</sup> C serial data pin. Do not leave floating. Connect a pullup resistor to a logic high level. Connect to GND for secondary devices in stacked operation and for device variants without I <sup>2</sup> C.
SCL	13	I/O	I <sup>2</sup> C serial clock pin. Do not leave this pin floating. Connect a pullup resistor to a logic high level. Connect this pin to GND for secondary devices in stacked operation and for device variants without I <sup>2</sup> C.

表 7-1. Pin Functions (続き)

Pin		Type <sup>(1)</sup>	Description
Name	No.		
SYNC_OUT	14	O	Internal clock output pin for synchronization in stacked mode. Leave this pin floating for single device operation. Connect this pin to the MODE/SYNC pin of the next device in the daisy-chain in stacked operation. <i>Do not use this pin to connect to a non-TPS6287x-Q1 device.</i> During start-up, this pin is used to identify if a device must operate as a secondary converter in stacked operation. Connect a 47-kΩ resistor from this pin to GND to define a secondary converter in stacked operation. See <a href="#">セクション 9.3.17</a> for a detailed description.
VSEL	15	—	Start-up output voltage select pin. A resistor or short circuit to GND or $V_{IN}$ defines the selected output voltage. See <a href="#">セクション 9.3.6.2</a> .
FSEL	16	—	Frequency select pin. A resistor or a short circuit to GND or $V_{IN}$ determines the free-running switching frequency. See <a href="#">セクション 9.3.6.2</a> .
Exposed Thermal Pad		—	The thermal pad must be soldered to GND to achieve an appropriate thermal resistance and for mechanical stability.

(1) I = input, O = output, P = power, GND = ground

## 8 Specifications

### 8.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	VIN <sup>(4)</sup>	-0.3	6.5	V
	SW (DC)	-0.3	V <sub>IN</sub> + 0.3	
	SW (AC, less than 10ns) <sup>(3)</sup>	-3	10	
	VOSNS	-0.3	3.8	
	SCL, SDA	-0.3	5.5	
	FSEL, VSEL, EN, MODE/SYNC	-0.3	6.5	
	GOSNS	-0.3	0.3	
Voltage <sup>(2)</sup>	PG	-0.3	6.5	
Current	SYNC_OUT	-1	1	mA
	COMP	-1	1	
	PG		5	
T <sub>J</sub>	Junction temperature	-40	150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to the GND pin.
- (3) While switching.
- (4) The voltage at the pin can exceed the 6.5 V absolute max condition for a short period of time, but must remain less than 8 V. VIN at 8 V for a 100ms duration is equivalent to approximately 8 hours of aging for the device at room temperature.

### 8.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> HBM ESD classification level 2	±2000	V
		Charged device model (CDM) per AEC Q100-011 CDM ESD classification level C4A	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 8.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Input voltage	VIN	2.7	6	V
		SDA, SCL		5	
V <sub>OUT</sub>	Output voltage	0.4		3.35 V or (V <sub>IN</sub> - 1.4 V) <sup>(1)</sup>	V
I <sub>OUT</sub>	Output current	TPS62870-Q1		6	A
		TPS62871-Q1		9	
		TPS62872-Q1		12	
		TPS62873-Q1		15	
L	Inductance		110	330	nH
		f <sub>SW</sub> ≥ 2.25 MHz and V <sub>OUT</sub> ≤ 1.675 V	55	330	

### 8.3 Recommended Operating Conditions (続き)

Over operating temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
C <sub>IN</sub>	Input capacitance (per pin) <sup>(2)</sup>	V <sub>IN</sub>	5	10		μF
C <sub>OUT</sub>	Output capacitance <sup>(2)</sup>		40		<sup>(3)</sup>	
C <sub>PAR</sub>	Parasitic capacitance	VSEL, FSEL			100	pF
		SYNC_OUT			20	
	Resistor tolerance	VSEL, FSEL			±2%	
T <sub>J</sub>	Operating junction temperature		−40		150	

- (1) Whichever value is lower.
- (2) Effective capacitance.
- (3) The maximum recommended output capacitance depends on the specific operating conditions of an application. Output capacitance values up to a few millifarad are typically possible, however.

### 8.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS6287x		UNIT
		RXS (JEDEC)	RXS (EVM)	
		16 PINS	16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	43.2	28	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	19.2	N/A	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	7.7	N/A	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.5	1.5	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	7.7	9.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	6.3	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 8.5 Electrical Characteristics

over operating junction temperature (T<sub>J</sub> = −40 °C to 150 °C) and V<sub>IN</sub> = 2.7 V to 6 V. Typical values at V<sub>IN</sub> = 3.3 V and T<sub>J</sub> = 25 °C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>SUPPLY</b>							
I <sub>Q</sub>	Supply current (V <sub>IN</sub> )	Operating	EN = high, I <sub>OUT</sub> = 0 mA, V <sub>(SW)</sub> = 0 V, primary operation, device not switching, T <sub>J</sub> = 25 °C		1.75	3	mA
		Standby	EN = low, V <sub>(SW)</sub> = 0 V, T <sub>J</sub> = 25 °C		16.5	40	μA
V <sub>IT+</sub>	Positive-going UVLO threshold voltage (V <sub>IN</sub> )			2.5	2.6	2.7	V
V <sub>IT−</sub>	Negative-going UVLO threshold voltage (V <sub>IN</sub> )			2.4	2.5	2.6	V
V <sub>hys</sub>	UVLO hysteresis voltage (V <sub>IN</sub> )			90			mV
V <sub>IT+</sub>	Positive-going OVLO threshold voltage (V <sub>IN</sub> )			6.1	6.3	6.5	V
V <sub>IT−</sub>	Negative-going OVLO threshold voltage (V <sub>IN</sub> )			6.0	6.2	6.4	V
V <sub>hys</sub>	OVLO hysteresis voltage (V <sub>IN</sub> )			85			mV
V <sub>IT−</sub>	Negative-going power-on reset threshold			1.4			V



## 8.5 Electrical Characteristics (続き)

over operating junction temperature ( $T_J = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ ) and  $V_{IN} = 2.7\text{ V}$  to  $6\text{ V}$ . Typical values at  $V_{IN} = 3.3\text{ V}$  and  $T_J = 25\text{ }^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{SD}$	Thermal shutdown threshold temperature	$T_J$ rising		170		$^\circ\text{C}$
	Thermal shutdown hysteresis			20		$^\circ\text{C}$
$T_W$	Thermal warning threshold temperature	$T_J$ rising		150		$^\circ\text{C}$
	Thermal warning hysteresis			20		$^\circ\text{C}$
<b>CONTROL and INTERFACE</b>						
$V_{IT+}$	Positive-going input threshold voltage (EN)		0.97	1.0	1.03	V
$V_{IT-}$	Negative-going input threshold voltage (EN)		0.87	0.9	0.93	V
$V_{hys}$	Hysteresis voltage (EN)		95			mV
$I_{IH}$	High-level input current (EN)	$V_{IH} = V_{IN}$ , internal pulldown resistor disabled			200	nA
$I_{IL}$	Low-level input current (EN)	$V_{IL} = 0\text{ V}$ , internal pulldown resistor disabled	-200			nA
$V_{IH}$	High-level input voltage (SDA, SCL, MODE/SYNC, VSEL, FSEL, SYNC_OUT)		0.8			V
$V_{IL}$	Low-level input voltage (SDA, SCL, MODE/SYNC, VSEL, FSEL, SYNC_OUT)				0.4	V
$V_{OL}$	Low-level output voltage (SDA)	$I_{OL} = 3\text{ mA}$			0.4	V
		$I_{OL} = 9\text{ mA}$			0.4	V
		$I_{OL} = 5\text{ mA}$			0.2	V
$I_{OH}$	High-level output current (SDA, SCL)	$V_{OH} = 3.3\text{ V}$			200	nA
$I_{IL}$	Low-level input current (MODE/SYNC)	$V_{IL} = 0\text{ V}$	-150		150	nA
$I_{IH}$	High-level input current (MODE/SYNC)	$V_{IH} = V_{IN}$			3	$\mu\text{A}$
$I_{IL}$	Low-level input current (SYNC_OUT)	$V_{IL} = 0\text{ V}$	-250			nA
$I_{IH}$	High-level input current (SYNC_OUT)	$V_{IH} = 2\text{ V}$			150	nA
$t_{d(EN)1}$	Enable delay time when EN tied to $V_{IN}$	Measured from when EN goes high to when device starts switching $SR_{VIN} = 1\text{ V}/\mu\text{s}$		175	500	$\mu\text{s}$
$t_{d(EN)2}$	Enable delay time when $V_{IN}$ already applied	Measured from when EN goes high to when device starts switching			100	$\mu\text{s}$
$t_{d(RAMP)}$	Output voltage ramp time	Measured from when device starts switching to rising edge of PG	0.35	0.5	0.65	ms
			0.7	1	1.3	ms
			1.4	2	2.6	ms
			2.8	4	5.2	ms
	Time to lock external frequency			50		$\mu\text{s}$
	Internal pullup resistance (VSEL, FSEL)		5.5		9	k $\Omega$
	Internal pulldown resistance (VSEL, FSEL)		1.3		2.2	k $\Omega$
$V_{T+}$	Positive-going power good threshold voltage (output undervoltage)		94	96	98	$\%V_{OUT}$
$V_{T-}$	Negative-going power good threshold voltage (output undervoltage)		92	94	96	$\%V_{OUT}$
$V_{T+}$	Positive-going power good threshold voltage (output overvoltage)		104	106	108	$\%V_{OUT}$
$V_{T-}$	Negative-going power good threshold voltage (output overvoltage)		102	104	106	$\%V_{OUT}$

## 8.5 Electrical Characteristics (続き)

over operating junction temperature ( $T_J = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ ) and  $V_{IN} = 2.7\text{ V}$  to  $6\text{ V}$ . Typical values at  $V_{IN} = 3.3\text{ V}$  and  $T_J = 25\text{ }^\circ\text{C}$  (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OL}$	Low-level output voltage (PG)	$I_{OL} = 1\text{ mA}$			0.3	V
$I_{OH}$	High-level output current (PG)	$V_{OH} = 3.3\text{ V}$			200	nA
$V_{IH}$	High-level input voltage (PG)	Device configured as a secondary device in stacked operation	0.8			V
$V_{IL}$	Low-level input voltage (PG)	Device configured as a secondary device in stacked operation			0.4	V
$I_{IH}$	High-level input current (PG)	Device configured as a secondary device in stacked operation			1	$\mu\text{A}$
$I_{IL}$	Low-level input current (PG)	Device configured as a secondary device in stacked operation	-1			$\mu\text{A}$
$t_{d(PG)}$	Deglintch time (PG)	High-to-low or low-to-high transition on the PG pin	34	40	46	$\mu\text{s}$
<b>OUTPUT</b>						
$V_{OUT}$	Output accuracy	$V_{IN} \geq V_{OUT} + 1.4\text{ V}$	-1		1	%
$I_{IB}$	Input bias current (GOSNS)	$V_{(GOSNS)} = -100\text{ mV}$ to $100\text{ mV}$	-6			$\mu\text{A}$
$I_{IB}$	Input bias current (VOSNS)	$V_{(VOSNS)} = 3.3\text{ V}$ , $V_{IN} = 6\text{ V}$			6	$\mu\text{A}$
$V_{ICR}$	Input common-mode range (GOSNS)		-100		100	mV
$f_{SW}$	Switching frequency (SW)	$f_{SW} = 1.5\text{ MHz}$ , PWM operation, $V_{IN} 3.3\text{ V}$ , $V_{OUT} = 0.75\text{ V}$	1.35	1.5	1.65	MHz
		$f_{SW} = 2.25\text{ MHz}$ , PWM operation, $V_{IN} 3.3\text{ V}$ , $V_{OUT} = 0.75\text{ V}$	2.025	2.25	2.475	
		$f_{SW} = 2.5\text{ MHz}$ , PWM operation, $V_{IN} 3.3\text{ V}$ , $V_{OUT} = 0.75\text{ V}$	2.25	2.5	2.75	
		$f_{SW} = 3\text{ MHz}$ , PWM operation, $V_{IN} 3.3\text{ V}$ , $V_{OUT} = 0.75\text{ V}$	2.7	3	3.3	
$f_{mod}$	Frequency of the spread-spectrum sweep			$f_{sw}/2048$		kHz
$\Delta f_{SW}$	Switching frequency variation during spread-spectrum operation			$\pm 10\%$		
$\tau$	Emulated current time constant			12.5		$\mu\text{s}$
$r_{DS(on)}$	High-side FET static on-state resistance	$V_{IN} = 3.3\text{ V}$		7	16	$\text{m}\Omega$
$r_{DS(on)}$	Low-side FET static on-state resistance	$V_{IN} = 3.3\text{ V}$		4.1	9.4	$\text{m}\Omega$
$I_{(SW)(off)}$	High-side FET off-state current	$V_{IN} = 6\text{ V}$ , $V_{(SW)} = 0\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$	-1			$\mu\text{A}$
	Low-side FET off-state current	$V_{IN} = 6\text{ V}$ , $V_{(SW)} = 6\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$			100	
$I_{LIM}$	High-side FET forward switch current limit, DC	TPS62870-Q1	9	12	14	A
		TPS62871-Q1	12	16	18	
		TPS62872-Q1	15	20	22	
		TPS62873-Q1	18	24	26	
	Low-side FET negative current limit, DC		7.5		12	A

## 8.6 I<sup>2</sup>C Interface Timing Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{SCL}$	SCL clock frequency	Standard mode			100	kHz
		Fast mode			400	
		Fast mode plus			1000	

## 8.6 I<sup>2</sup>C Interface Timing Characteristics (続き)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>HD</sub> ; t <sub>STA</sub>	Hold time (repeated) START condition	Standard mode	4			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
t <sub>LOW</sub>	LOW period of the SCL clock	Standard mode	4.7			μs
		Fast mode	1.3			
		Fast mode plus	0.5			
t <sub>HIGH</sub>	HIGH period of the SCL clock	Standard mode	4			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
t <sub>SU</sub> ; t <sub>STA</sub>	Setup time for a repeated START condition	Standard mode	4.7			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
t <sub>HD</sub> ; t <sub>DAT</sub>	Data hold time	Standard mode	0		3.45	μs
		Fast mode	0		0.9	
		Fast mode plus	0			
t <sub>SU</sub> ; t <sub>DAT</sub>	Data setup time	Standard mode	250			ns
		Fast mode	100			
		Fast mode plus	50			
t <sub>r</sub>	Rise time of both SDA and SCL signals	Standard mode			1000	ns
		Fast mode	20		300	
		Fast mode plus			120	
t <sub>f</sub>	Fall time of both SDA and SCL signals	Standard mode			300	ns
		Fast mode	20×V <sub>DD</sub> /5.5V		300	
		Fast mode plus	20×V <sub>DD</sub> /5.5V		120	
t <sub>SU</sub> ; t <sub>STO</sub>	Setup time for STOP condition	Standard mode	4			μs
		Fast mode	0.6			
		Fast mode plus	0.26			
t <sub>BUF</sub>	Bus free time between a STOP and START condition	Standard mode	4.7			μs
		Fast mode	1.3			
		Fast mode plus	0.5			
C <sub>b</sub>	Capacitive load for each bus line	Standard mode			400	pF
		Fast mode			400	
		Fast mode plus			550	

## 8.7 Timing Requirements

			MIN	NOM	MAX	UNIT
f <sub>(SYNC)</sub>	Synchronization clock frequency range (MODE/SYNC)	Nominal f <sub>SW</sub> = 1.5 MHz	1.3		2.0	MHz
f <sub>(SYNC)</sub>	Synchronization clock frequency range (MODE/SYNC)	Nominal f <sub>SW</sub> = 2.25 MHz	1.8		2.7	MHz
f <sub>(SYNC)</sub>	Synchronization clock frequency range (MODE/SYNC)	Nominal f <sub>SW</sub> = 2.5 MHz	2.0		3.0	MHz
f <sub>(SYNC)</sub>	Synchronization clock frequency range (MODE/SYNC)	Nominal f <sub>SW</sub> = 3.0 MHz	2.5		3.3	MHz

		MIN	NOM	MAX	UNIT
$D_{(SYNC)}$	Synchronization clock duty cycle range (MODE/SYNC)	45%		55%	

## 8.8 Typical Characteristics

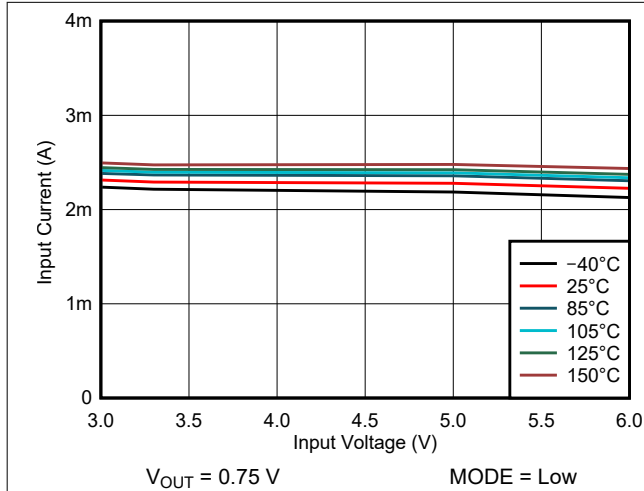


图 8-1. Operating Supply Current (Power Save Mode)

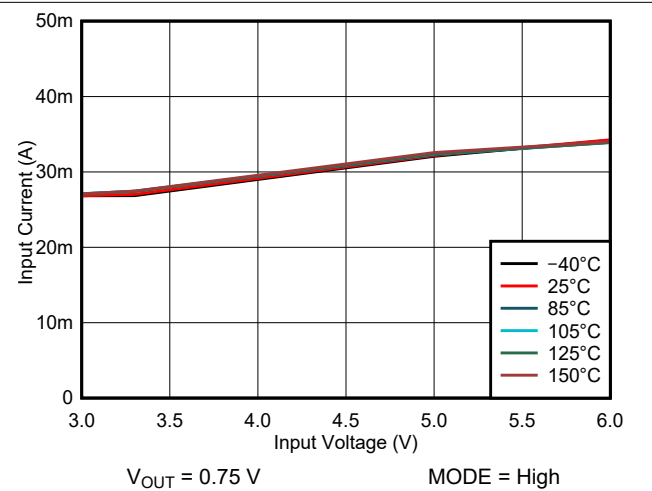


图 8-2. Operating Supply Current (Forced PWM)

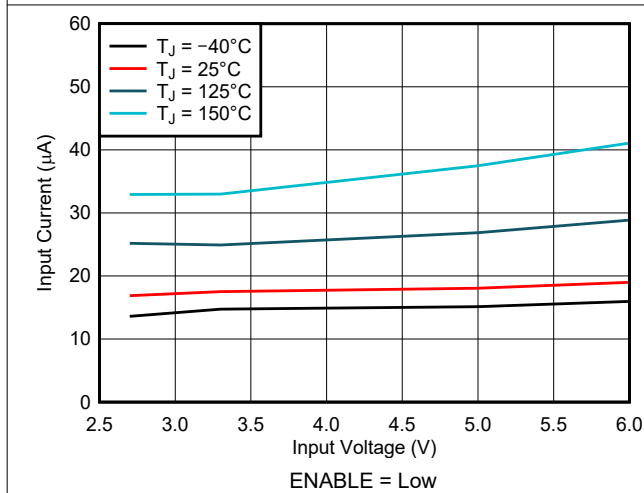


图 8-3. Quiescent Supply Current

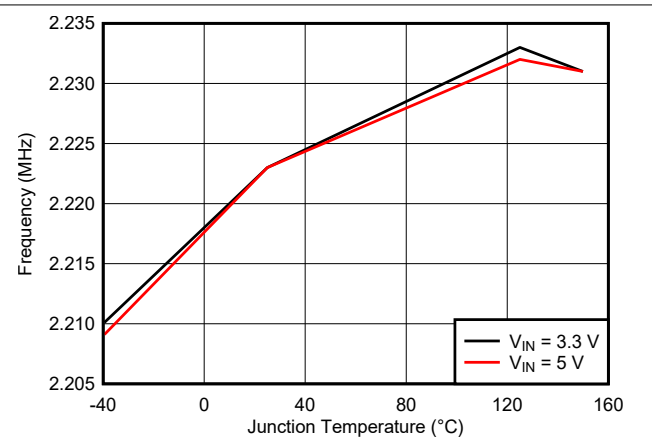
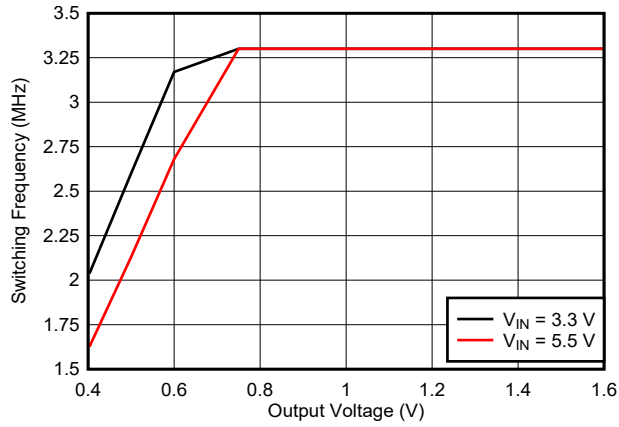


图 8-4. Switching Frequency vs Temperature

## 8.8 Typical Characteristics (continued)




**8-5. Maximum Switching Frequency vs  $V_{IN}$  and  $V_{OUT}$**

## 9 Detailed Description

### 9.1 Overview

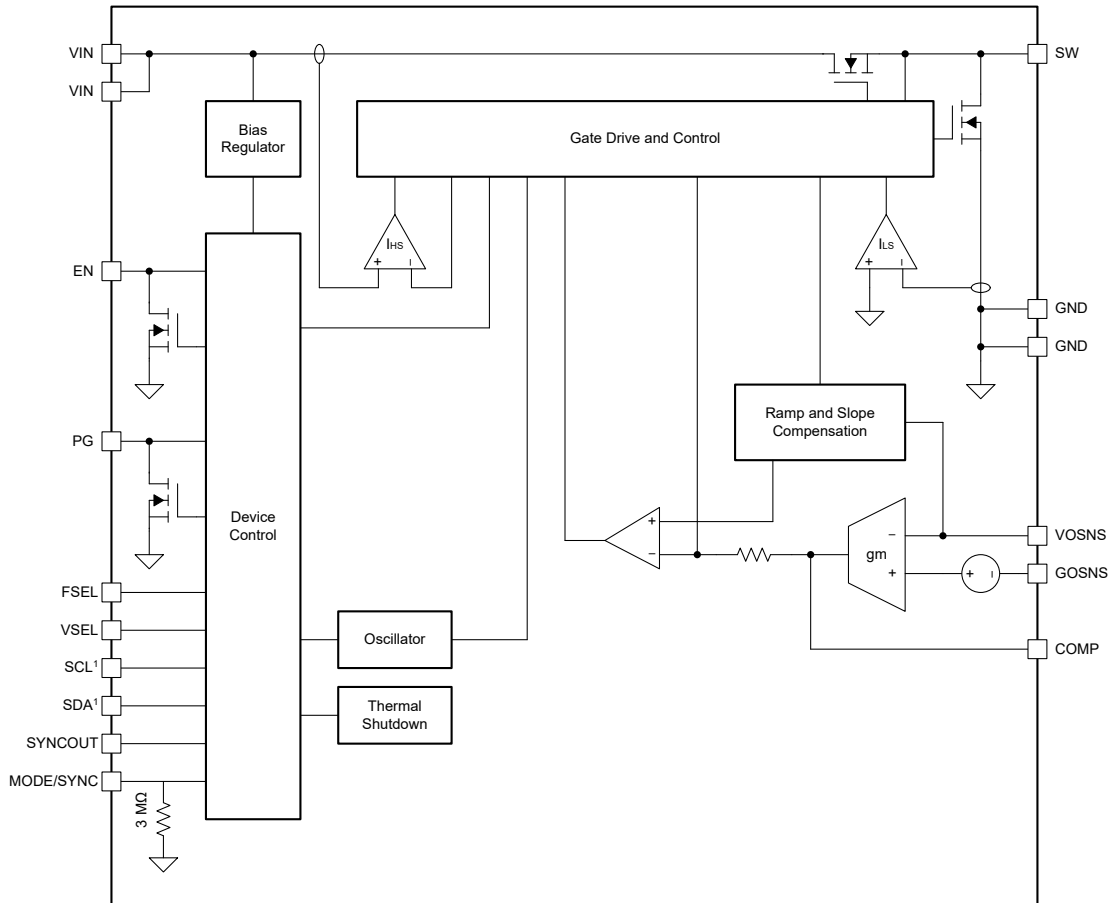
The TPS6287x-Q1 devices are synchronous step-down (buck) DC/DC converters. These devices use an enhanced DCS control topology to achieve fast transient response while switching with a fixed frequency. Together, with their low output voltage ripple, high DC accuracy, and differential remote sensing, these devices are ideal for supplying the cores of modern high-performance processors.

The family of devices includes 6-A, 9-A, 12-A, and 15-A devices. To further increase the output current capability, the user can combine multiple devices in a “stack”. For example, a stack of two TPS62873-Q1 devices have a current capability of 30 A. Each device of a stack must have the same current rating to avoid that one device enters current limit too early.

For each current rating, there are full-featured devices with an I<sup>2</sup>C interface and limited-featured devices without an I<sup>2</sup>C interface (see the [Device Options](#)). The user can use a device variant without I<sup>2</sup>C in exactly the same way as a device variant with I<sup>2</sup>C, except that:

- The user must connect the unused SCL and SDA pins to GND.
- The user must be aware of the (fixed) factory settings for parameters and functions that are programmable in the I<sup>2</sup>C device variants.

## 9.2 Functional Block Diagram



1. In device variants without I<sup>2</sup>C the SDA and SCL pins are internally connected, but their functionality is disabled.

## 9.3 Feature Description

### 9.3.1 Fixed-Frequency DCS Control Topology

Figure 9-1 shows a simplified block diagram of the fixed-frequency enhanced DCS control topology used in the TPS6287x-Q1 devices. This topology is comprised of an inner emulated current loop, a middle direct feedback loop, and an outer voltage-regulating loop.

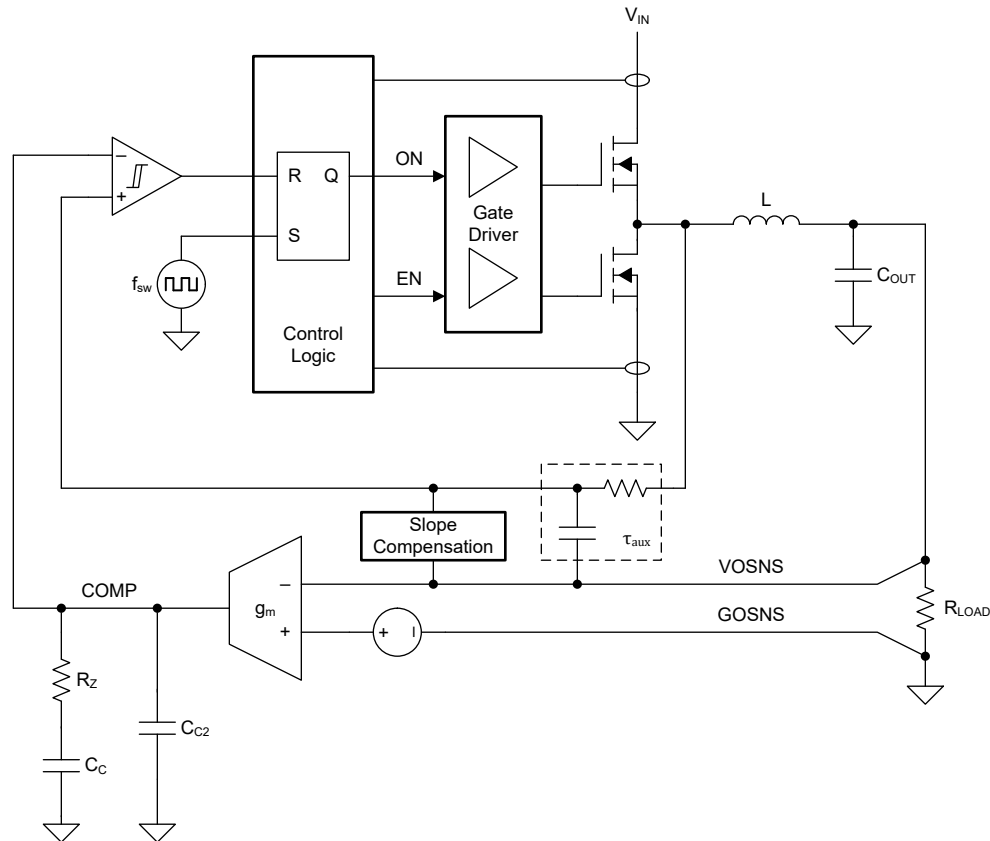


Figure 9-1. Fixed-Frequency DCS Control Topology (Simplified)

### 9.3.2 Forced PWM and Power Save Modes

The device can control the inductor current in three different ways to regulate the output:

- Pulse-width modulation with continuous inductor current (PWM-CCM)
- Pulse-width modulation with discontinuous inductor current (PWM-DCM)
- Pulse-frequency modulation with discontinuous inductor current and pulse skipping (PFM-DCM)

During PWM-CCM operation, the device switches at a constant frequency and the inductor current is continuous (see Figure 9-2). PWM operation achieves the lowest output voltage ripple and the best transient performance.



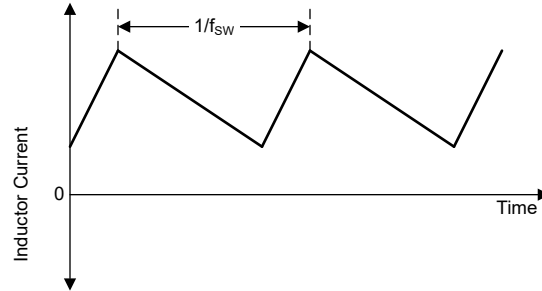


図 9-2. Continuous Conduction Mode (PWM-CCM) Current Waveform

During PWM-DCM operation, the device switches at a constant frequency and the inductor current is discontinuous (see 図 9-3). In this mode, the device controls the peak inductor current to maintain the selected switching frequency while still being able to regulate the output.

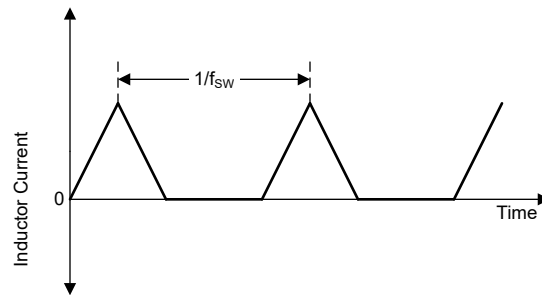


図 9-3. Discontinuous Conduction Mode (PWM-DCM) Current Waveform

During PFM-DCM operation, the device keeps the peak inductor current constant (at a level corresponding to the minimum on time of the converter) and skips pulses to regulate the output (see 図 9-4). The switching pulses that occur during PFM-DCM operation are synchronized to the internal clock.

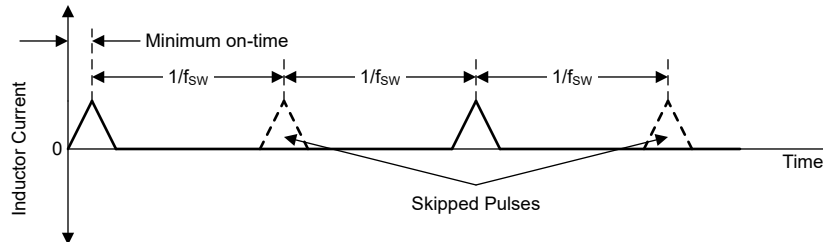


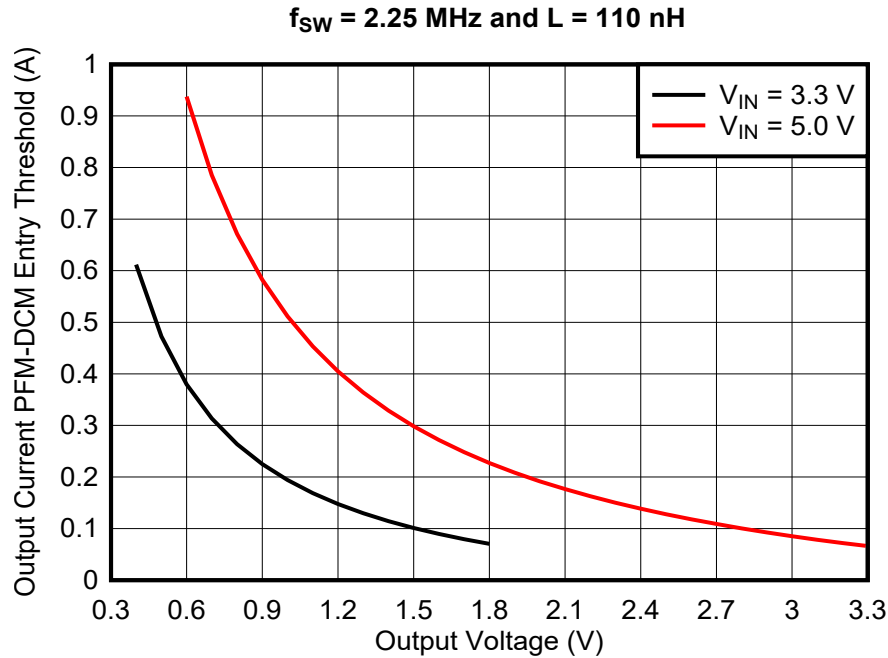
図 9-4. Discontinuous Conduction Mode (PFM-DCM) Current Waveform

For very small output voltages, an absolute minimum on time of approximately 50 ns reduces the switching frequency from the set value. 図 8-5 shows the maximum switching frequency with 3.3-V and 5.5-V supplies.

Use 式 1 to calculate the output current threshold at which the device enters PFM-DCM.

$$I_{OUT(PFM)} = \frac{(V_{IN} - V_{OUT})}{2L} t_{ON}^2 \left( \frac{V_{IN}}{V_{OUT}} \right) f_{sw} \quad (1)$$

図 9-5 shows how this threshold typically varies with  $V_{IN}$  and  $V_{OUT}$  for a switching frequency of 2.25 MHz.



**図 9-5. Output Current PFM-DCM Entry Threshold**

The user can configure the device to use either forced PWM (FPWM) mode or power save mode (PSM):

- In forced PWM mode, the device uses PWM-CCM at all times.
- In power save mode, the device uses PWM-CCM at medium and high loads, PWM-DCM at low loads, and PFM-DCM at very low loads. The transition between the different operating modes is seamless.

表 9-1 shows the function table of the MODE/SYNC pin and the FPWMEN bit in the CONTROL1 register, which control the operating mode of the device.

**表 9-1. FPWM Mode and Power-Save Mode Selection**

MODE/SYNC Pin	FPWMEN Bit	Operating Mode	Remark
Low	0	PSM	Do not use in a stacked configuration.
	1	FPWM	
High	X	FPWM	
Sync Clock	X	FPWM	

### 9.3.3 Precise Enable

The Enable (EN) pin is bidirectional and has two functions:

- As an input, EN enables and disables the DC/DC converter in the device.
- As an output, EN provides a SYSTEM\_READY signal to other devices in a stacked configuration.

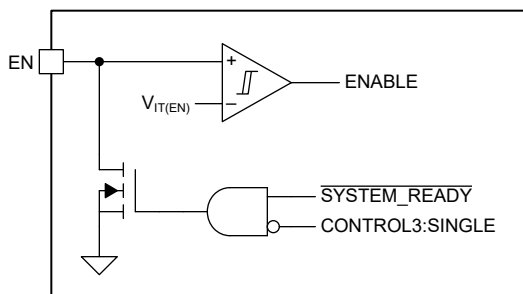


図 9-6. Enable Functional Block Diagram

Because there is an internal open-drain transistor connected to the EN pin, do not drive this pin directly from a low-impedance source. Instead, use a resistor to limit the current flowing into the EN pin (see [セクション 10](#)).

When power is first applied to the VIN pin, the device pulls the EN pin low until it has loaded its default register settings from nonvolatile memory and read the state of the VSEL, FSEL, and SYNCOUT pins. The device also pulls EN low if a fault, such as thermal shutdown or overvoltage lockout, occurs. In stacked configurations, all devices share a common enable signal, which means that the DC/DC converters in the stack cannot start to switch until *all* devices in the stack have completed their initialization. Similarly, a fault in one or more devices in the stack disables *all* converters in the stack (see [セクション 9.3.17](#)).

In standalone (nonstacked) applications, the user can disable the active pulldown of the EN pin if the user sets SINGLE = 1 in the CONTROL3 register. Fault conditions have no effect on the EN pin when SINGLE = 1 (the EN pin is *always* pulled down during device initialization). In stacked applications, ensure that SINGLE = 0.

When the internal `SYSTEM_READY` signal is low (that is, initialization is complete and there are no fault conditions), the internal open-drain transistor is high impedance and the EN pin functions like a standard input. A high level on the EN pin enables the DC/DC converter in the device. A low level disables the DC/DC converter (the I<sup>2</sup>C interface is enabled as soon as the device has completed its initialization and is not affected by the state of the internal ENABLE or `SYSTEM_READY` signals).

A low level on the EN pin forces the device into shutdown. During shutdown, the MOSFETs in the power stage are off, the internal control circuitry is disabled, and the device consumes only 20  $\mu$ A (typical).

The rising threshold voltage of the EN pin is 1.0 V and the falling threshold voltage is 0.9 V. The tolerance of the threshold voltages is  $\pm 30$  mV, which means that the user can use the EN pin to implement precise turn-on and turn-off behavior.

When power is applied to the VIN pin, the toggling of the EN pin does not reset the loaded default register settings.

### 9.3.4 Start-Up

When the voltage on the VIN pin exceeds the positive-going UVLO threshold, the device initializes as follows:

- The device pulls the EN pin low.
- The device enables the internal reference voltage.
- The device reads the state of the VSEL, FSEL, and SYNC\_OUT pins.
- The device loads the default values into the device registers.

When initialization is complete, the device enables I<sup>2</sup>C communication and releases the EN pin. The external circuitry controlling the EN pin now determines the behavior of the device:

- If the EN pin is low, the device is disabled. The user can write to and read from the device registers, but the DC/DC converter does not operate.
- If the EN pin is high, the device is enabled. The user can write to and read from the device registers and, after a short delay, the DC/DC converter starts to ramp up its output.

図 9-7 shows the start-up sequence when the EN pin is pulled up to  $V_{IN}$ .

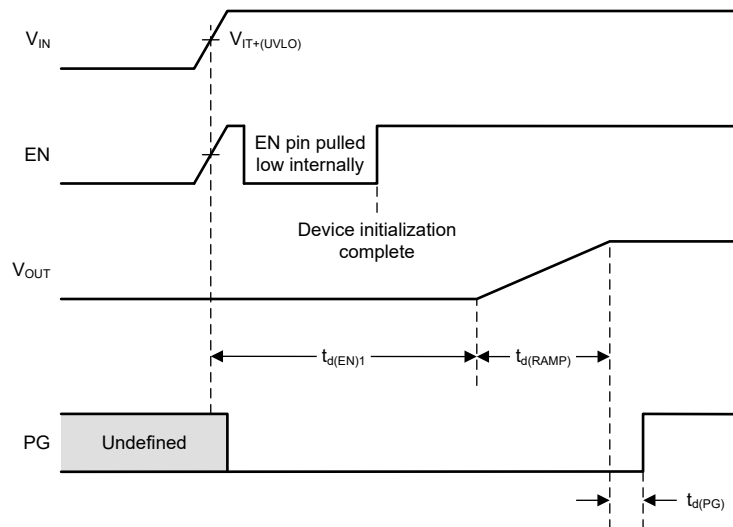


図 9-7. Start-Up Timing When EN is Pulled Up to  $V_{IN}$

図 9-8 shows the start-up sequence when an external signal is connected to the EN pin.

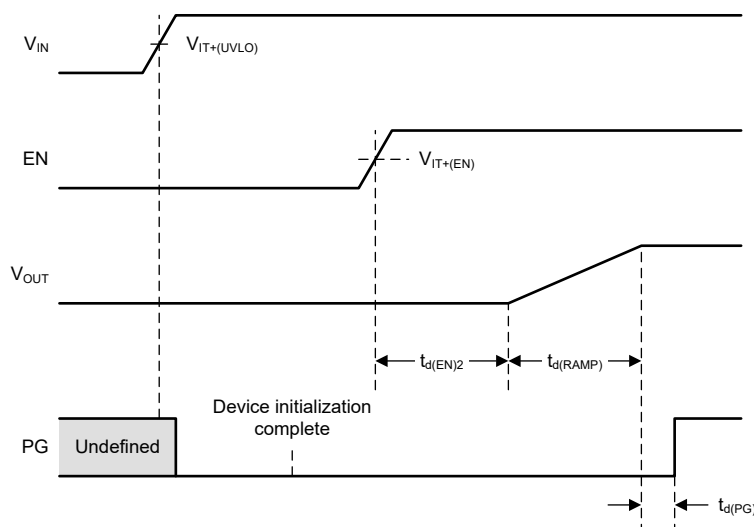


図 9-8. Start-Up Timing When an External Signal is Connected to the EN Pin

The SSTIME[1:0] bits in the CONTROL2 register select the duration of the soft-start ramp:

- $t_{d(RAMP)} = 500 \mu s$
- $t_{d(RAMP)} = 1 \text{ ms}$  (default)
- $t_{d(RAMP)} = 2 \text{ ms}$
- $t_{d(RAMP)} = 4 \text{ ms}$

The device ignores new values until the soft-start sequence is complete if the user programs the following when the device soft-start sequence has already started:

- A new output voltage setpoint ( $V_{OUT}[7:0]$ )
- An output voltage range ( $V_{RANGE}[1:0]$ )
- Soft-start time (SSTIME[1:0]) settings

If the user change the value of VSET[7:0] during soft start, the device first ramps to the value that VSET[7:0] had when the soft-start sequence began. Then, when soft start is complete, the device ramps up or down to the new value.

The device can start up into a prebiased output. In this case, only a portion of the internal voltage ramp is seen externally (see 図 9-9).

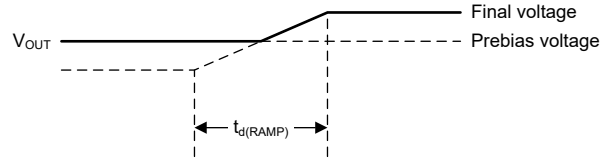


図 9-9. Start-Up into a Prebiased Output

Note that the device *always* operates in DCM during the start-up ramp, regardless of other configuration settings or operating conditions.

### 9.3.5 Switching Frequency Selection

During device initialization, a resistor-to-digital converter in the device determines the state of the FSEL pin and sets the switching frequency of the DC/DC converter according to 表 9-2.

表 9-2. Switching Frequency Options

FSEL Pin 1	Switching Frequency
Short to GND	1.5 MHz
6.2 kΩ to GND	2.25 MHz
47 kΩ to V <sub>IN</sub>	2.5 MHz
Short to V <sub>IN</sub>	3 MHz

- For a reliable voltage setting, ensure there is no stray current path connected to the FSEL pin and that the parasitic capacitance between the FSEL pin and GND is less than 100 pF.

図 9-10 shows a simplified block diagram of the R2D converter used to detect the state of the FSEL pin (an identical circuit detects the state of the VSEL pin – see セクション 9.3.6.2).

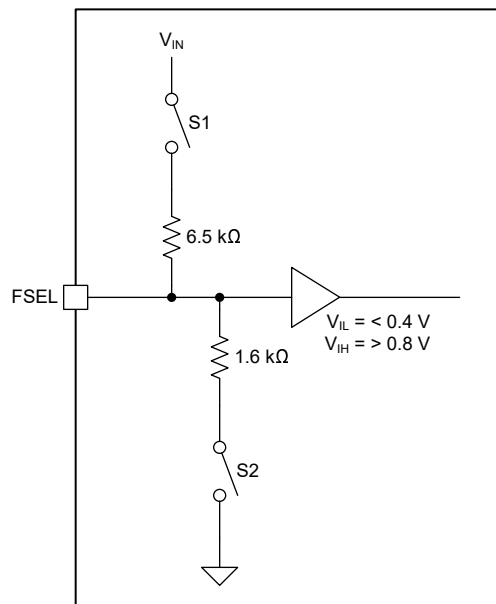


図 9-10. FSEL R2D Converter Functional Block Diagram

Detection of the state of the FSEL pin works as follows:

To detect the most significant bit (MSB), the circuit opens S1 and S2, and the input buffer detects if a high or a low level is connected to the FSEL pin.

To detect the least significant bit (LSB):

- If the MSB was 0, the circuit closes S1. If the input buffer detects a high level, LSB = 1. If the circuit detects a low level, LSB = 0.
- If the MSB was 1, the circuit closes S2. If the input buffer detects a low level, LSB = 0. If the circuit detects a high level, LSB = 1.

### 9.3.6 Output Voltage Setting

#### 9.3.6.1 Output Voltage Range

The device has four different voltage ranges. The VRANGE[1:0] bits in the CONTROL1 register control which range is active (see 表 9-3). The default output voltage range after device initialization is 0.4 V to 1.675 V in 5-mV steps.

**表 9-3. Voltage Ranges**

VRANGE[1:0]	Voltage Range
0b00	0.4 V to 0.71875 V in 1.25-mV steps
0b01	0.4 V to 1.0375 V in 2.5-mV steps
0b10	0.4 V to 1.675 V in 5-mV steps
0b11	0.8 V to 3.35 V in 10-mV steps

Note that every change to the VRANGE[1:0] bits must be followed by a write to the VSET register, even if the value of the VSET[7:0] bits does not change. This sequence is required for the device to start to use the new voltage range.

Also note that the 0.8-V to 3.35-V range uses a 0.8-V reference and the other ranges use a 0.4-V reference. Switching to and from the 0.8-V to 3.35-V range can therefore cause increased output voltage undershoot or overshoot while the device switches its internal reference.

In device variants that do not have I<sup>2</sup>C, the output voltage range is factory-set to 0.4 V to 1.675 V.

#### 9.3.6.2 Output Voltage Setpoint

Together with the selected range, the VSET[7:0] bits in the VSET register control the output voltage setpoint of the device (see 表 9-4).

**表 9-4. Start-Up Voltage Settings**

VRANGE[1:0]	Output Voltage Setpoint
0b00	0.4 V + VSET[7:0] × 1.25 mV
0b01	0.4 V + VSET[7:0] × 2.5 mV
0b10	0.4 V + VSET[7:0] × 5 mV
0b11	0.8 V + VSET[7:0] × 10 mV

During initialization, the device reads the state of the VSEL pin and selects the default output voltage according to 表 9-5. Note that the VSEL pin also selects the I<sup>2</sup>C target address of the device (see 表 9-10).

表 9-5. Default Output Voltage Setpoints

VSEL Pin <sup>(1)</sup>	Device Number	VSET[7:0]	Output Voltage Setpoint
6.2 kΩ to GND	TPS6287x-Q1	0x5A	850 mV
	TPS6287xY0-Q1	0x14	500 mV
	TPS6287xY1-Q1	0x50	800 mV
	TPS6287xY2-Q1	0x64	1800 mV
	TPS6287xY3-Q1	0x52	810 mV
	TPS6287xY4-Q1	0x5A	850 mV
	TPS6287xY5-Q1	0x1E	1100 mV
	TPS6287xY6-Q1	0x28	1200 mV
	TPS6287xN0-Q1	0x14	500 mV
	TPS6287xN1-Q1	0x50	800 mV
	TPS6287xN2-Q1	0x64	1800 mV
	TPS6287xN3-Q1	0x78	1000 mV
Short Circuit to GND	All, Except TPS6287xx2-Q1, TPS6287xY5-Q1, TPS6287xY6-Q1	0x46	750 mV
Short Circuit to GND	TPS6287xx2-Q1, TPS6287xY5-Q1, TPS6287xY6-Q1	0x46	1500 mV
Short Circuit to V <sub>IN</sub>	All, Except TPS6287xx2-Q1, TPS6287xY5-Q1, TPS6287xY6-Q1	0x5F	875 mV
Short Circuit to V <sub>IN</sub>	TPS6287xx2-Q1, TPS6287xY5-Q1, TPS6287xY6-Q1	0x5F	1750 mV
47 kΩ to V <sub>IN</sub>	TPS6287x-Q1	0x78	1000 mV
	TPS6287xY0-Q1	0x82	1050 mV
	TPS6287xY1-Q1	0x50	800 mV
	TPS6287xY2-Q1	0xFA	3300 mV
	TPS6287xY3-Q1	0x78	1000 mV
	TPS6287xY4-Q1	0x5A	850 mV
	TPS6287xY5-Q1	0xFA	3300 mV
	TPS6287xY6-Q1	0xAA	2500 mV
	TPS6287xN0-Q1	0x82	1050 mV
	TPS6287xN1-Q1	0x58	840 mV
	TPS6287xN2-Q1	0xFA	3300 mV
	TPS6287xN3-Q1	0x8C	1100 mV

(1) For a reliable voltage setting, ensure there is no stray current path connected to the VSEL pin and that the parasitic capacitance between the VSEL pin and GND is less than 100 pF.

If the user programs new output voltage setpoint (VOUT[7:0]), output voltage range (VRANGE[1:0]), or soft-start time (SSTIME[1:0]) settings when the device has already begun its soft-start sequence, the device ignores the new values until the soft-start sequence is complete. If the user changes the value of VSET[7:0] during soft start, the device first ramps to the value that VSET[7:0] had when the soft-start sequence began. Then, when soft start is complete, ramps up or down to the new value.

If the user changes VOUT[7:0], VRAMP[1:0], or SSTIME[1:0] while EN is low, the device uses the new values the next time the user enables it.

During start-up, the output voltage ramps up to the target value set by the VSEL pin before ramping up or down to any new value programmed to the device over the I<sup>2</sup>C interface.

### 9.3.6.3 Non-Default Output Voltage Setpoint

If none of the default voltage range or voltage setpoint combinations are suitable for the application, the user can change these device settings through I<sup>2</sup>C before the user enables the device. Then, when the user pulls the EN pin high, the device starts up with the desired start-up voltage.

Note that if the user changes the device settings through I<sup>2</sup>C *while the device is ramping*, the device ignores the changes until the ramp is complete.

### 9.3.6.4 Dynamic Voltage Scaling

If the user changes the output voltage setpoint while the DC/DC converter is operating, the device ramps up or down to the new voltage setting in a controlled way.

The VRAMP[1:0] bits in the CONTROL1 register sets the slew rate when the device ramps from one voltage to another during DVS (see [表 9-6](#)).

**表 9-6. Dynamic Voltage Scaling Slew Rate**

VRAMP[1:0]	DVS Slew Rate
0b00	10 mV/μs (0.5 μs/step)
0b01	5 mV/μs (1 μs/step)
0b10	1.25 mV/μs (5 μs/step)
0b11	0.5 mV/μs (10 μs/step)

Note that ramping the output to a higher voltage requires additional output current, so that during DVS, the converter must generate a total output current given by:

$$I_{OUT} = I_{OUT(DC)} + C_{OUT} \frac{dV_{OUT}}{dt} \quad (2)$$

where

- $I_{OUT}$  is the total current the converter must generate while ramping to a higher voltage.
- $I_{OUT(DC)}$  is the DC load current.
- $C_{OUT}$  is the total output capacitance.
- $dV_{OUT}/dt$  is the slew rate of the output voltage (programmable in the range 0.5 mV/μs to 10 mV/μs).

For correct operation, ensure that the total output current during DVS does not exceed the current limit of the device.

### 9.3.7 Compensation (COMP)

The COMP pin is the connection point for an external compensation network. A series-connected resistor and capacitor to GOSNS is sufficient for typical applications. The series-connected resistor also provides enough scope to optimize the loop response for a wide range of operating conditions.

When using multiple devices in a stacked configuration, all devices share a common compensation network, and the COMP pin makes sure there is equal current sharing between them (see [セクション 9.3.17](#)).

### 9.3.8 Mode Selection and Clock Synchronization (MODE/SYNC)

A high level on the MODE/SYNC pin selects forced PWM operation. A low level on the MODE/SYNC pin selects power save operation, in which, the device automatically transitions between PWM and PFM, according to the load conditions.



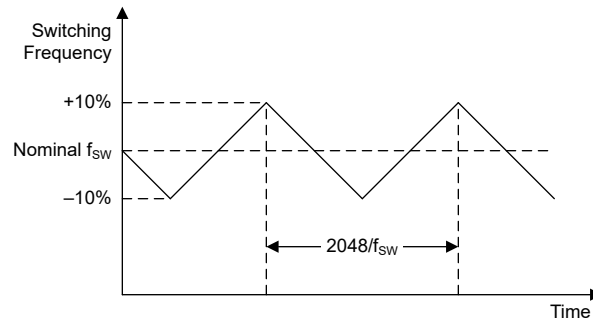
If the user applies a valid clock signal to the MODE/SYNC pin, the device synchronizes its switching cycles to the external clock and automatically selects forced PWM operation.

The MODE/SYNC pin is logically ORed with the FPWMEN bit in the CONTROL1 register (see [表 9-1](#)).

When multiple devices are used together in a stacked configuration, the MODE/SYNC pin of the secondary devices is the input for the clock signal (see [セクション 9.3.17](#)).

### 9.3.9 Spread Spectrum Clocking (SSC)

The device has a spread spectrum clocking function that can reduce electromagnetic interference (EMI). When the SSC function is active, the device modulates the switching frequency to approximately  $\pm 10\%$  the nominal value. The frequency modulation has a triangular characteristic (see [図 9-11](#)).



**図 9-11. Spread Spectrum Clocking Behavior**

To use the SSC function, make sure that:

- SSCEN = 1 in the CONTROL1 register.
- The device is not synchronized to an external clock.

TI recommends to use FPWM operation when using SSC, but SSC is available with PSM operation. To disable the SSC function, make sure that SSCEN = 0 in the CONTROL1 register.

To use the SSC function with multiple devices in a stacked configuration, ensure that the primary converter runs from its internal oscillator and synchronize all secondary converters to the primary clock (see [図 9-14](#)).

### 9.3.10 Output Discharge

The device has an output discharge function that ensures a defined ramp down of the output voltage when the device is disabled and keeps the output voltage close to 0 V while the device is off. The output discharge function is enabled when DISCHEN = 1 in the CONTROL1 register. The output discharge function is enabled by default.

If enabled, the device discharges the output under the following conditions:

- A low level is applied to the EN pin.
- SWEN = 0 in the CONTROL1 register.
- A thermal shutdown event occurs.
- A UVLO event occurs.
- An OVLO event occurs.

The output discharge function is not available until the user has enabled the device at least once after power up. During power down, the device continues to discharge the output for as long as the internal supply voltage is greater than approximately 1.8 V.

### 9.3.11 Undervoltage Lockout (UVLO)

The device has an undervoltage lockout function that disables the device if the supply voltage is too low for correct operation. The negative-going threshold of the UVLO function is 2.5 V (typical). If the supply voltage

decreases below this value, the device stops switching and, if DISCHEN = 1 in the CONTROL1 register, turns on the output discharge.

### 9.3.12 Overvoltage Lockout (OVLO)

The device has an overvoltage lockout function that disables the DC/DC converter if the supply voltage is too high for correct operation. The positive-going threshold of the OVLO function is 6.3 V (typical). If the supply voltage increases above this value, the device stops switching and, if DISCHEN = 1 in the CONTROL1 register, turns on the output discharge.

The device automatically starts switching again – it begins a new soft-start sequence – when the supply voltage falls below 6.2 V (typical).

### 9.3.13 Overcurrent Protection

#### 9.3.13.1 Cycle-by-Cycle Current Limiting

If the peak inductor current increases above the high-side current limit threshold, the device turns off the high-side switch and turns on the low-side switch to ramp down the inductor current. The device only turns on the high-side switch again if the inductor current has decreased below the low-side current limit threshold.

Note that because of the propagation delay of the current limit comparator, the current limit threshold in practice can be greater than the DC value specified in the [Electrical Characteristics](#). The current limit in practice is given by:

$$I_L = I_{LIMH} + \left( \frac{V_{IN} - V_{OUT}}{L} \right) t_{pd} \quad (3)$$

where:

- $I_L$  is the inductor current.
- $I_{LIMH}$  is the high-side current limit threshold measured at DC.
- $V_{IN}$  is the input voltage.
- $V_{OUT}$  is the output voltage.
- $L$  is the effective inductance at the peak current level.
- $t_{pd}$  is the propagation delay of the current limit comparator (typically 50 ns).

#### 9.3.13.2 Hiccup Mode

To enable hiccup operation, ensure that HICCUPEN = 1 in the CONTROL1 register.

If hiccup operation is enabled and the high-side switch current exceeds the current limit threshold on 32 consecutive switching cycles, the device:

- Stops switching for 128  $\mu$ s, after which it automatically starts switching again (it starts a new soft-start sequence)
- Sets the HICCUP bit in the STATUS register
- Pulls the PG pin low. The PG pin stays low until the overload condition goes away and the device can start up correctly and regulate the output voltage. Note that power-good function has a deglitch circuit, which delays the rising edge of the power-good signal by 40  $\mu$ s (typical).

Hiccup operation continues in a repeating sequence of 32 cycles in current limit, followed by a pause of 128  $\mu$ s, followed by a soft-start attempt for as long as the output overload condition exists.

The device clears the HICCUP bit if the user reads the STATUS register when the overload condition has been removed.

#### 9.3.13.3 Current Limit Mode

To enable current limit mode, ensure that HICCUPEN = 0 in the CONTROL1 register.

When current limit operation is enabled, the device limits the high-side switch current cycle-by-cycle for as long as the overload condition exists. If the device limits the high-side switch current for four or more consecutive switching cycles, the device sets ILIM = 1 in the STATUS register.

The device clears the ILIM bit if the user reads the STATUS register when the overload condition no longer exists.

### 9.3.14 Power Good (PG)

The power good (PG) pin is bidirectional and has two functions:

- In a standalone configuration and in the primary device of a stacked configuration, the PG pin is an open-drain output that indicates the status of the converter or stack.
- In a secondary device of a stacked configuration, the PG pin is an input that indicates when the soft-start sequence is complete and all converters in the stack can change from DCM switching to CCM switching.

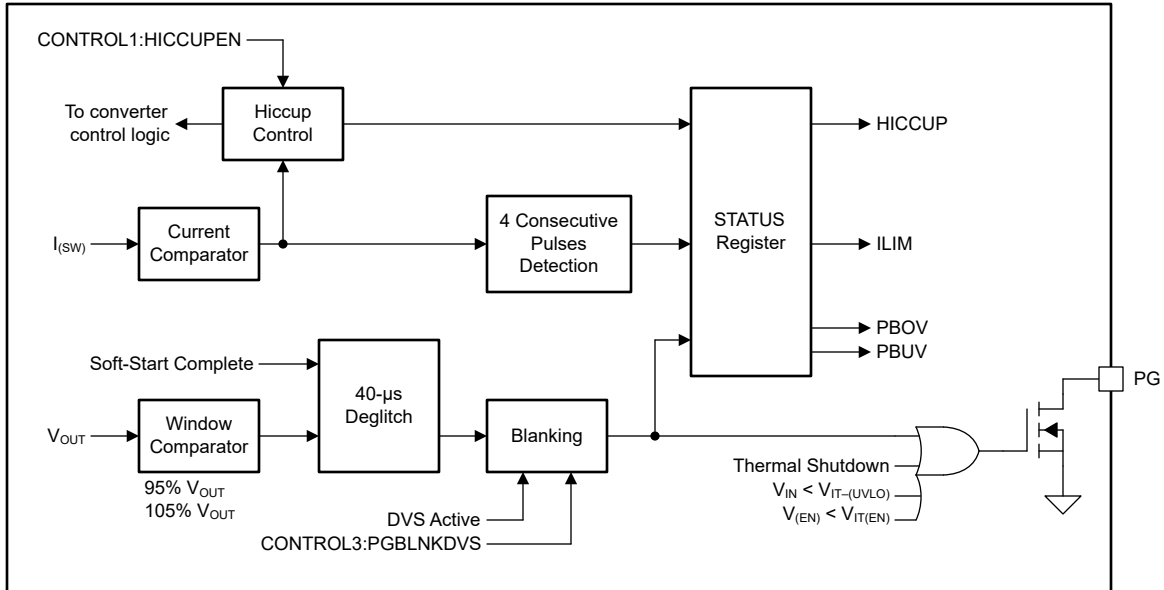
#### 9.3.14.1 Standalone or Primary Device Behavior

The primary purpose of the PG pin is to indicate if the output voltage is in regulation, but it also indicates if the device is in thermal shutdown or disabled. 表 9-7 summarizes the behavior of the PG pin in a standalone or primary device.

表 9-7. Power-Good Function Table

V <sub>IN</sub>	EN	V <sub>OUT</sub>	Soft Start	PGBLNKDVS	T <sub>J</sub>	PG
2 V > V <sub>IN</sub>	X	X	X	X	X	Undefined
V <sub>IT(UVLO)</sub> ≥ V <sub>IN</sub> ≥ 2 V	X	X	X	X	X	Low
V <sub>IN</sub> > V <sub>IT(UVLO)</sub>	L	X	X	X	X	Low
	H	X	Active	X	X	Low
		V <sub>OUT</sub> > V <sub>T(PGOV)</sub> or < V <sub>T(PGUV)</sub> > V <sub>OUT</sub>	Inactive	0	X	low
		V <sub>T(PGOV)</sub> > V <sub>OUT</sub> > V <sub>T(PGUV)</sub>		1 (and DVS is active)	T <sub>J</sub> < T <sub>SD</sub>	Hi-Z
		X		X	T <sub>J</sub> < T <sub>SD</sub>	Hi-Z
X	X	X	X	T <sub>J</sub> > T <sub>SD</sub>	Low	

図 9-12 shows a functional block diagram of the power-good function in a standalone or primary device. A window comparator monitors the output voltage, and the output of the comparator goes high if the output voltage is either less than 95% (typical) or greater than 105% (typical) of the nominal output voltage. The output of the window comparator is deglitched – the typical deglitch time is 40 μs – and then used to drive the open-drain PG pin.



**図 9-12. Power-Good Functional Block Diagram (Standalone or Primary Device)**

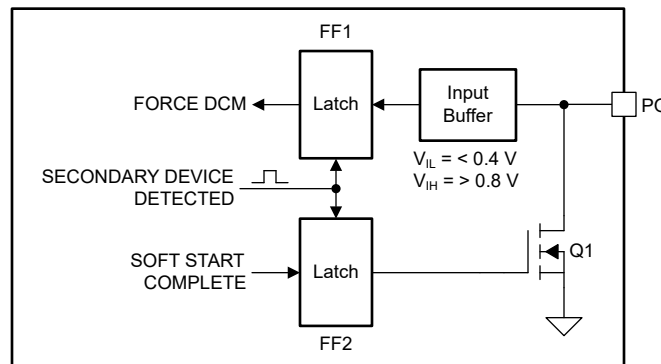
During DVS activity, when the DC/DC converter transitions from one output voltage setting to another, the output voltage can temporarily exceed the limits of the window comparator and pull the PG pin low. The device has a feature to disable this behavior. If PGBLNKDVS = 1 in the CONTROL3 register, the device ignores the output of the power-good window comparator while DVS is active.

Note that the PG pin is always low, regardless of the output of the window comparator, when:

- The device is in thermal shutdown.
- The device is disabled.
- The device is in undervoltage lockout.
- The device is in soft start.

### 9.3.14.2 Secondary Device Behavior

Figure 9-13 shows a functional block diagram of the power-good function in a secondary device. During initialization, the device presets FF1 and FF2, which pulls down the PG pin and forces the device to operate in DCM. When the device completes its soft start, it resets FF2, which turns off Q1. However, in a stacked configuration, all devices share the same PG signal, and therefore the PG pin stays low until *all* devices in the stack have completed their soft start. When that happens, FF1 is reset and the converters operate in CCM.



**図 9-13. Power-Good Functional Block Diagram (Secondary Device)**

### 9.3.15 Remote Sense

The device has two pins, VOSNS and GOSNS, to remotely sense the output voltage. Remote sensing lets the converter sense the output voltage directly at the point-of-load and increases the accuracy of the output voltage regulation.

### 9.3.16 Thermal Warning and Shutdown

The device has a two-level overtemperature detection function.

If the junction temperature rises above the thermal warning threshold of 150°C (typical), the device sets the TWARN bit in the STATUS register. The device clears the TWARN bit if the user reads the STATUS register when the junction temperature is below the TWARN threshold of 130°C (typical).

If the junction temperature rises above the thermal shutdown threshold of 170°C (typical), the device:

- Stops switching
- Pulls down the EN pin (if SINGLE = 0 in the CONTROL3 register)
- Enables the output discharge (if DISCHEN = 1 in the CONTROL1 register)
- Sets the TSHUT bit in the STATUS register
- Pulls the PG pin low

If the junction temperature falls below the thermal shutdown threshold of 150°C (typical), the device:

- Starts switching again, starting with a new soft-start sequence
- Sets the EN pin to high impedance
- Sets the PG pin to high-impedance

The device clears the TSHUT bit if the user reads the STATUS register when the junction temperature is below the TSHUT threshold of 150°C (typical).

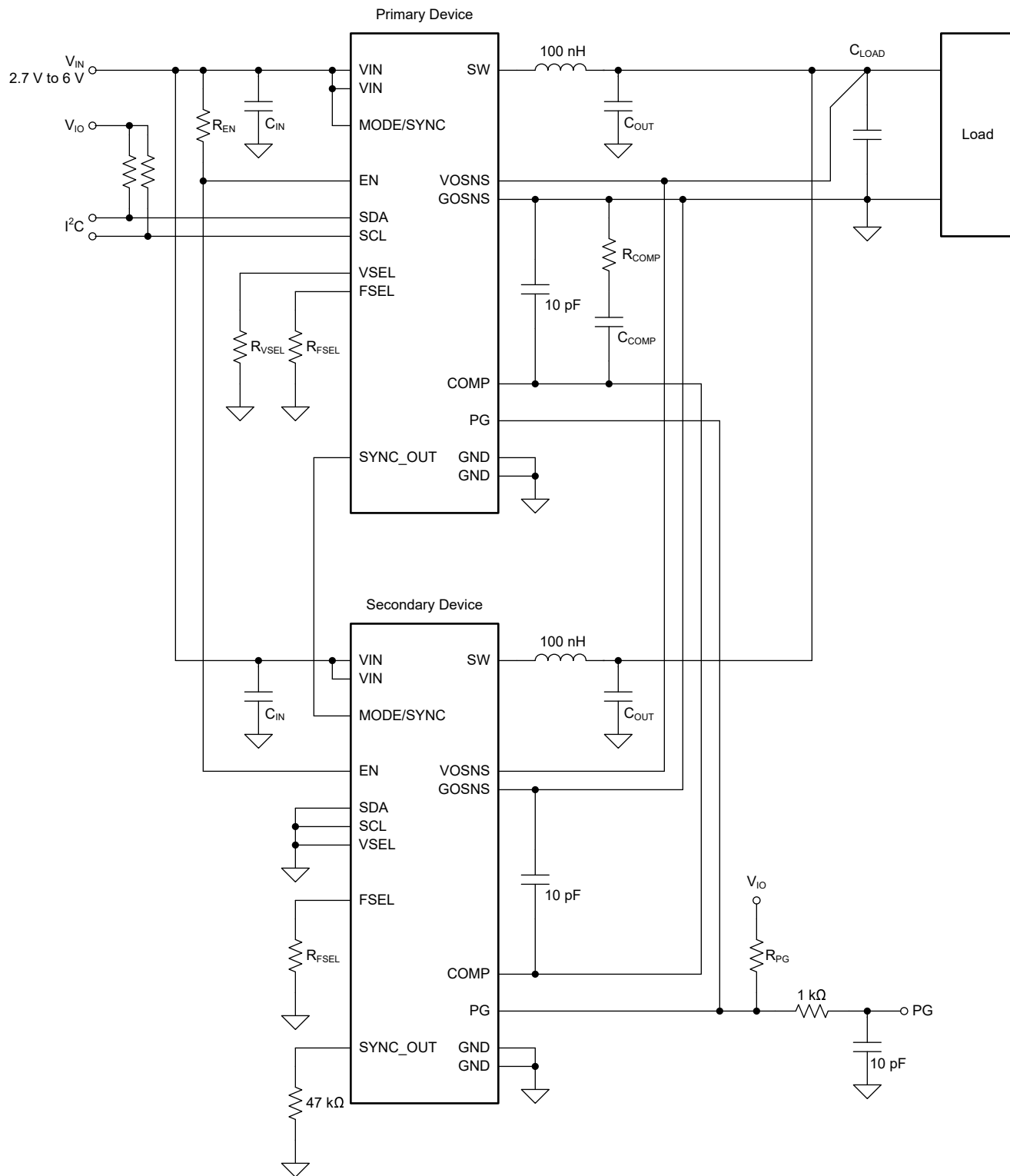
In a stacked configuration, in which all devices share a common enable signal, a thermal shutdown condition in one device disables the entire stack. When the hot device cools down, the whole stack automatically starts switching again.

### 9.3.17 Stacked Operation

The user can connect multiple devices in parallel in what is known as a "stack"; for example, to increase output current capability or reduce device junction temperature. A stack comprises one *primary* device and one or more *secondary* devices. During initialization, each device monitors its SYNC\_OUT pin to determine if must operate as a primary device or a secondary device:

- If there is a 47-kΩ resistor between the SYNC\_OUT pin and ground, the device operates as a secondary device.
- If the SYNC\_OUT pin is high impedance, the device operates as a primary device.

 9-14 shows the recommended interconnections in a stack of two TPS6287x-Q1 devices.



☒ 9-14. Two TPS6287x-Q1 Devices in a Stacked Configuration

The key points to note are:

- All the devices in the stack share a common enable signal, which must be pulled up with a resistance of at least 15 kΩ.

- All the devices in the stack share a common power-good signal.
- All the devices in the stack share a common compensation signal.
- All secondary devices must connect a 47-kΩ resistor between the SYNC\_OUT pin and ground.
- The remote sense pins (VOSNS and GOSNS) of each device must be connected (do not leave these pins floating).
- Each device must be configured for the same switching frequency.
- The primary device must be configured for forced PWM operation (secondary devices are automatically configured for forced PWM operation).
- A stacked configuration can support synchronization to an external clock or spread-spectrum clocking.
- Only the VSEL pin of the primary device is used to set the default output voltage. The VSEL pin of secondary devices is not used and must be connected to ground.
- The SDA and SCL pins of secondary devices are not used and must be connected to ground.
- A stacked configuration uses a daisy-chained clocking signal, in which each device switches with a phase offset of approximately 140° relative to the adjacent devices in the daisy-chain. To daisy-chain the clocking signal, connect the SYNC\_OUT pin of the primary device to the MODE/SYNC pin of the first secondary device. Connect the SYNC\_OUT pin of the first secondary device to the MODE/SYNC pin of the second secondary device. Continue this connection scheme for all devices in the stack, to daisy-chain them together.
- Hiccup overcurrent protection must not be used in a stacked configuration.

In a stacked configuration, the common enable signal also acts as a SYSTEM\_READY signal (see [セクション 9.3.3](#)). Each device in the stack can pull its EN pin low during device start-up or when a fault occurs. Thus, the stack is only enabled when all devices have completed their start-up sequence and are fault-free. A fault in any one device disables the whole stack for as long as the fault condition exists.

During start-up, the primary converter pulls the COMP pin low for as long as the enable signal (SYSTEM\_READY) is low. When the enable signal goes high, the primary device actively controls the COMP pin and all converters in the stack follow the COMP voltage. During start-up, each device in the stack pulls its PG pin low while it initializes. When initialization is complete, each secondary device in the stack sets its PG pin to a high impedance and the primary device alone controls the state of the PG signal. The PG pin goes high when the stack has completed its start-up ramp and the output voltage is within specification. The secondary converters in the stack detect the rising edge of the power-good signal and switch from DCM operation to CCM operation. After the stack has successfully started up, the primary device controls the power-good signal in the normal way. In a stacked configuration, there are some faults that only affect individual devices, and other faults that affect all devices. For example, if one device enters current limit, only that device is affected. But a thermal shutdown or undervoltage lockout event in one device disables all devices through the shared enable (SYSTEM\_READY) signal.

### Functionality During Stacked Operation

Some device features are not available during stacked operation, or are only available in the primary converter. [表 9-8](#) summarizes the available functionality during stacked operation.

**表 9-8. Functionality During Stacked Operation**

Function	Primary Device	Secondary Device	Remark
UVLO	Yes	Yes	Common enable signal
OVLO	Yes	Yes	Common enable signal
OCP – Current Limit	Yes	Yes	Individual
OCP – Hiccup OCP	No	No	Do not use during stacked operation.
Thermal Shutdown	Yes	Yes	Common enable signal
Power-Good (Window Comparator)	Yes	No	Primary device only
I <sup>2</sup> C Interface	Yes	No	Primary device only
DVS	Through I <sup>2</sup> C	No	Voltage loop controlled by primary device only

**表 9-8. Functionality During Stacked Operation (続き)**

Function	Primary Device	Secondary Device	Remark
SSC	Through I <sup>2</sup> C	No	Daisy-chained from primary device to secondary devices
SYNC	Yes	Yes	Synchronization clock applied to primary device
Precise Enable	No	No	Only binary enable
Output Discharge	Yes	Yes	Always enabled in secondary devices

### Fault Handling During Stacked Operation

In a stacked configuration, there are some faults that only affect individual devices and other faults that affect all devices. For example, if one device enters current limit, only that device is affected. A thermal shutdown or undervoltage lockout event in one device disables all devices through the shared enable (SYSTEM\_READY) signal. 表 9-9 summarizes the fault handling of the TPS6287x-Q1 devices during stacked operation.

**表 9-9. Fault Handling During Stacked Operation**

Fault Condition	Device Response	System Response
UVLO	Enable signal pulled low	New soft start
OVLO		
Thermal shutdown		
Current limit	Enable signal remains high	Error amplifier clamped

## 9.4 Device Functional Modes

### 9.4.1 Power-On Reset

The device operates in POR mode when the supply voltage is less than the POR threshold, 1.4 V (typical).

In POR mode, no functions are available and the content of the device registers is not valid.

The device leaves POR mode and enters UVLO mode when the supply voltage increases above the POR threshold.

### 9.4.2 Undervoltage Lockout

The device operates in UVLO mode when the supply voltage is between the POR and UVLO thresholds.

If the device enters UVLO mode from POR mode, no functions are available. If the device enters UVLO mode from standby mode, the output discharge function is available. The content of the device registers is valid in UVLO mode.

The device leaves UVLO mode and enters POR mode when the supply voltage decreases below the POR threshold. The device leaves UVLO mode and enters standby mode when the supply voltage increases above the UVLO threshold.

### 9.4.3 Standby

The device operates in standby mode when the supply voltage is greater than the UVLO threshold (and the device has completed its initialization) and any of the following conditions is true:

- A low level is applied to the EN pin.
- SWEN = 0 in the CONTROL1 register.
- The device junction temperature is greater than the thermal shutdown threshold.
- The supply voltage is greater than the OVLO threshold.

The device initializes for 400 μs (typical) after the supply voltage increases above the UVLO threshold voltage following a device power-on reset. If the supply voltage decreases below the UVLO threshold but not below the



POR threshold, the device does not reinitialize when the supply voltage increases again. During initialization, the device reads the state of the FSEL, VSEL, and SYNC\_OUT pins.

The following functions are available in standby mode:

- I<sup>2</sup>C interface
- Output discharge
- Power good

The device leaves standby mode and enters UVLO mode when the supply voltage decreases below the UVLO threshold. The device leaves standby mode and enters on mode when all of the following conditions are true:

- A high-level is applied to the EN pin.
- SWEN = 1 in the CONTROL1 register.
- The device junction temperature is below the thermal shutdown threshold.
- The supply voltage is below the OVLO threshold.

#### 9.4.4 On

The device operates in on mode when the supply voltage is greater than the UVLO threshold and all of the following conditions are true:

- A high-level is applied to the EN pin.
- SWEN = 1 in the CONTROL1 register.
- The device junction temperature is below the thermal shutdown threshold.
- The supply voltage is below the OVLO threshold.

All functions are available in on mode.

The device leaves on mode and enters UVLO mode when the supply voltage decreases below the UVLO threshold. The device leaves on mode and enters standby mode when any of the following conditions is true:

- A low level is applied to the EN pin.
- SWEN = 0 in the CONTROL1 register.
- The device junction temperature is greater than the thermal shutdown threshold.
- The supply voltage is greater than the OVLO threshold.

## 9.5 Programming

### 9.5.1 Serial Interface Description

I<sup>2</sup>C is a 2-wire serial interface developed by Philips Semiconductor, now NXP Semiconductors (see I<sup>2</sup>C-Bus Specification and User Manual, Revision 6, 4 April 2014). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is *idle*, both SDA and SCL lines are pulled high. All I<sup>2</sup>C-compatible devices connect to the I<sup>2</sup>C bus through open-drain I/O pins, SDA and SCL. A *controller*, usually a microcontroller or a digital signal processor, controls the bus. The controller is responsible for generating the SCL signal and device addresses. The controller also generates specific conditions that indicate the START and STOP of data transfer. A *target* receives data, transmits data, or both on the bus under control of the controller.

The TPS6287x-Q1 device operates as a target and supports the following data transfer *modes*, as defined in the I<sup>2</sup>C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and fast mode plus (1 Mbps). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents remain intact as long as the input voltage remains above 1.4 V.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The device supports 7-bit addressing; general call addresses are not supported.

The state of the VSEL pin during power up defines the I<sup>2</sup>C target address of the device (see 表 9-10). Note that the VSEL pin also sets the default start-up voltage of the device (see 表 9-4).

**表 9-10. I<sup>2</sup>C Interface Target Address Selection**

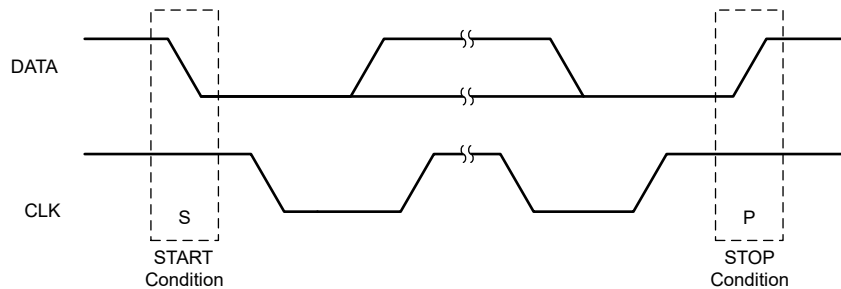
VSEL Pin	I <sup>2</sup> C Target Address <sup>(1)</sup>
6.2 kΩ to GND	0x40 or 0x30 or 0x20 or 0x10
Short Circuit to GND	0x41 or 0x31 or 0x21 or 0x11
Short Circuit to V <sub>IN</sub>	0x42 or 0x32 or 0x22 or 0x12
47 kΩ to V <sub>IN</sub>	0x43 or 0x33 or 0x23 or 13

(1) Available I<sup>2</sup>C address. This parameter is Device number dependent. Refer to the Device option Table in [セクション 6](#)

TI recommends that the I<sup>2</sup>C controller initiates a STOP condition on the I<sup>2</sup>C bus after the initial power up of SDA and SCL pullup voltages to ensure reset of the I<sup>2</sup>C engine.

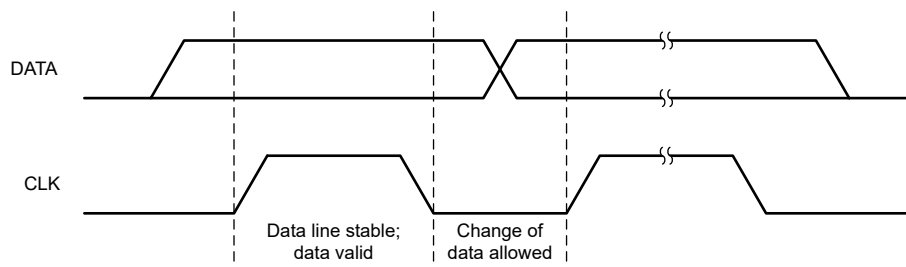
### 9.5.2 Standard, Fast, Fast Mode Plus Protocol

The controller initiates a data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, as shown in [図 9-15](#). All I<sup>2</sup>C-compatible devices must recognize a start condition.



**図 9-15. START and STOP Conditions**

The controller then generates the SCL pulses, and transmits the 7-bit address and the read and write direction bit R/W on the SDA line. During all transmissions, the controller makes sure that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse (see [図 9-16](#)). All devices recognize the address sent by the controller and compare the address to their internal fixed addresses. Only the target with a matching address generates an acknowledge (see [図 9-17](#)) by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the controller knows that a communication link with a target has been established.

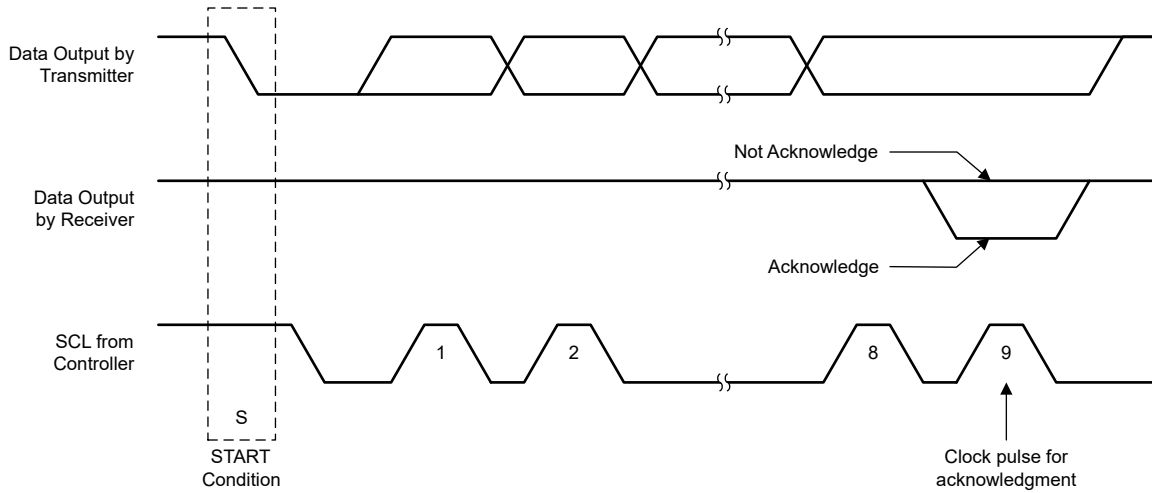


**図 9-16. Bit Transfer on the Serial Interface**

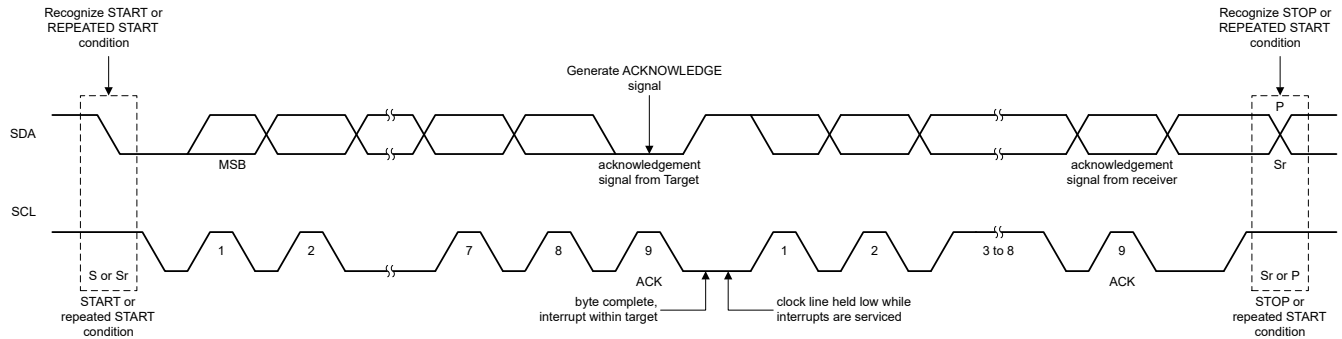
The controller generates further SCL cycles to either transmit data to the target (R/W bit 0) or receive data from the target (R/W bit 1). In either case, the target must acknowledge the data sent by the controller. So an acknowledge signal can either be generated by the controller or by the target, depending on which one is the receiver. 9-bit valid data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

To signal the end of the data transfer, the controller generates a stop condition by pulling the SDA line from low to high while the SCL line is high (see 9-15). This stop condition releases the bus and stops the communication link with the addressed target. All I<sup>2</sup>C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address.

Attempting to read data from register addresses not listed in this section will result in 0x00 being read out.



9-17. Acknowledge on the I<sup>2</sup>C Bus



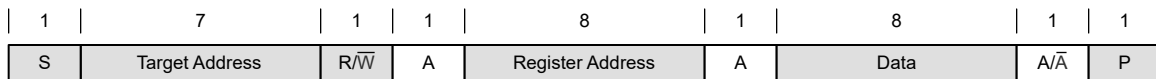
9-18. Bus Protocol

### 9.5.3 I<sup>2</sup>C Update Sequence

The following are required for a single update:

- A start condition
- A valid I<sup>2</sup>C address
- A register address byte
- A data byte

After the receipt of each byte, the receiving device acknowledges by pulling the SDA line low during the high period of a single clock pulse. A valid I<sup>2</sup>C address selects the target. The target performs an update on the falling edge of the acknowledge signal that follows the LSB byte.

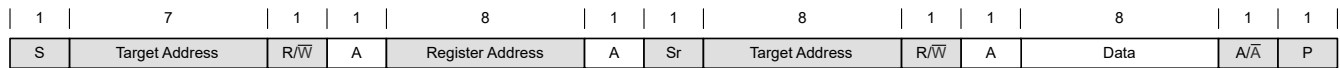


"0" Write

- From Controller to Target
- From Target to Controller

A = Acknowledge (SDA low)  
 A̅ = Not acknowledge (SDA high)  
 S = START condition  
 Sr = REPEATED START condition  
 P = STOP condition

**9-19. "Write" Data Transfer Format in Standard, Fast, Fast Plus Modes**



"0" Write

"1" Read

- From Controller to Target
- From Target to Controller

A = Acknowledge (SDA low)  
 A̅ = Not acknowledge (SDA high)  
 S = START condition  
 Sr = REPEATED START condition  
 P = STOP condition

**9-20. "Read" Data Transfer Format in Standard, Fast, Fast Plus Modes**

**9.5.4 I<sup>2</sup>C Register Reset**

The I<sup>2</sup>C registers can be reset by:

- Pulling the input voltage below 1.4 V (typical).
- Setting the RESET bit in the CONTROL register. When RESET = 1, all registers are reset to their default values and a new start-up begins immediately. After  $t_{d(EN)}$ , you can program the I<sup>2</sup>C registers again.

## 9.6 Register Map

表 9-11 lists the device registers. Consider all register offset addresses not listed in 表 9-11 as reserved locations. Do not modify the register contents.

**表 9-11. Device Registers**

Address	Acronym	Register Name	Section
0h	VSET	Output Voltage Setpoint	<a href="#">Go</a>
1h	CONTROL1	Control 1	<a href="#">Go</a>
2h	CONTROL2	Control 2	<a href="#">Go</a>
3h	CONTROL3	Control 3	<a href="#">Go</a>
4h	STATUS	Status	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. 表 9-12 shows the codes that are used for access types in this section.

**表 9-12. Device Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
- n		Value after reset or the default value

### 9.6.1 VSET Register (Address = 0h) [Reset = X]

VSET is shown in [図 9-21](#) and described in [表 9-13](#).

Return to the [Summary Table](#).

This register controls the output voltage setpoint.

**図 9-21. VSET Register**

7	6	5	4	3	2	1	0
VSET							
R/W-X							

**表 9-13. VSET Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-0	VSET	R/W	X	Output voltage setpoint (see the range-setting bits in the CONTROL2 register.) Range 1: Output voltage setpoint = 0.4 V + VSET[7:0] × 1.25 mV Range 2: Output voltage setpoint = 0.4 V + VSET[7:0] × 2.5 mV Range 3: Output voltage setpoint = 0.4 V + VSET[7:0] × 5 mV Range 4: Output voltage setpoint = 0.8 V + VSET[7:0] × 10 mV The state of the VSEL pin during power up determines the reset value.

### 9.6.2 CONTROL1 Register (Address = 1h) [Reset = 2Ah]

CONTROL1 is shown in [図 9-22](#) and described in [表 9-14](#).

Return to the [Summary Table](#).

This register controls various device configuration options.

**図 9-22. CONTROL1 Register**

7	6	5	4	3	2	1	0
RESET	SSCEN	SWEN	FPWMEN	DISCHEN	HICCUPEN	VRAMP	
R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-1b	R/W-0b	R/W-10b	

**表 9-14. CONTROL1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7	RESET	R/W	0b	Reset device 0b = No effect 1b = Resets all registers to their default values Reading this bit always returns 0.
6	SSCEN	R/W	0b	Spread spectrum clocking enable 0b = SSC operation disabled 1b = SSC operation enabled
5	SWEN	R/W	1b	Software enable 0b = Switching disabled (register values retained) 1b = Switching enabled (without the enable delay)
4	FPWMEN	R/W	0b	Forced PWM enable 0b = Power-save operation enabled 1b = Forced-PWM operation enabled This bit is logically ORed with the MODE/SYNC pin. If a high level or a synchronization clock is applied to the MODE/SYNC pin, the device operates in forced-PWM, regardless of the state of this bit.
3	DISCHEN	R/W	1b	Output discharge enable 0b = Output discharge disabled 1b = Output discharge enabled
2	HICCUPEN	R/W	0b	Hiccup operation enable 0b = Hiccup operation disabled 1b = Hiccup operation enabled. Do not enable hiccup operation during stacked operation.
1-0	VRAMP	R/W	10b	Output voltage ramp speed when changing from one output voltage setting to another 00b = 10 mV/μs 01b = 5 mV/μs 10b = 1.25 mV/μs 11b = 0.5 mV/μs

### 9.6.3 CONTROL2 Register (Address = 2h) [Reset = 9h]

CONTROL2 is shown in [図 9-23](#) and described in [表 9-15](#).

Return to the [Summary Table](#).

This register controls various device configuration options.

**図 9-23. CONTROL2 Register**

7	6	5	4	3	2	1	0
RESERVED				VRANGE		SSTIME	
R-0000b				R/W-10b		R/W-01b	

**表 9-15. CONTROL2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0000b	Reserved for future use. For compatibility with future device variants, program these bits to 0.
3-2	VRANGE	R/W	10b	Output voltage range 00b = 0.4 V to 0.71875 V in 1.25-mV steps 01b = 0.4 V to 1.0375 V in 2.5-mV steps 10b = 0.4 V to 1.675 V in 5-mV steps 11b = 0.8 V to 3.35 V in 10-mV steps
1-0	SSTIME	R/W	01b	Soft-start ramp time 00b = 0.5 ms 01b = 1 ms 10b = 2 ms 11b = 4 ms



### 9.6.4 CONTROL3 Register (Address = 3h) [Reset = 0h]

CONTROL3 is shown in [図 9-24](#) and described in [表 9-16](#).

Return to the [Summary Table](#).

This register controls various device configuration options.

**図 9-24. CONTROL3 Register**

7	6	5	4	3	2	1	0
RESERVED						SINGLE	PGBLNKDVS
R-000000b						R/W-0b	R/W-0b

**表 9-16. CONTROL3 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	000000b	Reserved for future use. For compatibility with future device variants, program these bits to 0.
1	SINGLE	R/W	0b	Single operation. This bit controls the internal EN pulldown and SYNCOUT functions. 0b = EN pin pulldown and SYNCOUT enabled 1b = EN pin pulldown and SYNCOUT disabled. Do not use during stacked operation.
0	PGBLNKDVS	R/W	0b	Power-good blanking during DVS 0b = PG pin reflects the output of the window comparator. 1b = PG pin is high impedance during DVS.

### 9.6.5 STATUS Register (Address = 4h) [Reset = 2h]

STATUS is shown in [図 9-25](#) and described in [表 9-17](#).

Return to the [Summary Table](#).

This register returns the device status flags.

**図 9-25. STATUS Register**

7	6	5	4	3	2	1	0
RESERVED		HICCUP	ILIM	TWARN	TSHUT	PBUV	PBOV
R-00b		R-0b	R-0b	R-0b	R-0b	R-1b	R-0b

**表 9-17. STATUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	00b	Reserved for future use. For compatibility with future device variants, ignore these bits.
5	HICCUP	R	0b	Hiccup. This bit reports whether a hiccup event occurred since the last time the STATUS register was read. 0b = No hiccup event occurred 1b = A hiccup event occurred
4	ILIM	R	0b	Current limit. This bit reports whether an current limit event occurred since the last time the STATUS register was read. 0b = No current limit event occurred 1b = An current limit event occurred
3	TWARN	R	0b	Thermal warning. This bit reports whether a thermal warning event occurred since the last time the STATUS register was read. 0b = No thermal warning event occurred 1b = A thermal warning event occurred
2	TSHUT	R	0b	Thermal shutdown. This bit reports whether a thermal shutdown event occurred since the last time the STATUS register was read. 0b = No thermal shutdown event occurred 1b = A thermal shutdown event occurred
1	PBUV	R	1b	Power-bad undervoltage. This bit reports whether a power-bad event (output voltage too low) occurred since the last time the STATUS register was read. 0b = No power-bad undervoltage event occurred 1b = A power-bad undervoltage event occurred
0	PBOV	R	0b	Power-bad overvoltage. This bit reports whether a power-bad event (output voltage too high) occurred since the last time the STATUS register was read. 0b = No power-bad overvoltage event occurred 1b = A power-bad overvoltage event occurred

## 10 Application and Implementation

### 注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくこととなります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

### 10.1 Application Information

The following section discusses selection of the external components to complete the power supply design for typical a application.

### 10.2 Typical Application

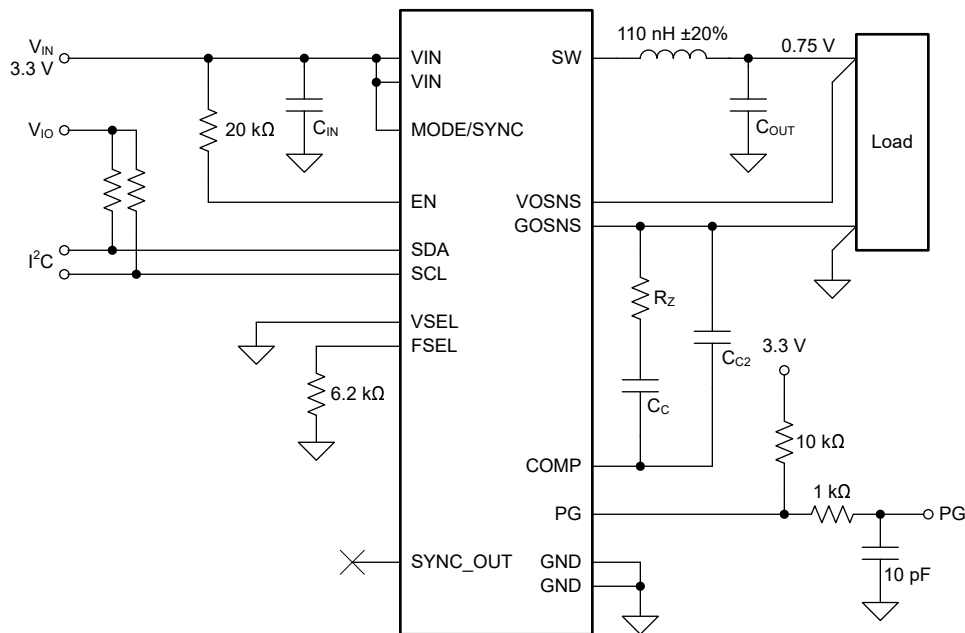


図 10-1. Typical Application Schematic

#### 10.2.1 Design Requirements

表 10-1 lists the operating parameters for this application example.

表 10-1. Design Parameters

Symbol	Parameter	Value
$V_{IN}$	Input voltage	3.3 V
$V_{OUT}$	Output voltage	0.75 V
$TOL_{V_{OUT}}$	Output voltage tolerance allowed by the application	±3.3%
$TOL_{DC}$	Output voltage tolerance of the TPS6287x-Q1 (DC accuracy)	±1%
$\Delta I_{OUT}$	Output current load step	±7.5 A
$t_t$	Load step transition time	1 $\mu$ s
$f_{sw}$	Switching frequency	2.25 MHz
L	Inductance	110 nH
$TOL_{IND}$	Inductor tolerance	±20%
$g_m$	Error amplifier transconductance	1.5 mS
$\tau$	Internal timing parameter	12.5 $\mu$ s

**表 10-1. Design Parameters (続き)**

Symbol	Parameter	Value
TOL <sub>T</sub>	Tolerance of the internal timing parameter	±30%
k <sub>BW</sub>	Ratio of switching frequency to converter bandwidth (must be ≥ 4)	4
Nφ	Number of phases	1

### Preliminary Calculations

The maximum allowable deviation of the power supply is ±3.3%. The DC accuracy of the TPS6287x-Q1 is specified as ±1%, therefore, the maximum output voltage variation during a transient is given by:

$$\Delta V_{OUT} = \pm V_{OUT} \times (3.3\% - 1\%) = \pm 17.25 \text{ mV} \quad (4)$$

### 10.2.2 Detailed Design Procedure

The following subsections describe how to calculate the external components required to meet the specified transient requirements of a given application. The calculations include the worst-case variation of components and use the RMS method to combine the variation of uncorrelated parameters.

#### 10.2.2.1 Selecting the Inductor

The TPS6287x-Q1 devices have been optimized for inductors in the range 50 nH to 300 nH. If the transient response of the converter is limited by the slew rate of the current in the inductor, using a smaller inductor can improve performance. However, the output ripple current increases as the value of the inductor decreases, and higher output current ripple generates higher output voltage ripple, which adds to the transient overshoot or undershoot. The optimal configuration for a given application is always a trade-off between a number of parameters. TI recommends a starting value of 110 nH for typical applications.

The peak-to-peak inductor current ripple is given by:

$$I_{L(PP)} = \frac{V_{OUT}}{V_{IN}} \left( \frac{V_{IN} - V_{OUT}}{N\phi \times L \times f_{sw}} \right) \quad (5)$$

$$I_{L(PP)} = \frac{0.75}{3.3} \left( \frac{3.3 - 0.75}{1 \times 110 \times 10^{-9} \times 2.25 \times 10^6} \right) = 2.342 \text{ A} \quad (6)$$

表 10-2 lists a number of inductors suitable for use with this application. This list is not exhaustive and other inductors from other manufacturers can also be suitable.

**表 10-2. List of Recommended Inductors**

Inductance	Current Rating	Dimensions	DC Resistance	Part Number <sup>(1)</sup>
	(I <sub>SAT</sub> at 25°C)	(L × W × H)		
92 nH	24 A	4 × 4 × 1.2 mm	5.2 mΩ (typical)	Coilcraft, XEL4012-920NE
100 nH	30 A	4 × 4 × 3.2 mm	1.5 mΩ (typical)	Coilcraft, XEL4030-101ME
110 nH	29 A	4 × 4 × 2.1 mm	1.4 mΩ (typical)	Coilcraft, XGL4020-111ME
110 nH	29 A	3.2 × 2.5 × 2.5 mm	1.9 mΩ (typical)	TDK, CLT32-R11
55 nH	39.5 A	3.2 × 2.5 × 2.5 mm	1.0 mΩ (typical)	TDK, CLT32-55N
110 nH	17.0 A	3.2 × 2.5 × 2.5 mm	3.0 mΩ (typical)	Cyntec, VCTA32252E-R11MS6
100 nH	25 A	4.2 × 4.0 × 2.1 mm	1.9 mΩ (typical)	Cyntec, VCHA042A-R10MS62M
100 nH	44 A	5.45 × 5.25 × 2.8 mm	0.8 mΩ (typical)	Cyntec, VCHW053T-R10NMS5

(1) See the [Third-Party Products Disclaimer](#).

### 10.2.2.2 Selecting the Input Capacitors

As with all buck converters, the input current of the TPS6287x-Q1 devices is discontinuous. The input capacitors provide a low-impedance energy source for the device, and their value, type, and location are critical for correct operation. TI recommends low-ESR multilayer ceramic capacitors for best performance. In practice, the total input capacitance is typically comprised of a combination of different capacitors, in which larger capacitors provide the decoupling at lower frequencies and smaller capacitors provide the decoupling at higher frequencies.

The TPS6287x-Q1 devices feature a *butterfly* layout with two pairs of VIN and GND pins on opposite sides of the package. This allows the input capacitors to be placed symmetrically on the PCB so that the electromagnetic fields generated cancel each other out, thereby reducing EMI.

The duty cycle of the converter is given by:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}} \quad (7)$$

where

- $V_{IN}$  is the input voltage.
- $V_{OUT}$  is the output voltage.
- $\eta$  is the efficiency.

$$D = \frac{0.75}{0.9 \times 3.3} = 0.253 \quad (8)$$

The value of input capacitance needed to meet the input voltage ripple requirements is given by:

$$C_{IN} = \frac{D \times (1 - D) \times I_{OUT}}{V_{IN(PP)} \times f_{sw}} \quad (9)$$

where

- $D$  is the duty cycle.
- $f_{sw}$  is the switching frequency.
- $L$  is the inductance.
- $I_{OUT}$  is the output current.

100mV is used as the input voltage ripple target.

$$C_{IN} = \frac{0.253 \times (1 - 0.253) \times 11.3}{0.1 \times 2.25 \times 10^6} = 9.5 \mu\text{F} \quad (10)$$

The value of  $C_{IN}$  calculated with 式 9 is the *effective* capacitance after all derating, tolerance, and aging effects have been considered. 5  $\mu\text{F}$  effective capacitance per input pin is required. TI recommends multilayer ceramic capacitors with an X7R dielectric (or similar) for  $C_{IN}$ , and these capacitors must be placed as close to the VIN and GND pins as possible to minimize the loop area.

表 10-3 lists a number of capacitors suitable for this application. This list is not exhaustive and other capacitors from other manufacturers can also be suitable.

**表 10-3. List of Recommended Input Capacitors**

Capacitance	Dimensions	Voltage Rating	Manufacturer, Part Number <sup>(1)</sup>
	mm (Inch)		
470 nF $\pm 10\%$	1005 (0402)	10 V	Murata, GCM155C71A474KE36D
470 nF $\pm 10\%$	1005 (0402)	10 V	TDK, CGA2B3X7S1A474K050BB
10 $\mu\text{F}$ $\pm 10\%$	2012 (0805)	10 V	Murata, GCM21BR71A106KE22L
10 $\mu\text{F}$ $\pm 10\%$	2012 (0805)	10 V	TDK, CGA4J3X7S1A106K125AB
22 $\mu\text{F}$ $\pm 10\%$	3216 (1206)	10 V	Murata, GCM31CR71A226KE02L

表 10-3. List of Recommended Input Capacitors (続き)

Capacitance	Dimensions	Voltage Rating	Manufacturer, Part Number <sup>(1)</sup>
	mm (Inch)		
22 μF ±20%	3216 (1206)	10 V	TDK, CGA5L1X7S1A226M160AC

(1) See the [Third-Party Products Disclaimer](#).

### 10.2.2.3 Selecting the Compensation Resistor

Use 式 11 to calculate the recommended value of compensation resistor,  $R_Z$ :

$$R_Z = \frac{1}{g_m} \left( \frac{\pi \times \left( \Delta I_{OUT} + \frac{I_{L(PP)}}{2} \right) \times \frac{L}{N\Phi}}{4 \times \tau \times \Delta V_{OUT}} - 1 \right) \left( 1 + \sqrt{TOL_{IND}^2 + TOL_{\tau}^2} \right) \quad (11)$$

$$R_Z = \frac{1}{1.5 \times 10^{-3}} \left( \frac{\pi \times \left( 7.5 + \frac{2.342}{2} \right) \times \frac{110 \times 10^{-9}}{1}}{4 \times 12.5 \times 10^{-6} \times 17.25 \times 10^{-3}} - 1 \right) \left( 1 + \sqrt{20\%^2 + 30\%^2} \right) = 2.244 \text{ k}\Omega \quad (12)$$

Rounding up, the closest standard value from the E24 series is 2.4 kΩ.

### 10.2.2.4 Selecting the Output Capacitors

In practice, the total output capacitance is typically comprised of a combination of different capacitors, in which larger capacitors provide the load current at lower frequencies and smaller capacitors provide the load current at higher frequencies. The value, type, and location of the output capacitors are critical for correct operation. TI recommends low-ESR multilayer ceramic capacitors with an X7R dielectric (or similar) for best performance.

The TPS6287x devices feature a butterfly layout with two GND pins on opposite sides of the package. This allows the output capacitors to be placed symmetrically on the PCB such that the electromagnetic fields generated cancel each other out, thereby reducing EMI.

The transient response of the converter is limited by one of two criteria:

- The slew rate of the current through the inductor, in which case, the feedback loop of the converter saturates.
- The maximum allowed ratio of converter bandwidth to switching frequency, in which the converter remains in regulation (that is, its loop does not saturate). TI recommends a minimum ratio of four for typical applications.

Which of the above criteria applies in any given application depends on the operating conditions and component values used. Therefore, TI recommends that the user calculate the output capacitance for both cases, and select the higher of the two values.

If the converter remains in regulation, the minimum output required capacitance is given by:

$$C_{OUT(min)(reg)} = \left( \frac{\tau \times (1 + g_m \times R_Z)}{2 \times \pi \times \frac{L}{N\Phi} \times \frac{f_{SW}}{4}} \right) \left( 1 + \sqrt{TOL_{\tau}^2 + TOL_{IND}^2 + TOL_{fSW}^2} \right) \quad (13)$$

$$C_{OUT(min)(reg)} = \left( \frac{12.5 \times 10^{-6} \times \left( 1 + 1.5 \times 10^{-3} \times 2.4 \times 10^3 \right)}{2 \times \pi \times \frac{110 \times 10^{-9}}{1} \times 10^{-9} \times \frac{2.25 \times 10^6}{4}} \right) \left( 1 + \sqrt{30\%^2 + 20\%^2 + 10\%^2} \right) = 203.2 \text{ }\mu\text{F} \quad (14)$$

If the converter loop saturates, the minimum output capacitance is given by:

$$C_{OUT(min)(sat)} = \frac{1}{\Delta V_{OUT}} \left( \frac{\frac{L}{N\Phi} \times \left( \Delta I_{OUT} + \frac{I_{L(PP)}}{2} \right)^2}{2 \times V_{OUT}} - \frac{\Delta I_{OUT} \times t_t}{2} \right) (1 + TOL_{IND}) \quad (15)$$

$$C_{OUT(min)(sat)} = \frac{1}{17.25 \times 10^{-3}} \left( \frac{\frac{110 \times 10^{-9}}{1} \times \left(7.5 + \frac{2.342}{2}\right)^2}{2 \times 0.75} - \frac{7.5 \times 1 \times 10^{-6}}{2} \right) (1 + 20\%) = 122.7 \mu\text{F} \quad (16)$$

In this case, choose  $C_{OUT(min)} = 203 \mu\text{F}$  as the larger of the two values for the output capacitance.

When calculating worst-case component values, use the value calculated above as the *minimum* output capacitance required. For ceramic capacitors, the *maximum* capacitance when considering tolerance, DC bias, temperature, and aging effects is typically two times the minimum capacitance. In this case, the maximum capacitance  $C_{OUT(max)}$  is  $406 \mu\text{F}$ .

表 10-4. List of Recommended Output Capacitors

Capacitance	Dimensions	Voltage Rating	Manufacturer, Part Number <sup>(1)</sup>
	mm (Inch)		
22 $\mu\text{F} \pm 20\%$	2012 (0805)	6.3 V	TDK, CGA4J1X7T0J226M125AC
22 $\mu\text{F} \pm 10\%$	2012 (0805)	6.3 V	Murata, GCM31CR71A226KE02
47 $\mu\text{F} \pm 20\%$	3216 (1206)	4 V	TDK, CGA5L1X7T0G476M160AC
47 $\mu\text{F} \pm 20\%$	2012 (1210)	6.3 V	Murata, GCM32ER70J476ME19
100 $\mu\text{F} \pm 20\%$	3225 (1210)	4 V	TDK, CGA6P1X7T0G107M250AC
100 $\mu\text{F} \pm 20\%$	3216 (1210)	6.3 V	Murata, GRT32EC70J107ME13

(1) See the [Third-Party Products Disclaimer](#).

### 10.2.2.5 Selecting the Compensation Capacitor, $C_C$

First, use 式 17 to calculate the bandwidth of the inner loop:

$$BW_{INNER} = \frac{\tau}{2\pi \times \frac{L}{N\Phi} \times C_{OUT(max)}} \quad (17)$$

$$BW_{INNER} = \frac{12.5 \times 10^{-6}}{2\pi \times \frac{110 \times 10^{-9}}{1} \times 203.2 \times 10^{-6}} = 89 \text{ kHz} \quad (18)$$

Next, calculate the product of  $g_m R_Z$ :

$$g_m \times R_Z = 1.5 \times 10^{-3} \times 2.4 \times 10^3 = 3.6 \quad (19)$$

If  $g_m R_Z > 1$ , use 式 20 to calculate the recommended value of  $C_C$ . If  $g_m R_Z < 1$ , use 式 22 to calculate the recommended value of  $C_C$ .

$$C_C = \frac{2}{\pi \times BW_{INNER} \times g_m \times R_Z^2} \quad (20)$$

$$C_C = \frac{2}{\pi \times 89 \times 10^3 \times 1.5 \times 10^{-3} \times (2.4 \times 10^3)^2} = 0.828 \text{ nF} \quad (21)$$

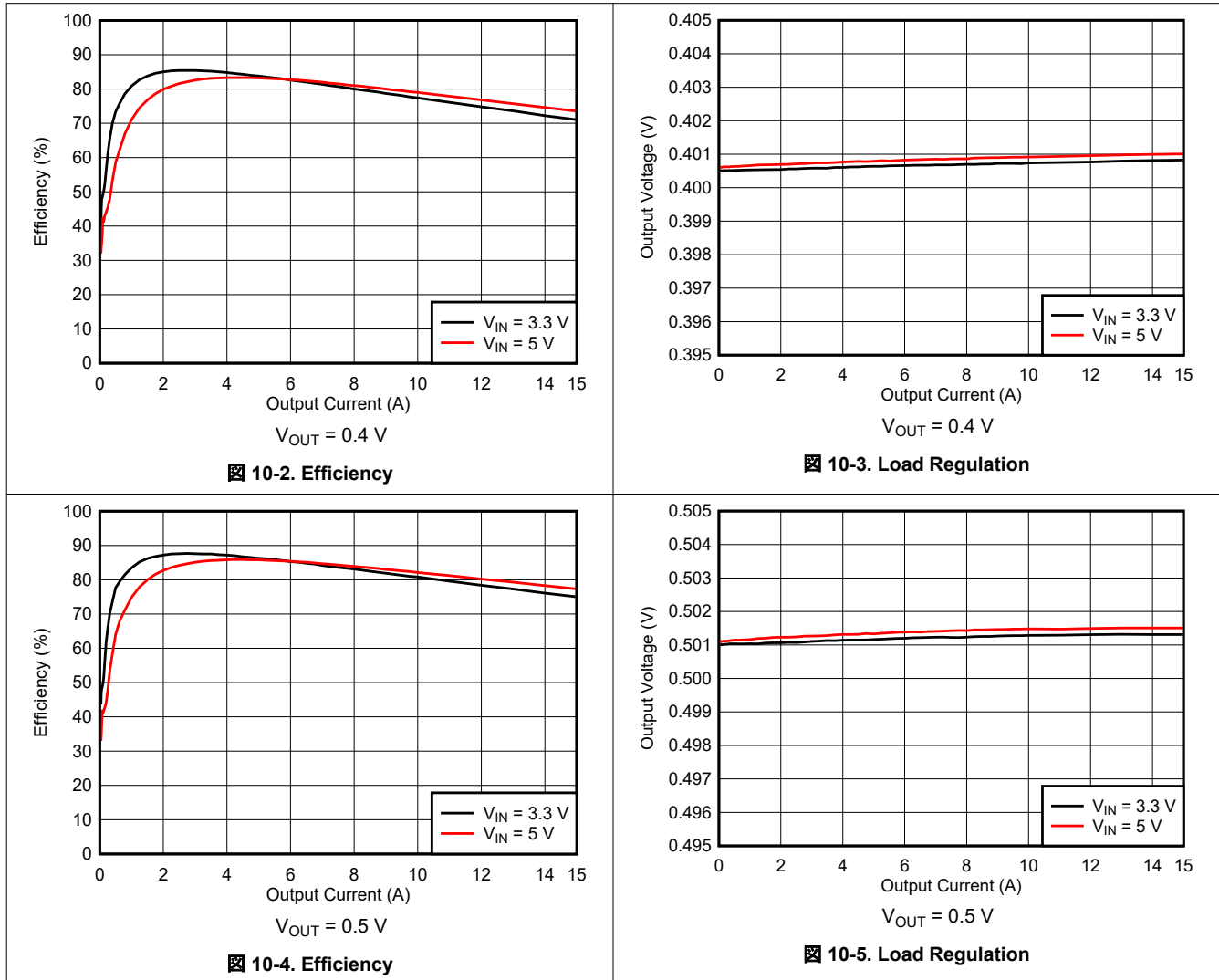
The closest standard value from the E12 series is 0.82 nF.

$$C_C = \frac{2 \times g_m}{\pi \times BW_{INNER}} \quad (22)$$

### 10.2.2.6 Selecting the Compensation Capacitor, $C_{C2}$

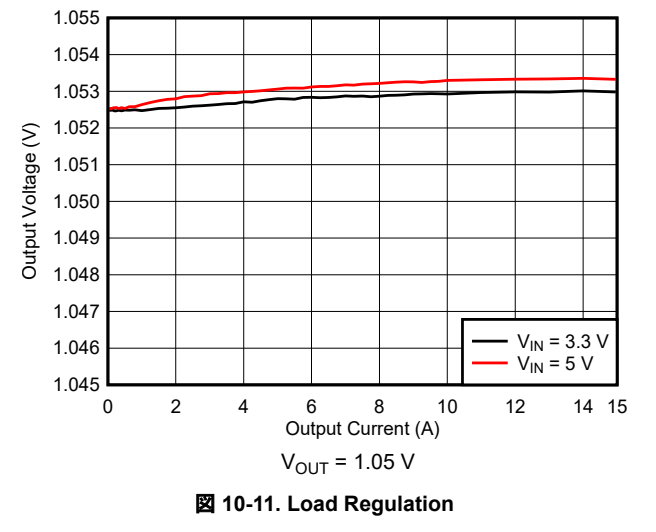
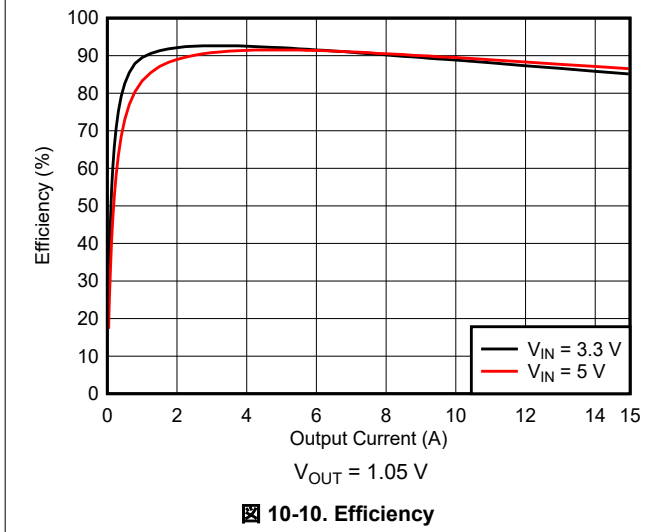
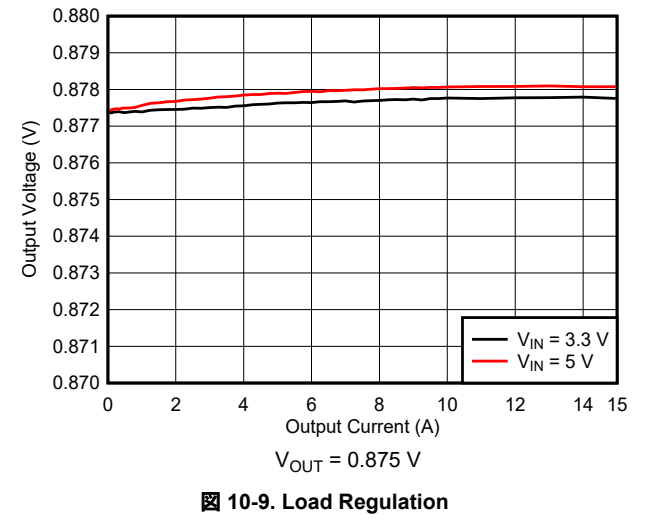
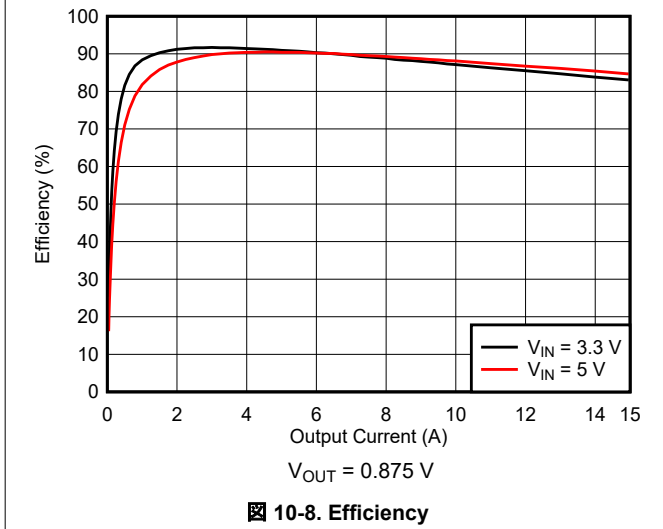
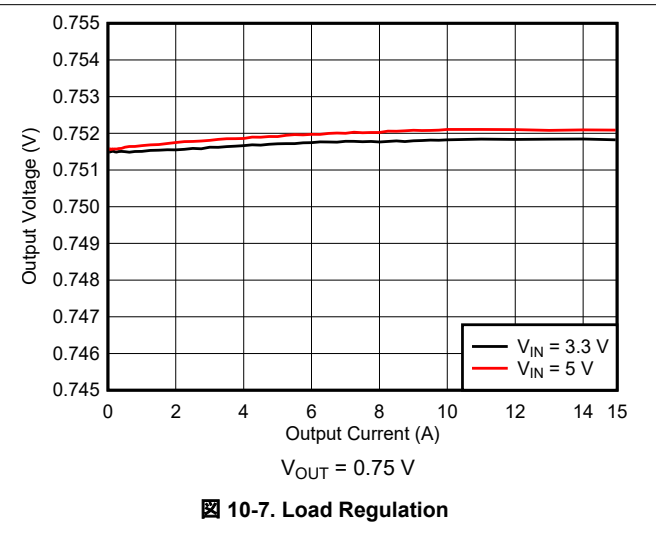
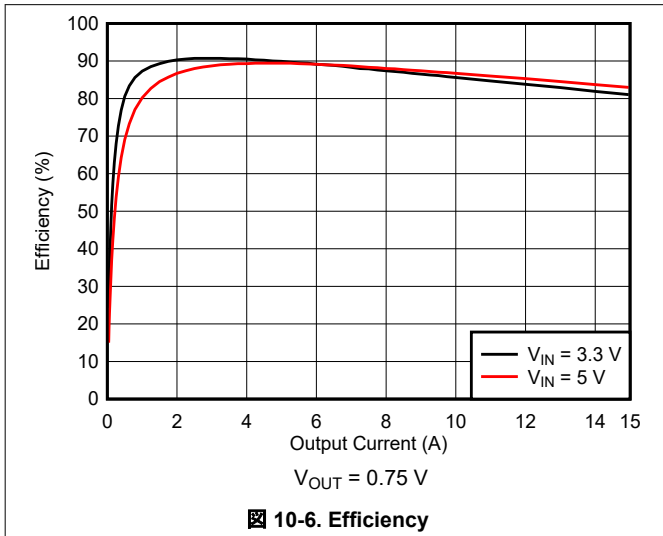
The compensation capacitor,  $C_{C2}$ , is an optional capacitor that TI recommends the user include to bypass high-frequency noise away from the COMP pin. The value of this capacitor is not critical; 10-pF or 22-pF capacitors are suitable for typical applications.

### 10.2.3 Application Curves

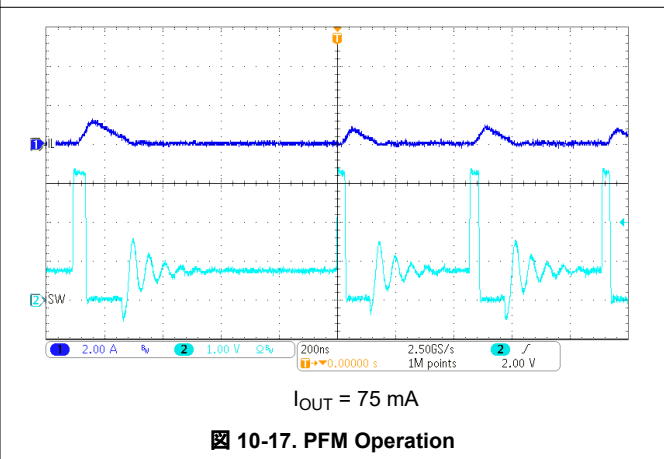
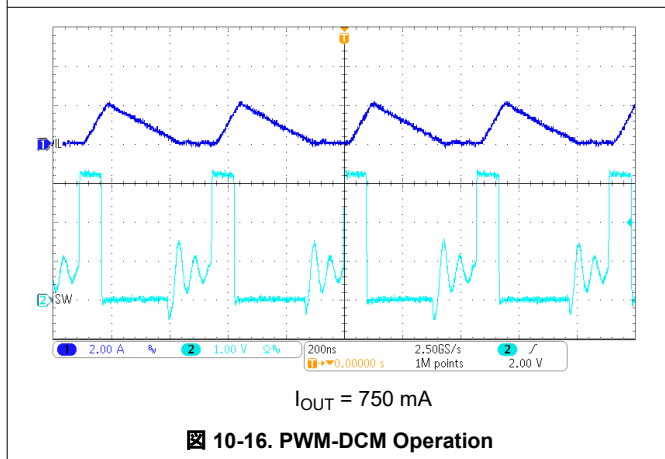
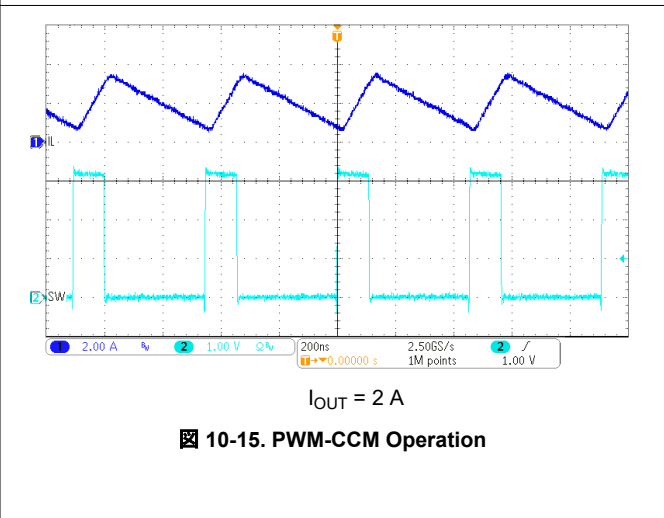
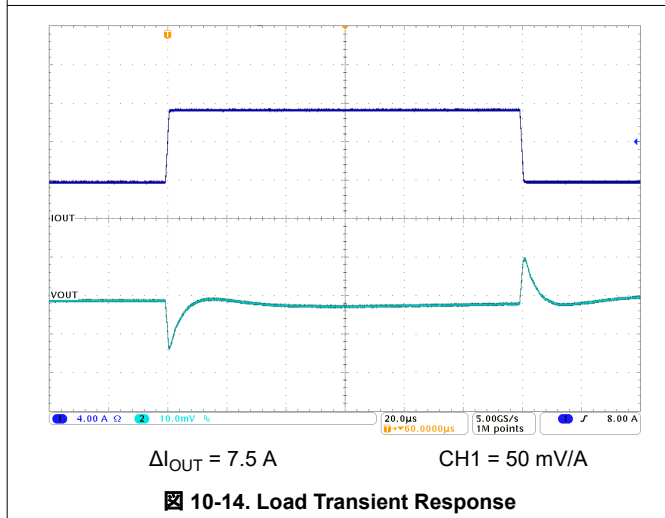
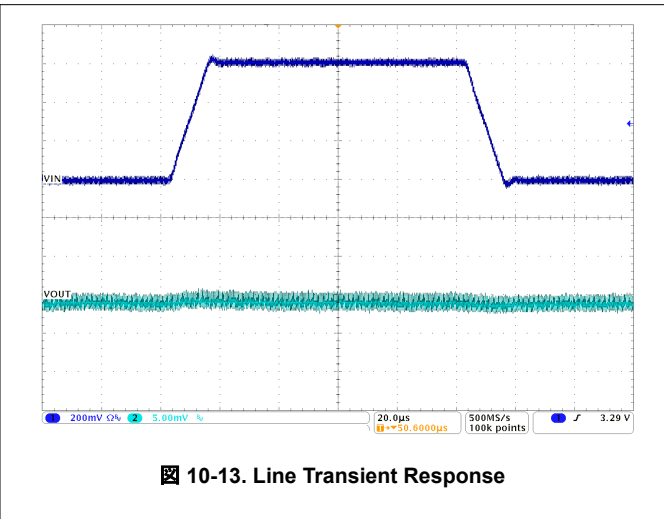
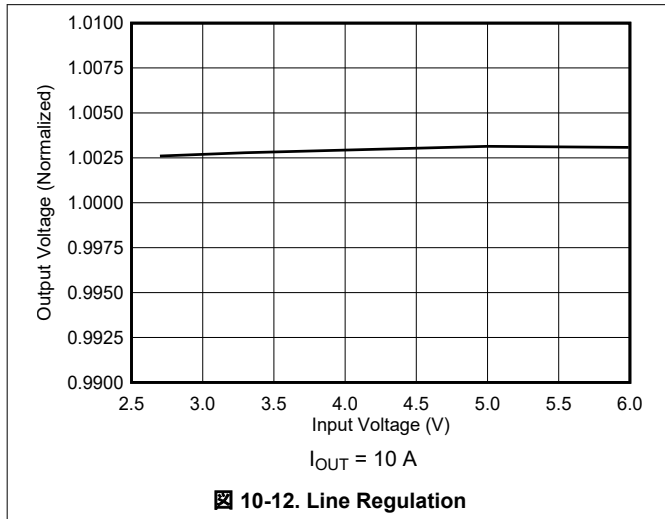




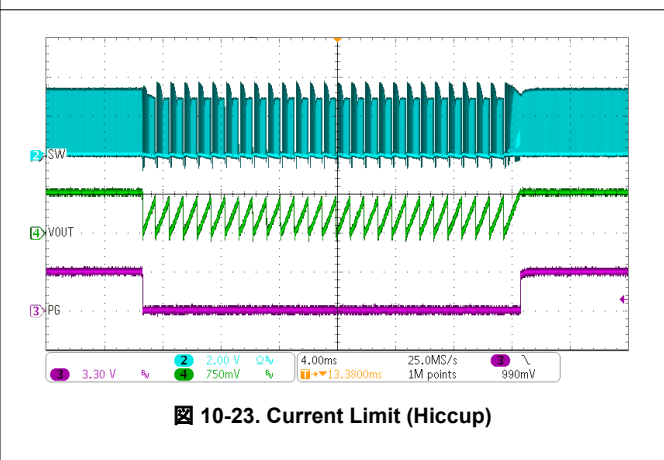
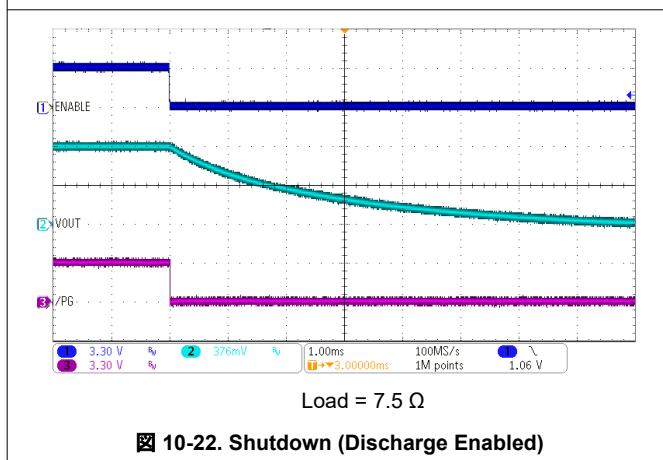
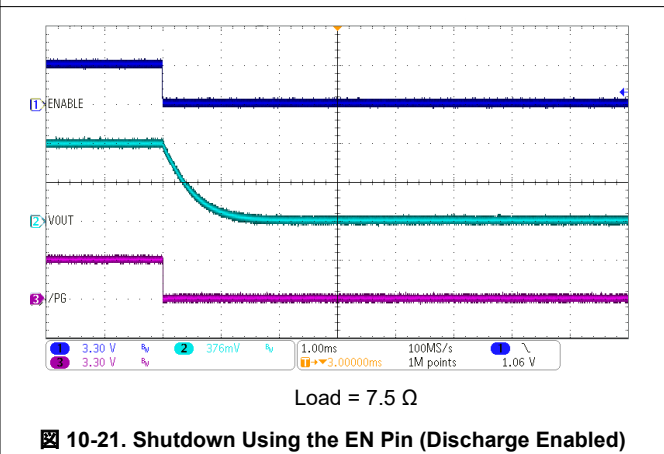
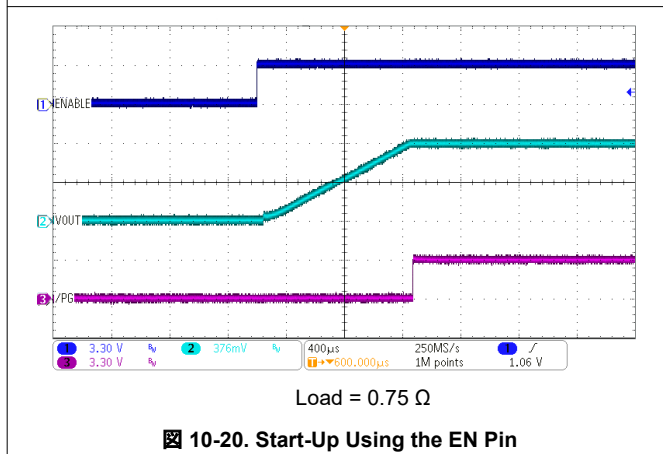
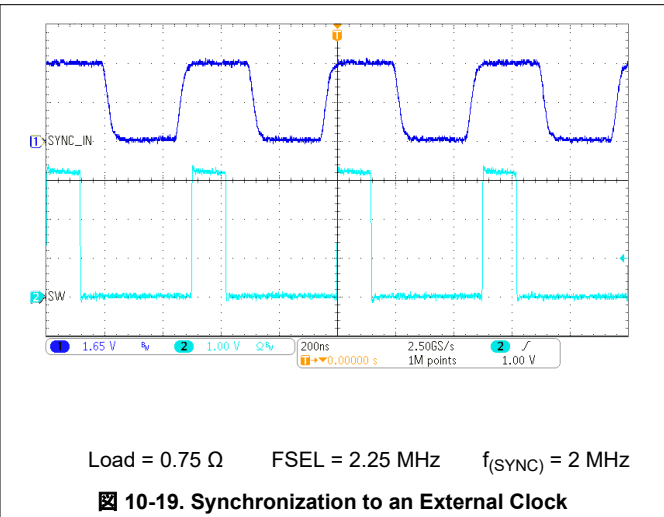
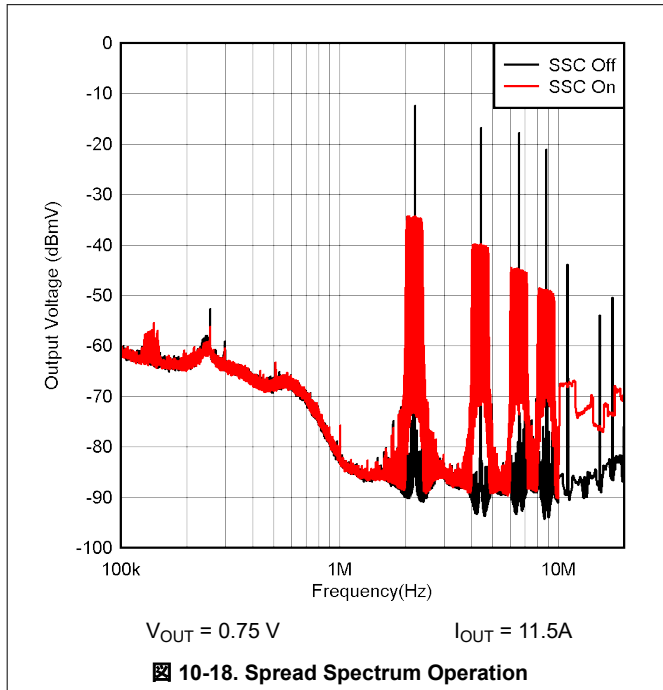
### 10.2.3 Application Curves (continued)



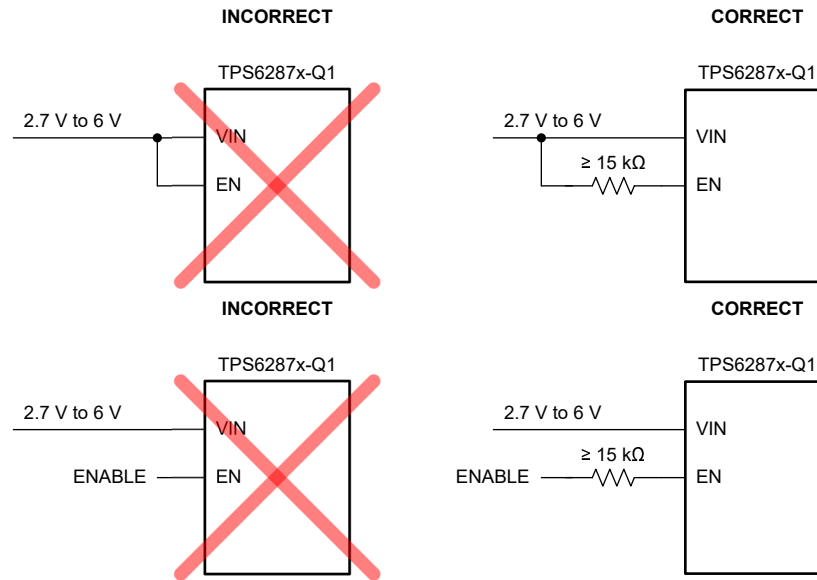
### 10.2.3 Application Curves (continued)



### 10.2.3 Application Curves (continued)



## 10.3 Best Design Practices



## 10.4 Power Supply Recommendations

The TPS6287x-Q1 family has no special requirements for its input power supply. The output current rating of the input power supply must be rated according to the supply voltage and current requirements of the TPS6287x-Q1.

## 10.5 Layout

### 10.5.1 Layout Guidelines

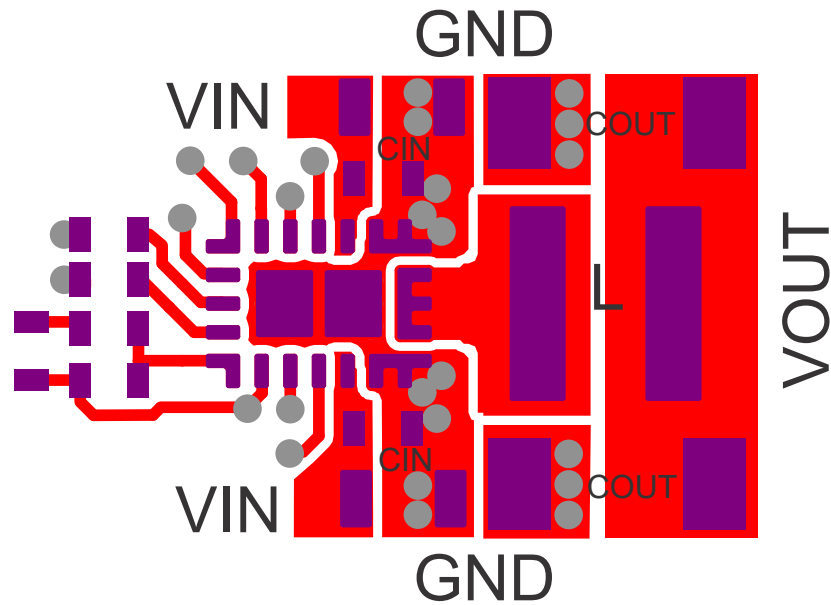
Achieving the performance the TPS6287x-Q1 devices are capable of requires proper PDN and PCB design. TI therefore recommends the user perform a power integrity analysis on their design. There are a number of commercially available power integrity software tools, and the user can use these tools to model the effects on performance of the PCB layout and passive components.

In addition to the use of power integrity tools, TI recommends the following basic principles:

- Place the input capacitors close to the VIN and GND pins. Position the input capacitors in order of increasing size, starting with the smallest capacitors closest to the VIN and GND pins. Use an identical layout for both VIN-GND pin pairs of the package, to gain maximum benefit from the butterfly configuration.
- Place the inductor close to the device and keep the SW node small.
- Connect the exposed thermal pad and the GND pins of the device together. Use multiple thermal vias to connect the exposed thermal pad of the device to one or more ground planes (TI's EVM uses nine 150- $\mu\text{m}$  thermal vias).
- Use multiple power and ground planes.
- Route the VOSNS and GOSNS remote sense lines as a differential pair and connect them to the lowest-impedance point of the PDN. If the desired connection point is not the lowest impedance point of the PDN, optimize the PDN until it is. Do not route the VOSNS and GOSNS close to any of the switch nodes.
- Connect the compensation components between VOSNS and GOSNS. Do not connect the compensation components directly to power ground.
- Use multiple vias to connect each capacitor pad to the power and ground planes (TI's EVM typically uses four vias per pad).
- Use plenty of stitching vias to ensure a low impedance connection between different power and ground planes.

### 10.5.2 Layout Example

☒ 10-24 shows the top layer of one of the evaluation modules for this device. It demonstrates the practical implementation of the PCB layout principles previously listed. The user can find a complete set of drawings of all the layers used in this PCB in the evaluation module's user guide.



☒ 10-24. Layout Example

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 サード・パーティ製品に関する免責事項

サード・パーティ製品またはサービスに関するテキサス・インスツルメンツの出版物は、単独またはテキサス・インスツルメンツの製品、サービスと一緒に提供される場合に関係なく、サード・パーティ製品またはサービスの適合性に関する是認、サード・パーティ製品またはサービスの是認の表明を意味するものではありません。

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation see the following:

Texas Instruments, [Semiconductor and IC Package Thermal Metrics](#) application report

### 11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.4 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの[使用条件](#)を参照してください。

### 11.5 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

### 11.6 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

### 11.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62870N0QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	870N0B	<a href="#">Samples</a>
TPS62870QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	870B	<a href="#">Samples</a>
TPS62870Y0QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	870Y0B	<a href="#">Samples</a>
TPS62870Y1QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	870Y1B	<a href="#">Samples</a>
TPS62870Y2QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	870Y2B	<a href="#">Samples</a>
TPS62870Y3QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	870Y3B	<a href="#">Samples</a>
TPS62871N0QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	871N0B	<a href="#">Samples</a>
TPS62871N1QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	871N1B	<a href="#">Samples</a>
TPS62871QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	871B	<a href="#">Samples</a>
TPS62871Y1QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	871Y1B	<a href="#">Samples</a>
TPS62871Y5QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	871Y5B	<a href="#">Samples</a>
TPS62872N0QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	872N0B	<a href="#">Samples</a>
TPS62872N3QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	872N3B	<a href="#">Samples</a>
TPS62872QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	872B	<a href="#">Samples</a>
TPS62872Y1QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	872Y1B	<a href="#">Samples</a>
TPS62872Y2QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	872Y2B	<a href="#">Samples</a>
TPS62872Y4QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	872Y4B	<a href="#">Samples</a>
TPS62872Y7QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	872Y7B	<a href="#">Samples</a>
TPS62873N0QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	873N0B	<a href="#">Samples</a>
TPS62873N1QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	873N1B	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62873QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	873B	<a href="#">Samples</a>
TPS62873Y1QWRXSRQ1	ACTIVE	VQFN-FCRLF	RXS	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	873Y1B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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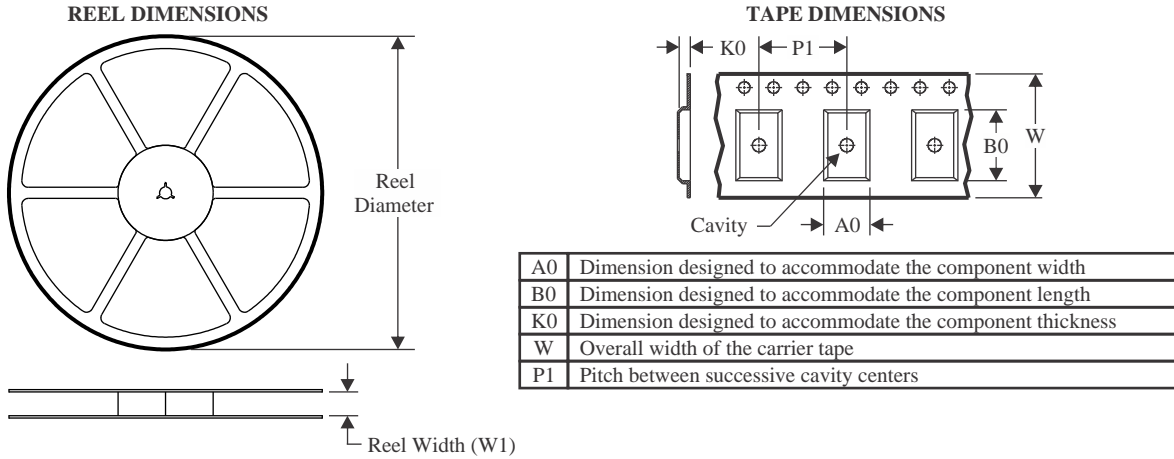
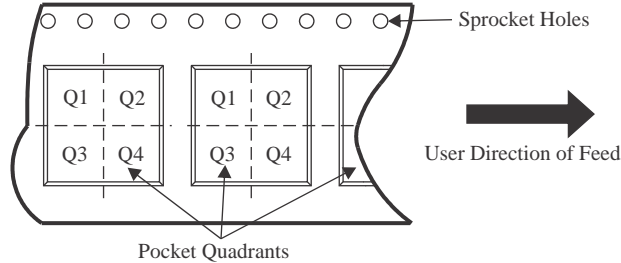
**OTHER QUALIFIED VERSIONS OF TPS62870-Q1, TPS62871-Q1, TPS62872-Q1, TPS62873-Q1 :**



- Catalog : [TPS62870](#), [TPS62871](#), [TPS62872](#), [TPS62873](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62870N0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62870QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62870Y0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62870Y1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62870Y2QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62870Y3QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62871N0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62871N1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62871QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62871Y1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62871Y5QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62872N0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62872N3QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62872QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62872Y1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62872Y2QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62872Y4QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62872Y7QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62873N0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62873N1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62873QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1
TPS62873Y1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	330.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

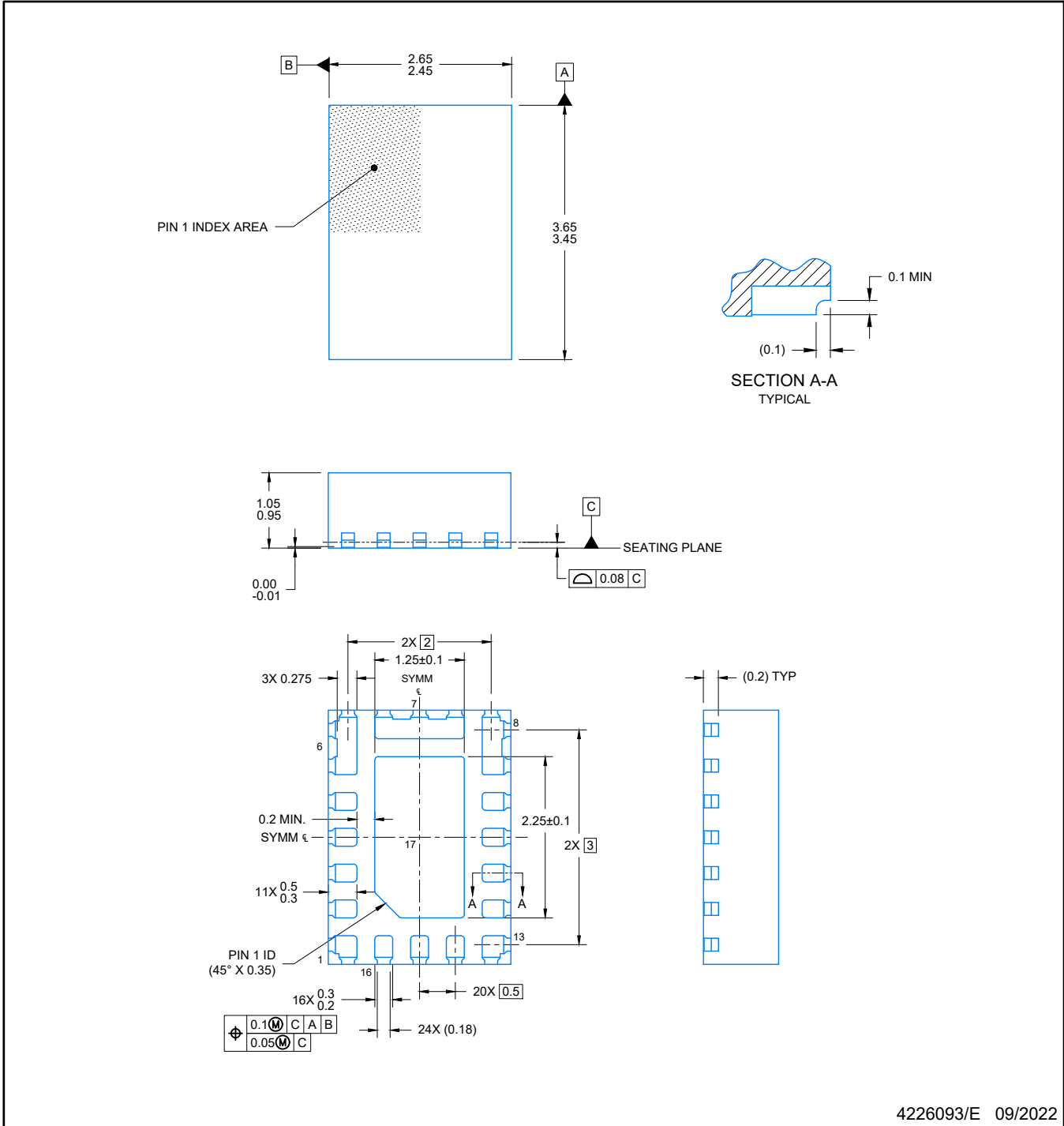
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62870N0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62870QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62870Y0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62870Y1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62870Y2QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62870Y3QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62871N0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62871N1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62871QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62871Y1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62871Y5QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62872N0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62872N3QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62872QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62872Y1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62872Y2QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62872Y4QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62872Y7QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0

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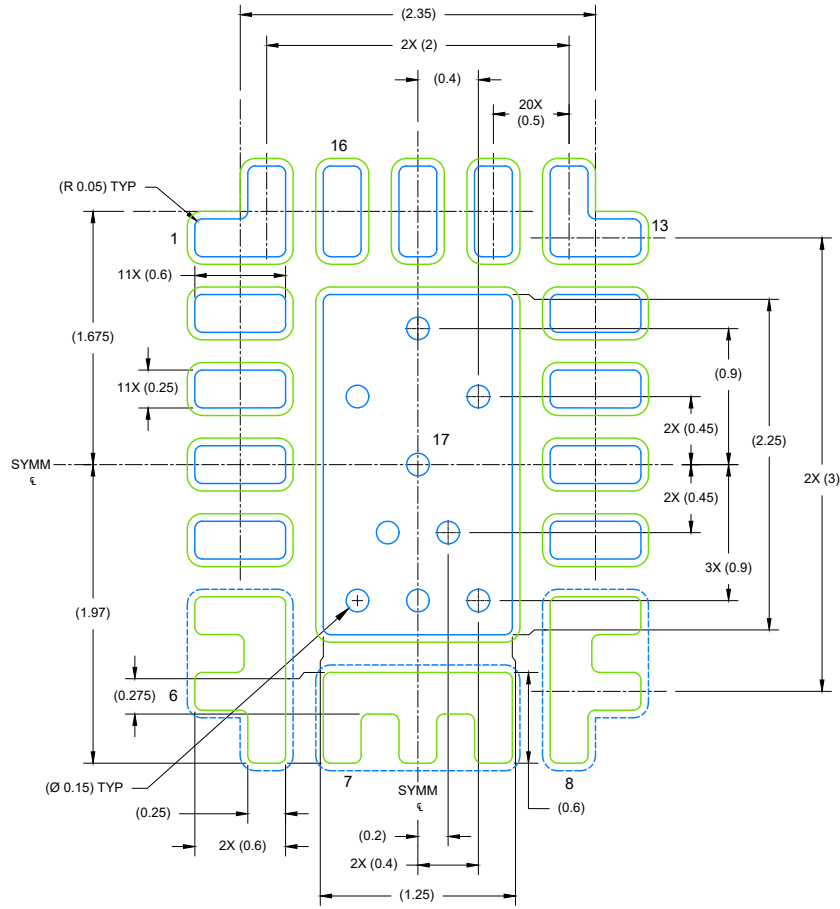
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62873N0QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62873N1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62873QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0
TPS62873Y1QWRXSRQ1	VQFN-FCRLF	RXS	16	3000	338.0	355.0	50.0



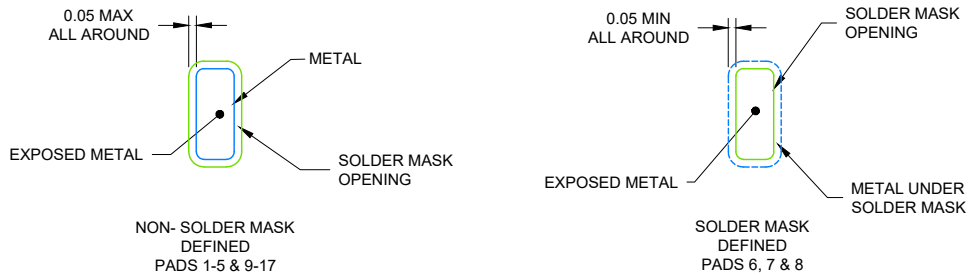
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X

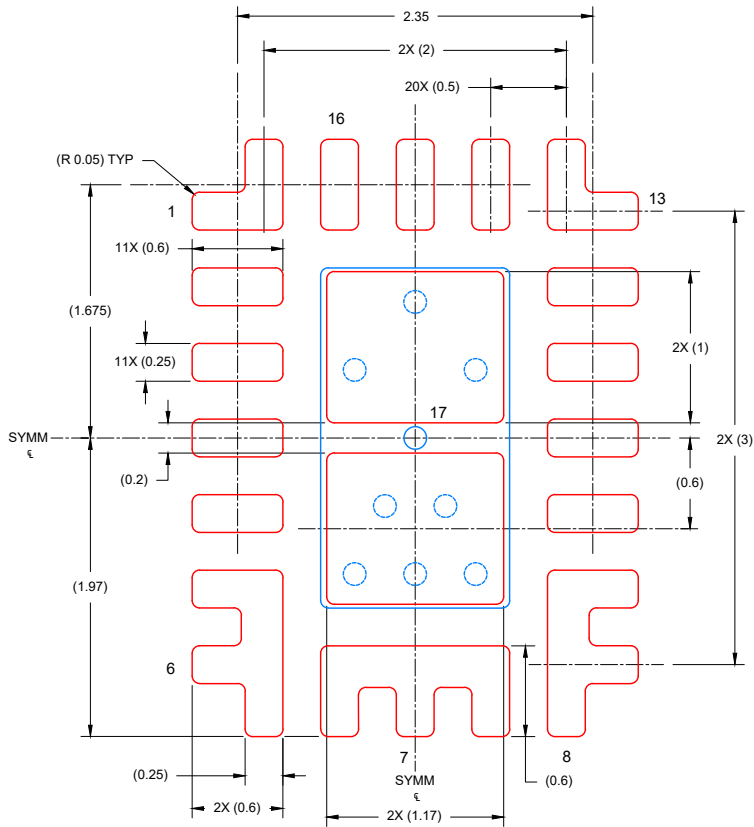


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



**SOLDER PASTE EXAMPLE**  
**BASED ON 0.1 mm THICK STENCIL**

SCALE: 15X

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NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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