TEXAS INSTRUMENTS
TPS62865, TPS62867
JAJSLM0 – MARCH 2021

TPS62865/TPS62867 2.4V～5.5V 入力、4A および 6A 同期整流降圧コンバータ、1.5 x 2.5mm QFN パッケージ

1 特長

- DCS-Control トポロジにより、高速過渡応答を実現
- 11mΩ および 10.5mΩ のパワー MOSFET を内蔵
- ±1% の出力電圧精度
- 動作時の静止電流:4μA
- 入力電圧範囲:2.4V～5.5V
- 可変出力電圧範囲: 0.6V～V_{IN}
- 固定 (外付け抵抗で選択可能) および可変出力電圧バージョン
- 2.4MHz のスイッチング周波数
- 強制 PWM またはパワーセーブ・モード
- 出力電圧放電
- 100% デューティ・サイクル・モード
- ヒカップ短絡保護機能
- パワー・グッド・インジケータとウィンドウ・コンパレータ
- サーマル・シャットダウン
- 最小 30mm^2 のソリューション・サイズ が可能
- 1.5Mm×2.5mm の QFN、0.5mm ピッチで供給
- WEBENCH® Power Designer により、TPS62865 を使用するカスタム設計を作成
- WEBENCH® Power Designer により、TPS62867 を使用するカスタム設計を作成

2 アプリケーション

- FPGA、CPU、ASIC、ビデオ・チップセット用のコア電源
- マシン・ビジョン・カメラ
- IP ネットワーク・カメラ
- ソリッドステート・ドライブ
- 光モジュール
- マルチファンクション・プリンタ

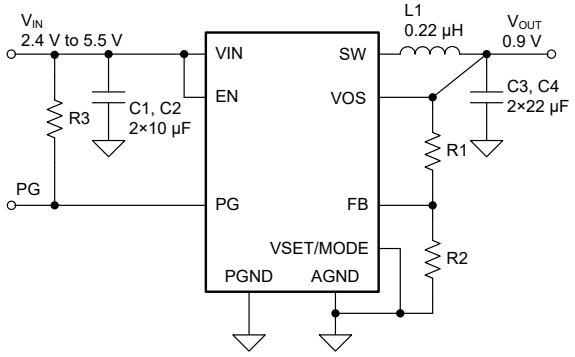
3 概要

TPS62865 および TPS62867 は、高効率で柔軟性が高く高電力密度のソリューションを実現する高周波数同期整流降圧コンバータです。中負荷から重負荷では PWM モードで動作し、軽負荷時には自動的にパワーセーブ・モードへ移行するので、負荷電流の全範囲にわたって高効率が維持されます。このデバイスは、強制的に PWM モードで動作させ、出力電圧リップルを最小化することもできます。DCS-Control アーキテクチャと相まって、優れた負荷過渡性能と厳格な出力電圧精度を実現します。このデバイスは、パワー・グッド信号と、内部のソフトスタート回路を備えています。100% モードで動作可能です。フォルト保護としては、ヒカップ短絡保護機能と、サーマル・シャットダウンが内蔵されています。

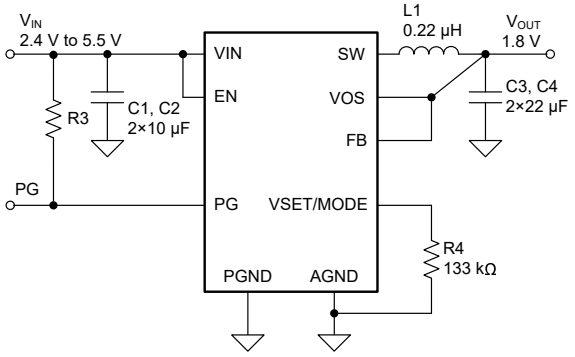
製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS62865	QFN (9)	1.5 × 2.5 × 1mm
TPS62867		

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図 - 可変出力電圧



代表的なアプリケーション回路図 - 固定出力電圧

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
March 2021	*	Initial Release

5 Device Options

PART NUMBER(1)	OUTPUT CURRENT
TPS62865	4 A
TPS62867	6 A

(1) For all available packages, see the orderable addendum at the end of the data sheet.

6 Pin Configuration and Functions

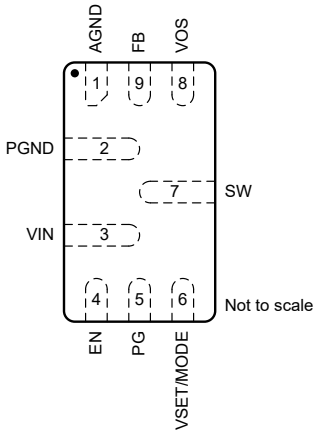


図 6-1. 9-Pin RQY QFN Package (Top View)

表 6-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
AGND	1	Analog ground pin
FB	9	Feedback pin. For the fixed output voltage versions, the pin must be connected to the output directly.
VOS	8	Output voltage sense pin. This pin must be directly connected to the output capacitor.
PGND	2	Power ground pin
SW	7	Switch pin of the power stage
VIN	3	Power supply input voltage pin
EN	4	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
VSET/MODE	6	Voltage Set pin In fixed output voltage applications, connect a resistor between this pin and GND to set the output voltage (see 表 8-2). After start-up, connect this pin to a high level to enable forced-PWM operation, or to a low level to enable power-save mode. In adjustable output voltage applications, connect this pin to a high level to enable forced-PWM operation, or to a low level to enable power-save mode operation.
PG	5	Power-good open-drain output pin. The pullup resistor can be connected to voltages up to 5.5 V. If unused, leave it floating.

7 Specifications

7.1 Absolute Maximum Ratings

See (1)

		MIN	MAX	UNIT
Voltage(2)	VIN, EN, VOS, FB, PG, VSET/MODE	–0.3	6	V
	SW (DC)	–0.3	V_{IN} + 0.3	
	SW (AC, less than 10 ns)(3)	–2.5	10	
I_{SINK_PG}	Sink current at PG		1	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network ground terminal.
(3) While switching

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply Voltage Range	2.4		5.5	V
V_{OUT}	Output Voltage Range	0.6		V_{IN}	V
SR	Slew rate at VIN(1)	–10			mV/µs
I_{OUT}	Output current, TPS62865			4	A
	Output current, TPS62867			6	
T_J	Junction temperature	–40		125	°C

(1) The falling slew rate of V_{IN} must be limited if V_{IN} goes below V_{UVLO}.

7.4 Thermal Information

THERMAL METRIC(1)		TPS6286x		UNIT
		JEDEC 51-7	TPS62867EVM-121	
		9 PINS	9 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.9	60.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	68.2	n/a(2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.0	n/a(2)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.9	3.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	24.7	31.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Not applicable to an EVM

7.5 Electrical Characteristics

T_J = –40°C to 125°C, and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current	EN = High, no load, device not switching		4	10	µA
I_{Q_VOS}	Operating quiescent current into VOS pin	EN = High, no load, device not switching, V_{VOS} = 1.8 V		8		µA
I_{SD}	Shutdown current	EN = Low, T_J = –40°C to 85°C		0.24	1	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising	2.2	2.3	2.4	V
		V_{IN} falling	2.1	2.2	2.3	V
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE						
V_{IH}	High-level input threshold voltage at EN and VSET/MODE		0.84			V
V_{IL}	Low-level input threshold voltage at EN and VSET/MODE				0.4	V
$I_{EN,LKG}$	Input leakage current into EN pin			0.01	0.1	µA
STARTUP, POWER GOOD						
t_{Delay}	Enable delay time	Time from EN high to device starts switching 249-kΩ resistor connected between VSET/MODE and GND	420	700	1100	µs
t_{Ramp}	Output voltage ramp time	Time from device starts switching to power good	0.8	1	1.5	ms
V_{PG}	Power good lower threshold	V_{VOS} referenced to V_{OUT} nominal	85%	91%	96%	
	Power good upper threshold	V_{VOS} referenced to V_{OUT} nominal	103%	111%	120%	
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1 mA, PG pin version			0.36	V
$t_{PG,DLY}$	Power good deglitch delay	Rising and falling edges		34		µs
OUTPUT						
V_{OUT}	Output voltage accuracy	Fixed voltage operation, FPWM, no load, T_J = 0°C to 85°C	–1%		1%	
		Fixed voltage operation, FPWM, no load	–2%		2%	
V_{FB}	Feedback voltage	Adjustable voltage operation	594	600	606	mV
$I_{FB,LKG}$	Input leakage into FB pin	Adjustable voltage operation, V_{FB} = 0.6 V		0.01	0.4	µA
$I_{VOS,LKG}$	Input leakage current into VOS pin	Output discharge disabled, V_{VOS} = 1.8 V		0.2	2.5	µA
R_{DIS}	Output discharge resistor at VOS pin			3.5		Ω
	Load regulation	V_{OUT} = 0.9 V, FPWM		0.04		%/A
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			11		mΩ
	Low-side FET on-resistance			10.5		mΩ
I_{LIM}	High-side FET forward current limit	TPS62865	5	5.5	6	A
		TPS62867	7	7.7	8.5	A
	Low-side FET forward current limit	TPS62865		4.5		A
		TPS62867		6.5		A
	Low-side FET negative current limit	TPS62865, TPS62867		–3		A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A, V_{OUT} = 0.9 V		2.4		MHz

7.6 Typical Characteristics

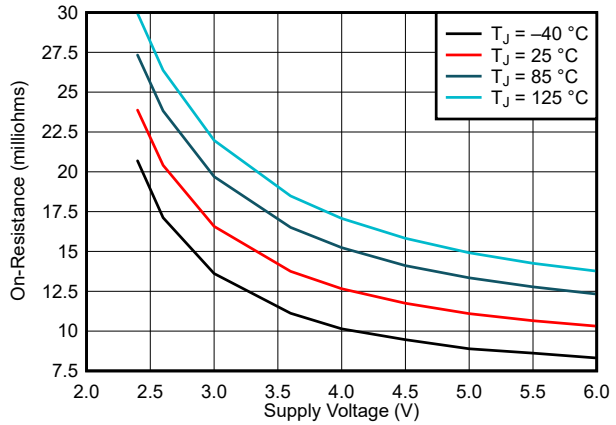


図 7-1. High-Side FET On-Resistance

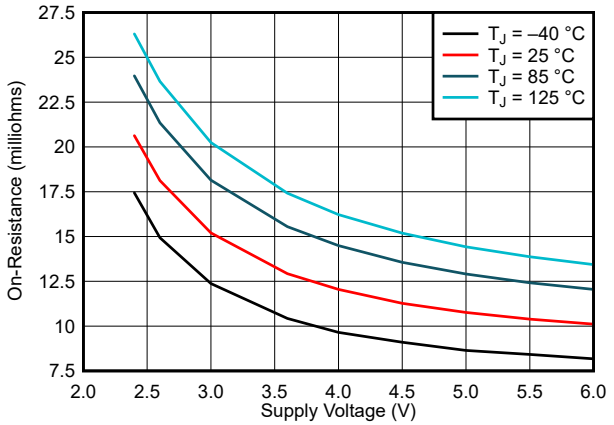


図 7-2. Low-Side FET On-Resistance

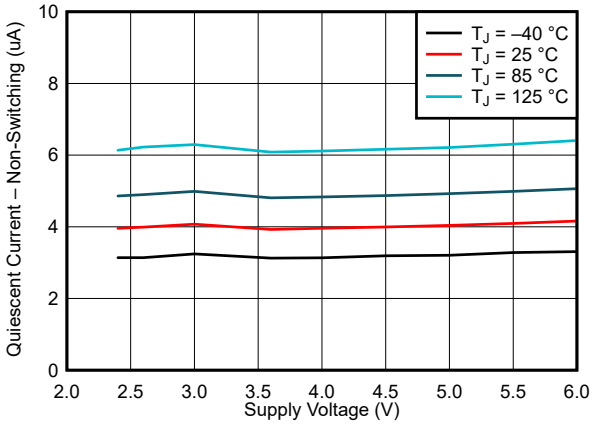


図 7-3. Quiescent Current

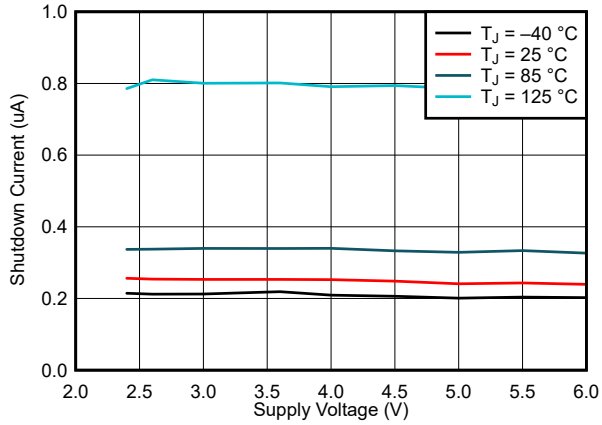


図 7-4. Shutdown Current

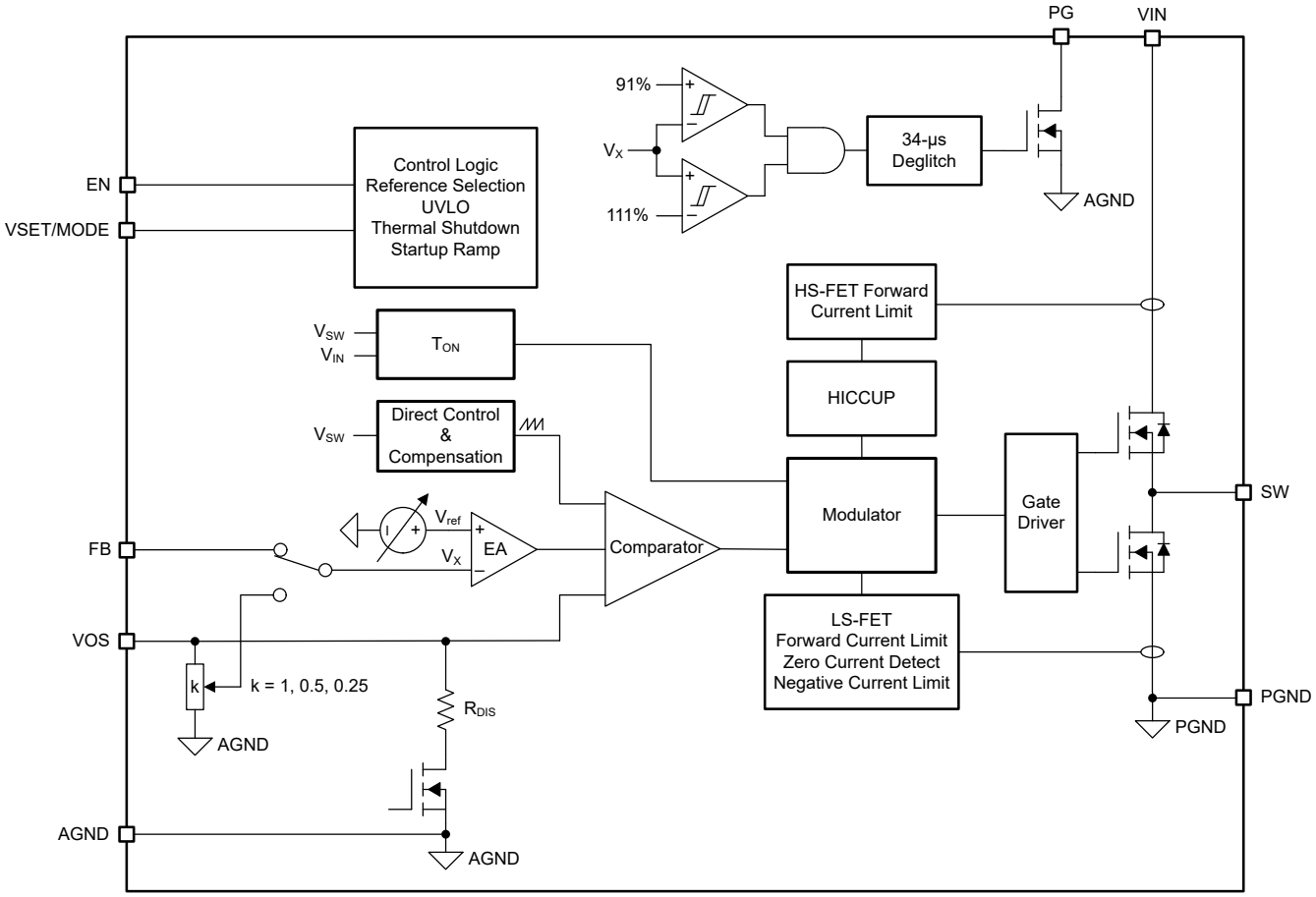
8 Detailed Description

8.1 Overview

The TPS62865 and TPS62867 synchronous step-down converters use the DCS-Control (Direct Control with Seamless transition into Power Save Mode) topology. This is an advanced regulation topology that combines the advantages of hysteretic and current-mode control schemes.

The DCS-Control topology operates in PWM (pulse width modulation) mode for medium to heavy load conditions and in Power Save Mode at light load currents. In PWM mode, the converter operates with its 2.4-MHz nominal switching frequency, having a controlled frequency variation over the input voltage range. Since DCS-Control supports both operation modes (PWM and PFM) within a single building block, the transition from PWM mode to Power Save Mode is seamless and does not affect on the output voltage. The devices offer both excellent DC voltage and superior load transient regulation combined with very low output voltage ripple.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power Save Mode

As the load current decreases, the device enters Power Save Mode (PSM) operation. PSM occurs when the inductor current becomes discontinuous, which is when it reaches 0 A during a switching cycle. Power Save Mode is based on a fixed on-time architecture, as shown in 式 1.

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 416\ ns \tag{1}$$

In Power Save Mode, the output voltage rises slightly above the nominal output voltage. This effect is minimized by increasing the output capacitor or inductor value.

When V_{IN} decreases to typically 15% above V_{OUT}, the TP6286x does enter Power Save Mode, regardless of the load current. The device maintains output regulation in PWM mode.

8.3.2 Forced PWM Mode

Connecting the VSET/MODE pin to logic high after the start-up, the device switches at 2.4 MHz, even with a light load. This reduces the output voltage ripple and allows simple filtering of the switching frequency for noise-sensitive applications. Efficiency at light load is lower in Forced PWM mode (FPWM).

8.3.3 100% Duty Cycle Mode Operation

There is no limitation for small duty cycles since even at very low duty cycles, the switching frequency is reduced as needed to always ensure a proper regulation.

If the output voltage level comes close to the input voltage, the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. The difference between V_{IN} and V_{OUT} is determined by the voltage drop across the high-side MOSFET and the DC resistance of the inductor. The minimum V_{IN} that is needed to maintain a specific V_{OUT} value is estimated as:

$$V_{IN,MIN} = V_{OUT} + (R_{DS(ON)} + R_L) I_{OUT,MAX} \quad (2)$$

where

- $V_{IN,MIN}$ is the minimum input voltage to maintain an output voltage
- $I_{OUT,MAX}$ is the maximum output current
- $R_{DS(on)}$ is the high-side FET ON-resistance
- R_L is the inductor ohmic resistance (DCR)

8.3.4 Soft Start

After enabling the device, there is a 700-µs (typical) enable delay (t_{delay}) before the device starts switching. After the enable delay, an internal soft start-up circuitry ramps up the output voltage with a period of 1 ms (t_{Ramp}). This avoids excessive inrush current and creates a smooth output voltage rise-slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to start into a pre-biased output capacitor. It starts with the applied bias voltage and ramps the output voltage to its nominal value.

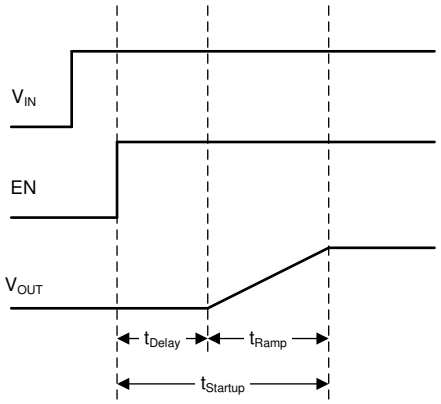


図 8-1. Start-up Sequence

8.3.5 Switch Current Limit and HICCUP Short-Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold I_{LIM}, cycle by cycle, the high-

side MOSFET is turned off and the low-side MOSFET is turned on, while the inductor current ramps down to the low-side MOSFET current limit.

When the high-side MOSFET current limit is triggered 32 times, the device stops switching. The device then automatically re-starts with an internal soft start-up after a typical delay time of 128 µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

8.3.6 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, undervoltage lockout (UVLO) is implemented when the input voltage is lower than V_{UVLO}. The device stops switching and the output voltage discharge is active when the device is in UVLO. When the input voltage recovers, the device automatically returns to operation with an internal soft start-up.

8.3.7 Thermal Shutdown

When the junction temperature exceeds T_{JSD}, the device goes into thermal shutdown, stops switching, and activates the output voltage discharge. When the device temperature falls below the threshold by the hysteresis, the device returns to normal operation automatically with an internal soft start-up. During thermal shutdown, the internal register values are kept.

8.4 Device Functional Modes

8.4.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic high. In shutdown mode (EN = low), the internal power switches and the entire control circuitry are turned off. An internal switch smoothly discharges the output through the VOS pin in shutdown mode. Do not leave the EN pin floating.

8.4.2 Power Good (PG)

The device has an open-drain power-good pin, which is specified to sink up to 1 mA. The power-good output requires a pullup resistor connecting to any voltage rail less than 5.5 V. The PG has a deglitch delay of 34 µs.

The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

表 8-1. PG Function Table

DEVICE CONDITIONS		PG PIN
Enable	$0.9 \times V_{OUT\_NOM} \le V_{VOS} \le 1.1 \times V_{OUT\_NOM}$	Hi-Z
	$V_{VOS} < 0.9 \times V_{OUT\_NOM}$ or $V_{VOS} > 1.1 \times V_{OUT\_NOM}$	Low
Shutdown	EN = low	Low
Thermal shutdown	$T_J > T_{JSD}$	Low
UVLO	$1.8\ V < V_{IN} < V_{UVLO}$	Low
Power supply removal	$V_{IN} < 1.8\ V$	Undefined

8.4.3 Voltage Setting and Mode Selection (VSET/MODE)

During the enable delay (t_{Delay}), the device configuration is set by an external resistor connected to the VSET/MODE pin through an internal R2D (resistor to digital) converter. 表 8-2 shows the options.

The R2D converter has an internal current source that applies current through the external resistor and an internal ADC that reads back the resulting voltage level. Depending on the level, the output voltage is set. Once this R2D conversion is finished, the current source is turned off to avoid current flowing through the external resistor. Ensure that there is no additional current path or capacitance greater than 30 pF from this pin to GND during R2D conversion. Otherwise, a false value is set.

表 8-2. Voltage Selection Table

RESISTOR (E96 SERIES, ±1% ACCURACY) AT VSET/MODE PIN	FIXED OR ADJUSTABLE OUTPUT VOLTAGE
249 kΩ or logic high	adjustable
205 kΩ	3.30 V
162 kΩ	2.50 V
133 kΩ	1.80 V
105 kΩ	1.50 V
86.6 kΩ	reserved
68.1 kΩ	1.35 V
56.2 kΩ	1.20 V
44.2 kΩ	1.10 V
36.5 kΩ	1.05 V
28.7 kΩ	1.00 V
23.7 kΩ	0.95 V
18.7 kΩ	0.90 V
15.4 kΩ	0.85 V
12.1 kΩ	0.80 V
10 kΩ or logic low	adjustable

When the device is set as a fixed output voltage converter, then FB pin must be connected to the output directly. Refer to 図 8-2.

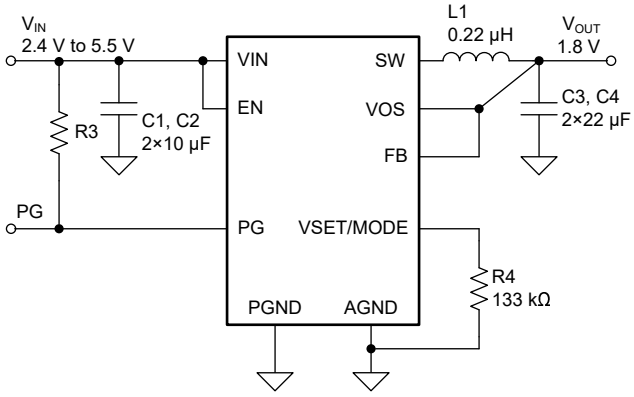


図 8-2. Fixed Start-up Output Voltage Application Circuit

After the start-up period ($t_{Startup}$), a different operation mode can be selected. When VSET/MODE is high, the device operates in forced PWM mode, otherwise the device operates in power save mode.

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。また、お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

9.2 Typical Application

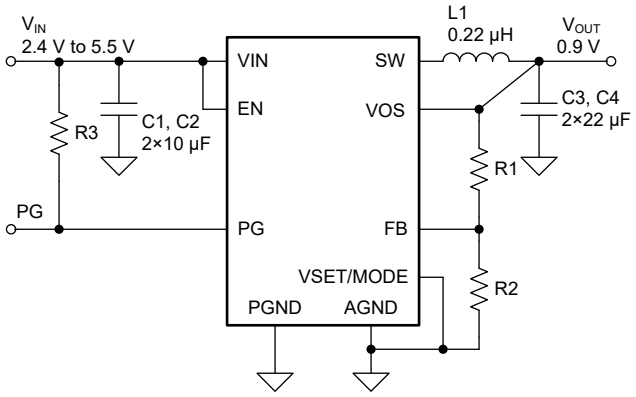


図 9-1. Typical Application

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as the input parameters.

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	2.4 V to 5.5 V
Output voltage	0.9 V
Maximum output current	6 A

表 9-2 lists the components used for the example.

表 9-2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER(1)
C1, C2	10 µF, ceramic capacitor, 10 V, X7R, size 0603,GRM188Z71A106KA73	Murata
C3, C4	22 µF, ceramic capacitor, 6.3 V, X7R, size 0805, GRM21BZ70J226ME44	Murata
L1	0.22 µH, power inductor, XAL4020-221ME (12 A, 5.81 mΩ)	Coilcraft
R1	Depending on the output voltage, chip resistor, 1/16 W, 1%, size 0402	Std
R2	100 kΩ, chip resistor, 1/16 W, 1%, size 0402	Std
R3	100 kΩ, chip resistor, 1/16 W, 1%, size 0402	Std

(1) See the *Third-party Products* disclaimer.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62865 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62867 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting The Output Voltage

The output voltage is set by an external resistor divider according to 式 3:

$$R1 = R2\left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2\left(\frac{V_{OUT}}{0.6\ V} - 1\right) \quad (3)$$

R2 must not be higher than 200 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity.

For the fixed output versions, connect the FB pin to the output. R1 and R2 are not needed.

9.2.2.3 Output Filter Design

The inductor and the output capacitor together provide a low-pass filter. To simplify this process, 表 9-3 outlines possible inductor and capacitor value combinations for most applications. Checked cells represent combinations that are proven for stability by simulation and lab testing. Further combinations must be checked for each individual application.

表 9-3. Matrix of Output Capacitor and Inductor Combinations

NOMINAL L [µH](2)	NOMINAL C_{OUT} [µF](3)			
	10	2 × 22 or 47	3 × 22	150
0.22		+(1)	+	+

(1) This LC combination is the standard value and recommended for most applications.
(2) Inductor tolerance and current derating is anticipated. The effective inductance can vary by 20% and –30%.
(3) Capacitance tolerance and bias voltage derating is anticipated. The effective capacitance can vary by 20% and –50%.

9.2.2.4 Inductor Selection

The main parameter for the inductor selection is the inductor value, then the saturation current of the inductor. To calculate the maximum inductor current under static load conditions, 式 4 is given.

$$I_{L,MAX} = I_{OUT,MAX} + \frac{\Delta I_L}{2}$$

$$\Delta I_L = V_{OUT}\left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f_{SW}}\right) \quad (4)$$

where

- $I_{OUT,MAX}$ is the maximum output current
- ΔI_L is the inductor current ripple
- f_{SW} is the switching frequency
- L is the inductor value

It is recommended to choose a saturation current for the inductor that is approximately 20% to 30% higher than $I_{L,MAX}$. In addition, DC resistance and size must also be taken into account when selecting an appropriate inductor. 表 9-4 lists recommended inductors.

表 9-4. List of Recommended Inductors

INDUCTANCE [µH](1)	CURRENT RATING [A]	DIMENSIONS [L × W × H mm]	DC RESISTANCE [mΩ]	PART NUMBER
0.22	18.7	4 × 4 × 2	5.81	Coilcraft, XAL4020-221ME
0.24	6.6	2 × 1.6 × 1.2	13	Murata, DFE201612E-R24M

(1) See the *Third-party Products* disclaimer.

9.2.2.5 Capacitor Selection

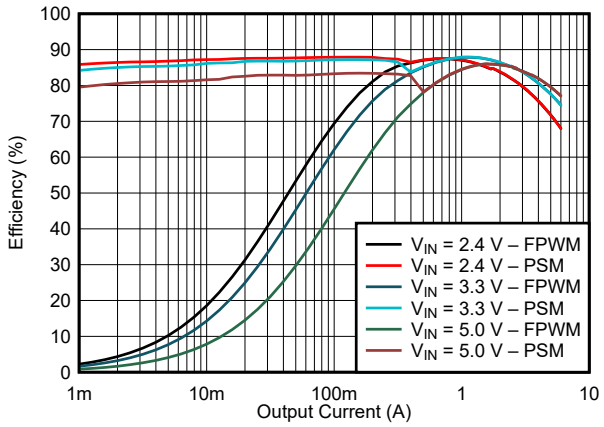
The input capacitor is the low-impedance energy source for the convertersm which helps to provide stable operation. A low-ESR multilayer ceramic capacitor is recommended for the best filtering and must be placed between VIN and GND as close as possible to those pins. For most applications, 8 µF of *effective* [1] capacitance is sufficient, however, a larger value reduces input current ripple.

The architecture of the device allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, TI recommends using X7R or X5R dielectrics. The recommended typical output capacitor value is 30 µF of *effective* [1] capacitance. This capacitance can vary over a wide range as outlined in the output filter selection table.

[1] The effective capacitance is the capacitance after tolerance, temperature, and DC bias effects have been considered.

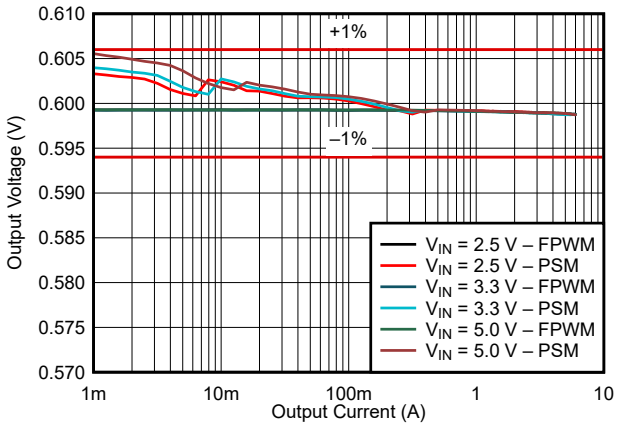
9.2.3 Application Curves

V_{IN} = 5.0 V, V_{OUT} = 0.9 V, T_A = 25 °C, BOM = 表 9-2, unless otherwise noted.



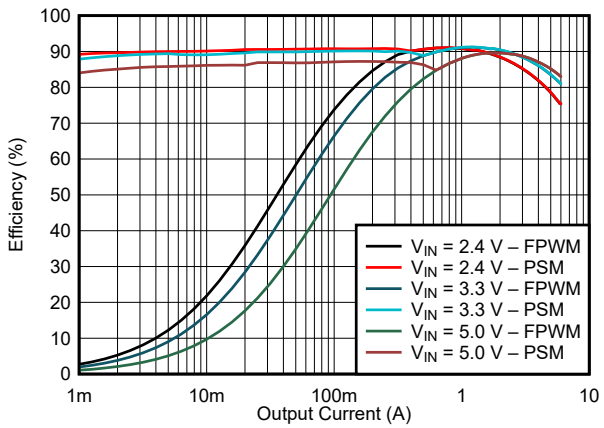
V_{OUT} = 0.6 V

図 9-2. Efficiency



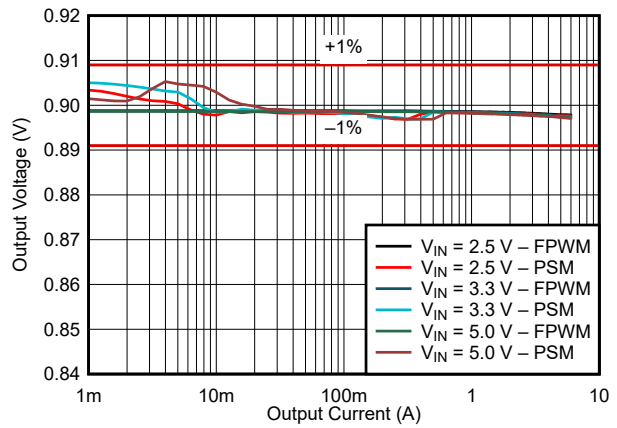
V_{OUT} = 0.6 V

図 9-3. Load Regulation



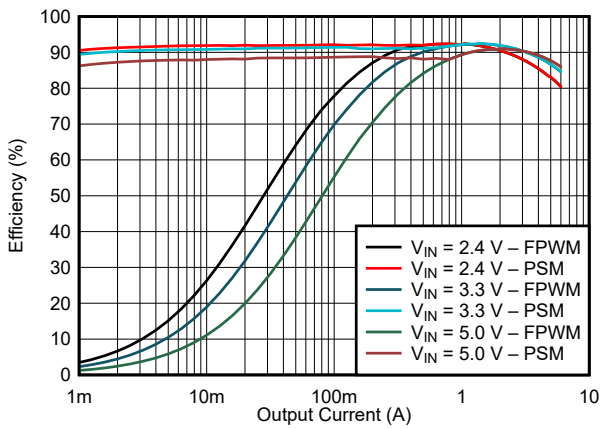
V_{OUT} = 0.9 V

図 9-4. Efficiency



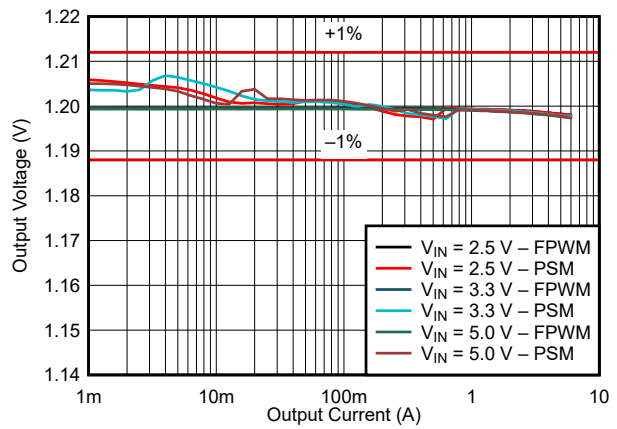
V_{OUT} = 0.9 V

図 9-5. Load Regulation



V_{OUT} = 1.2 V

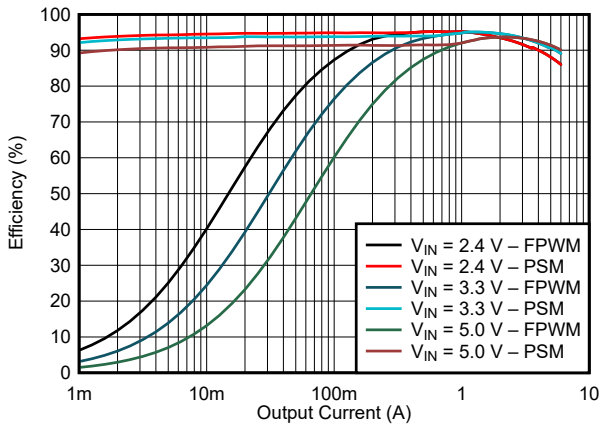
図 9-6. Efficiency



V_{OUT} = 1.2 V

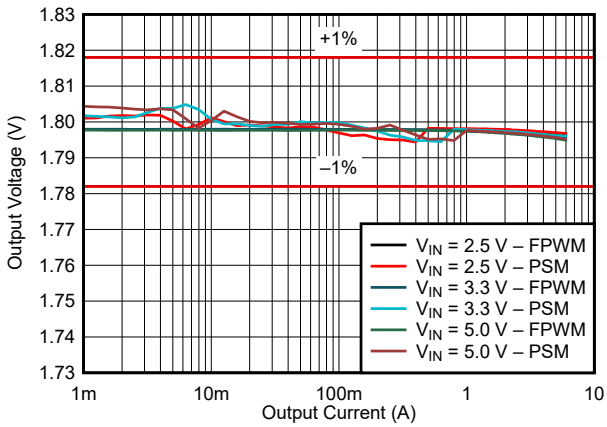
図 9-7. Load Regulation

9.2.3 Application Curves (continued)



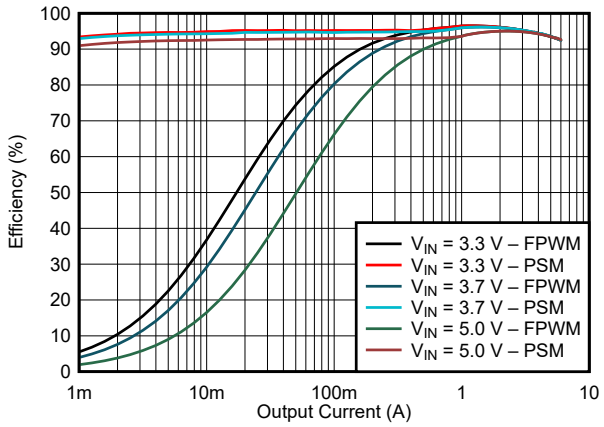
V_{OUT} = 1.8 V

図 9-8. Efficiency



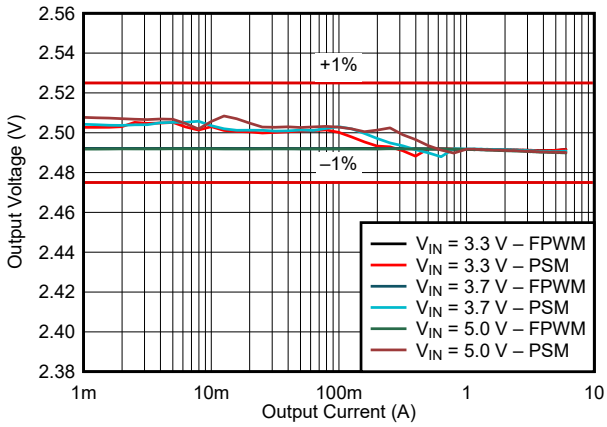
V_{OUT} = 1.8 V

図 9-9. Load Regulation



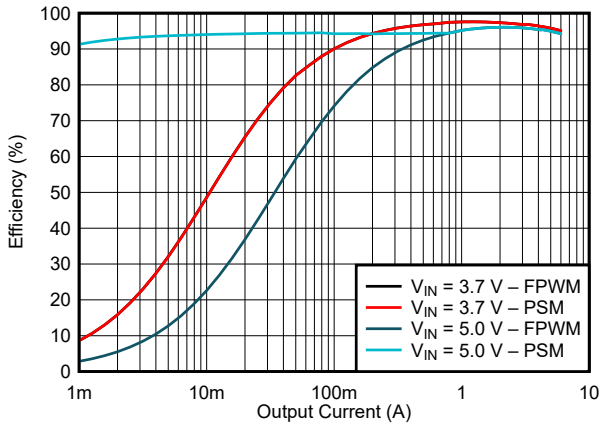
V_{OUT} = 2.5 V

図 9-10. Efficiency



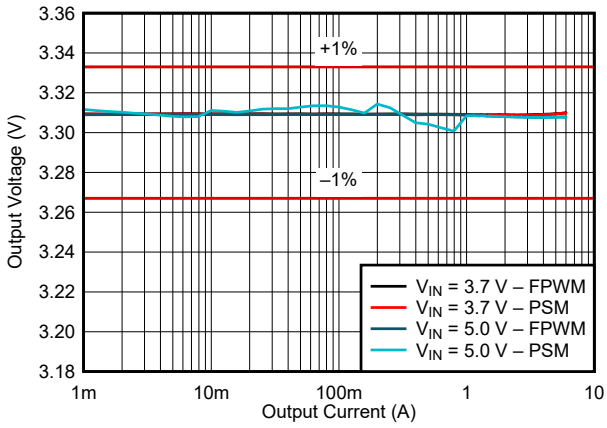
V_{OUT} = 2.5 V

図 9-11. Load Regulation



V_{OUT} = 3.3 V

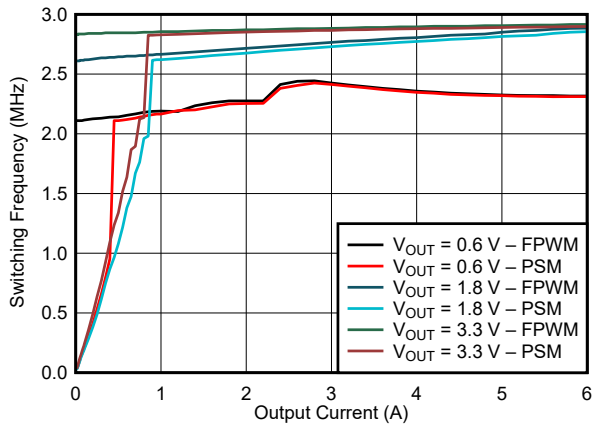
図 9-12. Efficiency



V_{OUT} = 3.3 V

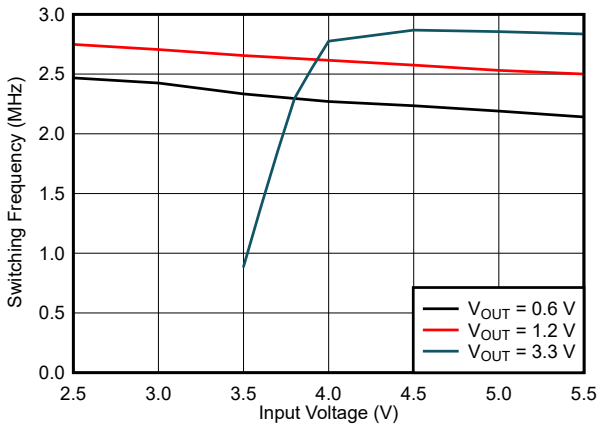
図 9-13. Load Regulation

9.2.3 Application Curves (continued)



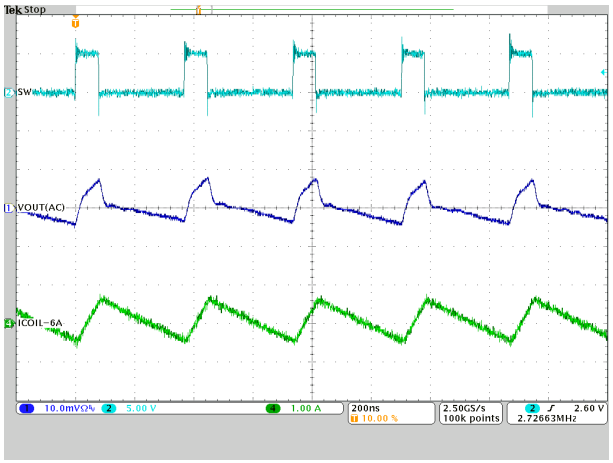
V_{IN} = 5 V

図 9-14. Switching Frequency



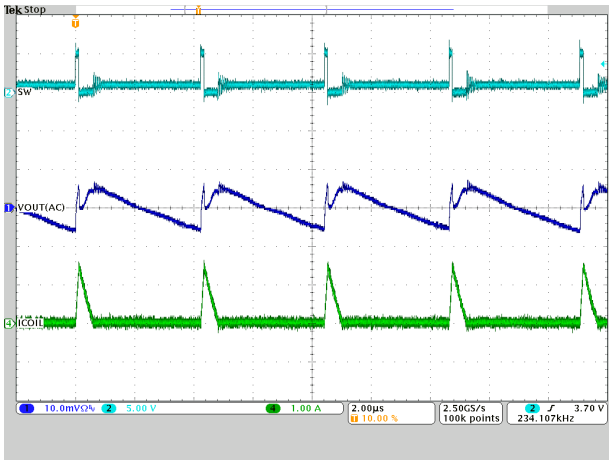
I_{OUT} = 1 A

図 9-15. Switching Frequency



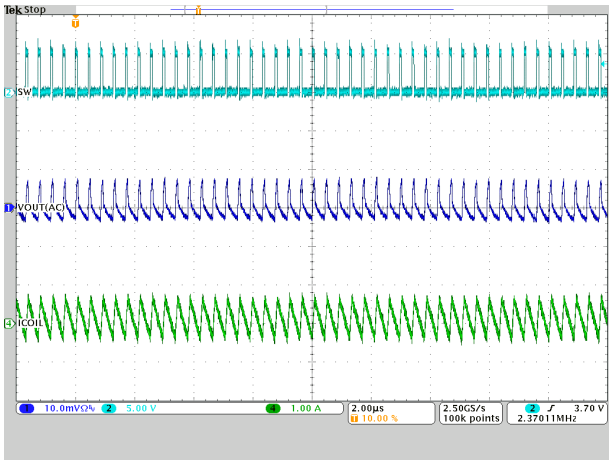
I_{OUT} = 6 A

図 9-16. PWM Operation



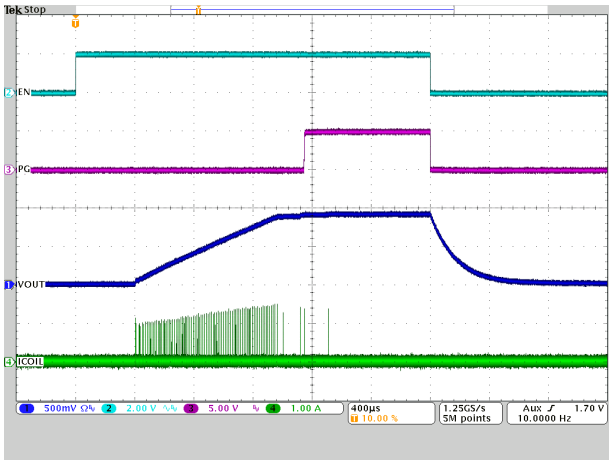
I_{OUT} = 0.1 A

図 9-17. PSM Operation



I_{OUT} = 0.1 A

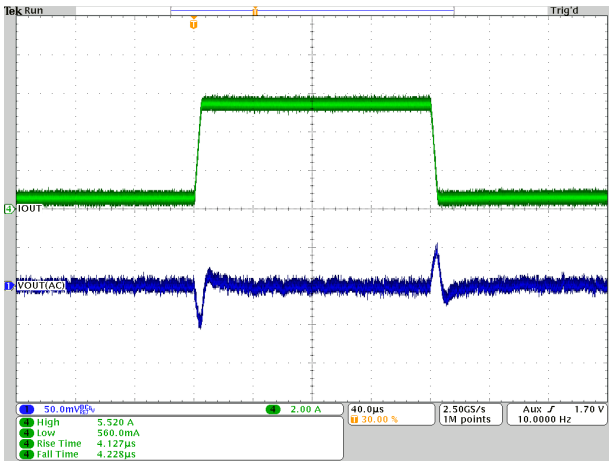
図 9-18. Forced-PWM Operation



No Load

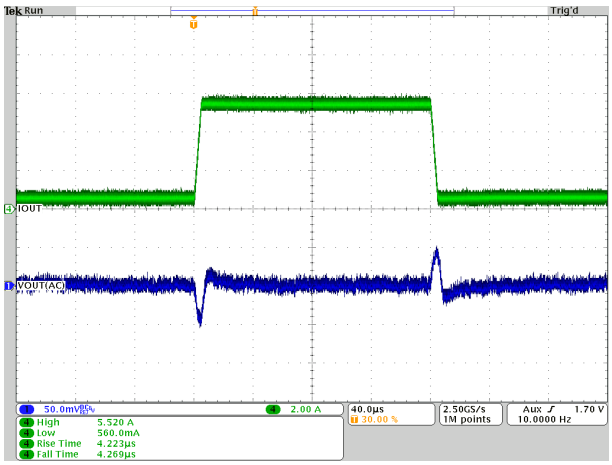
図 9-19. Startup with No-Load

9.2.3 Application Curves (continued)



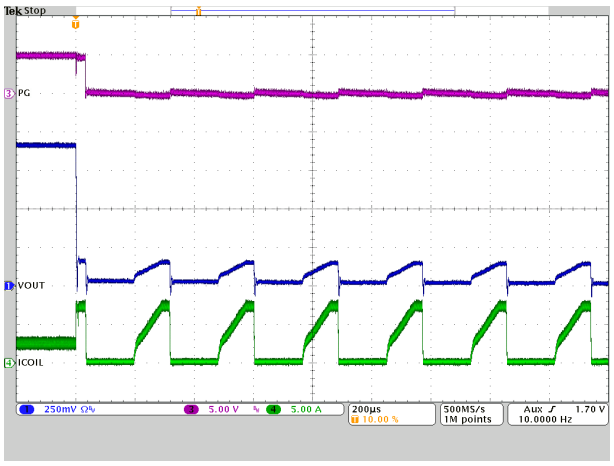
I_{OUT} = 0.6 A to 5.4 A

図 9-20. Load Transient - PWM Operation



I_{OUT} = 0.6 A to 5.4 A

図 9-21. Load Transient - PSM Operation



I_{OUT} = 1 A

図 9-22. HICCUP Short Circuit Protection

10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.4 V to 5.5 V. Ensure that the input power supply has a sufficient current rating for the application.

11 Layout

11.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. The PCB layout of the TPS62865 and TPS62867 devices requires careful attention to ensure best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* technical brief for a detailed discussion of general best practices. The following are specific recommendations for the TPS62865 and TPS62867:

- The input capacitor or capacitors must be placed as close as possible to the VIN and PGND pins of the device. This is the most critical component placement. Route the input capacitor or capacitors directly to the VIN and PGND pins, avoiding vias.
- Place the output inductor close to the SW pins. Minimize the copper area at the switch node.
- Place the output capacitor or capacitors ground close to the PGND pin and route it directly, avoiding vias. Minimize the length of the connection from the inductor to the output capacitor. Connect the VOS pin directly to the output capacitor.
- Sensitive traces, such as the connections to the VOS, FB, and VSEL pins, must be connected with short traces and be routed away from any noise source, such as the SW pin.
- Make the connections from the input voltage of the system and the connection to the load as wide as possible to minimize voltage drops.
- Have a solid ground plane between PGND and the input and output capacitor ground connections.
- The sensitive signal ground connections for the feedback voltage divider must be connected to a separate signal ground trace.

11.2 Layout Example

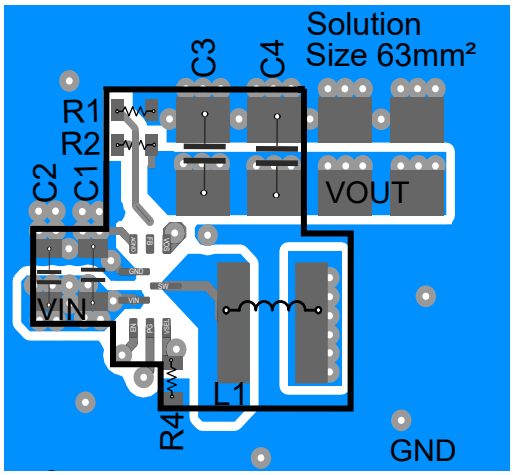


図 11-1. Layout Example

11.2.1 Thermal Considerations

After the layout recommendations for component placement and routing have been followed, the PCB design must focus on thermal performance. Thermal design is important and must be considered to remove the heat generated in the device during operation. The device junction temperature must stay below its maximum rated temperature of 125°C for correct operation.

Use wide traces and planes, especially to the PGND, VIN, and VOUT pins, and use vias to internal planes to improve the power dissipation capability of the design. If the application allows it, use airflow in the system to further improve cooling.

The *Thermal Information* table provides the thermal parameters of the device and its package based on the JEDEC standard 51-7. See the *Semiconductor and IC Package Thermal Metrics* application report for a detailed

explanation of each parameter. In addition to the JEDEC standard, the thermal information table also contains the thermal parameters of the EVM. The EVM better reflects a real-world PCB design with thicker traces connecting to the device.

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.1.2 Development Support

12.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS62865 device with the WEBENCH® Power Designer.

Click here to create a custom design using the TPS62867 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report

12.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

12.6 用語集

TI 用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62865RQYR	ACTIVE	VQFN-HR	RQY	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2EAH	Samples
TPS62867RQYR	ACTIVE	VQFN-HR	RQY	9	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2DWH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

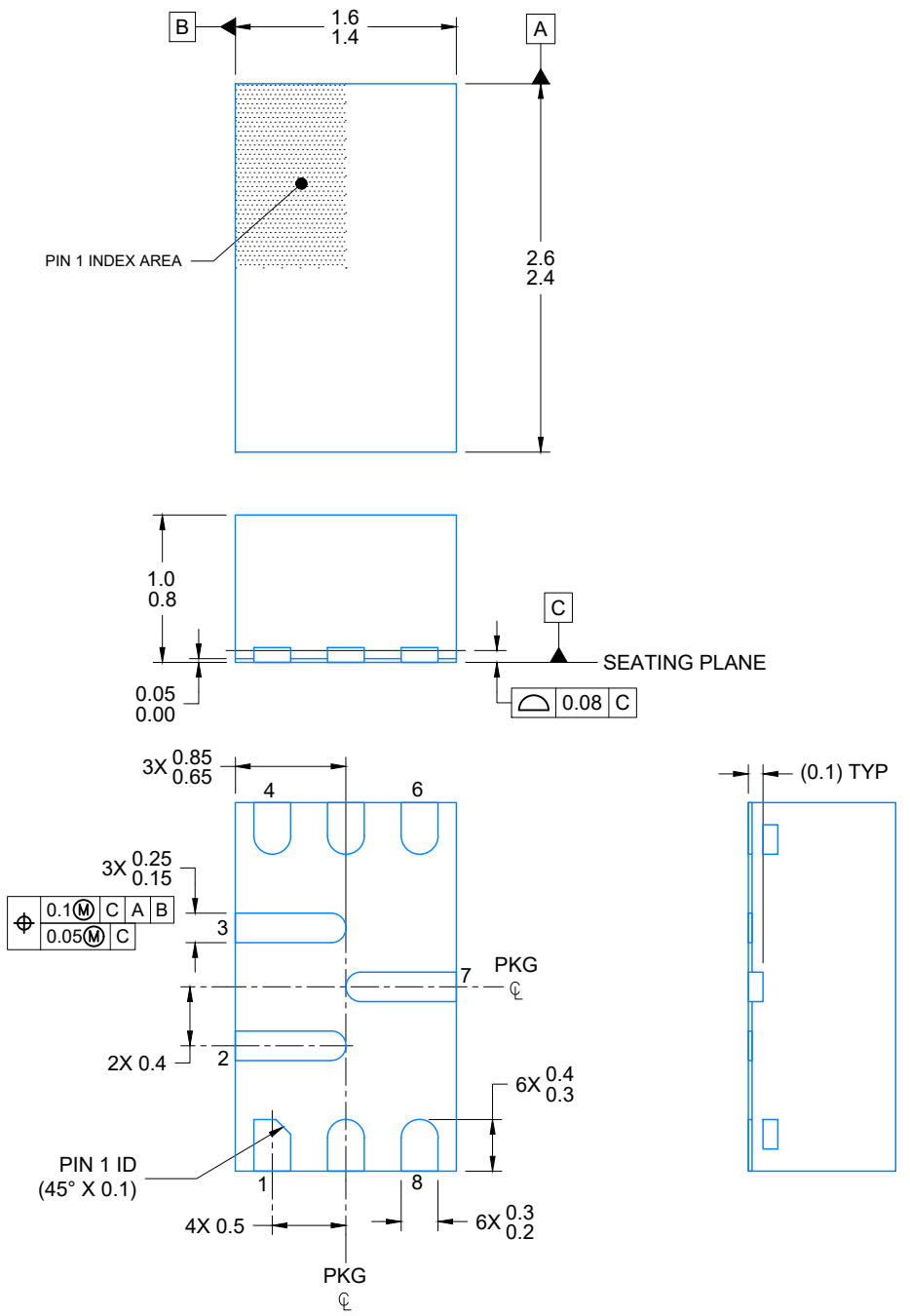
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RQY0009A

VQFN-HR - 1 mm max height

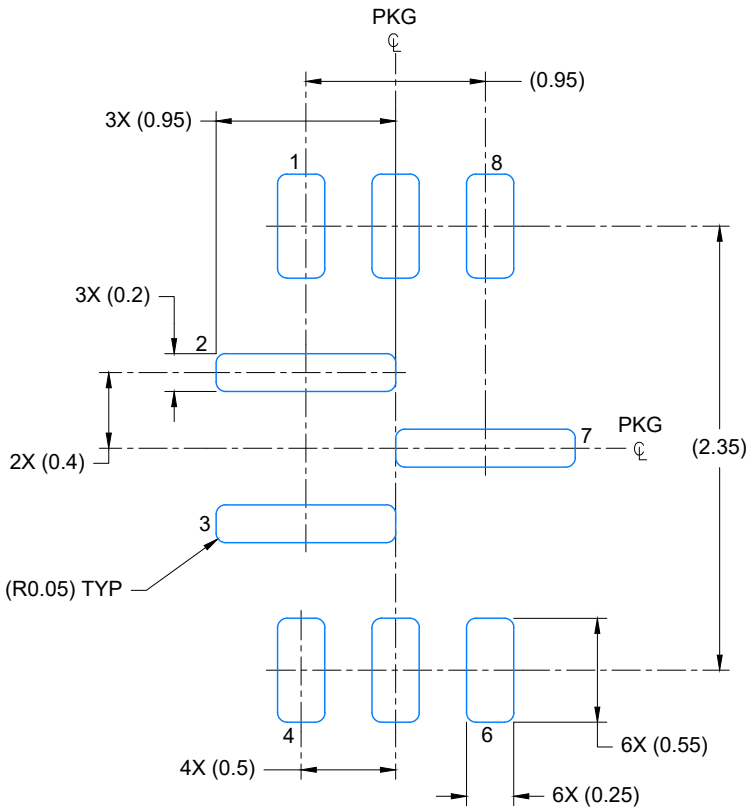
PLASTIC QUAD FLATPACK- NO LEAD



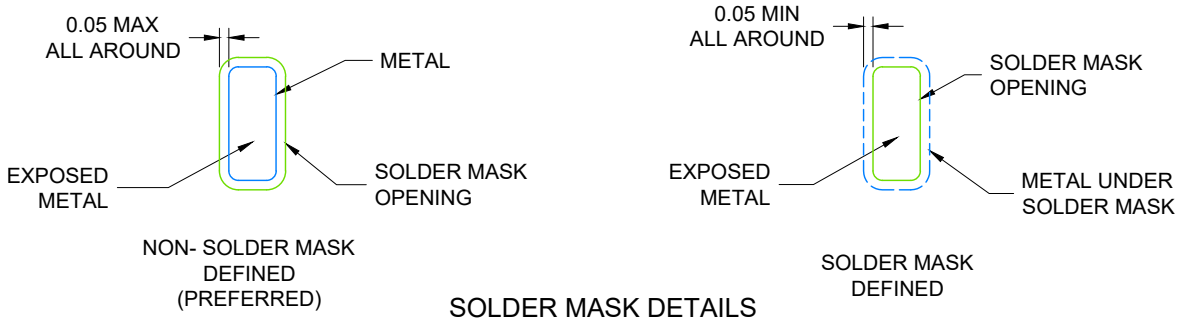
4225639/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

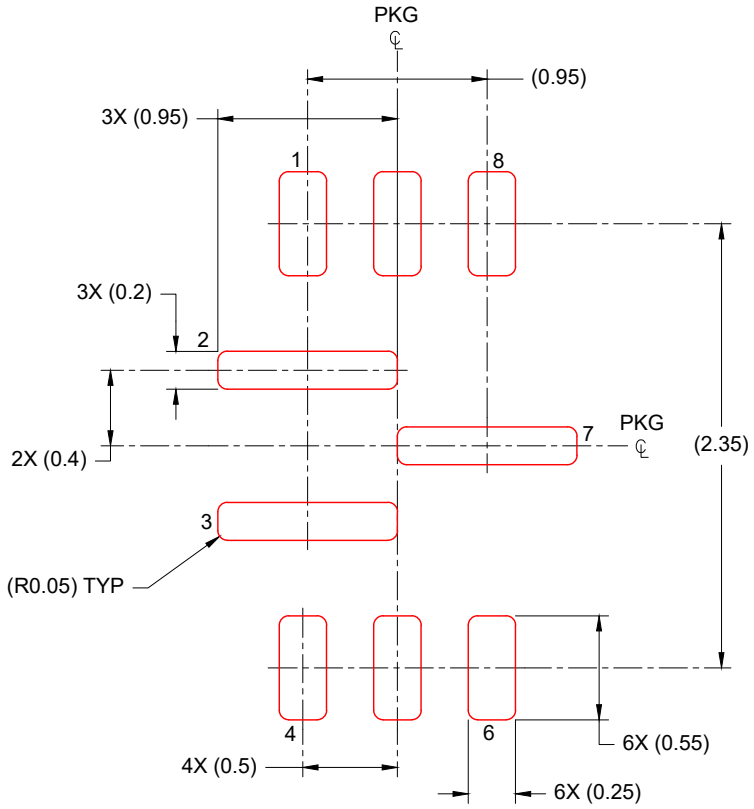


SOLDER MASK DETAILS
NOT TO SCALE

4225639/A 03/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1mm THICK STENCIL
SCALE: 25X

4225639/A 03/2020

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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