参考資料

TPS62843 1.8V～5.5V、600mA、275nA I_Q、小型の降圧型コンバータ

1 特長

- 入力電圧範囲：1.8V～5.5V
- 出力電圧範囲：0.4V ～ 3.6V
- 静止電流：275nA (代表値)
- 出力電流：600mA
- 出力電圧精度：1%
- シャットダウン電流：4nA (代表値)
- 出力放電
- VSET ピンでは 1 つの抵抗により出力電圧を選択可能
  - TPS628436：0.4V～0.8V
  - TPS628437：0.8V～1.8V
  - TPS628438：1.8V～3.6V
- 小型のパッシブ部品向けに設計
  - 1µH インダクタ
  - 4µF C_{OUT} の実効容量まで最小化
- 高い PSRR (最大 83dB)
- パワー セーブ モードでは小さい出力電圧リップル
- RF フレンドリで高速過渡の DCS-Control
- リップルなし 100% モードへの自動遷移
- 0603 インダクタと 0402 コンデンサ サイズに対応
- 小型 6 ピン、サイズ 0.84mm² の 0.35mm ピッチ WCSP パッケージ
- WCSP パッケージ封止の TPS6280x ファミリとピン互換 (1A)
- 1.60mm × 1.60mm の SOT563 パッケージで供給

2 アプリケーション

- ウェアラブル電子機器
- ヘッドセット、ヘッドホン、小型イヤホン
- 携帯電話 / スマートフォン
- 医療用センサ・パッチ
- 補聴器

3 概要

TPS62843 は、静止電流が 275nA (代表値) と非常に小さい、高効率の降圧コンバータ ファミリです。ディセーブル時のシャットダウン電流は 4nA (代表値) です。

このデバイスは、RF フレンドリな低い出力電圧リップルを備えた DCS-Control を使用して、無線機に電力を供給します。

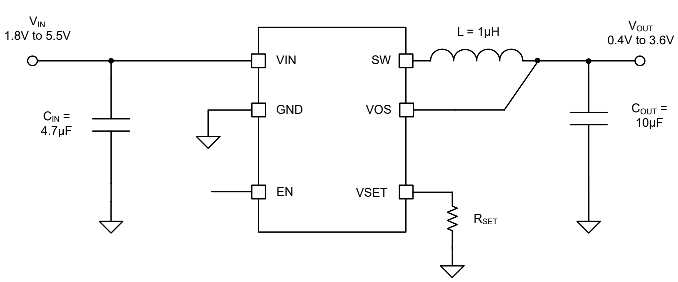
このデバイスは標準スイッチング周波数 1.5MHz で動作し、負荷電流が 100µA 以下のときまで軽負荷時の高効率が維持されます。

VSET ピンに抵抗を接続することで、3 × 18 の事前定義された出力電圧を選択できるため、本ファミリは最小限のパッシブ部品の組み合わせだけで、さまざまなアプリケーションに使用できます。

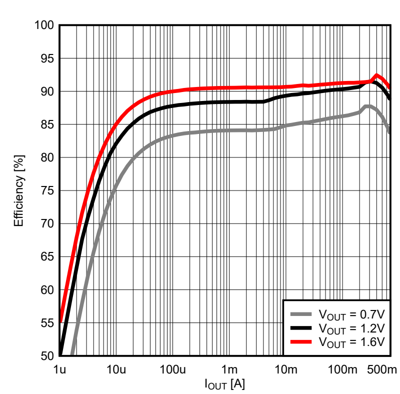
製品情報

部品番号(2)	V_{OUT} 範囲	パッケージ(1)	本体サイズ (公称)
TPS628436	0.4V～0.8V	YKA (DSBGA、6)	0.80mm × 1.05mm × 0.40mm
TPS628437	0.8V～1.8V		
TPS628438	1.8V～3.6V		
TPS628436	0.4V～0.8V	DRL (SOT563、6)	1.6mm × 1.6mm × 0.6mm
TPS628437	0.8V～1.8V		
TPS628438	1.8V～3.6V		

(1) 詳細については、セクション 11 を参照してください。
(2) 「製品比較」表を参照してください。



代表的なアプリケーション



$3.6V_{IN}$ での出力電流と効率の関係

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4 Device Comparison Table

Device	Fixed V_{OUT} VSET = GND	Selectable Output Voltages	f_{SW} [MHz]	Soft Start t_{SS}	Inductor
TPS628436	1.0V	0.4V – 0.8V in 25mV steps	1.5	400µs	1µH
TPS628437	1.8V	0.8V – 1.6V in 50mV steps	1.5	800µs	1µH
TPS628438	3.6V	1.8V – 3.4V in 100mV steps	1.5	800µs	1µH

5 Pin Configuration and Functions

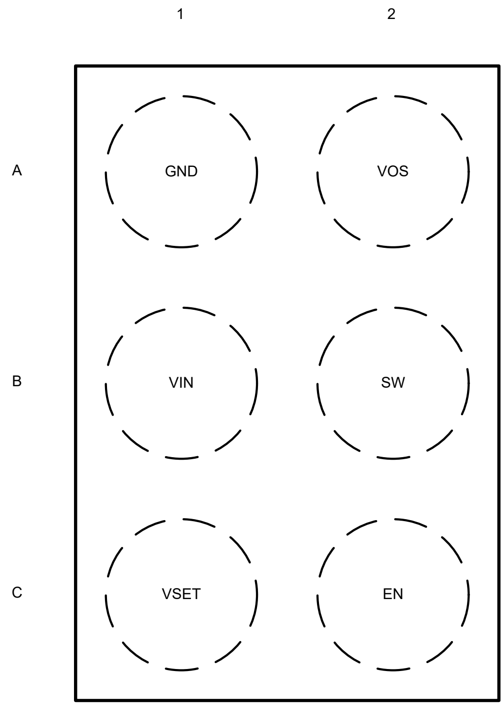


図 5-1. 6-Pin DSBGA YKA Package (Top View)

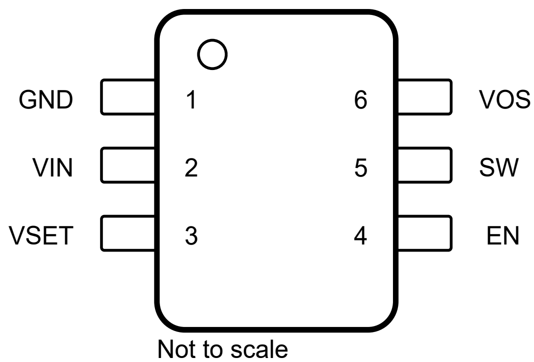


図 5-2. 6-Pin DRL SOT563 Package (Top View)

表 5-1. Pin Functions

PIN NUMBER			TYPE	DESCRIPTION
NAME	SOT563	DSBGA		
GND	1	A1	PWR	GND supply pin. Connect this pin close to the GND terminal of the input and output capacitor.
VIN	2	B1	PWR	V_{IN} power supply pin. Connect the input capacitor close to this pin for best noise and voltage spike suppression. A ceramic capacitor is required.
VSET	3	C1	I	Connecting a resistor to GND selects a pre-defined output voltage.
VOS	6	A2	I	Output voltage sense pin for the internal feedback divider network and regulation loop. This pin also discharges V_{OUT} by an internal MOSFET when the converter is disabled. Connect this pin directly to the output capacitor with a short trace.
SW	5	B2	O	The switch pin is connected to the internal MOSFET switches. Connect the inductor to this terminal.
EN	4	C2	I	A high level enables the devices and a low level turns the device off. The pin features an internal pulldown resistor, which is disabled once the device has started up.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN	-0.3	6	V
Pin voltage	SW, DC	-0.3	V_{IN}+0.3V	V
Pin voltage	SW, transient < 10 ns, while switching	-2.5	9	V
Pin voltage	VSET	-0.3	6	V
Pin voltage	EN	-0.3	6	V
Pin voltage	VOS	-0.3	5	V
T_J	Operating junction temperature	-40	150	°C
T_{stg}	Storage temperature	-55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage V_{IN}	1.8		5.5	V
I_{OUT}	Output current			0.6	A
L	Effective inductance	0.7	1.0	1.2	µH
C_{OUT}	Effective output capacitance	4		25	µF
C_{IN}	Effective input capacitance	0.5	4.7		µF
C_{VSET}	External parasitic capacitance at VSET pin			30	pF
R_{SET}	Resistance range for external resistor at VSET pin (E96 1% resistor values)	10		249	kΩ
	External resistor tolerance E96 series at VSET pin			1%	
	E96 resistor series temperature coefficient (TCR)	-200		+200	ppm/°C
T_J	Operating junction temperature range	-40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		YKA (DSBGA) 6 PINS	DRL (SOT563) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.7	138.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.7	57.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	47.5	24.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	1.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	47.6	24.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	–	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{IN} = 1.8V to 5.5V. Typical values are at T_J = 25°C, V_{IN} = 3.6V and V_{OUT} = 0.7V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating Quiescent Current (Power Save Mode)	Non-switching, V_{EN} = V_{IN}, I_{OUT} = 0µA, T_J = -40°C to 85°C		275	1500	nA
		Switching, V_{EN} = V_{IN}, I_{OUT} = 0µA, V_{OUT} = 0.7V		350		nA
I_{SD}	Shutdown Current	V_{EN} = 0V, VSET = GND, T_J = -40°C to 85°C		4	850	nA
UVLO						
$V_{UVLO(R)}$	Undervoltage Lockout Rising Threshold	V_{IN} rising, I_{OUT} = 0µA		1.75	1.8	V
$V_{UVLO(F)}$	Undervoltage Lockout Falling Threshold	V_{IN} falling, I_{OUT} = 0µA		1.65	1.7	V
$V_{UVLO(H)}$	Undervoltage Lockout Hysteresis			100		mV
VSET PIN						
$V_{SET(LKG)}$	VSET Input leakage current	T_J = -40°C to 85°C		10	800	nA
$V_{SET(H)}$	VSET High-level detection	Voltage at VSET during startup	1.0			V
R_{SET}	RSET accuracy	T_J = -20°C to 125°C	-4		4	%
R_{SET}	RSET accuracy	T_J = -40°C to 125°C	-3.5		3.5	%
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	0.8			V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching			0.4	V
$V_{EN(LKG)}$	EN Input leakage current	V_{EN} > 0.8V, T_J = -40°C to 85°C		1	25	nA
$R_{EN;PD}$	EN internal pull-down resistance	EN pin to GND	425	500		kΩ
VOUT VOLTAGE						
V_{OUT}	DC Output voltage accuracy	PWM operation, T_J = -20°C to 125°C	-1		+1	%
V_{OUT}	DC Output voltage accuracy	PWM operation, T_J = -40°C to 125°C	-1.5		+1.5	%
V_{OUT}	TPS628436		0.4		0.8	V
	TPS628437		0.8		1.8	V
	TPS628438		1.8		3.6	V
$I_{VOS(LKG)}$	VOS input leakage current	TPS628436, V_{EN} = V_{IN}, V_{VOS} = 0.7V, T_J = -40°C to 85°C			100	nA
		TPS628437, V_{EN} = V_{IN}, V_{VOS} = 1.2V, T_J = -40°C to 85°C		100	250	nA
		TPS628438, V_{EN} = V_{IN}, V_{VOS} = 3.3V, T_J = -40°C to 85°C		275	450	nA
f_{SW}		I_{OUT} = 400mA		1.5		MHz
STARTUP						

6.5 Electrical Characteristics (続き)

T_J = –40°C to +125°C, V_{IN} = 1.8V to 5.5V. Typical values are at T_J = 25°C, V_{IN} = 3.6V and V_{OUT} = 0.7V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SS}	TPS628436 soft-start time	From V_{OUT}= 0% to V_{OUT}= 95% of V_{OUT} nominal		0.45	0.6	ms
	TPS628438 soft-start time			1.0	1.4	
	TPS628437 soft-start time			0.7	1.0	
$t_{Startup\_delay}$	EN HIGH to start of switching delay	R2D = GND		330	560	µs
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	V_{IN} = 3.6V, I_{OUT} = 300mA		170	260	mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6V, I_{OUT} = 300mA		70	115	mΩ
ILKG_SW	Leakage Current into SW-Pin	V_{SW} = 0.7V, T_J = -40°C to 85°C		0	35	nA
ILKG_SW	Leakage Current into SW-Pin	V_{SW} = 1.2V, T_J = -40°C to 85°C		0	45	nA
ILKG_SW	Leakage Current into SW-Pin	$V_{VIN} > V_{SW}$, V_{SW} = 3.3V, T_J = -40°C to 85°C		0	45	nA
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	V_{IN} ≧ 2.2V	0.9	1.1	1.3	A
$I_{LS(OC)}$	Low-side valley current limit	V_{IN} ≧ 2.2V	0.79	1.0	1.11	A
OUTPUT DISCHARGE						
R_{DSCH_VOS}	Output discharge resistor on VOS pin	V_{EN} = GND, I(VOS) = -10mA		7	22	Ω
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		160		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis			20		°C

6.6 Typical Characteristics

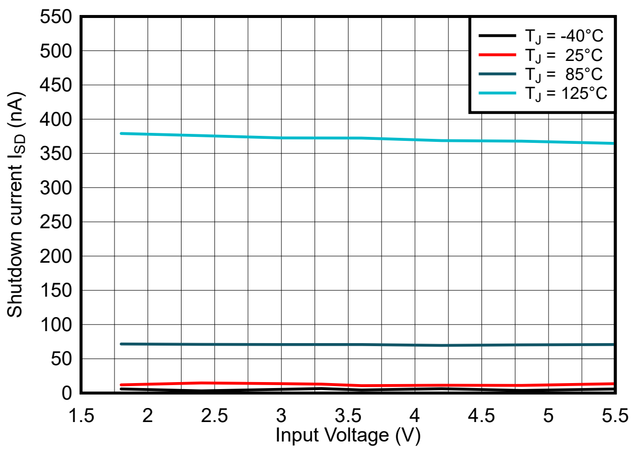


図 6-1. Shutdown Current I_{SD}

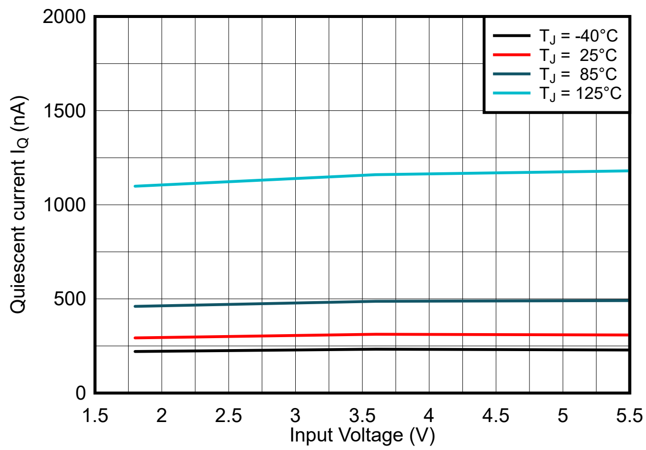


図 6-2. Quiescent Current I_Q

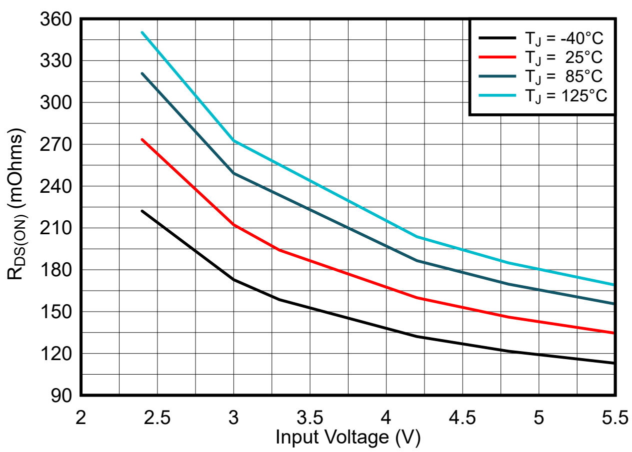


図 6-3. High Side Switch Drain Source Resistance $R_{DS(ON)}$

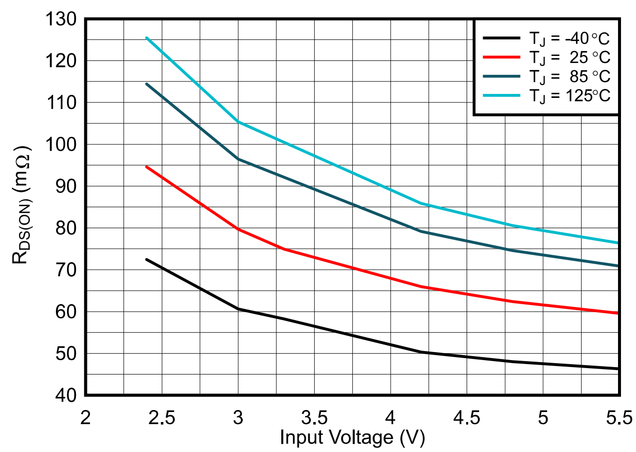


図 6-4. Low Side Switch Drain Source Resistance $R_{DS(ON)}$

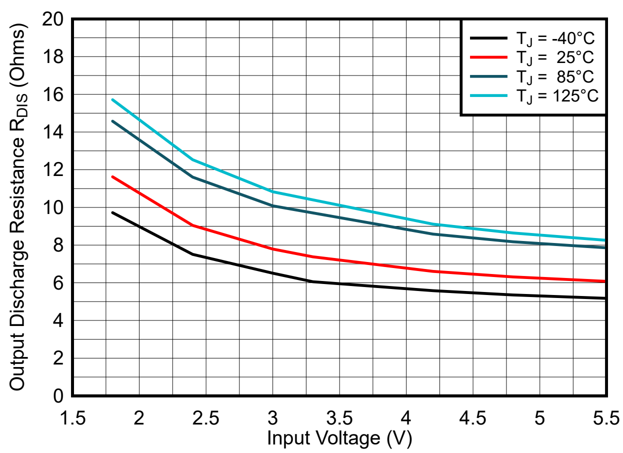


図 6-5. VOS Discharge Switch Drain Source Resistance R_{DIS}

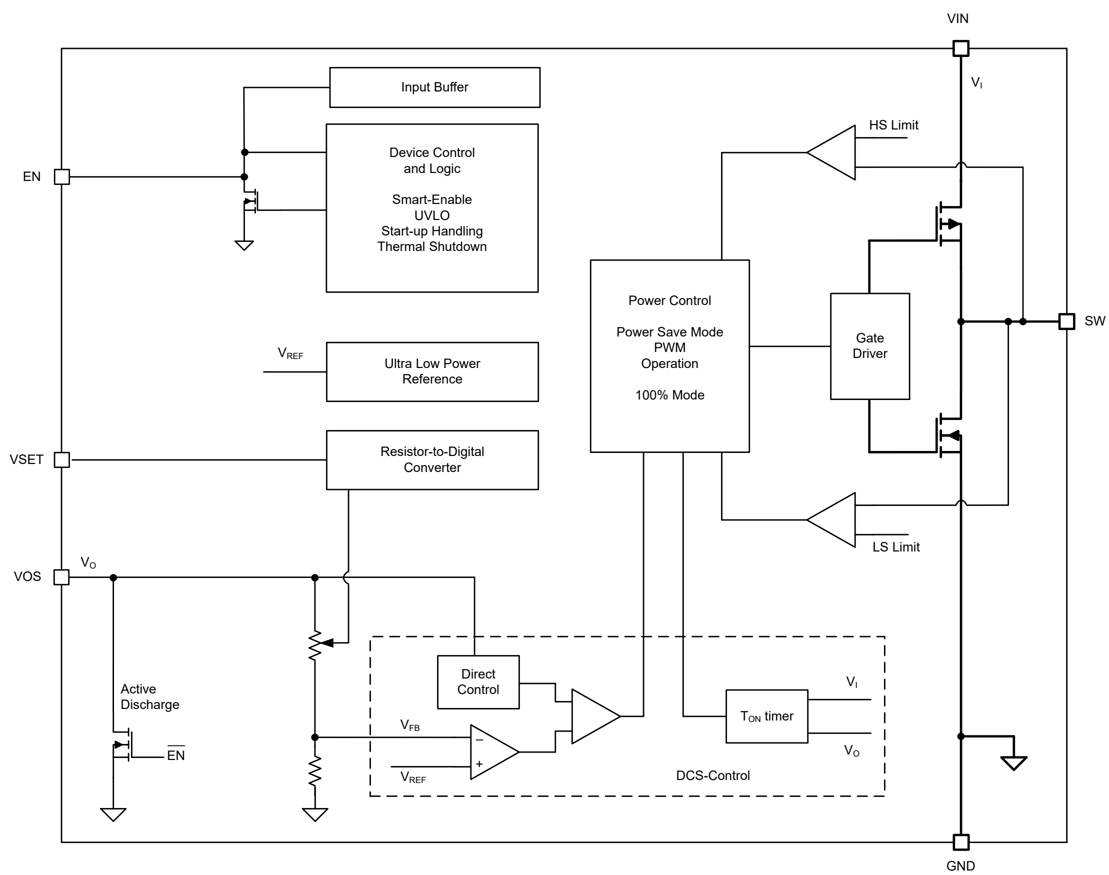
7 Detailed Description

7.1 Overview

The TPS62843 is a high-frequency, synchronous step-down converter with ultra-low quiescent current of typically 275nA in a 0.84-mm² chip size. The device operates with a tiny 1-µH inductor and 10-µF output capacitor over the entire recommended operation range to provide one of the industry's smallest chip and solution size.

Using TI's DCS-Control topology, the device extends the high efficiency operation area down to microamperes of load current during power save mode operation. TI's DCS-Control (Direct Control with Seamless Transition into power save mode) is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control. Characteristics of DCS-Control are excellent AC load regulation and transient response, low output ripple voltage, and a seamless transition between PFM and PWM mode operation. DCS-Control includes an AC loop that senses the output voltage (VOS pin) and directly feeds the information to a fast comparator stage. This comparator sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To achieve accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low-ESR capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Smart Enable and Shutdown (EN)

An internal 500kΩ resistor pulls the EN pin to GND and avoids floating the pin. This action prevents an uncontrolled start-up of the device in case the EN pin cannot be driven to low level safely. With EN low, the device is in shutdown mode. The device is turned on with EN set to a high level. The pulldown control circuit disconnects the pulldown resistor on the EN pin after the internal control logic and the reference have been powered up. With EN set to a low level, the device enters shutdown mode and the pulldown resistor is activated again. The high level of the EN pin must not exceed VIN voltage level.

7.3.2 Soft Start

After the device has been enabled with EN high, the device initializes and powers up the internal circuits. This action occurs during the regulator start-up delay time, $t_{Startup\_delay}$. After $t_{Startup\_delay}$ expires, the internal soft-start circuitry ramps up the output voltage within the soft-start time, t_{SS}. See 図 7-1.

The start-up delay time, $t_{Startup\_delay}$, varies depending on the selected VSET value. The start-up delay is shortest with VSET = 0 and longest with VSET = 16.

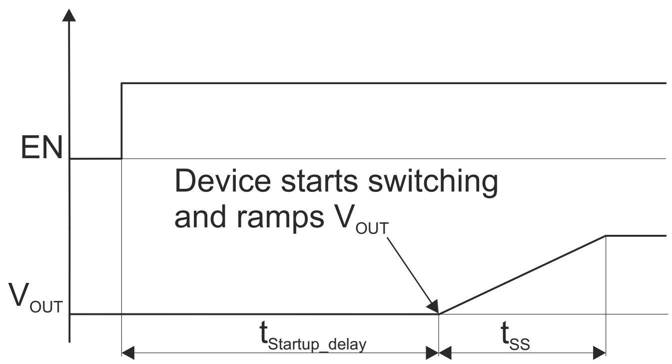


図 7-1. Device Start-Up

7.3.3 VSET Pin: Output Voltage Selection

The output voltage is set with a single external resistor connected between the VSET pin and GND. After the device has been enabled and the control logic as well as the internal reference have been powered up, a R2D (resistor-to-digital) conversion is started to detect the external resistor, R_{SET}, within the regulator start-up delay time, $t_{Startup\_delay}$. An internal current source applies current through the external resistor and an internal ADC reads back the resulting voltage level. Depending on the level, an internal feedback divider network is selected to set the correct output voltage. After this R2D conversion is finished, the current source is turned off to avoid current flow through the external resistor. The circuit can detect resistive values, high-level, low-level, and a pin-open.

For a proper reading, ensure that there is no additional current path or capacitance greater than 30pF total to GND during R2D conversion. Otherwise, the additional current to GND is interpreted as a lower resistor value and a false output voltage is set. 表 7-1 lists the correct resistor values for R_{SET} to set the appropriate output voltages. The R2D converter is designed to operate with resistor values out of the E96 table and requires 1% resistor value accuracy. The external resistor R_{SET} is not a part of the regulator feedback loop and has therefore no impact on the output voltage accuracy. Ensure that there is no other leakage path than the R_{SET} resistor at the VSET pin during an undervoltage lockout event. Otherwise, a false output voltage is set.

表 7-1. Output Voltage Setting

VSET	Output Voltage Setting [V]			R_{SET} [Ω]
	TPS628436	TPS628437	TPS628438	
1	0.400	0.80	1.8	10.0k
2	0.425	0.85	1.9	12.1k
3	0.450	0.90	2.0	15.4k
4	0.475	0.95	2.1	18.7k
5	0.500	1.00	2.2	23.7k
6	0.525	1.05	2.3	28.7k
7	0.550	1.10	2.4	36.5k
8	0.575	1.15	2.5	44.2k
9	0.600	1.20	2.6	56.2k
10	0.625	1.25	2.7	68.1k
11	0.650	1.30	2.8	86.6k
12	0.675	1.35	2.9	105.0k
13	0.700	1.40	3.0	133.0k
14	0.725	1.45	3.1	162.0k
15	0.750	1.50	3.2	205.0k
16	0.775	1.55	3.3	249.0k or larger
17	0.8	1.6	3.4	VIN
0	1.0	1.8	3.6	GND

7.3.4 Undervoltage Lockout (UVLO)

To avoid misoperation of the device at low input voltages, an undervoltage lockout (UVLO) comparator monitors the supply voltage. The UVLO comparator shuts down the device at an input voltage of 1.7V (maximum) with falling V_{IN}. The device starts at an input voltage of 1.8V (maximum) rising V_{IN}. After the device re-enters operation out of an undervoltage lockout condition, the device behaves like it does being enabled. The internal control logic is powered up and the external resistor at the VSET pin is read out.

7.3.5 Switch Current Limit, Short-Circuit Protection

The TPS62843 integrates a current limit on the high-side and low-side MOSFETs to protect the device against overload or short circuit conditions. The current in the switches is monitored cycle by cycle. If the high-side MOSFET current limit, $I_{HS(OC)}$ trips, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. After the inductor current through the low-side switch decreases beneath the low-side MOSFET current limit, $I_{LS(OC)}$, the low-side MOSFET is turned off and the high-side MOSFET turns on again.

7.3.6 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds the thermal shutdown temperature, $T_{J(SD)}$, of 160°C (typical), the device enters thermal shutdown. Both the high-side and low-side power FETs are turned off. When T_J decreases below the hysteresis amount of typically 20°C, the converter resumes operation, beginning with a soft start to the originally set V_{OUT} (there is no R2D conversion of R_{SET}). The thermal shutdown is not active in power save mode.

7.3.7 Output Voltage Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0V.

The internal discharge resistor is connected to the VOS pin. The discharge function is enabled as soon as the device is disabled. The minimum supply voltage required to keep the discharge function active is V_{IN} > $V_{TH\_UVLO(R)}$.

7.4 Device Functional Modes

7.4.1 Power Save Mode Operation

The DCS-Control topology supports power save mode operation. At light loads, the device operates in PFM (pulse frequency modulation) mode that generates a single switching pulse to ramp up the inductor current and recharge the output capacitor, followed by a sleep period where most of the internal circuits are shut down to achieve the lowest operating quiescent current. During this time, the load current is supported by the output capacitor. The duration of the sleep period depends on the load current and the inductor peak current. During the sleep periods, the current consumption is reduced to typically 275nA. This low quiescent current consumption is achieved by an ultra-low power voltage reference, an integrated high impedance feedback divider network, and an optimized power save mode operation.

In PFM mode, the switching frequency varies linearly with the load current. At medium and high load conditions, the device enters automatically PWM (pulse width modulation) mode and operates in continuous conduction mode with a nominal switch frequency f_{sw} of typically 1.5MHz. The switching frequency in PWM mode is controlled and depends on V_{IN} and V_{OUT}. The boundary between PWM and PFM mode is when the inductor current becomes discontinuous.

If the load current decreases, the converter seamlessly enters PFM mode to maintain high efficiency down to very light loads. Because DCS-Control supports both operation modes within one single building block, the transition from PWM to PFM mode is seamless with minimum output voltage ripple.

7.4.2 100% Mode Operation

The duty cycle of the buck converter operating in PWM mode is given as $D = V_{OUT}/V_{IN}$. The duty cycle increases as the input voltage comes close to the output voltage. In 100% duty cycle mode, the device keeps the high-side switch on continuously. The high-side switch stays turned on as long as the output voltage is below the internal set point. This allows the conversion of small input to output voltage differences.

8 Application and Implementation

注

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8.1 Application Information

The following sections discuss the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

8.2 Typical Application

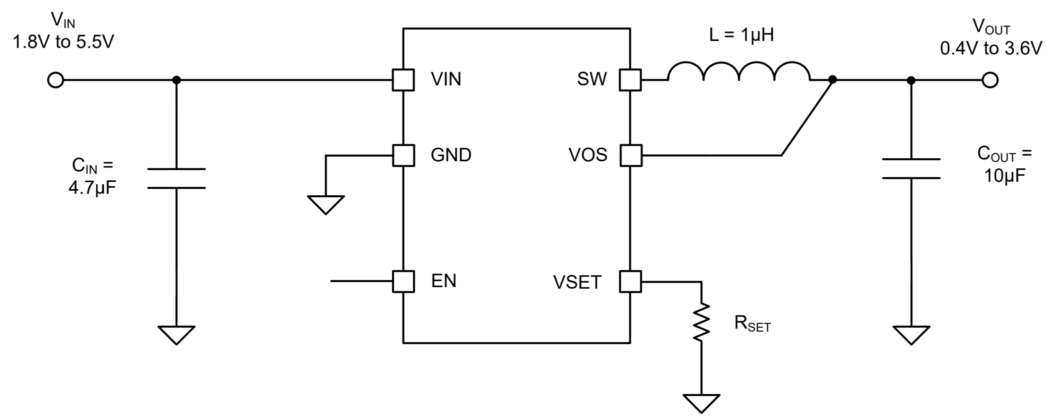

図 8-1. TPS62843 Typical Application Circuit

8.2.1 Design Requirements

表 8-1 shows the list of components for the application circuit and the characteristic application curves.

表 8-1. Components for Application Characteristic Curves

Reference	Description	Value	Size Code Inch [metric L × W × T]	Manufacturer
TPS628436, TPS628437, TPS628438	275nA-I_Q buck converter		[1.05mm × 0.8mm × 0.4mm]	TI
C_{IN}	Ceramic capacitor GRM155R60J475ME47D	4.7µF	0402 [1.0mm × 0.5mm × 0.5mm]	Murata
L	Inductor DFE201610-1R0M	1µH	0806 [2.0mm × 1.6mm × 1.0mm]	Murata
C_{OUT}	Ceramic capacitor GRM155R60J106ME15D	10µF	0402 [1.0mm × 0.5mm × 0.5mm]	Murata
R_{SET}	See voltage setting table		0402 [1.0mm × 0.5mm × 0.5mm]	

8.2.2 Detailed Design Procedure

Follow the passive component selection per the typical application circuit.

8.2.3 Application Curves

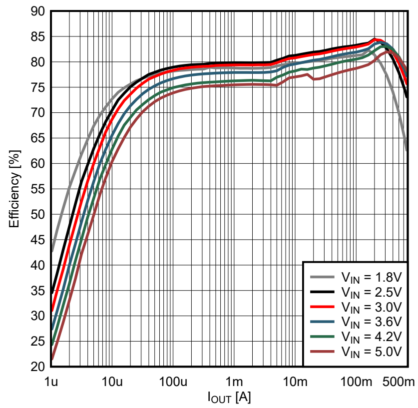

図 8-2. Efficiency at V_{OUT} = 0.4V

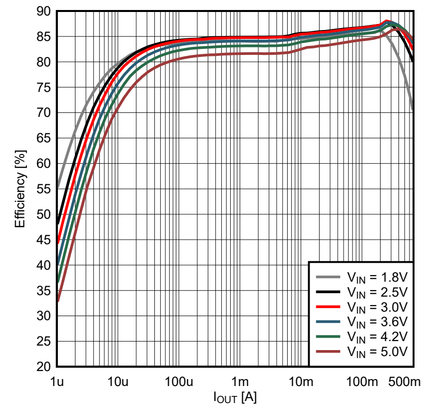

図 8-3. Efficiency at V_{OUT} = 0.7V

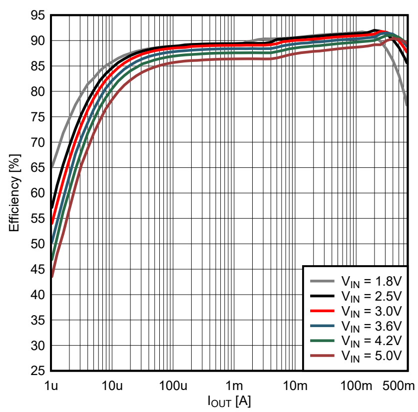

図 8-4. Efficiency at V_{OUT} = 1.2V

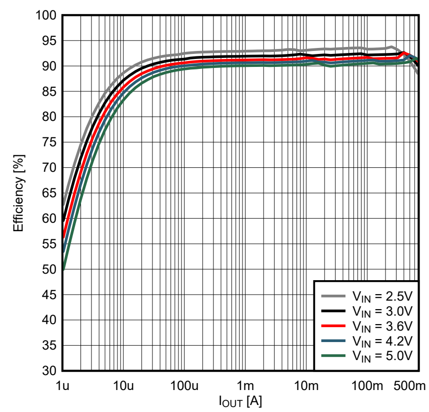

図 8-5. Efficiency at V_{OUT} = 1.8V

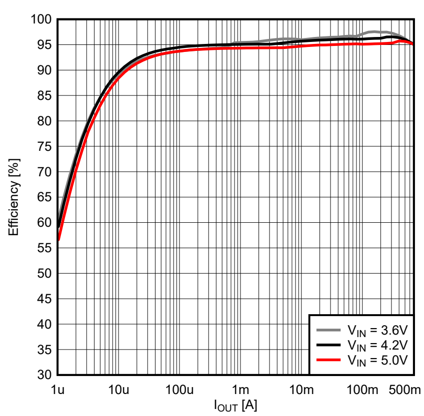

図 8-6. Efficiency at V_{OUT} = 3.3V

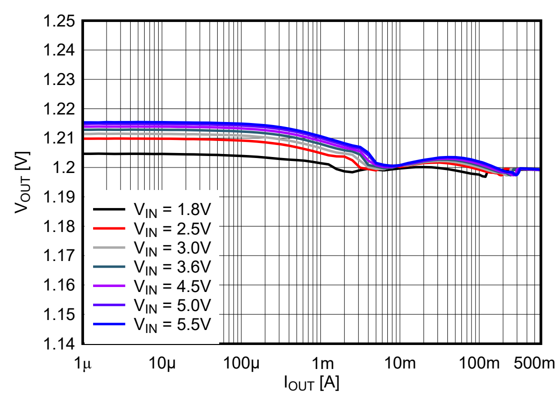

図 8-7. Output Voltage vs Output Current at V_{OUT} = 1.2V

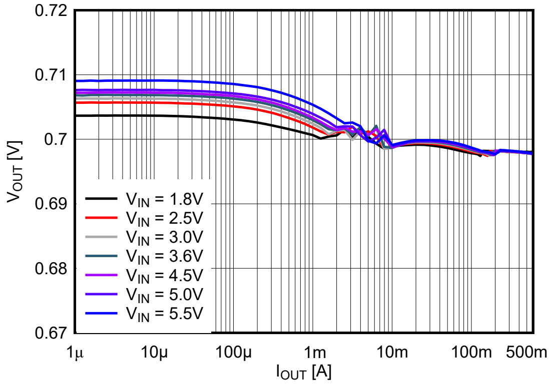

図 8-8. Output Voltage vs Output Current at V_{OUT} = 0.7V

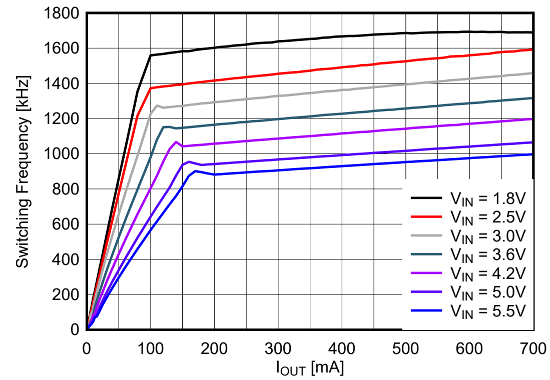

図 8-9. Switching Frequency vs Output Current at V_{OUT} = 0.4V

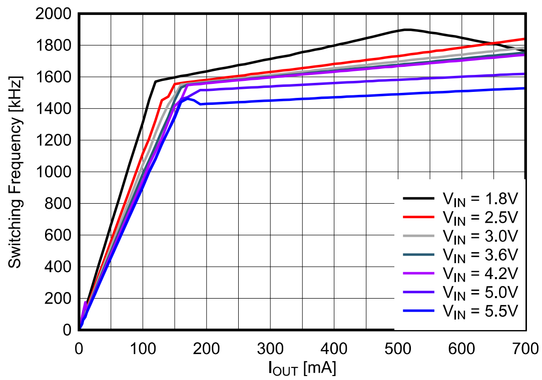

図 8-10. Switching Frequency vs Output Current at V_{OUT} = 0.7V

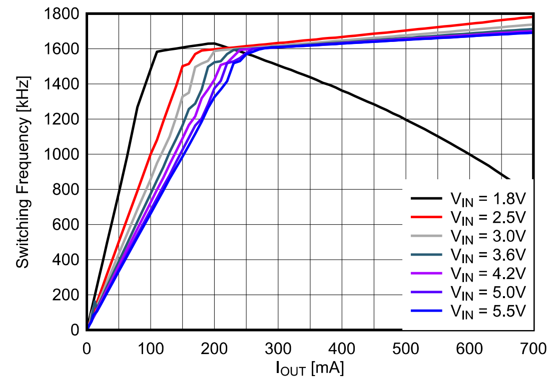

図 8-11. Switching Frequency vs Output Current at V_{OUT}= 1.2V

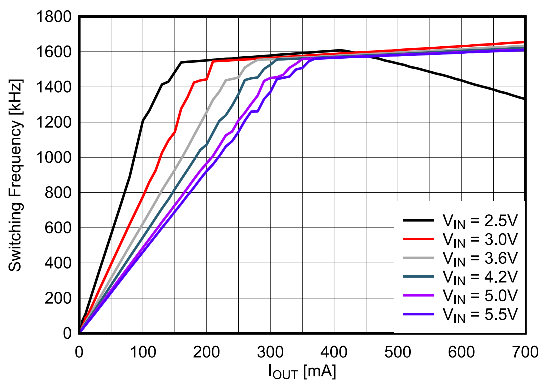

図 8-12. Switching Frequency vs Output Current at V_{OUT}= 1.8V

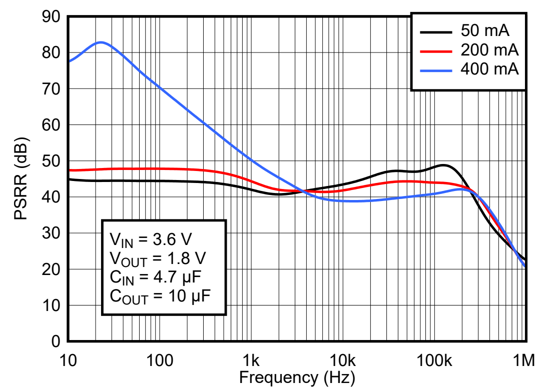

図 8-13. Power Supply Rejection Ratio (PSRR) at V_{OUT} = 1.8V

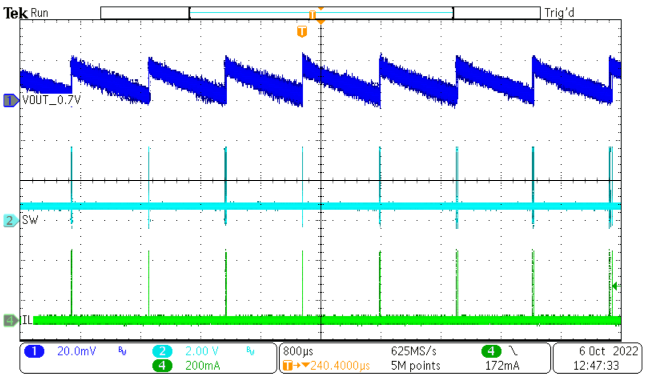

図 8-14. Typical Operation at V_{OUT} = 0.7V, I_{OUT} = 100µA

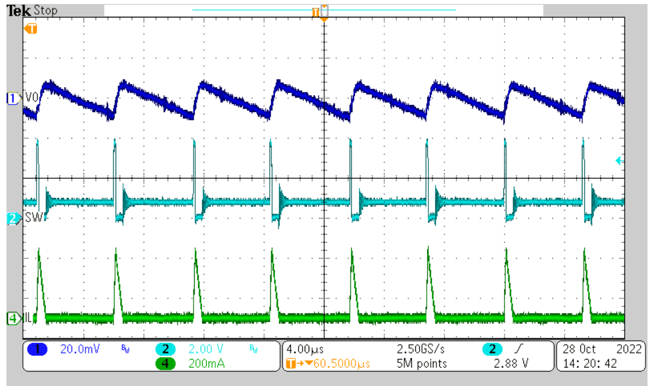

図 8-15. Typical Operation at V_{OUT} = 0.7V, I_{OUT} = 20mA

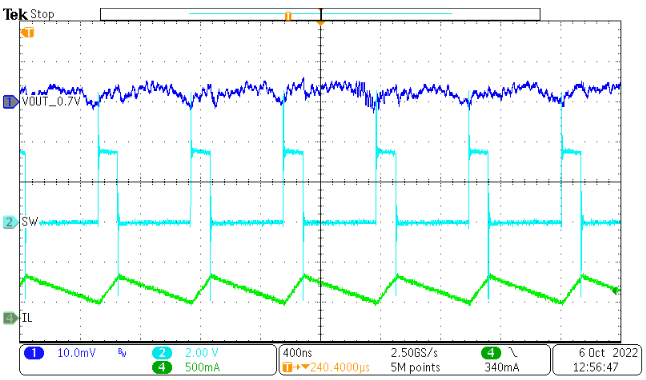

図 8-16. Typical Operation at V_{OUT} = 0.7V, I_{OUT} = 400mA

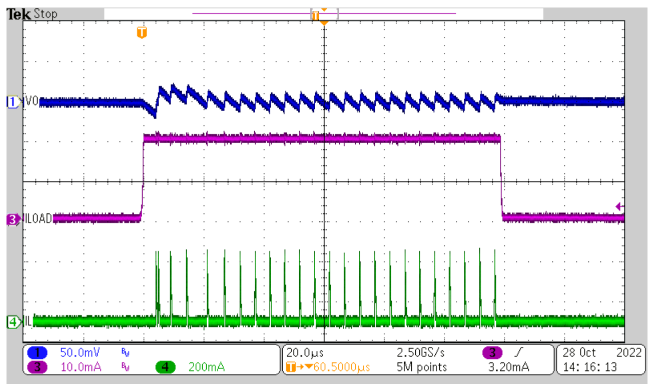

図 8-17. Load Transient at V_{OUT} = 0.7V, I_{OUT} = 100 µA to 20 mA

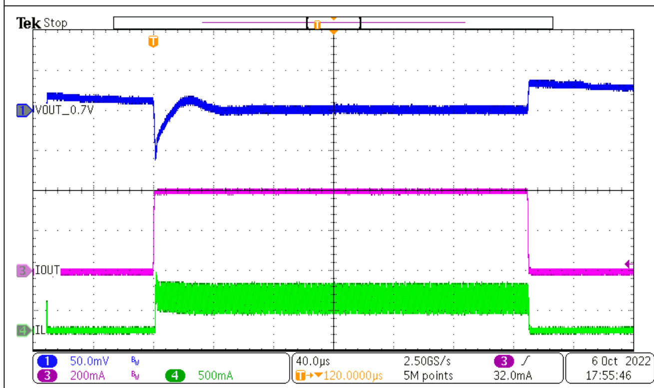

図 8-18. Load Transient at V_{OUT} = 0.7V, I_{OUT} = 100µA to 400mA

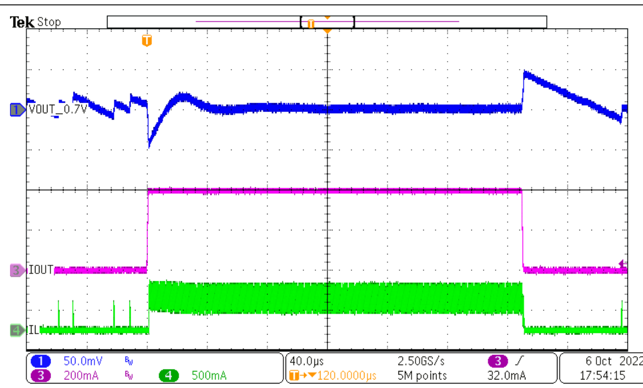

図 8-19. Load Transient at V_{OUT} = 0.7V, I_{OUT} = 5mA to 400mA

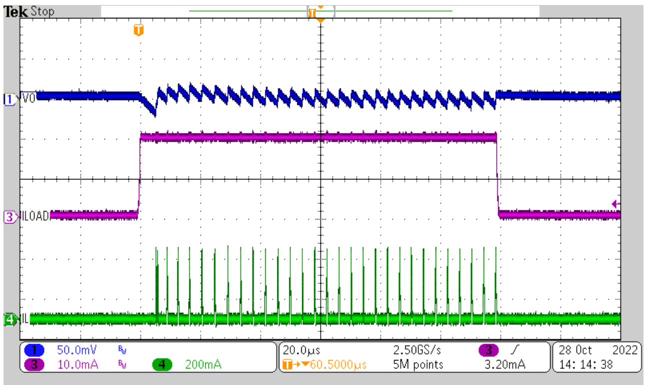

図 8-20. Load Transient at V_{OUT} = 1.2V, I_{OUT} = 100µA to 20mA

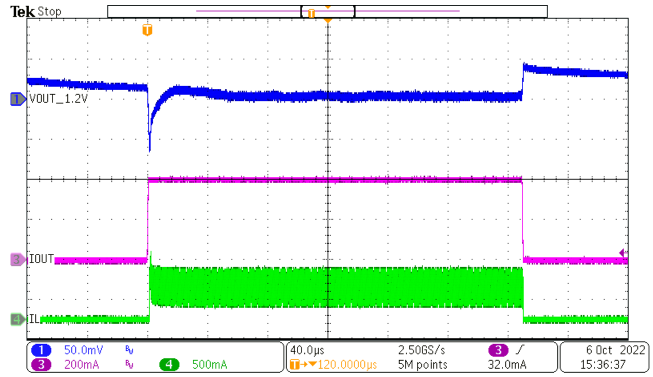

図 8-21. Load Transient at V_{OUT} = 1.2V, I_{OUT} = 100µA to 400mA

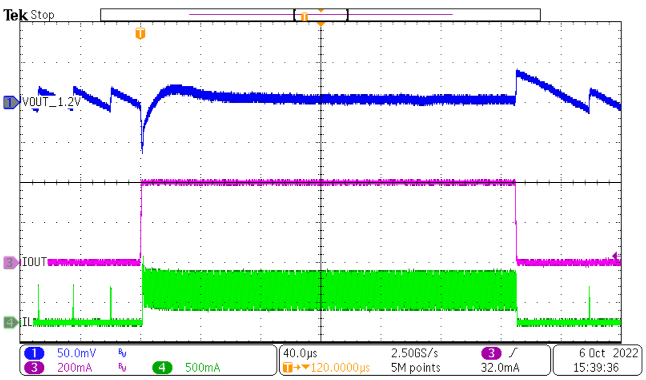

図 8-22. Load Transient at V_{OUT} = 1.2V, I_{OUT} = 5mA to 400mA

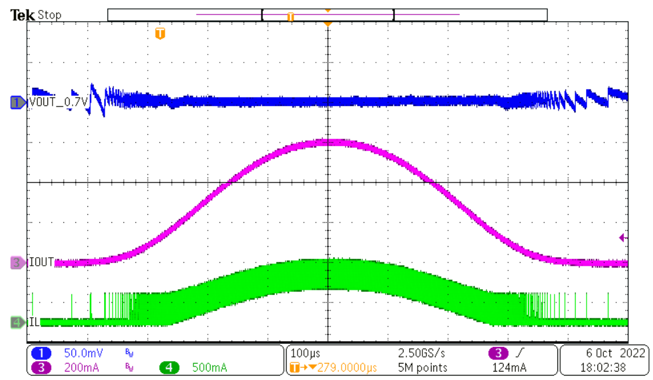

図 8-23. AC Load Sweep at V_{OUT} = 0.7V, I_{OUT} = 1mA to 600mA

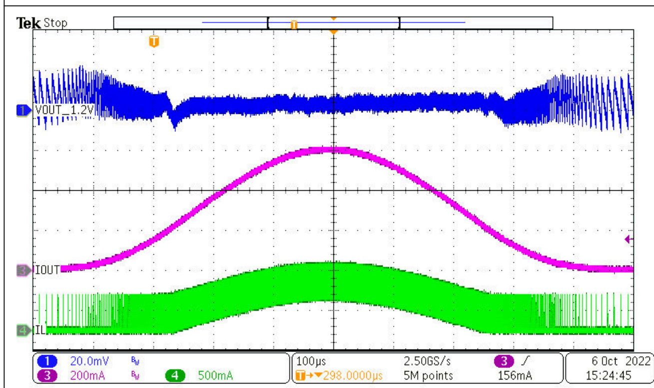

図 8-24. AC Load Sweep at V_{OUT} = 1.2V, I_{OUT} = 1mA to 600mA

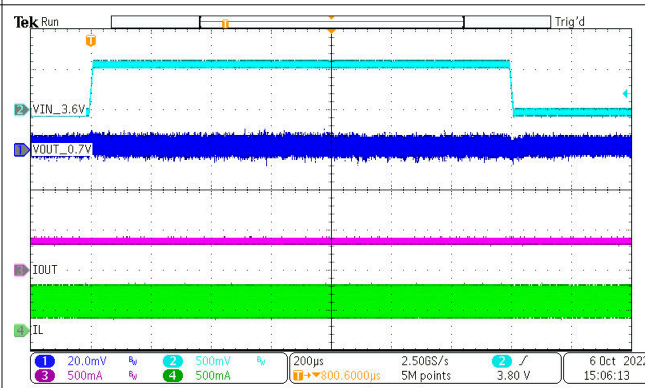

図 8-25. Line Transient at V_{OUT} = 0.7V, I_{OUT} = 400mA, V_{IN} = 3.6V to 4.2V

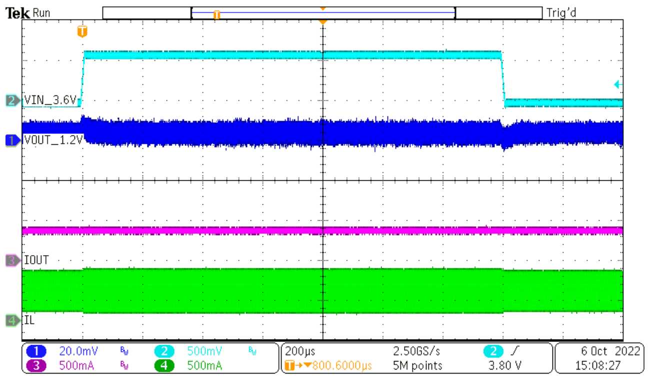

図 8-26. Line Transient at V_{OUT} = 1.2V, I_{OUT} = 400mA, V_{IN} = 3.6V to 4.2V

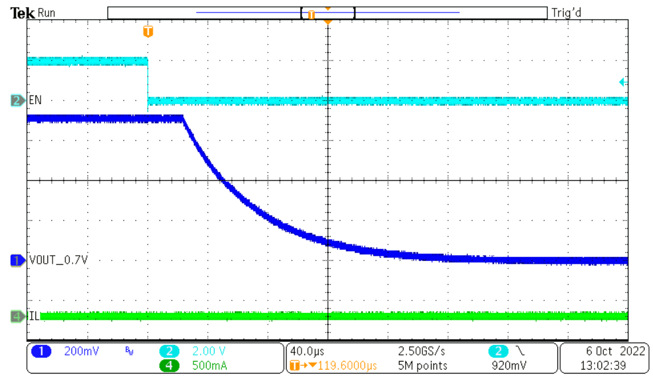

図 8-27. Shutdown, Output Discharge at V_{OUT} = 0.7V

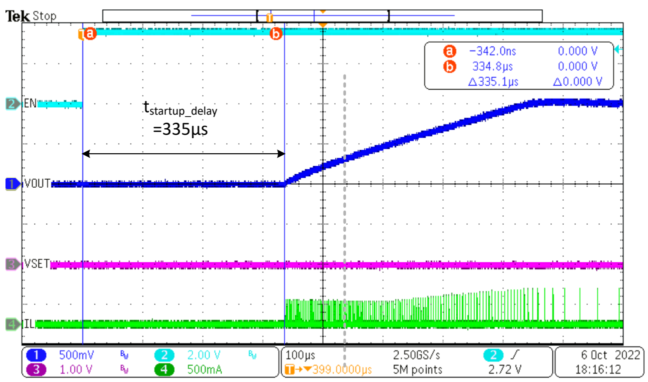

図 8-28. Start-Up Delay Time, VSET = GND

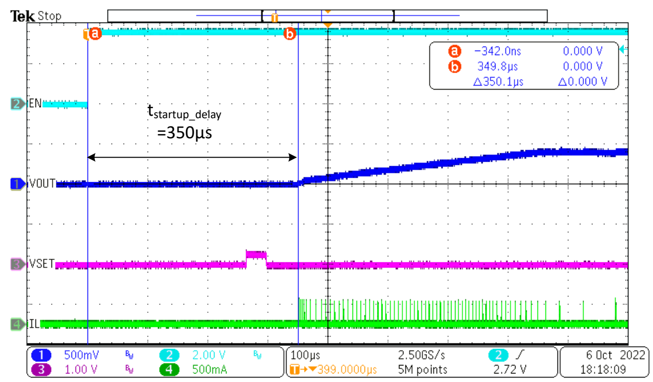

図 8-29. Start-Up Delay Time, VSET = 10kohms

8.3 Power Supply Recommendations

The power supply must provide a current rating according to the supply voltage, output voltage, and output current of the TPS62843.

8.4 Layout

8.4.1 Layout Guidelines

The pinout of the TPS62843 has been optimized to enable a single top layer PCB routing of the IC and its critical passive components such as CIN, COUT, and L. Furthermore, this pinout allows the user to connect tiny components such as 0201 (0603 Metric) size capacitors and 0402 (1005 Metric) size inductors. A solution size smaller than $5mm^2$ can be achieved with a fixed output voltage. As for all switching power supplies, the layout is an important step in the design. Care must be taken in board layout to get the specified performance. Providing a low inductance, low impedance ground path is critical. Therefore, use wide and short traces for the main current paths. Place the input capacitor as close as possible to the VIN of the IC and GND pins. This placement is the most critical component placement. The VOS line is a sensitive, high impedance line and must be connected to the output capacitor and routed away from noisy components and traces (for example, the SW line) or other noise sources.

8.4.2 Layout Example

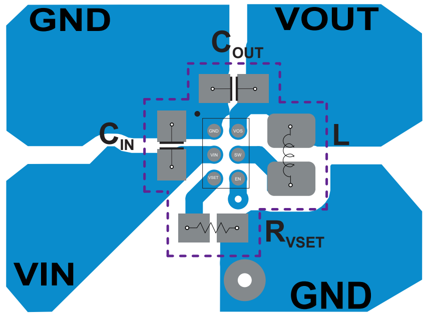

図 8-30. Layout Example (YKA Package)

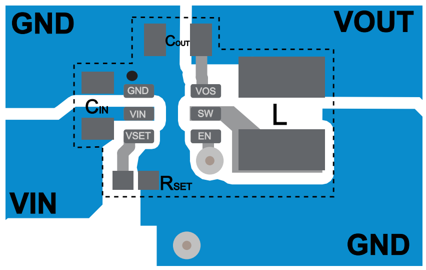

図 8-31. Layout Example (DRL Package)

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (September 2023) to Revision C (June 2024) **Page**

- 最小実効出力容量が 4μF であることを明確化 1
- SOT563 パッケージからプレビューの注を削除 1
- Added a column for the SOT563 package to add the pin numbers for the SOT563 package 4
- Added an Input Buffer block to the EN pin in the functional block diagram 9
- Added a statement in the description saying " The high level of the EN pin must not exceed VIN voltage level" to clarify correct pin usage 10
- Deleted the term I_{LIMF} and replaced with $I_{HS(OC)}$ for the high side FET and replaced with $I_{LS(OC)}$for the low side FET 11
- Deleted the erroneous load transient plot (Output Voltage vs Output Current for V_{OUT} 1.2V, and I_{OUT} step = 100uA to 400mA) and replaced with the correct plot 14

Changes from Revision A (May 2023) to Revision B (September 2023) **Page**

- ドキュメントに SOT563 パッケージを追加 1

Changes from Revision * (January 2022) to Revision A (May 2023) **Page**

- ドキュメントのステータスを「事前情報」から「量産データ」に変更 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS628436DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	436	Samples
TPS628436YKAR	ACTIVE	DSBGA	YKA	6	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	J	Samples
TPS628437DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	437	Samples
TPS628437YKAR	ACTIVE	DSBGA	YKA	6	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	K	Samples
TPS628438DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	438	Samples
TPS628438YKAR	ACTIVE	DSBGA	YKA	6	12000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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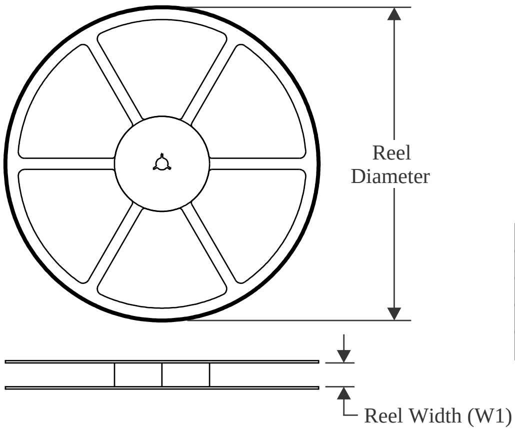
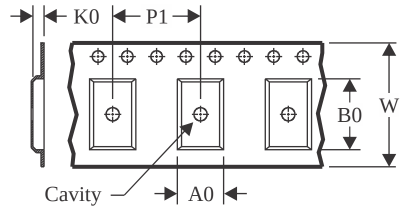
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

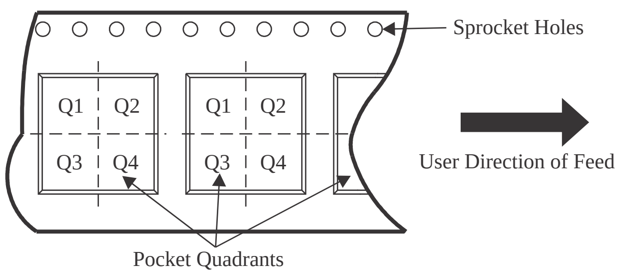


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

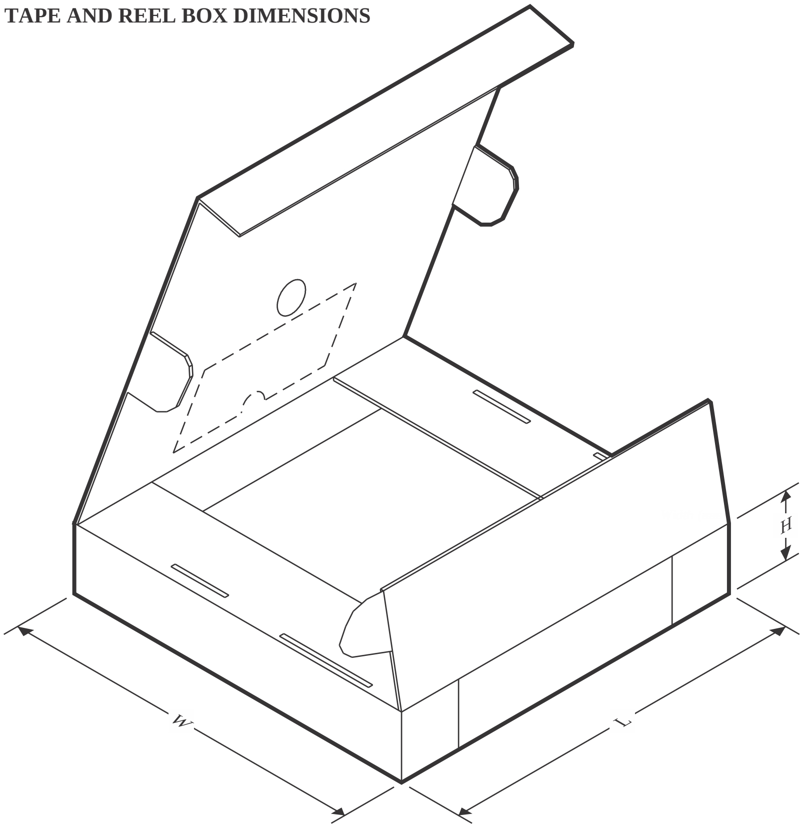
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

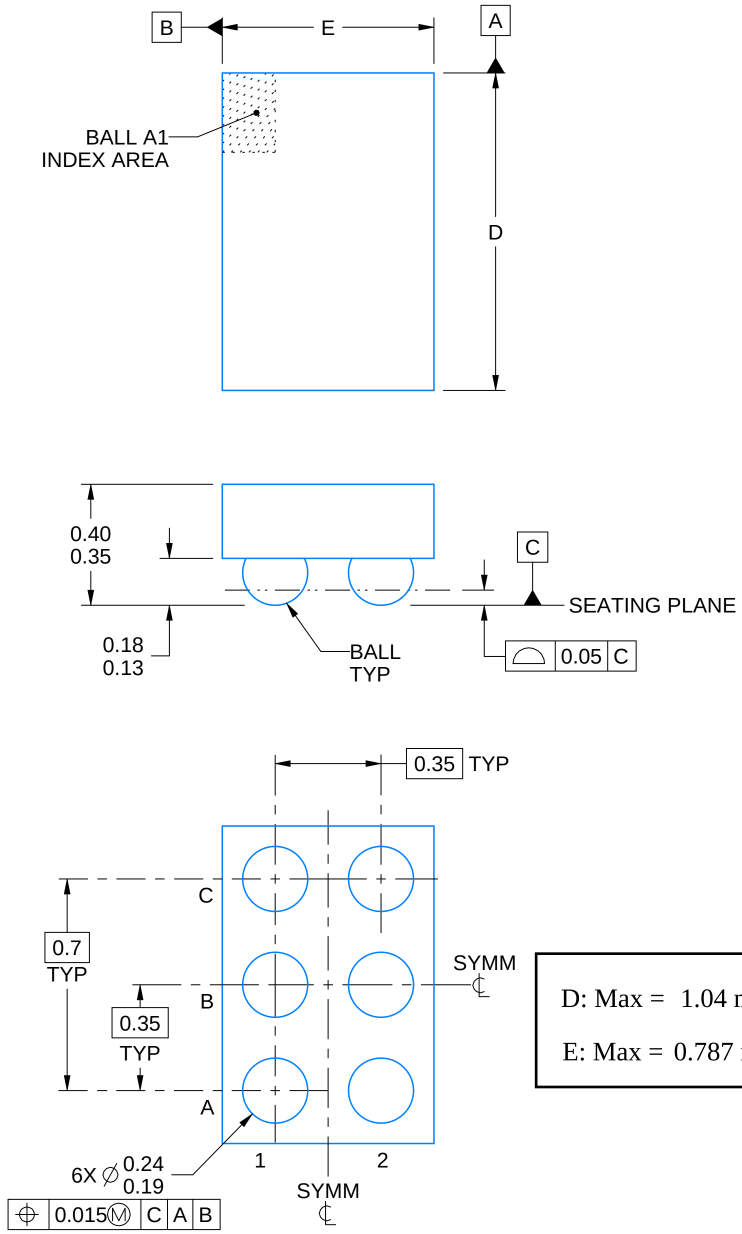
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS628436DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS628436YKAR	DSBGA	YKA	6	12000	180.0	8.4	0.9	1.16	0.47	2.0	8.0	Q1
TPS628437DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS628437YKAR	DSBGA	YKA	6	12000	180.0	8.4	0.9	1.16	0.47	2.0	8.0	Q1
TPS628438DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
TPS628438YKAR	DSBGA	YKA	6	12000	180.0	8.4	0.9	1.16	0.47	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS628436DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS628436YKAR	DSBGA	YKA	6	12000	182.0	182.0	20.0
TPS628437DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS628437YKAR	DSBGA	YKA	6	12000	182.0	182.0	20.0
TPS628438DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS628438YKAR	DSBGA	YKA	6	12000	182.0	182.0	20.0



D: Max = 1.04 mm, Min = 0.98 mm	
E: Max = 0.787 mm, Min =0.727 mm	

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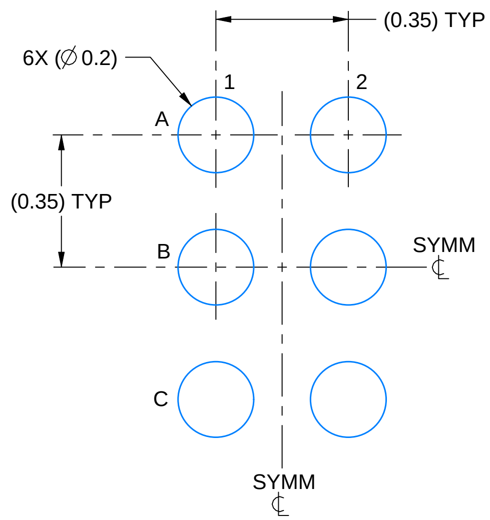
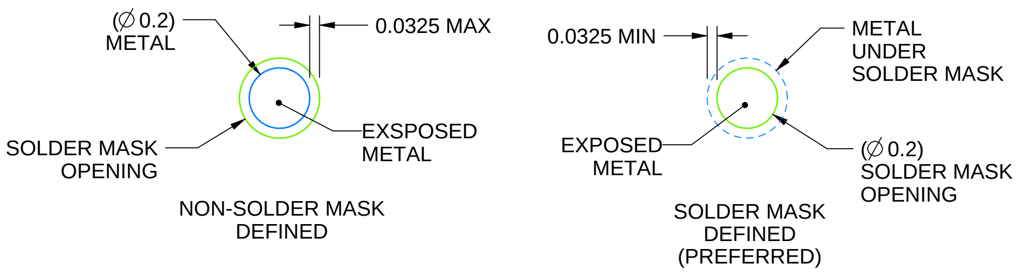
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

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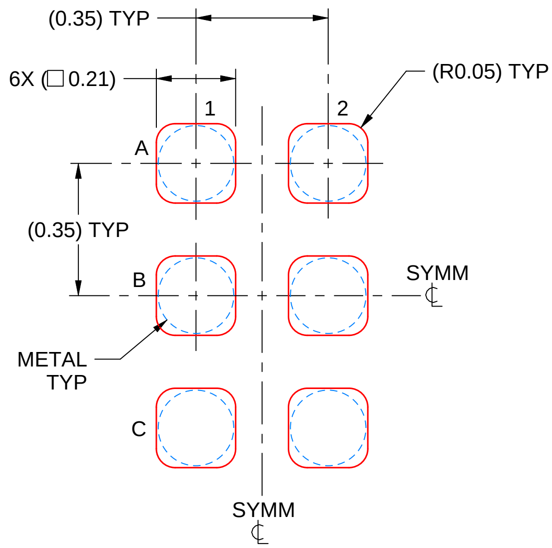
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm - 0.1 mm THICK STENCIL
SCALE:50X

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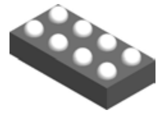
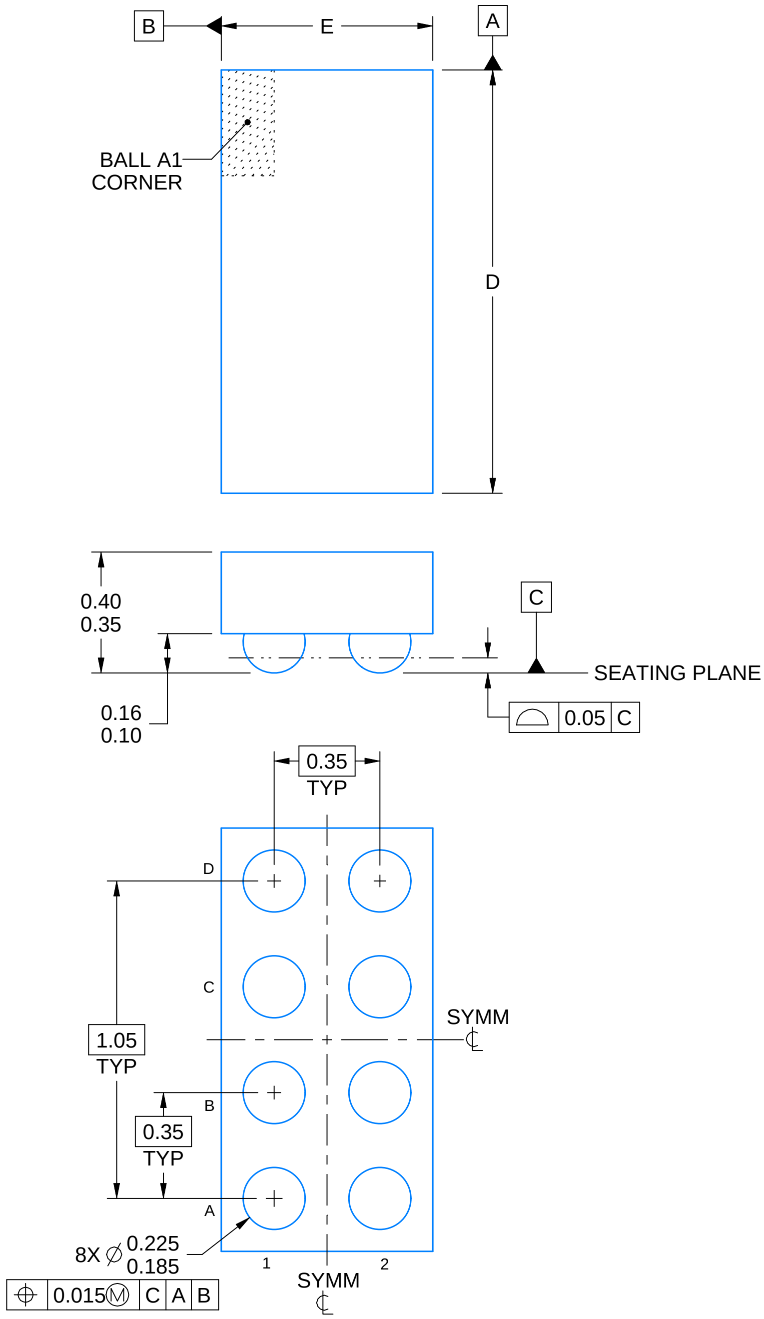
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.





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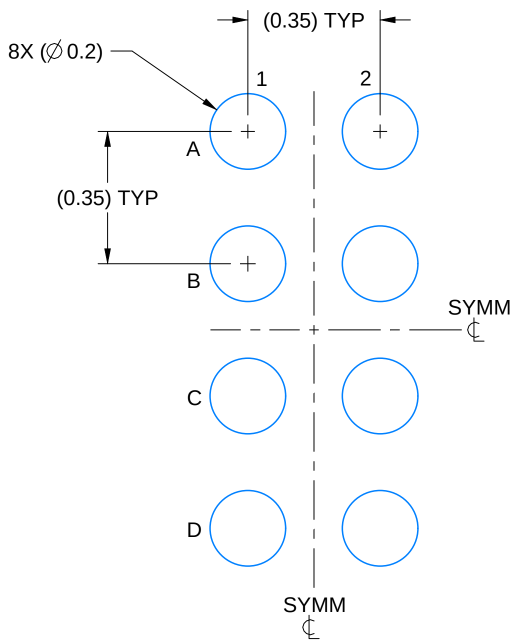
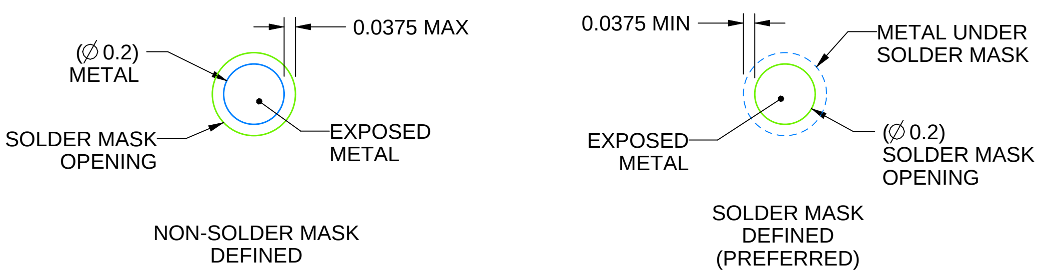
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 50X

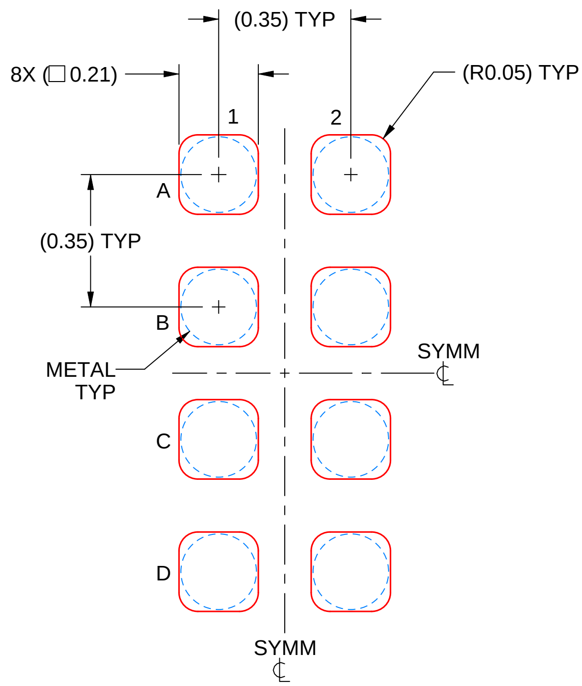


SOLDER MASK DETAILS
NOT TO SCALE

4225328/B 06/2023

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.075 mm THICK STENCIL
SCALE: 50X

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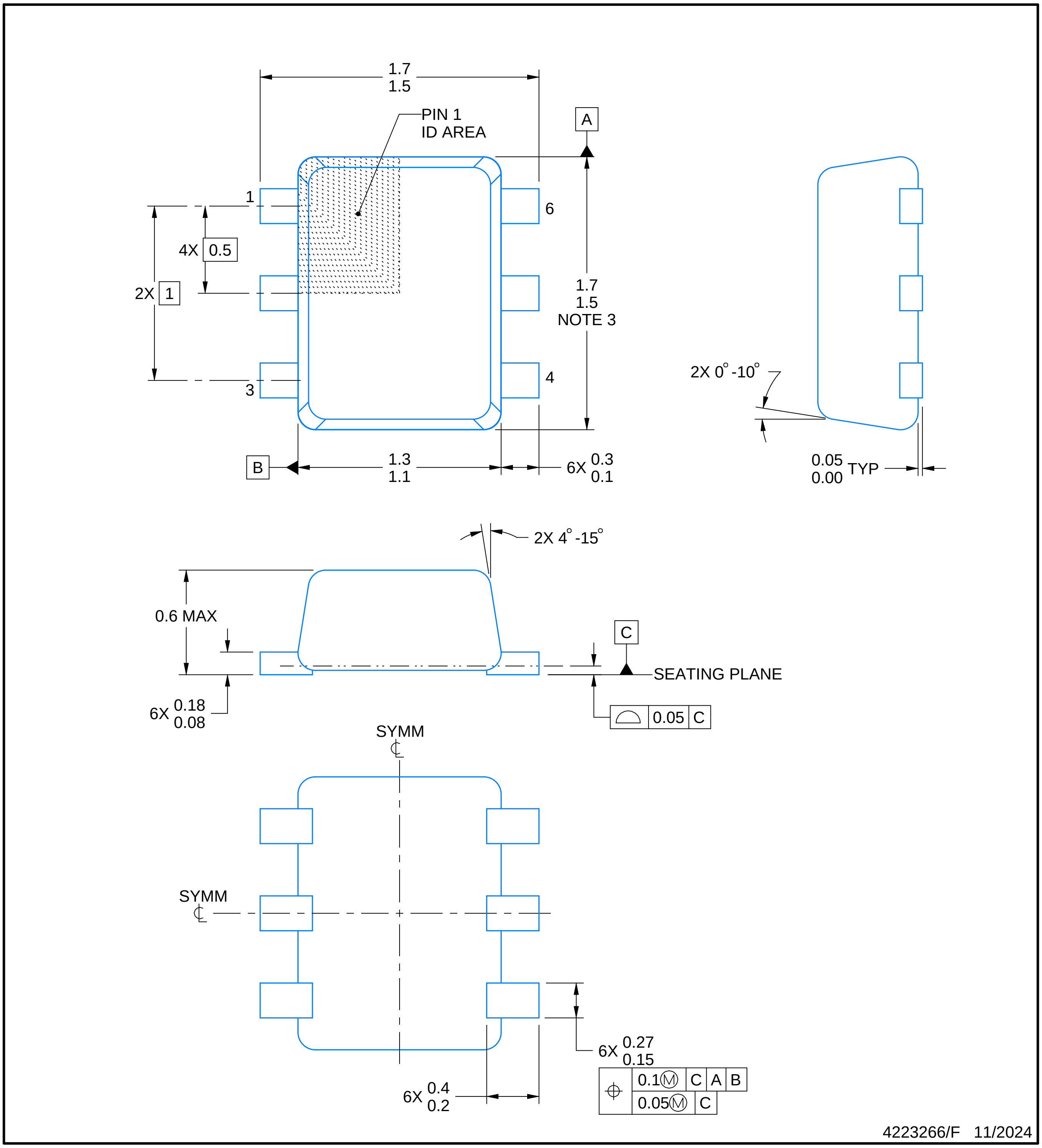
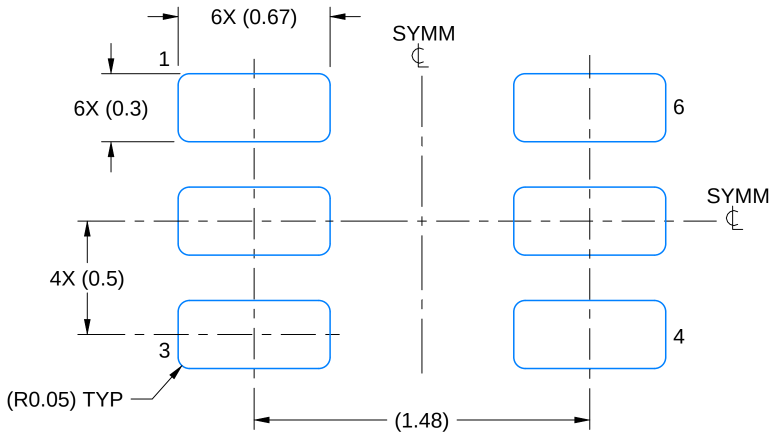
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

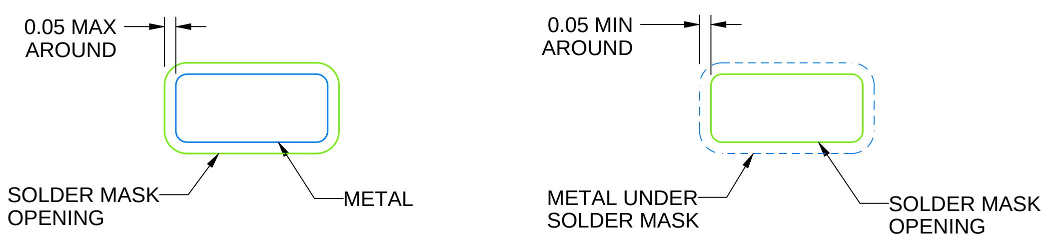


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD



LAND PATTERN EXAMPLE
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDERMASK DETAILS

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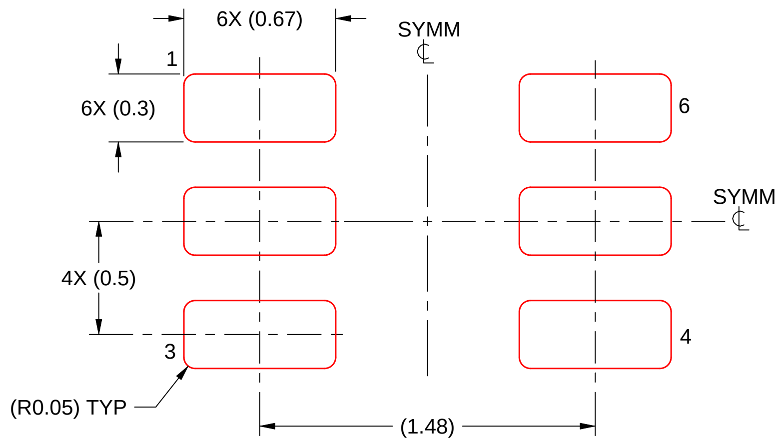
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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