

## TPS6216x 3V~17V、1A降圧型コンバータ、DCS-Control™搭載

### 1 特長

- DCS-Control™トポロジ
- 入力電圧範囲: 3V~17V
- 最大1Aの出力電流
- 出力電圧を0.9V~6Vの範囲で調整可能
- 固定出力電圧バージョン
- シームレスなパワーセーブ・モード移行
- 静止電流17μA (標準値)
- パワー・グッド出力
- 100%デューティ・サイクル・モード
- 短絡保護
- 過熱保護機能
- TPS62170およびTPS62125とピン互換
- 3.00mm×3.00mmの8ピンVSSOPパッケージおよび2.00mm×2.00mmの8ピンWSOパッケージで供給
- WEBENCH® Power Designerにより、TPS62160を使用するカスタム設計を作成

### 2 アプリケーション

- 標準の12Vレール電源
- 単一または複数のLiイオン・バッテリーを使用するPOL電源
- LDOの代替品
- 組み込みシステム
- デジタル静止画カメラ、ビデオ
- モバイルPC、タブレットPC、モデム

### 3 概要

TPS6216xデバイス・ファミリーは使いやすい同期整流降圧型DC/DCコンバータで、電力密度の高いアプリケーションに最適化されています。スイッチング周波数が標準値で2.25MHzと高いため、小型のインダクタを使用でき、高速な過渡応答が実現されるとともに、DCS-Control™トポロジの使用によって出力電圧の高い精度が得られます。

3V~17Vの広い入力電圧範囲で動作するため、このデバイスはリチウムイオンや他のバッテリー、および12Vの中間電源レールで動作するシステムに最適です。0.9V~6Vの出力電圧で、1Aまでの出力電流を連続的にサポートします(100%デューティ・サイクル・モード時)。

イネーブル・ピンおよびオープン・ドレインのパワー・グッド・ピンの構成により、電源シーケンシングも可能です。

パワーセーブ・モードでは、このデバイスはVINから約17μAの静止電流を消費します。負荷が小さい時には自動的かつシームレスにパワーセーブ・モードへ移行するため、負荷範囲全体にわたって高い効率が維持されます。シャットダウン・モードではデバイスがオフになり、シャットダウン時の消費電流は2μA未満です。

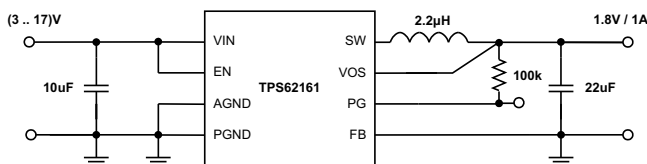
このデバイスには出力電圧が可変と固定のバージョンがあり、2.00mm×2.00mmの8ピンWSOパッケージ(DSG)、または3.00mm×3.00mmの8ピンVSSOPパッケージ(DGK)に封入されています。

#### 製品情報(1)

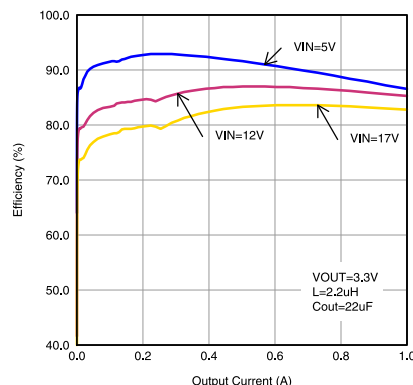
| 型番       | パッケージ     | 本体サイズ(公称)     |
|----------|-----------|---------------|
| TPS6216x | WSO (8)   | 2.00mm×2.00mm |
| TPS62160 | VSSOP (8) | 3.00mm×3.00mm |

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

#### 代表的なアプリケーションの回路図



#### 効率と出力電流との関係



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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Revision D (October 2014) から Revision E に変更  | Page |
|--|------|
| • WEBENCH® Designerへのリンクを追加  | 1    |
| • Added "SW (AC), less than 10ns" specification to Absolute Maximum Ratings table  | 5    |
| • Changed T <sub>J</sub> MAX spec from "125" to "150"  | 5    |
| • Added I <sub>Q</sub> and I <sub>SD</sub> specifications  | 6    |
| • Added 125°C plot line in <a href="#">Figure 1</a> and <a href="#">Figure 4</a> Typical Characteristics graphic entities. | 7    |

| Revision C (September 2013) から Revision D に変更  | Page |
|--|------|
| • 「製品情報」表、「ESD定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 | 1    |

| Revision B (August 2013) から Revision C に変更                           | Page |
|--|------|
| • Changed 50mV/μs to 50mV/s in <i>Enable / Shutdown (EN)</i> section | 9    |

| Revision A (March 2012) から Revision B に変更  | Page |
|--|------|
| • Added note to Terminal Functions         | 4    |
| • Changed <a href="#">Equation 13</a>      | 25   |
| • Added diode to <a href="#">Figure 41</a> | 25   |

**2011年11月発行のものから更新****Page**

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|  |    |
|--|----|
| • データシートを混在ステータスから量産データへ 変更.....                 | 1  |
| • 「特長」にVSSOP-8パッケージを 追加.....                     | 1  |
| • 「概要」に8ピンVSSOPパッケージを 追加.....                    | 1  |
| • Added DGK package pinout.....                  | 4  |
| • Added DGK package to Thermal Information ..... | 5  |
| • Changed <a href="#">Table 2</a> .....          | 14 |

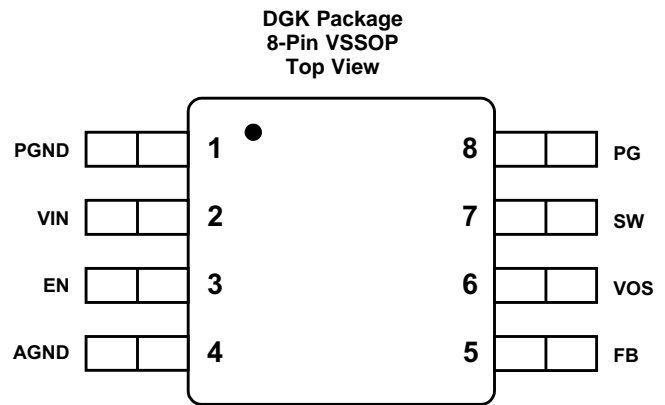
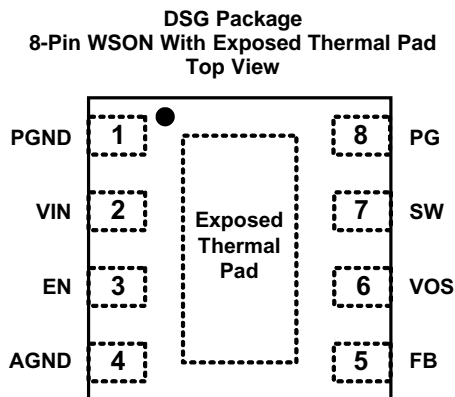
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## 5 Device Voltage Options

| OUTPUT VOLTAGE <sup>(1)</sup> | PART NUMBER | PACKAGE   |
|-------------------------------|-------------|-----------|
| adjustable                    | TPS62160    | WSOP (8)  |
| 1.8 V                         | TPS62161    |           |
| 3.3 V                         | TPS62162    |           |
| 5.0 V                         | TPS62163    |           |
| adjustable                    | TPS62160    | VSSOP (8) |

(1) Contact the factory to check availability of other fixed output voltage versions.

## 6 Pin Configuration and Functions



### Pin Functions

| PIN <sup>(1)</sup>                 |     | I/O | DESCRIPTION   |
|------------------------------------|-----|-----|---|
| NAME                               | NO. |     |   |
| PGND                               | 1   | —   | Power ground  |
| VIN                                | 2   | I   | Supply voltage  |
| EN                                 | 3   | I   | Enable input (High = enabled, Low = disabled)   |
| AGND                               | 4   | —   | Analog ground   |
| FB                                 | 5   | I   | Voltage feedback of adjustable version. Connect resistive voltage divider to this pin. It is recommended to connect FB to AGND on fixed output voltage versions for improved thermal performance. |
| VOS                                | 6   | I   | Output voltage sense pin and connection for the control loop circuitry.   |
| SW                                 | 7   | O   | Switch node, which is connected to the internal MOSFET switches. Connect inductor between SW and output capacitor.  |
| PG                                 | 8   | O   | Output power good (High = VOUT ready, Low = VOUT below nominal regulation); open drain (requires pull-up resistor; goes high impedance, when device is switched off)                              |
| Exposed Thermal Pad <sup>(2)</sup> |     | —   | Must be connected to AGND. Must be soldered to achieve appropriate power dissipation and mechanical reliability.  |

(1) For more information about connecting pins, see [Detailed Description](#) and [Application Information](#) sections.

(2) The exposed thermal pad is available with the DSG package only, not with DGK package.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

|  |  | MIN  | MAX                   | UNIT |
|--|--|------|-----------------------|------|
| Pin voltage range <sup>(2)</sup>               | V <sub>IN</sub>                        | -0.3 | 20                    | V    |
|  | EN, SW (DC)                            | -0.3 | V <sub>IN</sub> + 0.3 | V    |
|  | SW (AC), less than 10ns <sup>(3)</sup> | -2   | 24.5                  |      |
|  | FB, PG, VOS                            | -0.3 | 7                     | V    |
| Power good sink current                        | PG                                     |      | 10                    | mA   |
| Operating junction temperature, T <sub>J</sub> |  | -40  | 150                   | °C   |
| Storage temperature, T <sub>stg</sub>          |  | -65  | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.
- (3) While switching.

### 7.2 ESD Ratings

|  |  | VALUE | UNIT |
|--|--|-------|------|
| V <sub>(ESD)</sub> Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | ±2000 | V    |
|  | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

|  | MIN | NOM | MAX | UNIT |
|--|-----|-----|-----|------|
| Supply Voltage, V <sub>IN</sub>                | 3   |     | 17  | V    |
| Output Voltage, V <sub>OUT</sub>               | 0.9 |     | 6   | V    |
| Operating junction temperature, T <sub>J</sub> | -40 |     | 125 | °C   |

### 7.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TPS6216X   |             | UNIT |
|-------------------------------|--|------------|-------------|------|
|                               |  | DSG (WSON) | DGK (VSSOP) |      |
|                               |  | 8 PINS     | 8 PINS      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 61.8       | 184.3       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 61.3       | 74.6        | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 15.5       | 105.8       | °C/W |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.4        | 13.3        | °C/W |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 15.4       | 104.2       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 8.6        | —           | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

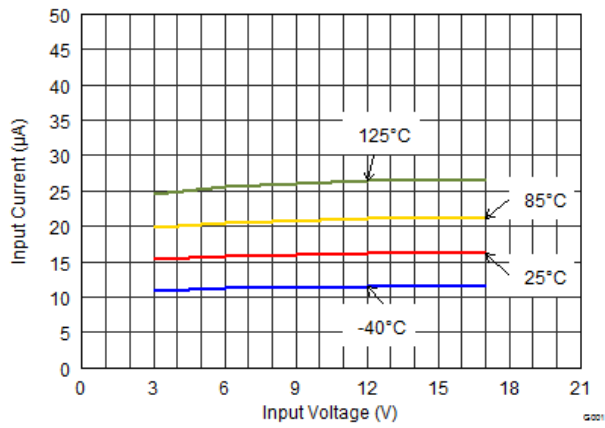
## 7.5 Electrical Characteristics

 Over junction temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ), typical values at  $V_{IN} = 12\text{ V}$  and  $T_J = 25^\circ\text{C}$  (unless otherwise noted)

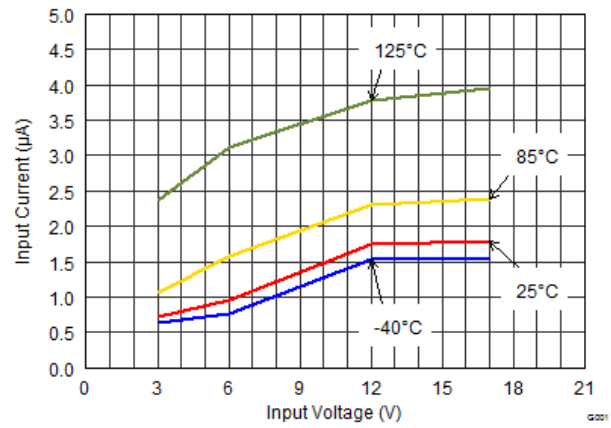
| PARAMETER  |  | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNIT             |
|--|--|--|--|------|------|------------------|
| <b>SUPPLY</b>                                    |  |  |  |      |      |                  |
| $V_{IN}$   | Input voltage range <sup>(1)</sup>   |  | 3  |      | 17   | V                |
| $I_Q$  | Operating quiescent current  | EN = High, $I_{OUT} = 0\text{ mA}$ ,<br>device not switching           |  | 17   | 30   | $\mu\text{A}$    |
|  |  |  | $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | 17   | 25   |                  |
| $I_{SD}$   | Shutdown current <sup>(2)</sup>  | EN = Low   |  | 1.5  | 25   | $\mu\text{A}$    |
|  |  |  | $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ | 1.5  | 4    |                  |
| $V_{UVLO}$                                       | Undervoltage lockout threshold   | Falling input voltage  | 2.6  | 2.7  | 2.82 | V                |
|  |  | Hysteresis   |  | 180  |      | mV               |
| $T_{SD}$   | Thermal shutdown temperature   | Rising temperature   |  | 160  |      | $^\circ\text{C}$ |
|  | Thermal shutdown hysteresis  | Falling temperature  |  | 20   |      |                  |
| <b>CONTROL (EN, PG)</b>                          |  |  |  |      |      |                  |
| $V_{EN\_H}$                                      | High level input threshold voltage (EN)  |  | 0.9  | 0.6  |      | V                |
| $V_{EN\_L}$                                      | Low level input threshold voltage (EN)   |  |  | 0.56 | 0.3  | V                |
| $I_{LKG\_EN}$                                    | Input leakage current (EN)   | EN = $V_{IN}$ or GND   |  | 0.01 | 1    | $\mu\text{A}$    |
| $V_{TH\_PG}$                                     | Power good threshold voltage   | Rising (% $V_{OUT}$ )  | 92%  | 95%  | 98%  |                  |
|  |  | Falling (% $V_{OUT}$ )   | 87%  | 90%  | 93%  |                  |
| $V_{OL\_PG}$                                     | Power good output low voltage  | $I_{PG} = -2\text{ mA}$  |  | 0.07 | 0.3  | V                |
| $I_{LKG\_PG}$                                    | Input leakage current (PG)   | $V_{PG} = 1.8\text{ V}$  |  | 1    | 400  | nA               |
| <b>POWER SWITCH</b>                              |  |  |  |      |      |                  |
| $R_{DS(ON)}$                                     | High-side MOSFET ON-resistance   | $V_{IN} \geq 6\text{ V}$   |  | 300  | 600  | m $\Omega$       |
|  |  | $V_{IN} = 3\text{ V}$  |  | 430  |      |                  |
|  | Low-side MOSFET ON-resistance  | $V_{IN} \geq 6\text{ V}$   |  | 120  | 200  | m $\Omega$       |
|  |  | $V_{IN} = 3\text{ V}$  |  | 165  |      |                  |
| $I_{LIMF}$                                       | High-side MOSFET forward current limit <sup>(3)</sup>  | $V_{IN} = 12\text{ V}$ , $T_J = 25^\circ\text{C}$                      | 1.45   | 1.95 | 2.45 | A                |
| <b>OUTPUT</b>                                    |  |  |  |      |      |                  |
| $V_{REF}$  | Internal reference voltage <sup>(4)</sup>  |  |  | 0.8  |      | V                |
| $I_{LKG\_FB}$                                    | Pin leakage current (FB)   | TPS62160, $V_{FB} = 1.2\text{ V}$                                      |  | 5    | 400  | nA               |
| $V_{OUT}$  | Output voltage range (TPS62160)  | $V_{IN} \geq V_{OUT}$  | 0.9  |      | 6.0  | V                |
|  | Initial output voltage accuracy <sup>(5)</sup>   | PWM mode operation, $V_{IN} \geq V_{OUT} + 1\text{ V}$                 | -3%  |      | 3%   |                  |
|  |  | Power save mode operation, $C_{OUT} = 22\text{ }\mu\text{F}$           | -3.5%  |      | 4%   |                  |
|  | DC output voltage load regulation <sup>(6)</sup>   | $V_{IN} = 12\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , PWM mode operation |  | 0.05 |      | %/A              |
| DC output voltage line regulation <sup>(6)</sup> | $3\text{ V} \leq V_{IN} \leq 17\text{ V}$ , $V_{OUT} = 3.3\text{ V}$ , $I_{OUT} = 0.5\text{ A}$ , PWM mode operation |  | 0.02   |      | %/V  |                  |

- (1) The device is still functional down to under voltage lockout (see parameter  $V_{UVLO}$ ).
- (2) Current into  $V_{IN}$  pin.
- (3) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see [Current Limit and Short Circuit Protection](#) section).
- (4) This is the voltage regulated at the FB pin.
- (5) This is the accuracy provided by the device itself (line and load regulation effects are not included). For fixed voltage versions, the (internal) resistive feedback divider is included.
- (6) Line and load regulation are depending on external component selection and layout (see [Figure 18](#) and [Figure 19](#)).

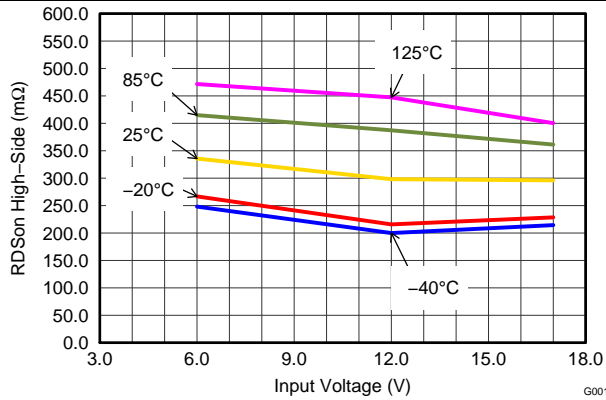
## 7.6 Typical Characteristics



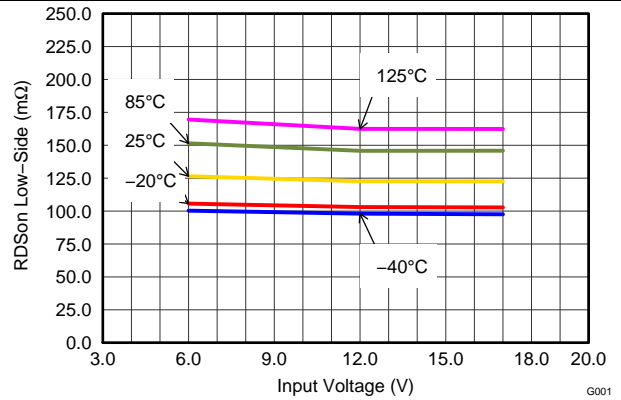
**Figure 1. Quiescent Current**



**Figure 2. Shutdown Current**



**Figure 3. High-Side Switch**



**Figure 4. Low-Side Switch**

## 8 Detailed Description

### 8.1 Overview

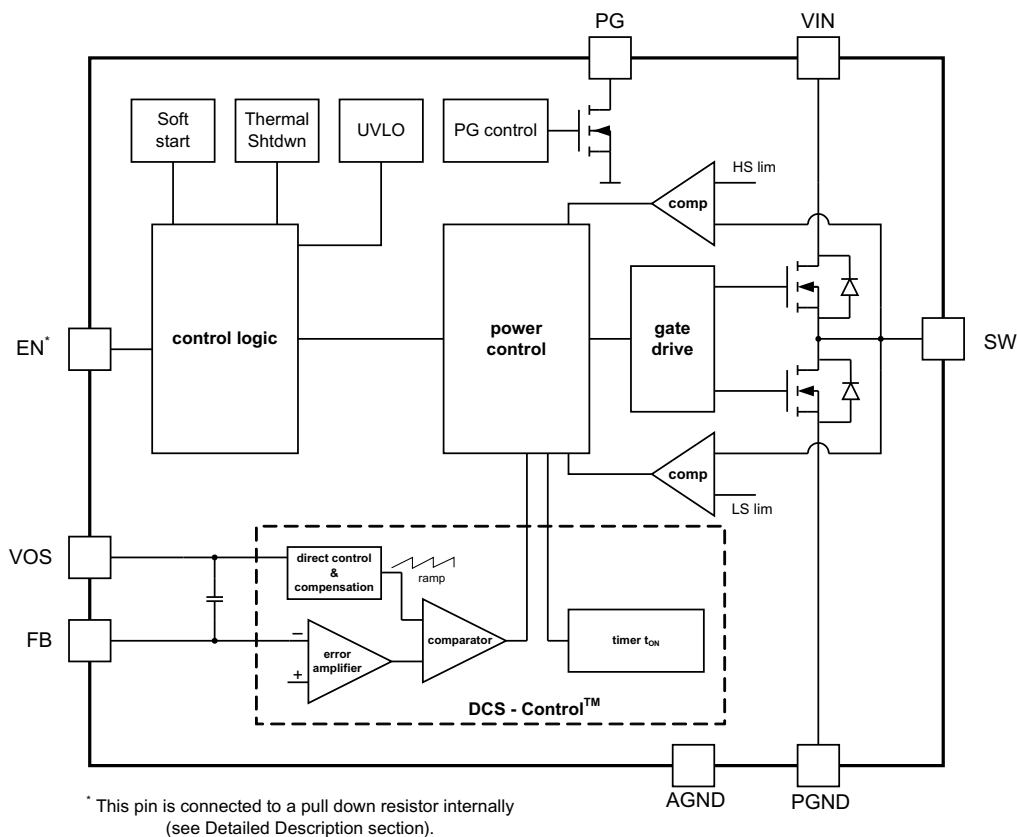
The TPS6216x synchronous step-down DC/DC converters are based on DCS-Control™ (Direct Control with Seamless transition into power save mode), an advanced regulation topology, that combines the advantages of hysteretic, voltage mode and current mode control including an AC loop directly associated to the output voltage. This control loop takes information about output voltage changes and feeds it directly to a fast comparator stage. It sets the switching frequency, which is constant for steady state operating conditions, and provides immediate response to dynamic load changes. To get accurate DC load regulation, a voltage feedback loop is used. The internally compensated regulation network achieves fast and stable operation with small external components and low ESR capacitors.

The DCS-Control™ topology supports pulse width modulation (PWM) mode for medium and heavy load conditions and a power save mode at light loads. During PWM mode, it operates at its nominal switching frequency in continuous conduction mode. This frequency is typically about 2.25 MHz with a controlled frequency variation depending on the input voltage. If the load current decreases, the converter enters power save mode to sustain high efficiency down to very light loads. In power save mode, the switching frequency decreases linearly with the load current. Since DCS-Control™ supports both operation modes within one single building block, the transition from PWM to power save mode is seamless without effects on the output voltage.

Fixed output voltage versions provide smallest solution size and lowest current consumption, requiring only 3 external components. An internal current limit supports nominal output currents of up to 1 A.

The TPS6216x family offers both excellent DC voltage and superior load transient regulation, combined with very low output voltage ripple, minimizing interference with RF circuits.

### 8.2 Functional Block Diagrams



**Figure 5. TPS62160 (Adjustable Output Voltage)**



## Functional Block Diagrams (continued)

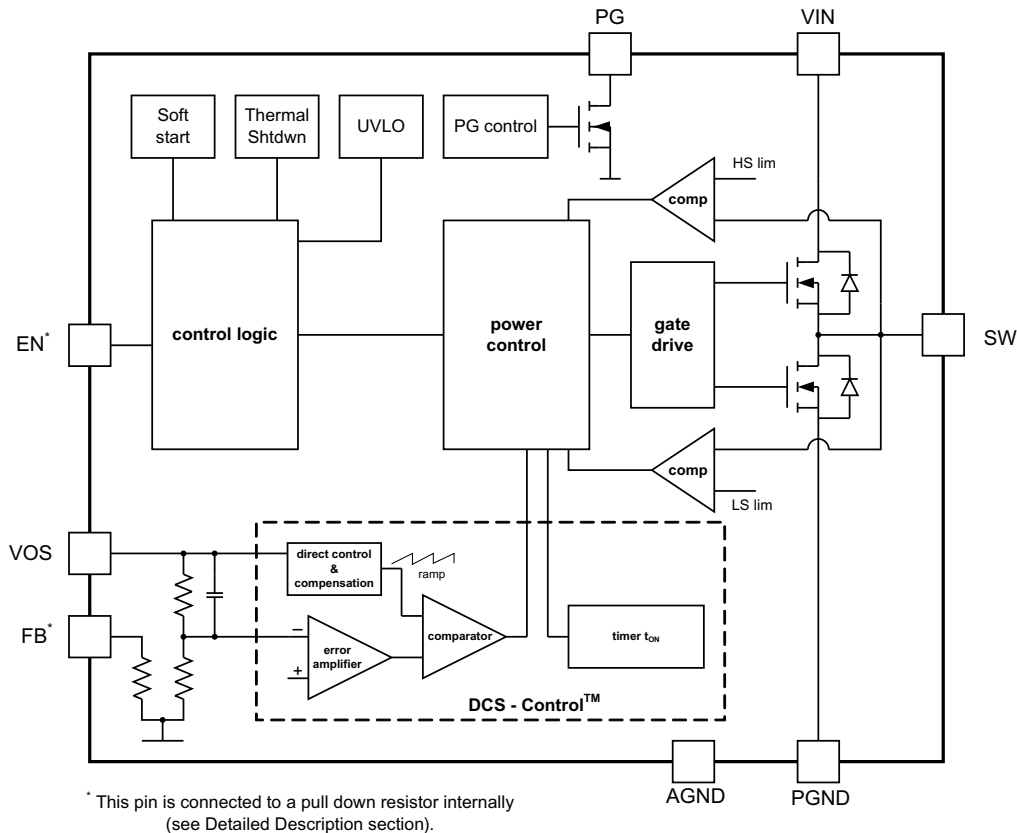


Figure 6. TPS62161/TPS62162/TPS62163 (Fixed Output Voltage)

## 8.3 Feature Description

### 8.3.1 Enable and Shutdown (EN)

When enable (EN) is set high, the device starts operation.

Shutdown is forced if EN is pulled low with a shutdown current of typically 1.5  $\mu\text{A}$ . During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off. The internal resistive divider pulls down the output voltage smoothly. If the EN pin is low, an internal pull-down resistor of about 400 k $\Omega$  is connected and keeps it low, to avoid bouncing.

Connecting the EN pin to an appropriate output signal of another power rail provides sequencing of multiple power rails.

### 8.3.2 Current Limit and Short Circuit Protection

The TPS6216x devices are protected against heavy load and short circuit events. At heavy loads, the current limit determines the maximum output current. If the current limit is reached, the high-side FET is turned off. Avoiding shoot through current, the low-side FET is switched on to allow the inductor current to decrease. The high-side FET turns on again, only if the current in the low-side FET decreases below the low-side current limit threshold of typically 1.2 A.

The output current of the device is limited by the current limit (see [Electrical Characteristics](#)). Due to internal propagation delay, the actual current can exceed the static current limit during that time. The dynamic current limit is calculated as follows:

## Feature Description (continued)

$$I_{peak(typ)} = I_{LIMF} + \frac{V_L}{L} \cdot t_{PD}$$

where

- $I_{LIMF}$  is the static current limit, specified in [Electrical Characteristics](#)
- $L$  is the inductor value
- $V_L$  is the voltage across the inductor
- $t_{PD}$  is the internal propagation delay

(1)

The dynamic high-side switch peak current is calculated as follows:

$$I_{peak(typ)} = I_{LIMF} + \frac{(V_{IN} - V_{OUT})}{L} \cdot 30ns$$

(2)

Take care with the current limit, if the input voltage is high and very small inductances are used.

### 8.3.3 Power Good (PG)

The TPS6216x has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 7 V). It can sink 2 mA of current and maintain its specified logic low level. It is high impedance when the device is turned off due to EN, UVLO or thermal shutdown. If not used, the PG pin should be connected to GND but may be left floating.

**Table 1. Power Good Pin Logic Table**

| Device State         |                                    | PG Logic Status |     |
|----------------------|------------------------------------|-----------------|-----|
|                      |                                    | High Impedance  | Low |
| Enable (EN=High)     | $V_{FB} \geq V_{TH\_PG}$           | √               |     |
|                      | $V_{FB} \leq V_{TH\_PG}$           |                 | √   |
| Shutdown (EN=Low)    |                                    | √               |     |
| UVLO                 | $0.7\text{ V} < V_{IN} < V_{UVLO}$ | √               |     |
| Thermal Shutdown     | $T_J > T_{SD}$                     | √               |     |
| Power Supply Removal | $V_{IN} < 0.7\text{ V}$            | √               |     |

### 8.3.4 Undervoltage Lockout (UVLO)

If the input voltage drops, the under voltage lockout prevents misoperation of the device by switching off both the power FETs. The under voltage lockout threshold is set typically to 2.7 V. The device is fully operational for voltages above the UVLO threshold and turns off if the input voltage trips the threshold. The converter starts operation again once the input voltage exceeds the threshold by a hysteresis of typically 180 mV.

### 8.3.5 Thermal Shutdown

The junction temperature ( $T_J$ ) of the device is monitored by an internal temperature sensor. If  $T_J$  exceeds 160°C (typical), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and PG goes high impedance. When  $T_J$  decreases below the hysteresis amount, the converter resumes normal operation, beginning with soft start. To avoid unstable conditions, a hysteresis of typically 20°C is implemented on the thermal shut down temperature.

## 8.4 Device Functional Modes

### 8.4.1 Soft Start

The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high-impedance power sources or batteries. When EN is set to start device operation, the device starts switching after a delay of about 50  $\mu\text{s}$  and  $V_{\text{OUT}}$  rises with a slope of about 25 mV/ $\mu\text{s}$ . See [Figure 30](#) and [Figure 31](#) for typical startup operation.

The TPS6216x can start into a pre-biased output. During monotonic pre-biased startup, the low-side MOSFET is not allowed to turn on until the device's internal ramp sets an output voltage above the pre-bias voltage.

### 8.4.2 Pulse Width Modulation (PWM) Operation

The TPS6216x operates with pulse width modulation in continuous conduction mode (CCM) with a nominal switching frequency of about 2.25 MHz. The frequency variation in PWM is controlled and depends on  $V_{\text{IN}}$ ,  $V_{\text{OUT}}$  and the inductance. The device operates in PWM mode as long the output current is higher than half the inductor's ripple current. To maintain high efficiency at light loads, the device enters power save mode at the boundary to discontinuous conduction mode (DCM). This happens if the output current becomes smaller than half the inductor's ripple current.

### 8.4.3 Power Save Mode Operation

The TPS6216x's built in power save mode is entered seamlessly, if the load current decreases. This secures a high efficiency in light load operation. The device remains in power save mode as long as the inductor current is discontinuous.

In power save mode the switching frequency decreases linearly with the load current maintaining high efficiency. The transition into and out of power save mode happens within the entire regulation scheme and is seamless in both directions.

The TPS6216x includes a fixed on-time circuitry. This on-time, in steady-state operation, is estimated as:

$$t_{\text{ON}} = \frac{V_{\text{OUT}}}{V_{\text{IN}}} \cdot 420\text{ns} \quad (3)$$

For very small output voltages, the on-time increases beyond the result of [Equation 3](#), to stay above an absolute minimum on-time,  $t_{\text{ON}(\text{min})}$ , which is around 80 ns, to limit switching losses. The peak inductor current in PSM is approximated by:

$$I_{\text{LPSM}(\text{peak})} = \frac{(V_{\text{IN}} - V_{\text{OUT}})}{L} \cdot t_{\text{ON}} \quad (4)$$

When  $V_{\text{IN}}$  decreases to typically 15% above  $V_{\text{OUT}}$ , the TPS6216x does not enter power save mode, regardless of the load current. The device maintains output regulation in PWM mode.

### 8.4.4 100% Duty-Cycle Operation

The duty cycle of the buck converter is given by  $D = V_{\text{OUT}}/V_{\text{IN}}$  and increases as the input voltage comes close to the output voltage. In this case, the device starts 100% duty cycle operation turning on the high-side switch 100% of the time. The high-side switch stays turned on as long as the output voltage is below the internal setpoint. This allows the conversion of small input to output voltage differences, such as for longest operation time of battery-powered applications. In 100% duty cycle mode, the low-side FET is switched off.

The minimum input voltage to maintain output voltage regulation, depending on the load current and the output voltage level, is calculated as:

**Device Functional Modes (continued)**

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} (R_{DS(on)} + R_L)$$

where

- $I_{OUT}$  is the output current
- $R_{DS(on)}$  is the  $R_{DS(on)}$  of the high-side FET
- $R_L$  is the DC resistance of the inductor used

(5)

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS6216x device family are easy to use synchronous step-down DC/DC converters optimized for applications with high power density. A high switching frequency of typically 2.25 MHz allows the use of small inductors and provides fast transient response as well as high output voltage accuracy by utilization of the DCS-Control™ topology. With its wide operating input voltage range of 3 V to 17 V, the devices are ideally suited for systems powered from either a Li-Ion or other battery as well as from 12-V intermediate power rails. It supports up to 1-A continuous output current at output voltages between 0.9 V and 6 V (with 100% duty cycle mode).

### 9.2 Typical Application

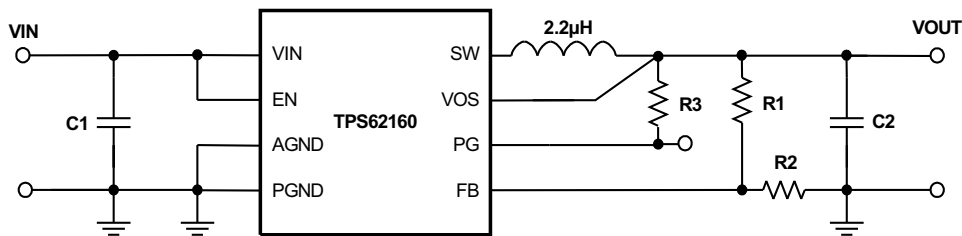


Figure 7. TPS62160 Adjustable Power Supply

#### 9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the [Recommended Operating Conditions](#).

#### 9.2.2 Detailed Design Procedure

##### 9.2.2.1 Custom Design with WEBENCH® Tools

[Click here](#) to create a custom design using the TPS62160 device with the WEBENCH® Power Designer.

1. Start by entering your  $V_{IN}$ ,  $V_{OUT}$ , and  $I_{OUT}$  requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
  - Run electrical simulations to see important waveforms and circuit performance
  - Run thermal simulations to understand the thermal performance of your board
  - Export your customized schematic and layout into popular CAD formats
  - Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at [www.ti.com/WEBENCH](http://www.ti.com/WEBENCH).

## Typical Application (continued)

### 9.2.2.2 Programming the Output Voltage

While the output voltage of the TPS62160 is adjustable, the TPS62161/TPS62162/TPS62163 are programmed to fixed output voltages. For fixed output versions, the FB pin is pulled down internally and may be left floating. It is recommended to connect it to AGND to improve thermal resistance. The adjustable version can be programmed for output voltages from 0.9 V to 6 V by using a resistive divider from VOUT to AGND. The voltage at the FB pin is regulated to 800 mV. The value of the output voltage is set by the selection of the resistive divider from [Equation 6](#). It is recommended to choose resistor values which allow a current of at least 2  $\mu$ A, meaning the value of R2 should not exceed 400 k $\Omega$ . Lower resistor values are recommended for highest accuracy and most robust design. For applications requiring lowest current consumption, the use of fixed output voltage versions is recommended.

$$R_1 = R_2 \left( \frac{V_{OUT}}{0.8V} - 1 \right) \quad (6)$$

If the FB pin becomes open, the device clamps the output voltage at the VOS pin to about 7.4 V.

### 9.2.2.3 External Component Selection

The external components have to fulfill the needs of the application, but also the stability criteria of the devices control loop. The TPS6216x is optimized to work within a range of external components. The LC output filter's inductance and capacitance have to be considered together, creating a double pole, responsible for the corner frequency of the converter (see [Output Filter and Loop Stability](#) section). [Table 2](#) can be used to simplify the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations should be checked for each individual application.

**Table 2. Recommended LC Output Filter Combinations<sup>(1)</sup>**

|             | 4.7 $\mu$ F | 10 $\mu$ F | 22 $\mu$ F       | 47 $\mu$ F | 100 $\mu$ F | 200 $\mu$ F | 400 $\mu$ F |
|-------------|-------------|------------|------------------|------------|-------------|-------------|-------------|
| 1 $\mu$ H   |             |            |                  |            |             |             |             |
| 2.2 $\mu$ H |             | √          | √ <sup>(2)</sup> | √          | √           | √           |             |
| 3.3 $\mu$ H |             | √          | √                | √          | √           |             |             |
| 4.7 $\mu$ H |             |            |                  |            |             |             |             |

(1) The values in the table are nominal values. Variations of typically  $\pm 20\%$  due to tolerance, saturation and DC bias are assumed.

(2) This LC combination is the standard value and recommended for most applications.

More detailed information on further LC combinations can be found in [SLVA463](#).

### 9.2.2.4 Inductor Selection

The inductor selection is affected by several effects like inductor ripple current, output ripple voltage, PWM-to-PSM transition point and efficiency. In addition, the inductor selected has to be rated for appropriate saturation current and DC resistance (DCR). [Equation 7](#) and [Equation 8](#) calculate the maximum inductor current under static load conditions.

$$I_{L(max)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (7)$$

$$\Delta I_{L(\max)} = V_{OUT} \cdot \left( \frac{1 - \frac{V_{OUT}}{V_{IN(\max)}}}{L_{(\min)} \cdot f_{SW}} \right)$$

where

- $I_L(\max)$  is the maximum inductor current
- $\Delta I_L$  is the peak-to-peak inductor ripple current
- $L(\min)$  is the minimum effective inductor value
- $f_{SW}$  is the actual PWM switching frequency

(8)

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. A margin of about 20% is recommended to add. A larger inductor value is also useful to get lower ripple current, but increases the transient response time and size as well. The following inductors have been used with the TPS6216x and are recommended for use:

**Table 3. List of Inductors<sup>(1)</sup>**

| Type               | Inductance [ $\mu\text{H}$ ]   | Current [A] <sup>(2)</sup> | Dimensions [L x B x H] mm | Manufacturer |
|--------------------|--------------------------------|----------------------------|---------------------------|--------------|
| VLF3012ST-2R2M1R4  | 2.2 $\mu\text{H}$ , $\pm 20\%$ | 1.9 A                      | 3.0 x 2.8 x 1.2           | TDK          |
| VLF302512MT-2R2M   | 2.2 $\mu\text{H}$ , $\pm 20\%$ | 1.9 A                      | 3.0 x 2.5 x 1.2           | TDK          |
| VLS252012T-2R2M1R3 | 2.2 $\mu\text{H}$ , $\pm 20\%$ | 1.3 A                      | 2.5 x 2.0 x 1.2           | TDK          |
| XFL3012-222MEC     | 2.2 $\mu\text{H}$ , $\pm 20\%$ | 1.9 A                      | 3.0 x 3.0 x 1.2           | Coilcraft    |
| XFL3012-332MEC     | 3.3 $\mu\text{H}$ , $\pm 20\%$ | 1.6 A                      | 3.0 x 3.0 x 1.2           | Coilcraft    |
| LPS3015-332ML_     | 3.3 $\mu\text{H}$ , $\pm 20\%$ | 1.4 A                      | 3.0 x 3.0 x 1.4           | Coilcraft    |
| NR3015T-2R2M       | 2.2 $\mu\text{H}$ , $\pm 20\%$ | 1.5 A                      | 3.0 x 3.0 x 1.5           | Taiyo Yuden  |
| 744025003          | 3.3 $\mu\text{H}$ , $\pm 20\%$ | 1.5 A                      | 2.8 x 2.8 x 2.8           | Wuerth       |
| PSI25201B-2R2MS    | 2.2 $\mu\text{H}$ , $\pm 20\%$ | 1.3 A                      | 2.0 x 2.5 x 1.2           | Cyntec       |

(1) See the [Third-Party Products Disclaimer](#).

(2)  $I_{RMS}$  at 40°C rise or  $I_{SAT}$  at 30% drop.

The TPS6216x can operate with an inductor as low as 2.2  $\mu\text{H}$ . However, for applications with low input voltages, 3.3  $\mu\text{H}$  is recommended to allow the full output current. The inductor value also determines the load current at which Power Save Mode is entered:

$$I_{load(PSM)} = \frac{1}{2} \Delta I_L$$

(9)

Using [Equation 8](#), this current level is adjusted by changing the inductor value.

### 9.2.2.5 Capacitor Selection

#### 9.2.2.5.1 Output Capacitor

The recommended value for the output capacitor is 22  $\mu\text{F}$ . The architecture of the TPS6216x allows the use of tiny ceramic output capacitors with low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep its low resistance up to high frequencies and to get narrow capacitance variation with temperature, it is recommended to use an X7R or X5R dielectric. Using a higher value can have some advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode (see [SLVA463](#)).

Note: In power save mode, the output voltage ripple depends on the output capacitance, its ESR and the peak inductor current. Using ceramic capacitors provides small ESR and low ripple.

### 9.2.2.5.2 Input Capacitor

For most applications, 10  $\mu\text{F}$  is sufficient and is recommended, though a larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR multilayer ceramic capacitor is recommended for best filtering and should be placed between VIN and PGND as close as possible to those pins.

---

#### NOTE

**DC bias effect:** High capacitance ceramic capacitors have a DC bias effect, which has a strong influence on the final effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with dielectric material are responsible for differences between the rated capacitor value and the effective capacitance.

---

### 9.2.2.6 Output Filter and Loop Stability

The devices of the TPS6216x family are internally compensated to be stable with L-C filter combinations corresponding to a corner frequency calculated with [Equation 10](#):

$$f_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \quad (10)$$

Proven nominal values for inductance and ceramic capacitance are given in [Table 2](#) and are recommended for use. Different values may work, but care has to be taken on the loop stability which is affected. More information including a detailed L-C stability matrix is found in [SLVA463](#).

The TPS6216X devices, both fixed and adjustable versions, include an internal 25 pF feed forward capacitor, connected between the VOS and FB pins. This capacitor impacts the frequency behavior and sets a pole and zero in the control loop with the resistors of the feedback divider, per [Equation 11](#) and [Equation 12](#):

$$f_{zero} = \frac{1}{2\pi \cdot R_1 \cdot 25\text{pF}} \quad (11)$$

$$f_{pole} = \frac{1}{2\pi \cdot 25\text{pF}} \cdot \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \quad (12)$$

Though the TPS6216x devices are stable without the pole and zero being in a particular location, adjusting their location to the specific needs of the application can provide better performance in power save mode and/or improved transient response. An external feed-forward capacitor can also be added. A more detailed discussion on the optimization for stability versus transient response can be found in [SLVA289](#) and [SLVA466](#).

If using ceramic capacitors, the DC bias effect has to be considered. The DC bias effect results in a drop in effective capacitance as the voltage across the capacitor increases (see **NOTE** in [Input Capacitor](#) section).

### 9.2.2.7 TPS6216x Components List

[Table 4](#) shows the list of components for the [Application Curves](#).



**Table 4. List of Components**

| REFERENCE | DESCRIPTION                                | MANUFACTURER                   |
|-----------|--|--------------------------------|
| IC        | 17 V, 1 A Step-Down Converter, WSON        | TPS62160DSG, Texas Instruments |
| L1        | 2.2 $\mu$ H, 1.4 A, 3 mm x 2.8 mm x 1.2 mm | VLF3012ST-2R2M1R4, TDK         |
| C1        | 10 $\mu$ F, 25 V, Ceramic, 0805            | Standard                       |
| C2        | 22 $\mu$ F, 6.3 V, Ceramic, 0805           | Standard                       |
| R1        | depending on $V_{OUT}$                     |                                |
| R2        | depending on $V_{OUT}$                     |                                |
| R3        | 100 k $\Omega$ , Chip, 0603, 1/16 W, 1%    | Standard                       |

### 9.2.3 Application Curves

$V_{IN}=12\text{ V}$ ,  $V_{OUT}=3.3\text{ V}$ ,  $T_A=25^\circ\text{C}$ , (unless otherwise noted)

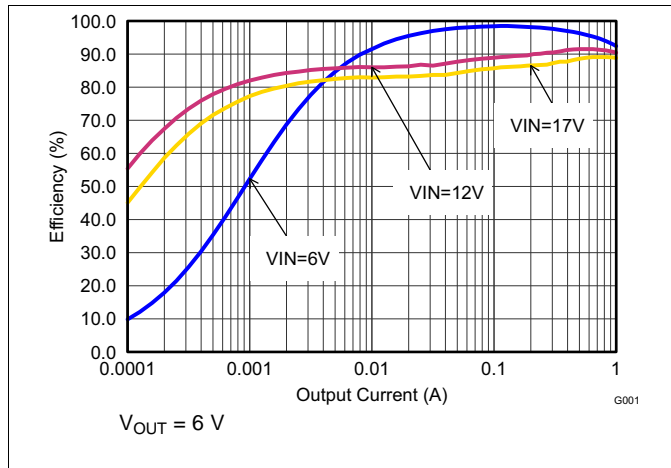


Figure 8. Efficiency vs Output Current

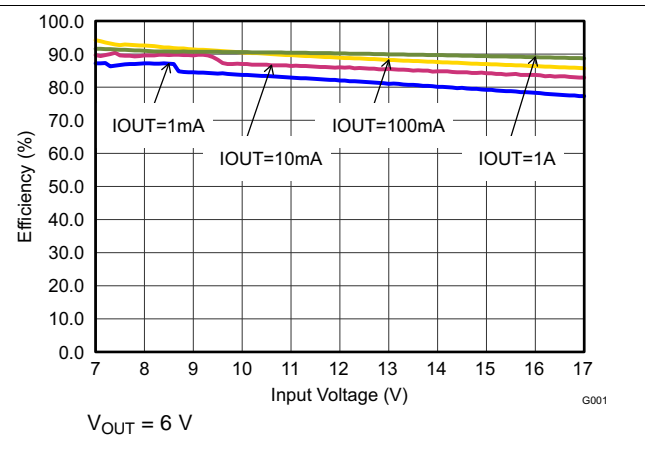


Figure 9. Efficiency vs Input Voltage

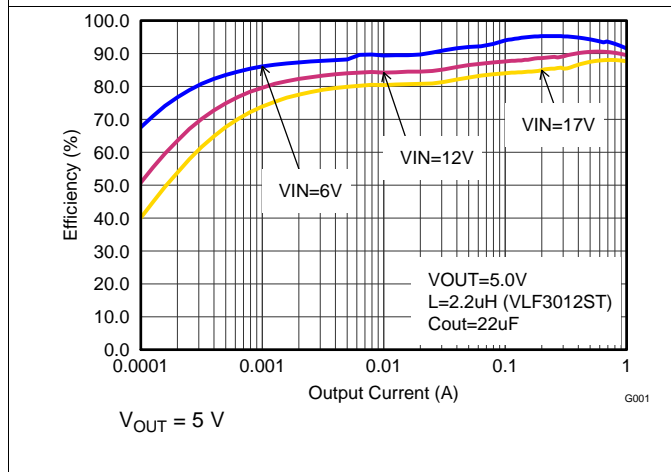


Figure 10. Efficiency vs Output Current

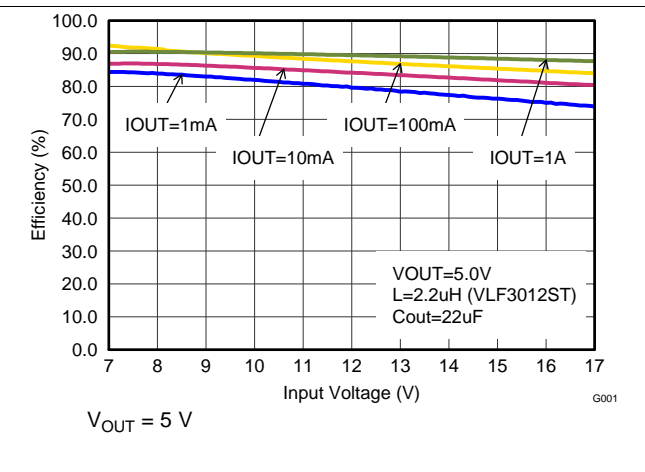


Figure 11. Efficiency vs Input Voltage

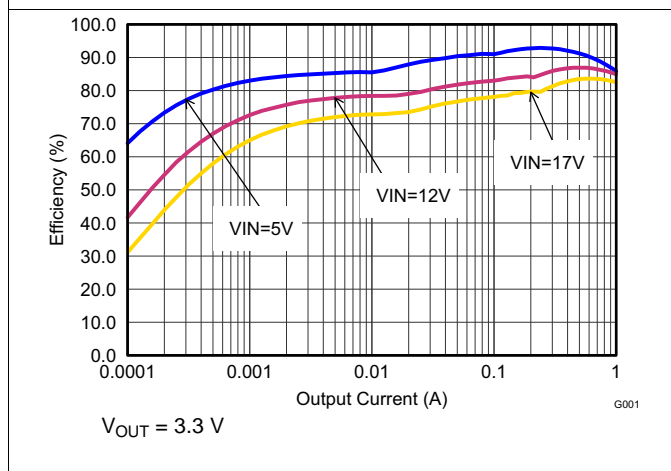


Figure 12. Efficiency vs Output Current

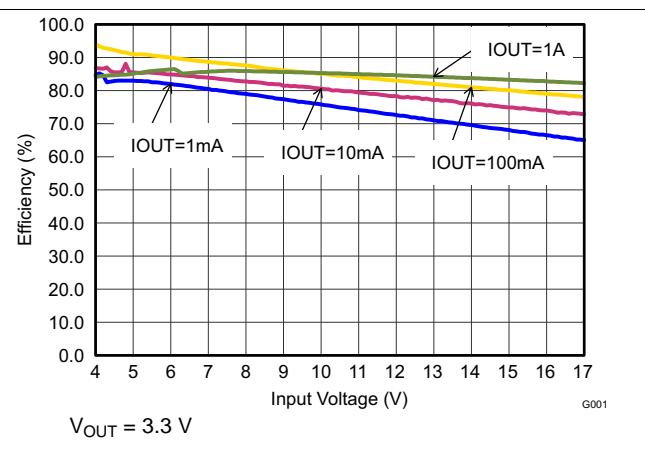


Figure 13. Efficiency vs Input Voltage

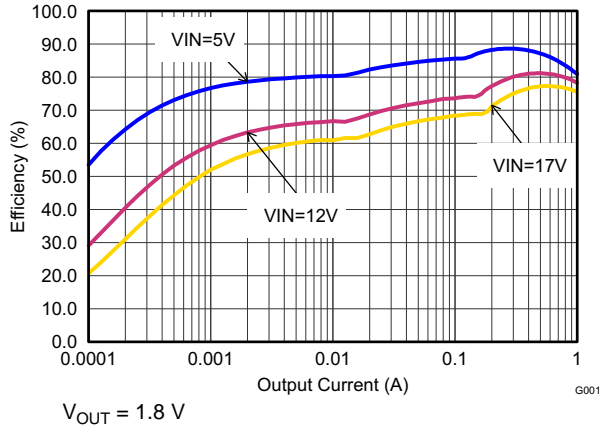


Figure 14. Efficiency vs Output Current

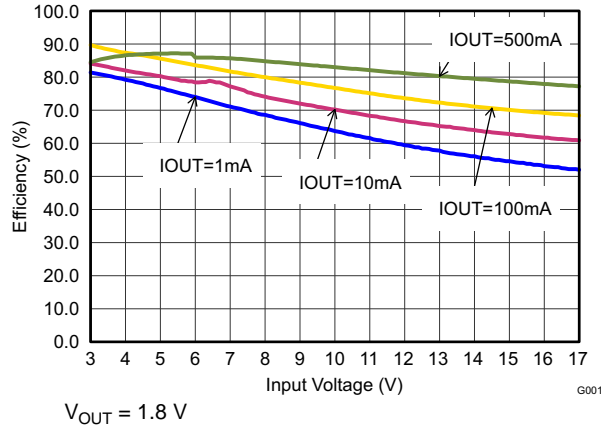


Figure 15. Efficiency vs Input Voltage

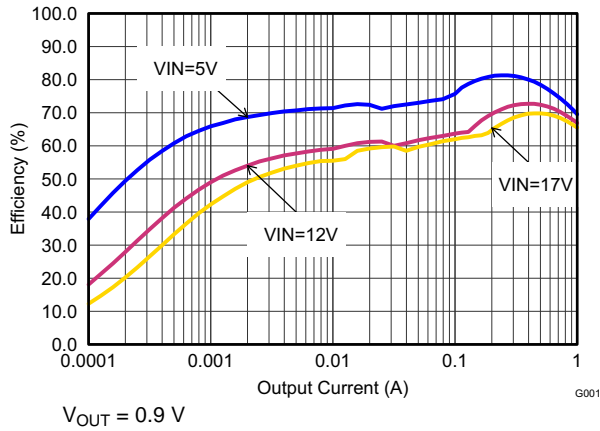


Figure 16. Efficiency vs Output Current

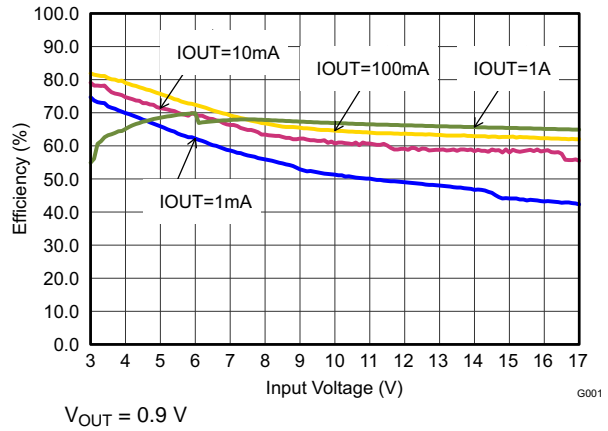


Figure 17. Efficiency vs Input Voltage

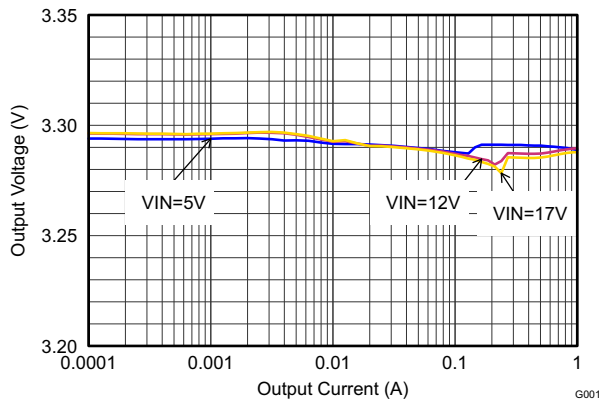


Figure 18. Output Voltage Accuracy (Load Regulation)

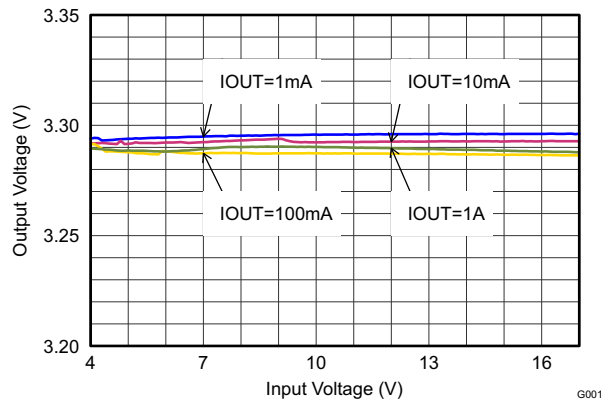


Figure 19. Output Voltage Accuracy (Line Regulation)

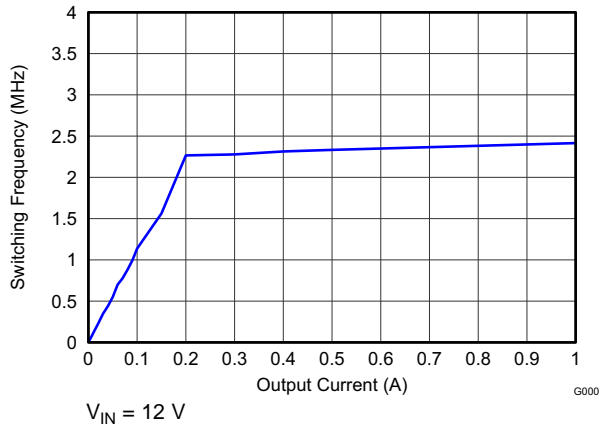


Figure 20. Switching Frequency

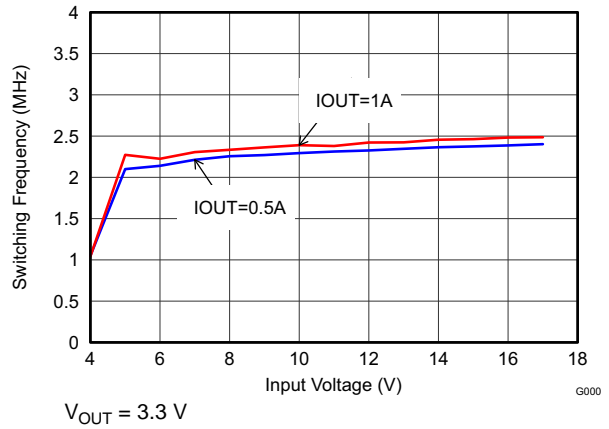


Figure 21. Switching Frequency

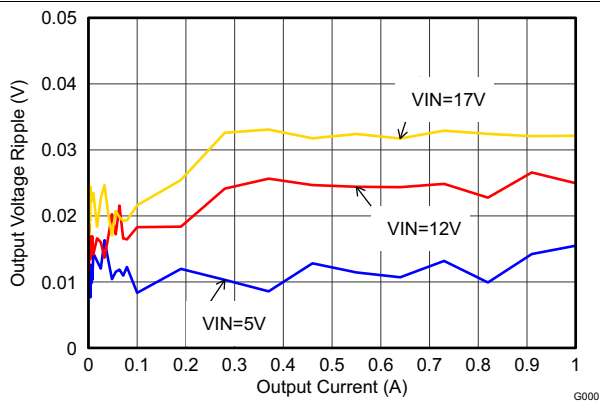


Figure 22. Output Voltage Ripple

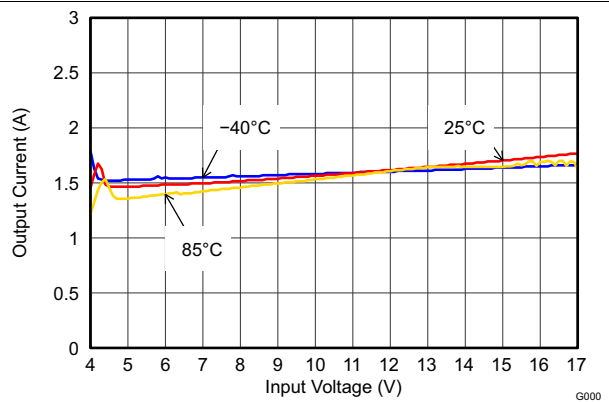


Figure 23. Maximum Output Current

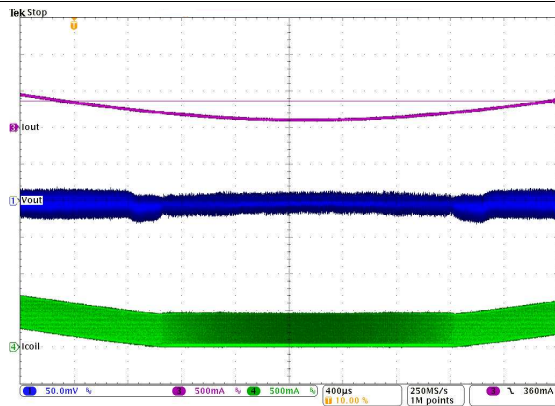


Figure 24. PWM to PSM Mode Transition

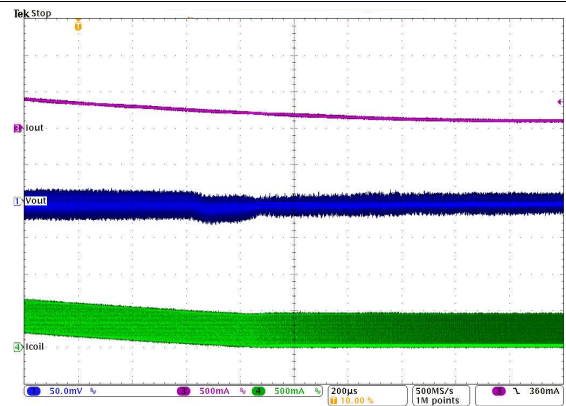


Figure 25. PSM to PWM Mode Transition

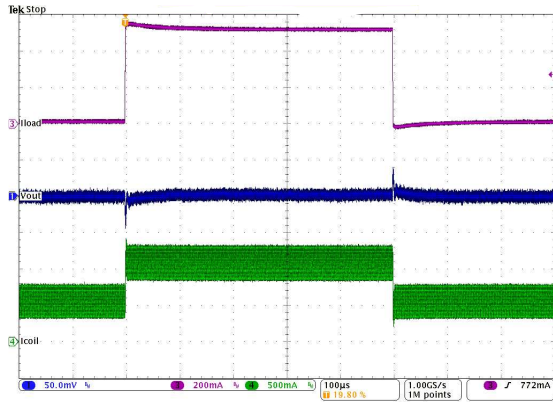


Figure 26. Load Transient Response in PWM Mode (500 mA to 1 A)

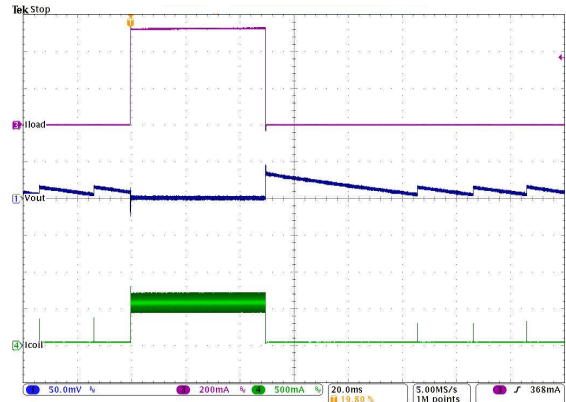


Figure 27. Load Transient Response from Power Save Mode (100 mA to 500 mA)

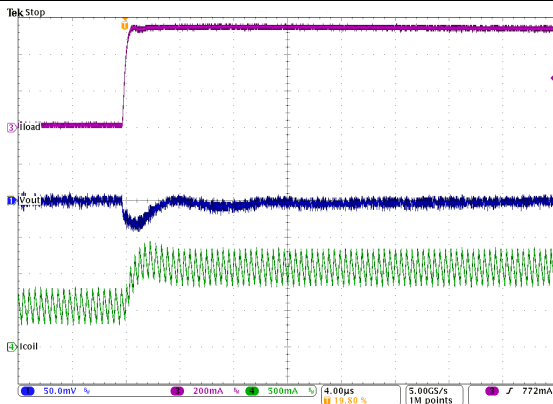


Figure 28. Load Transient Response in PWM Mode (500 mA to 1 A), Rising Edge

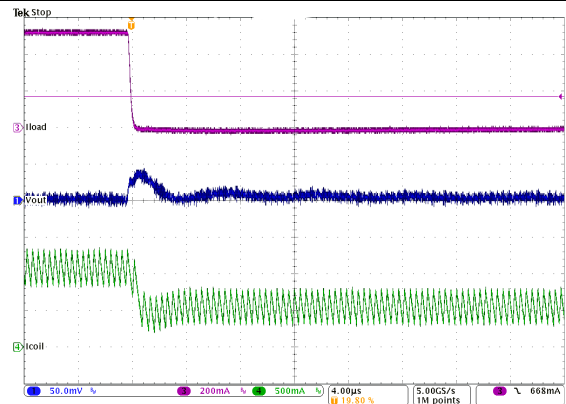


Figure 29. Load Transient Response in PWM Mode (500 mA to 1 A), Falling Edge

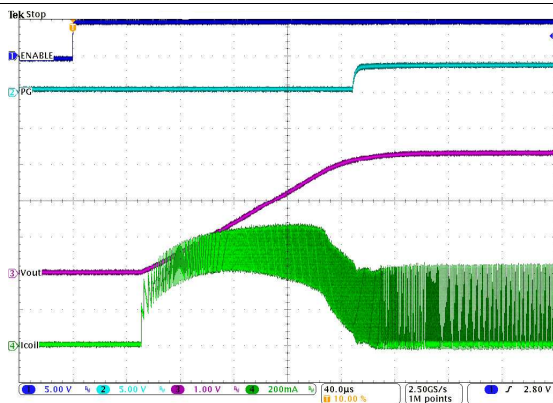


Figure 30. Startup with  $I_{OUT} = 100$  mA

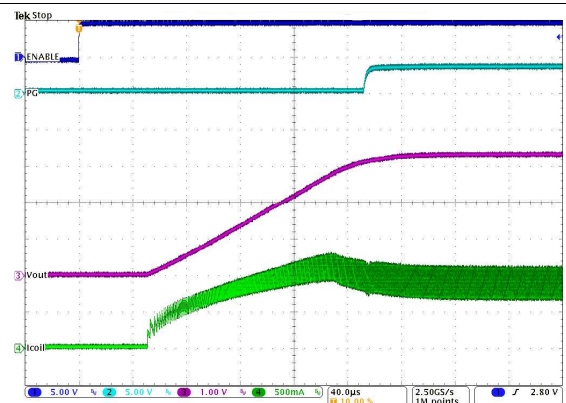
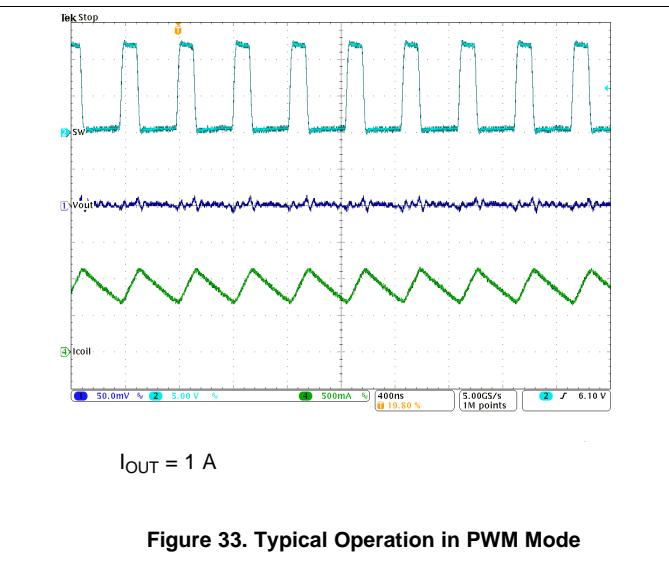
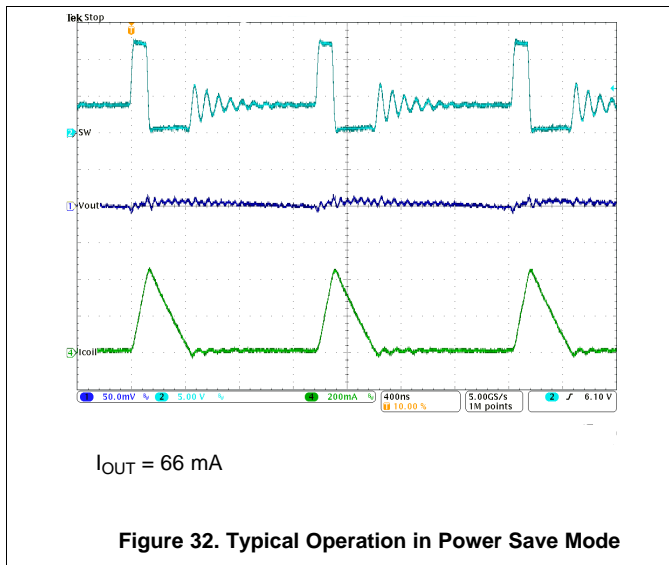


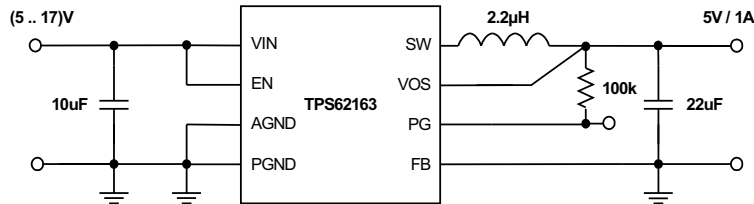
Figure 31. Startup with  $I_{OUT} = 1$  A



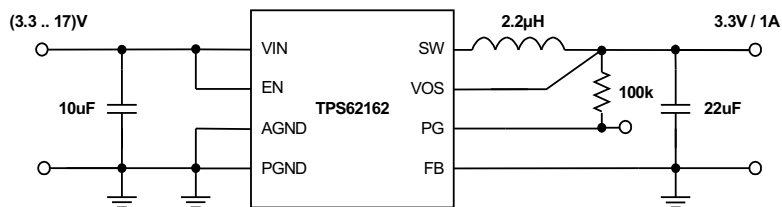
### 9.3 System Examples

#### 9.3.1 1-A Power Supply

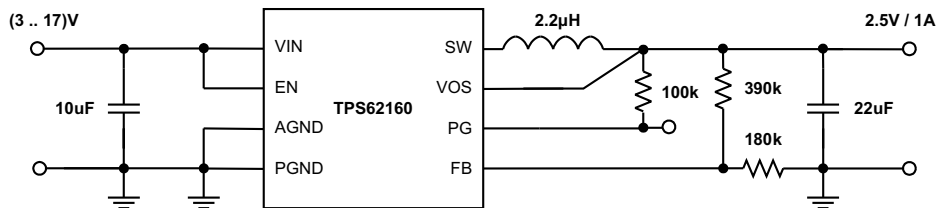
The following example circuits show various TPS6216x devices and input voltages that provide a 1-A power supply with output voltage options.



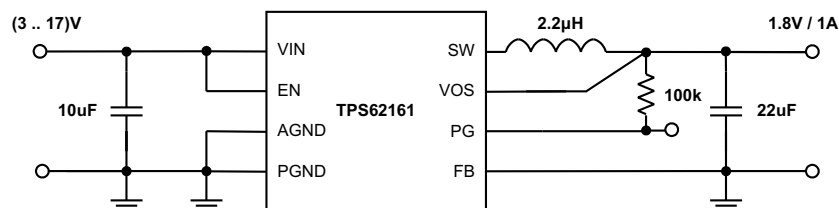
**Figure 34. 5 V / 1 A Power Supply**



**Figure 35. 3.3 V / 1 A Power Supply**



**Figure 36. 2.5 V / 1 A Power Supply**



**Figure 37. 1.8 V / 1 A Power Supply**

System Examples (continued)

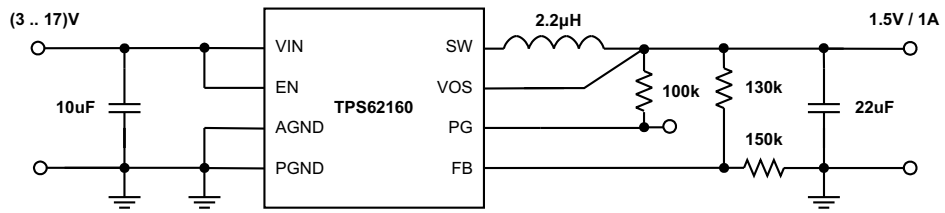


Figure 38. 1.5 V / 1 A Power Supply

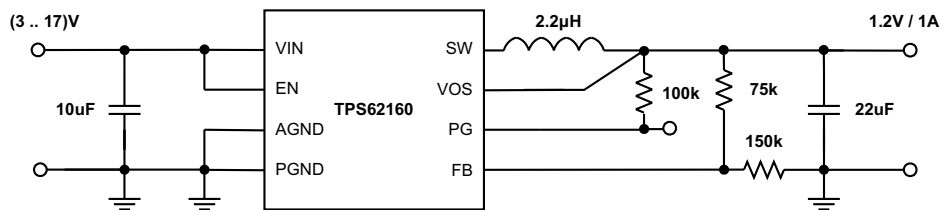


Figure 39. 1.2 V / 1 A Power Supply

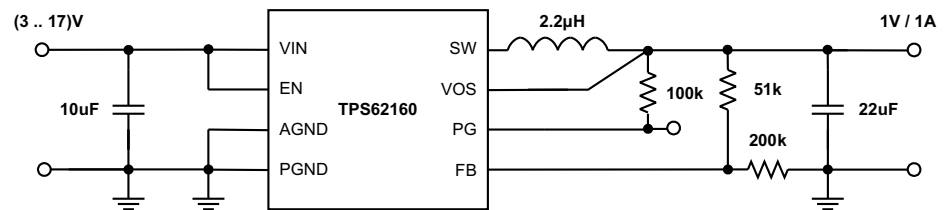


Figure 40. 1 V / 1 A Power Supply



## System Examples (continued)

### 9.3.2 Inverting Power Supply

The TPS6216x can be used as inverting power supply by rearranging external circuitry as shown in Figure 41. As the former GND node now represents a voltage level below system ground, the voltage difference between  $V_{IN}$  and  $V_{OUT}$  has to be limited for operation to the maximum supply voltage of 17 V (see Equation 13).

$$V_{IN} + |V_{OUT}| \leq V_{INmax} \quad (13)$$

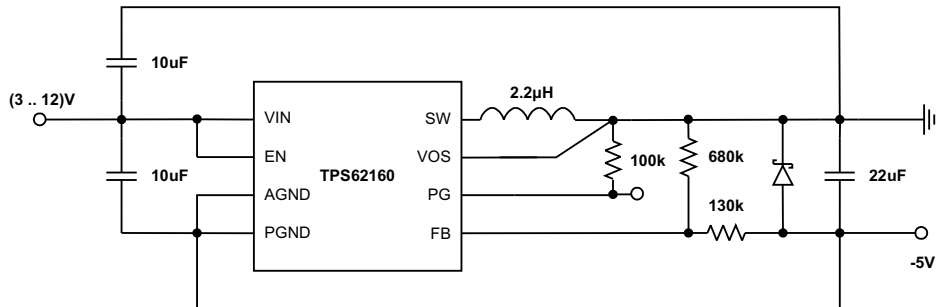


Figure 41. -5 V Inverting Power Supply

The transfer function of the inverting power supply configuration differs from the buck mode transfer function, incorporating a right half plane zero additionally. The loop stability has to be adapted and an output capacitance of at least 22  $\mu$ F is recommended. A detailed design example is given in [SLVA469](#).

## 10 Power Supply Recommendations

The TPS6216x device family has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage, and output current of the TPS6216x.

## 11 Layout

### 11.1 Layout Guidelines

A proper layout is critical for the operation of a switched mode power supply, even more at high switching frequencies. Therefore the PCB layout of the TPS6216x demands careful attention to ensure operation and to get the performance specified. A poor layout can lead to issues like poor regulation (both line and load), stability and accuracy weaknesses, increased EMI radiation, and noise sensitivity.

Provide low inductive and resistive paths to ground for loops with high  $di/dt$ . Therefore paths conducting the switched load current should be as short and wide as possible. Provide low capacitive paths, with respect to all other nodes, for wires with high  $dv/dt$ . Therefore the input and output capacitance should be placed as close as possible to the IC pins and parallel wiring over long distances as well as narrow traces should be avoided. Loops which conduct an alternating current should outline an area as small as possible, as this area is proportional to the energy radiated.

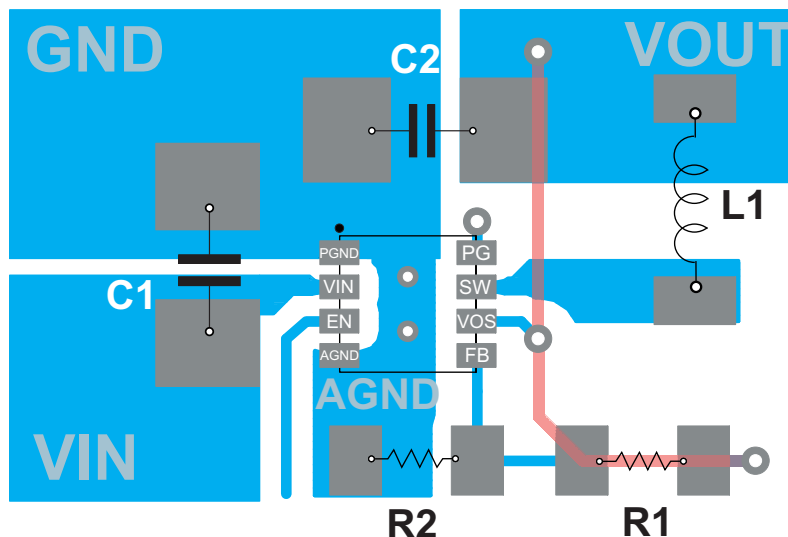
Also sensitive nodes like FB and VOS should be connected with short wires, not nearby high  $dv/dt$  signals, such as SW. As they carry information about the output voltage, they should be connected as close as possible to the actual output voltage (at the output capacitor). Signals not assigned to power transmission, such as the feedback divider, should refer to the signal ground (AGND) and always be separated from the power ground (PGND).

In summary, the input capacitor should be placed as close as possible to the VIN and PGND pin of the IC. This connections should be done with wide and short traces. The output capacitor should be placed such that its ground is as close as possible to the IC's PGND pins - avoiding additional voltage drop in traces. This connection should also be made short and wide. The inductor should be placed close to the SW pin and connect directly to the output capacitor - minimizing the loop area between the SW pin, inductor, output capacitor and PGND pin. The feedback resistors,  $R_1$  and  $R_2$ , should be placed close to the IC and connect directly to the AGND and FB pins. Those connections (including VOUT) to the resistors and especially to the VOS pin should stay away from noise sources, such as the inductor. The VOS pin should connect in the shortest way to VOUT at the output capacitor, while the VOUT connection to the feedback divider can connect at the load.

A single point grounding scheme should be implemented with all grounds (AGND, PGND and the thermal pad) connecting at the IC's exposed thermal pad. See [Figure 42](#) for the recommended layout of the TPS6216x. More detailed information can be found in the EVM Users Guide, [SLVU483](#).

The exposed thermal pad must be soldered to the circuit board for mechanical reliability and to achieve appropriate power dissipation. Although the exposed thermal pad can be connected to a floating circuit board trace, the device has better thermal performance if it is connected to a larger ground plane. The exposed thermal pad is electrically connected to AGND.

### 11.2 Layout Example



**Figure 42. TPS6216x Board Layout**

### 11.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB by soldering the exposed thermal pad
- Introducing airflow in the system

For more details on how to use the thermal parameters, see the application reports *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs*, [SZZA017](#) and *Semiconductor and IC Package Thermal Metrics*, [SPRA953](#).

The TPS6216x is designed for a maximum operating junction temperature ( $T_J$ ) of 125°C. Therefore the maximum output power is limited by the power losses that can be dissipated over the actual thermal resistance, given by the package and the surrounding PCB structures. If the thermal resistance of the package is given, the size of the surrounding copper area and a proper thermal connection of the IC can reduce the thermal resistance. To get an improved thermal behavior, TI recommends to use top layer metal to connect the device with wide and thick metal lines. Internal ground layers can connect to vias directly under the IC for improved thermal performance.

If short circuit or overload conditions are present, the device is protected by limiting internal power dissipation.

## 12 デバイスおよびドキュメントのサポート

### 12.1 WEBENCH®ツールによるカスタム設計

[ここをクリック](#)すると、WEBENCH® Power Designerにより、TPS62160デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧( $V_{IN}$ )、出力電圧( $V_{OUT}$ )、出力電流( $I_{OUT}$ )の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他のソリューションと比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

ほとんどの場合、次の操作を実行可能です。

- 電氣的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットでエクスポートする。
- 設計のレポートをPDFで印刷し、同僚と設計を共有する。

WEBENCHツールの詳細は、[www.ti.com/WEBENCH](http://www.ti.com/WEBENCH)でご覧になれます。

### 12.2 デバイス・サポート

#### 12.2.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

### 12.3 ドキュメントのサポート

#### 12.3.1 関連資料

関連資料については、以下を参照してください：

- 『TPS62130/40/50/60/70の出力フィルタの最適化』、[SLVA463](#)
- 『内部的に補正される、フィードフォワード・コンデンサを持つDC/DCコンバータの過渡応答の最適化』、[SLVA289](#)
- 『フィードフォワード・コンデンサを使用してTPS62130/40/50/60/70の安定性と帯域幅を改善する方法』、[SLVA466](#)
- 『JEDEC PCB設計を使用するリニアおよびロジック・パッケージの熱特性』、[SZZA017](#)

#### 12.4 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 5. 関連リンク

| 製品       | プロダクト・フォルダ              | サンプルとご購入                | 技術資料                    | ツールとソフトウェア              | サポートとコミュニティ             |
|----------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| TPS62160 | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| TPS62161 | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| TPS62162 | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |
| TPS62163 | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> | <a href="#">ここをクリック</a> |

### 12.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™オンライン・コミュニティ** *TIのE2E ( Engineer-to-Engineer )* コミュニティ。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることが出来ます。

## コミュニティ・リソース (continued)

**設計サポート** TIの設計サポート役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

### 12.6 商標

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### 12.7 静電気放電に関する注意事項



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### 12.8 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS62160DGKR     | ACTIVE        | VSSOP        | DGK             | 8    | 2500        | RoHS & Green    | NIPDAUAG   SN                        | Level-1-260C-UNLIM   | -40 to 125   | 62160                   | <a href="#">Samples</a> |
| TPS62160DGKT     | ACTIVE        | VSSOP        | DGK             | 8    | 250         | RoHS & Green    | NIPDAUAG   SN                        | Level-1-260C-UNLIM   | -40 to 125   | 62160                   | <a href="#">Samples</a> |
| TPS62160DSGR     | ACTIVE        | WSON         | DSG             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | QTV                     | <a href="#">Samples</a> |
| TPS62160DSGT     | ACTIVE        | WSON         | DSG             | 8    | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | QTV                     | <a href="#">Samples</a> |
| TPS62161DSGR     | ACTIVE        | WSON         | DSG             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | QUB                     | <a href="#">Samples</a> |
| TPS62161DSGT     | ACTIVE        | WSON         | DSG             | 8    | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | QUB                     | <a href="#">Samples</a> |
| TPS62162DSGR     | ACTIVE        | WSON         | DSG             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | QUC                     | <a href="#">Samples</a> |
| TPS62162DSGT     | ACTIVE        | WSON         | DSG             | 8    | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | QUC                     | <a href="#">Samples</a> |
| TPS62163DSGR     | ACTIVE        | WSON         | DSG             | 8    | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | QUD                     | <a href="#">Samples</a> |
| TPS62163DSGT     | ACTIVE        | WSON         | DSG             | 8    | 250         | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | QUD                     | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TPS62160, TPS62162 :**

- Automotive : [TPS62160-Q1](#), [TPS62162-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS62160DGKR | VSSOP        | DGK             | 8    | 2500 | 330.0              | 12.4               | 5.25    | 3.35    | 1.25    | 8.0     | 12.0   | Q1            |
| TPS62160DGKT | VSSOP        | DGK             | 8    | 250  | 330.0              | 12.4               | 5.25    | 3.35    | 1.25    | 8.0     | 12.0   | Q1            |
| TPS62160DSGR | WSO          | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS62160DSGT | WSO          | DSG             | 8    | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS62160DSGT | WSO          | DSG             | 8    | 250  | 178.0              | 8.4                | 2.25    | 2.25    | 1.0     | 4.0     | 8.0    | Q2            |
| TPS62161DSGR | WSO          | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS62161DSGT | WSO          | DSG             | 8    | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS62162DSGR | WSO          | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS62162DSGT | WSO          | DSG             | 8    | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS62163DSGR | WSO          | DSG             | 8    | 3000 | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |
| TPS62163DSGT | WSO          | DSG             | 8    | 250  | 180.0              | 8.4                | 2.3     | 2.3     | 1.15    | 4.0     | 8.0    | Q2            |



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS62160DGKR | VSSOP        | DGK             | 8    | 2500 | 366.0       | 364.0      | 50.0        |
| TPS62160DGKT | VSSOP        | DGK             | 8    | 250  | 366.0       | 364.0      | 50.0        |
| TPS62160DSGR | WSON         | DSG             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| TPS62160DSGT | WSON         | DSG             | 8    | 250  | 210.0       | 185.0      | 35.0        |
| TPS62160DSGT | WSON         | DSG             | 8    | 250  | 205.0       | 200.0      | 33.0        |
| TPS62161DSGR | WSON         | DSG             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| TPS62161DSGT | WSON         | DSG             | 8    | 250  | 210.0       | 185.0      | 35.0        |
| TPS62162DSGR | WSON         | DSG             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| TPS62162DSGT | WSON         | DSG             | 8    | 250  | 210.0       | 185.0      | 35.0        |
| TPS62163DSGR | WSON         | DSG             | 8    | 3000 | 210.0       | 185.0      | 35.0        |
| TPS62163DSGT | WSON         | DSG             | 8    | 250  | 210.0       | 185.0      | 35.0        |

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**DSG 8**

**WSON - 0.8 mm max height**

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224783/A

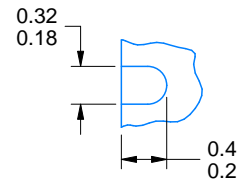
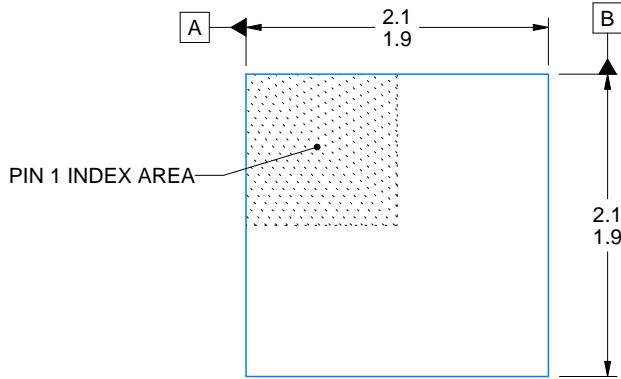
# DSG0008A



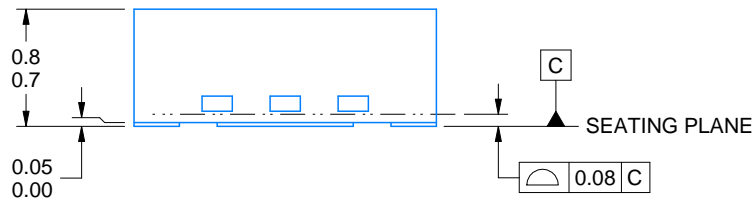
# PACKAGE OUTLINE

## WSON - 0.8 mm max height

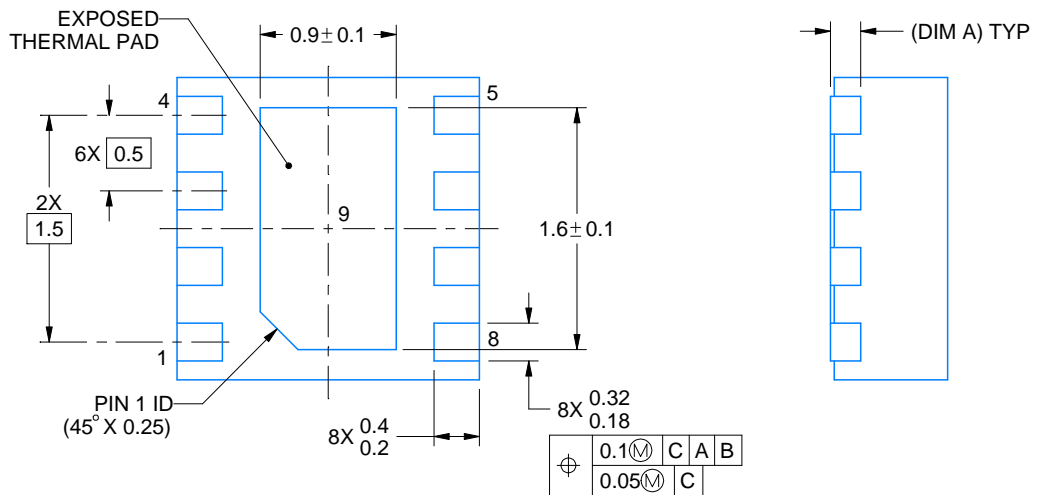
PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE  
TYPICAL



| SIDE WALL METAL THICKNESS DIM A |          |
|---------------------------------|----------|
| OPTION 1                        | OPTION 2 |
| 0.1                             | 0.2      |



4218900/E 08/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



## 重要なお知らせと免責事項

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