TEXAS INSTRUMENTS
TPS62090, TPS62091, TPS62092, TPS62093
JAJSBN1C – MARCH 2012 – REVISED OCTOBER 2016

TPS6209x 3A、高効率、同期整流降圧型コンバータ、 DCS-Control™

1 特長

- 入力電圧範囲: 2.5V～6V
- DCS-Control™
- 95%のコンバータ効率
- パワーセービング・モード
- 動作時の静止電流20µA
- 100%デューティ·サイクル動作により低いドロップアウト電圧を実現
- 標準スイッチング周波数2.8MHz/1.4MHz
- 出力電圧は0.8V～V_{IN}まで可変
- 固定出力電圧バージョン
- 出力放電機能
- 調整可能なソフト・スタート
- ヒカップ短絡保護
- 出力電圧トラッキング
- TPS62095とピン単位で互換

2 アプリケーション

- 分散型電源
- ノートPC、ネットブック
- ハードディスク・ドライブ(HDD)
- ソリッド・ステート・ドライブ(SSD)
- プロセッサの電源
- バッテリ駆動のアプリケーション

3 概要

TPS6209xデバイスは高周波数の同期整流降圧型コンバータで、サイズが小さく、高効率で、バッテリ駆動のアプリケーションに適したソリューションとなるよう最適化されています。最大の効率を実現するため、このコンバータはパルス幅変調(PWM)モードで動作します。公称スイッチング周波数は2.8MHz/1.4MHzで、負荷電流が小さいときには自動的にパワーセービング・モードの動作に移行します。分散型電源およびポイント・オブ・ロード・レギュレーションで使用するとき、他の電圧レールへの電圧トラッキングが可能で、10µFから150µFまで、さらにそれ以上の出力容量を許容できます。このデバイスは、DCS-Control™トポロジを使用して非常に優れた負荷過渡性能と、出力電圧の正確なレギュレーションを実現しています。

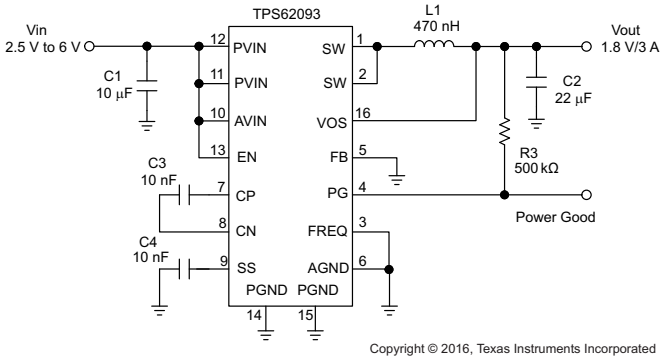
出力電圧のスタートアップ・ランプはソフトスタート・ピンにより制御されるため、スタンドアロンの電源またはトラッキング構成で動作できます。イネーブル・ピンおよびパワー・グッド・ピンの構成により、電源シーケンシングも可能です。パワーセービング・モードでは、デバイスは標準20µAの静止電流で動作します。パワーセービング・モードへの遷移は自動的かつシームレスに行われるため、負荷電流範囲の全体にわたって高い効率が維持されます。

製品情報(1)

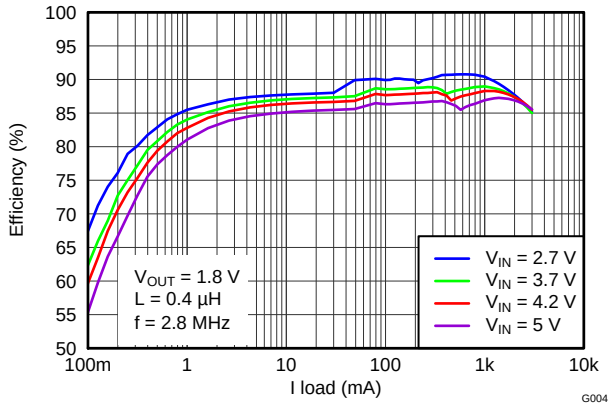
型番	パッケージ	本体サイズ(公称)
TPS62090	QFN (16)	3.00mm×3.00mm
TPS62091		
TPS62092		
TPS62093		

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



効率と出力電流との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (April 2014) から **Revision C** に変更 **Page**

- 「特長」で「出力容量を広範に選択可能」の箇条書きを削除、箇条書きテキストの「2レベルの…」を「ヒカップ…」へ 変更 ... 1
- Added CN and CP pin absolute maximum ratings ... 4
- Moved Storage Temp spec to the "Absolute Maximum Ratings" table ... 4
- Added Feedback voltage accuracy at T_J = 25°C ... 5
- 変更 Legend in 図 2 and 図 4 to show correct voltages ... 6
- Updated Voltage Tracking (SS) section ... 9
- 追加 Charge Pump (CP, CN) section ... 11
- Updated PCB layout example ... 19
- 追加 「コミュニティ・リソース」セクション ... 20

Revision A (March 2012) から **Revision B** に変更 **Page**

- 新しいTI標準フォーマットに合わせてデータシートを変更 ... 1
- Changed the Typical Characteristics. Moved graphs to the Application and Implementation section ... 6
- Added the Layout section ... 19

2012年3月 発行のものから更新 **Page**

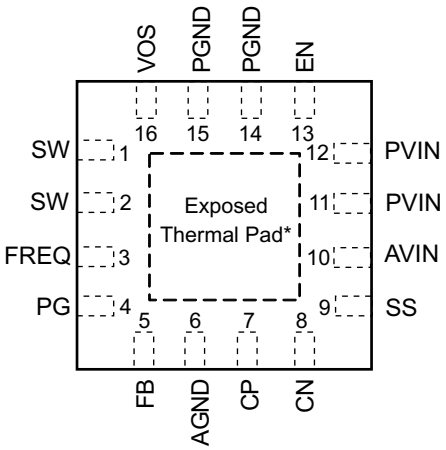
- Changed the FUNCTIONAL BLOCK DIAGRAM ... 8
- Changed R1 and R2 values in 図 9 ... 13

5 Device Comparison Table

DEVICE NUMBER	OUTPUT VOLTAGE
TPS62090RGT	Adjustable
TPS62091RGT	3.3 V
TPS62092RGT	2.5 V
TPS62093RGT	1.8 V

6 Pin Configuration and Functions

RGT Package
16-Pin QFN
Top View



NOTE: *The exposed thermal pad is connected to AGND.

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1, 2	SW	I/O	Switch pin of the power stage.
3	FREQ	I	This pin selects the switching frequency of the device. FREQ = Low sets the typical switching frequency to 2.8 MHz. FREQ = High sets the typical switching frequency to 1.4 MHz. This pin has an active pull down resistor of typically 400 kΩ and can be left floating for 2.8 MHz operation.
4	PG	O	Power good open drain output. This pin is high impedance if the output voltage is within regulation. This pin is pulled low if the output is below its nominal value. The pull up resistor can not be connected to any voltage higher than the input voltage of the device.
5	FB	I	Feedback pin of the device. For the adjustable version, connect a resistor divider to set the output voltage. For the fixed output voltage versions this pin may be connected to GND for improved thermal performance and has a pull down resistor of typically 400 kΩ, which is active when EN is low.
6	AGND		Analog ground.
7	CP	I/O	Internal charge pump flying capacitor. Connect a 10 nF capacitor between CP and CN.
8	CN	I/O	Internal charge pump flying capacitor. Connect a 10 nF capacitor between CP and CN.
9	SS	I	Softstart control pin. A capacitor is connected to this pin and sets the softstart time. Leaving this pin floating sets the minimum start-up time.
10	AVIN	I	Bias supply input voltage pin.
11,12	PVIN	I	Power supply input voltage pin.
13	EN	I	Device enable. To enable the device this pin needs to be pulled high. Pulling this pin low disables the device. This pin has a pull down resistor of typically 400 kΩ, which is active when EN is low.
14,15	PGND		Power ground connection.
16	VOS	I	Output voltage sense pin. This pin needs to be connected to the output voltage.
Exposed Thermal Pad		–	The exposed thermal pad is connected to AGND. It must be soldered for mechanical reliability.

7 Specifications

7.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage range(2)	PVIN, AVIN, FB, SS, EN, FREQ, VOS	–0.3	7	V
	SW, PG	–0.3	V_{IN} + 0.3	
	CN, CP	-0.3	V_{IN} + 7.0	
Power Good sink current	PG		1	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM) per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions(1)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range V_{IN}	2.5		6	V
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) See the application section for further information

7.4 Thermal Information

THERMAL METRIC(1)		TPS6209x	UNIT
		QFN (16 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	47	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	60	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	20	°C/W
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	5.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

7.5 Electrical Characteristics

V_{IN} = 3.6 V, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.5		6	V
I_{QIN}	Quiescent current	Not switching, FB = FB +5%, into PVIN and AVIN		20		µA
I_{sd}	Shutdown current	Into PVIN and AVIN		0.6	5	µA
UVLO	Undervoltage lockout threshold	V_{IN} falling	2.1	2.2	2.3	V
	Undervoltage lockout hysteresis			200		mV
	Thermal shutdown	Temperature rising		150		ºC
	Thermal shutdown hysteresis			20		ºC
Control SIGNALS EN, FREQ						
V_H	High level input voltage	V_{IN} = 2.5 V to 6 V	1	0.65		V
V_L	Low level input voltage	V_{IN} = 2.5 V to 6 V		0.6	0.4	V
I_{lkg}	Input leakage current	EN, FREQ = GND or V_{IN}		10	100	nA
R_{PD}	Pull down resistance			400		kΩ
Softstart						
I_{SS}	Softstart current		6.3	7.5	8.7	µA
POWER GOOD						
V_{th}	Power good threshold	Output voltage rising	93%	95%	97%	
		Output voltage falling	88%	90%	92%	
V_L	Low level voltage	$I_{(sink)}$ = 1 mA			0.4	V
I_{PG}	PG sinking current				1	mA
I_{lkg}	Leakage current	V_{PG} = 3.6 V		10	100	nA
POWER SWITCH						
$R_{DS(on)}$	High side FET on-resistance	I_{SW} = 500 mA		50		mΩ
	Low side FET on-resistance	I_{SW} = 500 mA		40		mΩ
I_{LIM}	High side FET switch current limit		3.7	4.6	5.5	A
f_s	Switching frequency	FREQ = GND, I_{OUT} = 3 A		2.8		MHz
		FREQ = VIN, I_{OUT} = 3 A		1.4		MHz
OUTPUT						
V_s	Output voltage range		0.8		V_{IN}	V
R_{od}	Output discharge resistor	EN = GND, V_{OUT} = 1.8 V		200		Ω
V_{FB}	Feedback regulation voltage			0.8		V
V_{FB}	Feedback voltage accuracy (1) (2)(3)	V_{IN} ≥ V_{OUT} + 1 V, TPS62090 adjustable output version				
		I_{OUT} = 1 A, PWM mode, T_J = 25°C	-1%		+1%	
		I_{OUT} = 1 A, PWM mode	-1.4%		+1.4%	
		I_{OUT} = 0 mA, FREQ = 2.8 MHz, V_{OUT} ≥ 0.8 V, PFM mode	-1.4%		+3%	
		I_{OUT} = 0 mA, FREQ = 1.4 MHz, V_{OUT} ≥ 1.2 V, PFM mode	-1.4%		+3%	
		I_{OUT} = 0 mA, FREQ = 1.4 MHz, V_{OUT} < 1.2V, PFM mode	-1.4%		+3.7%	
I_{FB}	Feedback input bias current	V_{FB} = 0.8 V, TPS62090 adjustable output version		10	100	nA
V_{OUT}	Output voltage accuracy (2)(3)	V_{IN} ≥ V_{OUT} + 1 V, fixed output voltage				
		I_{OUT} = 1 A, PWM mode	-1.4%		+1.4%	
		I_{OUT} = 0 mA, FREQ = High and Low, PFM mode	-1.4%		+2.5%	
	Line regulation	V_{OUT} = 1.8 V, PWM operation		0.016		%/V
	Load regulation	V_{OUT} = 1.8 V, PWM operation		0.04		%/A

(1) For output voltages < 1.2 V, use a 2 x 22 µF output capacitance to achieve +3% output voltage accuracy.
(2) Conditions: f = 2.8 MHz, L = 0.47 µH, C_{OUT} = 22 µF or f = 1.4 MHz, L = 1 µH, C_{OUT} = 22 µF.
(3) For more information, see the *Power Save Mode Operation* section of this data sheet.

7.6 Typical Characteristics

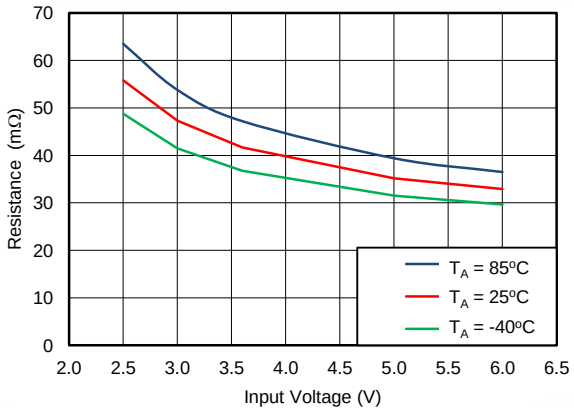


図 1. High Side FET On-Resistance vs Input Voltage

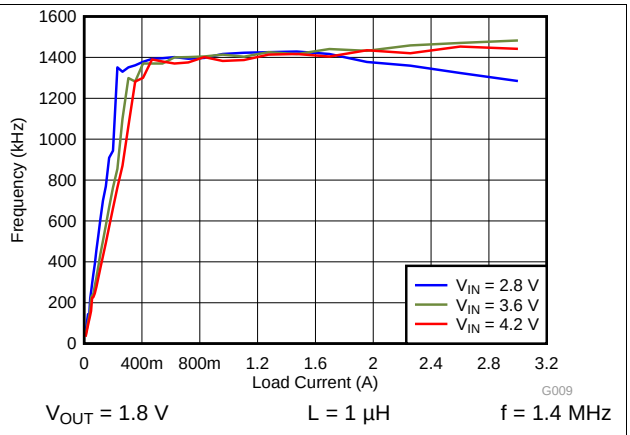


図 2. Switching Frequency vs Load Current

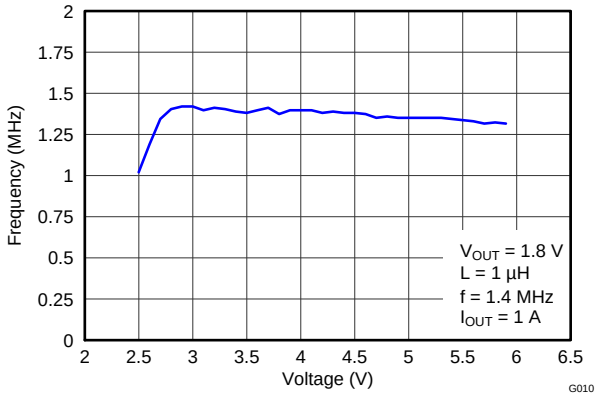


図 3. Switching Frequency vs Input Voltage

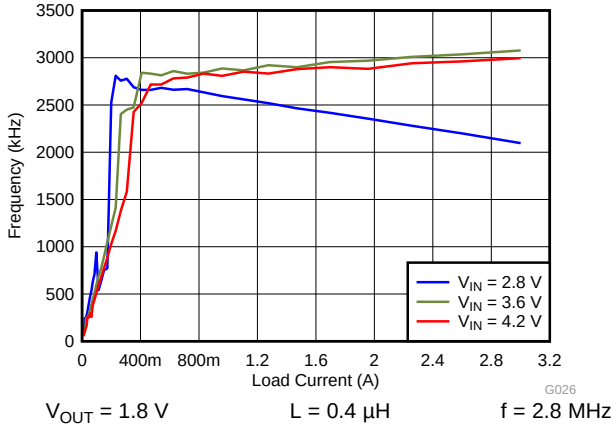


図 4. Frequency vs Load Current

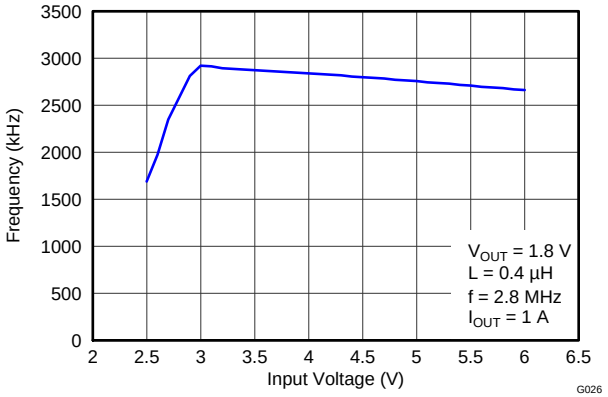


図 5. Frequency vs Input Voltage

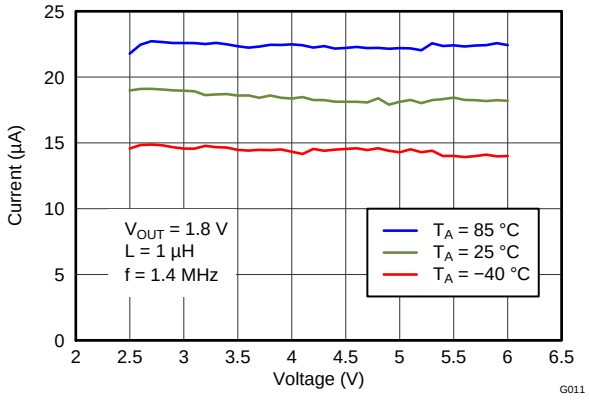


図 6. Quiescent Current vs Input Voltage

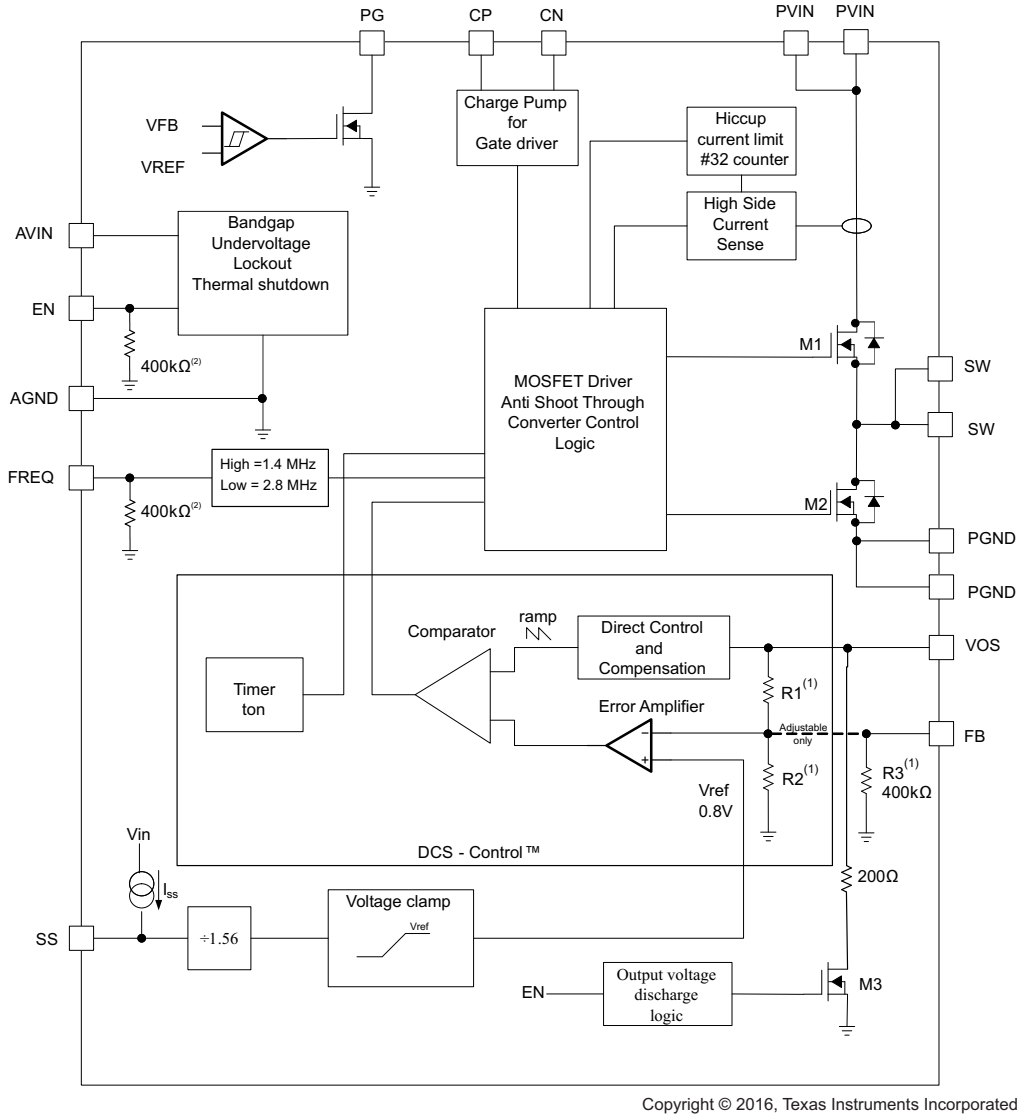
8 Detailed Description

8.1 Overview

The TPS6209x synchronous switched mode converters are based on DCS-Control™ (direct control with seamless transition into power save mode). This is an advanced regulation topology that combines the advantages of hysteretic and voltage mode control.

The DCS-Control™ topology operates in pulse width modulation (PWM) mode for medium to heavy load conditions and in power save mode at light load currents. In PWM, the converter operates with its nominal switching frequency of 2.8 MHz/1.4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters power save mode, reducing the switching frequency and minimizing the IC quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes (PWM and PFM) using a single building block having a seamless transition from PWM to power save mode without effects on the output voltage. Fixed output voltage versions provide smallest solution size combined with lowest quiescent current. The TPS6209x family offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

8.2 Functional Block Diagram



(1) R1, R2, R3 are implemented in the fixed output voltage version only.

(2) The resistors are disconnected when the pins are high.

8.3 Feature Description

8.3.1 Enable and Disable (EN)

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low with a shutdown current of typically 0.6 μA. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal resistor of 200 Ω discharges the output through the VOS pin smoothly. An internal pull-down resistor of 400 kΩ is connected to the EN pin when the EN pin is low. The pulldown resistor is disconnected when the EN pin is high.

Feature Description (continued)

8.3.2 Softstart (SS) and Hiccup Current Limit During Startup

To minimize inrush current during start up, the device has an adjustable softstart depending on the capacitor value connected to the SS pin. The device charges the softstart capacitor with a constant current of typically 7.5 µA. The feedback voltage follows this voltage with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The softstart operation is completed once the voltage at the softstart capacitor has reached typically 1.25 V. The soft-start time can be calculated using 式 1. The larger the softstart capacitor the longer the softstart time. The relation between softstart voltage and feedback voltage can be estimated using 式 2.

$$t_{SS} = C_{SS} \times \frac{1.25V}{7.5\mu A} \quad (1)$$

$$V_{FB} = \frac{V_{SS}}{1.56} \quad (2)$$

During startup, the switch current limit is reduced to 1/3 (~1.5 A) of its typical current limit of 4.6 A. Once the output voltage exceeds typically 0.6 V, the current limit is released to its nominal value. The device provides a reduced load current of ~1.5 A when the output voltage is below typically 0.6 V. Due to this, a small or no softstart time may trigger the short circuit protection during startup especially for larger output capacitors. This is avoided by using a larger softstart capacitance to extend the softstart time. See *Short Circuit Protection (Hiccup-Mode)* for details of the reduced current limit during startup. Leaving the softstart pin floating sets the minimum start-up time (around 50µs).

8.3.3 Voltage Tracking (SS)

The SS pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in 図 7. The internal reference voltage follows the voltage at the SS pin with a fraction of 1.56 until the internal reference voltage of 0.8 V is reached. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in 図 8.

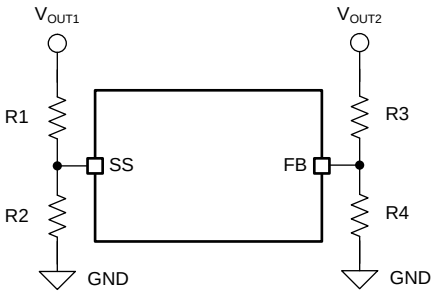


図 7. Output Voltage Tracking

Feature Description (continued)

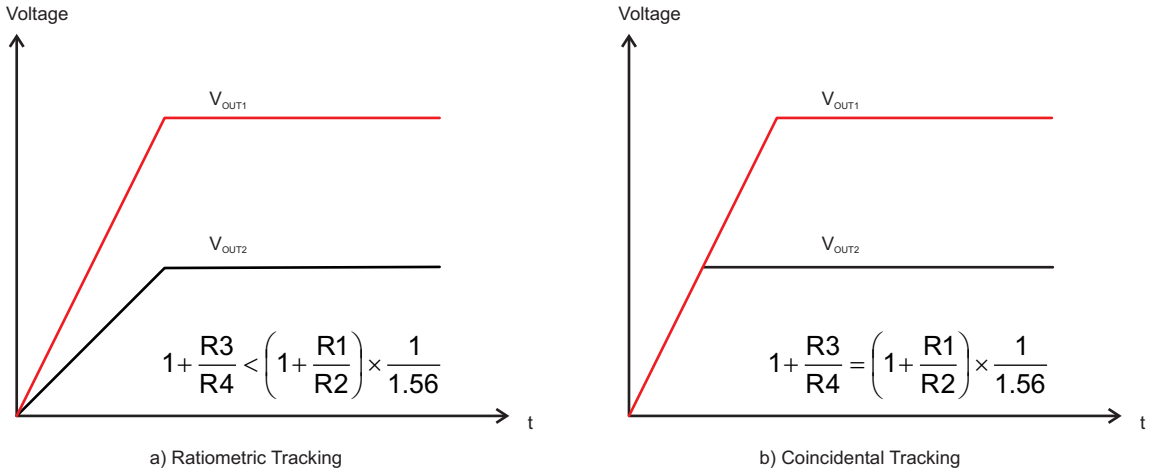


図 8. Voltage Tracking Options

The R2 value should be set properly to achieve accurate voltage tracking by taking 7.5 μA soft startup current into account. 1 kΩ or smaller is a sufficient value for R2.

For decreasing the SS pin voltage, the device doesn't sink current from the output when the device is in power save mode. So the resulting decreases of the output voltage may be slower than the SS pin voltage if the load is light. When driving the SS pin with an external voltage, do not exceed the voltage rating of the SS pin which is 7 V.

8.3.4 Short Circuit Protection (Hiccup-Mode)

The device is protected against hard short circuits to GND and over-current events. This is implemented by a two level short circuit protection. During start-up and when the output is shorted to GND the switch current limit is reduced to 1/3 of its typical current limit of 4.6 A. Once the output voltage exceeds typically 0.6 V the current limit is released to its nominal value. The full current limit is implemented as a hiccup current limit. Once the internal current limit is triggered 32 times the device stops switching and starts a new start-up sequence after a typical delay time of 66 μs passed by. The device will go through these cycles until the high current condition is released.

8.3.5 Output Discharge Function

To make sure the device starts up under defined conditions, the output gets discharged via the VOS pin with a typical discharge resistor of 200 Ω whenever the device shuts down. This happens when the device is disabled or if thermal shutdown, undervoltage lockout or short circuit hiccup-mode is triggered.

8.3.6 Power Good Output (PG)

The power good output is low when the output voltage is below its nominal value. The power good becomes high impedance once the output is within 5% of regulation. The PG pin is an open drain output and is specified to typically sink up to 1 mA. This output requires a pull-up resistor to be monitored properly. The pull-up resistor cannot be connected to any voltage higher than the input voltage of the device. The PG output is low when the device is disabled, in thermal shutdown or UVLO. The PG output can be left floating if unused.

Feature Description (continued)

8.3.7 Frequency Set Pin (FREQ)

The FREQ pin is a digital logic input which sets the nominal switching frequency. Pulling this pin to GND sets the nominal switching frequency to 2.8 MHz and pulling this pin high sets the nominal switching frequency to 1.4 MHz. Since this pin changes the switching frequency it also changes the on-time during pulse frequency modulation (PFM) mode. At 1.4 MHz the on-time is twice the on-time as operating at 2.8 MHz. This pin has an active pull-down resistor of typically 400 kΩ. For applications where efficiency is of highest importance, a lower switching frequency should be selected. A higher switching frequency allows the use of smaller external components, faster load transient response and lower output voltage ripple when using same L-C values.

8.3.8 Undervoltage Lockout (UVLO)

To avoid mis-operation of the device at low input voltages, an undervoltage lockout is included. UVLO shuts down the device at input voltages lower than typically 2.2 V with a 200 mV hysteresis.

8.3.9 Thermal Shutdown

The device goes into thermal shutdown once the junction temperature exceeds typically 150°C with a 20°C hysteresis.

8.3.10 Charge Pump (CP, CN)

The CP and CN pins must attach to an external 10 nF capacitor to complete a charge pump for the gate driver. This capacitor must be rated for the input voltage. It is not recommended to connect any other circuits to the CP or CN pins.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation Operation

At medium to heavy load currents, the device operates with pulse width modulation (PWM) at a nominal switching frequency of 2.8 MHz or 1.4 MHz depending on the setting of the FREQ pin. As the load current decreases, the converter enters the power save mode operation reducing its switching frequency. The device enters power save mode at the boundary to discontinuous conduction mode (DCM).

8.4.2 Power Save Mode Operation

As the load current decreases, the converter enters power save mode operation. During power save mode, the converter operates with reduced switching frequency maintaining high efficiency. The power save mode is based on a fixed on-time architecture following 式 3. When operating at 1.4 MHz the on-time is twice as long as the on-time for 2.8 MHz operation. This results in larger output voltage ripple, as shown in 図 19 and 図 20, and slightly higher output voltage at no load, as shown in 図 16 and 図 17. To have the same output voltage ripple at 1.4 MHz during PFM mode, either the output capacitor or the inductor value needs to be increased. As an example, operating at 2.8 MHz using 0.47 µH inductor gives the same output voltage ripple as operating with 1.4 MHz using 1 µH inductor.

$$ton_{2.8MHz} = \frac{V_{OUT}}{V_{IN}} \times 360ns$$

$$ton_{1.4MHz} = \frac{V_{OUT}}{V_{IN}} \times 360ns \times 2$$

$$f = \frac{2 \times I_{OUT}}{ton^2 \left(1 + \frac{V_{IN} - V_{OUT}}{V_{OUT}}\right) \times \frac{V_{IN} - V_{OUT}}{L}} \quad (3)$$

In power save mode the output voltage rises slightly above the nominal output voltage in PWM mode, as shown in 図 16 and 図 17. This effect can be reduced by increasing the output capacitance or the inductor value. This effect can also be reduced by programming the output voltage of the TPS62090 lower than the target value. As an example, if the target output voltage is 3.3 V, then the TPS62090 can be programmed to 3.3 V – 0.8%. As a result the output voltage accuracy is now -2.2% to +2.2% instead of -1.4% to 3%. The output voltage accuracy in PFM operation is reflected in the electrical specification table and given for a 22 µF output capacitor.

Device Functional Modes (continued)

8.4.3 Low Dropout Operation (100% Duty Cycle)

The device offers low input to output voltage difference by entering 100% duty cycle mode. In this mode the high side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage where the output voltage falls below its nominal regulation value is given by:

$$V_{IN(min)} = V_{OUT} + I_{OUT} \times (R_{DS(on)} + R_L) \quad (4)$$

Where:

$R_{DS(on)}$ = High side FET on-resistance

R_L = DC resistance of the inductor

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6209x 3 A family of devices, are high frequency synchronous step down converters optimized for small solution size, high efficiency and suitable for battery powered applications.

9.2 Typical Applications

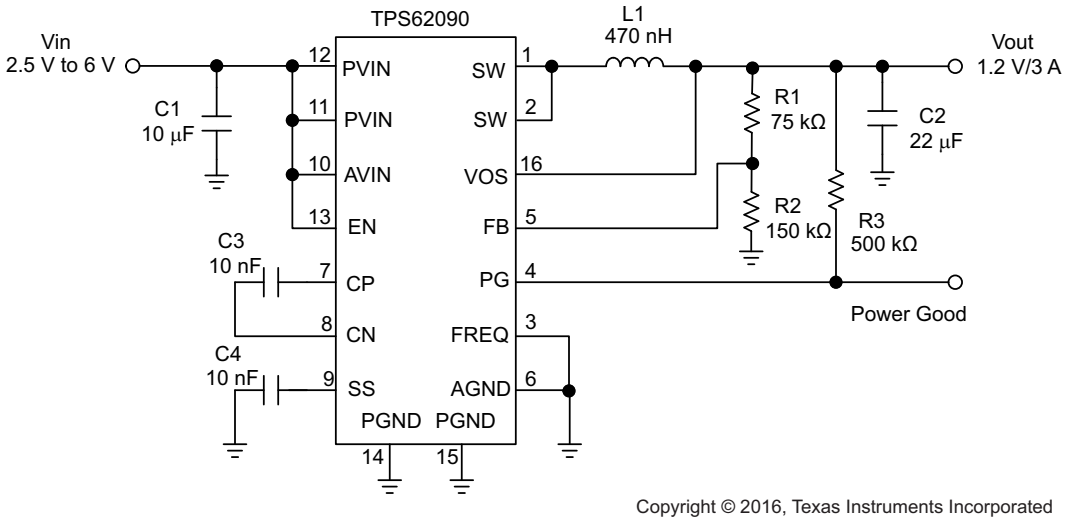


図 9. 1.2 V Adjustable Version Operating at 2.8 MHz

9.2.1 Design Requirements

The design guideline provides a component selection to operate the device within the recommended operating conditions.

The design can be optimized for highest efficiency or smallest solution size and lowest output voltage ripple. For highest efficiency set the device switching frequency to 1.4 MHz (FREQ = High) and select the output filter components according to 表 3. For smallest solution size and lowest output voltage ripple set the device switching frequency to 2.8 MHz (FREQ = Low) and select the output filter components according to 表 2. For the fixed output voltage option the feedback pin needs to be connected to GND.

表 1 shows the list of components for the *Application Curves*.

表 1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
TPS62090	High efficiency step down converter	Texas Instruments
L1	Inductor: 1uH, 0.47uH, 0.4uH	Coilcraft XFL4020-102, TOKO DEF252012C-R47, Coilcraft XAL4020-401
C1	Ceramic capacitor: 10uF, 22uF	(6.3V, X5R, 0603), (6.3V, X5R, 0805)
C2	Ceramic capacitor: 22uF	(6.3V, X5R, 0805)
C3, C4	Ceramic capacitor	Standard
R1, R2, R3	Resistor	Standard

9.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, 表 2 and 表 3 outline possible inductor and capacitor value combinations. Checked cells represent combinations that are proven for stability by simulation and lab. Further combinations should be checked for each individual application.

表 2. Output Filter Selection (2.8 MHz Operation, FREQ = GND)

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	47	100	150
0.47		√(3)	√	√	√
1.0	√	√	√	√	√
2.2					
3.3					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and -30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and -50%.
(3) Typical application configuration. Other check mark indicates alternative filter combinations

表 3. Output Filter Selection (1.4 MHz Operation, FREQ = V_{IN})

INDUCTOR VALUE [µH](1)	OUTPUT CAPACITOR VALUE [µF](2)				
	10	22	47	100	150
0.47		√	√	√	√
1.0	√	√(3)	√	√	√
2.2	√	√	√	√	√
3.3					

(1) Inductor tolerance and current de-rating is anticipated. The effective inductance can vary by +20% and –30%.
(2) Capacitance tolerance and bias voltage de-rating is anticipated. The effective capacitance can vary by +20% and –50%.
(3) Typical application configuration. Other check mark indicates alternative filter combinations

9.2.2.1 Inductor Selection

The inductor selection is affected by several parameter like inductor ripple current, output voltage ripple, transition point into power save mode, and efficiency. See 表 4 for typical inductors.

表 4. Inductor Selection

INDUCTOR VALUE	COMPONENT SUPPLIER(1)	SIZE (LxWxH mm)	Isat/DCR
0.6 µH	Coilcraft XAL4012-601	4 x 4 x 2.1	7.1 A/9.5 mΩ
1 µH	Coilcraft XAL4020-102	4 x 4 x 2.1	5.9 A/13.2 mΩ
1 µH	Coilcraft XFL4020-102	4 x 4 x 2.1	5.1 A/10.8 mΩ
0.47 µH	TOKO DFE252012 R47	2.5 x 2 x 1.2	3.7 A/39 mΩ
1 µH	TOKO DFE252012 1R0	2.5 x 2 x 1.2	3.0 A/59 mΩ
0.68 µH	TOKO DFE322512 R68	3.2 x 2.5 x 1.2	3.5 A/37 mΩ
1 µH	TOKO DFE322512 1R0	3.2 x 2.5 x 1.2	3.1 A/45 mΩ

(1) See *Third-Party Products Disclaimer*

In addition, the inductor has to be rated for the appropriate saturation current and DC resistance (DCR). 式 6 calculates the maximum inductor current under static load conditions. The formula takes the converter efficiency into account. The converter efficiency can be taken from the data sheet graph`s or 80% can be used as a conservative approach. The calculation must be done for the maximum input voltage where the peak switch current is highest.

$$\Delta I_L = \frac{\frac{V_{OUT}}{\eta} \times \left(1 - \frac{V_{OUT}}{V_{IN} \times \eta}\right)}{f \times L} \quad (5)$$

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

where:

- f = Converter switching frequency (typical 2.8 MHz or 1.4 MHz)
- L = Selected inductor value
- η = Estimated converter efficiency (use the number from the efficiency curves or 0.80 as an conservative assumption) (6)

Note: The calculation must be done for the maximum input voltage of the application

Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current. A margin of 20% needs to be added to cover for load transients during operation.

9.2.2.2 Input and Output Capacitor Selection

For best output and input voltage filtering, low ESR (X5R or X7R) ceramic capacitors are recommended. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 10-μF or larger input capacitor is recommended when FREQ = Low and a 22-uF or larger when FREQ = High.

The output capacitor value can range from 10 μF up to 150 μF and beyond. Load transient testing and measuring the bode plot are good ways to verify stability with larger capacitor values. The recommended typical output capacitor value is 22 μF (nominal) and can vary over a wide range as outline in the output filter selection table. For output voltages above 1.8 V, noise can cause duty cycle jitter. This does not degrade device performance. Using an output capacitor of 2 x 22 μF (nominal) for output voltages >1.8 V avoids duty cycle jitter.

Ceramic capacitor have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating.

9.2.2.3 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8\ V \times \left(1 + \frac{R1}{R2}\right) \quad (7)$$

$$R2 = \frac{V_{FB}}{I_{FB}} = \frac{0.8\ V}{5\ \mu A} \approx 160\ k\Omega \quad (8)$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (9)$$

When sizing R2, in order to achieve low quiescent current and acceptable noise sensitivity, use a minimum of 5 μA for the feedback current I_{FB}. Larger currents through R2 improve noise sensitivity and output voltage accuracy. Lowest current consumption and best output voltage accuracy can be achieved with the fixed output voltage versions. For the fixed output voltage versions, the FB pin can be left floating or connected to GND to improve the thermal performance. A feed forward capacitor is not required for proper operation.

9.2.2.4 Application Curves

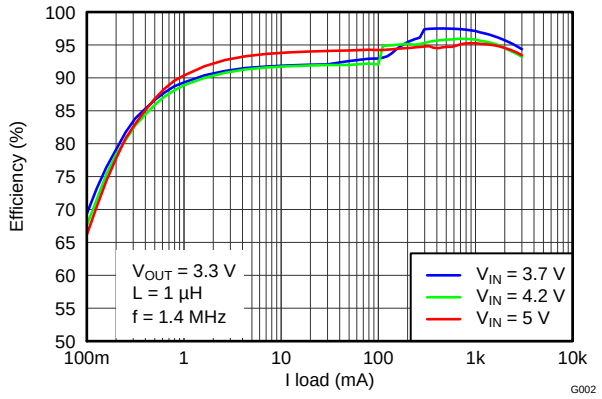


図 10. Efficiency vs Load Current

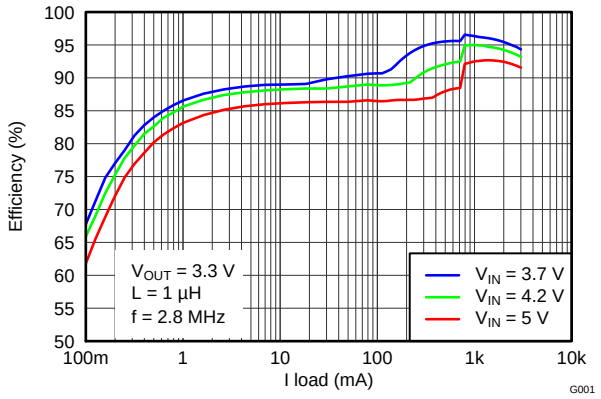


図 11. Efficiency vs Load Current

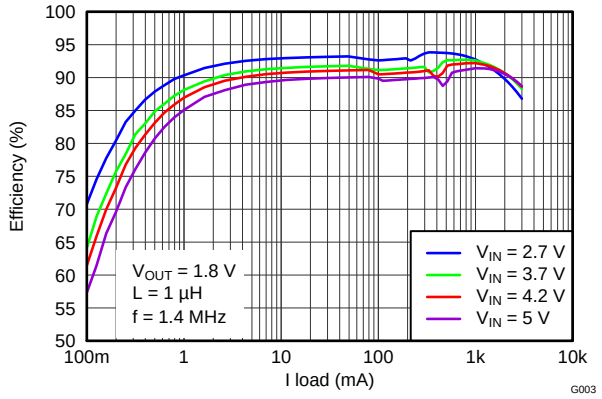


図 12. Efficiency vs Load Current

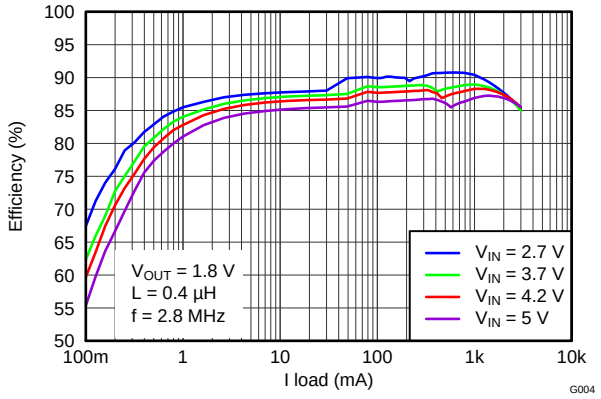


図 13. Efficiency vs Load Current

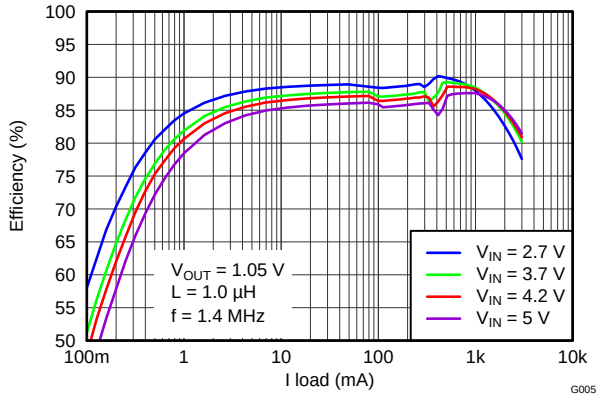


図 14. Efficiency vs Load Current

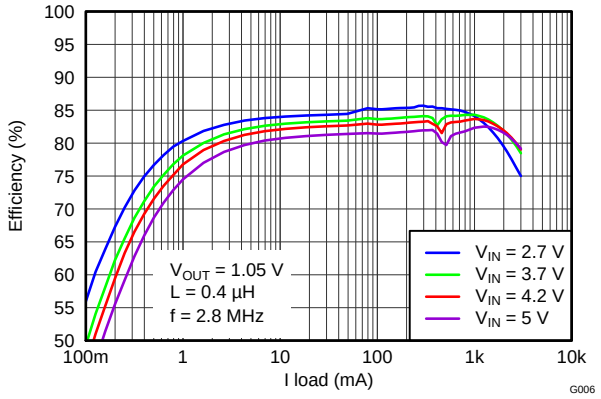


図 15. Efficiency vs Load Current

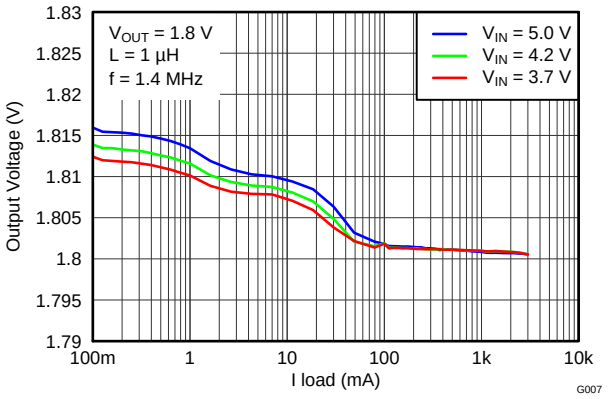


図 16. Output Voltage vs Load Current

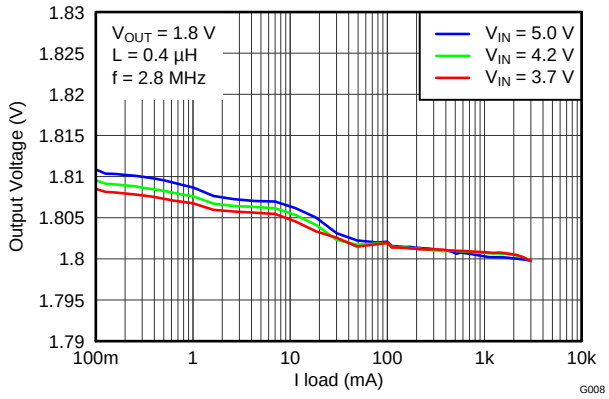


図 17. Output Voltage vs Load Current

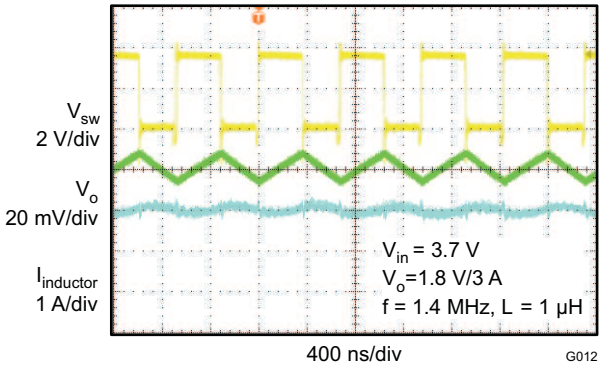


図 18. PWM Operation

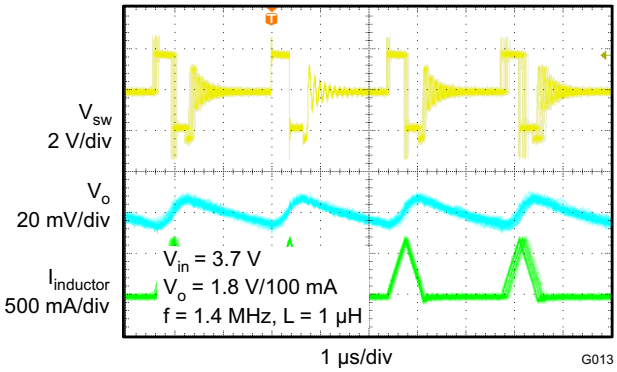


図 19. PFM Operation

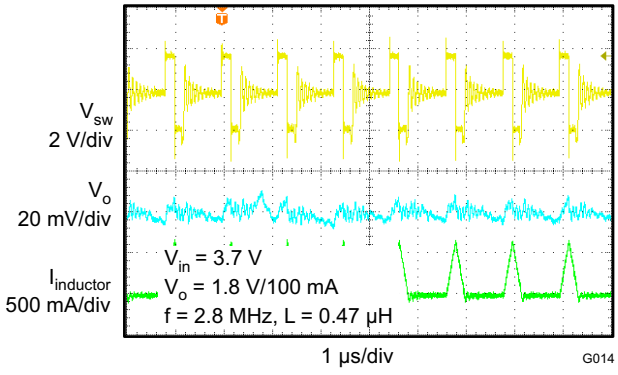


図 20. PFM Operation

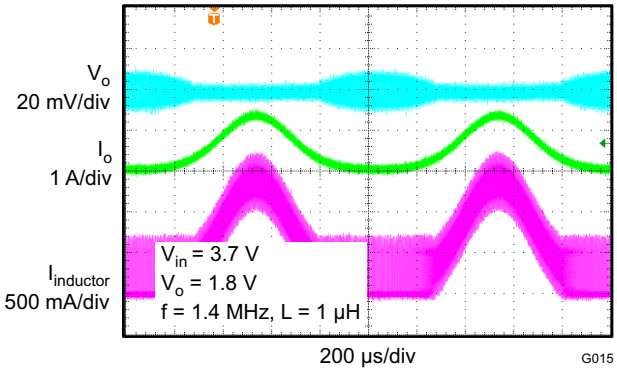


図 21. Load Sweep

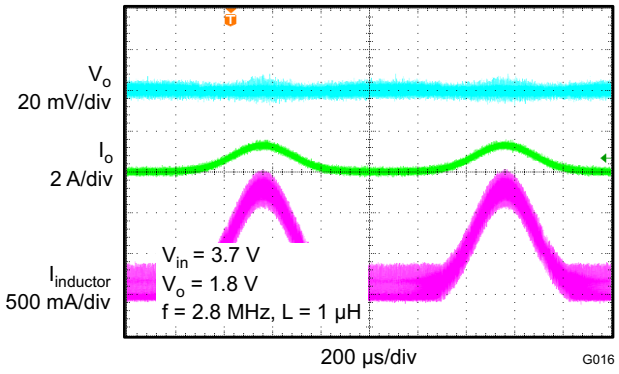


図 22. Load Sweep

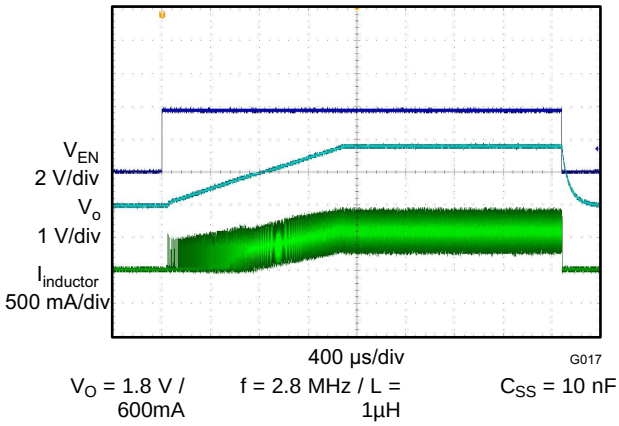


図 23. Start-Up

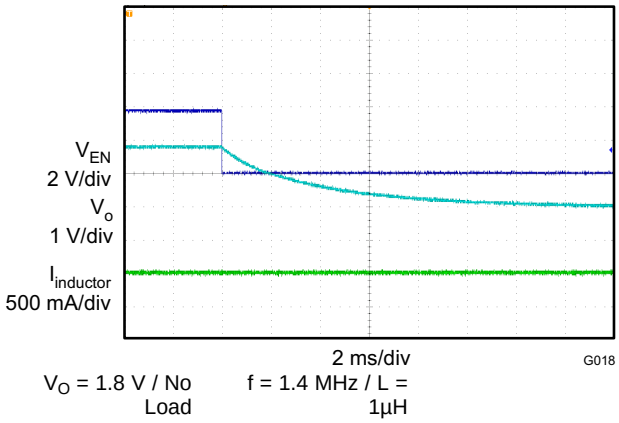


図 24. Shutdown

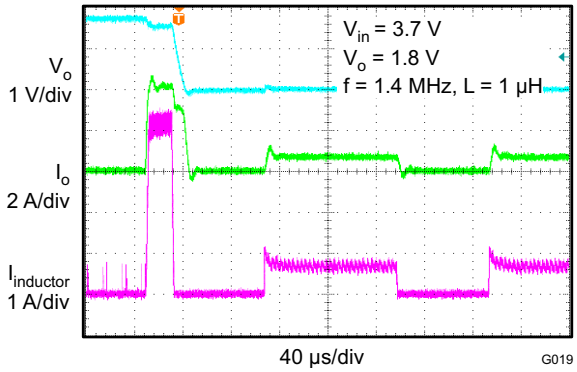


図 25. Hiccup Short Circuit Protection

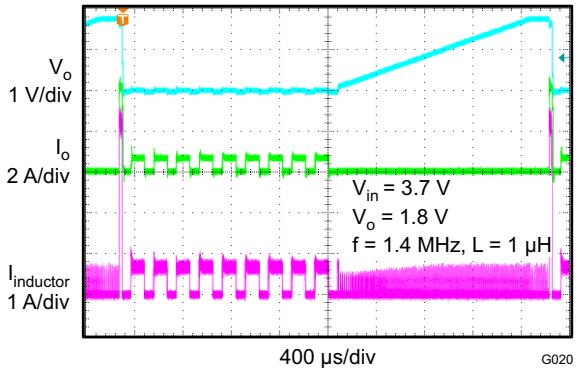


図 26. Hiccup Short Circuit Protection

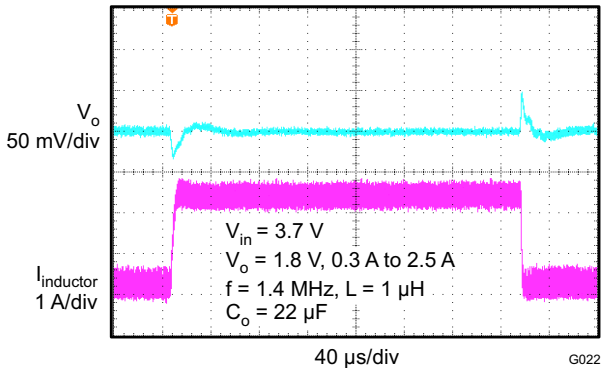


図 27. Load Transient Response

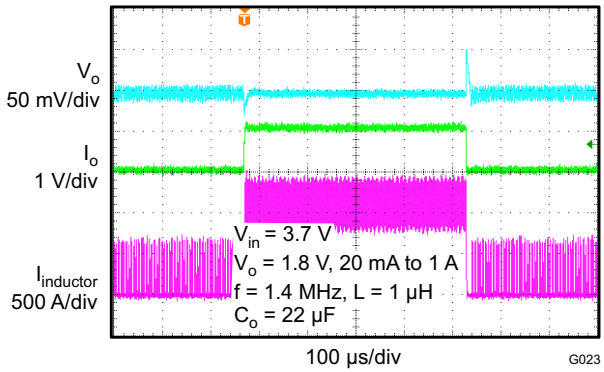


図 28. Load Transient Response

10 Power Supply Recommendations

The power supply to the TPS62090 needs to have a current rating according to the supply voltage, output voltage and output current of the TPS62090.

11 Layout

11.1 Layout Guideline

- It is recommended to place the input capacitor as close as possible to the IC pins PVIN and PGND.
- The VOS connection is noise sensitive and needs to be routed as short and directly to the output pin of the inductor.
- The exposed thermal pad of the package, analog ground (pin 6) and power ground (pin 14, 15) should have a single joint connection at the exposed thermal pad of the package. This minimizes switch node jitter.
- The charge pump capacitor connected to CP and CN should be placed close to the IC to minimize coupling of switching waveforms into other traces and circuits.
- Refer to 図 29 and the evaluation module User Guide (SLVU670) for an example of component placement, routing and thermal design.

11.2 Layout Example

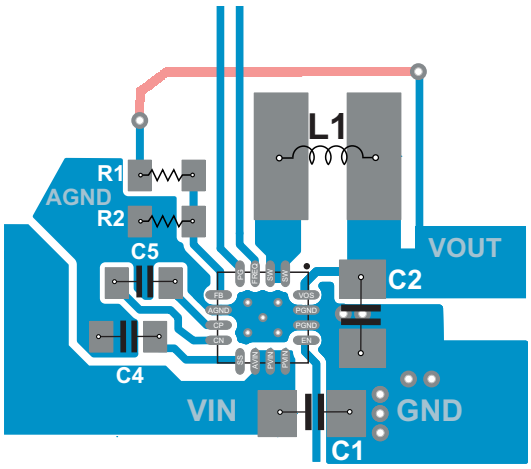


図 29. TPS6209x Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 Third-Party Products Disclaimer

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次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 5. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS62090	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62091	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62092	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS62093	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

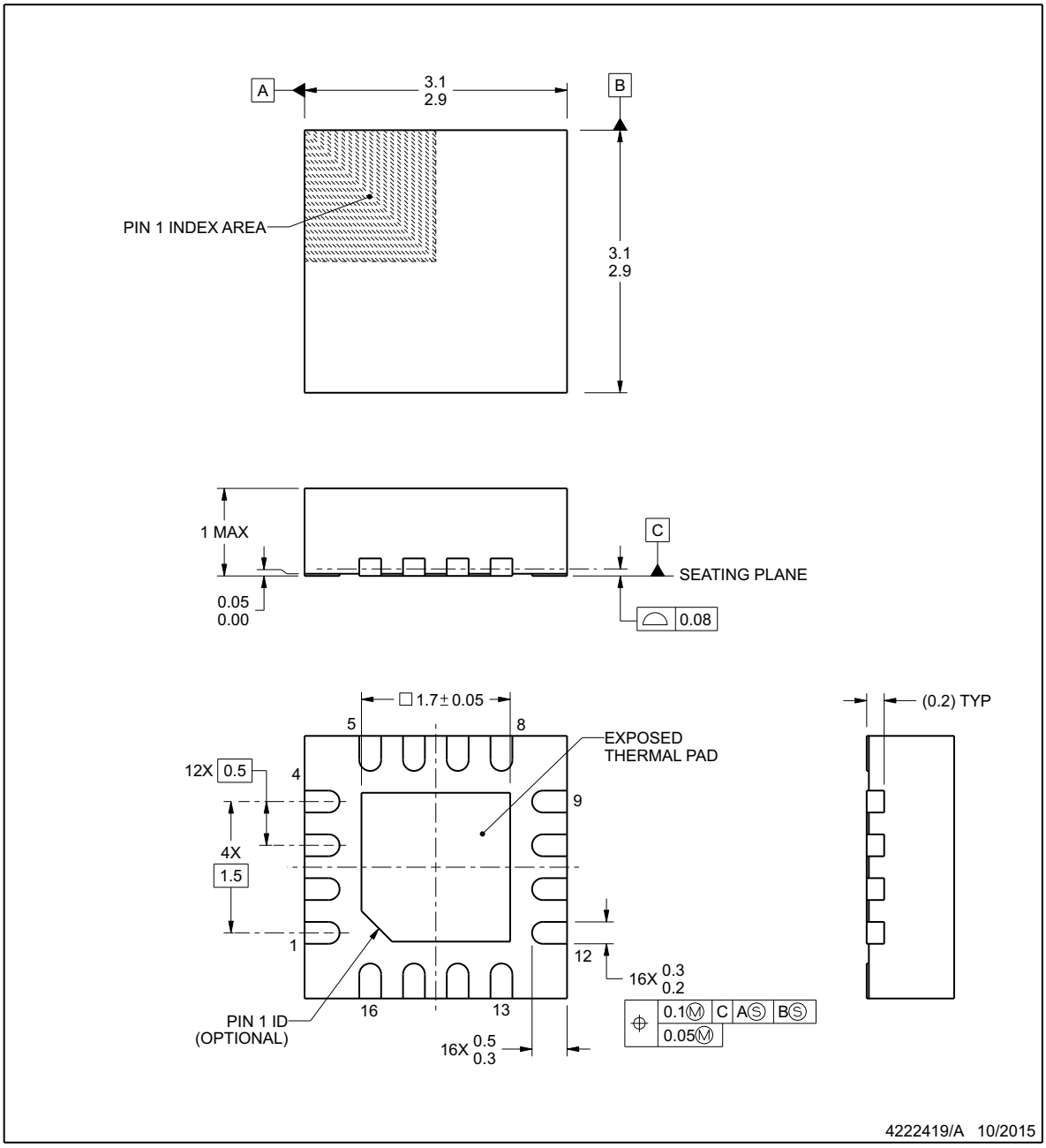
以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGE OUTLINE

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

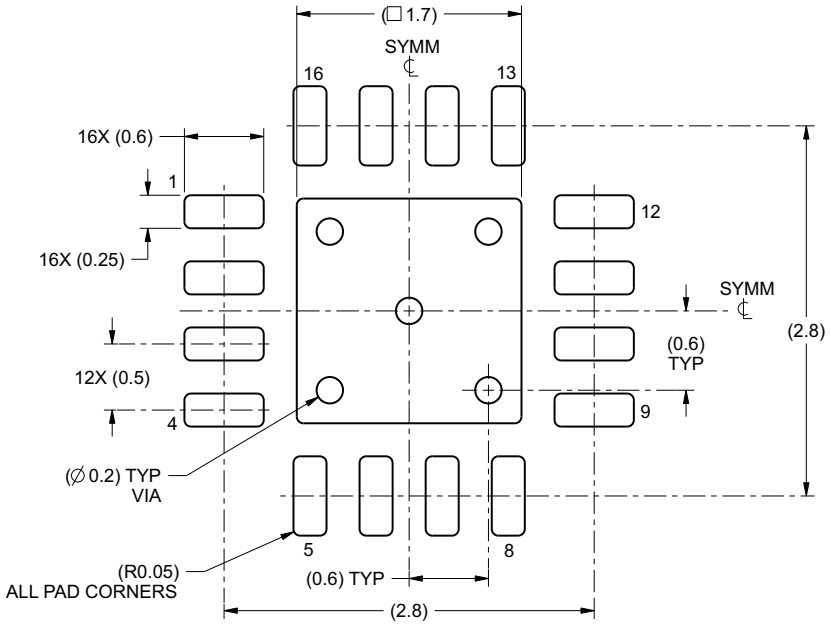
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

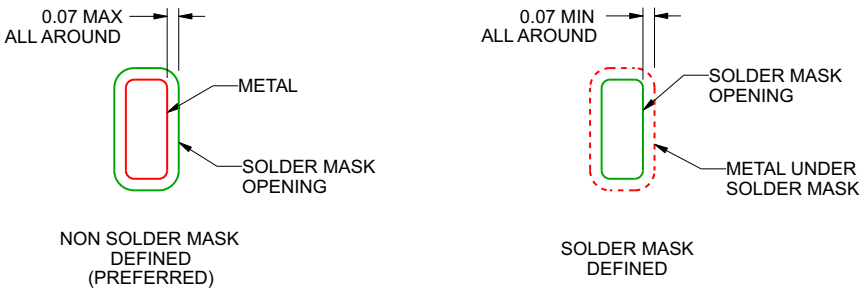
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222419/A 10/2015

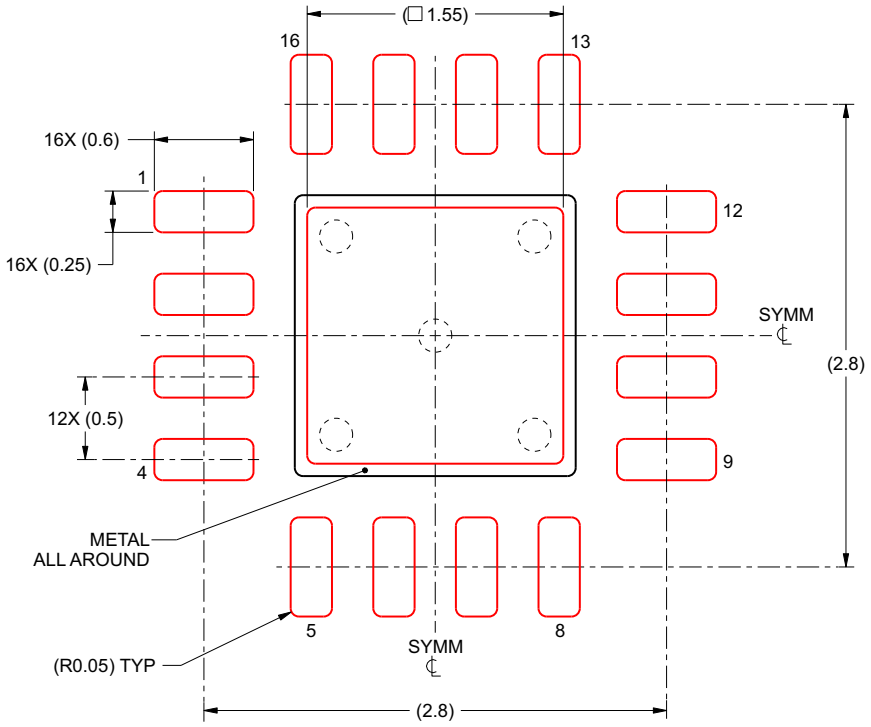
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RGT0016C — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222419/A 10/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62090RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW	Samples
TPS62090RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBW	Samples
TPS62091RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX	Samples
TPS62091RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBX	Samples
TPS62092RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBY	Samples
TPS62092RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBY	Samples
TPS62093RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBZ	Samples
TPS62093RGTT	ACTIVE	VQFN	RGT	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SBZ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

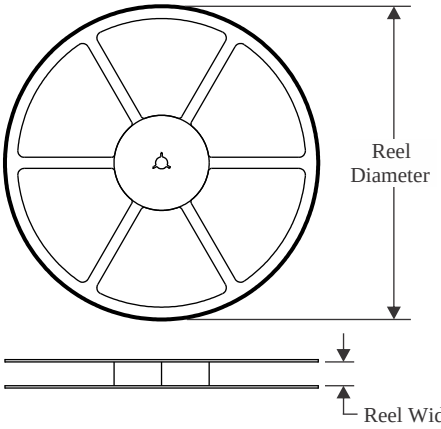
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

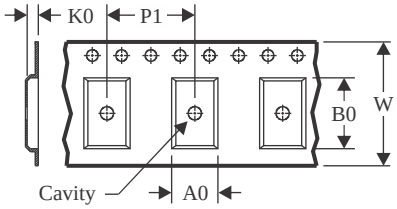
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

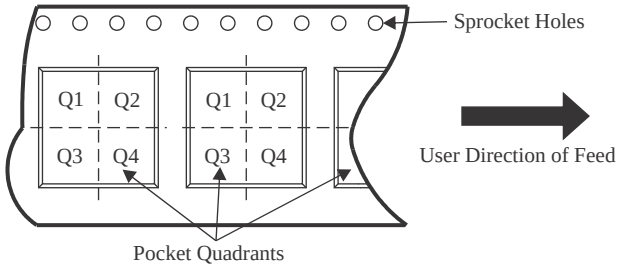


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

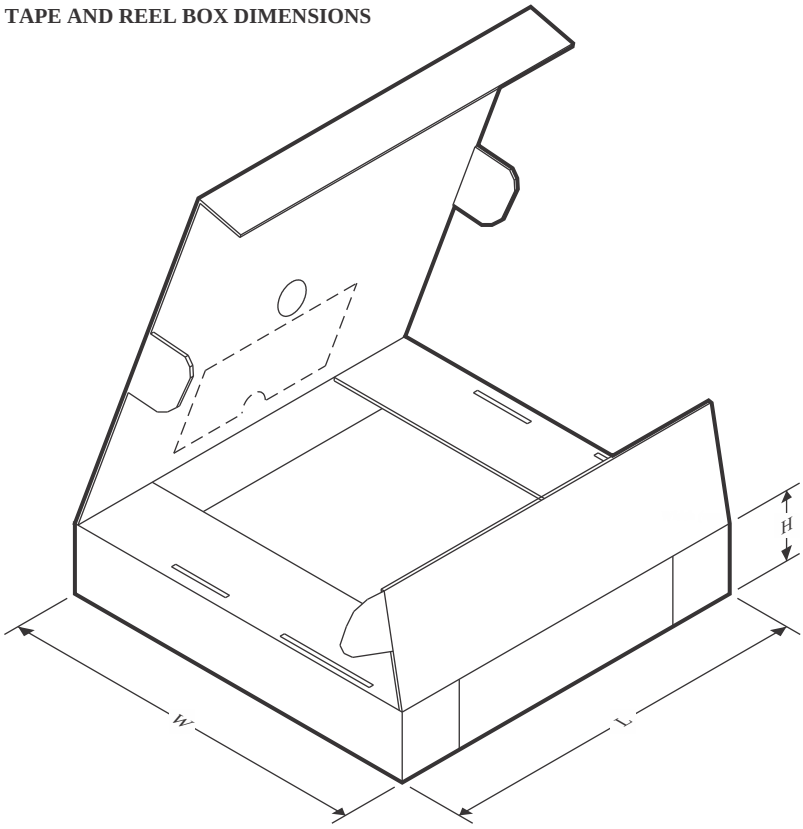
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62090RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62090RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS62091RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62092RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62092RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62092RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62092RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTT	VQFN	RGT	16	250	180.0	12.5	3.3	3.3	1.1	8.0	12.0	Q2
TPS62093RGTT	VQFN	RGT	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

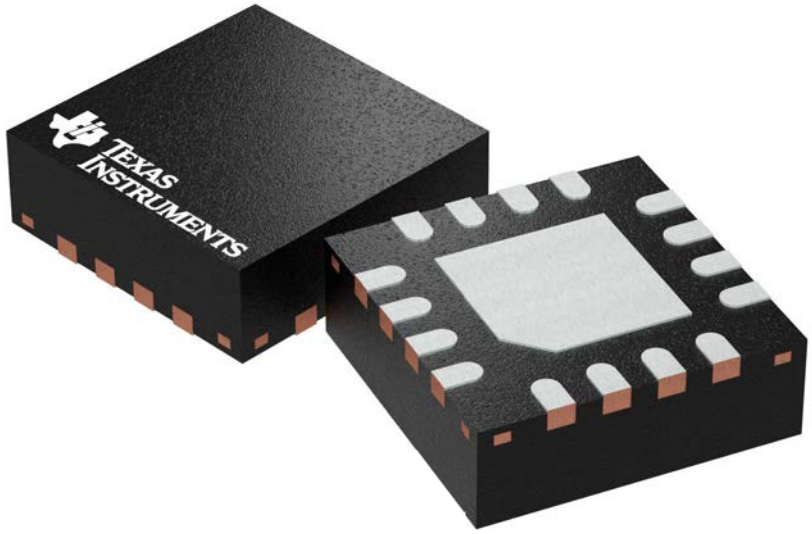


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62090RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS62090RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62091RGTR	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS62091RGTT	VQFN	RGT	16	250	338.0	355.0	50.0
TPS62091RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62092RGTR	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS62092RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS62092RGTT	VQFN	RGT	16	250	210.0	185.0	35.0
TPS62092RGTT	VQFN	RGT	16	250	338.0	355.0	50.0
TPS62093RGTR	VQFN	RGT	16	3000	346.0	346.0	33.0
TPS62093RGTR	VQFN	RGT	16	3000	338.0	355.0	50.0
TPS62093RGTT	VQFN	RGT	16	250	338.0	355.0	50.0
TPS62093RGTT	VQFN	RGT	16	250	210.0	185.0	35.0

RGT 16 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



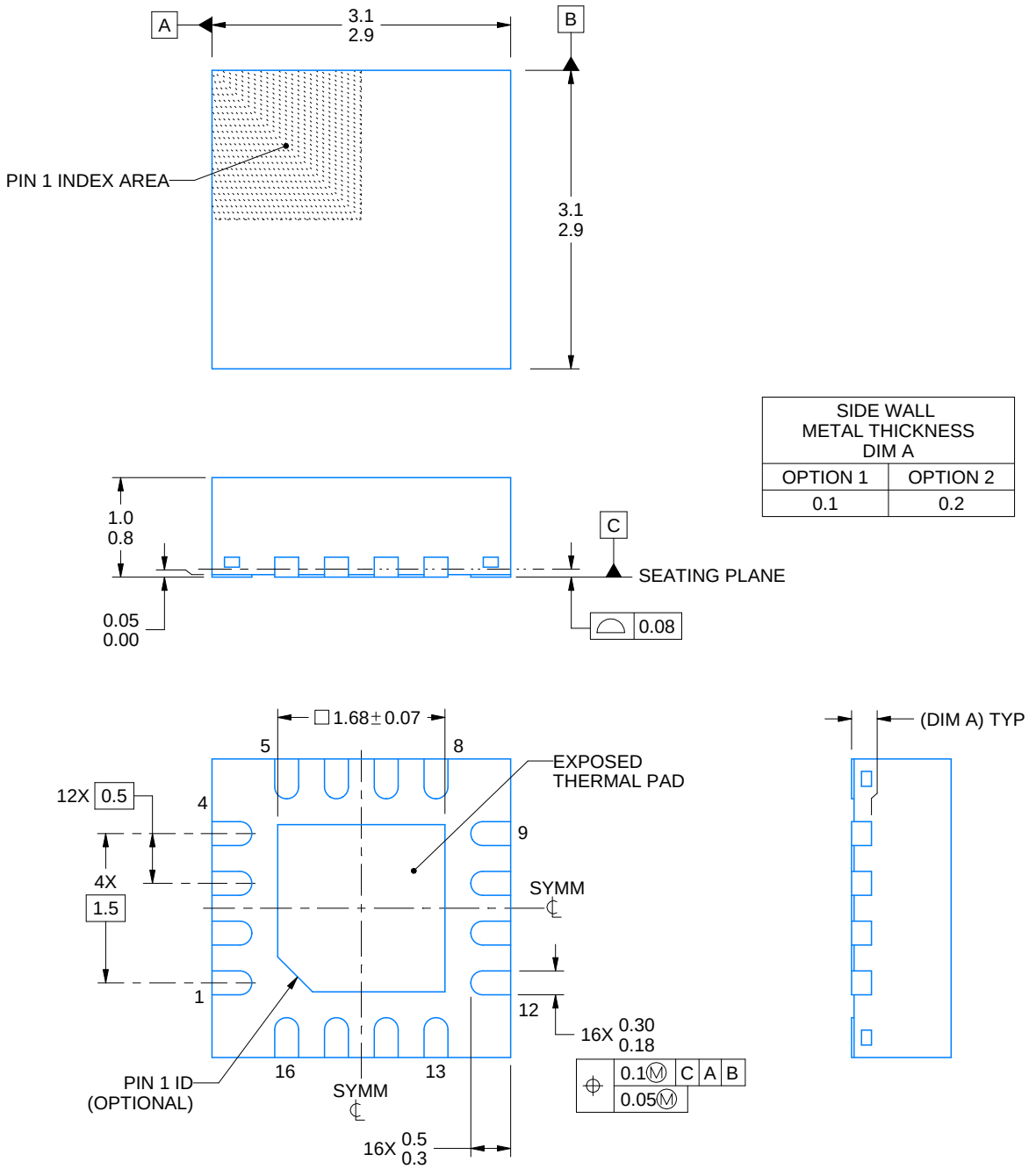
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

RGT0016C

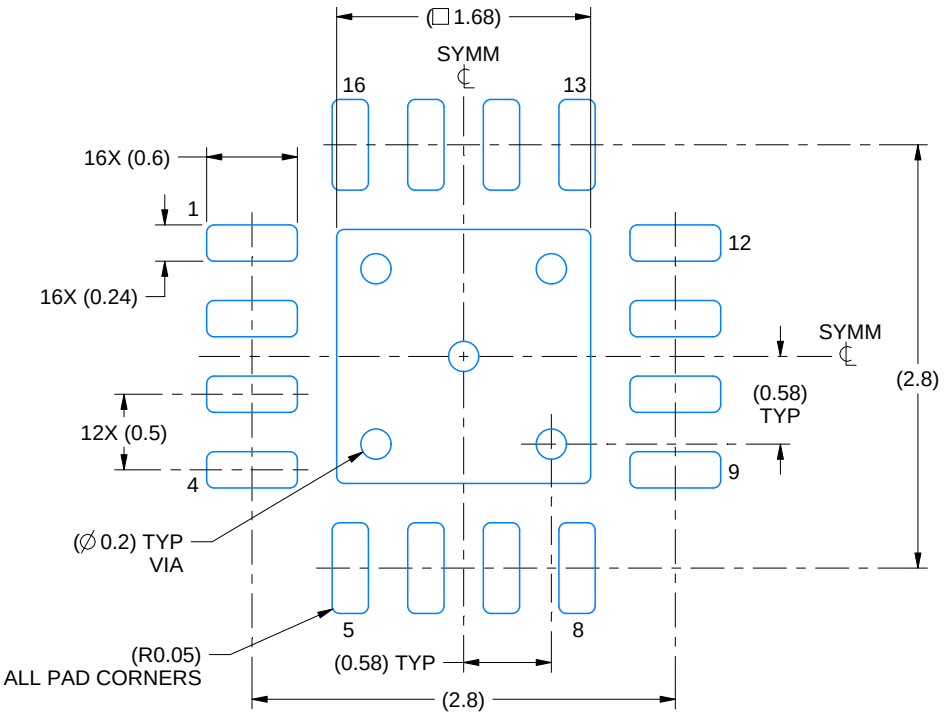
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

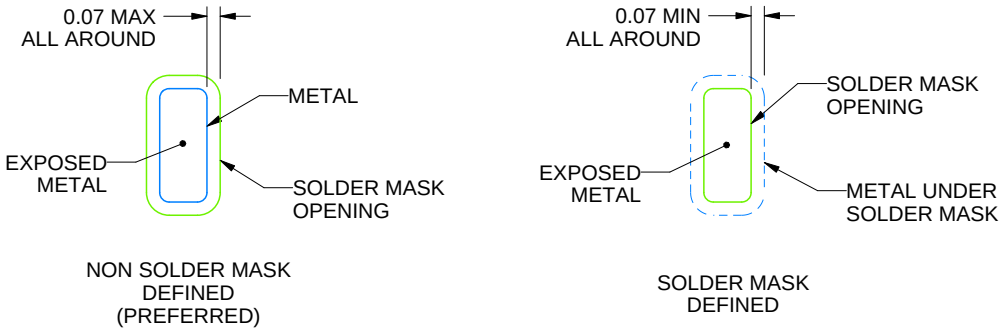


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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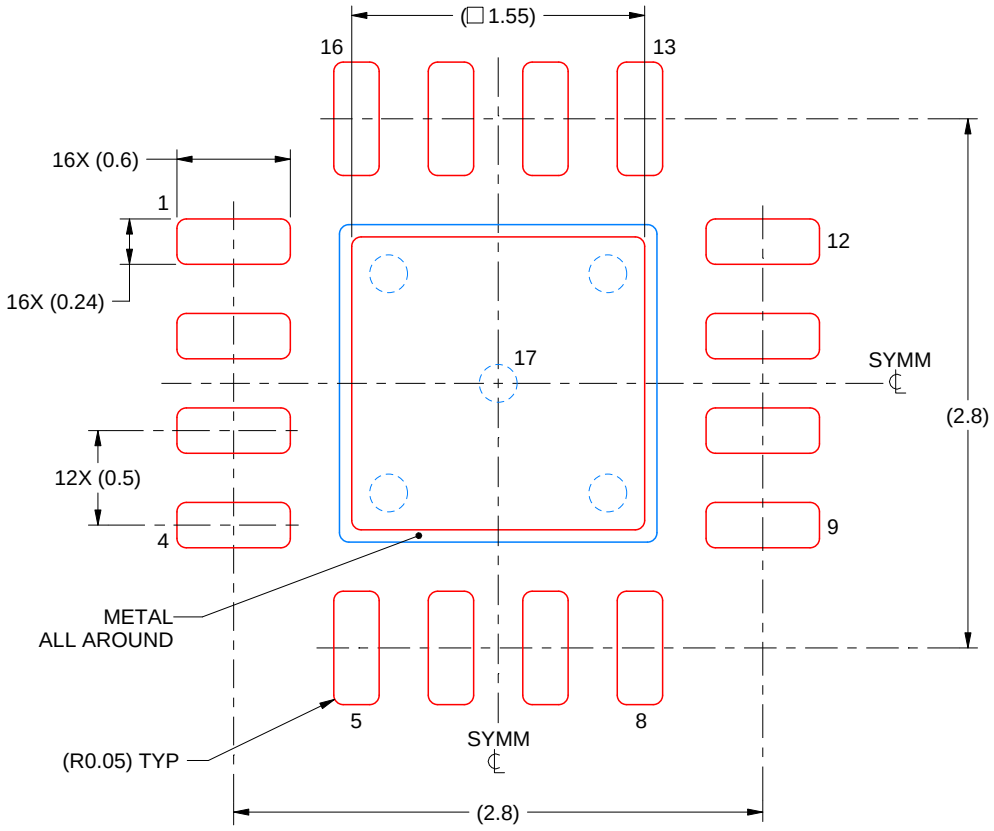
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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