TEXAS INSTRUMENTS
TPS62065-Q1, TPS62067-Q1
JAJSJ58B – JANUARY 2015 – REVISED AUGUST 2023

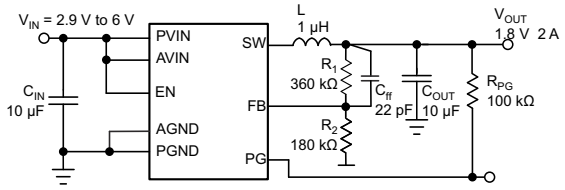
TPS6206x-Q1 2 × 2 SON パッケージ封止、3MHz、2A、車載用降圧コンバータ

1 特長

- 新製品を利用可能:TPS628502-Q1、6V 降圧コンバータ、SOT583 パッケージ
- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時の接合部温度範囲:-40℃～125℃
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 機能安全規格に対応
  - 機能安全システム設計に役立つ資料を利用可能
- 3MHz のスイッチング周波数
- V_{IN} 範囲:2.9V～6V
- 最大 97% の効率
- パワーセーブ・モードと 3MHz 固定 PWM モード
- パワー・グッド出力
- PWM モード時の出力電圧精度:±1.5%
- 出力コンデンサの放電機能
- 静止電流:18μA (代表値)
- 100% デューティ・サイクル動作による最小のドロップアウト電圧
- 電圧ポジショニング
- クロック・ディザリング
- 2 × 2 × 0.75mm の WSON で供給

2 アプリケーション

- 先進運転支援システム (ADAS)
- 車載用インフォテインメントおよびクラスタ



代表的なアプリケーション回路

3 概要

TPS62065-Q1、TPS62067-Q1、TPS62067A-Q1 デバイスは高効率の同期整流式降圧 DC/DC コンバータです。本デバイスは、最大 2A の出力電流を供給できます。

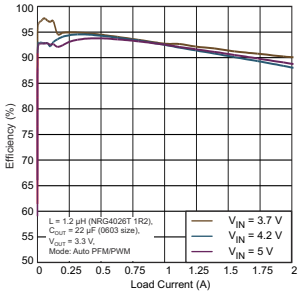
2.9V～6V の入力電圧範囲に対応でき、5V または 3.3V のシステム電源レールからの電力変換に最適です。TPS62065-Q1 および TPS62067-Q1 デバイスは、3MHz の固定スイッチング周波数で動作し、軽負荷電流時にはパワーセーブ・モードに自動的に切り替わり、負荷電流範囲の全体にわたって高効率を維持します。パワーセーブ・モードは、低出力電圧リップルに最適化されています。さらに低ノイズが要求されるアプリケーションの場合、TPS62065-Q1 デバイスは MODE ピンを High にすることで、強制的に固定周波数 PWM モードにすることができます。TPS62067-Q1 にはオープン・ドレインのパワー・グッド出力とパワーセーブ・モードがあり、TPS62067A-Q1 は固定周波数 PWM モードで動作します。シャットダウン・モードでは、消費電流が 5μA に低下し、内部回路により出力コンデンサが放電されます。TPS62065-Q1、TPS62067-Q1、および TPS62067A-Q1 デバイスは 1μH の小型インダクタと、10μF の小型出力コンデンサで動作するよう最適化されているため、最小のソリューション・サイズと、高いレギュレーション性能を実現できます。

新製品の TPS628502-Q1 は BOM コストとサイズを抑え、高効率などの特長を備えています。

製品情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)
TPS62065-Q1、TPS62067-Q1、TPS62067A-Q1	DSG (WSON、8)	2.00mm × 2.00mm × 0.80mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



効率と負荷電流との関係

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (May 2020) to Revision B (August 2023)	Page
• ドキュメント全体にわたって表、図、相互参照の採番方法を更新	1
• ドキュメント全体を通してデバイス表のフォーマットを更新し、TPS62067A-Q1 を追加	1
• ドキュメントのタイトルを更新	1

Changes from Revision * (January 2015) to Revision A (May 2020)	Page
• 機能安全対応の箇条書き項目を追加	1
• Updated power-good description	11
• Updated the output discharge function description	11
• Added PFM/PWM mode checking block description	12
• Updated the recommended list of the inductors	15
• Corrected the output current value on Figure 20	17

5 Device Comparison Table

PART NUMBER	MODE/PG FUNCTION
TPS62065-Q1	MODE = selectable; Power Good = no
TPS62067-Q1	Automatic PWM/PFM transition; Power Good = yes
TPS62067A-Q1	Forced PWM; Power Good = yes

6 Pin Configuration and Functions

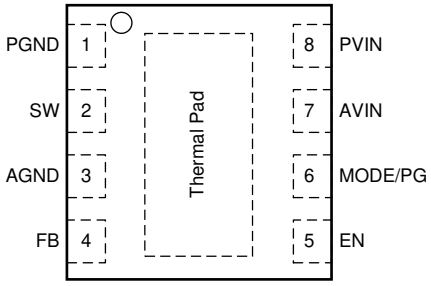


図 6-1. DSG Package 8-Pin WSON With Exposed Thermal Pad Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	PGND	—	GND supply pin for the output stage
2	SW	OUT	This pin is the switch pin and is connected to the internal MOSFET switches. Connect the external inductor between this terminal and the output capacitor.
3	AGND	—	Analog GND supply pin for the control circuit
4	FB	IN	Feedback pin for the internal regulation loop. Connect the external resistor divider to this pin. In case of the fixed output voltage option, connect this pin directly to the output capacitor.
5	EN	IN	This pin is the enable pin of the device. Pulling this pin to low forces the device into shutdown mode. Pulling this pin to high enables the device. This pin must be terminated.
6	MODE/PG	IN	**MODE**: MODE pin = high forces the device to operate in fixed frequency PWM mode. MODE pin = low enables the power save mode with automatic transition from PFM mode to fixed frequency PWM mode. This pin must be terminated. (TPS62065-Q1)
		Open Drain	**PG**: Power Good open-drain output. Connect an external pullup resistor to a rail which is below or equal AVIN. (TPS62067-Q1)
7	AVIN	IN	Analog V_{IN} power supply for the control circuit must be connected to PVIN and input capacitor.
8	PVIN	PWR	V_{IN} power supply pin for the output stage
—	Thermal Pad	—	For good thermal performance, this pad must be soldered to the land pattern on the PCB. Use this pad as device GND.

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage (2)	AVIN, PVIN	–0.3	7	V
	EN, MODE/PG, FB	–0.3	V_{IN} + 0.3 < 7	
	SW	–0.3	7	
Current (sink)	into PG		1	mA
Current (source)	Peak output	Internally limited		A
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2500	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 5, and 8)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
AV_{IN} , PV_{IN}	Supply voltage	2.9		6	V
	Output current capability			2000	mA
	Output voltage range for adjustable voltage	0.8		VIN	V
L	Effective Inductance Range	0.7	1	1.6	µH
C_{OUT}	Effective Output Capacitance Range	4.5	10	22	µF
T_J	Operating junction temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.78	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	80.60	
$R_{\theta JB}$	Junction-to-board thermal resistance	34.63	
ψ_{JT}	Junction-to-top characterization parameter	1.65	
ψ_{JB}	Junction-to-board characterization parameter	35.02	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.61	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over operating junction temperature range (T_J = –40°C to 125°C), typical values are at T_J = 25°C. Unless otherwise noted, specifications apply for condition V_{IN} = EN = 3.6 V. External components C_{IN} = 10 µF 0603, C_{OUT} = 10 µF 0603, L = 1 µH.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Input voltage range		2.9		6	V
I_Q	Operating quiescent current	I_{OUT} = 0 mA, device operating in PFM mode and not device not switching		18		µA
I_{SD}	Shutdown current	EN = GND, current into AVIN and PVIN combined		0.1	5	µA
V_{UVLO}	Undervoltage lockout threshold	Falling	1.73	1.78	1.83	V
		Rising	1.9	1.95	1.99	
ENABLE, MODE						
V_{IH}	High level input voltage	2.9 V ≤ V_{IN} ≤ 6 V	1		6	V
V_{IL}	Low level input voltage	2.9 V ≤ V_{IN} ≤ 6 V	0		0.4	V
I_{IN}	Input bias current	EN, Mode tied to GND or AVIN		0.01	1	µA
POWER GOOD OPEN DRAIN OUTPUT						
V_{THPG}	Power good threshold voltage	Rising feedback voltage	93%	95%	98%	
		Falling feedback voltage	87%	90%	92%	
V_{OL}	Output low voltage	I_{OUT} = –1 mA; must be limited by external pullup resistor (2)			0.3	V
I_{LKG}	Leakage current into PG pin	$V_{(PG)}$ = 3.6 V			100	nA
t_{PGDL}	Internal power good delay time			5		µs
POWER SWITCH						
$R_{DS(on)}$	High-side MOSFET on-resistance	V_{IN} = 3.6 V (2)		120	180	mΩ
		V_{IN} = 5 V(2)		95	150	
$R_{DS(on)}$	Low-side MOSFET on-resistance	V_{IN} = 3.6 V(2)		90	130	mΩ
		V_{IN} = 5 V(2)		75	100	
I_{LIMF}	Forward current limit MOSFET high-side and low-side	2.9 V ≤ V_{IN} ≤ 6 V	2300	2750	3300	mA
T_{SD}	Thermal shutdown	Increasing junction temperature		150		°C
	Thermal shutdown hysteresis	Decreasing junction temperature		10		
OSCILLATOR						
f_{SW}	Oscillator frequency	2.9 V ≤ V_{IN} ≤ 6 V	2.6	3	3.4	MHz
OUTPUT						
V_{ref}	Reference voltage			600		mV
$V_{FB(PWM)}$	Feedback voltage PWM Mode	PWM operation, MODE = V_{IN} , 2.9 V ≤ V_{IN} ≤ 6 V, 0-mA load	–1.5%	0%	1.5%	
$V_{FB(PFM)}$	Feedback voltage PFM mode, Voltage Positioning	device in PFM mode, voltage positioning active(1)		1%		
V_{FB}	Load regulation			–0.5		%/A
	Line regulation			0		%/V
$R_{(Discharge)}$	Internal discharge resistor	Activated with EN = GND, 2.9 V ≤ V_{IN} ≤ 6 V, 0.8 ≤ V_{OUT} ≤ 3.6 V	75	200	1450	Ω
t_{START}	Start-up time	Time from active EN to reach 95% of V_{OUT}		500		µs

(1) In PFM mode, the internal reference voltage is set to typ. 1.01 × V_{ref}. See the parameter measurement information.
(2) Maximum value applies for T_J = 85°C

Typical Characteristics

表 7-1. Table of Graphs

		FIGURE
Shutdown Current	Input Voltage and Ambient Temperature	図 7-1
Quiescent Current	Input Voltage	図 7-2
Oscillator Frequency	Input Voltage	図 7-3
Static Drain-Source On-State Resistance	Input Voltage, Low-Side Switch	図 7-4
	Input Voltage, High-Side Switch	図 7-5
$R_{DISCHARGE}$	Input Voltage vs. V_{OUT}	図 7-6

Typical Characteristics

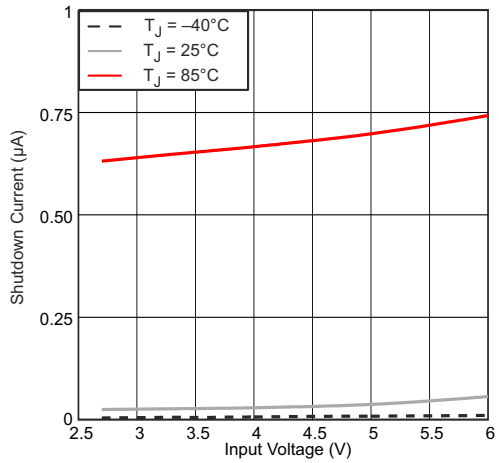


図 7-1. Shutdown Current vs Input Voltage and Ambient Temperature

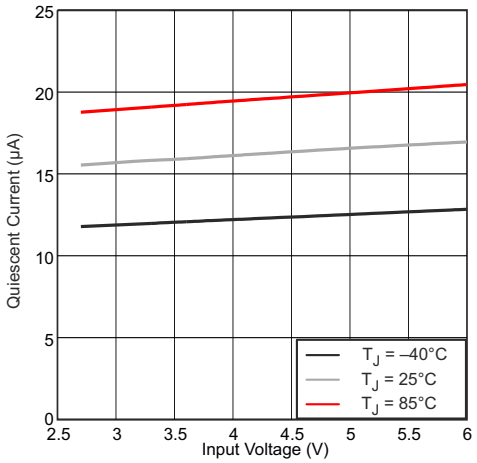


図 7-2. Quiescent Current vs Input Voltage

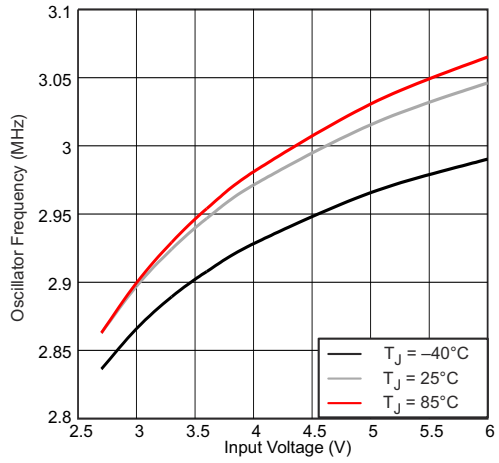
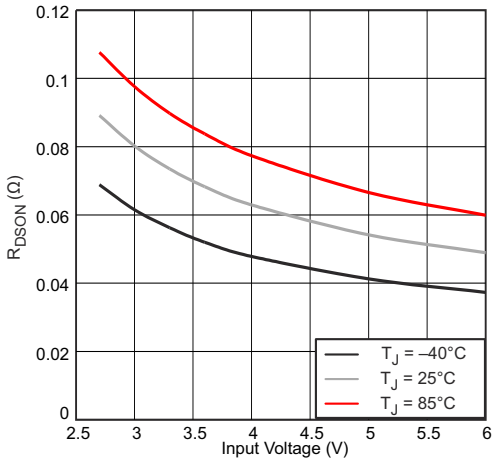


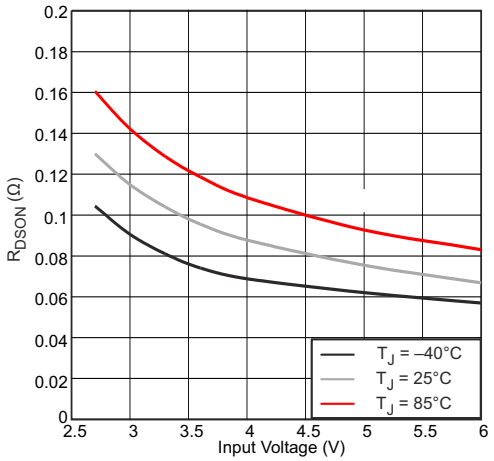
図 7-3. Oscillator Frequency vs Input Voltage



Low-Side Switch

図 7-4. Static Drain-Source On-State Resistance vs Input Voltage

Typical Characteristics



High-Side Switch

図 7-5. Static Drain-Source On-State Resistance vs Input Voltage

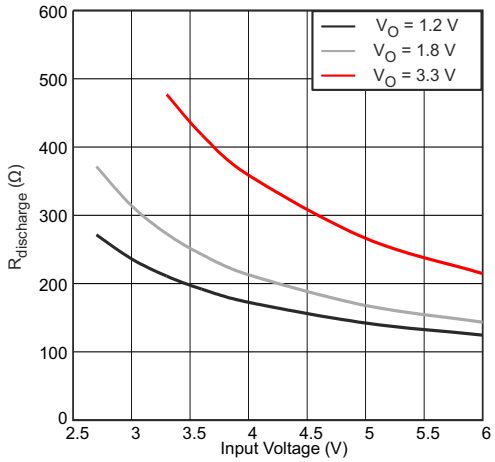
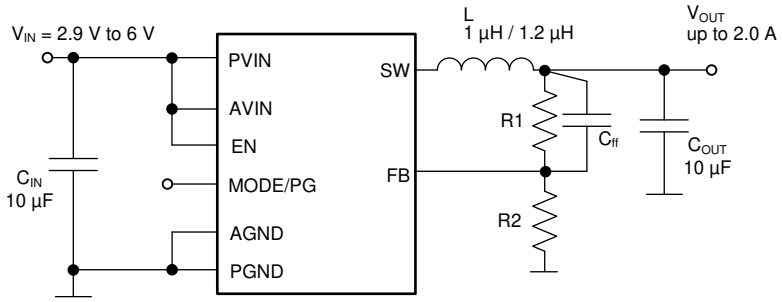


図 7-6. $R_{DISCHARGE}$ vs Input Voltage

8 Parameter Measurement Information



L: LQH44PN1R0NP0, L = 1 µH, Murata, NRG4026T1R2, L = 1.2 µH, Taiyo Yuden

C_{IN}/C_{OUT}: GRM188R60J106U, Murata 0603 size

9 Detailed Description

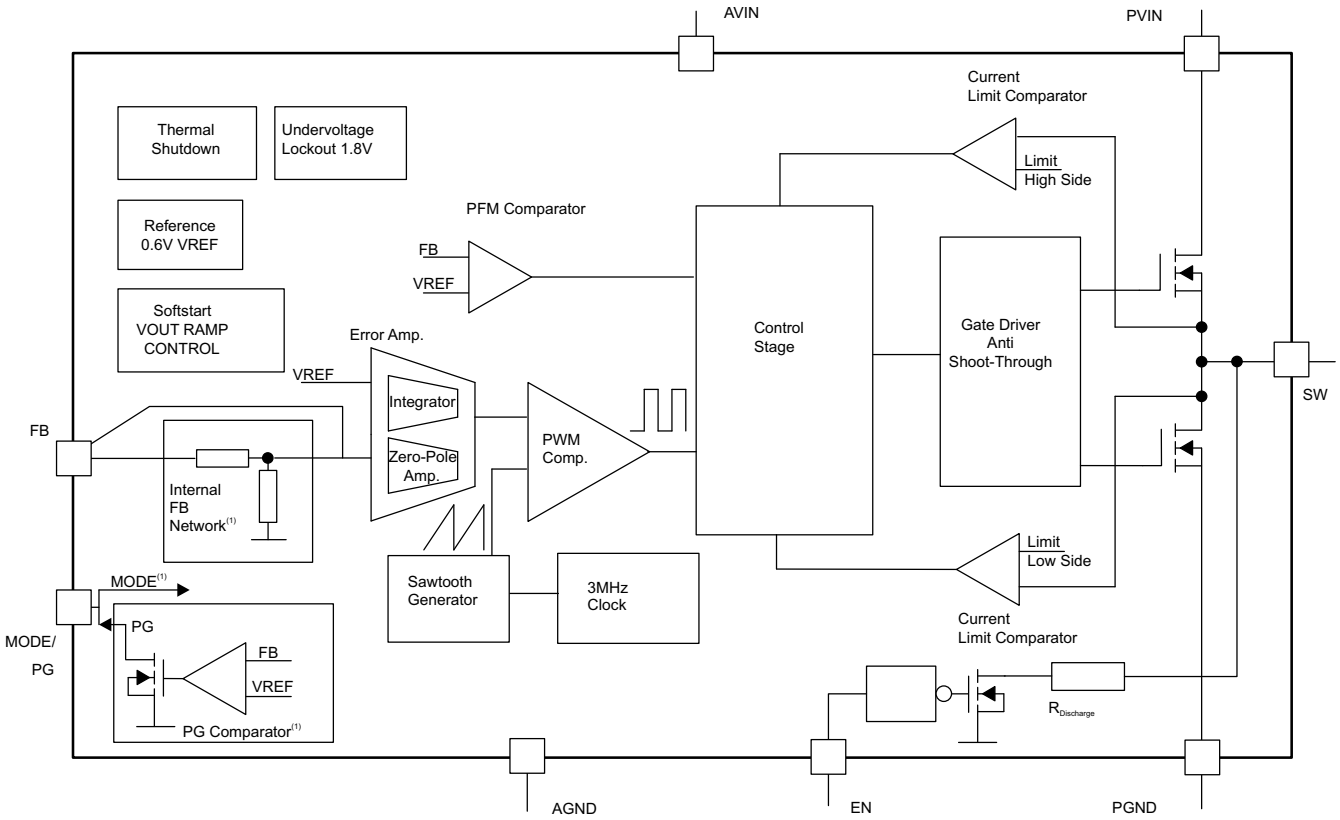
9.1 Overview

The TPS62065-Q1, TPS62067-Q1 step-down converters operates with 3-MHz (typical) fixed-frequency pulse-width modulation (PWM) at moderate to heavy load currents. At light load currents, the converter can automatically enter power save mode and then operate in pulse-frequency mode (PFM). The TPS62067A-Q1 operates with 3-MHz (typical) fixed-frequency pulse-width modulation (PWM) at all loads.

During PWM operation, the converter uses a unique fast-response voltage-mode controller scheme with input-voltage feedforward to achieve good line and load regulation, which allows the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the high-side MOSFET switch is turned on. The current flows from the input capacitor through the high-side MOSFET switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turns off the switch. The current-limit comparator also turns off the switch in case the current-limit of the high-side MOSFET switch is exceeded. After a dead time preventing shoot-through current, the low-side MOSFET rectifier is turned on and the inductor current ramps down. The current now flows from the inductor to the output capacitor and to the load. The current returns back to the inductor through the low-side MOSFET rectifier.

The next cycle is initiated by the clock signal again turning off the low-side MOSFET rectifier and turning on the high-side MOSFET switch.

9.2 Functional Block Diagram



A. Function depends on device option.

9.3 Feature Description

9.3.1 Mode Selection (TPS62065-Q1) and Forced PWM Mode (TPS62067A-Q1)

The MODE pin allows mode selection between forced PWM mode and power save mode.

Connecting this pin to GND enables the power save mode with an automatic transition between PWM and PFM mode. Pulling the MODE pin high forces the converter to operate in fixed frequency PWM mode, even at light load currents, which allows simple filtering of the switching frequency for noise-sensitive applications. In this mode, the efficiency is lower compared to when the device is in power save mode during light loads.

The condition of the MODE pin can be changed during operation and allows efficient power management by adjusting the operation mode of the converter to the specific system requirements.

For the TPS62067-Q1, where the MODE pin is replaced with the PG pin, the power save mode is enabled per default. On the other hand, the TPS62067A-Q1operate at forced PWM by default.

9.3.2 Power Good (PG, TPS62067x-Q1)

The Power Good (PG) pin indicates whether the output voltage has reached its regulation voltage. The PG pin can be used for sequencing of other system rails. The PG pin is an open-drain output that requires a pullup resistor to any voltage up to any voltage rail lower or equal the voltage applied to AVIN pin of the device. A 100-kΩ pullup resistor is recommended, and this value can be adjusted as described in the *Choosing an Appropriate Pulllup/Pulldown Resistor for Open Drain Outputs Application Report*.

If the power-good output is not used, it is recommended to tie to GND or leave open. The PG pin can sink a maximum of 1 mA. 表 9-1 shows the typical logic states of the PG pin.

表 9-1. PG Pin Functional Table

DEVICE CONDITIONS		PG STATUS	
		HIGH IMPEDANCE	LOW
Enable	EN = High, V_{FB} ≥ 0.57 V	√	
	EN = High, V_{FB} ≤ 0.54 V		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$V_{IN} < V_{UVLO}$	undefined	

9.3.3 Enable

Setting the EN pin high enables the device. At first, the internal reference is activated and the internal analog circuits are settled. Afterwards, the soft start is activated and the output voltage is ramped up. The output voltage reaches 95% of the nominal value within t_{START} which is 500 µs (typical) after the device has been enabled. The EN input can be used to control power sequencing in a system with various DC-DC converters. The EN pin can connect to the output of another converter to drive the EN pin high and get a sequencing of supply rails.

9.3.4 Shutdown and Output Discharge

When EN is pulled low, the device enters shutdown mode. In this mode, all circuits are disabled and the SW pin is connected to PGND through an internal resistor to discharge the output. This feature ensures a start-up in a discharged output capacitor after the converter is enabled again and prevents a floating charge on the output capacitor. The input voltage must remain higher than 1 V (TYP) to keep the output discharge function.

9.3.5 Soft Start

The devices have an internal soft-start circuit that controls the ramp up of the output voltage. When the converter is enabled and the input voltage is above the UVLO threshold, V_{UVLO}, the output voltage ramps up from 5% to 95% of the nominal value with a t_{Ramp} value of 250 µs (typical). The ramp time limits the inrush current in the converter during start-up and prevents possible input voltage drops when a battery or high impedance power source is used.

During soft start, the switch current-limit is reduced to 1/3 of the nominal value, I_{LIMF}, until the output voltage reaches 1/3 of the nominal value. When the output voltage trips this threshold, the device operates with the nominal current limit, I_{LIMF}.

9.3.6 Undervoltage Lockout (UVLO)

The UVLO circuit prevents the device from malfunctioning at low input voltages and from excessive discharge of the battery. It disables the output stage of the converter after the falling VIN trips the UVLO threshold, V_{UVLO}. The UVLO threshold, V_{UVLO}, for falling V_{IN} is typically 1.78 V. The device starts operation after the rising V_{IN} trips V_{UVLO} again at typically 1.95 V.

9.3.7 Internal Current Limit and Foldback Current Limit For Short-Circuit Protection

During normal operation, the high-side and low-side MOSFET switches are protected by the current limit I_{LIMF}. When the high-side MOSFET switch reaches the current limit, it turns off and the low-side MOSFET switch turns on. The high-side MOSFET switch can only turn on again when the current in the low-side MOSFET switch decreases below I_{LIMF}. The device is capable of providing peak-inductor currents up to the internal current limit,$_{ILIMF.}$.

As soon as the switch current limits are met and the output voltage falls below 1/3 of the nominal output voltage because of overload or short circuit condition, the foldback current limit is enabled. In this case, the switch current-limit is reduced to 1/3 of the nominal value I_{LIMF}.

Because the short-circuit protection is enabled during start-up, the device does not deliver more than 1/3 of the nominal current limit, I_{LIMF}, until the output voltage exceeds 1/3 of the nominal output voltage. This protection must be considered when a load is connected to the output of the converter, which acts as a current sink.

9.3.8 Clock Dithering

To reduce the noise level of switch-frequency harmonics in the higher RF bands, the devices have a built-in clock-dithering circuit. The oscillator frequency is slightly modulated with a sub clock, causing a clock dither of 6 ns (typical).

9.3.9 Thermal Shutdown

As soon as the junction temperature, T_J, exceeds 150°C (typical), the device enters thermal shutdown. In this mode, the high-side and low-side MOSFETs are turned off. The device continues operation with a soft start after the junction temperature falls below the thermal shutdown hysteresis.

9.4 Device Functional Modes

9.4.1 Power Save Mode

The TPS62065-Q1 pulling the MODE pin low enables power save mode. For the TPS62067-Q1, power-save mode is enabled per default. If the load current decreases, the converter enters power save mode operation automatically. During power save mode, the converter skips switching and operates with reduced frequency in PFM mode with a minimum quiescent current to maintain high efficiency. The converter positions the output voltage 1% (typical) above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

The transition from PWM mode to PFM mode occurs when the inductor current in the low-side MOSFET switch becomes zero, which indicates discontinuous conduction mode.

During power save mode, the output voltage is monitored with a PFM comparator. As the output voltage falls below the PFM comparator threshold of $V_{OUTnominal}$ +1%, the device starts a PFM current pulse. For this, the high-side MOSFET switch turns on and the inductor current ramps up. After the on-time expires, the switch is turned off and the low-side MOSFET switch is turned on until the inductor current becomes zero. In case the output voltage is still below the PFM comparator threshold, further PFM current pulses are generated until the PFM comparator reaches its threshold. The converter starts switching again after the output voltage drops below the PFM comparator threshold due to the load current.

If power save mode is enabled (TPS62065-Q1, MODE = Low), the device regularly checks to see if PFM mode must be entered. The checking occurs at about a 100-kHz rate and can show up as a small ripple on the output.

Enabled forced PWM mode (MODE = High) disables the checking circuit. The TPS62067-Q1 always checks for PFM mode.

9.4.1.1 Dynamic Voltage Positioning

This feature reduces the voltage undershoots or overshoots at load steps from light to heavy load and vice versa. This feature is active in power save mode and regulates the output voltage 1% higher than the nominal value. This provides more headroom for both the voltage drop at a load step, and the voltage increase at a load throw-off.

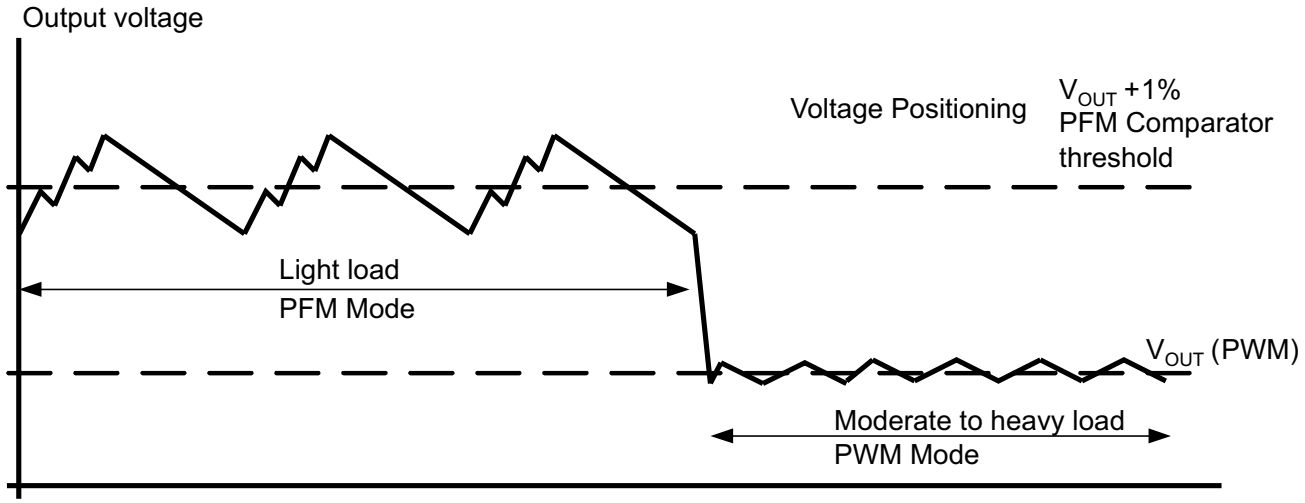


図 9-1. Power Save Mode Operation with Automatic Mode Transition

9.4.1.2 100% Duty-Cycle Low-Dropout Operation

The device starts to enter 100% duty cycle mode as the input voltage comes close to the nominal output voltage. To maintain the output voltage, the high-side MOSFET switch is turned on 100% for one or more cycles.

To further decrease VIN, the high-side MOSFET switch is turned on completely. In this case, the converter offers a low input-to-output voltage difference. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range.

The minimum input voltage to maintain regulation depends on the load current and output voltage, and can be calculated as:

$$V_{IN}min = V_Omax + I_Omax \times (R_{DS(on)}max + R_L) \quad (1)$$

where

- $I_O$max = maximum output current
- $R_{DS(on)}$max = maximum P-channel switch $R_{DS(on)}$
- R_L = DC resistance of the inductor
- $V_O$max = nominal output voltage plus maximum output voltage tolerance

10 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The TPS62065-Q1, TPS62067-Q1, and TPS62067A-Q1 are highly efficient, synchronous, 2-A, step-down DC/DC converters.

10.2 Typical Application

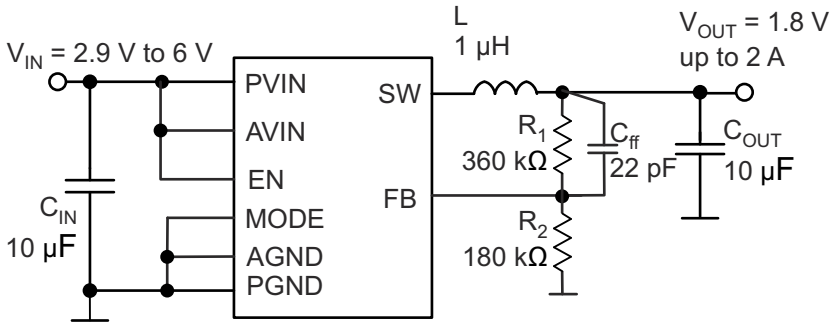


図 10-1. TPS62065-Q1 Adjustable 1.8-V Output-Voltage Configuration

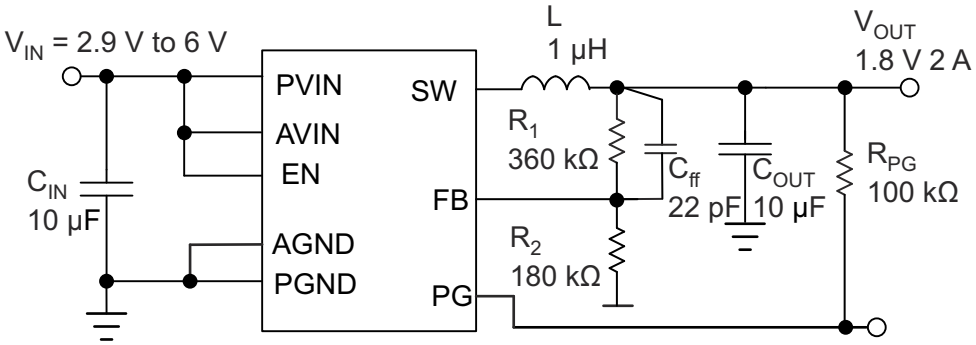


図 10-2. TPS62067x-Q1 Adjustable 1.8-V Output-Voltage Configuration

10.2.1 Design Requirements

The device operates over an input voltage range from 2.9 V to 6 V. The output voltage is adjustable using an external feedback divider.

10.2.2 Detailed Design Procedure

10.2.2.1 Output Voltage Setting

The output voltage can be calculated to:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \qquad R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_2 \tag{2}$$

with an internal reference voltage V_{REF} typically 0.6 V.

To minimize the current through the feedback divider network, R_2 must be within the range of 120 kΩ to 360 kΩ. The sum of R_1 and R_2 must not exceed approximately 1 MΩ in order to keep the network robust against noise. An external feedforward capacitor, C_{ff}, is required for optimum regulation performance. Lower resistor values can be used. R_1 and C_{ff} place a zero in the loop. The right value for C_{ff} can be calculated as:

$$f_z = \frac{1}{2 \times \pi \times R_1 \times C_{ff}} = 25 \text{ kHz} \quad (3)$$

$$C_{ff} = \frac{1}{2 \times \pi \times R_1 \times 25 \text{ kHz}} \quad (4)$$

10.2.2.2 Output Filter Design (Inductor And Output Capacitor)

The internal compensation network of the devices is optimized for a LC output filter with a corner frequency of:

$$f_C = \frac{1}{2 \times \pi \times \left(\sqrt{1 \text{ µH} \times 10 \text{ µF}}\right)} = 50 \text{ kHz} \quad (5)$$

The part operates with nominal inductors of 1 µH to 1.2 µH and with 10-µF to 22-µF small X5R and X7R ceramic capacitors. Refer to the lists of inductors and capacitors. The part is optimized for a 1-µH inductor and 10-µF output capacitor.

10.2.2.2.1 Inductor Selection

The inductor value has a direct effect on the ripple current. The selected inductor has to be rated for its DC resistance and saturation current. The inductor ripple current (ΔI_L) decreases with higher inductance and increases with higher V_I or V_O.

式 6 calculates the maximum inductor current in PWM mode under static load conditions. The saturation current of the inductor must be rated higher than the maximum inductor current as calculated with 式 7. TI makes this recommendation because during heavy load transient, the inductor current rises above the calculated value.

$$\Delta I_L = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \quad (6)$$

where

- ΔI_L = peak-to-peak inductor ripple current
- L = inductor value
- f = switching frequency (3-MHz typical)

$$I_{L\,max} = I_{OUT\,max} + \frac{\Delta I_L}{2} \quad (7)$$

where

- I_{Lmax} = maximum inductor current

A more conservative approach is to select the inductor current rating just for the switch current limit I_{LIMF} of the converter.

The total losses of the coil have a strong impact on the efficiency of the DC/DC conversion and consist of both the losses in the DC resistance $R_{(DC)}$ and the following frequency-dependent components:

- The losses in the core material (magnetic hysteresis loss, especially at high switching frequencies)
- Additional losses in the conductor from the skin effect (current displacement at high frequencies)
- Magnetic field losses of the neighboring windings (proximity effect)

表 10-1. List of Inductors

INDUCTOR TYPE	INDUCTANCE (µH)	CURRENT (A)	DIMENSIONS (mm)	MANUFACTURER
XEL4020-102ME	1.0	13.25	4 × 4 × 2	Coilcraft
DFE252012PD-1R0M	1.0	3.8	2.5 × 2.0 × 1.2	Murata

10.2.2.2.2 Output Capacitor Selection

The advanced fast-response voltage mode control scheme of the devices allows the use of tiny ceramic capacitors. Ceramic capacitors with low ESR values have the lowest output voltage ripple and are recommended. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies and can not be used. For most applications, a nominal 10-µF or 22-µF capacitor is suitable. At small ceramic capacitors, the DC-bias effect decreases the effective capacitance. Therefore, a 22-µF capacitor can be used for output voltages higher than 2 V, see the list of capacitors.

In case additional ceramic capacitors in the supplied system are connected to the output of the DC/DC converter, the output capacitor C_{OUT} must be decreased to not exceed the recommended effective capacitance range. In this case, a loop stability analysis must be performed as described later.

At nominal load current, the device operates in PWM mode and the RMS ripple current is calculated as:

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (8)$$

10.2.2.2.3 Input Capacitor Selection

Because the buck converter has a pulsating input current, a low-ESR input capacitor is required for the best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. For most applications, a 10-µF ceramic capacitor is recommended. The input capacitor can be increased without any limit for better input voltage filtering.

Take care when using only small ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output or VIN step on the input can induce ringing at the V_{IN} pin. This ringing can couple to the output and be mistaken as loop instability or can even damage the part by exceeding the maximum ratings.

表 10-2. List of Capacitors

CAPACITANCE	TYPE	SIZE [mm^3]	SUPPLIER
10 µF	GRM188R60J106M	0603: 1,6 × 0,8 × 0,8	Murata
22 µF	GRM188R60G226M	0603: 1,6 × 0,8 × 0,8	Murata
22 µF	CL10A226MQ8NRNC	0603: 1,6 × 0,8 × 0,8	Samsung
10 µF	CL10A106MQ8NRNC	0603: 1,6 × 0,8 × 0,8	Samsung

10.2.2.3 Checking Loop Stability

The first step of circuit and stability evaluation is to look from a steady-state perspective at the following signal:

- Switching node, SW
- Inductor current, I_L
- Output ripple voltage, $V_{OUT(AC)}$

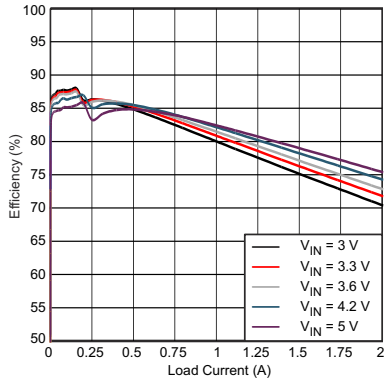
These are the basic signals that must be measured when evaluating a switching converter. When the switching waveform shows large duty cycle jitter or the output voltage or inductor current shows oscillations, the regulation loop can be unstable. This is often a result of board layout, wrong L-C output filter combinations, or both. As a next step in the evaluation of the regulation loop, test the load transient response. The results are most easily interpreted when the device operates in PWM mode at medium to high load currents.

During this recovery time, V_{OUT} can be monitored for settling time, overshoot, or ringing; that helps evaluate stability of the converter. Without any ringing, the loop has usually more than 45° of phase margin.

10.2.3 Application Curves

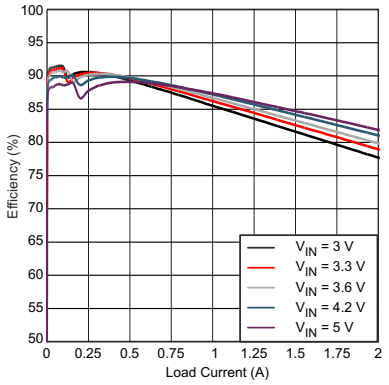
表 10-3. Table of Graphs

		FIGURE
η Efficiency	Load Current, V_{OUT} = 1.2 V, Auto PFM and PWM Mode, Linear Scale	図 10-3
	Load Current, V_{OUT} = 1.8 V, Auto PFM and PWM Mode, Linear Scale	図 10-4
	Load Current, V_{OUT} = 3.3 V, PFM and PWM Mode, Linear Scale	図 10-5
	Load Current, V_{OUT} = 1.8 V, Auto PFM and PWM Mode vs. Forced PWM Mode, Logarithmic Scale	図 10-6
Output Voltage Accuracy	Load Current, V_{OUT} = 1.8 V, Auto PFM and PWM Mode	図 10-7
	Load Current, V_{OUT} = 1.8 V, Forced PWM Mode	図 10-8
Typical Operation	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 500 mA, L = 1.2 µH, C_{OUT} = 10 µF	図 10-9
	PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 20 mA, L = 1.2 µH, C_{OUT} = 10 µF	図 10-10
Load Transient	PWM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 0.2 mA to 1 A	図 10-11
	PFM Mode, V_{IN} = 3.6 V, V_{OUT} = 1.2 V, 20 mA to 250 mA	図 10-12
	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, 200 mA to 1500 mA	図 10-13
Line Transient	PWM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	図 10-14
	PFM Mode, V_{IN} = 3.6 V to 4.2 V, V_{OUT} = 1.8 V, 500 mA	図 10-15
Start-Up into Load	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, Load = 2.2 Ω	図 10-16
Start-Up TPS62067-Q1	Into 2.2-Ω Load with Power Good	図 10-17
Output Discharge	V_{IN} = 3.6 V, V_{OUT} = 1.8 V, No Load	図 10-18
Shutdown TPS62067-Q1	V_{IN} = 4.2 V, V_{OUT} = 3.3 V, No Load, PG Pullup Resistor 10 kΩ	図 10-19



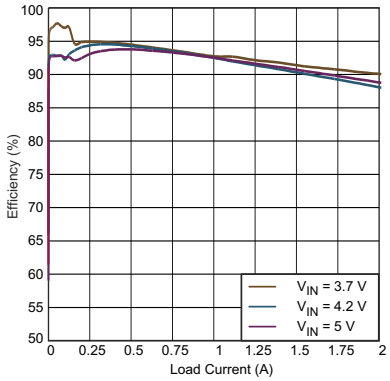
V_{OUT} = 1.2 V　　Linear Scale
L = 1.2 µH (NRG4026T 1R2)　　C_{OUT} = 10 µF (0603 size)

図 10-3. Efficiency vs Load Current Auto PFM and PWM MODE



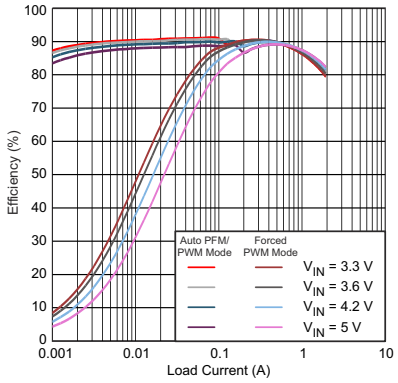
V_{OUT} = 1.8 V　　Linear Scale
L = 1.2 µH (NRG4026T 1R2)　　C_{OUT} = 10 µF (0603 size)

図 10-4. Efficiency vs Load Current PFM and PWM MODE



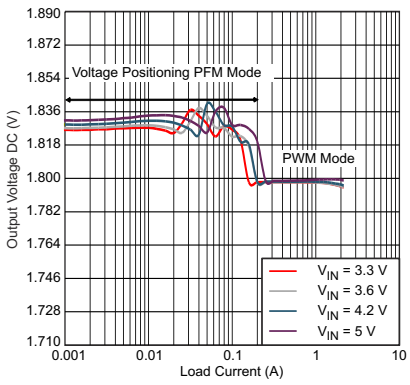
V_{OUT} = 3.3 V　　Linear Scale
L = 1.2 µH (NRG4026T 1R2)　　C_{OUT} = 22 µF (0603 size)

図 10-5. Efficiency vs Load Current Auto PFM and PWM MODE



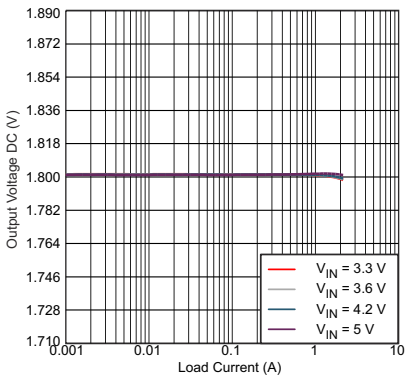
V_{OUT} = 1.8 V　　Logarithmic Scale
C_{OUT} = 10 µF (0603 size)　　L = 1.2 µH (NRG4026T 1R2)

図 10-6. Efficiency vs Load Current Auto PFM and PWM Mode vs. Forced PWM Mode



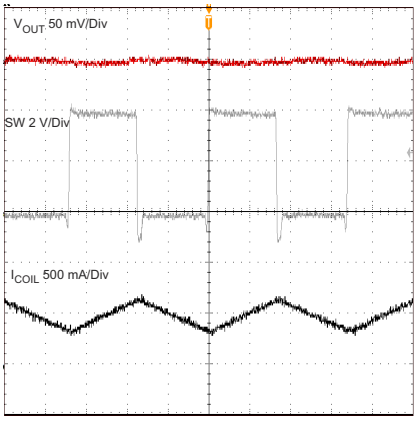
L = 1 µH　　V_{OUT} = 1.8 V　　C_{OUT} = 10 µF

図 10-7. Output Voltage Accuracy vs Load Current Auto PFM and PWM MODE



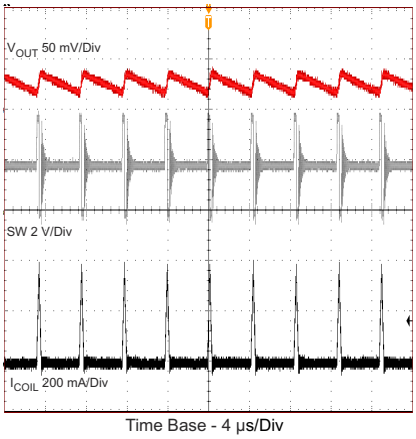
L = 1 µH　　V_{OUT} = 1.8 V　　C_{OUT} = 10 µF

図 10-8. Output Voltage Accuracy vs Load Current Forced PWM MODE



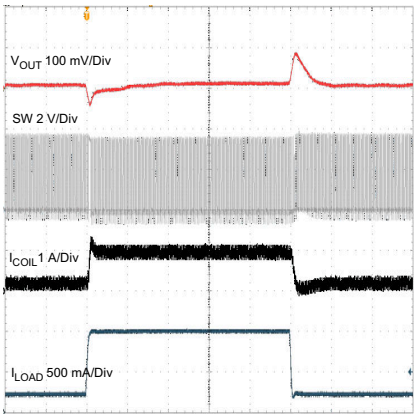
V_{IN} = 3.6 V　　V_{OUT} = 1.8 V　　MODE = GND
C_{OUT} = 10 µF　　L = 1.2 µH　　I_{OUT} = 500 mA

図 10-9. Typical Operation (PWM Mode)



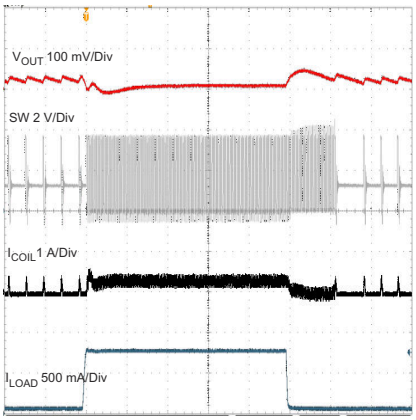
V_{IN} = 3.6 V　　V_{OUT} = 1.8 V　　MODE = GND
C_{OUT} = 10 µF　　L = 1.2 µH　　I_{OUT} = 20 mA

図 10-10. Typical Operation (PFM Mode)



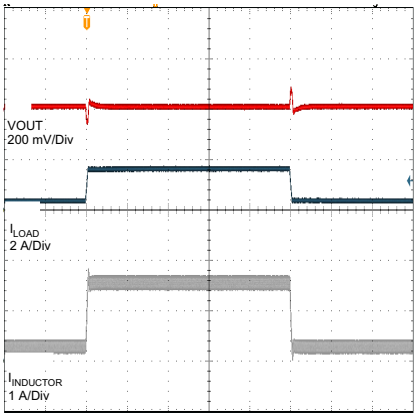
V_{IN} = 3.6 V V_{OUT} = 1.2 V I_{OUT} = 0.2 to 1 A

図 10-11. Load Transient Response, MODE = V_{IN} PWM Mode 0.2 A to 1 A



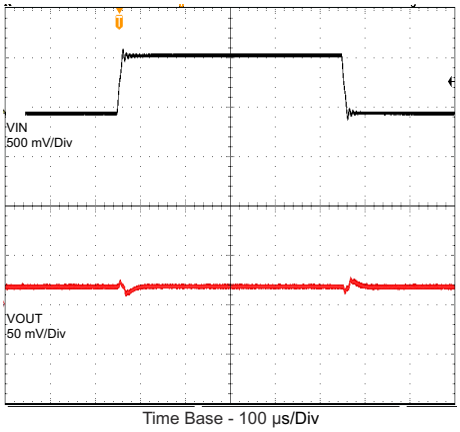
V_{IN} = 3.6 V V_{OUT} = 1.8 V I_{OUT} = 20 to 750 mA

図 10-12. Load Transient PFM Mode 20 mA to 750 mA



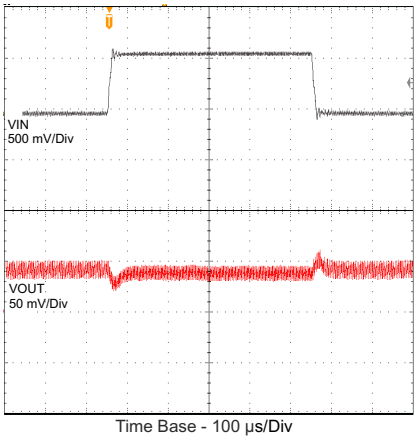
V_{IN} = 3.6 V V_{OUT} = 1.8 V L = 1.2 µH
C_{OUT} = 10 µF

図 10-13. Load Transient Response 200 mA To 1500 mA



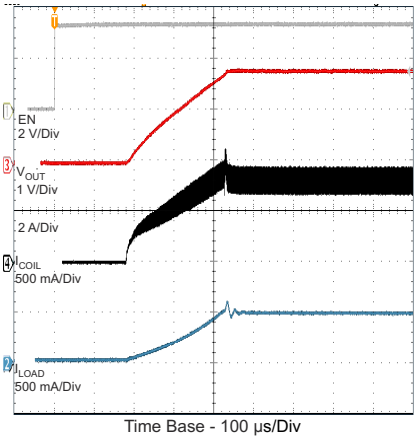
V_{IN} = 3.6 to 4.2 V V_{OUT} = 1.8 V I_{OUT} = 500 mA
C_{OUT} = 10 µF L = 1.2 µH

図 10-14. Line Transient Response PWM Mode



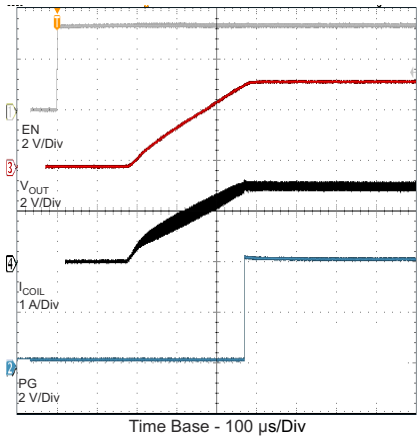
V_{IN} = 3.6 to 4.2 V V_{OUT} = 1.8 V I_{OUT} = 50 mA
C_{OUT} = 10 µF L = 1.2 µH

図 10-15. Line Transient PFM Mode



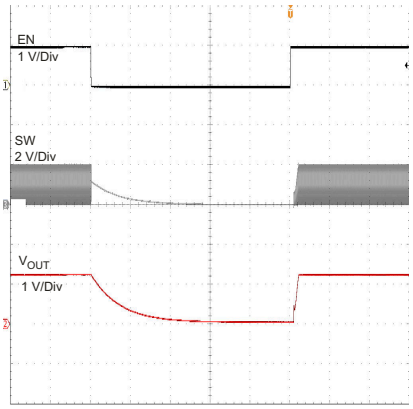
V_{IN} = 3.6 V V_{OUT} = 1.8 V Load = 2R2
C_{OUT} = 10 µF L = 1.2 µH

図 10-16. Start-Up Into Load



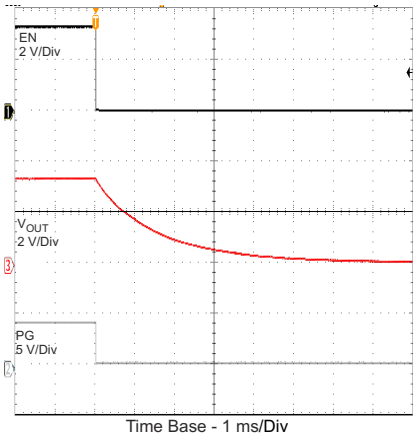
V_{IN} = 4.2 V V_{OUT} = 3.3 V Load = 2R2
PG Pullup resistor 10 kΩ

図 10-17. Start-Up TPS62067-Q1 into 2.2-Ω Load With Power Good



V_{IN} = 3.6 V V_{OUT} = 1.8 V No load
C_{OUT} = 1.8 µF

図 10-18. Output Discharge



V_{IN} = 4.2 V V_{OUT} = 3.3 V No load
PG pullup resistor, 10 kΩ

図 10-19. Shutdown TPS62067-Q1

10.3 Power Supply Recommendations

The power supply to the devices must have a current rating according to the supply voltage, output voltage, and output current.

10.4 Layout

10.4.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. The input capacitor must be placed as close as possible to the IC pins.

Provide a low inductance, impedance ground, and supply path. Therefore, use wide and short traces for the main current paths. Connect the AGND and PGND pins of the device to the thermal pad land of the PCB and use this pad as a star point. Use a common power PGND node and a different node for the signal AGND to minimize the effects of ground noise. The FB divider network must be connected right to the output capacitor and the FB line must be routed away from noisy components and traces (for example, SW line).

Due to the small package of this converter and the overall small design size, the thermal performance of the PCB layout is important. To get a good thermal performance, a four or more layer PCB design is recommended.

The PowerPAD of the IC must be soldered on the thermal pad area on the PCB to get a proper thermal connection. For good thermal performance, the exposed pad on the PCB must be connected to an inner GND plane with sufficient via connections. Refer to the documentation of the evaluation kit.

10.4.2 Layout Example

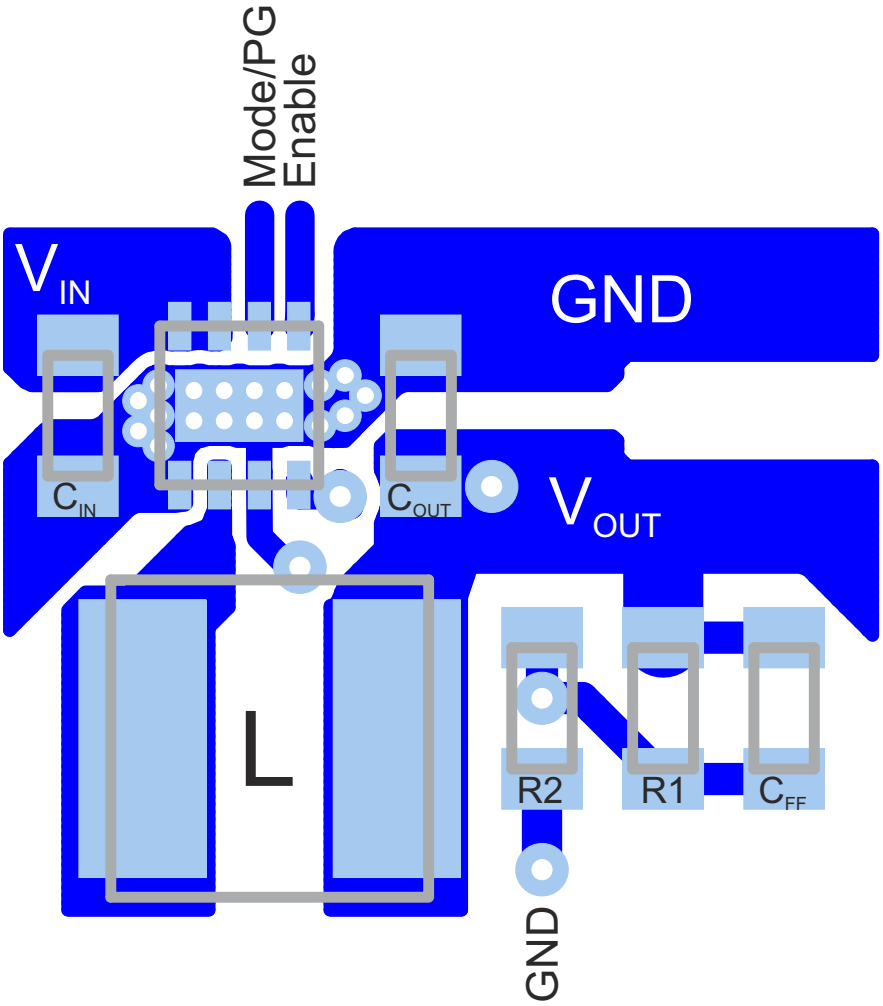


図 10-20. PCB Layout

11 Device and Documentation Support

11.1 Device Support

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11.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62065QDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SJF	Samples
TPS62067AQDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1RF	Samples
TPS62067QDSGRQ1	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS62065-Q1, TPS62067-Q1 :

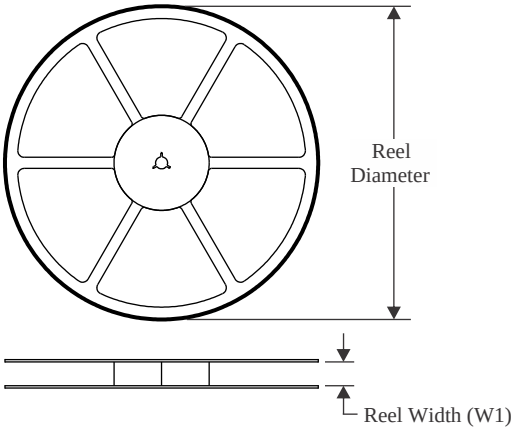
- Catalog : TPS62065, TPS62067

NOTE: Qualified Version Definitions:

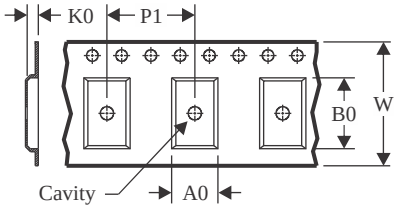
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

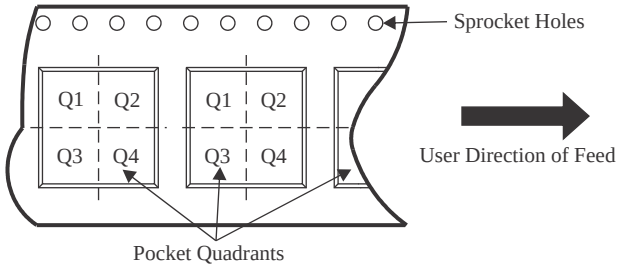


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

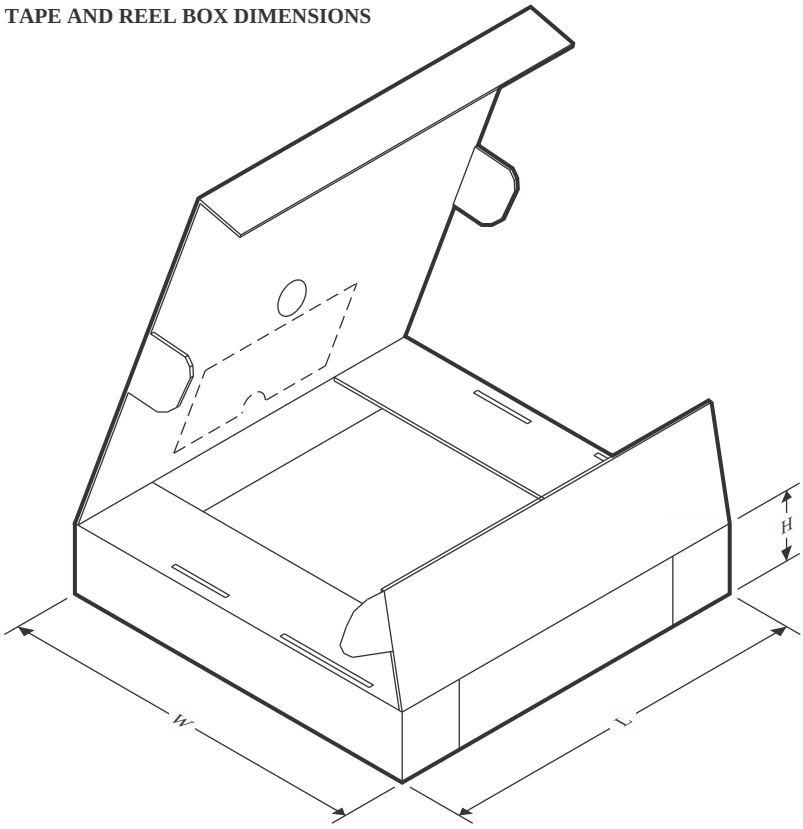
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62065QDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62067AQDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS62067QDSGRQ1	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62065QDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62067AQDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0
TPS62067QDSGRQ1	WSON	DSG	8	3000	210.0	185.0	35.0

GENERIC PACKAGE VIEW

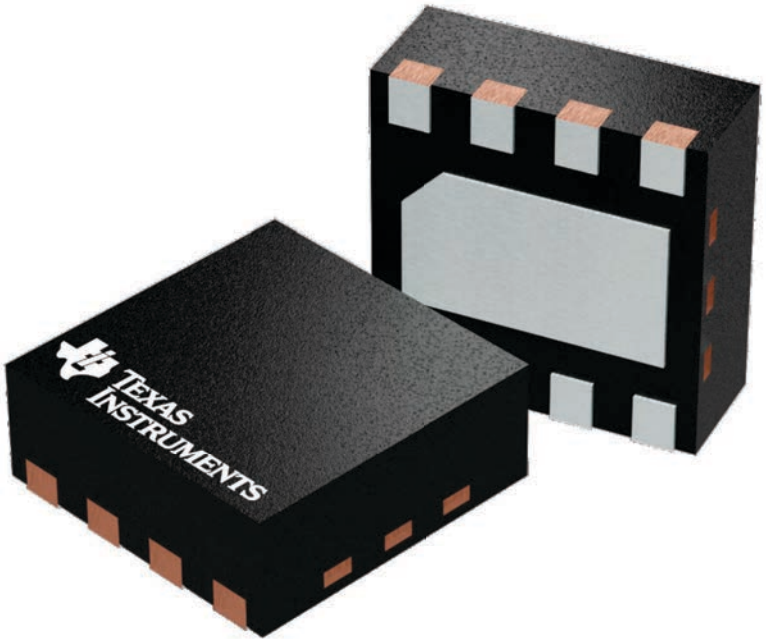
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



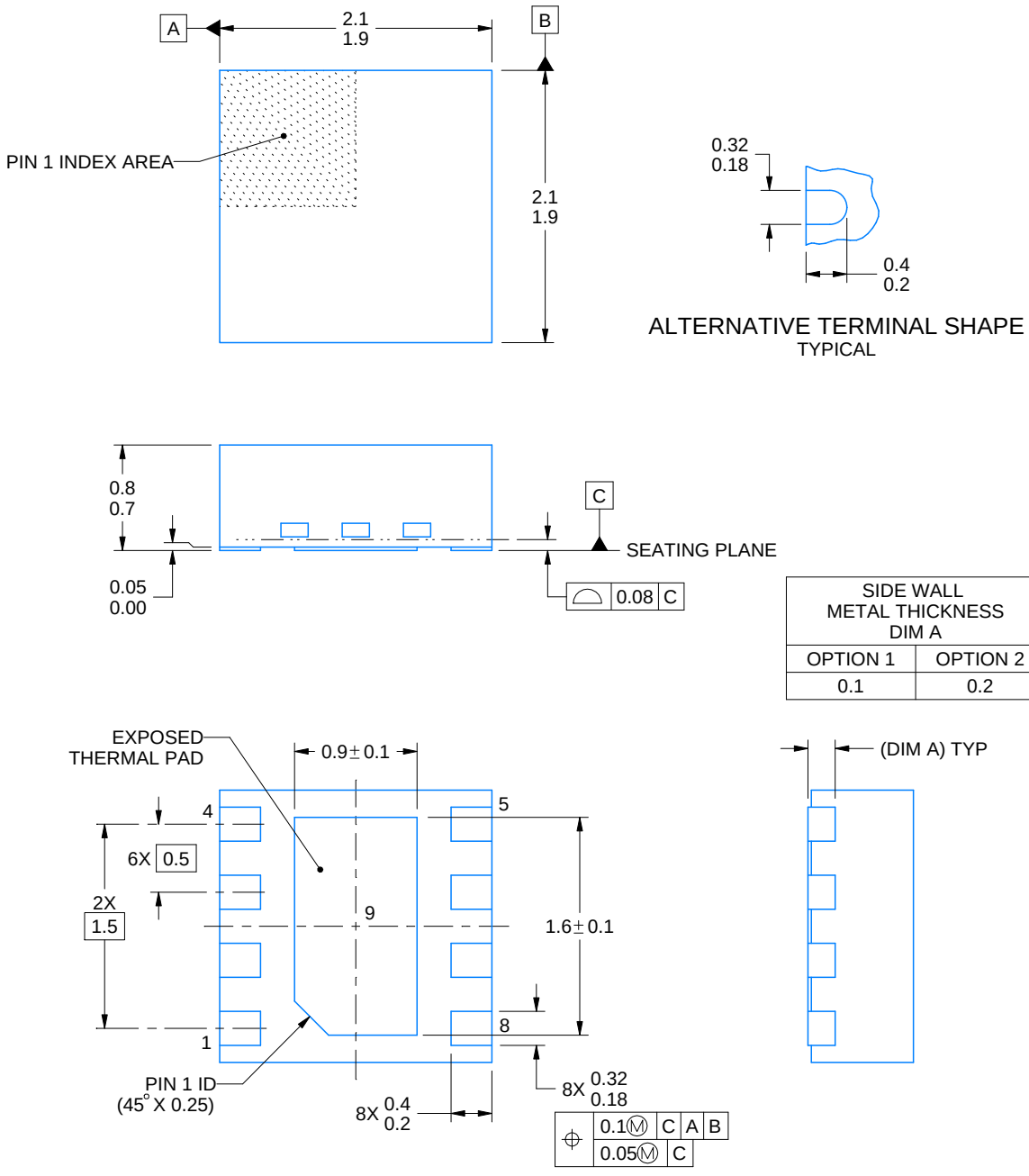
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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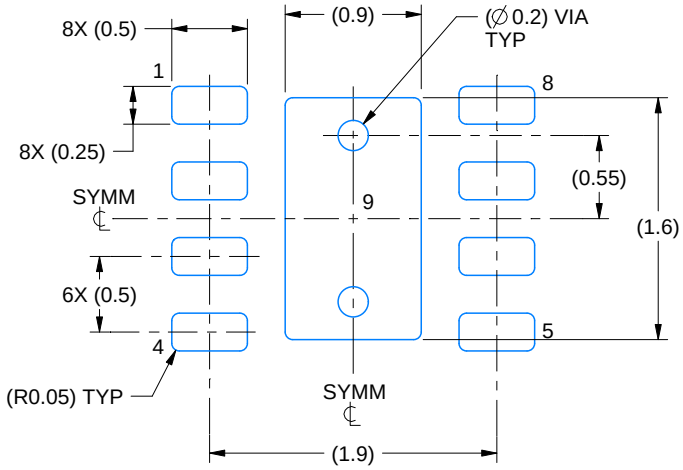
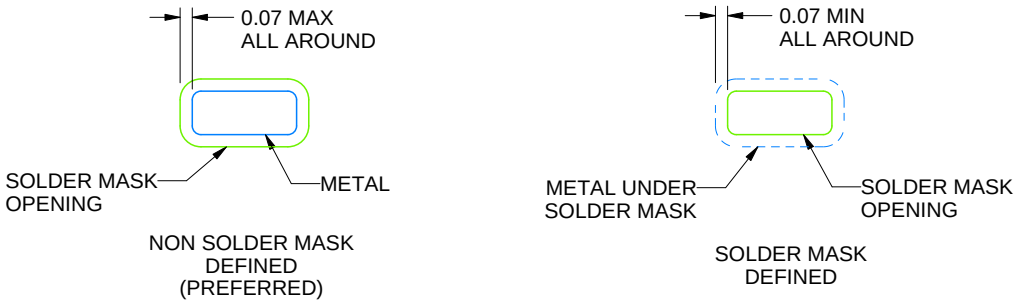
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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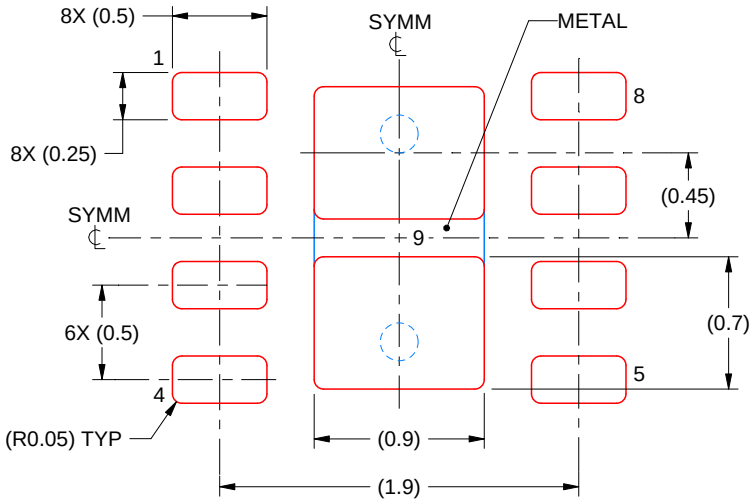
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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