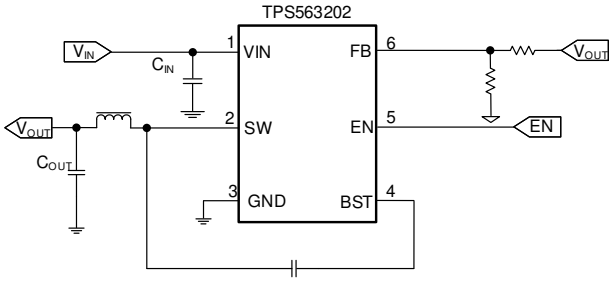
TPS563202 4.3V～17V 入力、3A、同期整流式降圧コンバータ、SOT563 パッケージ

1 特長

- 95mΩ および 57mΩ の FET を内蔵した 3A コンバータ
- D-CAP2™ モード制御による高速過渡応答
- 入力電圧範囲:4.3V～17V
- 出力電圧範囲:0.806V～7V
- 軽負荷時の ECO モード
- 580kHz (標準値) のスイッチング周波数
- 低いシャットダウン電流:3μA 未満
- 帰還電圧精度:2% (25℃)
- プリバイアス機能に対応
- サイクル単位の過電流制限
- ヒカップ・モードによる過電流保護
- 非ラッチ UVP および TSD 保護
- 固定ソフト・スタート:1.2ms

2 アプリケーション

- デジタル・テレビ用電源
- スマート・スピーカ
- 有線ネットワーク
- デジタル・セットトップ・ボックス (STB)
- 監視機器



概略回路図

3 概要

TPS563202 は単純で使いやすい 3A 同期整流式降圧コンバータで、SOT563 パッケージに搭載されています。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が低くなるよう最適化されています。

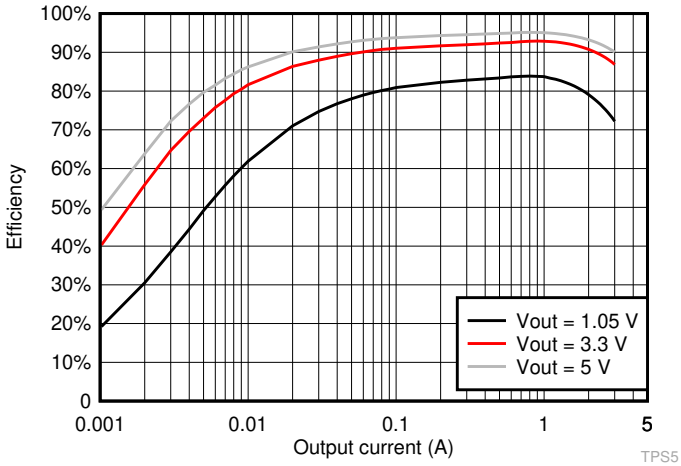
このスイッチ・モード電源 (SMPS) デバイスは、D-CAP2 モード制御を採用し、高速の過渡応答を実現します。また、特殊ポリマーなど ESR (等価直列抵抗) の低い出力コンデンサと、超低 ESR のセラミック・コンデンサの両方を、外部補償部品なしでサポートします。

TPS563202 は ECO モードで動作することで、軽負荷動作中も高い効率を維持できます。TPS563202 は 6 ピン、1.6mm × 1.6mm の SOT563 (DRL) パッケージで供給され、接合部温度 –40℃～125℃で動作が規定されています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS563202	DRL (6)	1.60mm × 1.60mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



TPS563202 の効率

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Changes from Revision * (December 2019) to Revision A (June 2020) **Page**

- マーケティング・ステータスを事前情報から初回リリースに変更.....1

5 Pin Configuration and Functions

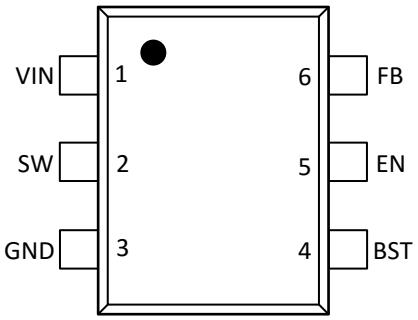


図 5-1. 6-Pin SOT563 DRL Package (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VIN	1	I	Input voltage supply pin.
SW	2	O	Switch node connection between high-side NFET and low-side NFET.
GND	3	—	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive FB to this GND at a single point.
BST	4	O	Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between BST and SW pin.
EN	5	I	Enable input control. Active high and must be pulled up to enable the device.
FB	6	I	Converter feedback input. Connect to output voltage with feedback resistor divider.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	19	V
	BST	–0.3	25	V
	BST (10 ns transient)	–0.3	27	V
	BST (vs SW)	–0.3	6.5	V
	FB	–0.3	6.5	V
	SW	–2	19	V
	SW (10 ns transient)	–3.5	21	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage range		4.3		17	V
V_I	Input voltage range	BST	–0.1		23	V
		BST (10 ns transient)	–0.1		26	
		BST (vs SW)	–0.1		6	
		EN	–0.1		17	
		FB	–0.1		5.5	
		SW	–1.8		17	
		SW (10 ns transient)	–3.5		20	
T_J	Operating junction temperature		–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS563202 DRL 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	137.0	°C/W
$R_{\theta JA\_effective}$	Junction-to-ambient thermal resistance with TI EVM board(2)	65.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W

THERMAL METRIC(1)		TPS563202 DRL 6 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	21.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) This $R_{\theta JA\_effective}$ is tested on TPS563202EVM board(2 layer, Copper thickness is 2 OZ) at V_{IN} = 12V, V_{OUT} =5V I_{OUT} = 3A , TA = 25ºC.

6.5 Electrical Characteristics

T_J = –40°C to 125°C, V_{IN} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{VIN}	Operating – non-switching supply current	V_{IN} current, EN = 5 V, V_{FB} = 1 V		380	520	µA
I_{VINSDN}	Shutdown supply current	V_{IN} current, EN = 0 V		1	3	µA
LOGIC THRESHOLD						
V_{ENH}	EN high-level input voltage	EN		1.35	1.6	V
V_{ENL}	EN low-level input voltage	EN	0.8	1.05		V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V	225	400	900	kΩ
V_{FB} VOLTAGE						
V_{FBTH}	V_{FB} threshold voltage	Eco-mode™ operation		815		mV
	V_{FB} threshold voltage	Continuous mode operation at T_A = 25ºC	790	806	822	mV
I_{FB}	V_{FB} input current	V_{FB} = 1 V		0	±0.1	µA
MOSFET						
$R_{DS(on)h}$	High-side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V		95		mΩ
$R_{DS(on)l}$	Low-side switch resistance	T_A = 25°C		57		mΩ
CURRENT LIMIT						
I_{ocl}	Low side current limit	Inductor valley current set point	3.3	4.4	5.6	A
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(1)	Shutdown temperature		172		°C
		Hysteresis		37		
ON-TIME TIMER CONTROL						
$t_{OFF(MIN)}$	Minimum off time	V_{FB} = 0.5 V		220	310	ns
SOFT START						
Tss	Soft-start time	Internal soft-start time, test V_{OUT} from 10% to 90%		1.2		ms
FREQUENCY						
F_{sw}	Switching frequency	V_O = 1.05 V, continue current conditions.		580		kHz
OUTPUT UNDERVOLTAGE						
V_{UVP}	Output UVP threshold	Hiccup detect (H > L)		65%		
T_{HICCUP_WAIT}	Hiccup on time			2.2		ms
T_{HICCUP_RE}	Hiccup time before restart			18.3		ms
UVLO						
UVLO	UVLO threshold	Wake up VIN voltage		4.0	4.3	V
		Shutdown VIN voltage	3.3	3.6		
		Hysteresis VIN voltage		0.4		

(1) Not production tested.

6.6 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

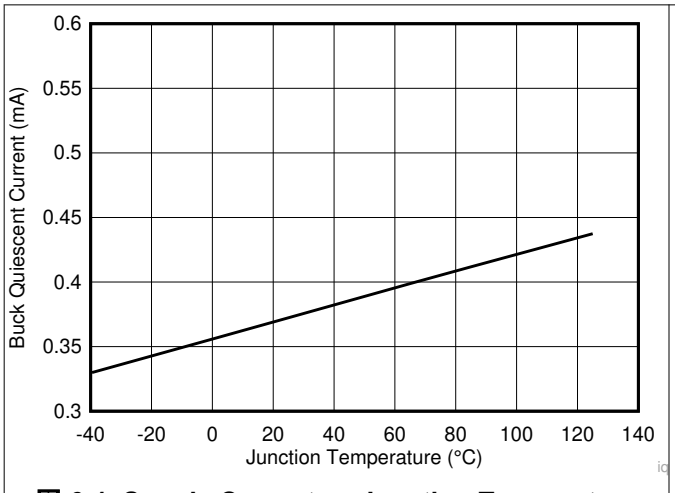


図 6-1. Supply Current vs Junction Temperature

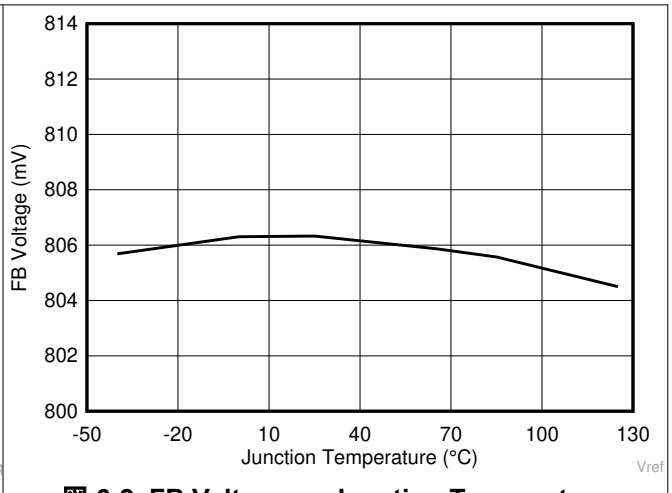


図 6-2. FB Voltage vs Junction Temperature

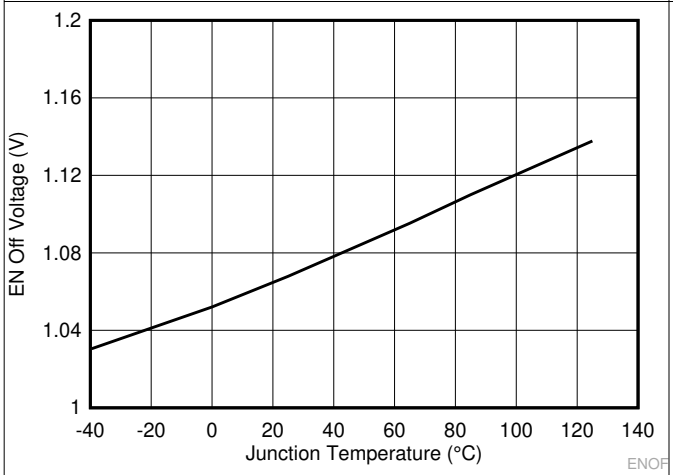


図 6-3. EN Pin EN Off Voltage vs Junction Temperature

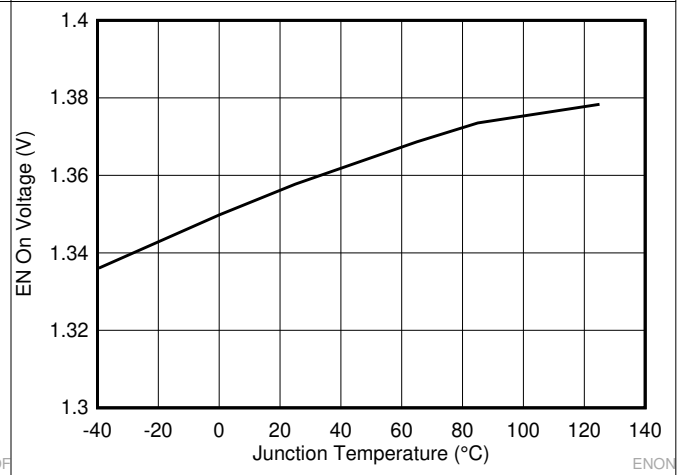


図 6-4. EN Pin EN On Voltage vs Junction Temperature

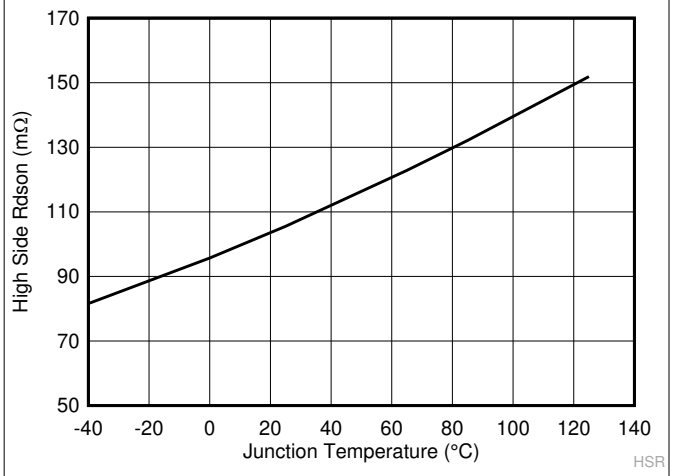


図 6-5. High-Side $R_{ds\text{-}On}$ vs Junction Temperature

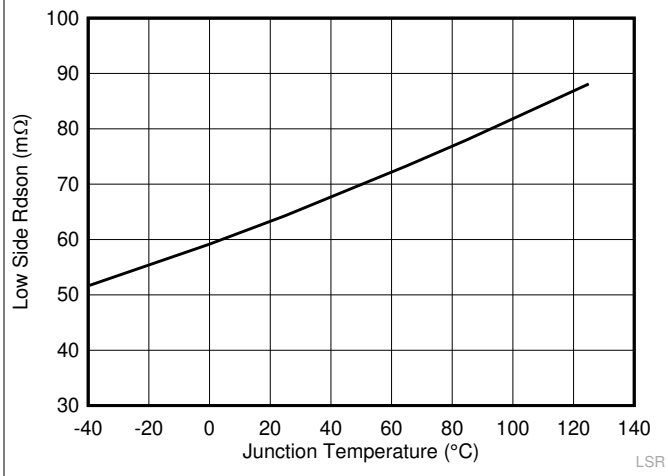


図 6-6. Low-Side $R_{ds\text{-}On}$ vs Junction Temperature

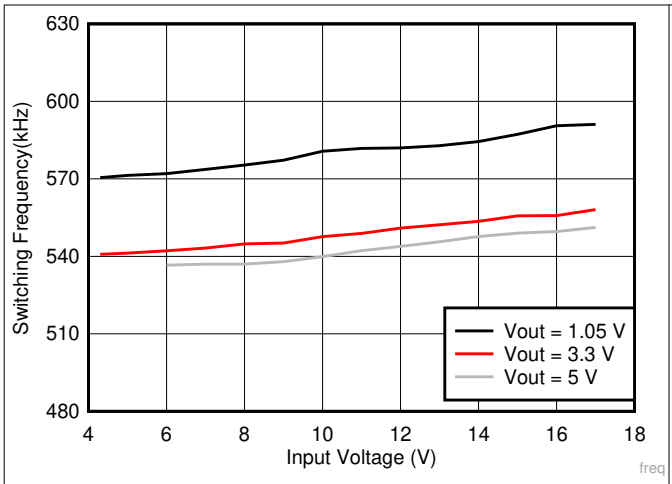


図 6-7. Switching Frequency vs Input Voltage

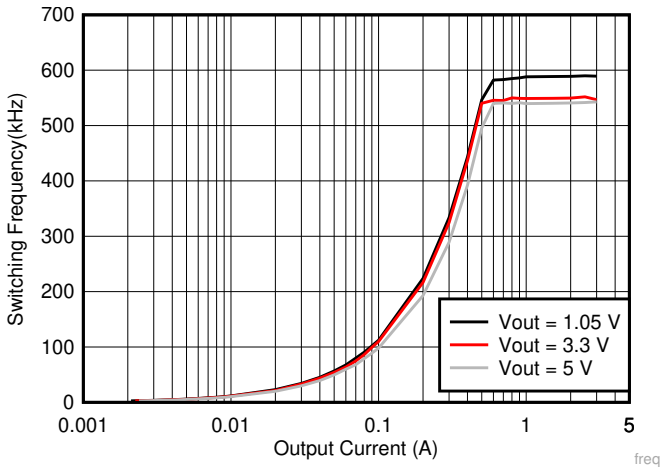


図 6-8. Switching Frequency vs Output Current

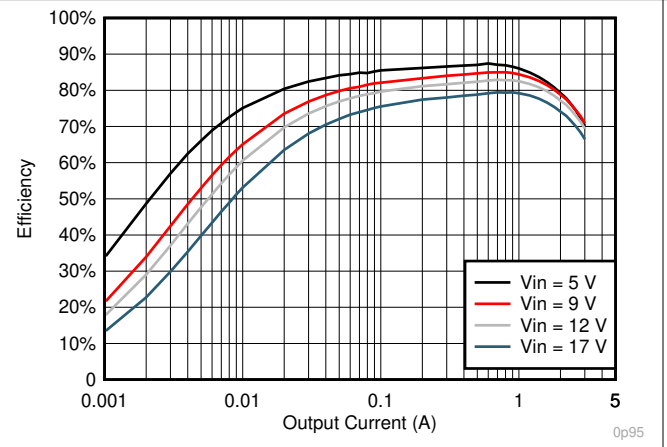


図 6-9. V_{OUT} = 0.95 V Efficiency, L = 1.2 µH

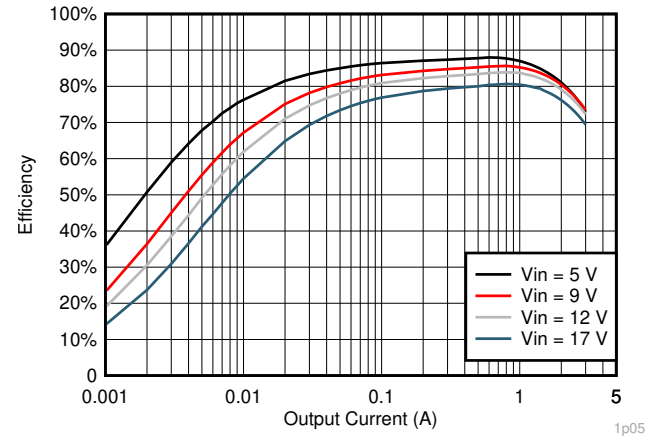


図 6-10. V_{OUT} = 1.05 V Efficiency, L = 1.2 µH

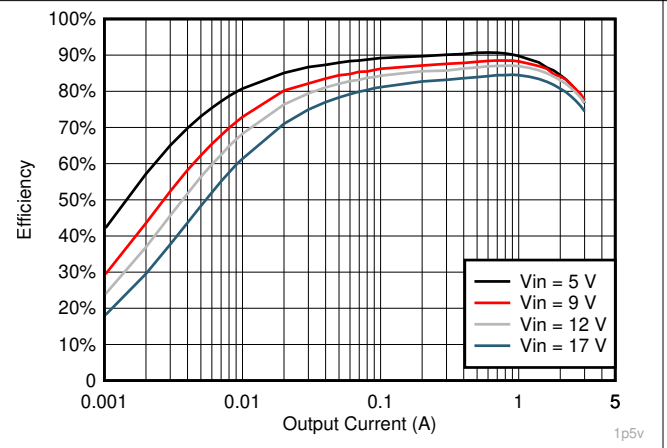


図 6-11. V_{OUT} = 1.5 V Efficiency, L = 1.5 µH

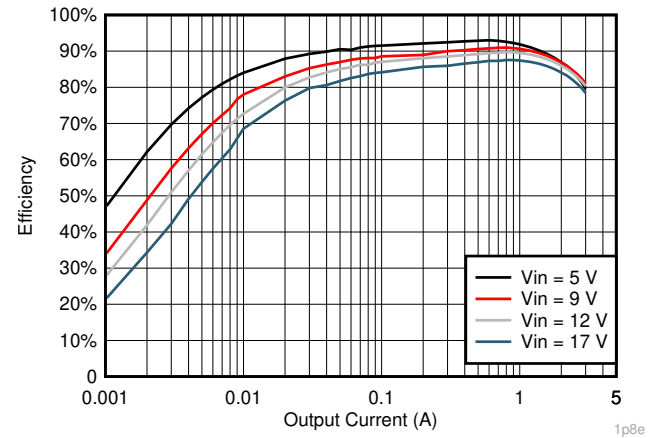


図 6-12. V_{OUT} = 1.8 V Efficiency, L = 2.2 µH

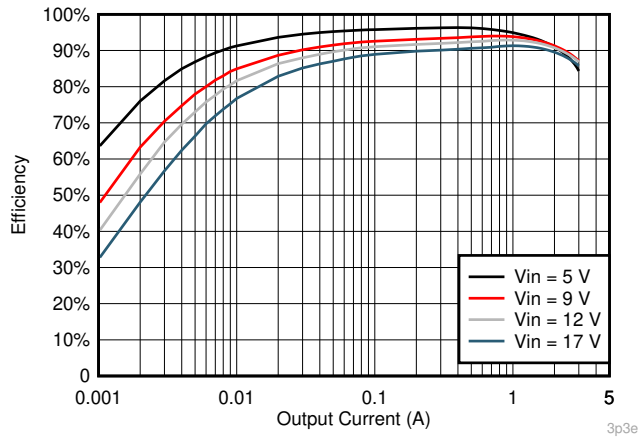


図 6-13. V_{OUT} = 3.3 V Efficiency, L = 3.3µH

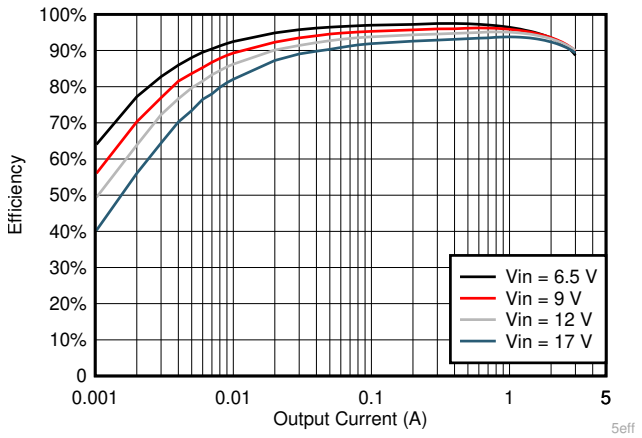


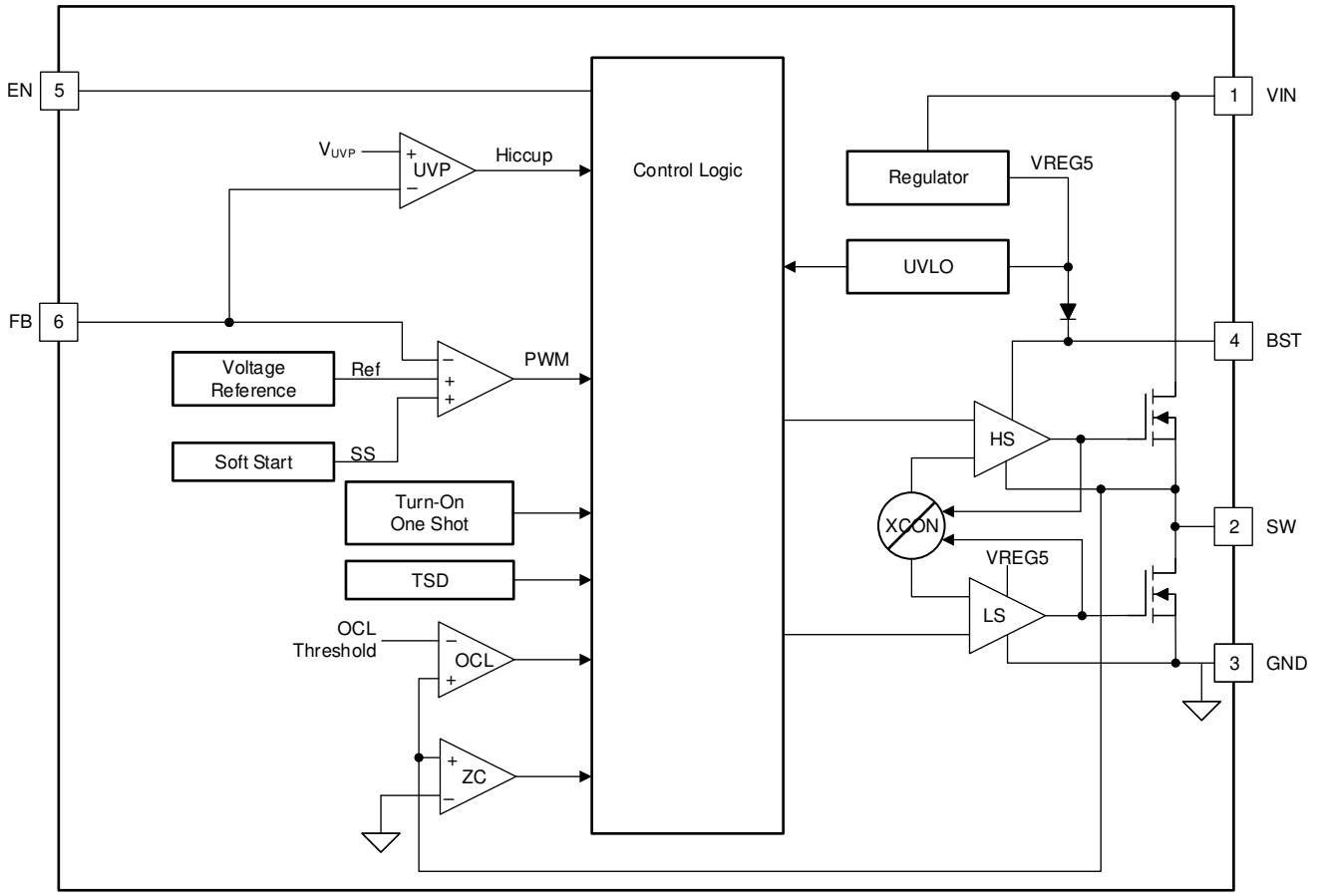
図 6-14. V_{OUT} = 5 V Efficiency, L = 4.7µH

7 Detailed Description

7.1 Overview

TPS563202 is a 3-A synchronous buck converter. The proprietary D-CAP2 mode control supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2 mode control can reduce the output capacitance required to meet a specific level of performance.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adaptive On-Time Control and PWM Operation

The main control loop of the TPS563202 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 mode control. The D-CAP2 mode control combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, VIN, and inversely proportional to the output voltage, V_O, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 mode control.

7.3.2 ECO Mode Control

TPS563202 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in 式 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

7.3.3 Soft Start and Pre-Biased Soft Start

TPS563202 have an internal 1.2-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.4 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{out}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the FB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 24 µs) and re-start after the hiccup time (typically 18 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

7.3.5 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.6 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 172°C), the device is shut off. This is a non-latch protection.

7.4 Device Functional Modes

7.4.1 Normal Operation

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, TPS563202 can operate in their normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, TPS563202 operate at a quasi-fixed frequency of 580 kHz.

7.4.2 Eco-mode Operation

When TPS563202 is in the normal CCM operating mode and the switch current falls to 0 A, TPS563202 begins operating in pulse skipping Eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the FB voltage falls below the Eco-mode threshold voltage. As the output current decreases, the perceived time between switching pulses increases.

7.4.3 Standby Operation

When TPS563202 is operating in either normal CCM or Eco-mode, they may be placed in standby by asserting the EN pin low.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The devices are typical buck DC-DC converters. It typically uses to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for TPS563202. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic in 図 8-1 was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

図 8-1 shows the TPS563202 4.3-V to 17-V input, 1.05-V output converter schematics.

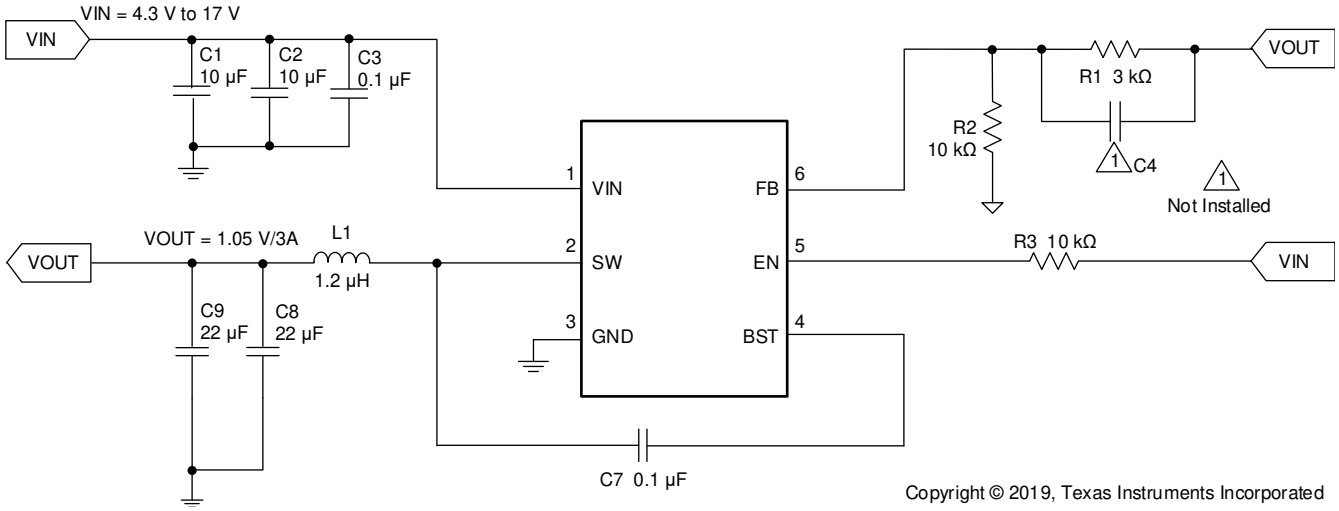


図 8-1. TPS563202 1.05-V/3-A Reference Design

8.2.1 Design Requirements

表 8-1 shows the design parameters for this application.

表 8-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.3 to 17 V
Output voltage	1.05 V
Transient response, 1.5-A load step	ΔVout = ±5%
Input ripple voltage	100 mV
Output ripple voltage	20 mV
Output current rating	3 A
Operating frequency	580 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 式 2 to calculate V_{OUT}.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the FB input current will be more noticeable.

$$V_{out}=0.806 \times (1 + R_{FBT}/R_{FBB}) \quad (2)$$

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 8-2.

表 8-2. Recommended Component Values

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	TYP L1 (uH)	C8 + C9 (µF)			CFF(pF)
				Min	Typ	Max	
0.85	0.55	10.0	1.2	20	44	110	-
0.9	1.2	10.0	1.2	20	44	110	-
1	2.4	10.0	1.2	20	44	110	-
1.05	3	10.0	1.2	20	44	110	-
1.2	4.9	10.0	1.5	20	44	110	-
1.5	8.6	10.0	1.5	20	44	110	-
1.8	12.3	10.0	2.2	20	44	110	-
2.5	21	10.0	2.2	20	44	110	10-220
3.3	31	10.0	3.3	20	44	110	10-220
5	52	10.0	4.7	20	44	110	10-220

表 8-2. Recommended Component Values (continued)

OUTPUT VOLTAGE (V)	R1 (kΩ)	R2 (kΩ)	TYP L1 (uH)	C8 + C9 (µF)			CFF(pF)
				Min	Typ	Max	
6.5	70.5	10.0	4.7	20	44	110	10-220

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 4, 式 5, and 式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$I_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$I_{PEAK} = I_O + \frac{I_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 3.68 A and the calculated RMS current is 3.03 A. The inductor used is a WE 74437349012 with a peak current rating of 18 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563202 are intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use 式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two MuRata GRM21BR61A226ME44L 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS563202 require an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

8.2.3 Application Curves

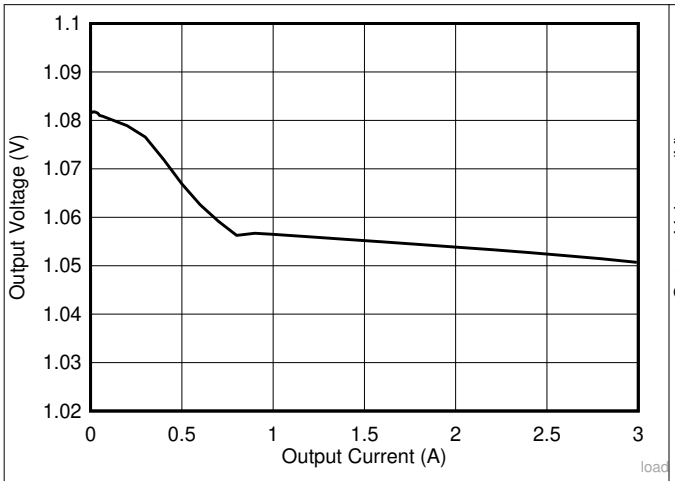


図 8-2. Load Regulation with different loading

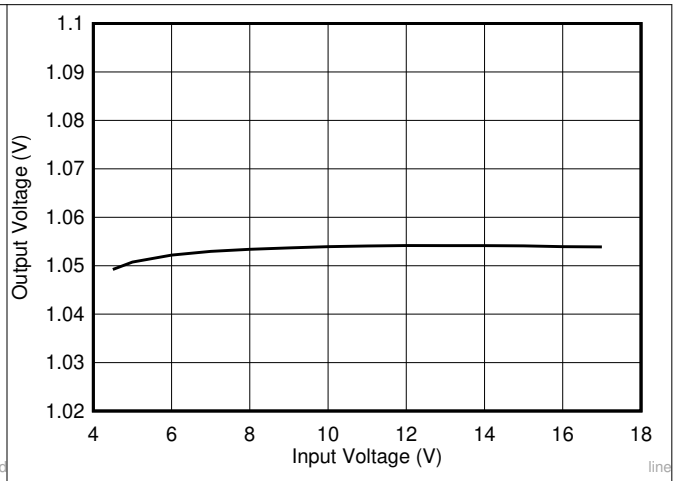


図 8-3. Load Regulation with different input voltage

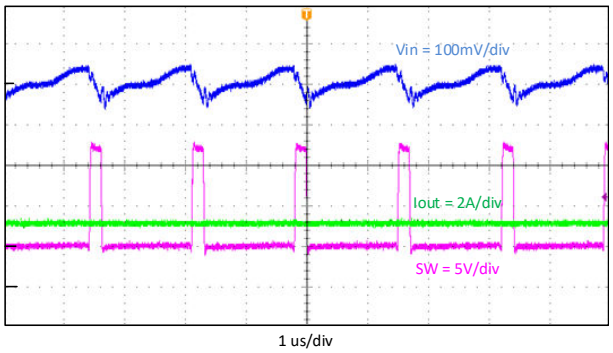


図 8-4. Input Voltage Ripple

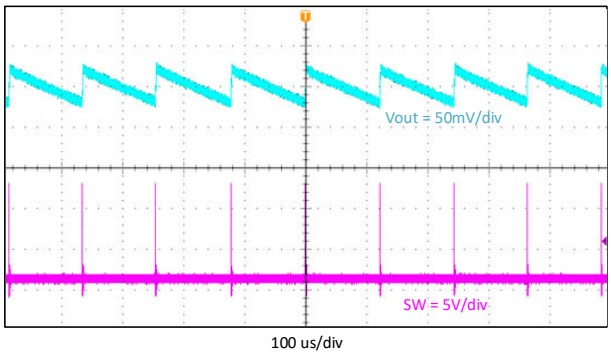


図 8-5. Output Voltage Ripple, 10 mA

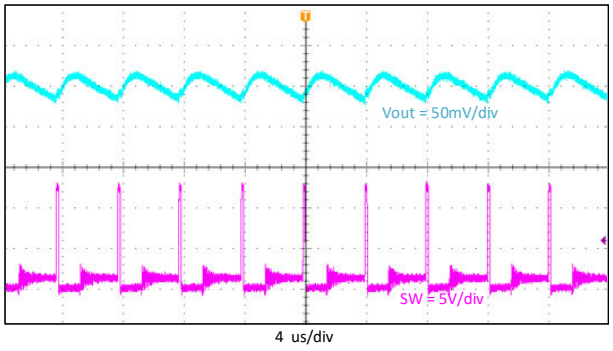


図 8-6. Output Voltage Ripple, I_{out} = 0.3 A

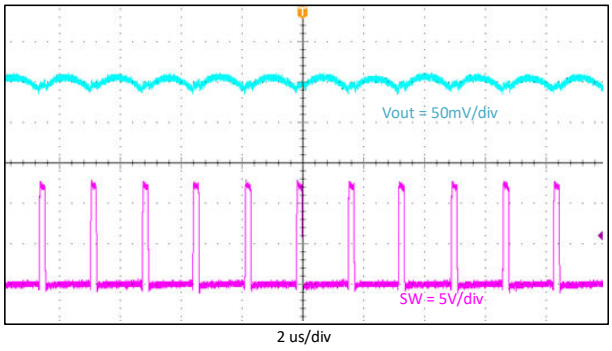


図 8-7. Output Voltage Ripple, I_{out} = 3 A

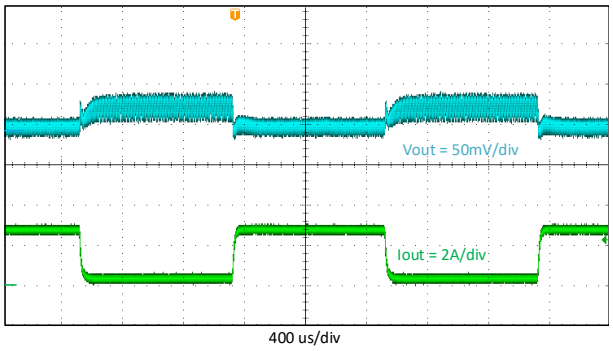


図 8-8. Transient Load Response, 0.3 to 2.7 A

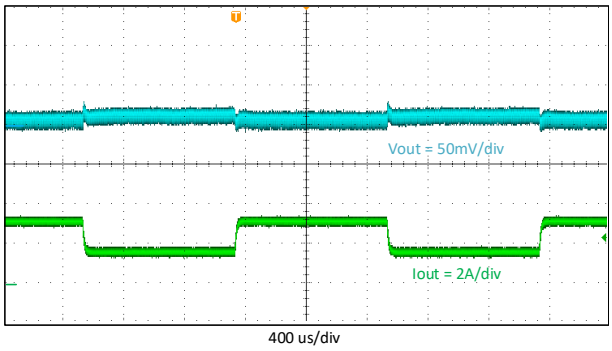


図 8-9. Transient Load Response, 1.5 to 3 A

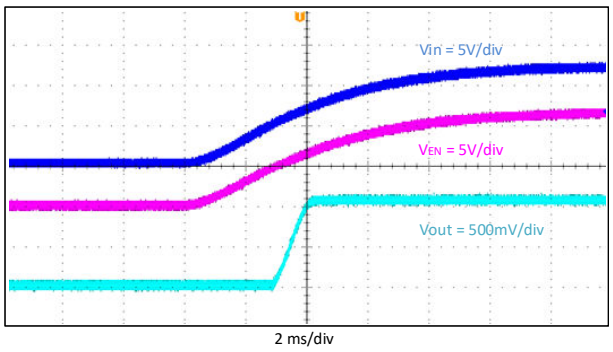


図 8-10. Start Up Relative to V_{IN}

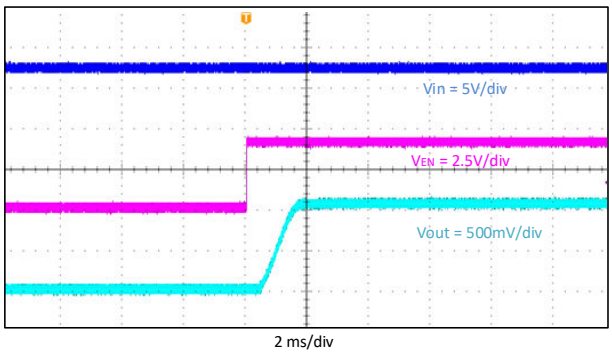


図 8-11. Start-Up Relative to EN

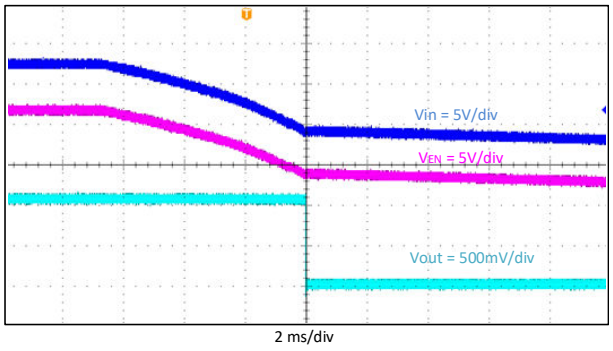


図 8-12. Shutdown Relative to V_{IN}

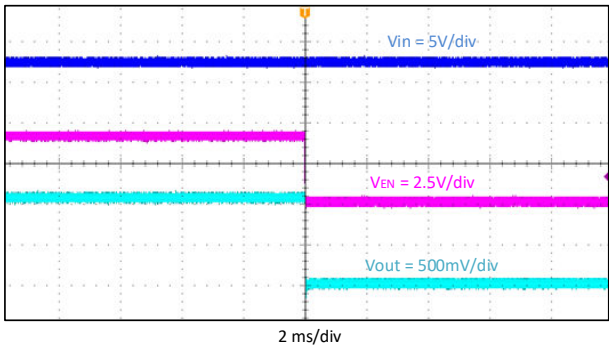


図 8-13. Shutdown Relative to EN

9 Layout

9.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the FB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

9.2 Layout Example

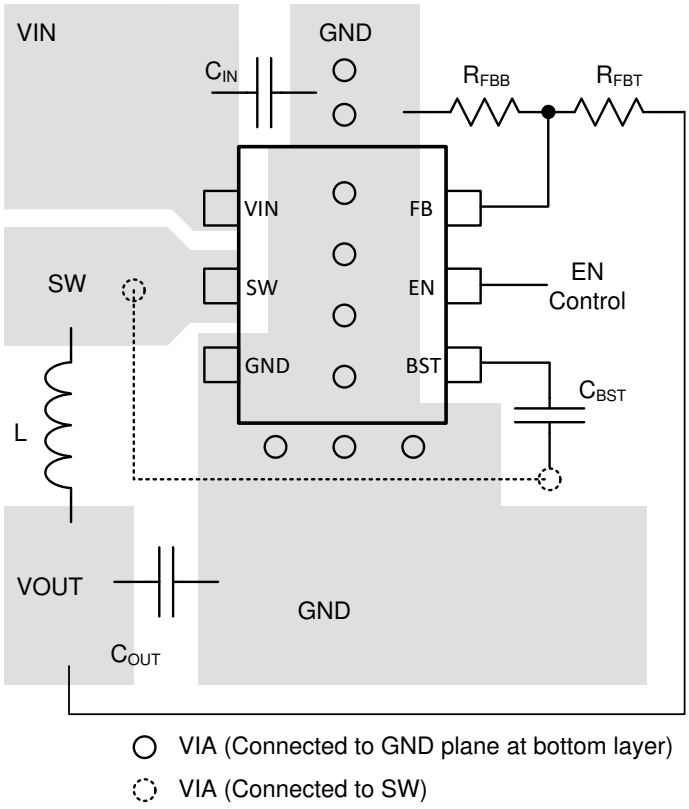


図 9-1. TPS563202 Layout

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS563202DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	3202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

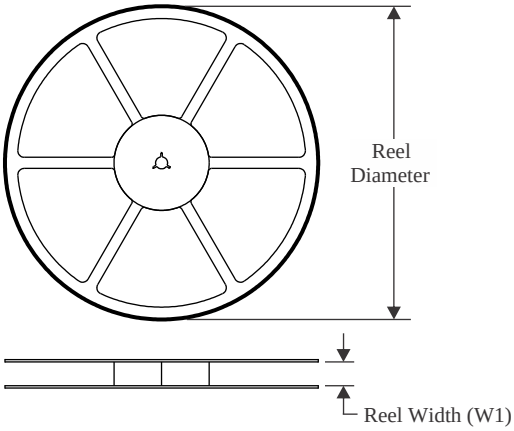
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

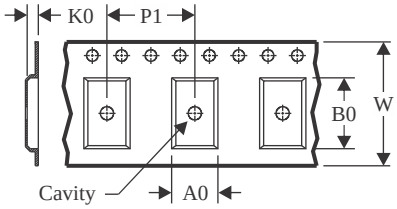
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

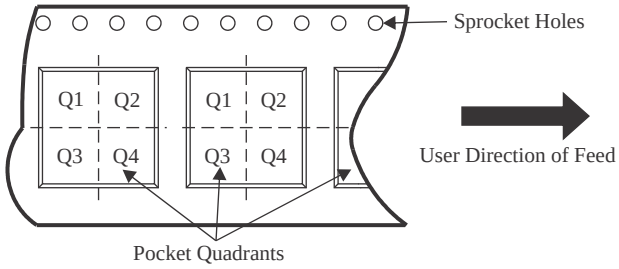


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

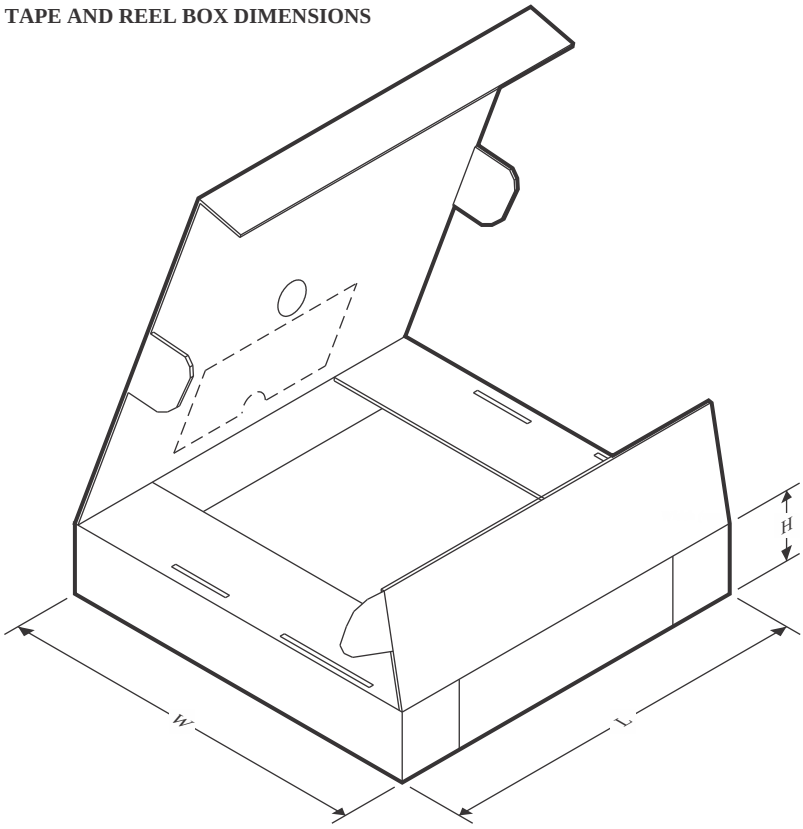
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS563202DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3
TPS563202DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.8	1.8	0.75	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

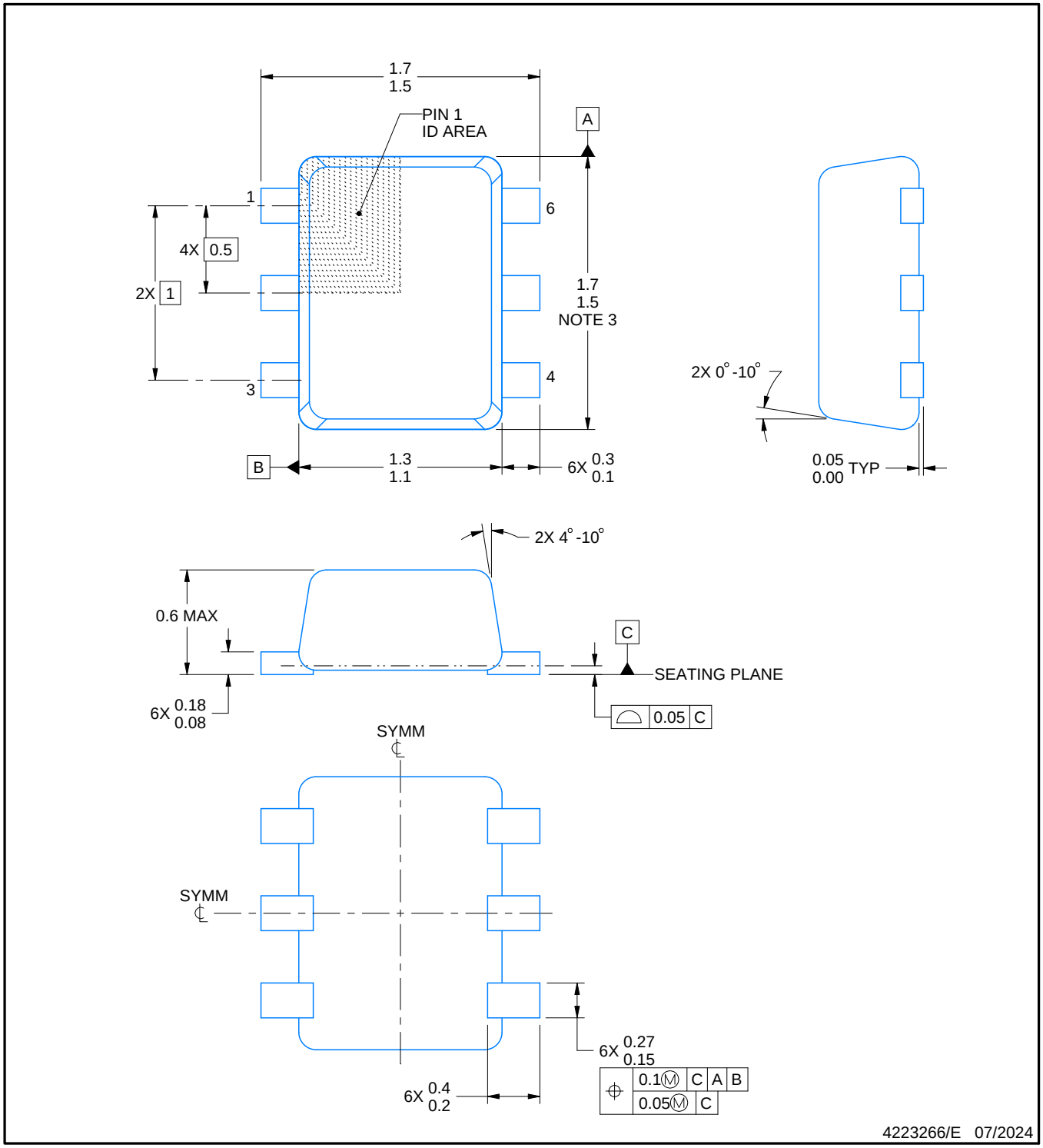
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS563202DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
TPS563202DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



NOTES:

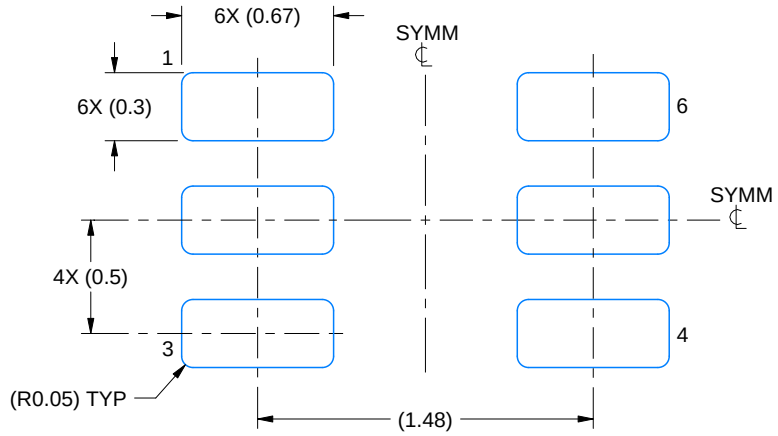
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

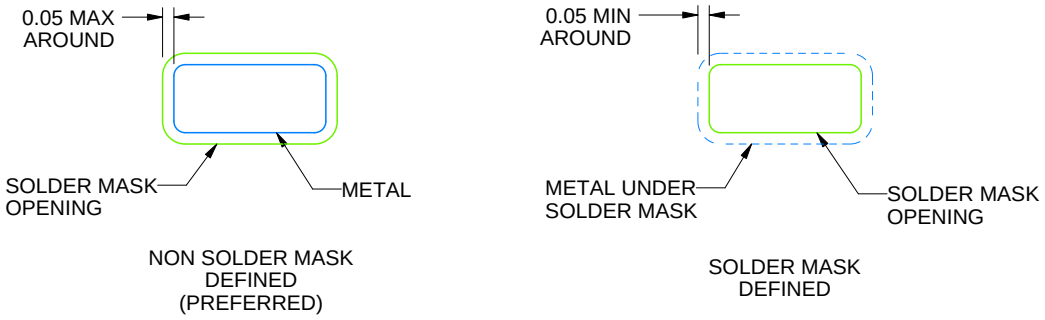
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X

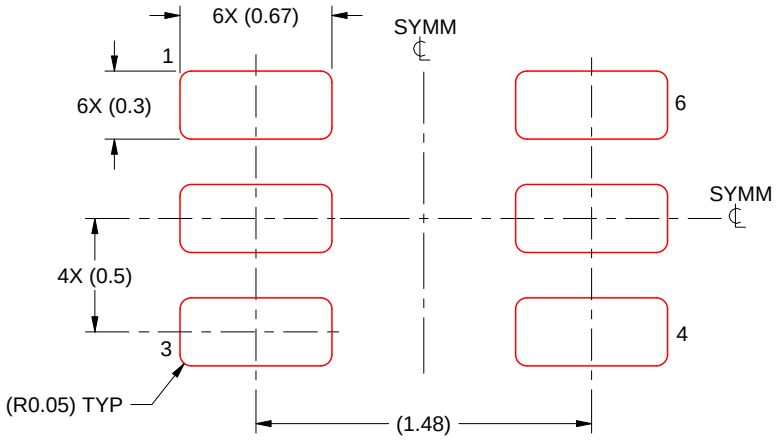


SOLDERMASK DETAILS

4223266/E 07/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/E 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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