TEXAS INSTRUMENTS
TPS563201, TPS563208
JAJSTY5B – DECEMBER 2015 – REVISED SEPTEMBER 2024

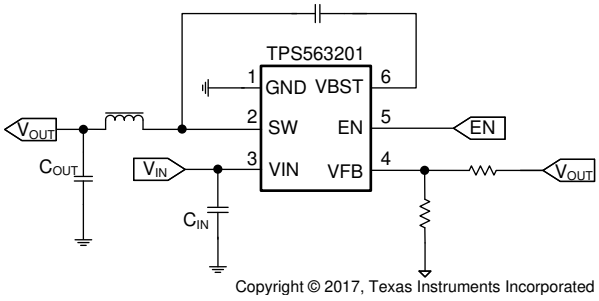
# TPS56320x、4.5V～17V 入力、3A 同期整流降圧電圧レギュレータ、SOT-23 パッケージ

## 1 特長

- TPS563201 および TPS563208 95mΩ および 57mΩ FET 内蔵の 3A コンバータ
- 高速過渡応答の D-CAP2™ 制御方式
- 入力電圧範囲:4.5V～17V
- 出力電圧範囲:0.76V～7V
- パルス スキップ モード (TPS563201) または連続電流モード (TPS563208)
- 580kHz のスイッチング周波数
- 低いシャットダウン電流:20μA 未満
- 帰還電圧精度:2% (25℃)
- プリバイアス出力電圧からのスタートアップ
- サイクル単位の過電流制限
- ヒカップ モードによる過電流保護
- 非ラッチ UVP および TSD 保護
- 固定ソフト スタート:1.0ms
- WEBENCH® Power Designer により、TPS56320x を使用するカスタム設計を作成

## 2 アプリケーション

- デジタル テレビ用電源
- 高精細 Blu-ray™ ディスク プレーヤー
- ネットワーク ホーム ターミナル
- デジタル セットトップ ボックス(STB)
- 監視機器






概略回路図

## 3 概要

TPS563201 および TPS563208 は単純で使いやすい 3A 同期整流降圧コンバータで、SOT-23 パッケージに収容されています。

このデバイスは最小の外付け部品数で動作し、スタンバイ電流が小さくなるよう設計されています。

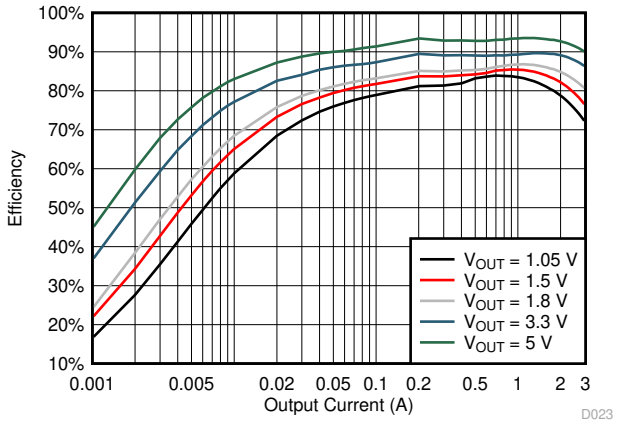
これらのスイッチ モード電源 (SMPS) デバイスは、D-CAP2 制御方式を採用し、高速の過渡応答を実現します。また、特殊ポリマーなど ESR (等価直列抵抗) の低い出力コンデンサと、超低 ESR のセラミック コンデンサの両方を、外部補償部品なしでサポートします。

TPS563201 はパルス スキップ モードで動作し、軽負荷での動作時に高い効率を維持します。TPS563208 は 6 ピン 1.6mm × 2.9mm SOT (DDC) パッケージで供給され、接合部温度 -40℃～125℃で動作が規定されています。

**製品情報**

| 部品番号 | モード | パッケージ (1) | パッケージ サイズ (2) |
|---|---|---|---|
| TPS563201 | ECO | DDC (SOT、6) | 1.6mm × 2.9mm |
| TPS563208 | FCCM | | |

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。




TPS563201 の効率

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# 4 Pin Configuration and Functions

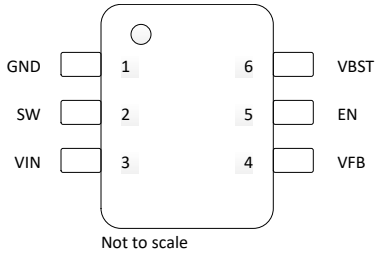



**図 4-1. DDC Package 6-Pin SOT Top View**

**表 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| GND | 1 | — | Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point. |
| SW | 2 | O | Switch node connection between high-side NFET and low-side NFET. |
| VIN | 3 | I | Input voltage supply pin. The drain terminal of high-side power NFET. |
| VFB | 4 | I | Converter feedback input. Connect to output voltage with feedback resistor divider. |
| EN | 5 | I | Enable input control. Active high and must be pulled up to enable the device. |
| VBST | 6 | O | Supply input for the high-side NFET gate drive circuit. Connect 0.1 µF capacitor between VBST and SW pins. |

(1) I = input, O = output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | VIN, EN | –0.3 | 19 | V |
| | VBST | –0.3 | 25 | V |
| | VBST (10 ns transient) | –0.3 | 27 | V |
| | VBST (vs SW) | –0.3 | 6 | V |
| | VFB | –0.3 | 6 | V |
| | SW | –2 | 19 | V |
| | SW (10 ns transient) | –3.5 | 21 | V |
| Operating junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage range | | 4.5 | | 17 | V |
| $V_I$ | Input voltage range | VBST | –0.1 | | 23 | V |
| | | VBST (10 ns transient) | –0.1 | | 26 | |
| | | VBST (vs SW) | –0.1 | | 5.5 | |
| | | EN | –0.1 | | 17 | |
| | | VFB | –0.1 | | 5.5 | |
| | | SW | –1.8 | | 17 | |
| | | SW (10 ns transient) | –3.5 | | 20 | |
| $T_J$ | Operating junction temperature | | –40 | | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC[1] | | TPS56320x DDC (SOT) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 92.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 48.5 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 15.5 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 15.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

## 5.5 Electrical Characteristics

$T_J$ = –40°C to 125°C, $V_{IN}$ = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | | |
| $I_{VIN}$ | Operating – non-switching supply current | $V_{IN}$ current, EN = 5 V, $V_{FB}$ = 0.9 V | TPS563201 | | 120 | 200 | µA |
| | | | TPS563208 | | 350 | 500 | |
| $I_{VINSDN}$ | Shutdown supply current | $V_{IN}$ current, EN = 0 V | | | 8 | 20 | µA |
| **LOGIC THRESHOLD** | | | | | | | |
| $V_{ENH}$ | EN high-level input voltage | | | 1.6 | | | V |
| $V_{ENL}$ | EN low-level input voltage | | | | | 0.8 | V |
| $R_{EN}$ | EN pin resistance to GND | $V_{EN}$ = 1.5 V | | 600 | 1500 | 2400 | kΩ |
| $I_{EN}$ | EN pulldown current | $V_{EN}$ = 1.5 V | | | 1 | | µA |
| **$V_{FB}$ VOLTAGE AND DISCHARGE RESISTANCE** | | | | | | | |
| $V_{FBTH}$ | $V_{FB}$ threshold voltage (1) | $V_O$ = 1.05 V, $I_O$ = 10 mA, Eco-mode operation | | | 774 | | mV |
| | $V_{FB}$ threshold voltage | $V_O$ = 1.05 V, continuous mode operation | | 749 | 768 | 787 | mV |
| $I_{VFB}$ | $V_{FB}$ input current | $V_{FB}$ = 0.8 V | | | 0 | ±0.1 | µA |
| **MOSFET** | | | | | | | |
| $R_{DS(on)h}$ | High-side switch resistance | $T_A$ = 25°C, $V_{BST}$ – SW = 5 V | | | 95 | | mΩ |
| $R_{DS(on)l}$ | Low-side switch resistance | $T_A$ = 25°C | | | 57 | | mΩ |
| **CURRENT LIMIT** | | | | | | | |
| $I_{ocl}$ | Current limit | DC current, $V_{OUT}$ = 1.05 V, $L_1$ = 1.5 µH | | 3.3 | 4.2 | 5.1 | A |
| **THERMAL SHUTDOWN** | | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold (1) | Shutdown temperature | | | 172 | | °C |
| | | Hysteresis | | | 37 | | |
| **ON-TIME TIMER CONTROL** | | | | | | | |
| $t_{OFF(MIN)}$ | Minimum off time | $V_{FB}$ = 0.5 V | | | 220 | 310 | ns |
| **SOFT START** | | | | | | | |
| Tss | Soft-start time | Internal soft-start time | | | 1.0 | | ms |
| **FREQUENCY** | | | | | | | |
| $F_{sw}$ | Switching frequency | $V_{IN}$ = 12 V, $V_O$ = 3.3 V, $I_O$ = 1 A | | | 580 | | kHz |
| **OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION** | | | | | | | |
| $V_{UVP}$ | Output UVP threshold | Hiccup detect (H > L) | | | 65% | | |
| $T_{HICCUP\_WAIT}$ | Hiccup on time | | | | 1.2 | | ms |
| $T_{HICCUP\_RE}$ | Hiccup time before restart | | | | 10 | | ms |
| **UVLO** | | | | | | | |
| UVLO | UVLO threshold | Wake up VIN voltage | | | 3.8 | 4.3 | V |
| | | Shutdown VIN voltage | | 3.3 | 3.4 | | |
| | | Hysteresis VIN voltage | | | 0.4 | | |

(1) Not production tested.

## 5.6 Typical Characteristics

$V_{IN}$ = 12 V (unless otherwise noted)

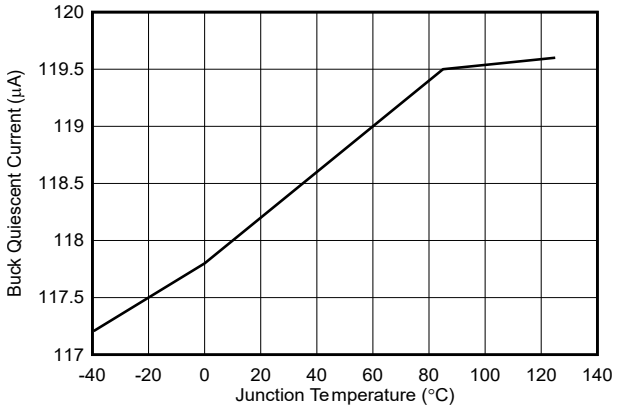



**図 5-1. TPS563201 Supply Current vs Junction Temperature**

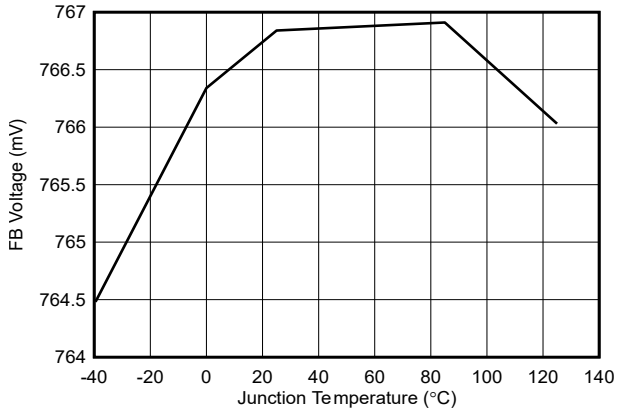



**図 5-2. VFB Voltage vs Junction Temperature**

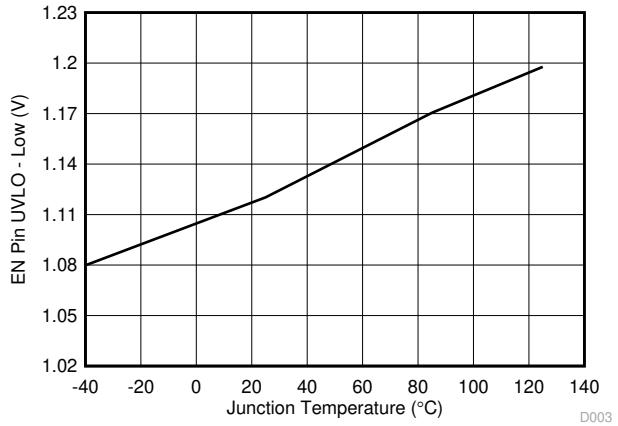



**図 5-3. EN Pin UVLO Low Voltage vs Junction Temperature**

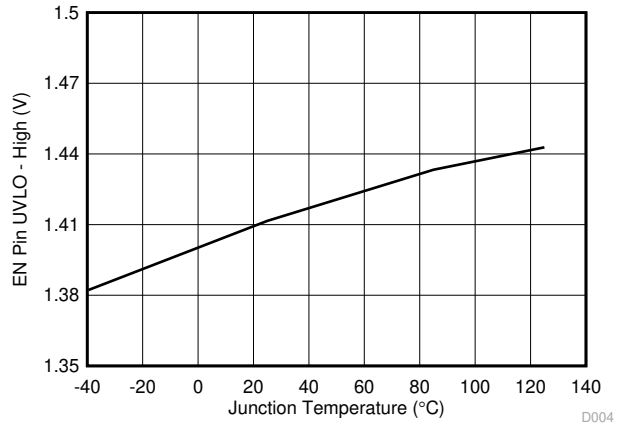



**図 5-4. EN Pin UVLO High Voltage vs Junction Temperature**

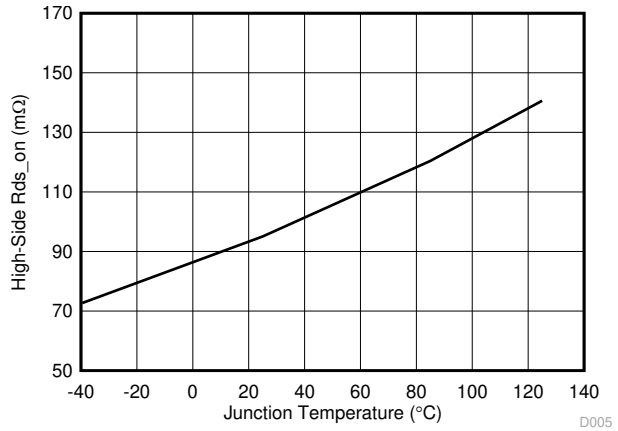



**図 5-5. High-Side $R_{ds-On}$ vs Junction Temperature**

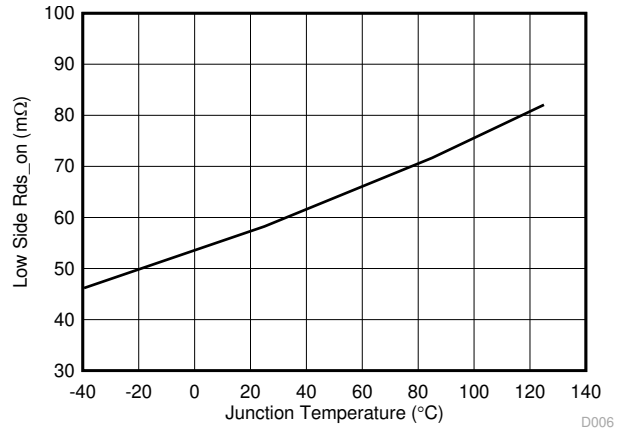



**図 5-6. Low-Side $R_{ds-On}$ vs Junction Temperature**

## 5.6 Typical Characteristics (continued)

$V_{IN}$ = 12 V (unless otherwise noted)

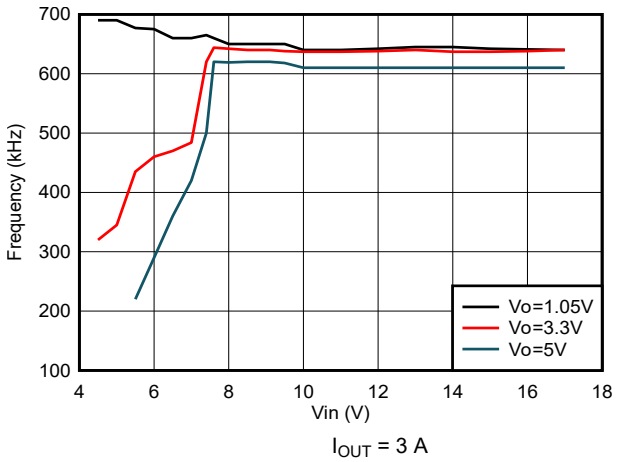



図 5-7. TPS563208 Switching Frequency vs Input Voltage

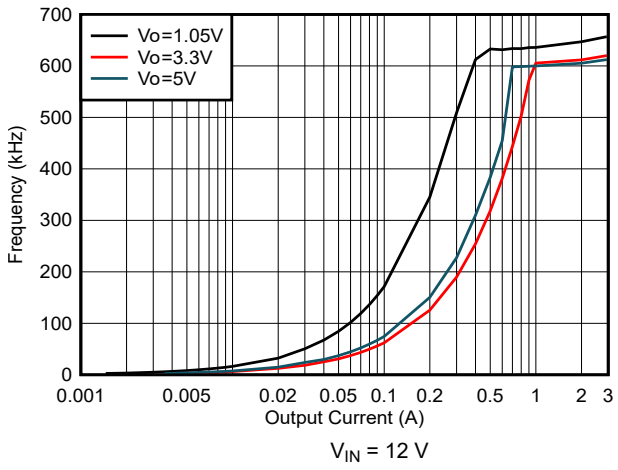



図 5-8. TPS563201 Switching Frequency vs Output Current

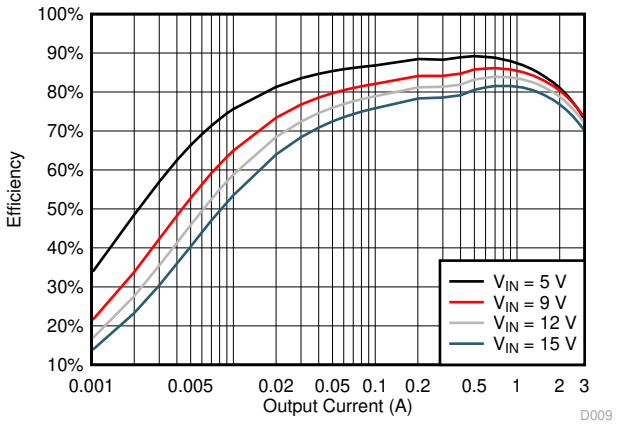



図 5-9. TPS563201 $V_{OUT}$ = 1.05 V Efficiency, L = 2.2 µH

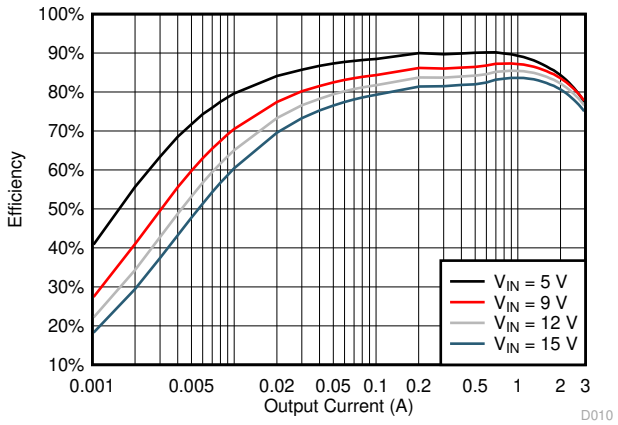



図 5-10. TPS563201 $V_{OUT}$ = 1.5 V Efficiency, L = 2.2 µH

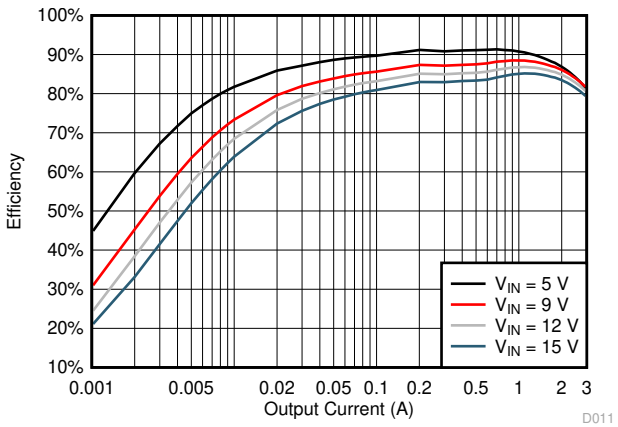



図 5-11. TPS563201 $V_{OUT}$ = 1.8 V Efficiency, L = 2.2 µH

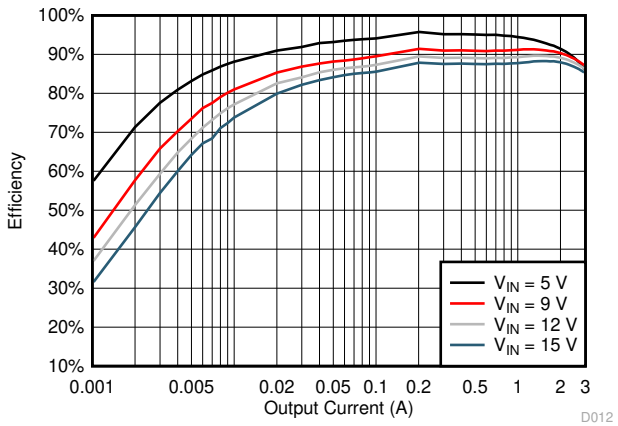



図 5-12. TPS563201 $V_{OUT}$ = 3.3 V Efficiency, L = 2.2 µH

## 5.6 Typical Characteristics (continued)

$V_{IN}$ = 12 V (unless otherwise noted)

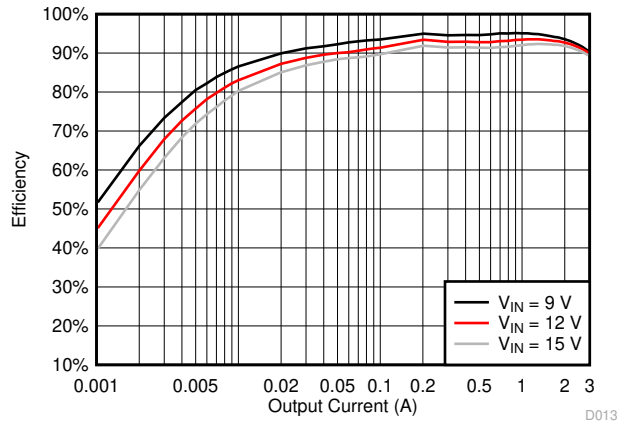



**図 5-13. TPS563201 $V_{OUT}$ = 5 V Efficiency, L = 3.3 µH**

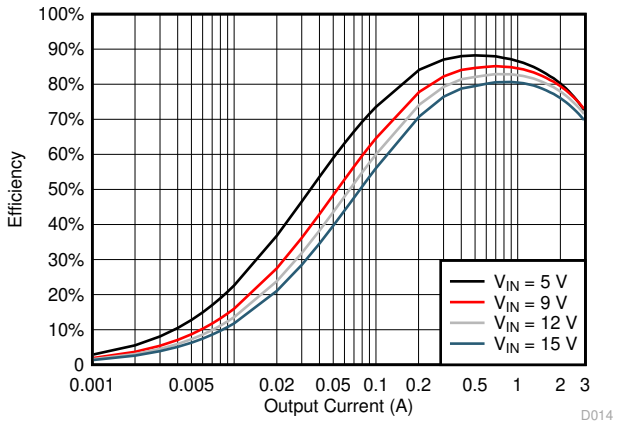



**図 5-14. TPS563208 $V_{OUT}$ = 1.05 V Efficiency, L = 2.2 µH**

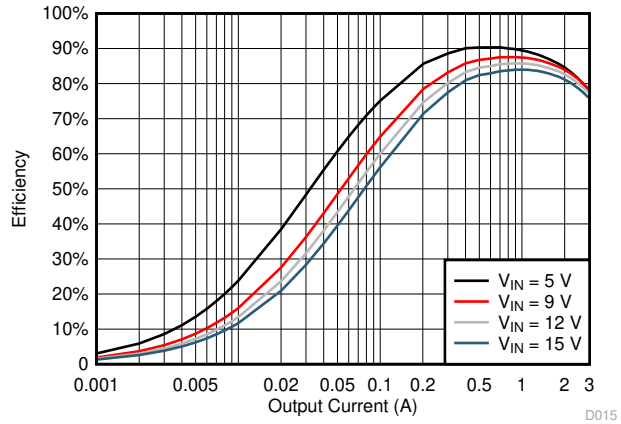



**図 5-15. TPS563208 $V_{OUT}$ = 1.5 V Efficiency, L = 2.2 µH**

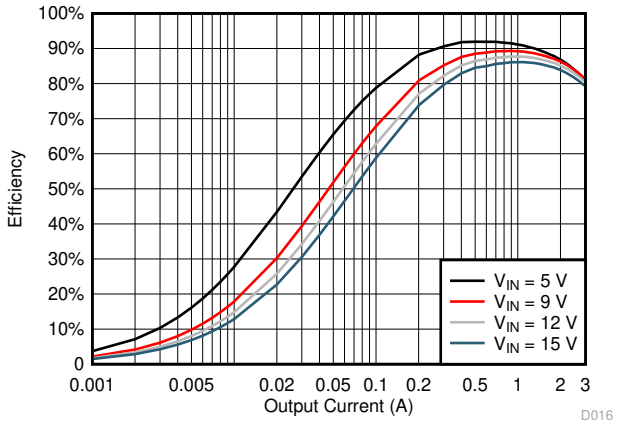



**図 5-16. TPS563208 $V_{OUT}$ = 1.8 V Efficiency, L = 2.2 µH**

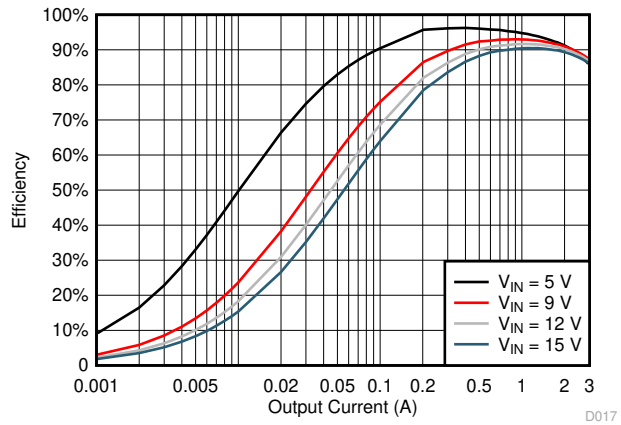



**図 5-17. TPS563208 $V_{OUT}$ = 3.3 V Efficiency, L = 2.2 µH**

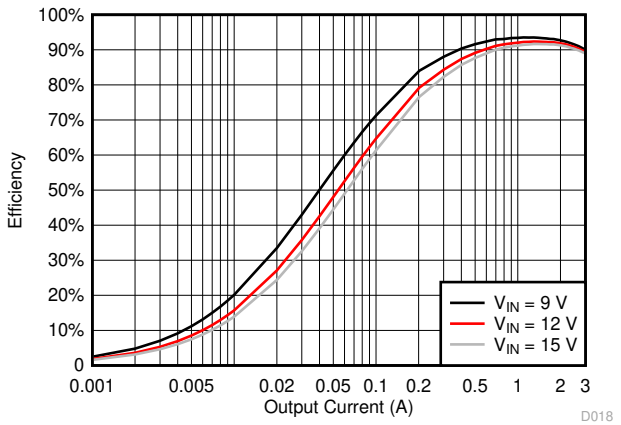


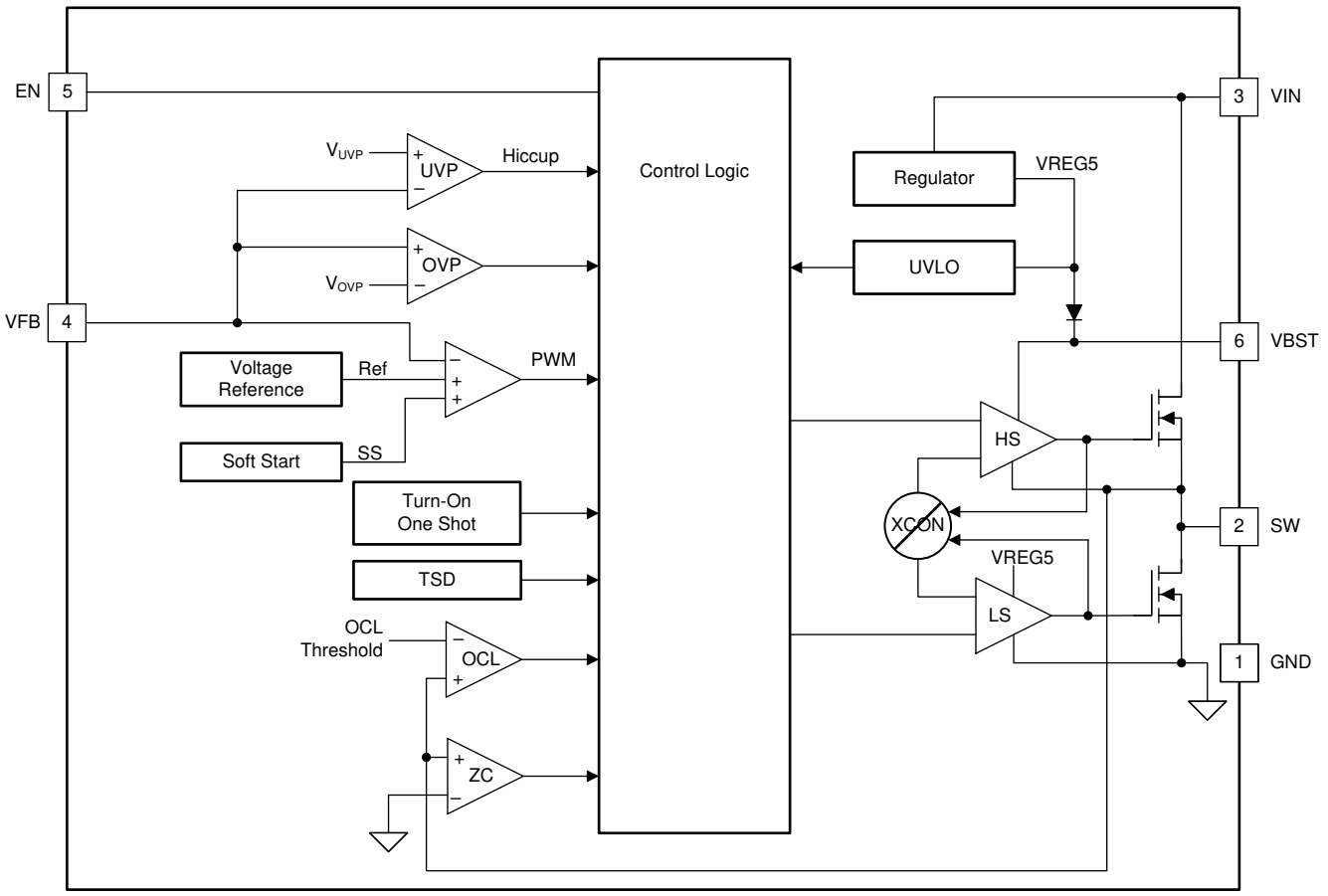

**図 5-18. TPS563208 $V_{OUT}$ = 5 V Efficiency, L = 3.3 µH**

# 6 Detailed Description

## 6.1 Overview

The TPS563201 and TPS563208 are 3-A synchronous step-down converters. The proprietary D-CAP2 control scheme supports low ESR output capacitors such as specialty polymer capacitors and multi-layer ceramic capacitors without complex external compensation circuits. The fast transient response of D-CAP2 control scheme can reduce the output capacitance required to meet a specific level of performance.

## 6.2 Functional Block Diagram






## 6.3 Feature Description

### *6.3.1 Adaptive On-Time Control and PWM Operation*

The main control loop of the TPS563201 and TPS563208 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2 control scheme. The D-CAP2 control scheme combines adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot duration is set proportional to the converter input voltage, VIN, and inversely proportional to the output voltage, $V_O$, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2 control scheme.

### 6.3.2 Pulse Skip Control (TPS563201)

The TPS563201 is designed with advanced Eco-mode to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in 式 1.

$$I_{OUT(LL)} = \frac{1}{2 \times L \times f_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (1)$$

### 6.3.3 Soft Start and Pre-Biased Soft Start

The TPS563201 and TPS563208 have an internal 1-ms soft-start. When the EN pin becomes high, the internal soft-start function begins ramping up the reference voltage to the PWM comparator.

If the output capacitor is pre-biased at startup, the devices initiate switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage $V_{FB}$. This scheme ensures that the converters ramp up smoothly into regulation point.

### 6.3.4 Current Protection

The output over-current limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by Vin, Vout, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current $I_{out}$. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over-current protection. The load current is higher than the over-current threshold by one half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. And then, the device will shut down after the UVP delay time (typically 256 µs) and re-start after the hiccup time (typically 10 ms).

When the over current condition is removed, the output voltage returns to the regulated value.

### 6.3.5 Undervoltage Lockout (UVLO) Protection

UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

### 6.3.6 Thermal Shutdown

The device monitors the temperature of itself. If the temperature exceeds the threshold value (typically 172°C), the device is shut off. This is a non-latch protection.

## 6.4 Device Functional Modes

### *6.4.1 Normal Operation*

When the input voltage is above the UVLO threshold and the EN voltage is above the enable threshold, the TPS563201 and TPS563208 can operate in the normal switching modes. The TPS563201 and TPS563208 operate at a quasi-fixed frequency of about 580kHz under CCM mode when $T_{ON}$ extension is not triggered. When input voltage $V_{IN}$ < 7V and $V_{FB}$ is lower than internal reference voltage, the switching frequency is allowed to smoothly drop to make $T_{ON}$ extended to keep output voltage and improve the load transient performance. The minimum switching frequency is limited to about 200kHz.

### *6.4.2 Eco-mode Operation*

When the TPS563201 and TPS563208 are in the normal CCM operating mode and the switch current falls to 0 A, the TPS563201 begins operating in pulse skipping Eco-mode. Each switching cycle is followed by a period of energy saving sleep time. The sleep time ends when the VFB voltage falls below the Eco-mode threshold voltage. As the output current decreases, the perceived time between switching pulses increases.

### *6.4.3 Standby Operation*

When the TPS563201 and TPS563208 are operating in either normal CCM or Eco-mode, they may be placed in standby by asserting the EN pin low.

# 7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 7.1 Application Information

The devices are typical step-down DC-DC converters. The devices are typically used to convert a higher dc voltage to a lower dc voltage with a maximum available output current of 3 A. The following design procedure can be used to select component values for the TPS563201 and TPS563208. Alternately, the WEBENCH software can be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

## 7.2 Typical Application

The application schematic in 図 7-1 was developed to meet the previous requirements. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

図 7-1 shows the TPS563201 and TPS563208 4.5-V to 17-V input, 1.05-V output converter schematics.

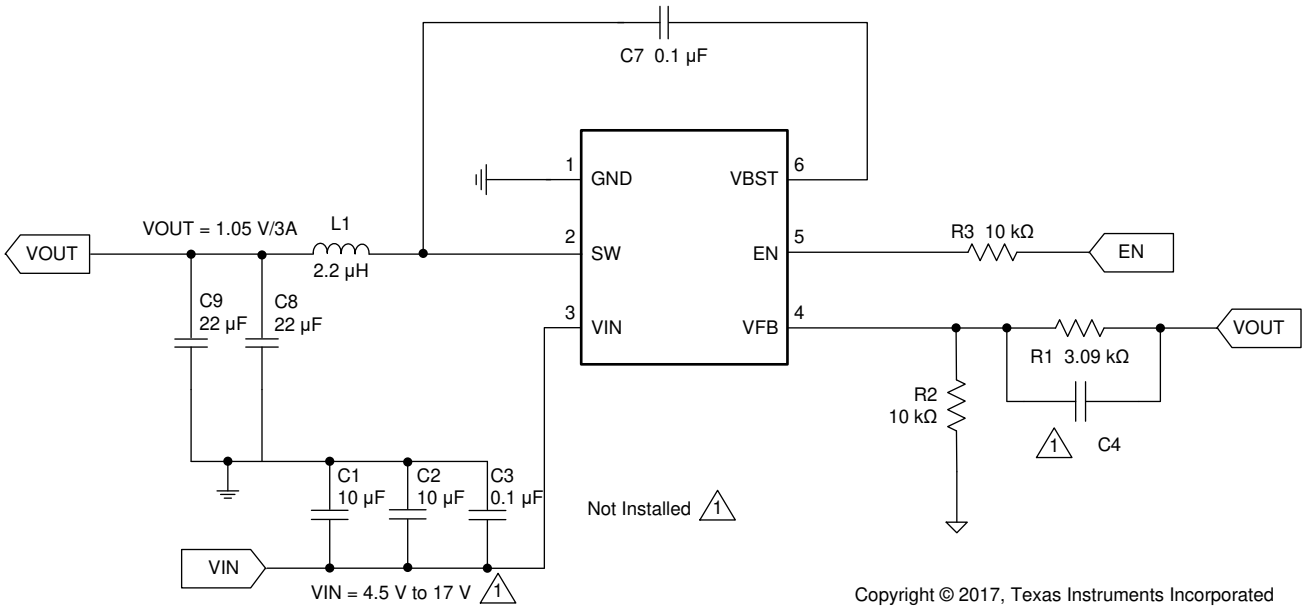



**図 7-1. TPS563201 and TPS563208 1.05-V/3-A Reference Design**

### 7.2.1 Design Requirements

表 7-1 shows the design parameters for this application.

**表 7-1. Design Parameters**

| PARAMETER | EXAMPLE VALUE |
|---|---|
| Input voltage range | 4.5 to 17 V |
| Output voltage | 1.05 V |
| Transient response, 1.5-A load step | ΔVout = ±5% |
| Input ripple voltage | 400 mV |
| Output ripple voltage | 30 mV |
| Output current rating | 3 A |
| Operating frequency | 580 kHz |

### 7.2.2 Detailed Design Procedure

#### 7.2.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS56320x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 7.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. TI recommends to use 1% tolerance or better divider resistors. Start by using 式 2 to calculate $V_{OUT}$.

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable.

$$V_{OUT} = 0.768 \times \left(1 + \frac{R1}{R2}\right) \tag{2}$$

#### 7.2.2.3 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 control scheme introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero

frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 式 3 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in 表 7-2.

**表 7-2. Recommended Component Values**

| OUTPUT VOLTAGE (V) | R1 (kΩ) | R2 (kΩ) | L1 (µH) | | | C8 + C9 (µF) |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| 1 | 3.09 | 10.0 | 1.5 | 2.2 | 4.7 | 20 to 68 |
| 1.05 | 3.74 | 10.0 | 1.5 | 2.2 | 4.7 | 20 to 68 |
| 1.2 | 5.76 | 10.0 | 1.5 | 2.2 | 4.7 | 20 to 68 |
| 1.5 | 9.53 | 10.0 | 1.5 | 2.2 | 4.7 | 20 to 68 |
| 1.8 | 13.7 | 10.0 | 1.5 | 2.2 | 4.7 | 20 to 68 |
| 2.5 | 22.6 | 10.0 | 2.2 | 2.2 | 4.7 | 20 to 68 |
| 3.3 | 33.2 | 10.0 | 2.2 | 2.2 | 4.7 | 20 to 68 |
| 5 | 54.9 | 10.0 | 3.3 | 3.3 | 4.7 | 20 to 68 |
| 6.5 | 75 | 10.0 | 3.3 | 3.3 | 4.7 | 20 to 68 |

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using 式 4, 式 5, and 式 6. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

$$II_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \quad (4)$$

$$II_{PEAK} = I_O + \frac{II_{P-P}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_O^2 + \frac{1}{12} II_{P-P}^2} \quad (6)$$

For this design example, the calculated peak current is 3.5 A and the calculated RMS current is 3.01 A. The inductor used is a WE 74431122 with a peak current rating of 13 A and an RMS current rating of 9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS563201 and TPS563208 are intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 68 µF. Use 式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (7)$$

For this design two TDK C3216X5R0J226M 22-µF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.286 A and each output capacitor is rated for 4 A.

#### 7.2.2.4 Input Capacitor Selection

The TPS563201 and TPS563208 require an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

#### 7.2.2.5 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

### 7.2.3 Application Curves

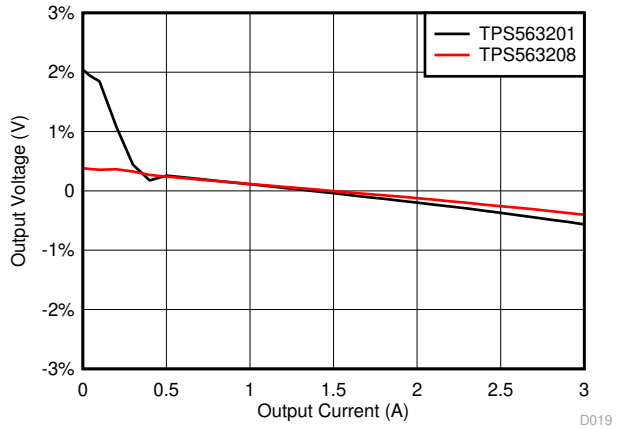



**図 7-2. TPS563201 and TPS563208 Load Regulation, $V_{IN}$ = 5 V**

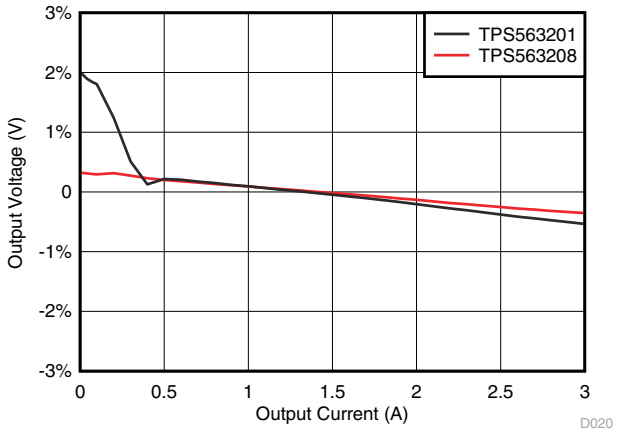
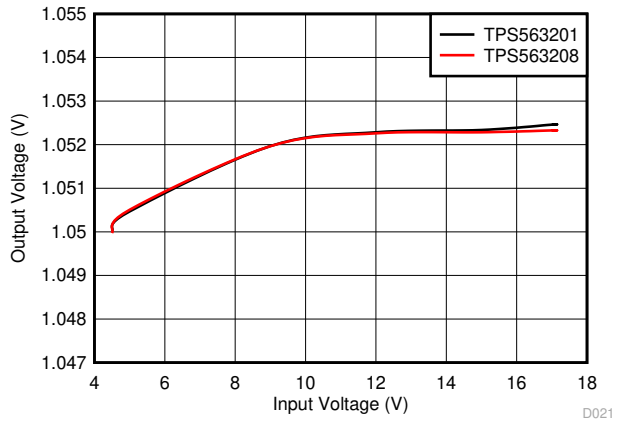



**図 7-3. TPS563201 and TPS563208 Load Regulation, $V_{IN}$ = 12 V**




$I_{OUT}$ of TPS563201: 1 A
$I_{OUT}$ of TPS563208: 10 mA

**図 7-4. TPS563201 and TPS563208 Line Regulation**

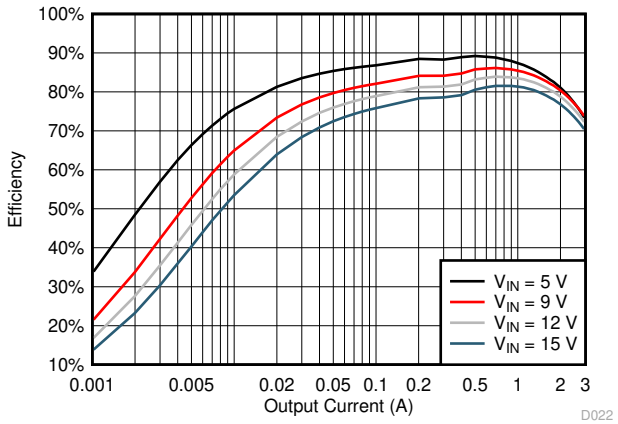
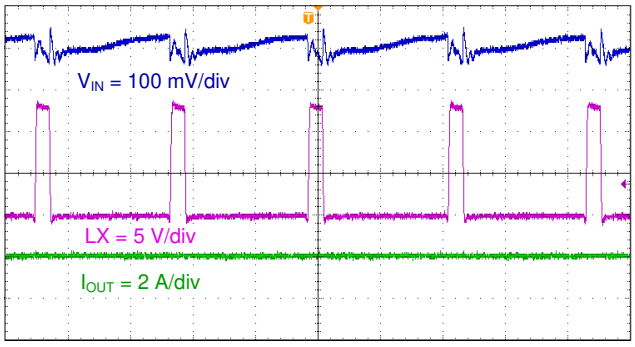
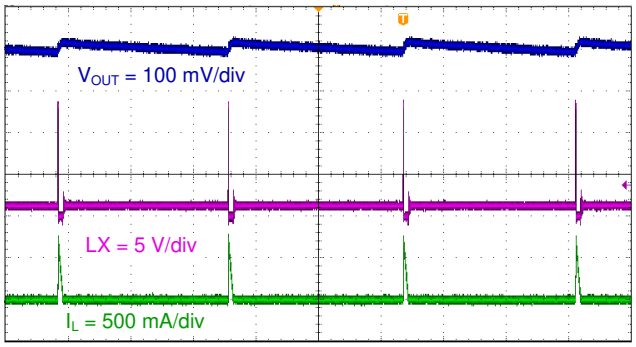



**図 7-5. TPS563201 Efficiency**




800 ns/div

**図 7-6. TPS563201 Input Voltage Ripple**




20 µs/div

**図 7-7. TPS563201 Output Voltage Ripple, 10 mA**

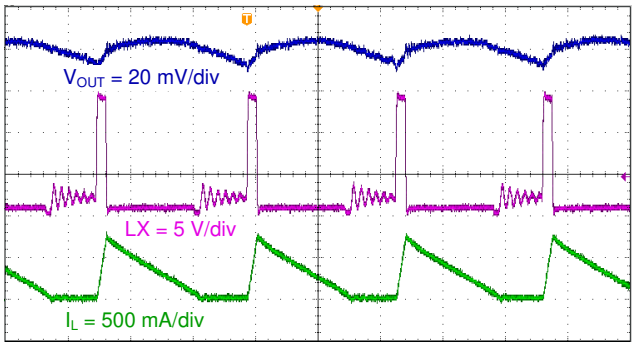



**図 7-8. TPS563201 Output Voltage Ripple, $I_{out}$ = 0.25 A**

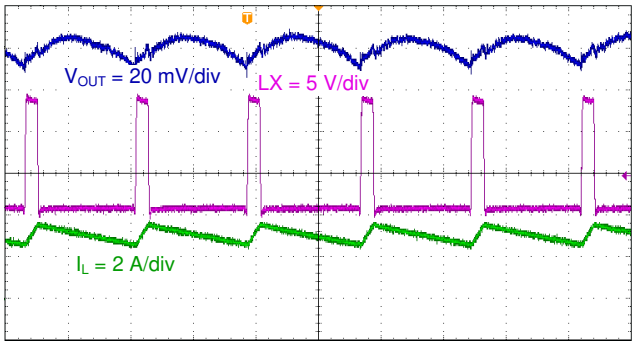



**図 7-9. TPS563201 Output Voltage Ripple, $I_{out}$ = 2 A**

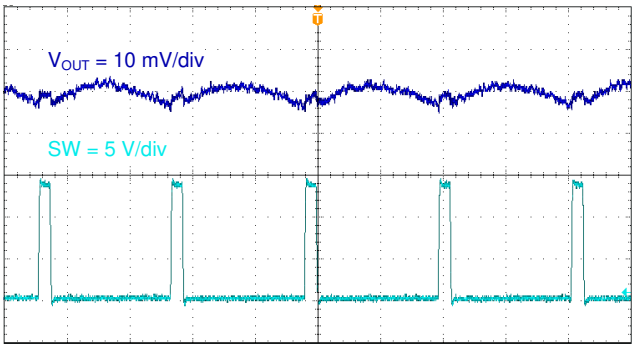



**図 7-10. TPS563208 Output Voltage Ripple, $I_{OUT}$ = 0 A**

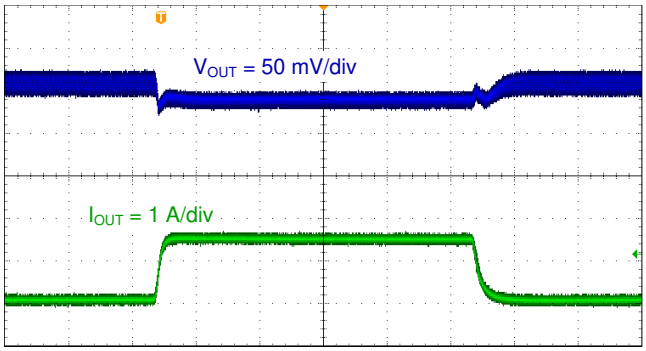



**図 7-11. TPS563201 Transient Response, 0.1 to 1.5 A**

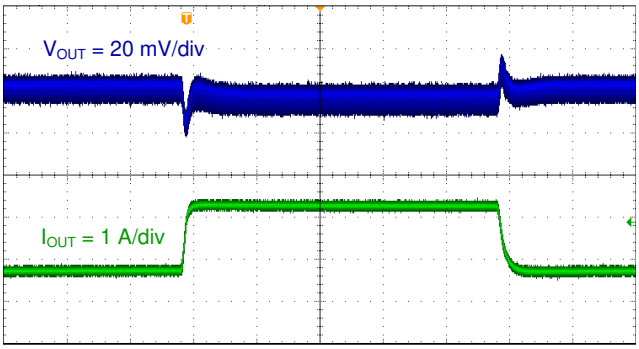



**図 7-12. TPS563201 Transient Response, 0.75 to 2.25 A**

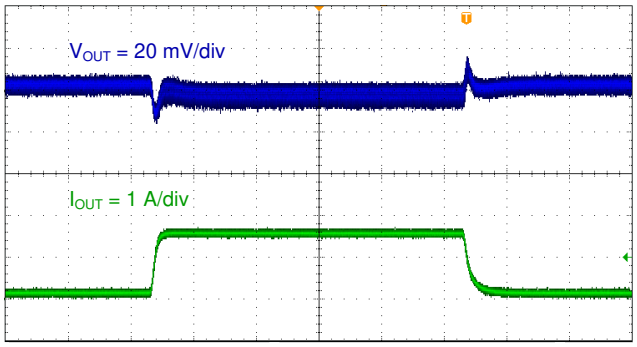



**図 7-13. TPS563208 Transient Response 0.1 to 2 A**

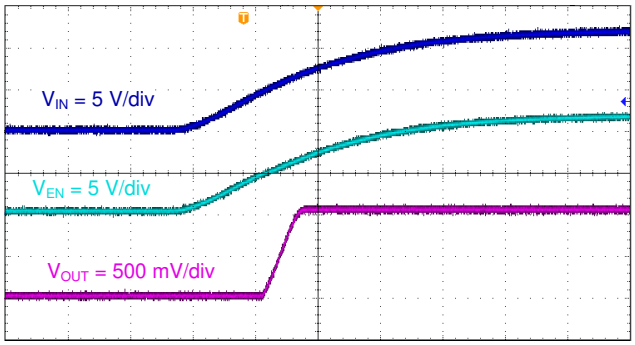



図 7-14. TPS563201 Start Up Relative to $V_I$

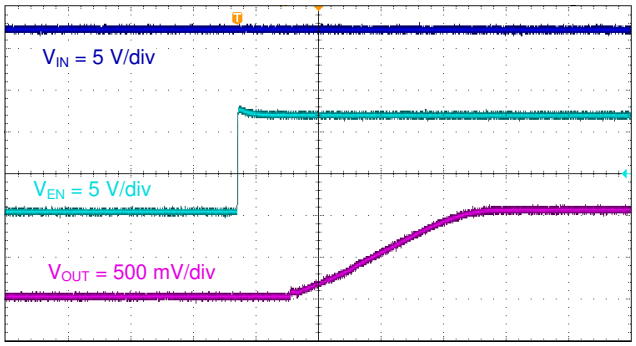



図 7-15. TPS563201 Start-Up Relative to EN

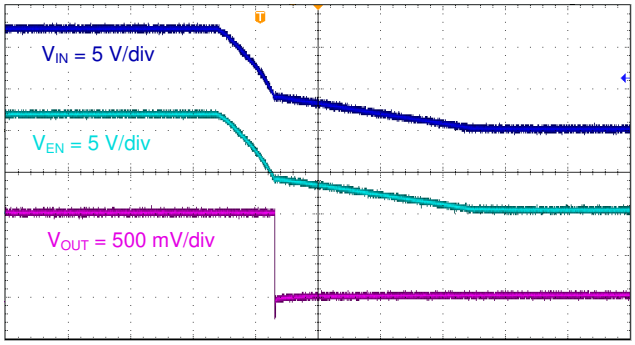



図 7-16. TPS563201 Shutdown Relative to $V_I$

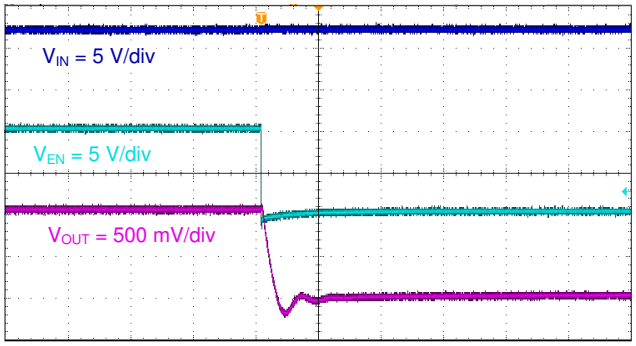



図 7-17. TPS563201 Shutdown Relative to EN

## 7.3 Power Supply Recommendations

TPS563201 and TPS563208 are designed to operate from input supply voltage in the range of 4.5 V to 17 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. The maximum recommended operating duty cycle is 75%. Using that criteria, the minimum recommended input voltage is $V_O$ / 0.75.

## 7.4 Layout

### *7.4.1 Layout Guidelines*

1. VIN and GND traces must be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor must be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path must be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop must be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the VFB node must be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin must be as wide as possible to minimize its trace impedance.

### 7.4.2 Layout Example

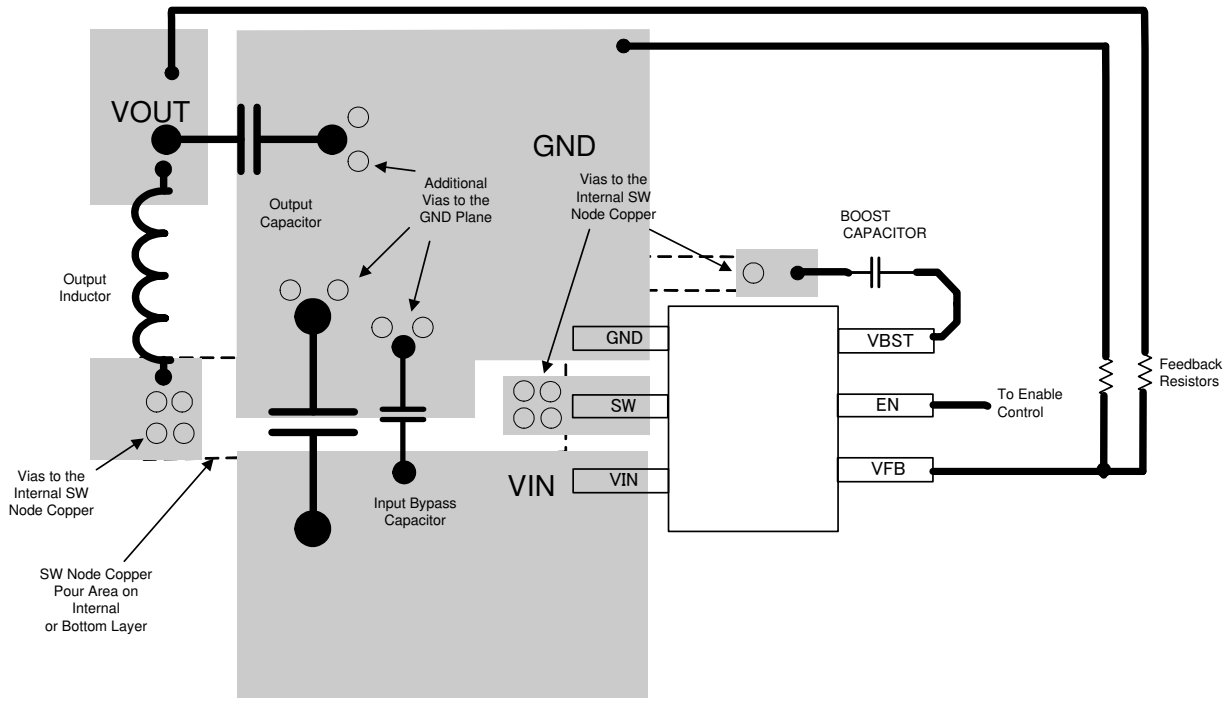



**図 7-18. TPS563201 and TPS563208 Layout**

# 8 Device and Documentation Support

## 8.1 Device Support

### *8.1.1 Development Support*

#### 8.1.1.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS56320x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
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- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

## 8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 8.3 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

## 9 Revision History

| Changes from Revision A (April 2024) to Revision B (September 2024) | Page |
|---|---|
| • Updated specifications in the *Electrical Characteristics* table | 6 |
| • Updated 図 5-7 and 図 5-8 | 7 |
| • Updated the *Normal Operation* description | 12 |

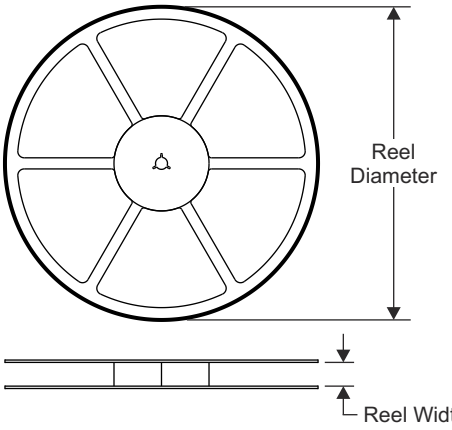
| Changes from Revision * (December 2015) to Revision A (April 2024) | Page |
|---|---|
| • ドキュメント全体にわたって表、図、相互参照の採番方法を更新 | 1 |
| • 低いシャットダウン電流 10μA 未満から 20μA に変更 | 1 |
| • ドキュメント全体にわたって WEBENCH 情報を追加 | 1 |
| • 商標の情報を更新 | 1 |
| • デバイス情報表のフォーマットを更新 | 1 |
| • Changed VBST (vs SW) and VFB MAX from 6.5 to 6 | 4 |
| • Changed Human-body model (HBM) value from 3000 to 2000 | 4 |
| • Changed VBST (vs SW) MAX from 6.0 to 5.5 | 4 |
| • Updated specifications in the *Electrical Characteristics* table | 6 |
| • Updated 図 5-1 and 図 5-2 | 7 |
| • Updated the *Current Protection* section | 11 |

## 10 Mechanical, Packaging, and Orderable Information

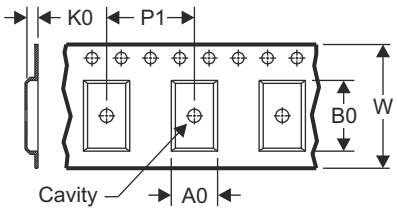
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 10.1 Tape and Reel Information

REEL DIMENSIONS

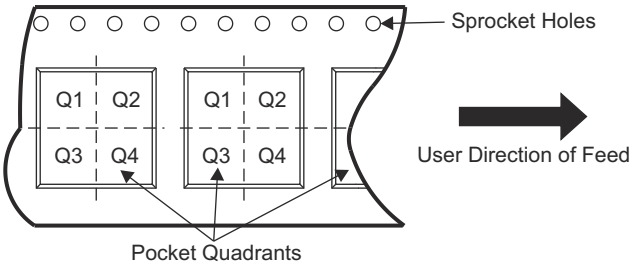



TAPE DIMENSIONS



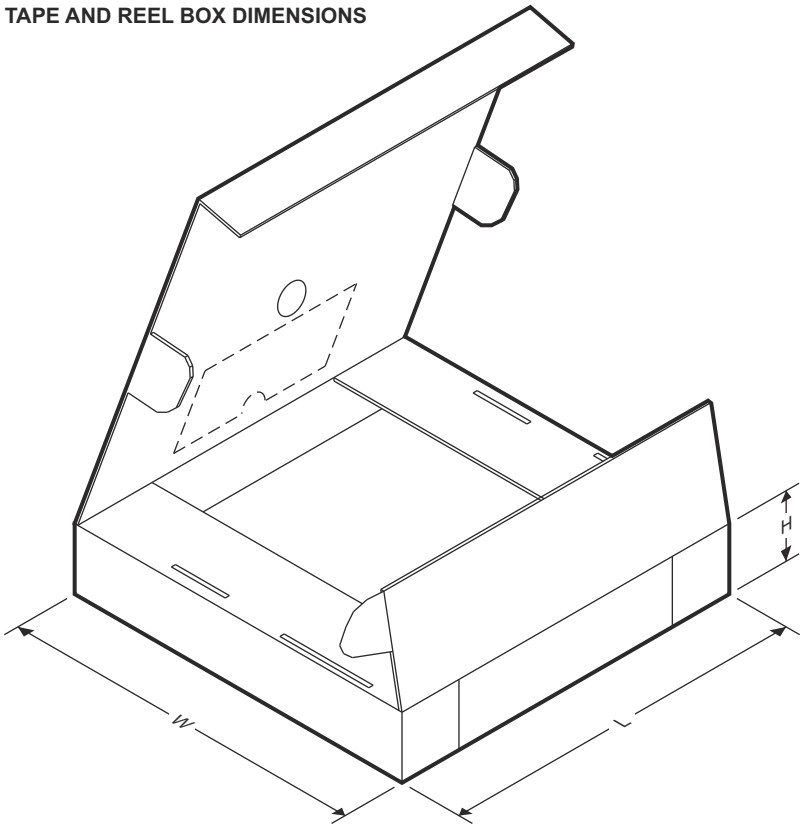

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS563201DDCR | SOT-23-THIN | DDC | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS563201DDCR | SOT-23-THIN | DDC | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS563201DDCT | SOT-23-THIN | DDC | 6 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS563201DDCT | SOT-23-THIN | DDC | 6 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS563208DDCR | SOT-23-THIN | DDC | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS563208DDCR | SOT-23-THIN | DDC | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS563208DDCT | SOT-23-THIN | DDC | 6 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

**TAPE AND REEL BOX DIMENSIONS**



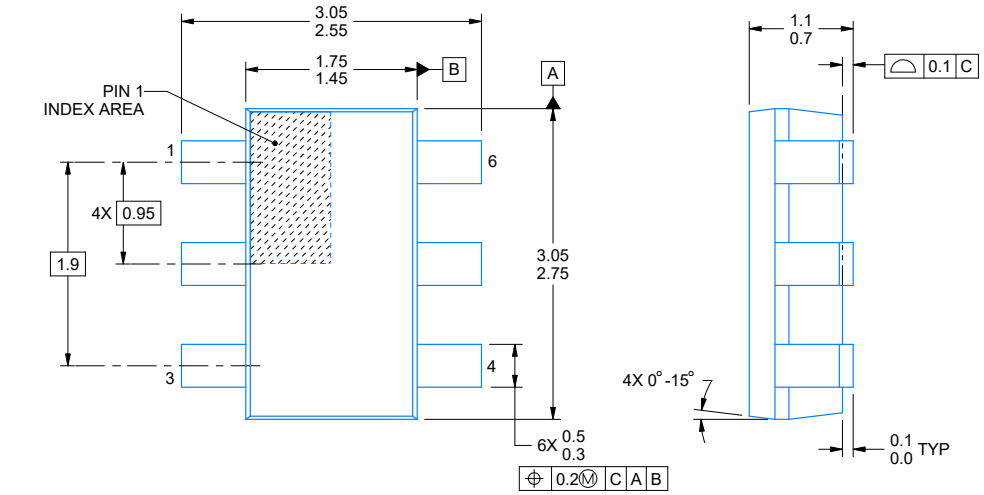

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS563201DDCR | SOT-23-THIN | DDC | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS563201DDCR | SOT-23-THIN | DDC | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS563201DDCT | SOT-23-THIN | DDC | 6 | 250 | 210.0 | 185.0 | 35.0 |
| TPS563201DDCT | SOT-23-THIN | DDC | 6 | 250 | 210.0 | 185.0 | 35.0 |
| TPS563208DDCR | SOT-23-THIN | DDC | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS563208DDCR | SOT-23-THIN | DDC | 6 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS563208DDCT | SOT-23-THIN | DDC | 6 | 250 | 210.0 | 185.0 | 35.0 |

# PACKAGE OUTLINE

## DDC0006A

## SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

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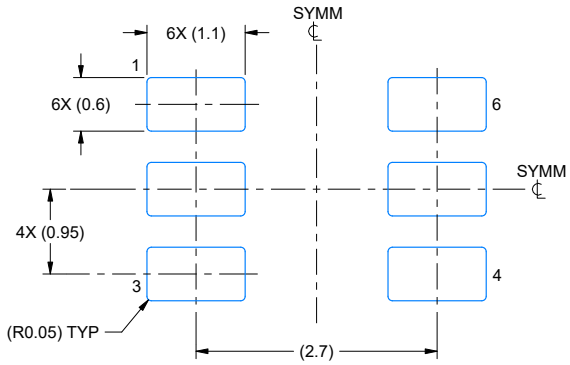
## EXAMPLE BOARD LAYOUT

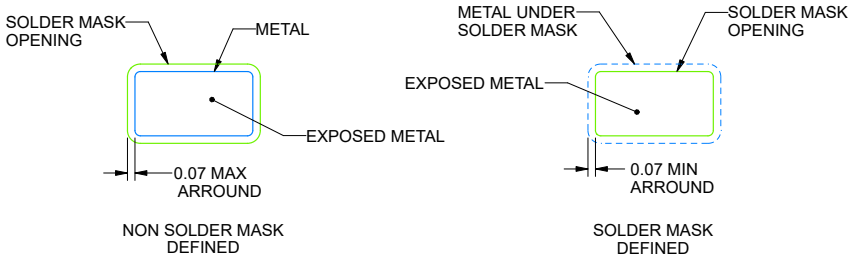
### DDC0006A

**SOT-23 - 1.1 max height**

SMALL OUTLINE TRANSISTOR




LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X




SOLDERMASK DETAILS

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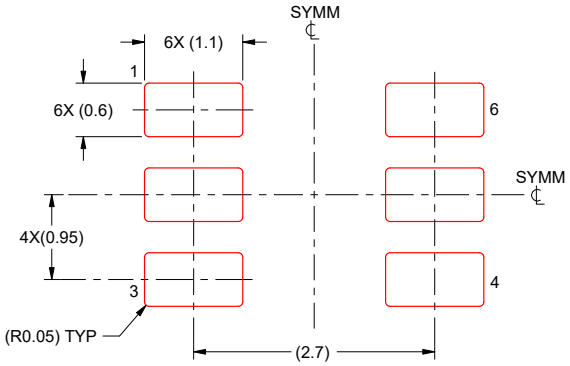
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

**DDC0006A** — **SOT-23 - 1.1 max height**

SMALL OUTLINE TRANSISTOR




SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS563201DDCR | ACTIVE | SOT-23-THIN | DDC | 6 | 3000 | RoHS & Green | Call TI \| SN | Level-1-260C-UNLIM | -40 to 125 | 3201 | Samples |
| TPS563201DDCT | ACTIVE | SOT-23-THIN | DDC | 6 | 250 | RoHS & Green | Call TI \| SN | Level-1-260C-UNLIM | -40 to 125 | 3201 | Samples |
| TPS563208DDCR | ACTIVE | SOT-23-THIN | DDC | 6 | 3000 | RoHS & Green | Call TI \| SN | Level-1-260C-UNLIM | -40 to 125 | 3208 | Samples |
| TPS563208DDCT | ACTIVE | SOT-23-THIN | DDC | 6 | 250 | RoHS & Green | Call TI \| SN | Level-1-260C-UNLIM | -40 to 125 | 3208 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

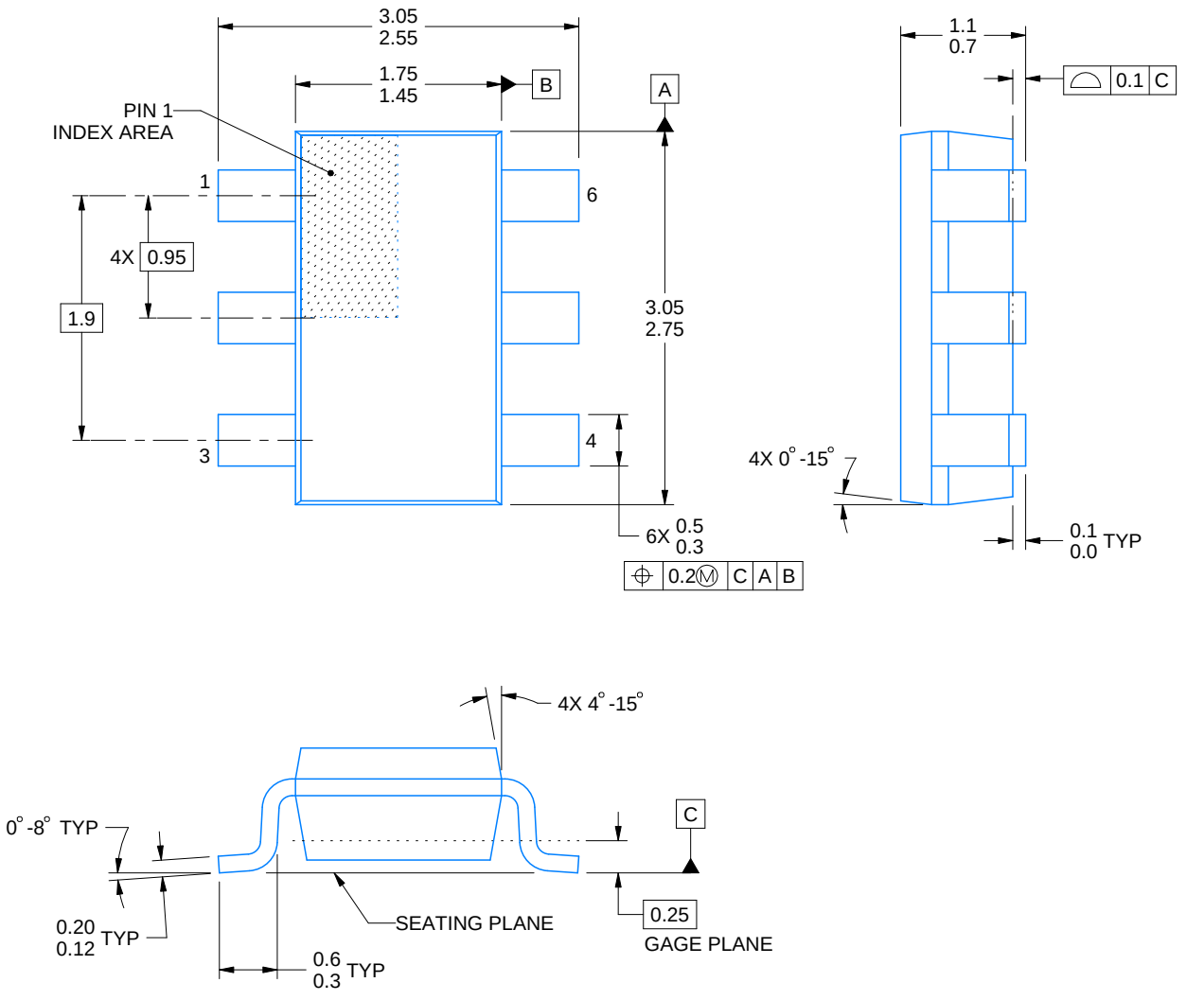
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

# PACKAGE OUTLINE

## DDC0006A

## SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR




4214841/E 08/2024

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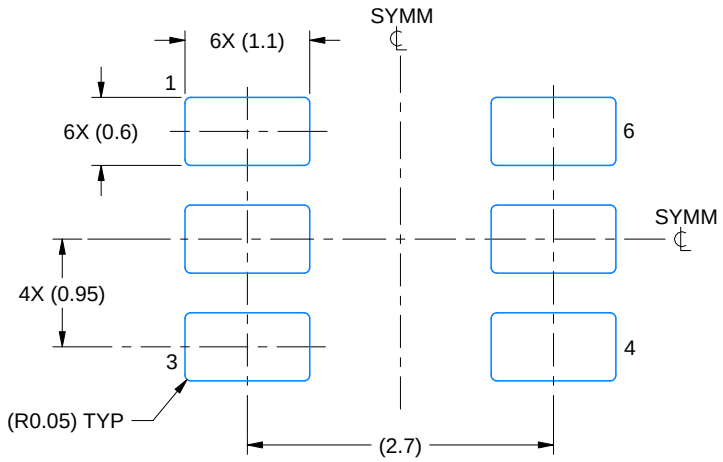
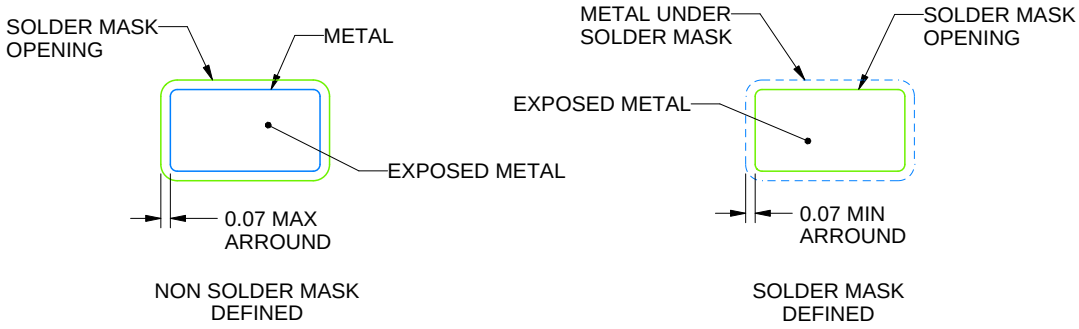
3. Reference JEDEC MO-193.




LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X




SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

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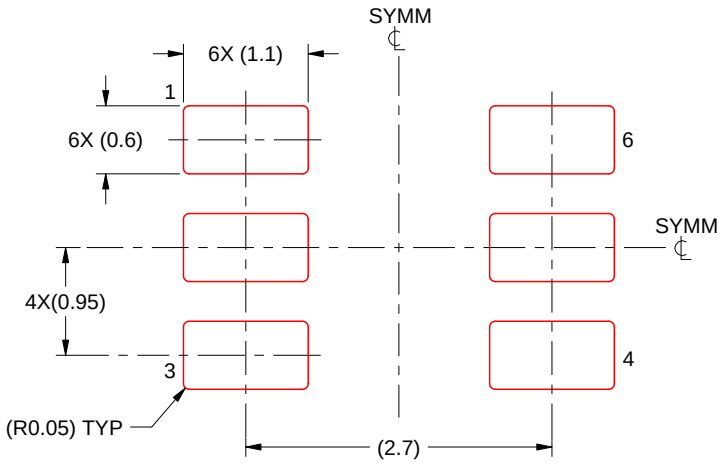


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

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