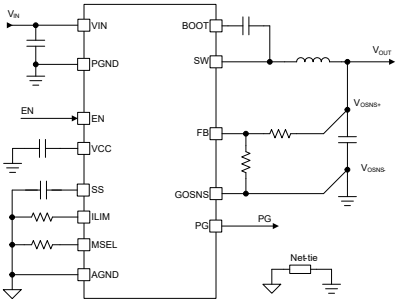
TPS54KB2x 4V～16V 入力、25A、リモート センス、D-CAP4 同期整流降圧コンバータ

1 特長

- 入力電圧範囲:4V～16V
- 3.1V～5.3V の外部 VCC バイアスをサポート
- 5.8mΩ および 2.3mΩ の MOSFET
- 連続出力電流:25A
- 効率と放熱性能向けに最適化された 16 ピン WQFN-HR パッケージ
- T_J = -40℃～+125℃で ±0.5% の基準電圧 (VREF)
- 出力電圧範囲:VREF～5.5V
- 差動リモート センス
- D-CAP4 による超高速負荷ステップ応答
- すべての出力コンデンサでセラミック コンデンサの使用をサポート
- 軽負荷時の高効率を実現する自動スキップ Eco-mode を選択可能
- 電流制限を R_{ILIM} でプログラム可能
- 選択可能なスイッチング周波数:800kHz、1.1MHz、1.4MHz
- ソフトスタート時間をプログラム可能
- プリバイアス付きスタートアップ機能
- オープン ドレインのパワー グッド出力
- バレー過電流制限保護
- 過電圧および低電圧フォルト保護
- 30A の TPS54KC23 とピン互換

2 アプリケーション

- ラック・サーバーとブレード・サーバー
- ハードウェア・アクセラレータおよびアドイン・カード
- データ・センター向けスイッチ
- 産業用 PC
- ベースバンド・ユニット (BBU)



概略回路図

3 概要

TPS54KB2x デバイスは、適応型オン時間 D-CAP4 制御モードを備えた小型で高効率の同期整流降圧コンバータです。この制御方式により、外部補償ネットワークを必要とせずに、出力電圧範囲全体にわたって低い最小オン時間と高速負荷過渡応答を実現できます。外部補償が不要のため、本デバイスは使いやすく、外付け部品をほとんど必要としません。このデバイスは、スペースに制約のあるデータ センター アプリケーションに適した設計になっています。

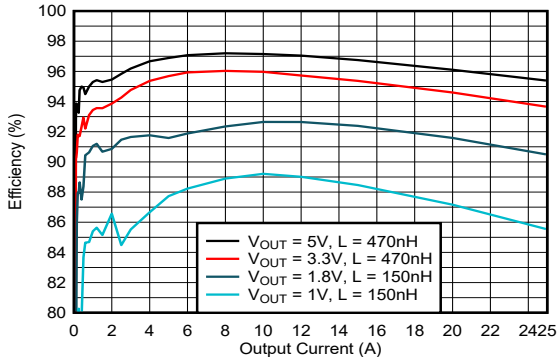
TPS54KB2x デバイスは、差動リモート センス、高性能の内蔵 MOSFET、動作時接合部温度の規定範囲にわたって高精度 ±0.5% 基準電圧を備えています。このデバイスは、高精度のロード レギュレーションとライン レギュレーション、Eco-mode または FCCM 動作、MSEL ピンによるプログラム可能な設定、プログラマブル ソフトスタートを特長としています。

TPS54KB2x デバイスは鉛フリー デバイスです。RoHS に準拠しています (適用除外なし)。

製品情報

部品番号	VREF (V)	フォルト応答	パッケージ サイズ(1)
TPS54KB20	0.9	ラッチオフ	3.00mm × 3.50mm
TPS54KB21	0.5		
TPS54KB22	0.9	ヒカップ	
TPS54KB23	0.5		

(1) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



代表的なアプリケーション効率 (V_{IN} = 12V、f_{SW} = 800kHz、内部 VCC、スキップ モード)

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4 Pin Configuration and Functions

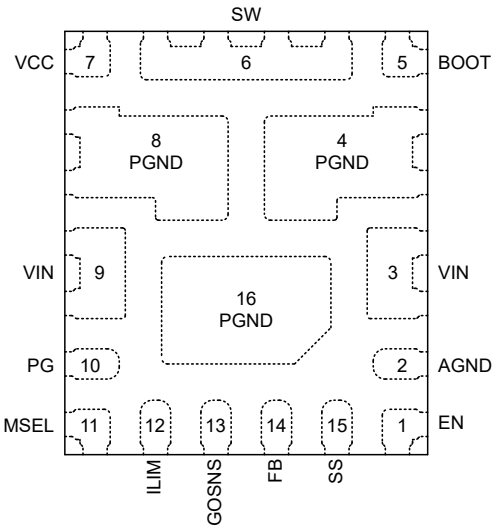


図 4-1. RZR Package 16-Pin WQFN-FCRLF Top View

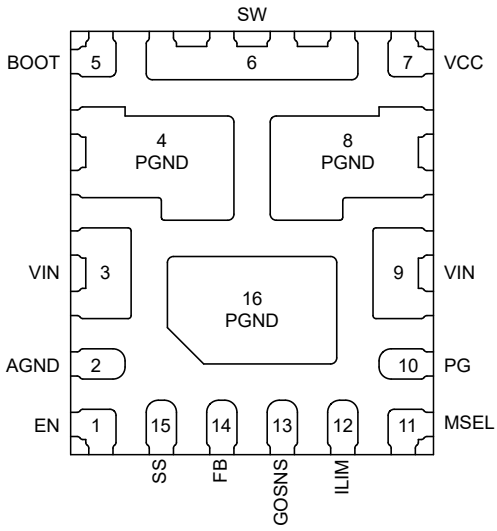


図 4-2. RZR Package 16-Pin WQFN-FCRLF Bottom View

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
2	AGND	G	Analog ground return and reference for the internal control circuits.
5	BOOT	I/O	Supply for the internal high-side MOSFET gate driver (boost terminal). Connect the bootstrap capacitor from this pin to SW node.
1	EN	I	Enable pin. The enable pin turns the DC/DC switching converter on or off. Floating EN pin before start-up disables the converter. The recommended maximum voltage applied to the EN pin is 5.5V. TI *does not* recommend connecting the EN pin to VIN pin directly.
14	FB	I	Output voltage feedback input. A resistor divider from the output voltage to GOSNS (tapped to FB pin) sets the output voltage. Connect the FB divider to the output voltage near the load.
13	GOSNS	I	Negative input of the differential remote sense circuit. Connect to a ground sense point near the load.
12	ILIM	I	Current limit setting pin. Connect a resistor to AGND to set the current limit trip point. TI recommends a ±1% tolerance resistor. See セクション 6.3.10 for details on OCL setting.
11	MSEL	I	Multi-function select pin. A resistor from the MSEL pin to AGND selects between forced continuous-conduction mode (FCCM) or skip-mode operation, the operating frequency, and the PWM ramp setting. A ±1% tolerance resistor is required. See 表 6-4 for details.
10	PG	O	Open-drain power-good status signal. Connect an external pullup resistor to a voltage source. When the FB voltage moves outside the specified limits, PG goes low after the specified delay.
4, 8, 16	PGND	G	Ground return for the power stage. This pin is internally connected to the source of the low-side MOSFET. Place as many vias as possible beneath the PGND pins and as close as possible to the PGND pins. This action minimizes parasitic impedance and also lowers thermal resistance.
15	SS	I	Connect a capacitor to AGND to set the SS time. A minimum 10nF capacitor is required for this pin to avoid overshoot during the charge of soft-start capacitor.
6	SW	O	Output switching terminal of the power converter. Connect this pin to the output inductor.
7	VCC	P	Internal 3V LDO output. A 3.3V or 5V external bias can be connected to this pin to save the power losses on the internal LDO. The voltage source on this pin powers both the internal circuitry and gate driver. Bypass with a 1µF, > 6.3V rating, ceramic capacitor from VCC pin to PGND. Place this capacitor as close to the VCC and PGND pins as possible.

表 4-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
3, 9	VIN	P	Power-supply input pins for both the power stage MOSFETs and the internal LDO. Place the decoupling input capacitors from VIN pins to PGND pins as close as possible. A capacitor from each VIN to PGND close to IC is required.

(1) I = Input, O = Output, P = Supply, G = Ground

5 Specifications

5.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN, across full recommended V_{VCC} range	–0.3	18	V
Pin voltage	VIN, V_{VCC} ≤ 3.6V	–0.3	19	V
Pin voltage	SW – PGND, DC	–0.3	19	V
Pin voltage	SW – PGND, transient < 10ns	–3	21	V
Pin voltage	VIN – SW, DC	–0.3	19	V
Pin voltage	VIN – SW, transient < 10ns	–3	25	V
Pin voltage	BOOT – PGND	–0.3	24.5	V
Pin voltage	BOOT – SW	–0.3	5.5	V
Pin voltage	EN, PG, SS, MSEL, VCC	–0.3	6	V
Pin voltage	ILIM, FB	–0.3	3	V
Pin voltage	GOSNS, PGND	–0.3	0.3	V
Sink current	PG		15	mA
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 (2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{IN}	Input voltage range	VIN	4		16	V
V_{VCC}	External bias range	VCC	3.1		5.3	V
V_{OUT}	Output voltage range		VREF		5.5	
Pin voltage		V_{GOSNS} versus V_{AGND}	–0.1		0.1	V
		EN, PG	–0.1		5.5	V
I_{PG}	Power-good sinking current	PG			10	mA
C_{SS}	Capacitance range	SS	10		1000	nF
I_{OUT}	Output current	SW			25	A
IL_{PEAK}	Maximum peak inductor current	SW			45	A
T_J	Operating junction temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC[1]		TPS54KB2x			UNIT
		RZR (WQFN-FCRLF, JEDEC layout)	RZR (WQFN-FCRLF, 4-layer application layout)	RZR (WQFN-FCRLF, 6-layer EVM layout)	
		16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.8	16.5 [2]	13.2 [3]	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.3	Not applicable [4]	Not applicable [4]	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.6	Not applicable [4]	Not applicable [4]	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	Not applicable [4]	Not applicable [4]	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.5	Not applicable [4]	Not applicable [4]	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.1	Not applicable [4]	Not applicable [4]	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Measured on 4 layer, 2 oz copper, 3 inch × 3 inch layout with the device not switching and 1.9W dissipated in the device.
(3) Measured on U2 device on EVM with the device not switching and 1.8W dissipated in the device.
(4) The thermal test or simulation setup is not applicable to an application layout.

5.5 Electrical Characteristics

T_J = –40°C to +125°C, V_{VCC} = 3V (internal), V_{VIN} = 4V to 16V. Typical values are at T_J = 25°C and V_{VIN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current	Non-switching, V_{EN} = 2V, V_{FB} = V_{FB_REG} + 10mV, no external bias on VCC pin		940	1200	µA
$I_{Q(VIN)}$	VIN quiescent current with external VCC bias	V_{IN} = 12V, V_{EN} = 2V, V_{FB} = V_{FB_REG} + 10mV (non-switching), 3.3V external bias on VCC pin		230	350	µA
$I_{Q(VCC)}$	VCC quiescent current	V_{IN} = 12V, V_{EN} = 2V, V_{FB} = V_{FB_REG} + 10mV (non-switching), 3.3V external bias on VCC pin		820	1000	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{IN} = 12V, V_{EN} = 0V, no external bias on VCC pin		9	20	µA
$I_{SD(VCC)}$	VCC shutdown current	V_{EN} = 0V, V_{IN} = 0V, 3.3V external bias on VCC pin		90	140	µA
I_{VCC}	VCC external bias current	T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, regular switching, R_{MSEL} = 10.5kΩ, f_{SW} = 800kHz, 3.3V external bias on VCC pin		12		mA
		T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, regular switching, R_{MSEL} = 13.3kΩ, f_{SW} = 1100kHz, 3.3V external bias on VCC pin		16		mA
		T_J = 25°C, V_{IN} = 12V, V_{EN} = 2V, regular switching, R_{MSEL} = 30.1kΩ, f_{SW} = 1400kHz, 3.3V external bias on VCC pin		20.5		mA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising		3.87	3.95	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	3.60	3.70		V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.17		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching		1.18	1.23	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.95	1		V
$V_{EN(H)}$	EN voltage hysteresis			0.18		V
	EN internal pull-down resistance	EN pin to AGND	0.74	1	1.27	MΩ
$V_{ENSTB(R)}$	EN standby rising threshold	EN rising, enable internal LDO, no switching		0.75	1.0	V
$V_{ENSTB(F)}$	EN standby falling threshold	EN falling, disable internal LDO	0.5	0.6		V
INTERNAL LDO (VCC)						

5.5 Electrical Characteristics (続き)

T_J = –40°C to +125°C, V_{VCC} = 3V (internal), V_{VIN} = 4V to 16V. Typical values are at T_J = 25°C and V_{VIN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{VCC}	Internal LDO output voltage	Non-switching, I_{VCC} = 25mA	2.82	2.94	3.05	V
I_{VCC}	Internal LDO short-circuit current limit	V_{VIN} = 10V	100	275		mA
$VCC_{UVLO(R)}$	VCC UVLO rising threshold	V_{VIN} = 4V		2.7	2.82	V
$VCC_{UVLO(F)}$	VCC UVLO falling threshold	V_{VIN} = 4V	2.45	2.55		V
$VCC_{UVLO(H)}$	VCC UVLO hysteresis	V_{VIN} = 4V		0.15		V
	FB threshold to turn off VCC LDO	EN high to low	25	50	85	mV
REFERENCE VOLTAGE (FB)						
V_{FB_REG}	Feedback regulation voltage	TPS54KB20 and TPS54KB22	895.5	900	904.5	mV
V_{FB_REG}	Feedback regulation voltage	TPS54KB21 and TPS54KB23	497.5	500	502.5	mV
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = V_{FB_REG}			160	nA
DIFFERENTIAL REMOTE SENSE AMPLIFIER						
I_{GOSNS}	Leakage current out of GOSNS pin	V_{GOSNS} - V_{AGND} = 100mV			80	µA
V_{ICM}	GOSNS common mode voltage for regulation	V_{GOSNS} versus V_{AGND}	–0.1		0.1	V
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FCCM operation	V_{VIN} = 12V, V_{OUT} = 3.3V, R_{MSEL} = 10.5kΩ (FCCM), No load	680	800	920	kHz
		V_{VIN} = 12V, V_{OUT} = 3.3V, R_{MSEL} = 24.9kΩ (FCCM), No load	910	1070	1230	kHz
		V_{VIN} = 12V, V_{OUT} = 3.3V, R_{MSEL} = 48.7kΩ (FCCM), No load	1150	1350	1550	kHz
STARTUP						
I_{SS}	Soft-start charge current	V_{SS} = 0V	26	36	45	µA
$V_{SS(DONE)}$	Soft-start voltage threshold for soft-start done	TPS54KB21 and TPS54KB23		1		V
$V_{SS(DONE)}$	Soft-start voltage threshold for soft-start done	TPS54KB20 and TPS54KB22		1.2		V
	EN HIGH to start of switching delay	C_{SS} = 33nF, Internal VCC, C_{VCC} = 2.2µF, R_{MSEL} = 158kΩ, Measured from EN high to V_{SS} = 50mV		740		µs
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	$V_{BOOT-SW}$ = 3.0V		5.8		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	V_{VCC} = 3.3V		2.3		mΩ
$t_{ON(min)}$	Minimum ON pulse width			40		ns
$t_{OFF(min)}$	Minimum OFF pulse width (1)			130	160	ns
BOOT CIRCUIT						
$I_{BOOT(LKG)}$	Leakage current into BOOT pin	V_{VIN} = 12V, $V_{BOOT-SW}$ = 3V, Enabled, Not switching		23	31	µA
OVERCURRENT PROTECTION						
	OC limit high clamp	Valley current on LS FET, 0Ω ≤ R_{ILIM} ≤ 4.32kΩ	25	27.5		A
K_{OCL}	Constant for R_{ILIM} equation			120000		A×Ω
$I_{LS(OC)}$	Low-side valley current limit, open loop	Valley current on LS FET, R_{ILIM} = 4.32kΩ	25	27.5		A
		Valley current on LS FET, R_{ILIM} = 5.36kΩ	17.9	22.1	26.5	A
		Valley current on LS FET, R_{ILIM} = 7.32kΩ	13.0	16.2	19.6	A
		Valley current on LS FET, R_{ILIM} = 10.7kΩ	8.5	11.1	13.7	A
		Valley current on LS FET, R_{ILIM} = 20kΩ	4.0	5.9	7.9	A
$I_{LS(NOC)}$	Low-side negative current limit, open loop	Sinking current limit on LS FET		–10	–7.5	A
R_{ILIM}	ILIM pin resistance range		0		20	kΩ
I_{ZC}	Zero-cross detection current threshold to enter DCM, open loop	V_{IN} = 12V		–700		mA

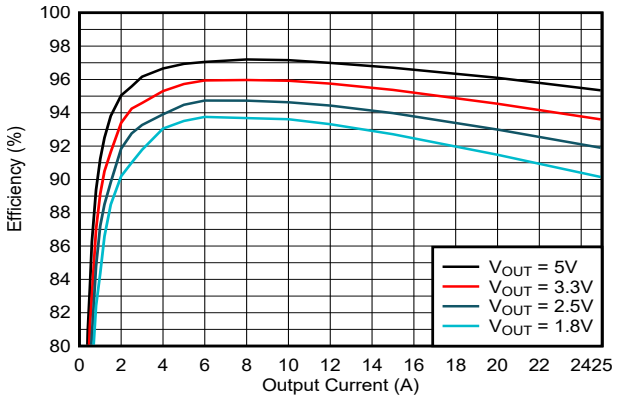
5.5 Electrical Characteristics (続き)

T_J = –40°C to +125°C, V_{VCC} = 3V (internal), V_{VIN} = 4V to 16V. Typical values are at T_J = 25°C and V_{VIN} = 12V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{ZC(HYS)}$	Zero-cross detection current threshold hysteresis after entering DCM, open loop	V_{IN} = 12V		1000		mA
OUTPUT OVP AND UVP						
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	TPS54KB21 and TPS54KB23, V_{FB} rising	113%	116%	119%	
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	TPS54KB21 and TPS54KB23, V_{FB} falling	76%	79%	82%	
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	TPS54KB20 and TPS54KB22, V_{FB} rising	115%	118%	121%	
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	TPS54KB20 and TPS54KB22, V_{FB} falling	77%	80%	83%	
t_{OVPDLY}	OVP delay	With 100mV overdrive		400		ns
t_{UVPDLY}	UVP filter delay			70		µs
	Hiccup wait time	TPS54KB22 and TPS54KB23		7 x t_{SS}		ms
POWER GOOD						
$V_{PGTH(RISE\_OV)}$	Power-good threshold	TPS54KB20 and TPS54KB22, FB rising, PG high to low	115%	118%	121%	
$V_{PGTH(RISE\_UV)}$	Power-good threshold	TPS54KB20 and TPS54KB22, FB rising, PG low to high	89%	92.5%	95%	
$V_{PGTH(FALL\_UV)}$	Power-good threshold	TPS54KB20 and TPS54KB22, FB falling, PG high to low	77%	80%	83%	
$V_{PGTH(RISE\_OV)}$	Power-good threshold	TPS54KB21 and TPS54KB23, FB rising, PG high to low	113%	116%	119%	
$V_{PGTH(RISE\_UV)}$	Power-good threshold	TPS54KB21 and TPS54KB23, FB rising, PG low to high		91%		
$V_{PGTH(FALL\_UV)}$	Power-good threshold	TPS54KB21 and TPS54KB23, FB falling, PG high to low		79%		
	PG delay going from low to high during startup			1.3		ms
	PG delay going from high to low			4	6.2	µs
$I_{PG(LKG)}$	PG pin leakage current when open drain output is high	V_{PG} = 6V			7	µA
	PG pin output low-level voltage	I_{PG} = 7mA			500	mV
	PG pin output low-level when VIN and VCC are low	V_{VIN} = 0V, V_{VCC} = 0V, V_{EN} = 0V, I_{PG} = 25µA		650		mV
	PG pin output low-level when VIN and VCC are low	V_{VIN} = 0V, V_{VCC} = 0V, V_{EN} = 0V, I_{PG} = 250µA		800		mV
THERMAL SHUTDOWN						
$T_{J(SD)}$	Thermal shutdown threshold (1)	Temperature rising	150	170		°C
$T_{J(HYS)}$	Thermal shutdown hysteresis (1)			13		°C
OUTPUT DISCHARGE						
	Output discharge resistor on SW pin	V_{IN} = 12V, V_{SW} = 1V, power conversion disabled		100		Ω

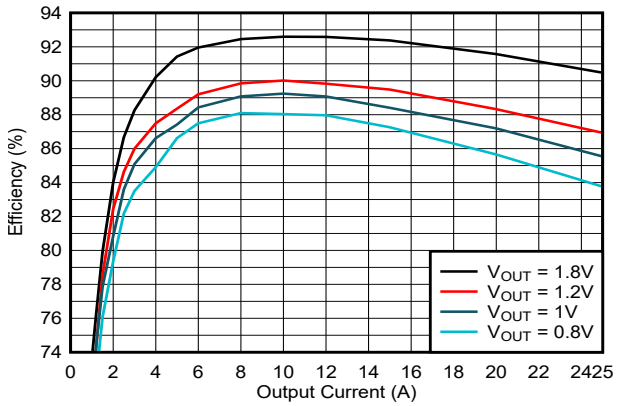
(1) This parameter is provided for reference only, and do not consitute part of TI's published device specifications for purpose of TI's product warranty.

5.6 Typical Characteristics



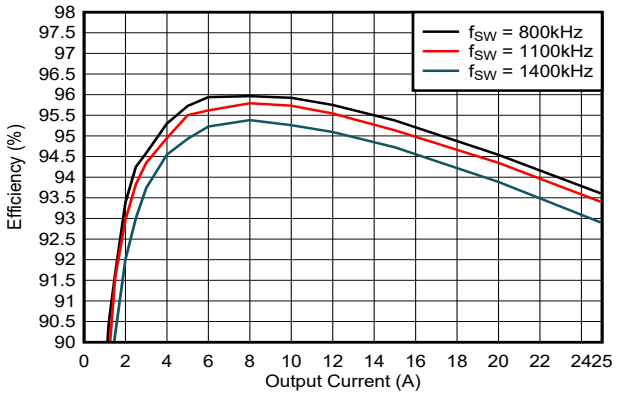
V_{IN} = 12V V_{VCC} = 3V internal f_{SW} = 800kHz
L_{OUT} = 470nH DCR = 1.35mΩ FCCM

図 5-1. Efficiency With V_{OUT} ≥ 1.8V



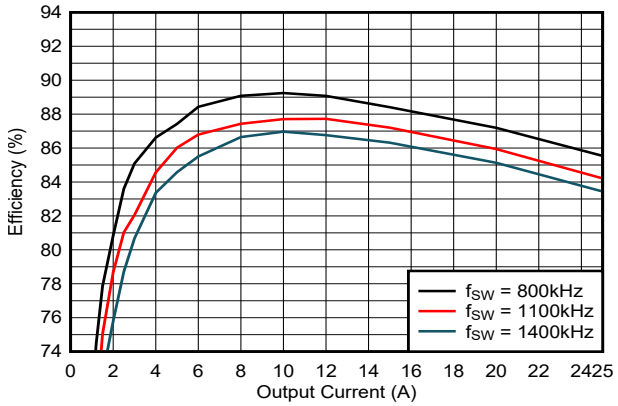
V_{IN} = 12V V_{VCC} = 3V internal f_{SW} = 800kHz
L_{OUT} = 150nH DCR = 0.15mΩ FCCM

図 5-2. Efficiency With V_{OUT} ≤ 1.8V



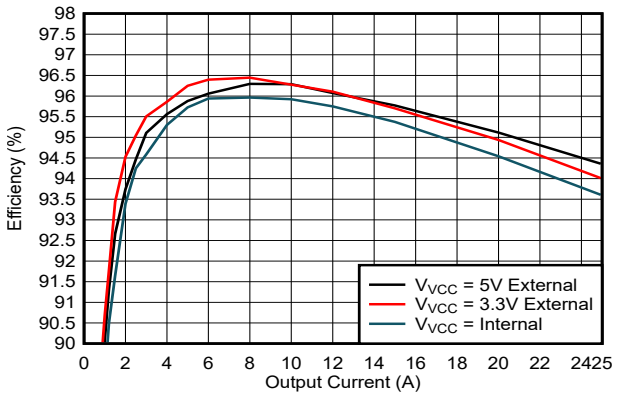
V_{IN} = 12V V_{VCC} = 3V internal V_{OUT} = 3.3V
L_{OUT} = 470nH DCR = 1.35mΩ FCCM

図 5-3. Efficiency versus f_{SW} With V_{OUT} = 3.3V



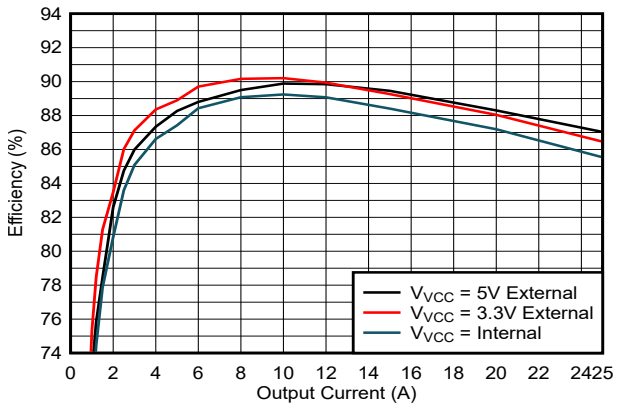
V_{IN} = 12V V_{VCC} = 3V internal V_{OUT} = 1.0V
L_{OUT} = 150nH DCR = 0.15mΩ FCCM

図 5-4. Efficiency versus f_{SW} With V_{OUT} = 1.0V



V_{IN} = 12V V_{OUT} = 3.3V f_{SW} = 800kHz
L_{OUT} = 470nH DCR = 1.35mΩ FCCM

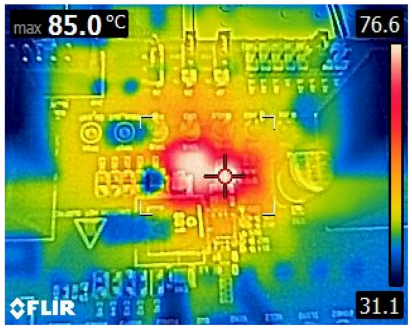
図 5-5. Efficiency versus VCC Bias With V_{OUT} = 3.3V



V_{IN} = 12V V_{OUT} = 1.0V f_{SW} = 800kHz
L_{OUT} = 150nH DCR = 0.15mΩ FCCM

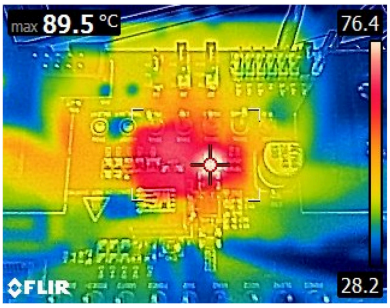
図 5-6. Efficiency versus VCC Bias With V_{OUT} = 1.0V

5.6 Typical Characteristics (continued)



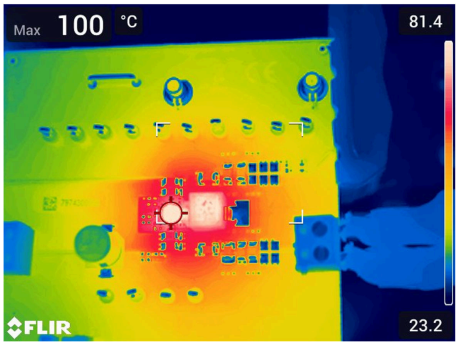
V_{IN} = 12V V_{VCC} = 3V internal I_{OUT} = 20A
L_{OUT} = 800nH f_{SW} = 800kHz

図 5-7. Thermal Image – 5V Output, TPS54KB20EVM, 6 Layers



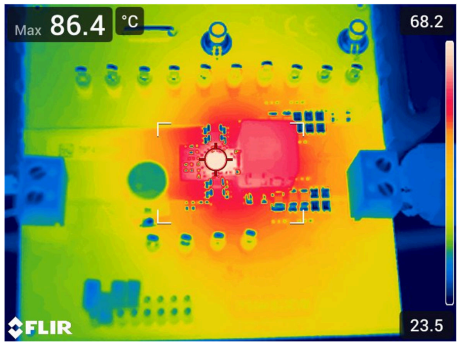
V_{IN} = 12V V_{VCC} = 3V internal I_{OUT} = 25A
L_{OUT} = 470nH f_{SW} = 800kHz

図 5-8. Thermal Image – 3.3V Output, TPS54KB20EVM, 6 Layers



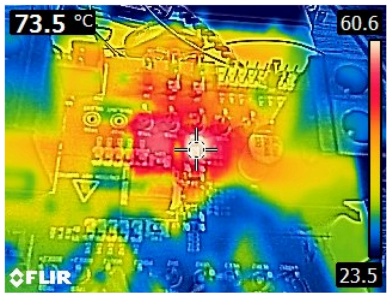
V_{IN} = 12V V_{VCC} = 3V internal I_{OUT} = 20A
L_{OUT} = 800nH f_{SW} = 800kHz

図 5-9. Thermal Image – 5V Output, 3 Inch × 3 Inch, 4 Layers



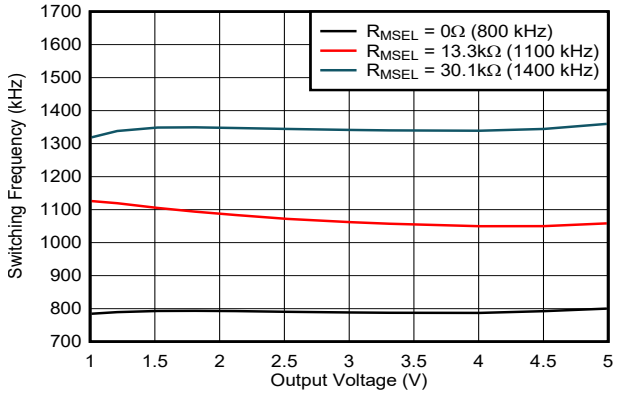
V_{IN} = 12V V_{VCC} = 3V internal I_{OUT} = 20A
L_{OUT} = 470nH f_{SW} = 800kHz

図 5-10. Thermal Image – 3.3V Output, 3 Inch × 3 Inch, 4 Layers



V_{IN} = 12V V_{VCC} = 3V internal I_{OUT} = 25A
L_{OUT} = 150nH f_{SW} = 1100kHz

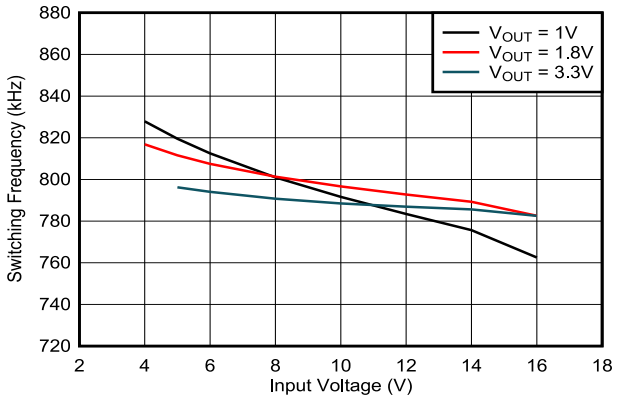
図 5-11. Thermal Image – 1V Output, TPS54KB20EVM, 6 Layers



V_{IN} = 12V V_{VCC} = 3V internal I_{OUT} = 5A
L_{OUT} = 470nH

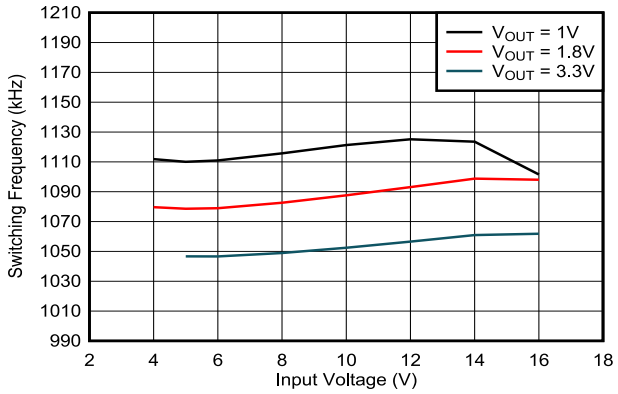
図 5-12. Switching Frequency versus Output Voltage

5.6 Typical Characteristics (continued)



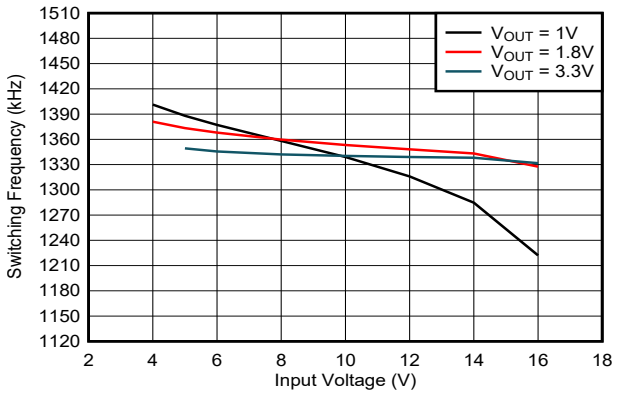
LOUT = 470nH VVCC = 3V internal IOUT = 5A

図 5-13. 800kHz Switching Frequency versus Input Voltage



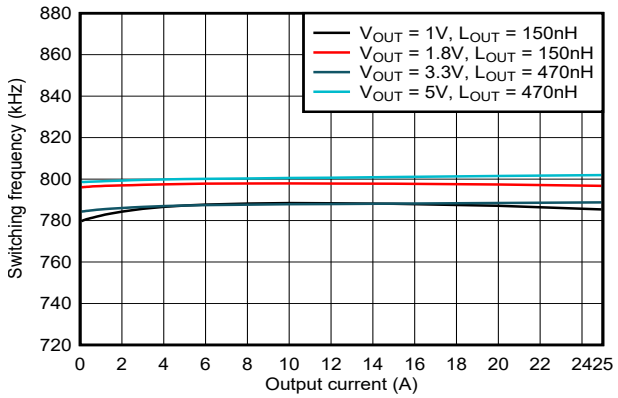
LOUT = 470nH VVCC = 3V internal IOUT = 5A

図 5-14. 1100kHz Switching Frequency versus Input Voltage



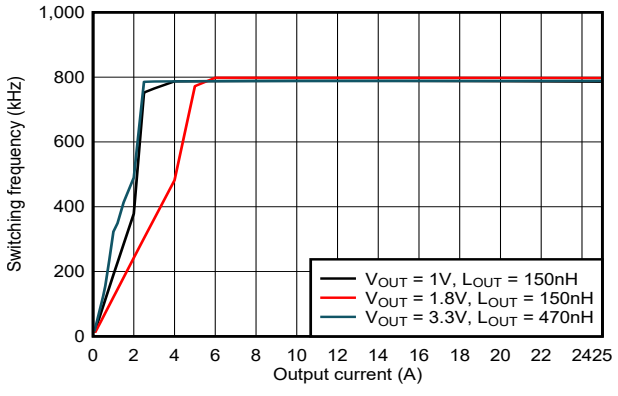
LOUT = 470nH VVCC = 3V internal IOUT = 5A

図 5-15. 1400kHz Switching Frequency versus Input Voltage



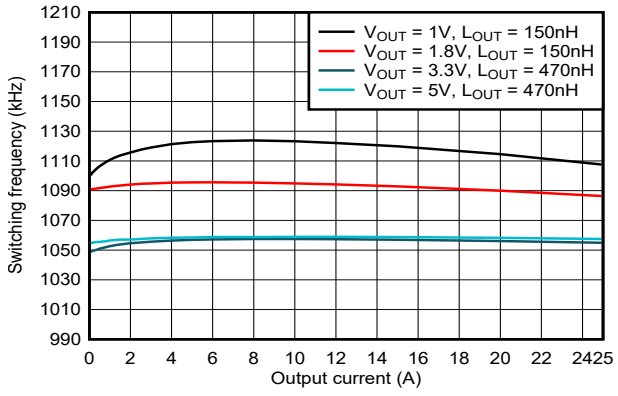
VIN = 12V VVCC = 3V internal FCCM

図 5-16. 800kHz FCCM Switching Frequency versus Output Current



VIN = 12V VVCC = 3V internal Skip-mode

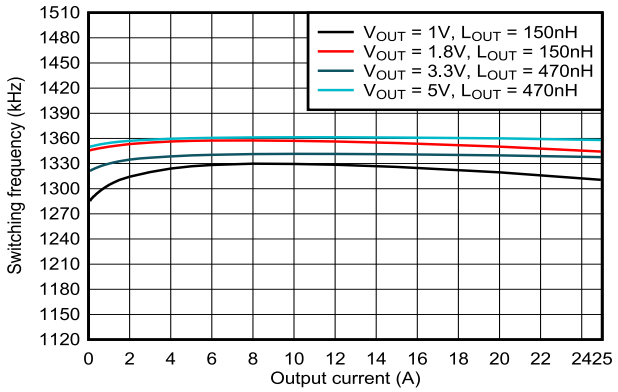
図 5-17. 800kHz Skip-mode Switching Frequency versus Output Current



VIN = 12V VVCC = 3V internal FCCM

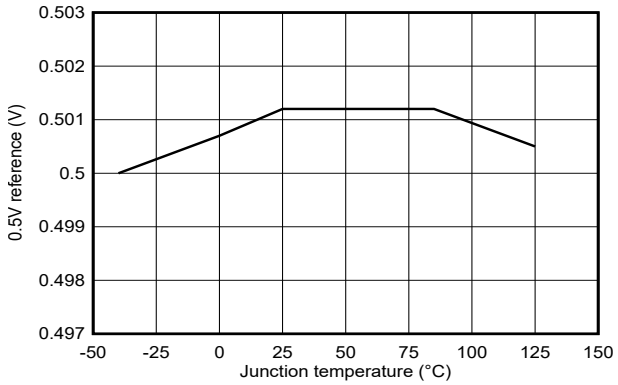
図 5-18. 1100kHz Switching Frequency versus Output Current

5.6 Typical Characteristics (continued)



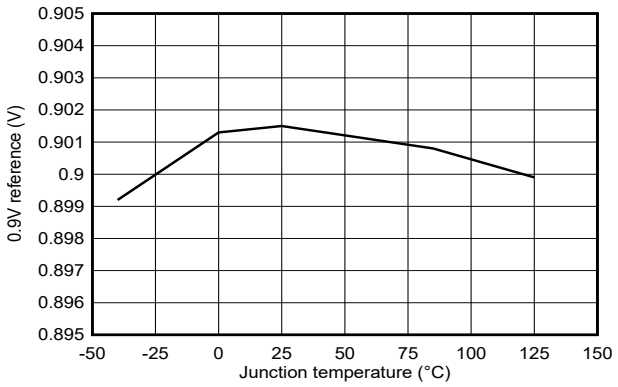
V_{IN} = 12V V_{VCC} = 3V internal FCCM

図 5-19. 1400kHz Switching Frequency versus Output Current



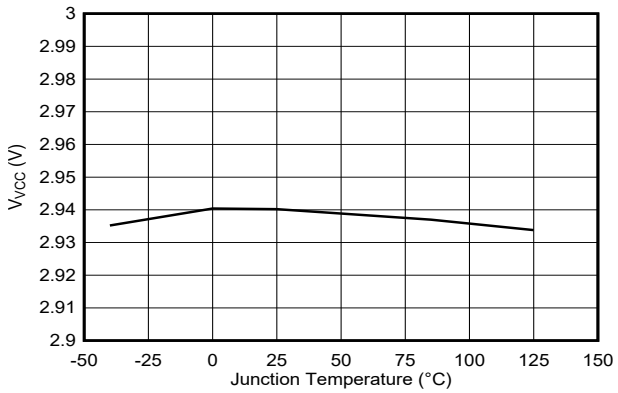
V_{IN} = 12V

図 5-20. 0.5V Reference Voltage versus Junction Temperature



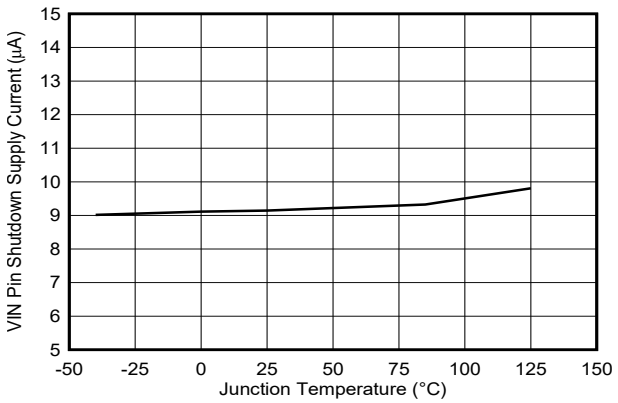
V_{IN} = 12V

図 5-21. 0.9V Reference Voltage versus Junction Temperature



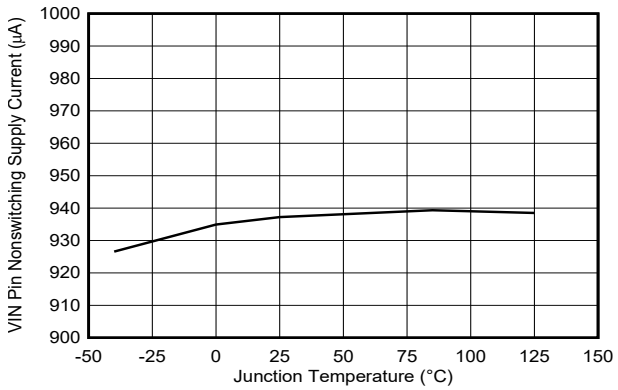
V_{IN} = 12V V_{EN} = 2V I_{VCC} = 25mA

図 5-22. VCC Pin Output Voltage versus Junction Temperature



V_{IN} = 12V V_{EN} = 0V No external VCC bias

図 5-23. VIN Pin Shutdown Quiescent Current versus Junction Temperature



V_{IN} = 12V V_{EN} = 2V No external VCC bias

V_{FB} = V_{REF} + 10mV

図 5-24. VIN Pin Nonswitching Quiescent Current versus Junction Temperature

5.6 Typical Characteristics (continued)

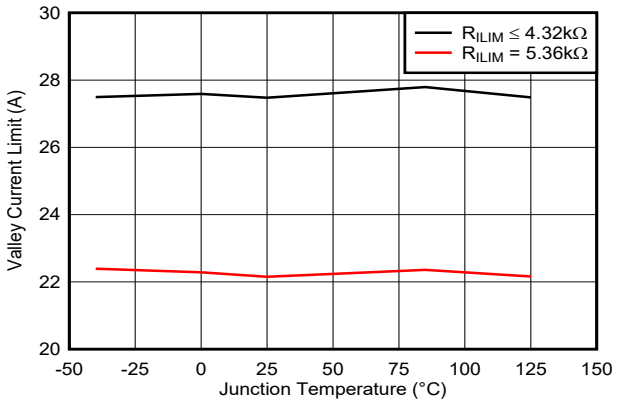


図 5-25. Valley Current Limit versus Junction Temperature (Low R_{ILIM})

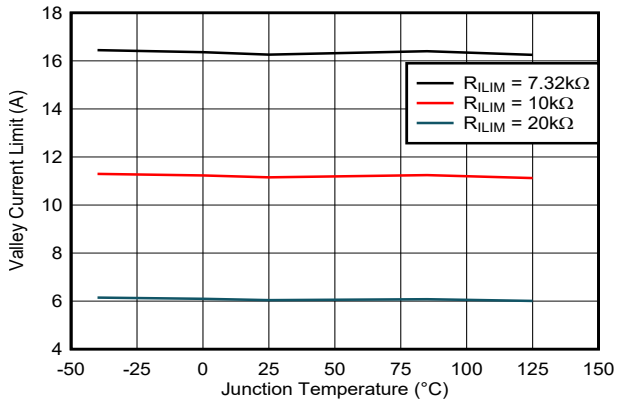


図 5-26. Valley Current Limit versus Junction Temperature (High R_{ILIM})

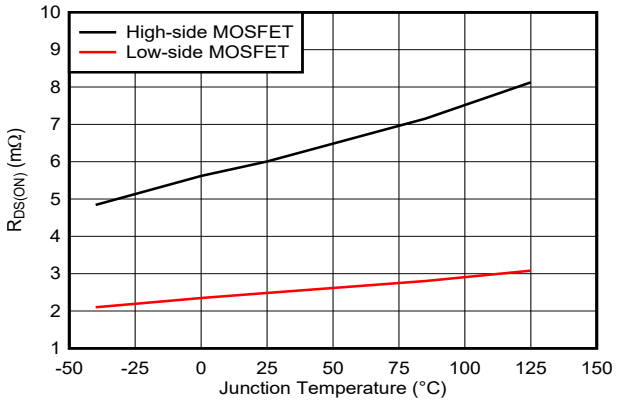


図 5-27. MOSFET $R_{DS(ON)}$ versus Junction Temperature

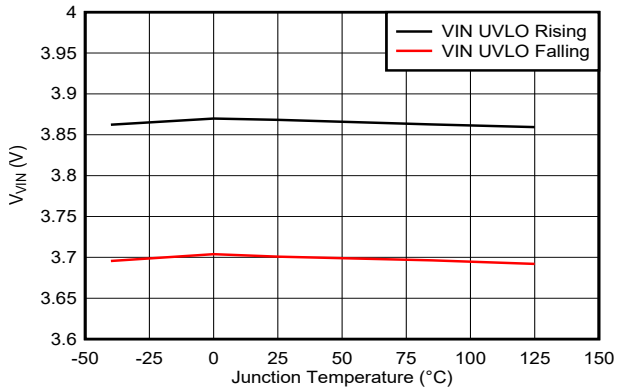


図 5-28. VIN Pin Undervoltage Lockout versus Junction Temperature

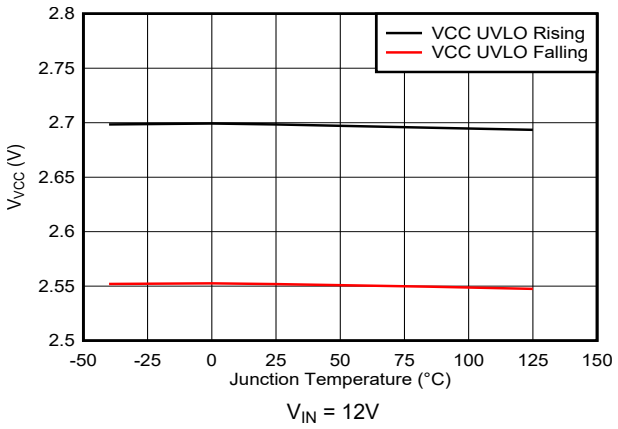


図 5-29. VCC Pin Undervoltage Lockout versus Junction Temperature

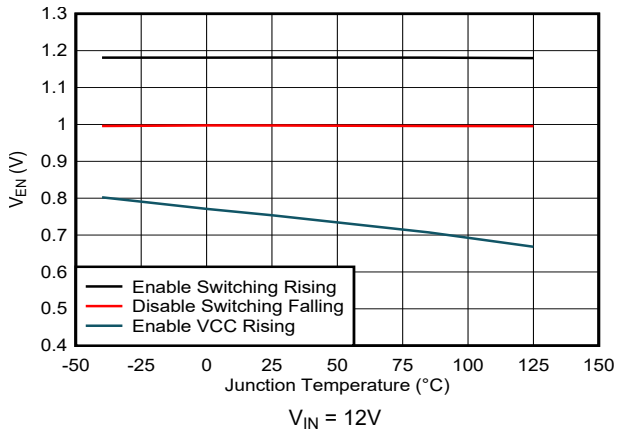


図 5-30. EN Pin Thresholds versus Junction Temperature

5.6 Typical Characteristics (continued)

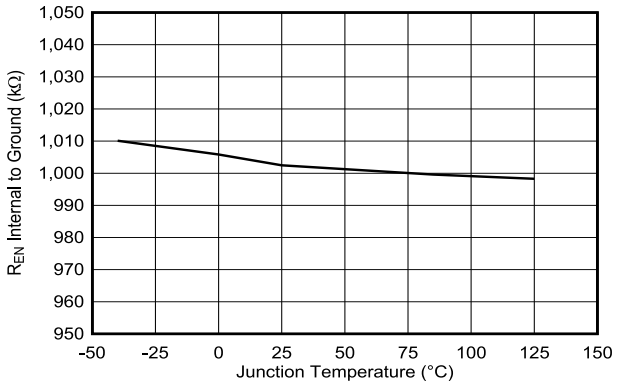


図 5-31. EN Pin Internal Resistance to Ground versus Junction Temperature

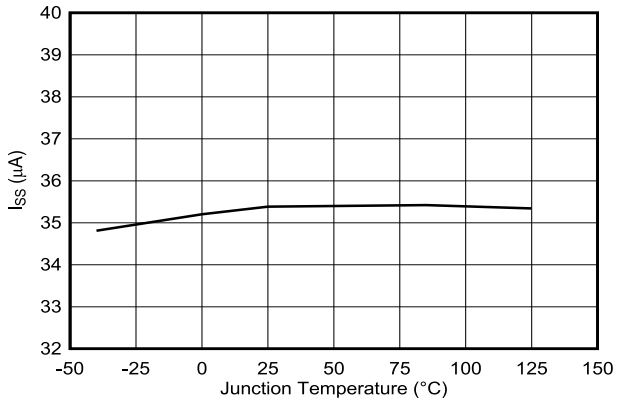


図 5-32. SS Pin Output Current versus Junction Temperature

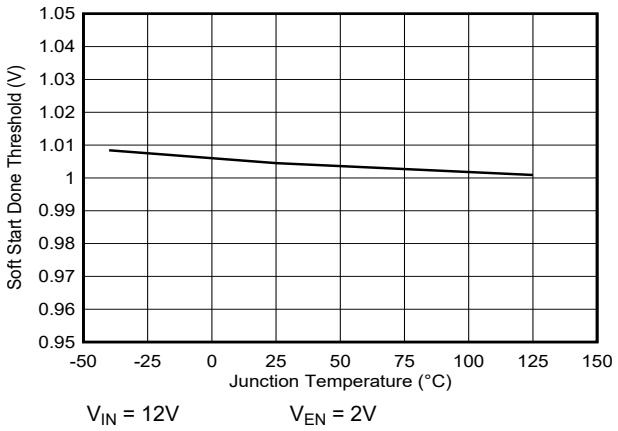


図 5-33. Soft-Start Done Voltage Threshold versus Junction Temperature (V_{REF} = 0.5V)

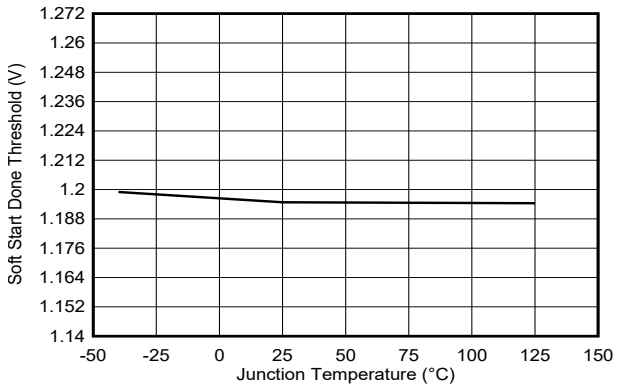


図 5-34. Soft-Start Done Voltage Threshold versus Junction Temperature (V_{REF} = 0.9V)

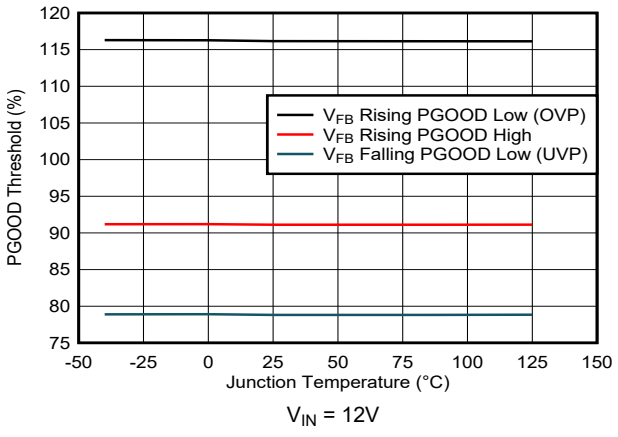


図 5-35. Power-Good Thresholds versus Junction Temperature (V_{REF} = 0.5V)

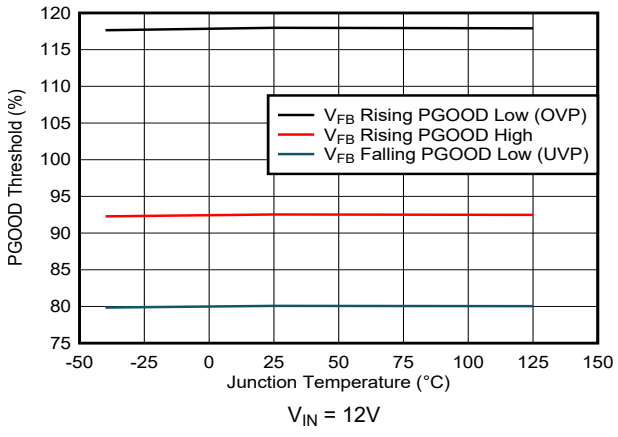
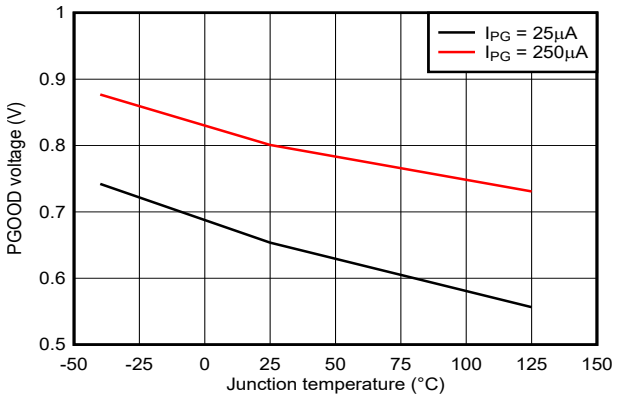


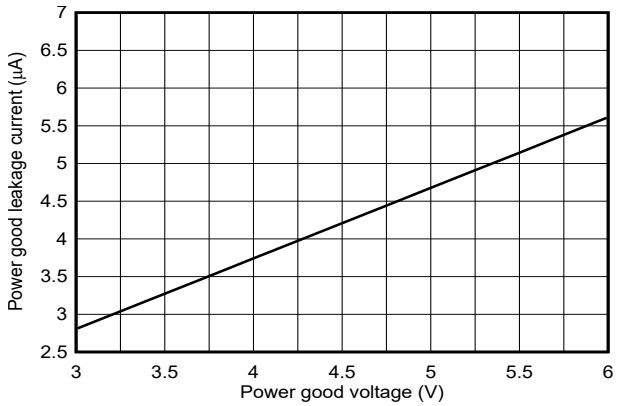
図 5-36. Power-Good Thresholds versus Junction Temperature (V_{REF} = 0.9V)

5.6 Typical Characteristics (continued)



V_{IN} = 0V V_{VCC} = 0V V_{EN} = 0V

図 5-37. Power-Good Clamp Voltage versus Junction Temperature



V_{IN} = 12V V_{EN} = 3V V_{FB} = V_{REF} + 10mV

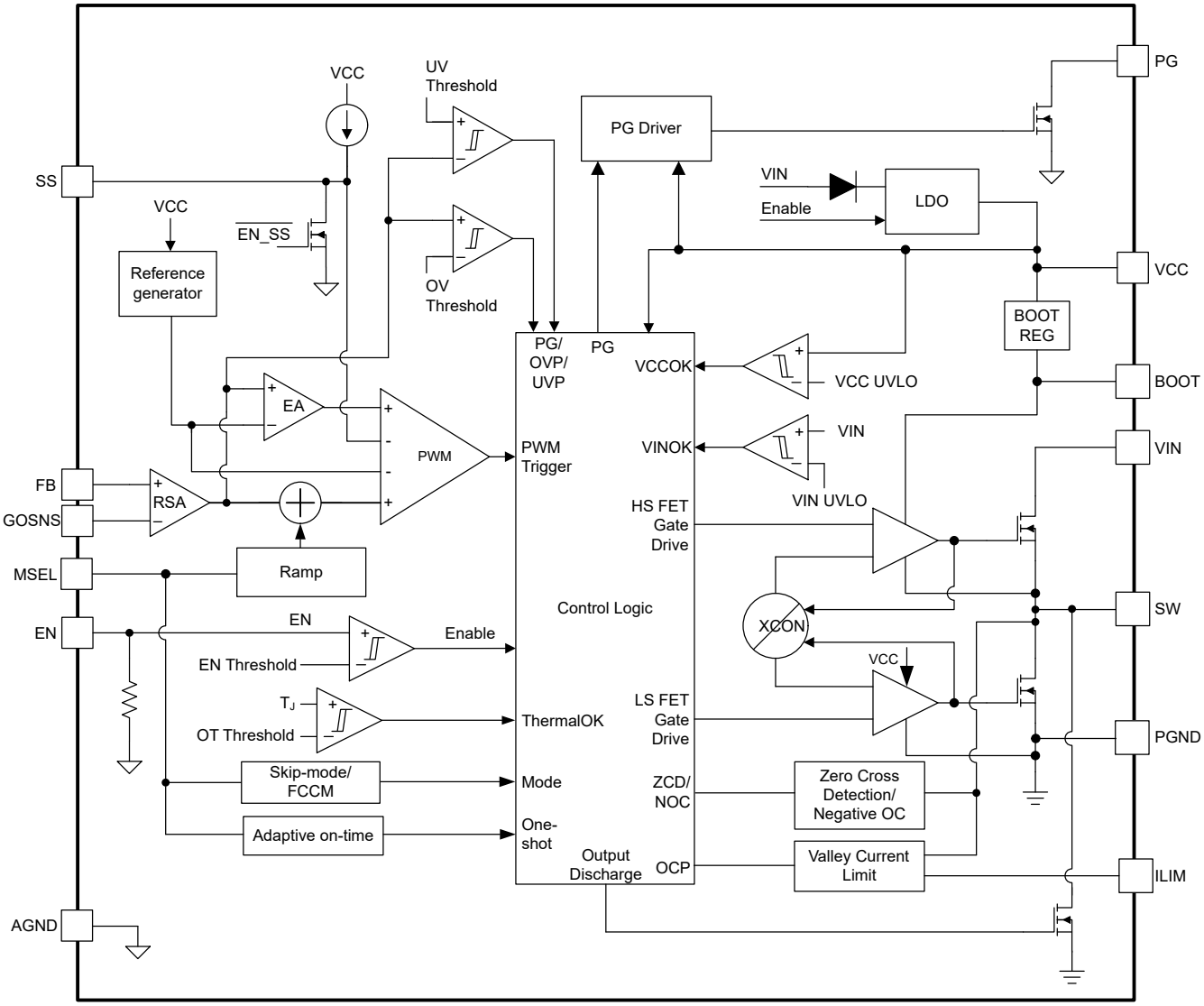
図 5-38. Power-Good Leakage Current versus Power-Good Voltage

6 Detailed Description

6.1 Overview

The TPS54KB2x device is a high-efficiency, single-channel, small-sized, synchronous buck converter. The device is designed for low output voltage point-of-load applications with 25A or lower output current in server, storage, and similar computing applications. The TPS54KB2x features proprietary D-CAP4 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an excellent fashion. The output voltage set by the feedback voltage divider ranges from the internal voltage reference to 5.5V. The conversion input voltage ranges from 4V to 16V, and the VCC input voltage ranges from 3.1V to 5.3V. The D-CAP4 modulator uses emulated current information to control the modulation. The D-CAP4 modulator reduces loop gain variation with different output voltages providing better transient response in higher output voltage applications. An advantage of this control scheme is that this control scheme does not require a phase-compensation network outside which makes the device easy-to-use and also allows low external component count. Another advantage of this control scheme is that this control scheme supports stable operation with all low ESR output capacitors (such as ceramic capacitors and low ESR polymer capacitors). Lastly, adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during load-step transients.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Internal VCC LDO and Using External Bias On the VCC Pin

The TPS54KB2x has an internal 3.0V LDO featuring input from VIN and output to VCC. When the EN voltage rises above the enable threshold ($V_{EN(R)}$), the internal LDO is enabled and starts regulating output voltage on the VCC pin. The VCC voltage provides the bias voltage for the internal analog circuitry and also provides the supply voltage for the gate drivers.

Bypass the VCC pin with a 1µF, at least 6.3V rating ceramic capacitor. An external bias that is above the output voltage of the internal LDO can override the internal LDO. This action enhances the efficiency of the converter because the VCC current now runs off this external bias instead of the internal linear regulator. An external bias of 5.0V can be used to provide additional efficiency enhancement by reducing the R_{DSON} of the integrated power MOSFETs.

The VCC UVLO circuit monitors the VCC pin voltage and disables the whole converter when VCC falls below the VCC UVLO falling threshold. Maintaining a stable and clean VCC voltage is required for a smooth operation of the device.

Considerations when using an external bias on the VCC pin are as follows:

- When the external bias is applied on the VCC pin early enough (for example, before EN signal comes in), the internal LDO pass device is always off and the internal analog circuits have a stable power supply rail at the power enable.
- (Not recommended) When the external bias is applied on the VCC pin late (for example, after EN signal comes in), any power-up and power-down sequencing can be applied as long as there is no excess current pulled out of the VCC pin. With this sequence, be cautious of external discharge paths on the VCC pin which can pull a current higher than the current limit of the internal VCC LDO. A load exceeding the current limit of the internal VCC LDO can potentially pull the VCC voltage low and turn off the VCC LDO through the UVLO, thereby shutting down the converter output.
- A good power-up sequence is when at least one of VIN UVLO rising threshold or EN rising threshold is satisfied later than VCC UVLO rising threshold. For example, a practical power-up sequence is: VIN applied first, then the external bias applied, and then the EN signal goes high.

6.3.2 Enable

When the EN pin voltage rises above the enable threshold voltage ($V_{EN(R)}$) and VIN rises above the VIN UVLO rising threshold, the device enters the internal power-up sequence. The EN to start of switching delay is specified in the STARTUP section of the *Electrical Characterisitcs* table.

The EN pin has an internal filter to avoid unexpected ON or OFF due to small glitches. The time constant of this RC filter is 2µs. For example, when applying 3.3V voltage source on the EN pin that jumps from 0V to 3.3V with an excellent rising edge, the internal EN signal reaches 2.1V after 2µs, which is 63.2% of applied 3.3V voltage level.

An internal pulldown resistor is implemented between the EN pin and AGND pin. With this pulldown resistor, floating the EN pin before start-up keeps the device in the disabled state. A resistor divider to the EN pin can be used to increase the input voltage the device begins the start-up sequence. The internal pulldown resistor must be accounted for when using an external resistor divider. To reduce impact to the EN rising and falling threshold, this internal pulldown resistor is 1MΩ. During nominal operation when the power stage switches, this large internal pulldown resistor can not have enough noise immunity to hold EN pin low for the device to enter the disabled state.

The recommended operating condition for the EN pin is a maximum of 5.5V. *Do not* connect the EN pin to the VIN pin directly if VIN can exceed 5.5V.

6.3.3 Adjustable Soft Start

The device implements an externally adjustable soft start set by the external soft-start capacitor (C_{SS}) connected between the SS and AGND pins. The SS pin has a 36µA internal pullup current source (I_{SS}) that charges C_{SS}. The FB voltage follows the SS pin voltage with a small offset. When the SS pin voltage is near the internal reference voltage, a smooth transition occurs to FB being regulated to the internal reference. The device soft-start period is complete when the SS pin voltage reaches $V_{SS(DONE)}$ given in the *Electrical Characteristics* table.

The C_{SS} value can be determined by 式 1. The soft-start capacitor must be in the range of 10nF to 1µF. TI does not recommend leaving the SS pin open. The soft-start time is typically selected to either satisfy timing requirements in the system or to minimize inrush current to charge the output capacitors during start-up.

$$C_{SS} = \frac{t_{SS} \times I_{SS}}{V_{FB\_REG}} \quad (1)$$

If during normal operation VIN goes below the UVLO, VCC goes below the UVLO, the EN pin is pulled below the $V_{EN(F)}$ threshold, the output turns off due to under voltage protection or a thermal shutdown event occurs, the device stops switching and an internal discharge path is enabled to discharge the SS pin capacitance. This internal discharge path remains active as long as there is sufficient VCC to enable the path, typically 1.5V. The internal discharge path is disabled when the device enters the soft-start period during power up.

C_{SS} also sets the hiccup wait-time before a restart attempt for the TPS54KB22 および TPS54KB23 devices. After a fault triggers the hiccup response the soft-start capacitor is discharged through the internal discharge path, then recharged with the internal pullup current source to $V_{SS(DONE)}$ seven times. This response sets the hiccup wait time to $7 \times t_{SS}$. 図 6-1 shows the device entering hiccup due to an output short circuit and 図 6-2 shows the device exiting hiccup after the output short has been removed.

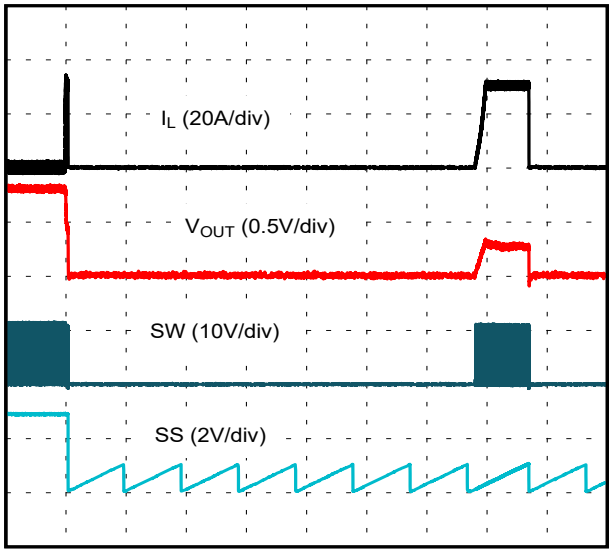


図 6-1. Entering Hiccup

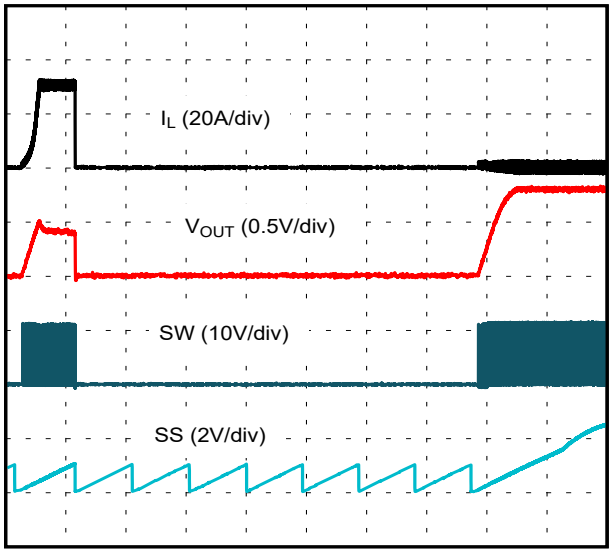


図 6-2. Exiting Hiccup

6.3.4 Power Good

The device has a power-good (PG or PGOOD) output that goes high to indicate when the converter output is in regulation. The power-good output is an open-drain output and must be pulled up to the VCC pin or an external voltage source (< 5.5V) through a pullup resistor to go high. The recommended power-good pullup resistor value is 1kΩ to 100kΩ.

After the soft-start ramp finishes, the power-good signal becomes high after a 1.3ms internal delay. An internal soft-start done signal goes high when the SS pin voltage reaches $V_{SS(DONE)}$ to indicate the soft-start ramp has finished. If the FB voltage drops to 80% of the V_{REF} voltage or exceeds 118% of the V_{REF} voltage, the power-good signal latches low after a 4µs internal delay. The power-good signal can only be pulled high again after re-toggling EN or a reset of VIN. The PGOOD thresholds given are for the 0.9V reference devices and vary slightly with the 0.5V reference devices. Refer to セクション 5 for more detailed specifications.

If an OV event causes the FB voltage to exceed the OV threshold during soft start, but the FB voltage drops below the OV threshold before soft start is completed, the power-good signal is not latched low. Power good pulls low if FB exceeds the OV threshold again or drops below the UV threshold, but does not latch low until after the soft-start ramp finishes. FB exceeding the OV threshold during soft start does however trigger the OV fault response, and the device response to OV typically pulls the output voltage below the UV threshold. The OV fault response is described in セクション 6.3.12.

If the input supply fails to power up the device (for example VIN and VCC both stay at zero volts) and this pin is pulled up through an external resistor, the power-good pin clamps low to the low-level specified in the POWER GOOD section in the *Electrical Characteristics*.

6.3.5 Output Voltage Setting

The output voltage is programmed by the voltage-divider resistors, R_{FB_T} and R_{FB_B}. Connect R_{FB_T} between the FB pin and the positive node of the load, and connect R_{FB_B} between the FB pin and GOSNS pin. The FB pin is regulated to the internal reference (V_{REF}). The recommended R_{FB_B} value is 10kΩ, ranging from 1kΩ to 15kΩ. Determine R_{FB_T} by using 式 2. The maximum R_{FB_B} is primarily limited by leakage current out of the SW pins. A larger R_{FB_B} is allowed if a minimum output load can be provided in the application to sink this leakage current.

$$R_{FB\_T} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FB\_B} \quad (2)$$

To improve the overall V_{OUT} accuracy, TI highly recommends using a ±1% accuracy or better resistor for the FB voltage divider. Regardless of remote sensing or single-ended sensing, always place the FB voltage divider, R_{FB_T} and R_{FB_B}, as close as possible to the device.

6.3.6 Remote Sense

The device integrates a remote sense amplifier across the FB and GOSNS pins. The remote sense function compensates for voltage drop on the PCB traces helping to maintain V_{OUT} accuracy under steady state operation and load transient events. The V_{OUT} connection of the remote sensing signal must be connected to the feedback resistor divider with the lower feedback resistor, R_{FB_B}, terminated at the GOSNS pin.

The FB voltage divider resistors must be kept near the device to minimize the trace length connected to the FB pin. The connections from the FB voltage divider resistors and the GOSNS pin to the remote location must be a pair of PCB traces with Kelvin sensing across a bypass capacitor of 0.1µF or higher. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below.

Single-ended V_{OUT} sensing can also be used for local sensing. For this configuration connect the higher FB resistor R_{FB_T} to a high-frequency local bypass capacitor of 0.1µF or higher, and short GOSNS to AGND.

The recommended GOSNS operating range (relative to the AGND pin) is –100mV to +100mV.

6.3.7 D-CAP4 Control

The device uses D-CAP4 control to achieve a fast load transient response while maintaining ease-of-use. The D-CAP4 control architecture includes an internal ripple generation network enabling the use of very low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC) and low ESR polymer capacitors. No external current sensing network or voltage compensators are required with D-CAP4 control architecture. The role of the internal ripple generation network is to emulate the ripple component of the inductor current information and then combine with the voltage feedback signal to regulate the loop operation.

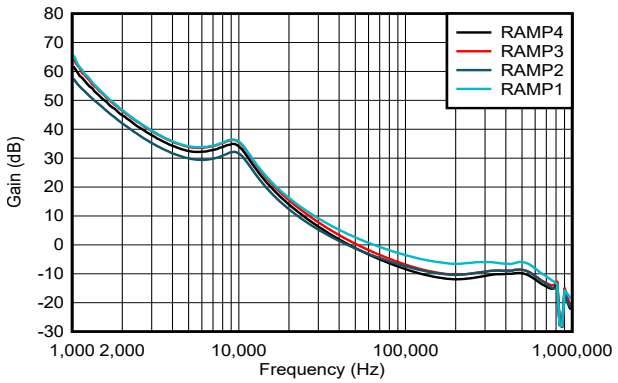
D-CAP4 control architecture reduces loop gain variation across V_{OUT}, enabling a fast load transient response across the entire output voltage range with one ramp setting. The R-C time-constant of the internal ramp circuit sets the zero frequency of the ramp, similar to other R-C based internal ramp generation architectures. The reduced variation in loop gain also mitigates the need for a feedforward capacitor to optimize the transient response. The ramp amplitude varies with V_{IN} to minimize variation in loop gain across input voltage, commonly referred to as input voltage feedforward. Lastly, the device uses internal circuitry to correct for the dc offset caused by the injected ramp, and removes the dc offset caused by the output ripple voltage, especially with light load current when skip mode operation is selected.

表 6-1 gives details on the different ramp settings selectable through the MSEL resistor value described in 表 6-4. The effective ramp amplitudes are given relative to VREF = 0.9V, RAMP1. The VREF = 0.5V ramp amplitudes include the change in gain due to a larger division ratio needed for the FB divider with the lower reference voltage.

表 6-1. Selectable Ramp Amplitudes

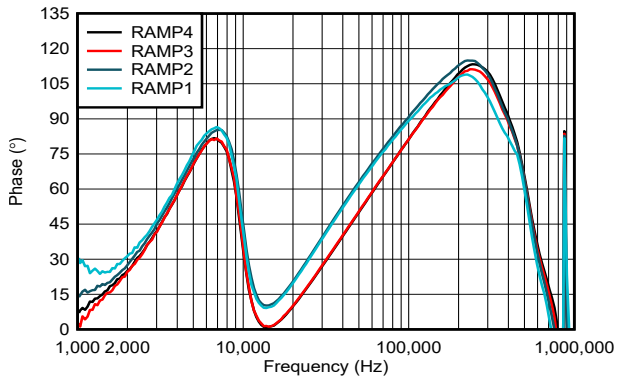
Ramp	Relative Effective Ramp Amplitude		Zero Location (kHz)
	VREF = 0.9V	VREF = 0.5V	
RAMP1	1×	1.2×	32
RAMP2	1.8×	2.3×	32
RAMP3	1.6×	2.1×	53
RAMP4	2.1×	3.8×	53

RAMP2 and RAMP3 result in similar loop bandwidth as the ramp amplitudes are similar. The primary difference between these two settings is the ramp zero frequency. The lower ramp zero location for RAMP2 increases phase margin. However, RAMP3 provides faster transient response than RAMP2 because RAMP3 gives higher gain across the entire frequency range due to smaller ramp amplitude and higher ramp zero location. For most applications, RAMP3 must be used instead of RAMP2. RAMP2 can be used to provide phase boost in applications using an L-C whose double pole frequency allows using RAMP1 but where minimizing jitter is more important than faster transient response. 図 6-3 and 図 6-4 show how the loop characteristics changes with the different ramp settings for devices with a 0.9V reference. 図 6-5 and 図 6-6 show how the loop characteristics changes with the different ramp settings for devices with a 0.5V reference.



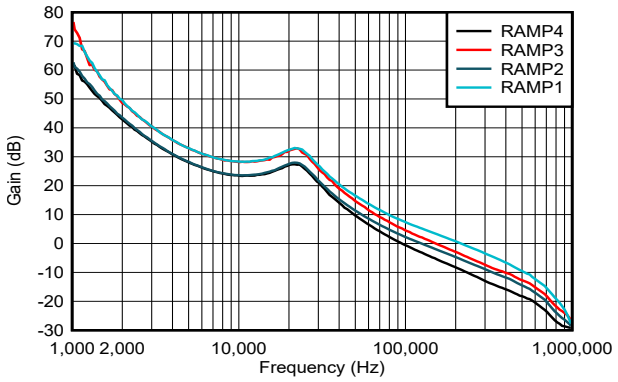
V_{IN} = 12V
Load = 250mΩ
f_{SW} = 800kHz
L_{OUT} = 470nH
V_{OUT} = 3.3V
C_{OUT} = 7 × 22µF + 2 × 220µF

図 6-3. Gain versus Ramp Setting - VREF = 0.9V



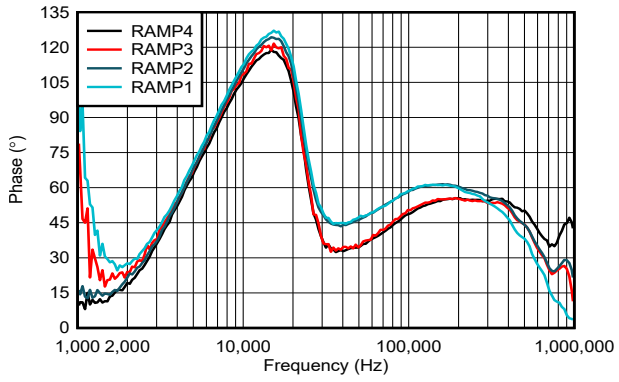
V_{IN} = 12V
Load = 250mΩ
f_{SW} = 800kHz
L_{OUT} = 470nH
V_{OUT} = 3.3V
C_{OUT} = 7 × 22µF + 2 × 220µF

図 6-4. Phase versus Ramp Setting - VREF = 0.9V



V_{IN} = 12V
Load = 50mΩ
f_{SW} = 1100kHz
L_{OUT} = 150nH
V_{OUT} = 0.8V
C_{OUT} = 12 × 47µF

図 6-5. Gain versus Ramp Setting - VREF = 0.5V



V_{IN} = 12V
Load = 50mΩ
f_{SW} = 1100kHz
L_{OUT} = 150nH
V_{OUT} = 0.8V
C_{OUT} = 12 × 47µF

図 6-6. Phase versus Ramp Setting - VREF = 0.5V

For any control topologies supporting no external compensation, there is a minimum range, maximum range, or both, for the output filter the control topologies can support. The output filter used for a typical buck converter is a low-pass L-C circuit. This L-C filter has double pole that is described in 式 3.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (3)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency L-C double pole has a 180-degree drop in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade. The zero also increases the phase by 45 degrees at the zero frequency and by 90 degrees at a decade above the zero frequency.

The inductor and capacitor selected for the output filter must be such that the f_P double pole of 式 3 is located no higher than the value given in 表 6-2 for VREF = 0.9V and 表 6-3 for VREF = 0.5V, then adjusted based on the nominal duty cycle in the application using 式 4. 式 4 scales up the $f_{P(TABLE)}$ because, as the duty cycle increases the gain of the D-CAP4 ramp decreases, so the maximum L-C double pole also increases.

$$f_{P(MAX)} = f_{P(TABLE)} \times \left(1 + \left(\frac{V_{OUT}}{V_{IN(typ)}}\right)^2\right) \quad (4)$$

表 6-2. 0.9V reference maximum L-C double pole

Switching frequency (kHz)	Maximum L-C Double Pole Frequency (kHz)		
	RAMP1	RAMP2 and RAMP3	RAMP4
800	14.0	18.3	20.3
1100	19.3	25.1	27.9
1400	24.5	31.9	35.5

表 6-3. 0.5V reference maximum L-C double pole

Switching Frequency (kHz)	Maximum L-C Double Pole Frequency (kHz)		
	RAMP1	RAMP2 and RAMP3	RAMP4
800	15.3	19.9	26.5
1100	21.0	27.4	36.4
1400	26.8	34.9	46.4

An L-C double pole frequency that violates these guidelines for each ramp setting can be possible, but must be validated in the application with measurements. Choosing very small output capacitance leads to a high frequency L-C double pole which causes the overall loop gain to stay high until the L-C double pole frequency. Given the zero from the internal ripple generation network is a relatively high frequency as well, the loop with very small output capacitance can have too high of a crossover frequency which can cause instability. In general, where reasonable (or smaller) output capacitance is desired, output ripple requirement and load transient requirement can be used to determine the necessary output capacitance for stable operation. The internal zero is selected by the resistor at the MSEL pin, as described earlier.

If MLCCs are used, consider the derating characteristics to determine the *effective* output capacitance for the design when calculating the L-C double pole frequency. For example, when using an MLCC with specifications of 10µF, X5R and 6.3V, the derating by DC bias and AC bias are 80% and 50%, respectively. The effective derating is the product of these two factors, which in this case is 40% and 4µF. Consult with capacitor manufacturers for specific characteristics of the capacitors to be used in the application.

As a simplified rule, if an output capacitor with an ESR zero that is less than 10× the L-C double pole frequency, TI recommends to ignore when calculating the L-C double pole frequency for stability purposes. The L-C double pole frequency must be recalculated using only the low ESR MLCCs. For more accurate analysis when using mixed type output capacitors, TI recommends simulations or measurements.

For the maximum output capacitance recommendation, select the inductor and capacitor values so that the L-C double pole frequency is no less than 1/100th of the operating frequency. With this starting point, verify the small signal response on the board using the following criteria: The phase margin at the loop crossover is greater than 50 degrees. The actual maximum output capacitance can go higher as long as phase margin is greater than 50 degrees. However, a small signal measurement (Bode plot) must be done to confirm the design.

If requiring an L-C double pole frequency <1/50th the operating frequency, TI recommends using a mixed type output capacitor to achieve the desired effective capacitance. In addition to providing higher density of capacitance, a bulk capacitor with higher ESR also provides phase boost at the L-C double pole frequency. If only low ESR MLCC capacitors are used with an L-C double pole frequency <1/50th the operating frequency, a feedfoward capacitor (C_{FF}) can be added to provide a zero at 10× the L-C double pole frequency. Besides boosting the phase, a C_{FF} feeds more V_{OUT} node information into the FB node through AC coupling. This feedforward during load transient event enables faster response of the control loop to a V_{OUT} deviation. However, this feedforward during steady state operation also feeds more V_{OUT} ripple and noise into FB. High ripple and noise on FB usually leads to more jitter, or even double-pulse behavior. To determine the final C_{FF} value, impacts to loop stability, load transient performance, ripple, and noise on FB must all be considered. TI recommends using frequency analysis equipment to measure the crossover frequency and the stability margin. In most applications, *a feedforward capacitor is typically not required* because the D-CAP4 architecture provides high loop bandwidth and adding a feedforward capacitor can result in low stability margin.

6.3.8 Multifunction Select (MSEL) Pin

The device provides Forced Continuous-Conduction Mode (FCCM) operation for tight output ripple applications and auto-skip Eco-mode for high light-load efficiency. The device allows users to select the switching frequency and operation mode by connecting a resistor from the MSEL pin to AGND pin. Additionally, the user can use the MSEL pin to select the internal ramp amplitude and ramp zero to optimize the control loop for fastest transient response. More details on the different ramp settings are given in セクション 6.3.7. 表 6-4 lists the resistor values for the switching frequency, operation mode, and ramp selection. A ±1% tolerance resistor with a typical temperature coefficient of ±100ppm/°C is required for accurate detection across the device operating range.

The MSEL state is set and latched during the internal power-on delay period. Changing the MSEL pin resistance after the power-on delay does not change the status of the device.

To make sure the internal circuit detects the resistor value correctly, *do not* place any capacitor on the MSEL pin.

表 6-4. MSEL Pin Selection

MSEL PIN RESISTANCE TO AGND (kΩ)	OPERATION MODE UNDER LIGHT LOAD	SWITCHING FREQUENCY (f_{SW}) (kHz)(1)	RAMP
0 (SHORT)	FCCM	800	RAMP4
4.99	FCCM	800	RAMP3
7.50	FCCM	800	RAMP2
10.5	FCCM	800	RAMP1
13.3	FCCM	1100	RAMP4
16.9	FCCM	1100	RAMP3
21.0	FCCM	1100	RAMP2
24.9	FCCM	1100	RAMP1
30.1	FCCM	1400	RAMP4
35.7	FCCM	1400	RAMP3
42.2	FCCM	1400	RAMP2
48.7	FCCM	1400	RAMP1
56.2	Skip-mode	800	RAMP4
64.9	Skip-mode	800	RAMP3
75.0	Skip-mode	800	RAMP2
86.6	Skip-mode	800	RAMP1
102	Skip-mode	1100	RAMP4
118	Skip-mode	1100	RAMP3
137	Skip-mode	1100	RAMP2
158	Skip-mode	1100	RAMP1
182	Skip-mode	1400	RAMP4
210	Skip-mode	1400	RAMP3
243	Skip-mode	1400	RAMP2
≥280 (FLOAT)	Skip-mode	1400	RAMP1

(1) Switching frequency varies across input voltage, output voltage, and load. See 図 5-12 through 図 5-19.

6.3.9 Low-side MOSFET Zero-Crossing

The device uses a zero-crossing (ZC) circuit to perform the zero inductor current detection during skip-mode operation. The ZC threshold is set to a small negative value before the low-side MOSFET is turned off, entering discontinuous conduction mode (DCM) operation. After entering DCM, the ZC threshold hysteresis increases the threshold to a small positive value. As a result, the device delivers better light-load efficiency.

When the load current increases enough such that the device exits DCM, the ZC circuit must detect 16 consecutive cycles of negative inductor current below the ZC threshold before returning to DCM. Only one cycle without ZC detection is required to exit DCM.

When the output is enabled, the ZC circuit is also enabled during the first 32 switching cycles while the device is in soft start. If the MSEL resistor value is for FCCM, ZC is disabled and the device transitions to FCCM when soft start is complete. See *Adjustable Soft Start* for description on soft-start completion. If there are not at least 32 switching cycles before soft start is done, such as during start-up with a high output prebias, the ZC is not disabled until the first high-side MOSFET on-time after soft-start done is complete.

6.3.10 Current Sense and Positive Overcurrent Protection

For a buck converter, during the on-time of the high-side MOSFET, the switch current increases at a linear rate determined by the input voltage, output voltage, on-time, and output inductor value. During the on-time of the low-side MOSFET, the current decreases linearly. The average value of the switch current equals the load current.

The output overcurrent limit (OCL) in the device is implemented using a cycle-by-cycle valley current detect control circuit. The inductor current is monitored during the on-time of the low-side MOSFET by measuring the low-side MOSFET drain-to-source current. If the measured drain-to-source current of the low-side MOSFET is above the current limit threshold, the low-side MOSFET stays ON until the current level becomes lower than the current limit threshold. This type of behavior reduces the average output current sourced by the device.

During an overcurrent condition, the current to the load exceeds the current to the output capacitors. Thus, the output voltage tends to decrease. Eventually, when the output voltage falls below the undervoltage-protection threshold (80%), the UVP comparator detects the fall and shuts down the device after a wait time of 70µs. Depending on the part number, the device either hiccups or latches off, as described in *Overvoltage and Undervoltage Protection*.

図 6-7 shows the cycle-by-cycle valley current limit behavior as well as the wait time before the device shuts down.

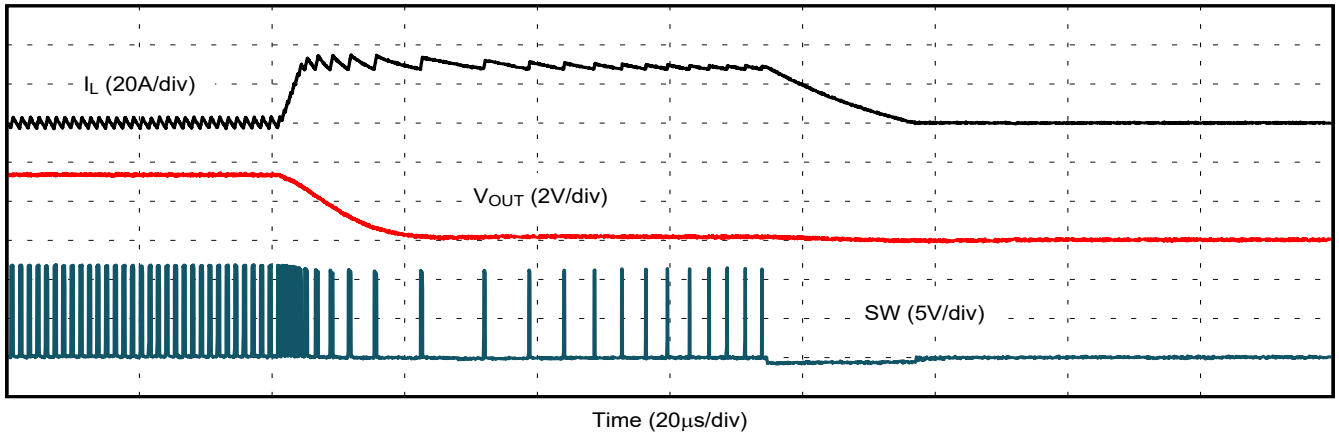


図 6-7. Overcurrent Protection

If an OCL condition happens during start-up, the device still has cycle-by-cycle current limit based on low-side valley current. After soft start is finished, the UV event which is caused by the OCL event shuts down the device

after a wait time of 70µs. Depending on the part number, the device either hiccups or latches off after the UV is tripped as described in *Overvoltage and Undervoltage Protection*.

The resistor, R_{ILIM} connected from the ILIM pin to AGND sets current limit threshold. TI recommends a ±1% tolerance resistor because a worse tolerance resistor provides less accurate OCL threshold. 式 5 calculates the R_{ILIM} for a given overcurrent limit threshold on the device. 式 6 calculates the overcurrent limit threshold for a given R_{ILIM} value.

To protect the device from an unexpected connection to the ILIM pin, an internal fixed OCL clamp is implemented. This internal OCL clamp limits the maximum valley current on the low-side MOSFET when the ILIM pin has too small of a resistance to AGND, or is accidentally shorted to ground. TI does not recommend designing with an R_{ILIM} < 4.32kΩ.

$$R_{ILIM} = \frac{K_{OCL}}{I_{OCLIM} - \frac{1}{2} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{L \times f_{SW}}} \quad (5)$$

where

- I_{OCLIM} is overcurrent limit threshold for load current in A
- R_{ILIM} is ILIM resistor value in Ω
- K_{OCL} is a constant of 120 × 10^3 for the calculation
- V_{IN} is input voltage value in V
- V_{OUT} is output voltage value in V
- L is output inductor value in µH
- f_{SW} is switching frequency in MHz

$$I_{OCLIM} = \frac{K_{OCL}}{R_{ILIM}} + \frac{1}{2} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \times \frac{1}{L \times f_{SW}} \quad (6)$$

6.3.11 Low-side MOSFET Negative Current Limit

The device has a fixed, cycle-by-cycle negative overcurrent limit ($I_{LS(NOC)}$). Similar with the positive overcurrent limit, the inductor current is monitored during the on-time of the low-side MOSFET. To prevent too large negative current flowing through the low-side MOSFET, when the device detects a – 10A current (typical threshold) through the low-side MOSFET, the device turns off the low-side MOSFET and then turns on the high-side MOSFET for the on-time set by the one-shot timer (determined by V_{IN}, V_{OUT}, and f_{SW}). After the high-side MOSFET on-time expires, the low-side MOSFET turns on again.

The device must not trigger the – 10A negative current limit threshold during nominal operation, unless a small inductor value that is too small is chosen or the inductor becomes saturated. This negative current limit is used to discharge output capacitors after an output OVP event. See *Overvoltage and Undervoltage* for details.

6.3.12 Overvoltage and Undervoltage Protection

The device monitors a resistor-divided feedback voltage to detect overvoltage and undervoltage events. The OVP function enables when the output is enabled. The UVP function enables after the soft-start period is complete. The OVP and UVP thresholds given in the following explanation are for the 0.9V reference devices and vary slightly with the 0.5V reference devices. Refer to the Electrical Characteristics in セクション 5 for more detailed specifications.

After soft start is complete, if the FB voltage becomes lower than 80% of the V_{REF} voltage, the UVP comparator trips and an internal UVP delay counter begins counting. After the 70µs UVP delay time, depending on the part number, the device either hiccup or latch off. The TPS54KB22 および TPS54KB23 enter hiccup mode and re-start after a sleep time of 7 × the soft-start period. The TPS54KB20 および TPS54KB21 latch off both high-side and low-side MOSFETs drivers. The latch-off fault can be cleared with a reset of VIN or by toggling the EN pin.

When the output is enabled, the FB voltage must rise above the 92.5% PG low-to-high threshold to clear the UVP comparator. If the FB voltage does not exceed the 92.5% threshold by the end of the soft-start period, the device responds to the undervoltage event.

During the UVP delay time, if the FB voltage becomes higher than the 92.5% PG low-to-high threshold, the undervoltage event is cleared and the timer is reset to zero. When the output voltage falls below the 80% UVP threshold again, the 70-µs timer re-starts.

When the FB voltage becomes higher than 118% of the V_{REF} voltage, the OVP comparator trips and the circuit latches the fault condition. The high-side MOSFET turns off and the low-side MOSFET turns on until reaching a negative current limit I_{NOCL}. Upon reaching the negative current limit, the low-side MOSFET is turned off, and the high-side MOSFET is turned on again, for a proper on-time (determined by V_{IN}, V_{OUT}, and f_{SW}).. The device operates in this mode until the output voltage is pulled down under the UVP threshold. The device then responds to the undervoltage event as described above. With a short OVP event that is longer than the OVP delay but shorter than the PG high-to-low delay time, the OVP response can trip while PG remains high. In such a scenario, the PG pin pulls low after the output voltage is pulled below the UVP threshold.

If there is an overvoltage condition prior to the output being enabled (such as a high prebiased output), the device responds to the overvoltage event as described above at the beginning of the soft-start period. The OVP threshold is relative to the final VREF voltage, including during the soft-start period. The device waits until the completion of the soft-start period for UVP to be enabled then, depending on the part number, the device either hiccups or latches off in response to the undervoltage event caused by the OVP response. The TPS54KB22 および TPS54KB23 enter hiccup, while the TPS54KB20 および TPS54KB21 latch off.

6.3.13 Output Voltage Discharge

When the device is disabled through EN, the device enables the output voltage discharge mode. This mode forces both high-side and low-side MOSFETs to latch off, but turns on the internal discharge MOSFET, which is connected from SW to PGND, to discharge the output voltage. After the FB voltage drops below 50mV, the discharge MOSFET and the internal VCC LDO is turned off.

When the EN pin goes low to disable the converter and while the VCC voltage is sufficient to turn on the discharge switch, the output voltage discharge mode is activated.

6.3.14 UVLO Protection

The device monitors the voltage on both the VIN and the VCC pins. If the VCC pin voltage is lower than the VCC_{UVLO} falling threshold voltage, the device shuts off. If the VCC voltage increases beyond the VCC_{UVLO} rising threshold voltage, the device turns back on. VCC UVLO is a non-latch protection.

When the VIN pin voltage is lower than the VIN_{UVLO} falling threshold voltage but the VCC pin voltage is still higher than VCC_{UVLO} rising threshold voltage, the device stops switching and discharges the SS pin. After the VIN voltage increases beyond the VIN_{UVLO} rising threshold voltage, the device re-initiates the soft start and switches again. VIN UVLO is a non-latch protection.

6.3.15 Thermal Shutdown

The device monitors internal junction temperature. If the temperature exceeds the threshold value (typically 165°C), the device stops switching and discharges the SS pin. When the temperature falls approximately 15°C below the threshold value, the device turns back on with a re-initiated soft start. Thermal shutdown is a non-latch protection.

6.4 Device Functional Modes

6.4.1 Auto-Skip Eco-mode Light Load Operation

If the MSEL resistor value used selects Skip-mode, the device automatically reduces the switching frequency at light-load conditions to maintain high efficiency. *Multifunction Select (MSEL) Pin* describes the selection in detail.

As the output current decreases from heavy load condition, the inductor current also decreases until the valley of the inductor ripple current touches the zero-crossing threshold (*Low-side MOSFET Zero-Crossing*). The zero-crossing threshold sets the boundary between the continuous-conduction and discontinuous-conduction modes. The synchronous MOSFET turns off when this zero-crossing threshold is detected. As the load current decreases further, the converter runs into discontinuous-conduction mode (DCM). The on-time is maintained to a level approximately the same as during continuous-conduction mode operation so that discharging the output capacitor with a smaller load current to the level of the reference voltage requires more time. The transition point to light-load operation $I_{OUT(LL)}$ (for example: the boundary between continuous- and discontinuous-conduction mode) is calculated as shown in 式 7.

For low output ripple, TI recommends using only ceramic output capacitors for designs that operate in skip-mode.

$$I_{OUT(LL)} = I_{ZC} + \frac{1}{2} \times \frac{(V_{IN} - V_{OUT})}{L} \times \frac{V_{OUT}}{V_{IN} \times f_{SW}} \quad (7)$$

6.4.2 Forced Continuous-Conduction Mode

If the MSEL resistor value used selects FCCM, the controller operates in continuous-conduction mode (CCM) during light-load conditions. *Multifunction Select (MSEL) Pin* describes the selection in detail. During FCCM, the switching frequency is maintained to an almost constant level over the entire load range, which is designed for applications requiring tight control of the switching frequency and output ripple at the cost of reduced light-load efficiency. Use 式 7 to calculate the typical light-load operation boundary. Below this calculated load current, the device operates in FCCM.

6.4.3 Powering the Device From a Single Bus

The device works well when powered by a single V_{IN} configuration. In a single V_{IN} configuration, the internal LDO is typically powered by a 5V or 12V bus and generates a 3.0V output to bias the internal analog circuitry and power MOSFET gate drivers. The V_{IN} input range under this configuration is 4V to 16V for up to 25A load current. 図 6-8 shows an example for this single V_{IN} configuration.

V_{IN} and EN are the two signals to enable the part. For start-up sequence, any sequence between the V_{IN} and EN signals can power the device up correctly.

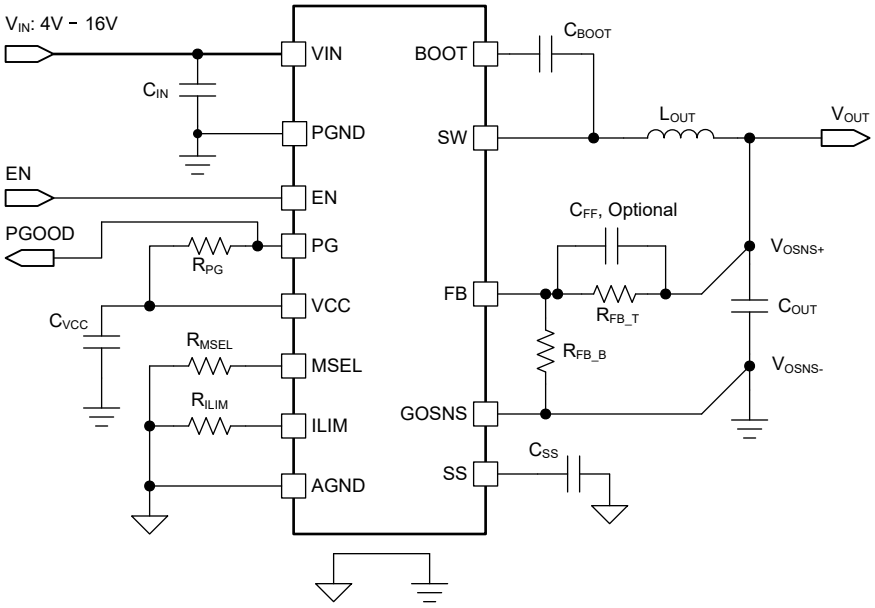


図 6-8. Single V_{IN} Configuration for a 12V Bus

In high output voltage applications, the device VCC can be biased through a low forward voltage diode from the V_{OUT} of the device to provide a boost in efficiency both at low load and high load currents. The output voltage must be greater than 3.1V plus the forward voltage of the external diode to save the power loss on the internal LDO. 図 6-9 shows an example for this configuration.

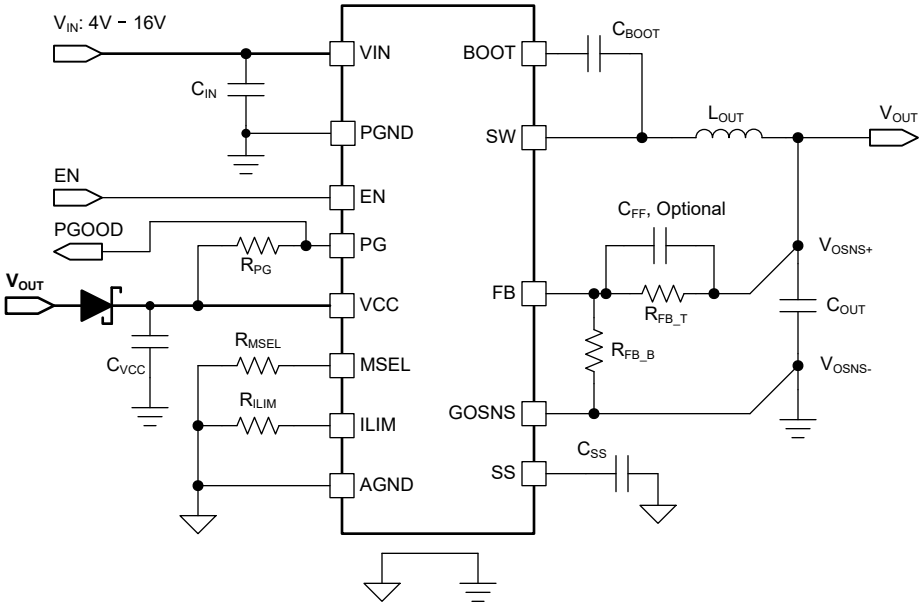


図 6-9. Single V_{IN} Configuration With VCC Biased from V_{OUT}

6.4.4 Powering the Device From a Split-rail Configuration

When an external bias, which is at a different level from main V_{IN} bus, is applied onto the VCC pin the device can be configured to split-rail by using both the main V_{IN} bus and the VCC bias. Connecting a valid VCC bias to the VCC pin overrides the internal LDO, thus saves power loss on the internal LDO. This configuration helps to improve overall system level efficiency but requires a valid VCC bias. A 3.3V or 5.0V rail is the common choice

as VCC bias. With a stable VCC bias, the recommended V_{IN} input range under this configuration remains the same, from 4.0V to 16V.

The noise of the external bias affects the internal analog circuitry. To make sure of a proper operation, a clean, low-noise external bias and good local decoupling capacitor from VCC pin to PGND pin are required. 図 6-10 shows an example for this split rail configuration.

The VCC external bias current during nominal operation varies with the bias voltage level and also the operating frequency. For example, by setting the device to skip-mode, the VCC pin draws less current from the external bias when the frequency decreases under a light load condition. The typical VCC external bias current under FCCM operation is listed in *Electrical Characteristics*. The external bias must be capable of supplying this current or the external bias voltage can drop and the internal LDO can no longer be overridden by it.

Under split rail configuration, V_{IN}, VCC bias, and EN are the signals to enable the part. For start-up sequence, TI recommends that at least one of VIN UVLO rising threshold or EN rising threshold is satisfied later than VCC UVLO rising threshold. A practical start-up sequence example is:

1. V_{IN} applied
2. External VCC bias applied
3. EN signal goes high

Similarly, for power-down sequence, TI recommends that at least one of the VIN UVLO falling threshold or the EN falling threshold is satisfied before the external VCC bias supply turns off. If the external VCC bias supply turns off first, the internal LDO of the device prevents the VCC voltage from dropping below 3.0-V and be loaded by other circuits powered by the external VCC bias supply.

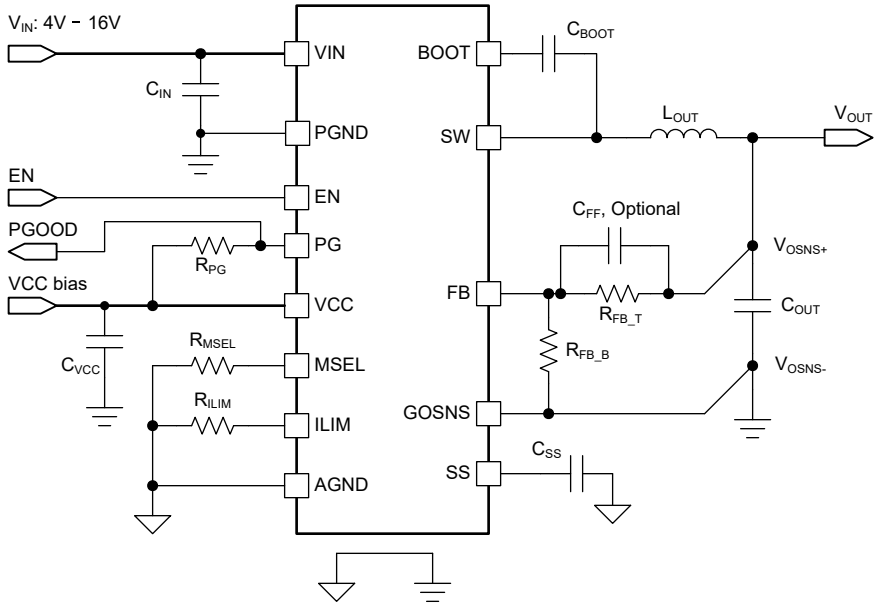


図 6-10. Split-Rail Configuration With External VCC Bias

7 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

7.1 Application Information

The TPS54KB2x device is a high-efficiency, single-channel, small-sized, synchronous-buck converter. The device is designed for low output voltage point-of-load applications with 25A or lower output current in server, storage, and similar computing applications. The TPS54KB2x features proprietary D-CAP4 mode control combined with adaptive on-time architecture. This combination builds modern low-duty-ratio and ultra-fast load-step-response DC/DC converters in an excellent fashion. The output voltage ranges from the internal voltage reference to 5.5V. The conversion input voltage ranges from 4V to 16V, and the VCC input voltage ranges from 3.13 to 5.3V. The D-CAP4 mode uses emulated current information to control the modulation. An advantage of this control scheme is that this control scheme does not require an external phase-compensation network, which makes the device easy-to-use and also allows for a low external component count. Another advantage of this control scheme is that this control scheme supports stable operation with all low ESR output capacitors (such as ceramic capacitor and low ESR polymer capacitor). Adaptive on-time control tracks the preset switching frequency over a wide range of input and output voltages while increasing switching frequency as needed during a load-step transient.

7.2 Typical Application

The schematic shows a typical application for the TPS54KB2x. This example describes the design procedure of converting an input voltage range of 4.5V to 16V down to 3.3V with a maximum output current of 25A.

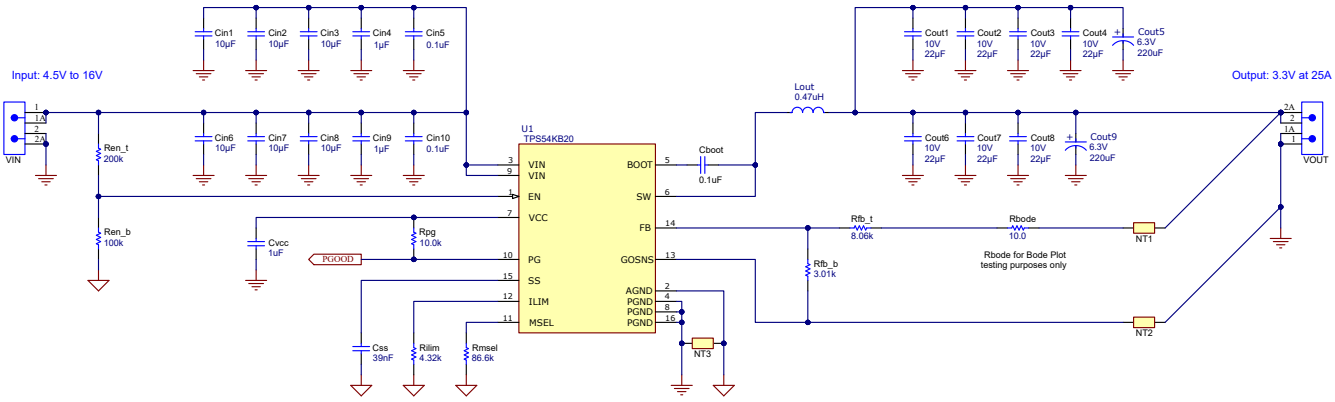


図 7-1. Application Circuit Diagram

7.2.1 Design Requirements

This design uses the parameters listed in 表 7-1.

表 7-1. Design Example Specifications

DESIGN PARAMETER		CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Voltage range		4.5	12	16	V
V_{OUT}	Output voltage			3.3		V
ILOAD	Output load current				25	A
V_{RIPPLE}	Output voltage ripple	V_{IN} = 12V, I_{OUT} = 25A		33		mV_{PP}
V_{TRANS}	Output voltage undershoot and overshoot after load step	I_{OUT} = 5A to 15A step, 1A/µs slew rate		99		mV
I_{OUT_LIM}	Output overcurrent	V_{IN} = 4.5V		28.7		A
t_{SS}	Soft-start time			1		ms
f_{SW}	Switching frequency			800		kHz
	Light load operating mode			Skip-mode		
T_A	Operating temperature			25		°C

7.2.2 Detailed Design Procedure

The external component selection is a simple process using D-CAP4 mode. Select the external components using the following steps.

7.2.2.1 Output Voltage Setting Point

To program the output voltage, use the voltage-divider resistors, R_{FB_T} and R_{FB_B}, as shown in 図 7-1. Connect R_{FB_T} between the FB pin and the output, and connect R_{FB_B} between the FB pin and GOSNS. The recommended value for R_{FB_B} value is 10 kΩ, but it can be set to any value between 1 kΩ to 15 kΩ. For this example, R_{FB_B} was set to 3.01 kΩ. To determine the value of R_{FB_T} for the TPS54KB20, use 式 8.

$$R_{FB\_T} = R_{FB\_B} \times \left(\frac{V_{OUT} - V_{REF}}{V_{REF}}\right) = 3.01\ k\Omega \times \left(\frac{3.3\ V - 0.9\ V}{0.9\ V}\right) = 8\ k\Omega \quad (8)$$

7.2.2.2 Choose the Switching Frequency and the Operation Mode

The switching frequency and operation mode are configured by the resistor on MSEL pin. Select one of three switching frequencies: 800kHz, 1.1MHz, or 1.4MHz. Refer to 表 6-4 for the relationship between the switching frequency, operation mode, ramp, and R_{MSEL}.

Switching frequency selection is a tradeoff between higher efficiency and smaller system design size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses which impact efficiency and thermal performance. For this design, set the switching frequency to 800kHz, and set the light load operating mode as Skip-mode (DCM).

When selecting the switching frequency of a buck converter, the minimum on-time and minimum off-time must be considered. 式 9 calculates the maximum f_{SW} before being limited by the minimum on-time. When hitting the minimum on-time limits of a converter with D-CAP4 control, the effective switching frequency changes to keep the output voltage regulated. This calculation ignores resistive drops in the converter to give a worst case estimation.

$$f_{SW}(max) = \frac{V_{OUT}}{V_{IN}(max)} \times \frac{1}{t_{ON\_MIN}} = \frac{3.3\ V}{16\ V} \times \frac{1}{30\ ns} = 6875\ kHz \quad (9)$$

式 10 calculates the maximum f_{SW} before being limited by the minimum off-time. When hitting the minimum off-time limits of a converter with D-CAP4 control, the operating duty cycle maxes out and the output voltage begins to drop with the input voltage. This equation requires the DC resistance of the inductor, R_{DCR}, selected in the

following step so this preliminary calculation assumes a resistance of 2.2mΩ. If operating near the maximum f_{SW} limited by the minimum off-time, the variation in resistance across temperature must be considered when using 式 10. The selected f_{SW} of 800kHz is below the two calculated maximum values.

$$f_{SW}(max) = \frac{V_{IN}(min) - V_{OUT} - I_{OUT}(max) \times \left(R_{DCR} + R_{DS(ON)\_HS}\right)}{t_{OFF\_MIN}(max) \times \left(V_{IN}(min) - I_{OUT}(max) \times \left(R_{DS(ON)\_HS} - R_{DS(ON)\_LS}\right)\right)} \quad (10)$$

$$f_{SW}(max) = \frac{4.5\ V - 3.3\ V - 25\ A \times (2.2\ m\Omega + 5.8\ m\Omega)}{150\ ns \times (4.5\ V - 25\ A \times (5.8\ m\Omega - 2.3\ m\Omega))} = 1510\ kHz \quad (11)$$

7.2.2.3 Choose the Inductor

To calculate the value of the output inductor (L_{OUT}), use 式 12. The output capacitor filters the inductor-ripple current (I_{RIPPLE}), 式 13. Therefore, selecting a high inductor-ripple current impacts the selection of the output capacitor because the output capacitor must have a ripple-current rating equal to or greater than the inductor-ripple current. Larger ripple current increases output ripple voltage, but improves signal-to-noise ratio and helps to stabilize operation. Generally speaking, the inductance value must set the ripple current at approximately 15% to 40% of the maximum output current for a balanced performance.

For this design, the inductor-ripple current is set to 30% of 25A output current. With a 800kHz switching frequency, 16V as maximum V_{IN}, and 3.3V as the output voltage, the calculated inductance is 0.437µH. A nearest standard value of 0.47µH is chosen.

$$L = \frac{(V_{IN}(max) - V_{OUT}) \times V_{OUT}}{I_{RIPPLE} \times V_{IN}(max) \times f_{SW}} = \frac{(16\ V - 3.3\ V) \times 3.3\ V}{0.3 \times 25A \times 16\ V \times 800\ kHz} = 0.437\ \mu H \quad (12)$$

The inductor requires a low DCR to achieve good efficiency. The inductor also requires enough room above peak inductor current before saturation. The peak inductor current is estimated using 式 14. Peak inductor current under maximum V_{IN} is calculated as 28.5A. 式 15 calculates the RMS current in the inductor and the heat current rating of the inductor must be greater than this.

$$I_{RIPPLE} = \frac{(V_{IN}(max) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(max) \times f_{SW}} = \frac{(16\ V - 3.3\ V) \times 3.3\ V}{0.47\mu H \times 16\ V \times 800\ kHz} = 7\ A \quad (13)$$

$$I_{L(PEAK)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 25\ A + \frac{7\ A}{2} = 28.5\ A \quad (14)$$

$$I_{L(RMS)} = \sqrt{{I_{OUT}}^2 + \frac{{I_{RIPPLE}}^2}{12}} = \sqrt{{25\ A}^2 + \frac{{7\ A}^2}{12}} = 25.08\ A \quad (15)$$

7.2.2.4 Set the Current Limit (ILIM)

The R_{ILIM} resistor sets the valley current limit. 式 16 and 式 17 calculate the recommended current limit target. This includes the tolerance of the inductor and a factor of 0.9 for the tolerance of the current limit threshold. This example uses an estimation of 10% tolerance. Refer to the specification table for tolerance across different R_{ILIM} values. 式 19 calculates the R_{ILIM} resistor to set the current limit. The typical valley current limit target is 27.5A and the closest standard value for R_{ILIM} is 4.32kΩ.

$$I_{LIM\_VALLEY} = \left(I_{OUT} - \frac{1}{2} \times \frac{(V_{IN}(min) - V_{OUT}) \times V_{OUT}}{L \times (1 + L_{TOL}) \times V_{IN}(min) \times f_{SW}}\right) \times \frac{1}{0.9} \quad (16)$$

$$I_{LIM\_VALLEY} = \left(25\ A - \frac{1}{2} \times \frac{(4.5\ V - 3.3\ V) \times 3.3\ V}{0.47\ \mu H \times (1 + 0.2) \times 4.5\ V \times 800\ kHz}\right) \times \frac{1}{0.9} = 26.7\ A \quad (17)$$

$$R_{ILIM} = \frac{120000}{I_{LIM\_VALLEY}} \quad (18)$$

$$R_{ILIM} = \frac{120000}{27.5\ A} = 4.36\ k\Omega \quad (19)$$

With the current limit set, 式 20 calculates the typical maximum output current at current limit. 式 21 calculates the typical peak current at current limit. As mentioned in *Choose the Inductor*, the saturation behavior of the inductor at the peak current during current limit must be considered. For worst case calculations, the tolerance of the inductance and the current limit must be included.

$$I_{OUT\_LIM}(min) = I_{LIM\_VALLEY} + \frac{1}{2} \times \frac{(V_{IN}(min) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(min) \times f_{SW}} = 27.5\ A + \frac{1}{2} \times \frac{(4.5\ V - 3.3\ V) \times 3.3\ V}{0.47\ \mu H \times 4.5\ V \times 800\ kHz} = 28.7\ A \quad (20)$$

$$I_{L(PEAK)} = I_{LIM\_VALLEY} + \frac{(V_{IN}(max) - V_{OUT}) \times V_{OUT}}{L \times V_{IN}(max) \times f_{SW}} = 27.5\ A + \frac{(16\ V - 3.3\ V) \times 3.3\ V}{0.47\ \mu H \times 16\ V \times 800\ kHz} = 34.5\ A \quad (21)$$

7.2.2.5 Choose the Output Capacitor

There are three considerations for selecting the value of the output capacitor:

1. Stability
2. Steady state output voltage ripple
3. Regulator transient response to a change load current

First, calculate the minimum output capacitance based on these three requirements. 式 22 calculates the minimum capacitance to keep the LC double pole below the $f_{P(MAX)}$ to meet stability requirements. This requirement helps to keep the LC double pole close to the internal zero. 式 23 calculates the minimum capacitance to meet the steady state output voltage ripple requirement of 33mV. This calculation is for CCM operation and does not include the portion of the output voltage ripple caused by the ESR or ESL of the output capacitors.

$$C_{OUT\_STABILITY} > \left(\frac{1}{2\pi \times f_{P(RAMP4)} \times \left(1 + \left(\frac{V_{OUT}}{V_{IN(TYP)}}\right)^2\right)} \right)^2 \times \frac{1}{L_{OUT}} = \left(\frac{1}{2\pi \times 20.3kHz \times \left(1 + \left(\frac{3.3V}{12V}\right)^2\right)} \right)^2 \times \frac{1}{0.47\mu H} \quad (22)$$

$$= 113\mu F$$

$$C_{OUT\_RIPPLE} > \frac{I_{RIPPLE}}{8 \times V_{RIPPLE} \times f_{SW}} = \frac{7\ A}{8 \times 33\ mV \times 800\ kHz} = 33\ \mu F \quad (23)$$

式 25 and 式 26 calculate the minimum capacitance to meet the transient response requirement of 99mV with a 10A step. These equations calculate the necessary output capacitance to hold the output voltage steady while the inductor current ramps up or ramps down after a load step. Calculations determine only 418.5µF is needed to meet the transient response requirement. This calculation assumes instant load step.

$$C_{OUT\_UNDERSHOOT} > \frac{L \times {I_{STEP}}^2 \times \left(\frac{V_{OUT}}{V_{IN}(min) \times f_{SW}} + t_{OFF\_MIN}(max)\right)}{2 \times V_{TRANS} \times V_{OUT} \times \left(\frac{V_{IN}(min) - V_{OUT}}{V_{IN}(min) \times f_{SW}} - t_{OFF\_MIN}(max)\right)} \quad (24)$$

$$C_{OUT\_UNDERSHOOT} > \frac{0.47\ \mu H \times 10\ A^2 \times \left(\frac{3.3\ V}{4.5\ V \times 800\ kHz} + 150\ ns\right)}{2 \times 99\ mV \times 3.3\ V \times \left(\frac{4.5\ V - 3.3\ V}{4.5\ V \times 800\ kHz} - 150\ ns\right)} = 418.5\ \mu F \quad (25)$$

$$C_{OUT\_OVERSHOOT} > \frac{L \times {I_{STEP}}^2}{2 \times V_{TRANS} \times V_{OUT}} = \frac{0.47\ \mu H \times 10\ A^2}{2 \times 99\ mV \times 3.3\ V} = 71.9\ \mu F \quad (26)$$

The output capacitance needed to meet the undershoot requirement is the highest value, so this sets the required minimum output capacitance for this example. Stability requirements can also limit the maximum output capacitance. 式 27 calculates the recommended maximum output capacitance. This calculation keeps the LC double pole above 1/100th the f_{SW}. Using more output capacitance is possible, but the stability must be checked through a bode plot or transient response measurement. The selected output capacitance is 7 × 22µF, 10V

ceramic capacitors. When using ceramic capacitors, the capacitance must be derated due to DC and AC bias effects. The selected capacitors derate to 58% the nominal value giving an effective total capacitance of 89µF. Additionally, 2 × 220µF, 6.3V bulk capacitors are also selected, increasing the effective total output capacitance to 529µF. This effective capacitance meets the minimum and maximum requirements.

$$C_{OUT\_STABILITY} < \left(\frac{50}{\pi \times f_{SW}}\right)^2 \times \frac{1}{L} = \left(\frac{50}{\pi \times 800\ kHz}\right)^2 \times \frac{1}{0.47\ \mu H} = 842\ \mu F \quad (27)$$

This application uses all ceramic capacitors so the effects of ESR on the ripple and transient were ignored. If using non ceramic capacitors, as a starting point, the ESR must be below the values calculated in 式 28 to meet the ripple requirement and 式 29 to meet the transient requirement. For more accurate calculations or if using mixed output capacitors, the impedance of the output capacitors must be used to determine if the ripple and transient requirements can be met.

$$R_{ESR\_RIPPLE} < \frac{V_{RIPPLE}}{I_{RIPPLE}} = \frac{33\ mV}{7\ A} = 4.7\ m\Omega \quad (28)$$

$$R_{ESR\_TRANS} < \frac{V_{TRANS}}{I_{STEP}} = \frac{99\ mV}{10\ A} = 9.9\ m\Omega \quad (29)$$

7.2.2.6 RAMP Selection

To determine the proper ramp selection for this design, the L-C double pole frequency and the maximum L-C double pole frequency must be calculated. The double pole frequency is based on the selected output inductance and output capacitance for this design. Using 式 30, the L-C double pole frequency for this design is 10kHz. Calculating the maximum L-C double pole frequency then helps guide the user to select one of the four ramp options. Generally, if the L-C double pole calculation lands within the RAMP1 margin, select RAMP1, as this results in the best transient response. Select RAMP2 or RAMP3 if the L-C double pole calculation does not fit within the RAMP1 margin. TI recommends RAMP2 for an increase in phase margin, while TI recommends RAMP3 for higher gain and a faster transient response than RAMP2. If RAMP1, RAMP2, or RAMP3 cannot be selected due to maximum L-C double pole frequency restriction, then choose RAMP4. The maximum L-C double pole frequency can be calculated using 式 31, where the variable $f_{P(TABLE)}$ equates to the RAMP1 maximum L-C double pole from 表 6-2. This calculation results in 15kHz, 19.7kHz, and 21.8kHz, for RAMP1, RAMP3, and RAMP4 respectively. Because the L-C double pole frequency in this design is 10kHz, which is less than RAMP1, RAMP1 is selected.

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} = \frac{1}{2 \times \pi \times \sqrt{0.47\ \mu H \times 529\ \mu F}} = 10\ kHz \quad (30)$$

$$f_{P(MAX)} = f_{P(TABLE)} \times \left(1 + \left(\frac{V_{OUT}}{V_{IN(typ)}}\right)^2\right) = 14.0\ kHz \times \left(1 + \left(\frac{3.3\ V}{12\ V}\right)^2\right) = 15\ kHz \quad (31)$$

After selecting RAMP1 for this design, connect the MSEL pin to AGND using a 86.6kΩ resistor to set the switching frequency to 800kHz and the ramp option to RAMP1.

7.2.2.7 Choose the Input Capacitors (C_{IN})

The device requires input bypass capacitors between both pairs of VIN and PGND pins to bypass the power-stage. The bypass capacitors must be placed as close as possible to the pins of the IC as the layout allows. At least 20µF nominal of ceramic capacitance and two high frequency ceramic bypass capacitors are required. This device has a hard limit of 20µF. Some applications can require greater capacitance and can even require a bulk capacitor. Derating can impact the effective input capacitance value. A 0.1µF to 1µF capacitor must be placed as close as possible to both VIN pins 3 and 9 on the same side of the board of the device to provide the required high frequency bypass, to reduce the high frequency overshoot and undershoot across the power-stage from VIN to SW and SW to PGND. TI recommends at least 1µF of bypass capacitance as close as possible to each VIN pin to minimize the input voltage ripple. The ceramic capacitors must be a high-quality dielectric of X6S or

better for the high capacitance-to-volume ratio and stable characteristics across temperature. In addition to this requirement, more bulk capacitance can be needed on the input depending on the application to minimize variations on the input voltage during transient conditions.

The input capacitance required to meet a specific input ripple target can be calculated with 式 32. A recommended target input voltage ripple is 5% the minimum input voltage, 225mV in this example. The calculated input capacitance is 27.2µF and this meets the minimum input capacitance of 20µF.

$$C_{IN} > \frac{V_{OUT} \times I_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN(min)}}\right)}{f_{SW} \times V_{IN(min)} \times V_{IN\_RIPPLE}} = \frac{3.3\ V \times 25\ A \times \left(1 - \frac{3.3\ V}{4.5\ V}\right)}{800\ kHz \times 4.5\ V \times 225\ mV} = 27.2\ \mu F \quad (32)$$

The capacitor must also have an RMS current rating greater than the maximum input RMS current in the application. The input RMS current the input capacitors must support is calculated by 式 34 and is 11.2A in this example. The ceramic input capacitors have a current rating greater than this value.

$$I_{CIN(RMS)} = \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \left(\frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}} \times {I_{OUT}}^2 + \frac{{I_{RIPPLE}}^2}{12}\right)} = \quad (33)$$

$$I_{CIN(RMS)} = \sqrt{\frac{3.3\ V}{4.5\ V} \times \left(\frac{(4.5\ V - 3.3\ V)}{4.5\ V} \times 25^2 + \frac{7^2}{12}\right)} = 11.2\ A \quad (34)$$

For applications requiring bulk capacitance on the input, such as ones with low input voltage and high current, TI recommends the selection process in *How to select input capacitors for a buck converter* analog design journal.

7.2.2.8 Soft-Start Capacitor (SS Pin)

This example uses a 1ms soft-start time and the required external capacitance can be calculated with 式 35. In this design, a 39nF capacitor is used as this value is the nearest standard value.

$$C_{SS} = \frac{I_{SS} \times t_{SS}}{V_{REF}} = \frac{36\ \mu A \times 1\ ms}{0.9\ V} = 40\ nF \quad (35)$$

A minimum capacitor value of 10nF is required at the SS pin. The SS capacitor must use the AGND pin for the ground.

7.2.2.9 EN Pin Resistor Divider

A resistor divider on the EN pin can be used to increase the input voltage the converter begins the start-up sequence. To set the start voltage, first select the bottom resistor (R_{EN_B}). The recommended value is between 1kΩ and 100kΩ. There is an internal pulldown resistance with a nominal value of 1MΩ and this internal pulldown resistance must be included for the most accurate calculations. This requirement is especially important when the bottom resistor is a higher value, near 100kΩ. This example uses a 100kΩ resistor, and this resistor combined with the internal resistance in parallel results in an equivalent bottom resistance of 90.9kΩ. The top resistor value for the target start voltage is calculated with 式 36. In this example, the nearest standard value of 200kΩ is selected for R_{EN_T}. When selecting a start voltage in a wide input range application, be cautious that the EN pin absolute maximum voltage of 7V is not exceeded.

$$R_{EN\_T} = \frac{R_{EN\_B} \times V_{START}}{V_{ENH}} - R_{EN_B} = \frac{90.9\ k\Omega \times 3.8\ V}{1.2\ V} - 90.9\ k\Omega = 197\ k\Omega \quad (36)$$

The start and stop voltages with the selected EN resistor divider can be calculated with 式 37 and 式 38.

$$V_{START} = V_{ENH} \times \frac{R_{EN\_B} + R_{EN\_T}}{R_{EN\_B}} = 1.2\ V \times \frac{90.9\ k\Omega + 200\ k\Omega}{90.9\ k\Omega} = 3.8\ V \quad (37)$$

$$V_{STOP} = V_{ENL} \times \frac{R_{EN\_B} + R_{EN\_T}}{R_{EN\_B}} = 1\ V \times \frac{90.9\ k\Omega + 200\ k\Omega}{90.9\ k\Omega} = 3.2\ V \quad (38)$$

7.2.2.10 VCC Bypass Capacitor

At a minimum, a 1.0µF, at least 6.3V rating, X5R ceramic bypass capacitor is needed on VCC pin located as close to the pin as the layout allows. Use the smallest sized capacitor possible, such as an 0402 package, to minimize the loop from the VCC pin to the PGND pin.

7.2.2.11 BOOT Capacitor

At a minimum, a 0.1µF, 10V X5R ceramic bypass capacitor is needed between the BOOT and SW pins located as close to the pin as the layout allows.

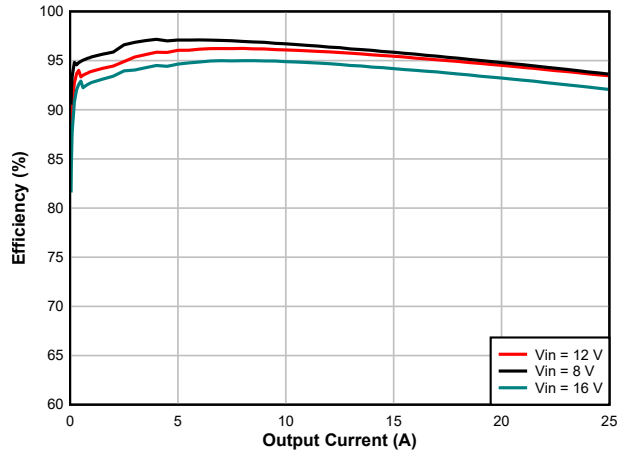
7.2.2.12 RC Snubber

An RC snubber on the SW pin can also help reduce voltage overshoot and ringing at the SW pin. For the RC snubber to be as effective as possible with the symmetrical pinout, place the RC snubber on the opposite side of the board from the IC with multiple vias in the SW node to minimize routing impedance and with a very low impedance return to the PGND pins.

7.2.2.13 PG Pullup Resistor

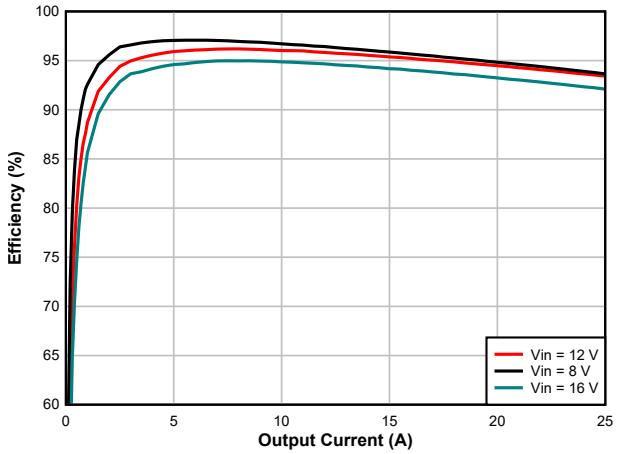
The PG pin is open-drain, so a pullup resistor is required when using this pin. The recommended value is between 1kΩ and 100kΩ.

7.2.3 Application Curves



V_{OUT} = 3.3V　V_{VCC} = 3V internal　f_{SW} = 800kHz
L_{OUT} = 470nH　DCR = 1.85mΩ　Skip-mode

図 7-2. Efficiency – Skip-mode



V_{OUT} = 3.3V　V_{VCC} = 3V internal　f_{SW} = 800kHz
L_{OUT} = 470nH　DCR = 1.85mΩ　FCCM

図 7-3. Efficiency – FCCM

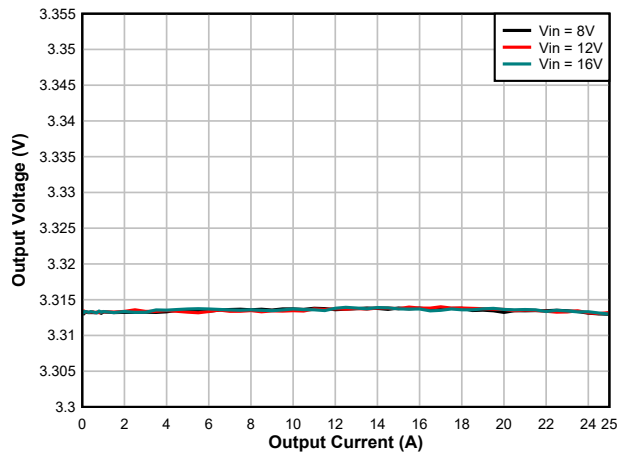


図 7-4. Load Regulation

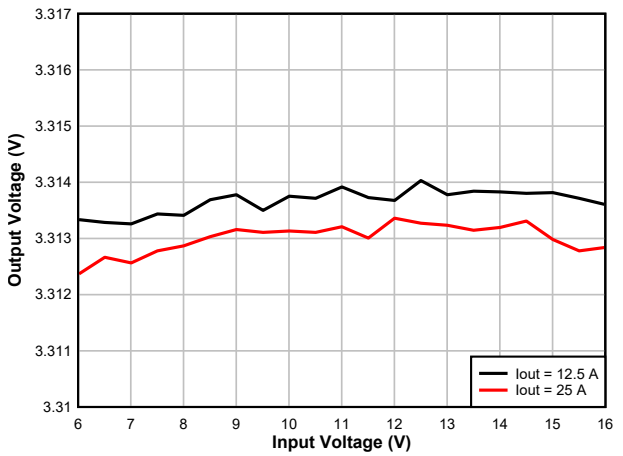
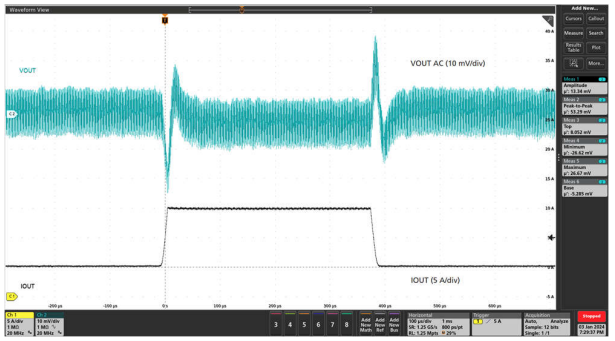
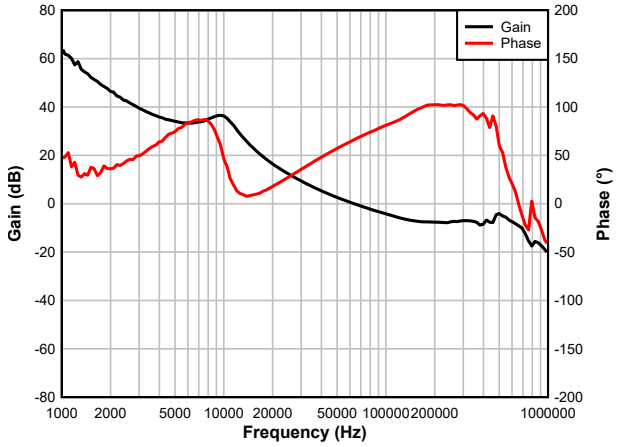


図 7-5. Line Regulation



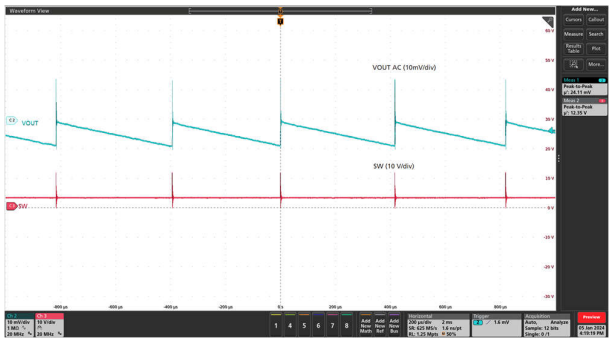
I_{OUT} = 5A to 15A at 1A/µs
R_{MSEL} = 86.6kΩ　f_{SW} = 800kHz　RAMP1

図 7-6. Load Transient



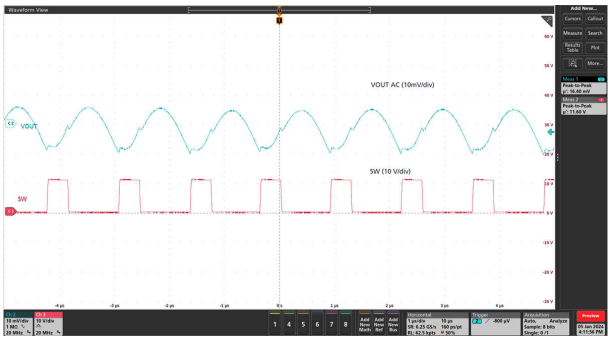
I_{OUT} = 10A
R_{MSEL} = 86.6kΩ　f_{SW} = 800kHz　RAMP1

図 7-7. Bode Plot



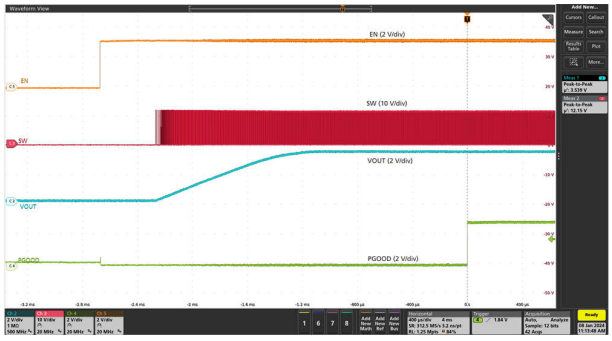
V_{IN} = 12V V_{OUT} = 3.3V I_{OUT} = 10mA

図 7-8. Output Voltage Ripple – Skip-mode



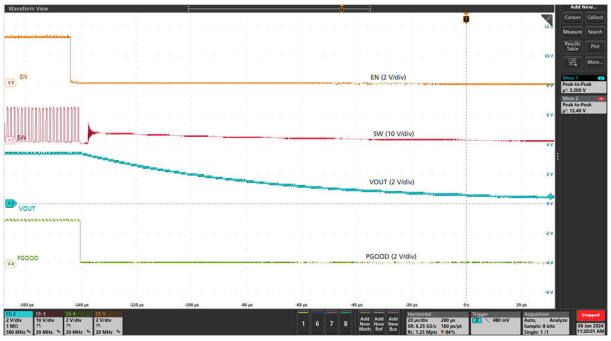
V_{IN} = 12V V_{OUT} = 3.3V I_{OUT} = 25A

図 7-9. Output Voltage Ripple – FCCM



V_{IN} = 12V V_{OUT} = 3.3V I_{OUT} = 25A

図 7-10. Start-Up With EN



V_{IN} = 12V V_{OUT} = 3.3V I_{OUT} = 25A

図 7-11. Shutdown With EN

7.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4V and 16V. Both input supplies (VIN and VCC bias) must be well regulated. Proper bypassing of input supplies (VIN and VCC bias) is also critical for noise performance, as are PCB layout and grounding scheme. See the recommendations in *Layout*.

7.4 Layout

7.4.1 Layout Guidelines

Before beginning a design using the device, consider the following:

- Make VIN, PGND, and SW traces as wide as possible to reduce trace impedance and improve heat dissipation.
- Place the power components (including input and output capacitors, the inductor, and the IC) on the top side of the PCB. To shield and isolate the small signal traces from noisy power lines, insert at least one solid ground inner plane.
- Make note that placement of the VIN decoupling capacitors are important for the power MOSFET robustness. A 1µF/25V/0402 ceramic high-frequency bypass capacitor on each VIN pin (pin 3 and 9) is required, connected to the adjacent PGND pins (pin 4 and 8 respectively). Place the remaining ceramic input capacitance next to these high frequency bypass capacitors. The remaining input capacitance can be placed on the other side of the board, but use as many vias as possible to minimize impedance between the capacitors and the pins of the IC.
- Place eight vias below the PGND pins (pins 4, 8, and 16) and as many vias as possible near the PGND pins (pin 4 and 8). This action minimizes parasitic impedance and also lowers thermal resistance.
- Use vias near both VIN pins and provide a low impedance connection between them through an internal layer. A via can also be placed below each of the VIN pins.
- Place the VCC decoupling capacitor as close as possible to the device, with a short return to PGND pin 8. Make sure the VCC decoupling loop is small and use traces with a width of 12 mil or wider to route the connection.
- Place the BOOT capacitor as close as possible to the BOOT and SW pins. Use traces with a width of 12 mil or wider to route the connection.
- Make the switch node as short and wide as possible. The PCB trace, which connects the SW pin and high-voltage side of the inductor, is defined as switch node.
- Always place the feedback resistors near the device to minimize the FB trace distance, no matter single-end sensing or remote sensing.
  - For remote sensing, the connections from the FB voltage divider resistors to the remote location must be a differential pair of PCB traces, and must implement Kelvin sensing across a bypass capacitor of 0.1µF or higher. The ground connection of the remote sensing signal must be connected to GOSNS pin. The V_{OUT} connection of the remote sensing signal must be connected to the feedback resistor divider with the bottom feedback resistor terminated to the GOSNS pin. To maintain stable output voltage and minimize the ripple, the pair of remote sensing lines must stay away from any noise sources such as inductor and SW nodes, or high frequency clock lines. TI recommends to shield the pair of remote sensing lines with ground planes above and below.
  - For single-end sensing, connect the top feedback resistor between the FB pin and the output voltage to a high-frequency local output bypass capacitor of 0.1µF or higher, and short GOSNS to AGND with a short trace.
- Connect the AGND pin (pin 2) to the PGND pad (pin 16) beneath the device.
- Return the MSEL resistor, ILIM resistor, and SS capacitor to a quiet AGND island.
- Avoid routing the PG signal and any other noisy signals in the application near noise sensitive signals, such as ILIM, FB and GOSNS to limit coupling.
- See *Layout Example* for the layout recommendation.

7.4.2 Layout Example

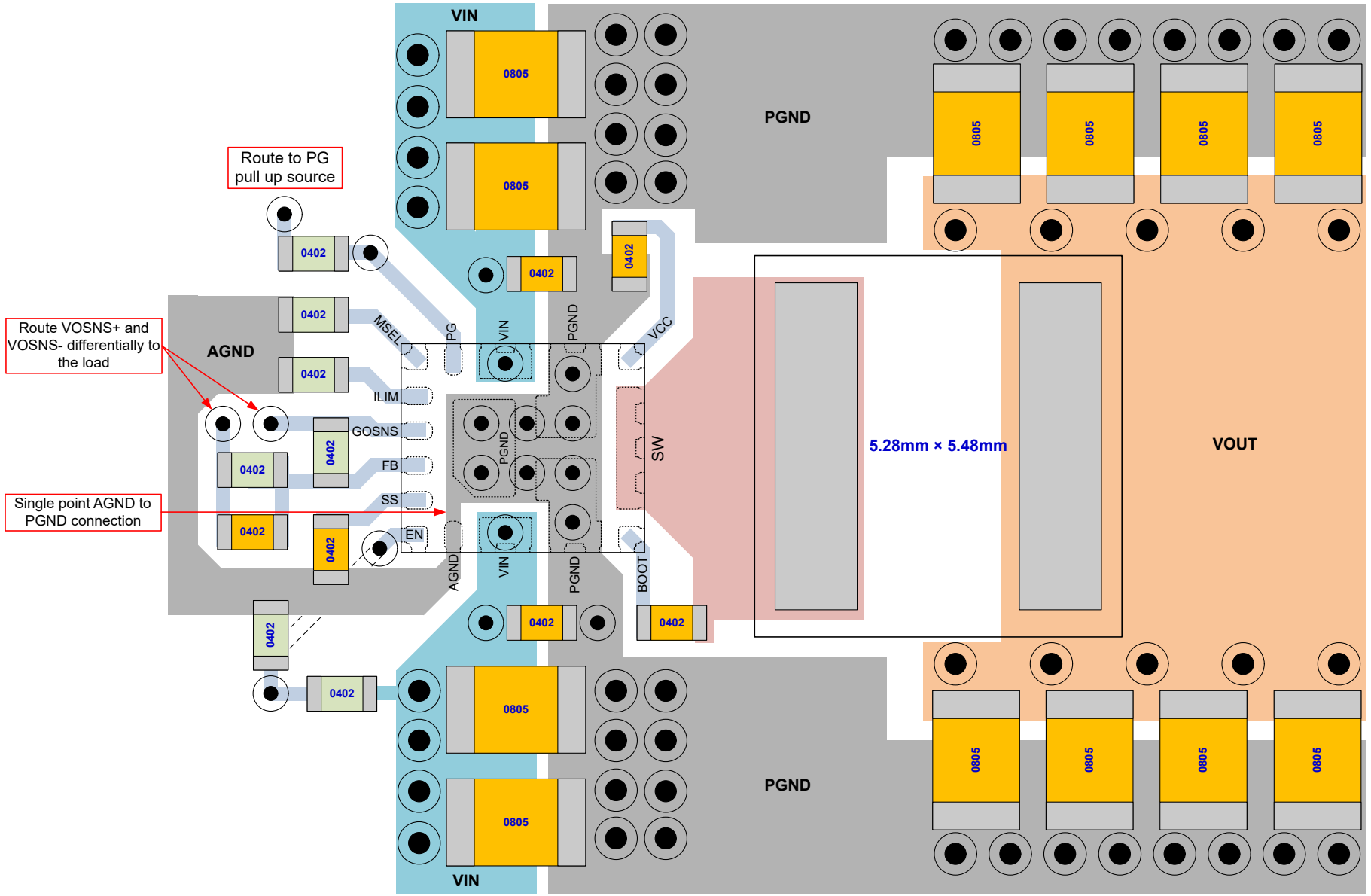


図 7-12. Layout Recommendation

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

- Texas Instruments, *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feedforward Capacitor* application report
- Texas Instruments, *Non-isolated Point-of-load Solutions for VR13.HC in Rack Server and Datacenter Applications* application report
- Texas Instruments, *How to select input capacitors for a buck converter* analog design journal

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (May 2023) to Revision A (February 2024)	Page
• ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54KB20RZRR	ACTIVE	WQFN-FCRLF	RZR	16	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T54KB0	Samples
TPS54KB21RZRR	ACTIVE	WQFN-FCRLF	RZR	16	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T54KB1	Samples
TPS54KB22RZRR	ACTIVE	WQFN-FCRLF	RZR	16	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T54KB2	Samples
TPS54KB23RZRR	ACTIVE	WQFN-FCRLF	RZR	16	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T54KB3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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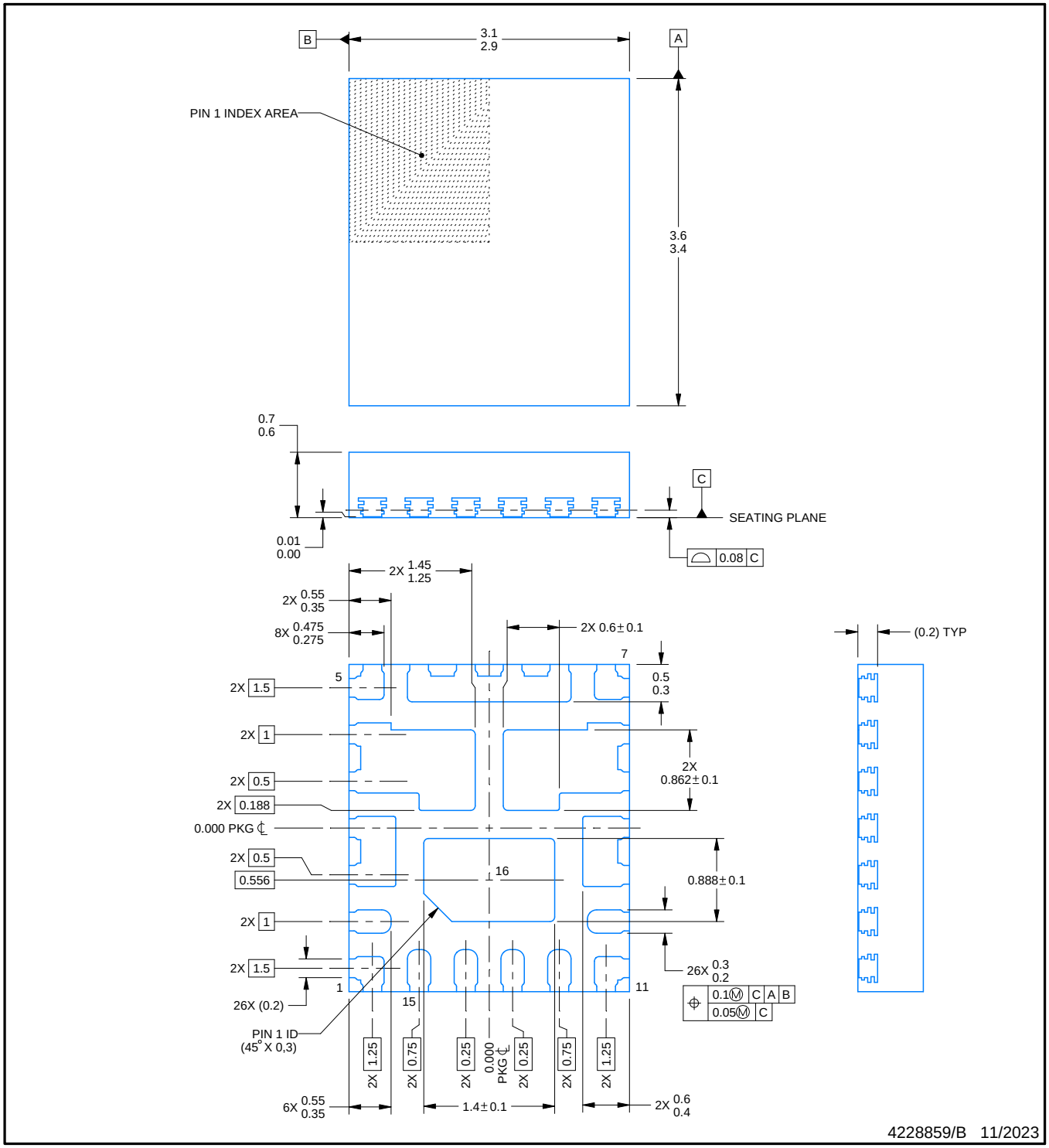
PACKAGE OUTLINE

RZR0016A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

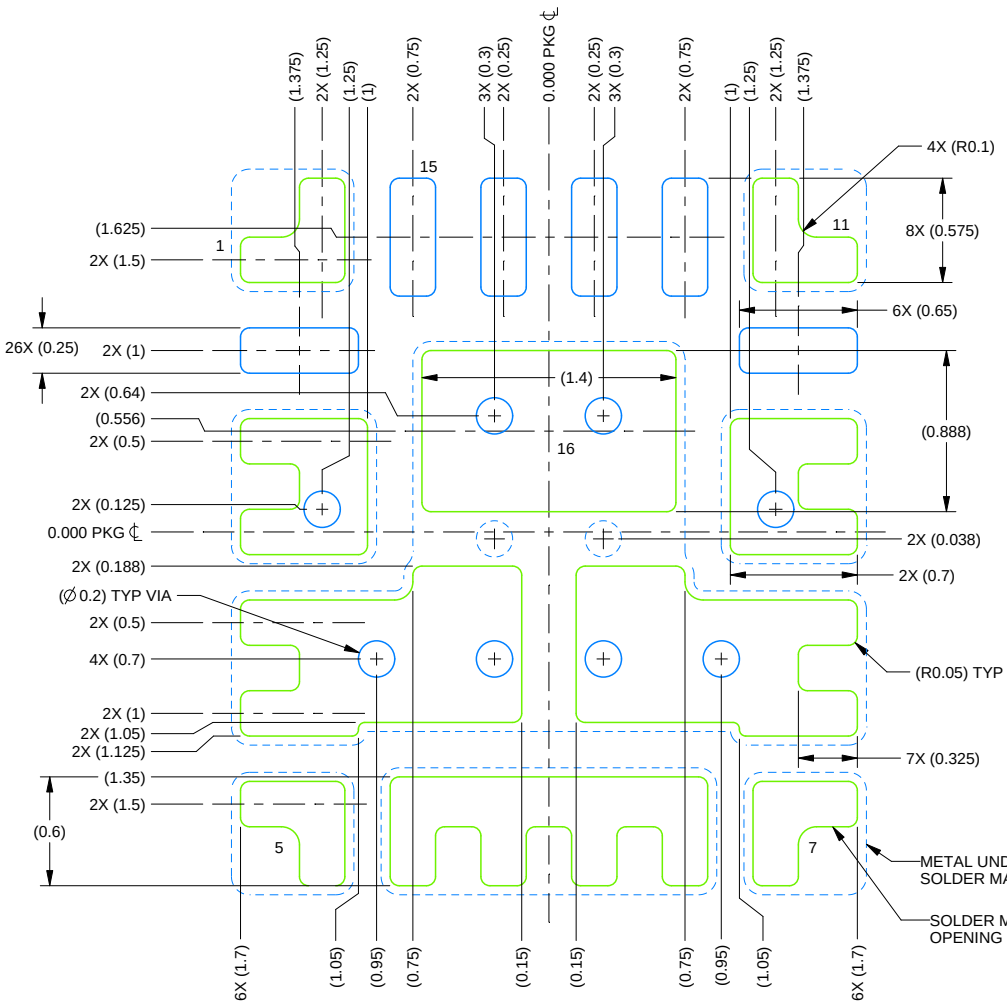
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

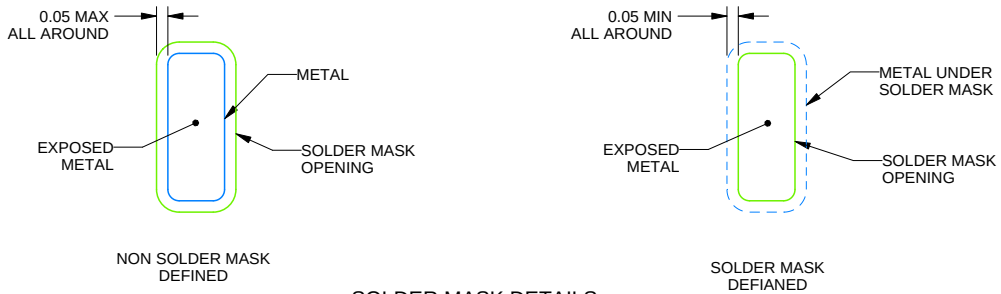
RZR0016A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 24X



SOLDER MASK DETAILS

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NOTES: (continued)

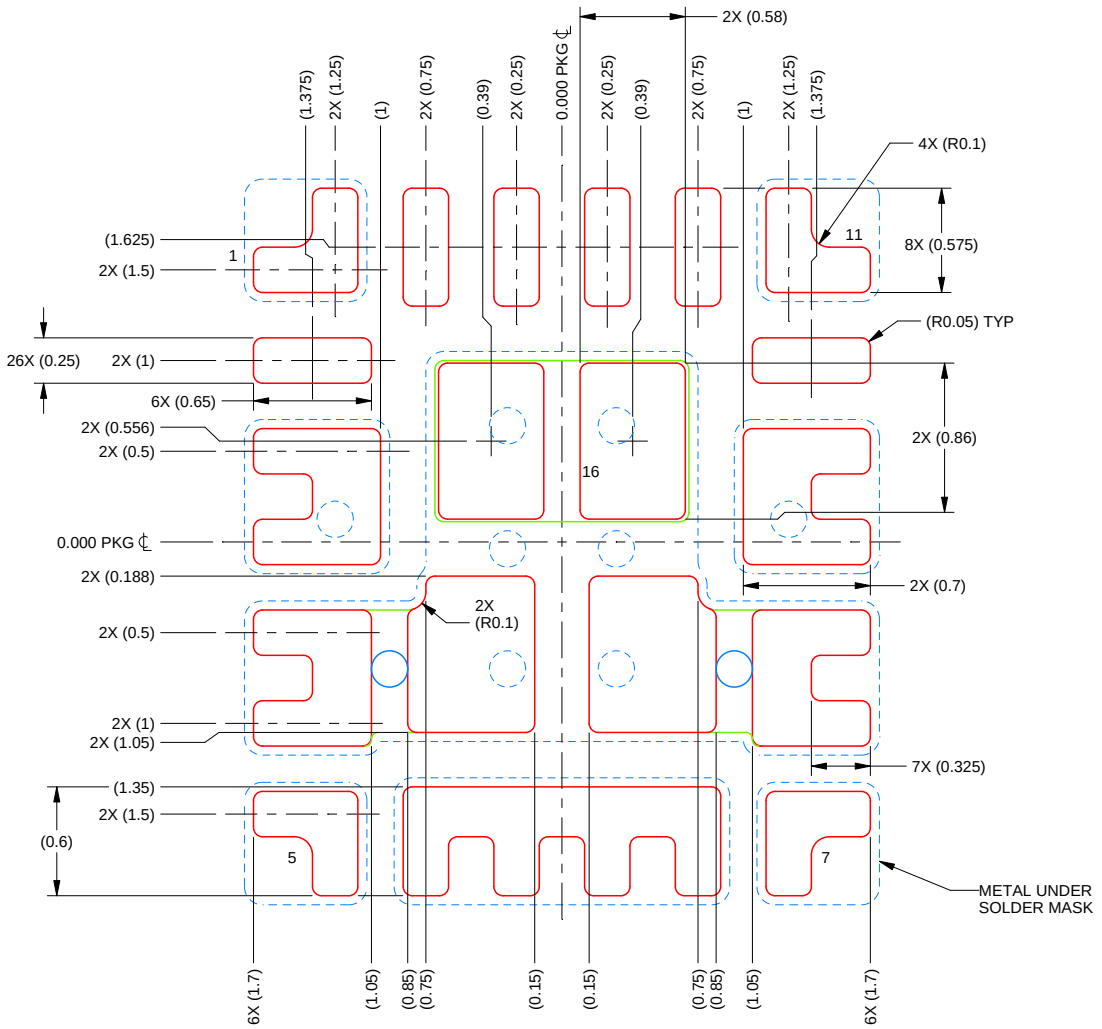
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RZR0016A

WQFN-FCRLF - 0.7 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 24X

PRINTED SOLDER COVERAGE BY AREA
PADS 4 & 8: 88%
PAD 16: 80%

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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