

## TPS3890-Q1

### 低静止電流で遅延をプログラム可能な1%精度のスーパーバイザ

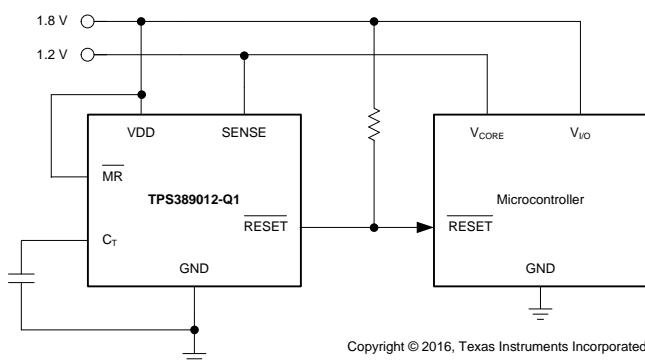
#### 1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み:
  - デバイス温度グレード1: 動作時周囲温度範囲  $-40^{\circ}\text{C} \sim 125^{\circ}\text{C}$
  - デバイスHBM ESD分類レベル2
  - デバイスCDM ESD分類レベルC4B
- パワーオン・リセット(POR)ジェネレータ、遅延時間を $25\mu\text{s} \sim 30\text{s}$ に設定可能
- 非常に低い静止電流:  $2.1\mu\text{A}$  (標準値)
- 高いスレッシュホールド精度: 1% (最大値)
- 高精度のヒステリシス
- 固定および可変のスレッシュホールド電圧
  - 標準レールの固定スレッシュホールド:  $1.2\text{V} \sim 5\text{V}$
  - 最低 $1.15\text{V}$ まで調整可能
- マニュアル・リセット(MR)入力
- オープン・ドレインRESET出力
- 温度範囲:  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$
- パッケージ:  $1.5\text{mm} \times 1.5\text{mm}$  WSON

#### 2 アプリケーション

- インフォテインメント用ヘッド・ユニット
- ハイブリッド/デジタル・クラスタ
- 外部アンプ
- ADASカメラ
- 車載用ゲートウェイ

代表的なアプリケーション回路



#### 3 概要

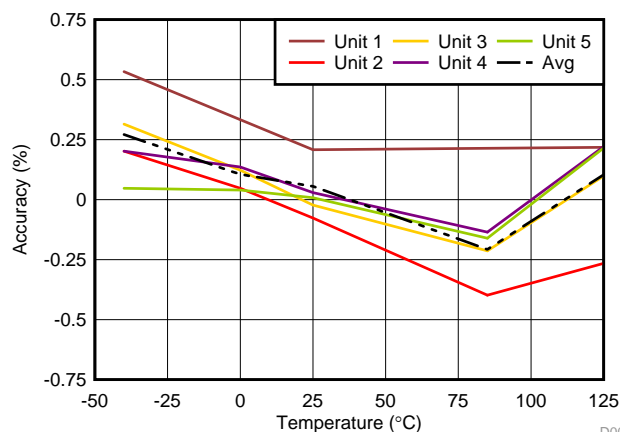
TPS3890-Q1は高精度の電圧スーパーバイザで、静止電流が低く、最低 $1.15\text{V}$ のシステム電圧を監視でき、SENSE電圧が設定済みのスレッシュホールドより低下したとき、またはマニュアル・リセット(MR)ピンが論理LOWに低下したとき、オープン・ドレインのRESET信号をアサートします。RESET出力は、SENSE電圧とマニュアル・リセット(MR)がそれぞれのスレッシュホールド以上に復帰した後も、ユーザーが設定した遅延時間だけLOWに維持されます。TPS3890-Q1ファミリは、高精度の基準電圧を使用して、1%のスレッシュホールド精度を実現しています。リセットの遅延時間は、CTピンを外付けのコンデンサへ接続することで、 $25\mu\text{s} \sim 30\text{s}$ の範囲に設定できます。TPS3890-Q1は静止電流が $2.1\mu\text{A}$ と非常に低く、小形の $1.5\text{mm} \times 1.5\text{mm}$ パッケージで供給されるため、バッテリー駆動および実装面積の制限されるアプリケーションに適しています。このデバイスは、 $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ の温度範囲( $T_j$ )にわたって完全に動作が規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS3890-Q1	WSON (6)	$1.50\text{mm} \times 1.50\text{mm}$

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

$V_{ITN}$ の精度と温度との関係



D001



## 目次

1	特長 .....	1	8.4	Device Functional Modes.....	14
2	アプリケーション .....	1	<b>9</b>	<b>Application and Implementation .....</b>	<b>15</b>
3	概要 .....	1	9.1	Application Information.....	15
4	改訂履歴.....	2	9.2	Typical Application .....	15
5	<b>Device Comparison Table .....</b>	<b>3</b>	<b>10</b>	<b>Power Supply Recommendations .....</b>	<b>16</b>
6	<b>Pin Configuration and Functions .....</b>	<b>3</b>	<b>11</b>	<b>Layout.....</b>	<b>17</b>
7	<b>Specifications.....</b>	<b>4</b>	11.1	Layout Guidelines .....	17
7.1	Absolute Maximum Ratings .....	4	11.2	Layout Example .....	17
7.2	ESD Ratings .....	4	<b>12</b>	<b>デバイスおよびドキュメントのサポート .....</b>	<b>18</b>
7.3	Recommended Operating Conditions.....	4	12.1	デバイス・サポート .....	18
7.4	Thermal Information .....	4	12.2	ドキュメントのサポート .....	18
7.5	Electrical Characteristics.....	5	12.3	ドキュメントの更新通知を受け取る方法.....	18
7.6	Timing Requirements .....	5	12.4	コミュニティ・リソース .....	18
7.7	Typical Characteristics .....	7	12.5	商標 .....	19
<b>8</b>	<b>Detailed Description .....</b>	<b>11</b>	12.6	静電気放電に関する注意事項 .....	19
8.1	Overview .....	11	12.7	Glossary .....	19
8.2	Functional Block Diagram .....	11	<b>13</b>	<b>メカニカル、パッケージ、および注文情報 .....</b>	<b>19</b>
8.3	Feature Description.....	11			

## 4 改訂履歴

### Revision A (October 2017) から Revision B に変更

Page

•	車載用の特長 追加 .....	1
•	Added new voltage options to Device Comparison Table.....	3

### 2017年3月発行のものから更新

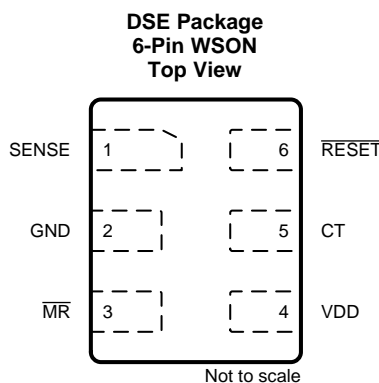
Page

•	Added TPS389050L-Q1 to Device Comparison Table .....	3
---	--	---

## 5 Device Comparison Table

PART NUMBER	NOMINAL SUPPLY VOLTAGE	NEGATIVE THRESHOLD ( $V_{ITN}$ )	POSITIVE THRESHOLD ( $V_{ITP}$ )
TPS389001-Q1	Adjustable	1.15 V	1.157 V
TPS389012-Q1	1.2 V	1.15 V	1.157 V
TPS389015-Q1	1.5 V	1.44 V	1.449 V
TPS389018-Q1	1.8 V	1.73 V	1.740 V
TPS389025-Q1	2.5 V	2.40 V	2.414 V
TPS389030-Q1	3.0 V	2.89 V	2.907 V
TPS389033-Q1	3.3 V	3.17 V	3.189 V
TPS389033G-Q1	3.3 V	3.06 V	3.084 V
TPS389033K-Q1	3.3 V	2.93 V	2.947 V
TPS389050-Q1	5.0 V	4.80 V	4.828 V
TPS389050G-Q1	5.0 V	4.65 V	4.677 V
TPS389050L-Q1	5.0 V	4.40 V	4.425 V

## 6 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SENSE	I	This pin is connected to the voltage to be monitored. When the voltage on SENSE falls below the negative threshold voltage $V_{ITN}$ , $\overline{\text{RESET}}$ goes low (asserts). When the voltage on SENSE rises above the positive threshold voltage $V_{ITP}$ , $\overline{\text{RESET}}$ goes high (deasserts).
2	GND	—	Ground
3	$\overline{\text{MR}}$	I	Driving the manual reset pin ( $\overline{\text{MR}}$ ) low causes $\overline{\text{RESET}}$ to go low (assert).
4	VDD	I	Supply voltage pin. Good analog design practice is to place a 0.1- $\mu\text{F}$ ceramic capacitor close to this pin.
5	CT	—	The CT pin offers a user-adjustable delay time. Connecting this pin to a ground-referenced capacitor sets the $\overline{\text{RESET}}$ delay time to deassert. $t_{PD(f)}$ (sec) = $C_{CT}$ ( $\mu\text{F}$ ) $\times$ 1.07 + 25 $\mu\text{s}$ (nom).
6	$\overline{\text{RESET}}$	O	$\overline{\text{RESET}}$ is an open-drain output that is driven to a low-impedance state when either the $\overline{\text{MR}}$ pin is driven to a logic low or the monitored voltage on the SENSE pin is lower than the negative threshold voltage ( $V_{ITN}$ ). $\overline{\text{RESET}}$ remains low (asserted) for the delay time period after both $\overline{\text{MR}}$ is set to a logic high and the SENSE input is above $V_{ITP}$ . A pullup resistor from 10 k $\Omega$ to 1 M $\Omega$ should be used on this pin.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	V <sub>DD</sub>	-0.3	7	V
	SENSE	-0.3	7	
	RESET	-0.3	7	
	MR	-0.3	7	
	V <sub>CT</sub>	-0.3	7	
Current	RESET	-20	20	mA
Temperature	Operating junction, T <sub>J</sub>	-40	125	°C
	Operating ambient, T <sub>A</sub>	-40	125	
	Storage, T <sub>stg</sub>	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per AEC Q100-011	±750	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Power-supply voltage	1.5		5.5	V
V <sub>SENSE</sub>	SENSE voltage	0		5.5	V
V <sub>RESET</sub>	RESET pin voltage	0		5.5	V
I <sub>RESET</sub>	RESET pin current	-5		5	mA
C <sub>IN</sub>	Input capacitor, V <sub>DD</sub> pin	0	0.1		μF
C <sub>CT</sub>	Reset timeout capacitor, CT pin	0		26	μF
R <sub>PU</sub>	Pullup resistor, RESET pin	1		1000	kΩ
T <sub>J</sub>	Junction temperature (free-air temperature)	-40	25	125	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS3890-Q1	UNIT
		DSE (WSO)	
		6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	321.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	207.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	281.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	42.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	284.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	142.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ( $T_A = T_J$ ),  $1.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{DD}$  (unless otherwise noted); typical values are at  $V_{DD} = 5.5\text{ V}$  and  $T_J = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DD}$	Input supply voltage		1.5		5.5	V
$V_{POR}$	Power-on-reset voltage	$V_{OL(max)} = 0.2\text{ V}$ , $I_{RESET} = 15\ \mu\text{A}$			0.8	V
$I_{DD}$	Supply current (into VDD pin)	$V_{DD} = 3.3\text{ V}$ , $I_{RESET} = 0\text{ mA}$ , $-40^{\circ}\text{C} < T_J < 85^{\circ}\text{C}$		2.09	3.72	$\mu\text{A}$
		$V_{DD} = 3.3\text{ V}$ , $I_{RESET} = 0\text{ mA}$ , $-40^{\circ}\text{C} < T_J < 105^{\circ}\text{C}$			4.5	
		$V_{DD} = 3.3\text{ V}$ , $I_{RESET} = 0\text{ mA}$			5.8	
		$V_{DD} = 5.5\text{ V}$ , $I_{RESET} = 0\text{ mA}$ , $-40^{\circ}\text{C} < T_J < 85^{\circ}\text{C}$		2.29	4	
		$V_{DD} = 5.5\text{ V}$ , $I_{RESET} = 0\text{ mA}$ , $-40^{\circ}\text{C} < T_J < 105^{\circ}\text{C}$			5.2	
		$V_{DD} = 5.5\text{ V}$ , $I_{RESET} = 0\text{ mA}$			6.5	
$V_{ITN}$ , $V_{ITP}$	SENSE input threshold voltage accuracy		-1%	$\pm 0.5\%$	1%	
$V_{HYST}$	Hysteresis <sup>(1)</sup>		0.325%	0.575%	0.825%	
$I_{SENSE}$	Input current	$V_{SENSE} = 5\text{ V}$			8	$\mu\text{A}$
		$V_{SENSE} = 5\text{ V}$ , TPS389001-Q1, TPS389012-Q1		10	100	nA
$I_{CT}$	CT pin charge current		0.90	1.15	1.35	$\mu\text{A}$
$V_{CT}$	CT pin comparator threshold voltage		1.17	1.23	1.29	V
$R_{CT}$	CT pin pulldown resistance	When $\overline{\text{RESET}}$ is deasserted		200		$\Omega$
$V_{IL}$	Low-level input voltage ( $\overline{\text{MR}}$ pin)			$0.25 \times V_{DD}$		V
$V_{IH}$	High-level output voltage		$0.7 \times V_{DD}$			V
$V_{OL}$	Low-level output voltage	$V_{DD} \geq 1.5\text{ V}$ , $I_{RESET} = 0.4\text{ mA}$			0.25	V
		$V_{DD} \geq 2.7\text{ V}$ , $I_{RESET} = 2\text{ mA}$			0.25	
		$V_{DD} \geq 4.5\text{ V}$ , $I_{RESET} = 3\text{ mA}$			0.3	
$I_{LKG(OD)}$	Open-drain output leakage	High impedance, $V_{SENSE} = V_{RESET} = 5.5\text{ V}$			250	nA

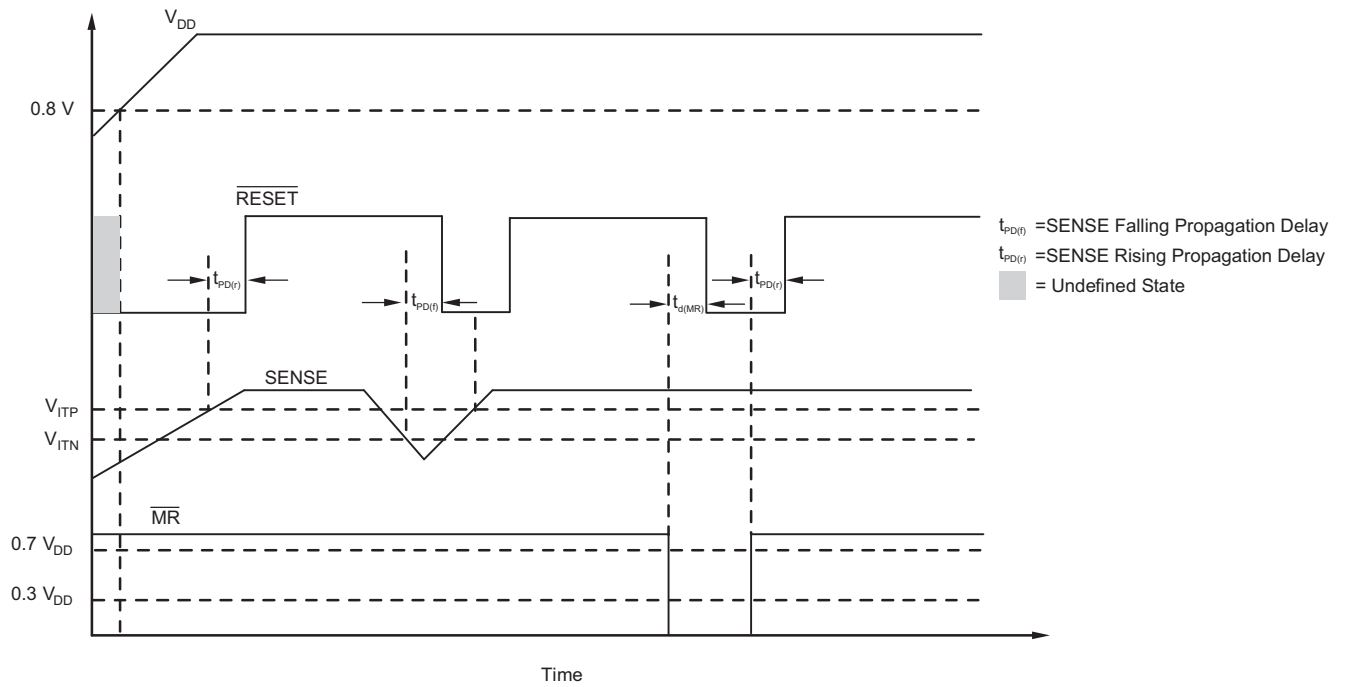
(1)  $V_{HYST} = [(V_{ITP} - V_{ITN}) / V_{ITN}] \times 100\%$ .

## 7.6 Timing Requirements

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  ( $T_A = T_J$ ),  $1.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $\overline{\text{MR}} = V_{DD}$ , and 5% input overdrive<sup>(1)</sup> (unless otherwise noted); typical values are at  $V_{DD} = 5.5\text{ V}$  and  $T_J = 25^{\circ}\text{C}$

		MIN	NOM	MAX	UNIT
$t_{PD(f)}$	SENSE (falling) to $\overline{\text{RESET}}$ propagation delay	$C_T = \text{open}$ , $V_{DD} = 3.3\text{ V}$	18		$\mu\text{s}$
		$C_T = \text{open}$ , $V_{DD} = 5.5\text{ V}$	8		
$t_{PD(r)}$	SENSE (rising) to $\overline{\text{RESET}}$ propagation delay	$C_T = \text{open}$ , $V_{DD} = 3.3\text{ V}$	25		$\mu\text{s}$
$t_{GI(SENSE)}$	SENSE pin glitch immunity	$V_{DD} = 5.5\text{ V}$	9		$\mu\text{s}$
$t_{GI(MR)}$	$\overline{\text{MR}}$ pin glitch immunity	$V_{DD} = 5.5\text{ V}$	100		ns
$t_{MRW}$	$\overline{\text{MR}}$ pin pulse duration to assert $\overline{\text{RESET}}$	1			$\mu\text{s}$
$t_{d(MR)}$	$\overline{\text{MR}}$ pin low to out delay		250		ns
$t_{STRT}$	Startup delay		325		$\mu\text{s}$

(1) Overdrive =  $| (V_{IN} / V_{THRESH} - 1) \times 100\% |$ .



**1. Timing Diagram**

### 7.7 Typical Characteristics

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{\text{DD}}$  (unless otherwise noted)

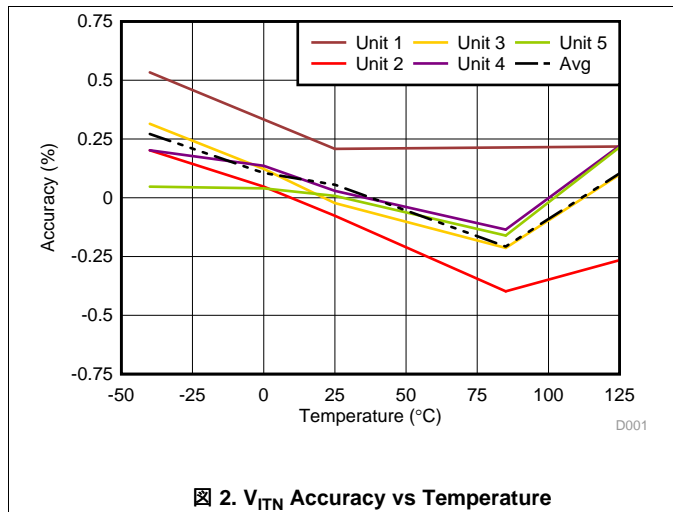


Figure 2.  $V_{\text{ITN}}$  Accuracy vs Temperature

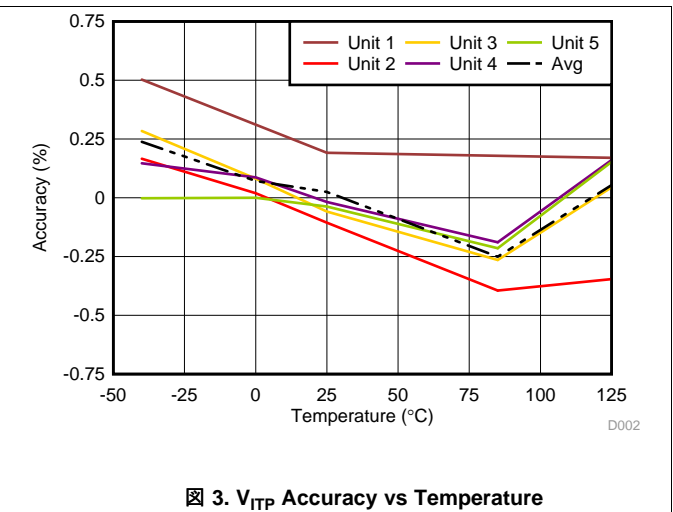


Figure 3.  $V_{\text{ITP}}$  Accuracy vs Temperature

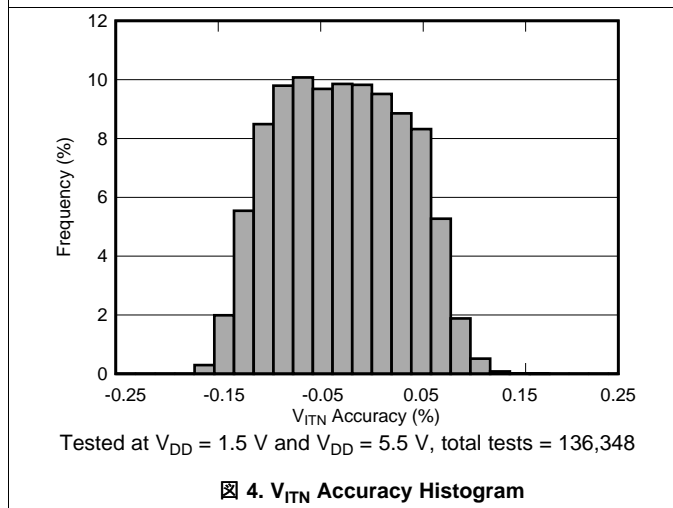


Figure 4.  $V_{\text{ITN}}$  Accuracy Histogram

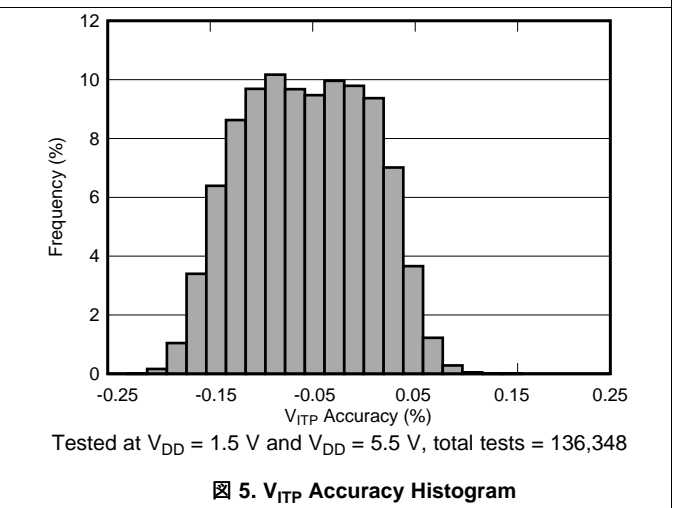


Figure 5.  $V_{\text{ITP}}$  Accuracy Histogram

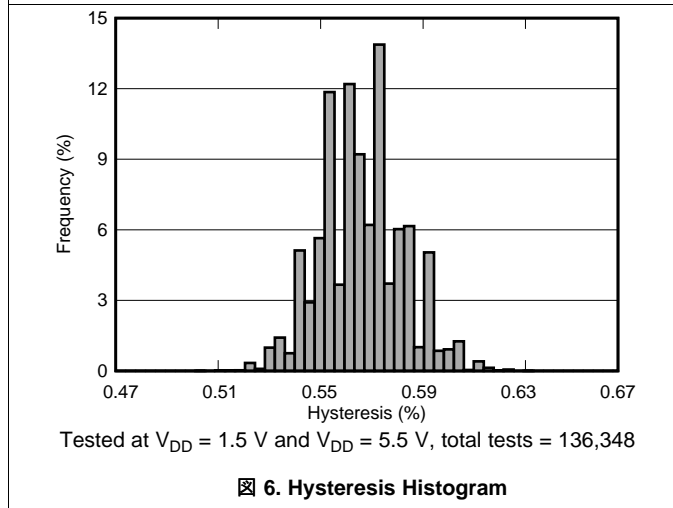


Figure 6. Hysteresis Histogram

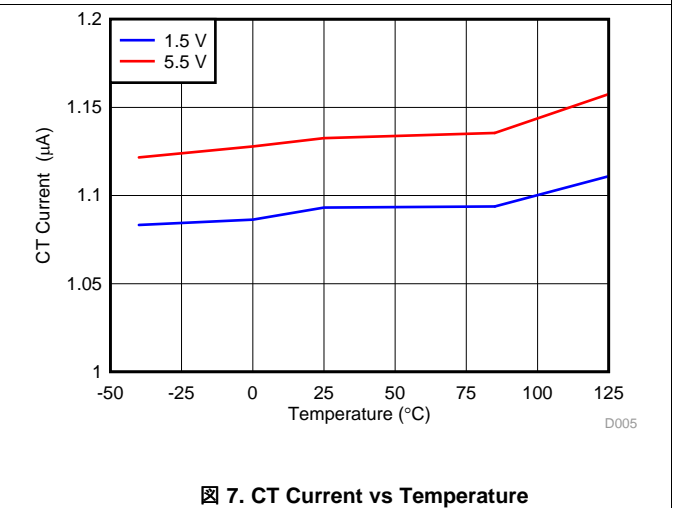
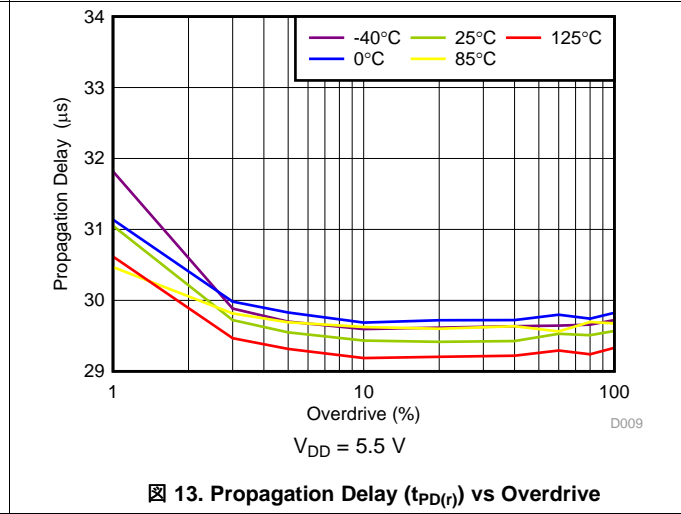
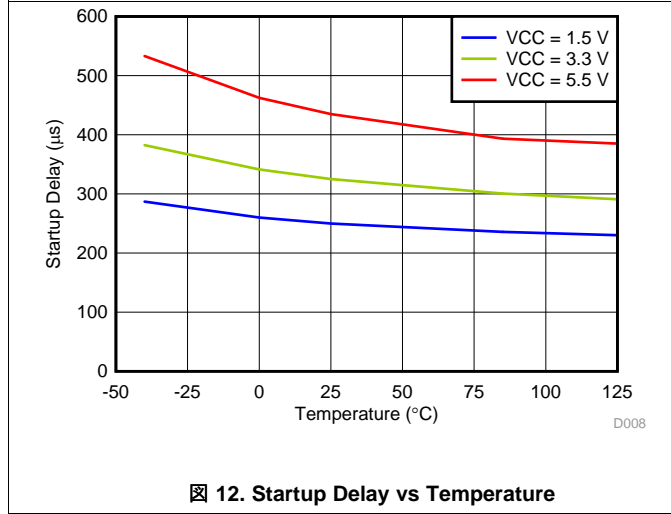
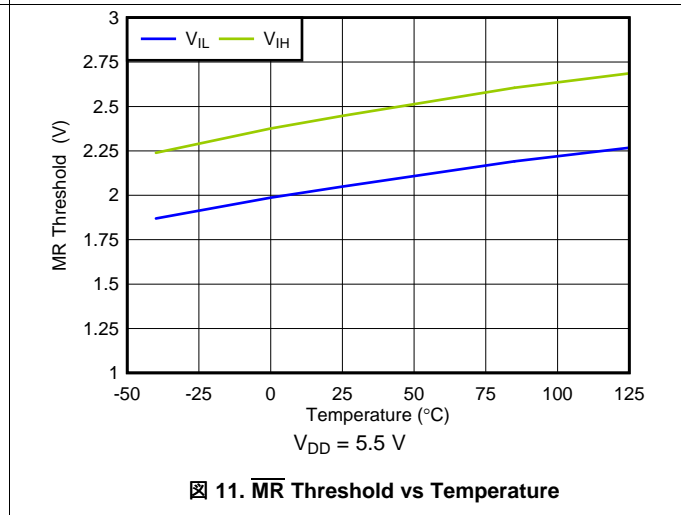
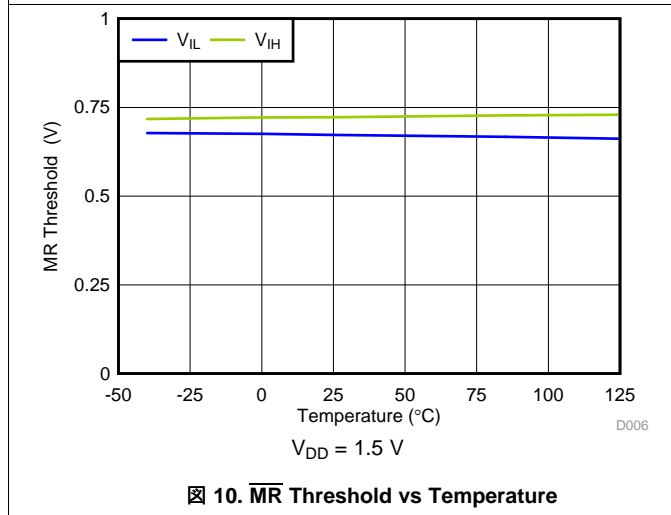
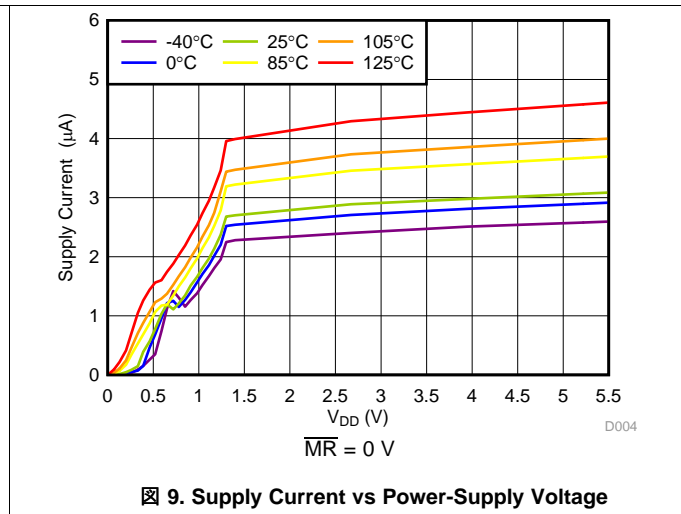
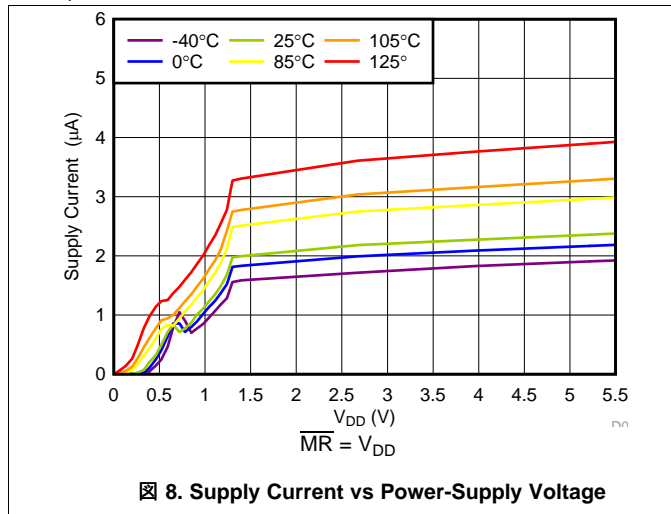


Figure 7. CT Current vs Temperature

### Typical Characteristics (continued)

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{\text{DD}}$  (unless otherwise noted)





Typical Characteristics (continued)

over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{\text{DD}}$  (unless otherwise noted)

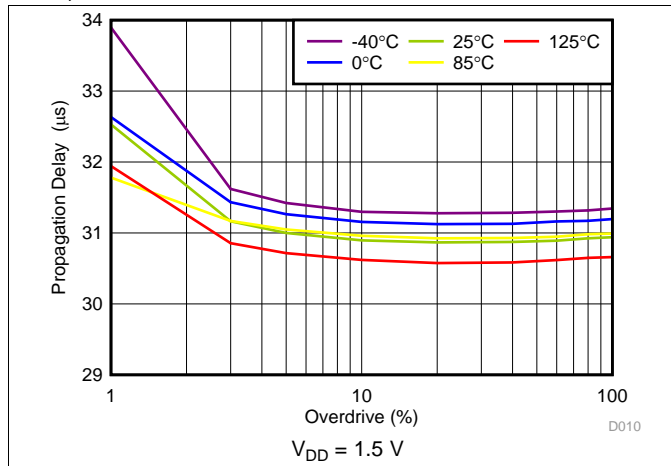


Figure 14. Propagation Delay ( $t_{\text{PD}(f)}$ ) vs Overdrive

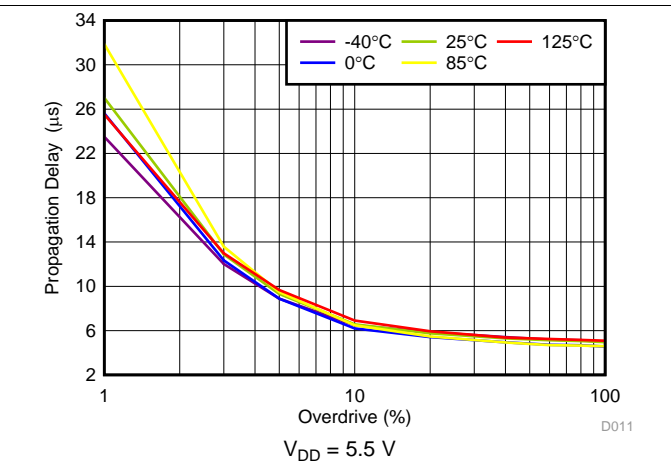


Figure 15. Propagation Delay ( $t_{\text{PD}(f)}$ ) vs Overdrive

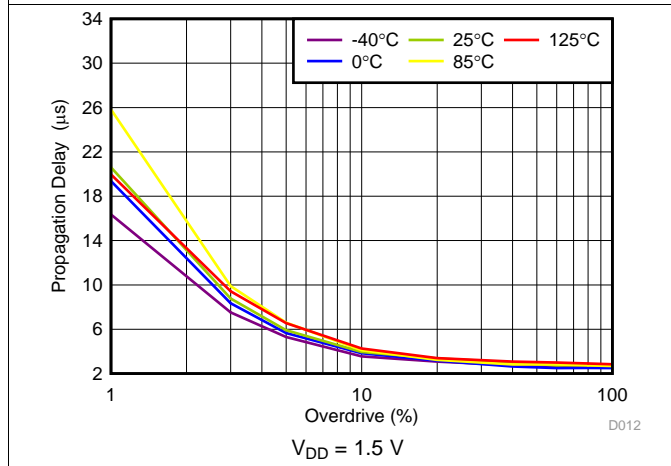


Figure 16. Propagation Delay ( $t_{\text{PD}(f)}$ ) vs Overdrive

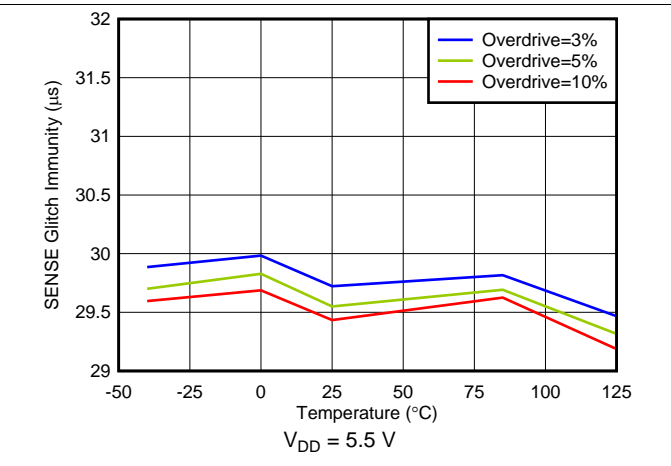


Figure 17. Low-to-High Glitch Immunity vs Temperature

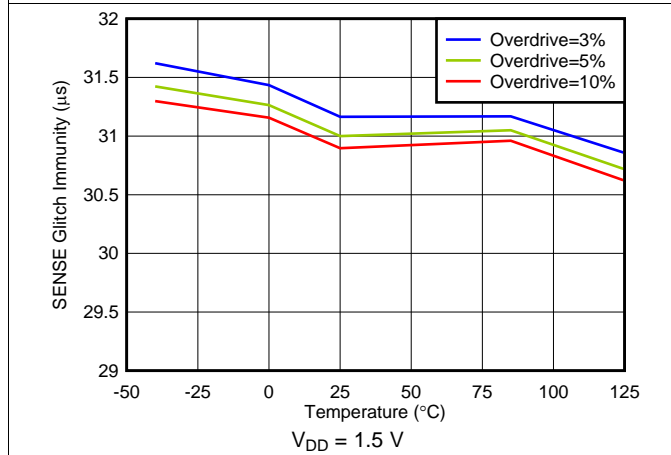


Figure 18. Low-to-High Glitch Immunity vs Temperature

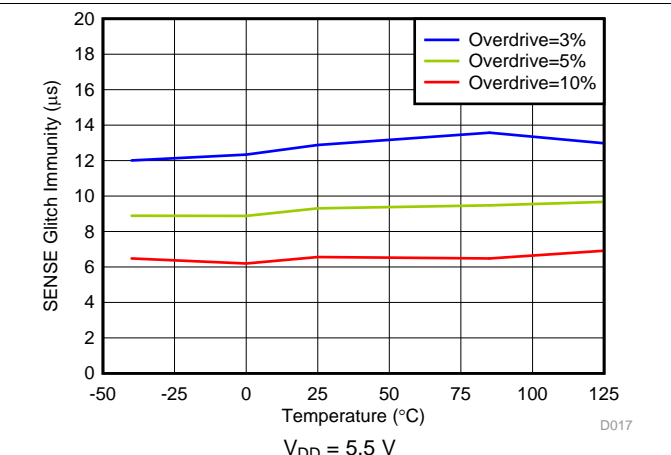
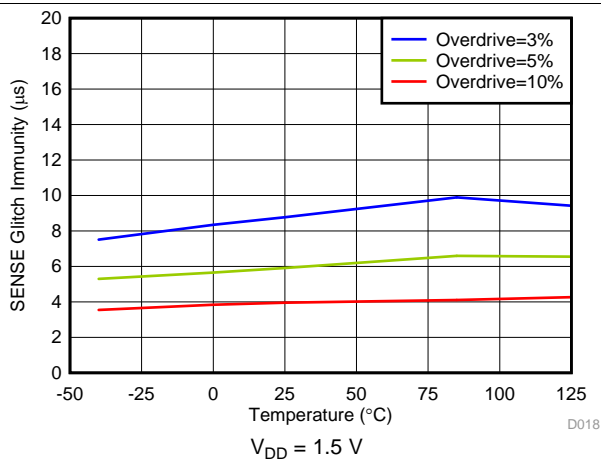


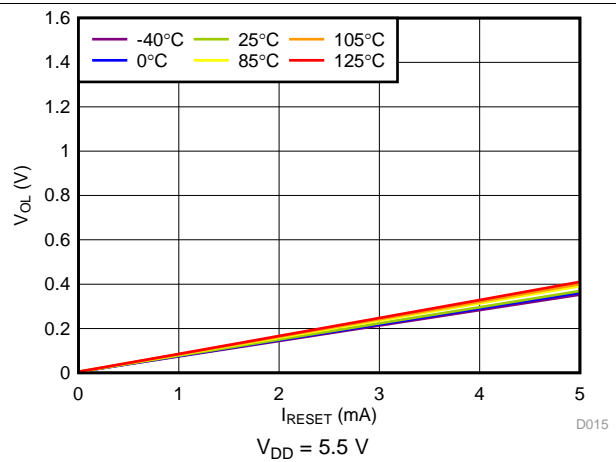
Figure 19. High-to-Low Glitch Immunity vs Temperature

**Typical Characteristics (continued)**

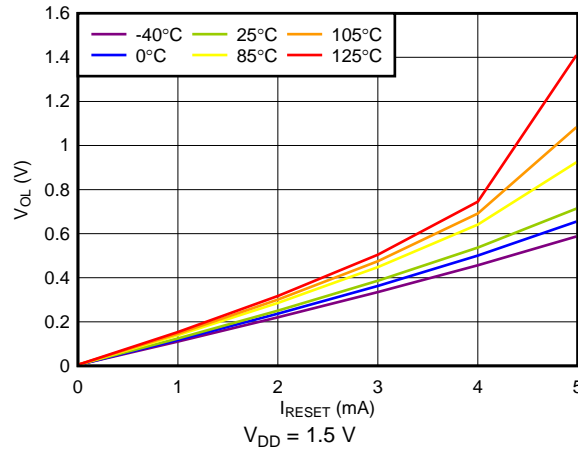
over the operating junction temperature range of  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $1.5\text{ V} \leq V_{\text{DD}} \leq 5.5\text{ V}$ , and  $\overline{\text{MR}} = V_{\text{DD}}$  (unless otherwise noted)



⊠ 20. High-to-Low Glitch Immunity vs Temperature



⊠ 21. Low-Level Output Voltage vs RESET Current



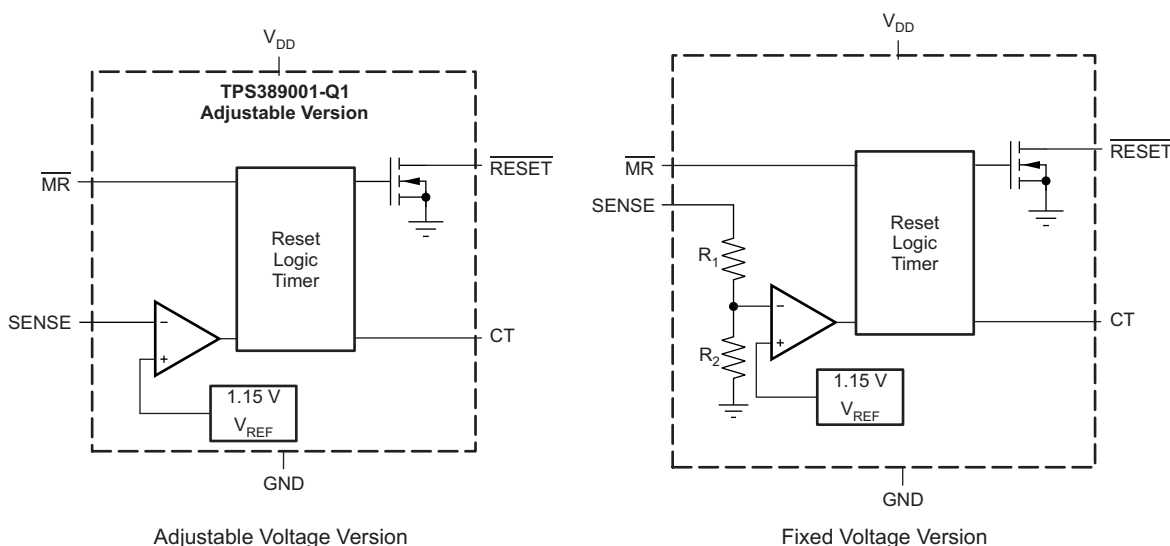
⊠ 22. Low-Level Output Voltage vs RESET Current

## 8 Detailed Description

### 8.1 Overview

The TPS3890-Q1 supervisory product family is designed to assert a  $\overline{\text{RESET}}$  signal when either the SENSE pin voltage drops below  $V_{\text{ITN}}$  or the manual reset ( $\overline{\text{MR}}$ ) is driven low. The  $\overline{\text{RESET}}$  output remains asserted for a user-adjustable time after both the manual reset ( $\overline{\text{MR}}$ ) and SENSE voltages return above their respective thresholds.

### 8.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

### 8.3 Feature Description

The combination of user-adjustable reset delay time with a broad range of threshold voltages allow these devices to be used in a wide array of applications. Fixed negative threshold voltages ( $V_{\text{ITN}}$ ) can be factory set from 1.15 V to 3.17 V (see the [Device Comparison Table](#) for available options), and the adjustable device can be used to customize the threshold voltage for other application needs by using an external resistor divider. The CT pin allows the reset delay to be set between 25  $\mu\text{s}$  and 30 s with the use of an external capacitor.

#### 8.3.1 User-Configurable $\overline{\text{RESET}}$ Delay Time

The rising  $\overline{\text{RESET}}$  delay time ( $t_{\text{PD}(r)}$ ) can be configured by installing a capacitor connected to the CT pin. The TPS3890-Q1 uses a CT pin charging current ( $I_{\text{CT}}$ ) of 1.15  $\mu\text{A}$  to help counter the effect of capacitor and board-level leakage currents that can be substantial in certain applications. The rising  $\overline{\text{RESET}}$  delay time can be set to any value between 25  $\mu\text{s}$  (no  $C_{\text{CT}}$  installed) and 30 s ( $C_{\text{CT}} = 26 \mu\text{F}$ ).

The capacitor value needed for a given delay time can be calculated using [式 1](#):

$$t_{\text{PD}(r)} (\text{SEC}) = C_{\text{CT}} \times V_{\text{CT}} \div I_{\text{CT}} + t_{\text{PD}(r)(\text{nom})} \quad (1)$$

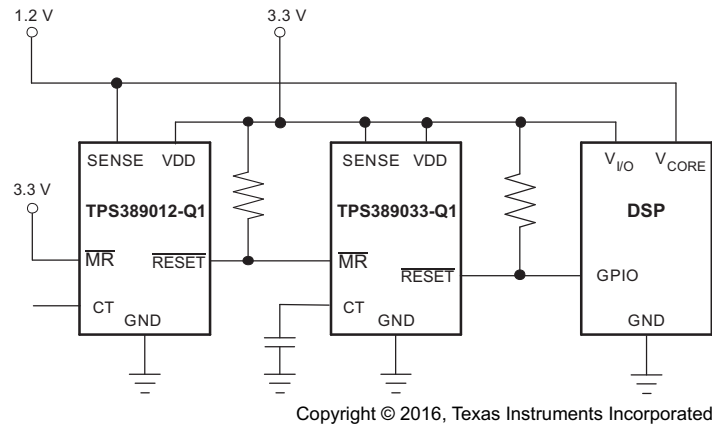
The slope of [式 1](#) is determined by the time that the CT charging current ( $I_{\text{CT}}$ ) takes to charge the external capacitor up to the CT comparator threshold voltage ( $V_{\text{CT}}$ ). When  $\overline{\text{RESET}}$  is asserted, the capacitor is discharged through the internal CT pulldown resistor ( $R_{\text{CT}}$ ). When the  $\overline{\text{RESET}}$  conditions are cleared, the internal precision current source is enabled and begins to charge the external capacitor and when the voltage on this capacitor reaches 1.22 V,  $\overline{\text{RESET}}$  is deasserted. Note that in order to minimize the difference between the calculated  $\overline{\text{RESET}}$  delay time and the actual  $\overline{\text{RESET}}$  delay time, use a low-leakage type capacitor (such as a ceramic capacitor) and minimize parasitic board capacitance around this pin.

## Feature Description (continued)

### 8.3.2 Manual Reset ( $\overline{\text{MR}}$ ) Input

The manual reset ( $\overline{\text{MR}}$ ) input allows a processor or other logic circuits to initiate a reset. A logic low on  $\overline{\text{MR}}$  causes  $\overline{\text{RESET}}$  to assert. After  $\overline{\text{MR}}$  returns to a logic high and  $\text{SENSE}$  is above  $V_{\text{ITP}}$ ,  $\overline{\text{RESET}}$  is deasserted after the user-defined reset delay. If  $\overline{\text{MR}}$  is not controlled externally, then  $\overline{\text{MR}}$  must be connected to  $V_{\text{DD}}$ . Note that if the logic signal driving  $\overline{\text{MR}}$  is not greater than or equal to  $V_{\text{DD}}$ , then some additional current flows into  $V_{\text{DD}}$  and out of  $\overline{\text{MR}}$  and the difference is apparent when comparing [Figure 8](#) and [Figure 9](#).

[Figure 23](#) shows how  $\overline{\text{MR}}$  can be used to monitor multiple system voltages when only a single CT capacitor is needed to set the  $\overline{\text{RESET}}$  delay time.



**Figure 23. Using  $\overline{\text{MR}}$  to Monitor Multiple System Voltages**

### 8.3.3 $\overline{\text{RESET}}$ Output

$\overline{\text{RESET}}$  remains high (deasserted) as long as  $\text{SENSE}$  is above the positive threshold ( $V_{\text{ITP}}$ ) and the manual reset signal ( $\overline{\text{MR}}$ ) is logic high. If  $\text{SENSE}$  falls below the negative threshold ( $V_{\text{ITN}}$ ) or if  $\overline{\text{MR}}$  is driven low, then  $\overline{\text{RESET}}$  is asserted, driving the  $\overline{\text{RESET}}$  pin to a low impedance.

When  $\overline{\text{MR}}$  is again logic high and  $\text{SENSE}$  is above  $V_{\text{ITP}}$ , a delay circuit is enabled that holds  $\overline{\text{RESET}}$  low for a specified reset delay period ( $t_{\text{PD}(r)}$ ). When the reset delay has elapsed, the  $\overline{\text{RESET}}$  pin goes to a high-impedance state and uses a pullup resistor to hold  $\overline{\text{RESET}}$  high. Connect the pullup resistor to the proper voltage rail to enable the outputs to be connected to other devices at the correct interface voltage level.  $\overline{\text{RESET}}$  can be pulled up to any voltage up to 5.5 V, independent of the device supply voltage. To ensure proper voltage levels, give some consideration when choosing the pullup resistor values. The pullup resistor value is determined by  $V_{\text{OL}}$ , the output capacitive loading, and the output leakage current ( $I_{\text{LKG(OD)}}$ ).

### 8.3.4 SENSE Input

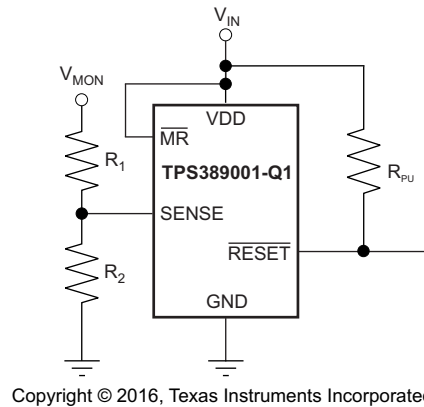
The  $\text{SENSE}$  input can vary from ground to 5.5 V (7.0 V, absolute maximum), regardless of the device supply voltage used. The  $\text{SENSE}$  pin is used to monitor the critical voltage rail. If the voltage on this pin drops below  $V_{\text{ITN}}$ , then  $\overline{\text{RESET}}$  is asserted. When the voltage on the  $\text{SENSE}$  pin exceeds the positive threshold voltage,  $\overline{\text{RESET}}$  deasserts after the user-defined  $\overline{\text{RESET}}$  delay time.

The internal comparator has built-in hysteresis to ensure well-defined  $\overline{\text{RESET}}$  assertions and deassertions even when there are small changes on the voltage rail being monitored.

The TPS3890-Q1 device is relatively immune to short transients on the  $\text{SENSE}$  pin. Glitch immunity is dependent on threshold overdrive, as illustrated in [Figure 19](#) for  $V_{\text{ITN}}$  and [Figure 18](#) for  $V_{\text{ITP}}$ . Although not required in most cases, for noisy applications good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the  $\text{SENSE}$  input to reduce sensitivity to transient voltages on the monitored signal.

## Feature Description (continued)

The adjustable version (TPS389001-Q1) can be used to monitor any voltage rail down to 1.15 V using the circuit shown in [Figure 24](#).



**Figure 24. Using the TPS389001-Q1 to Monitor a User-Defined Threshold Voltage**

The target threshold voltage for the monitored supply ( $V_{ITx(MON)}$ ) and the resistor divider values can be calculated by using [Equation 2](#) and [Equation 3](#), respectively:

$$V_{ITx(MON)} = V_{ITx} \times (1 + R_1 \div R_2) \quad (2)$$

[Equation 3](#) can be used to calculate either the negative threshold or the positive threshold by replacing  $V_{ITx}$  with either  $V_{ITN}$  or  $V_{ITP}$ , respectively.

$$R_{TOTAL} = R_1 + R_2 \quad (3)$$

Resistors with high values minimize current consumption; however, the input bias current of the device degrades accuracy if the current through the resistors is too low. Therefore, choosing an  $R_{TOTAL}$  value so that the current through the resistor divider is at least 100 times larger than the SENSE input current is simplest. See the [Optimizing Resistor Dividers at a Comparator Input](#) application report for more details on sizing input resistors.

### 8.3.4.1 Immunity to SENSE Pin Voltage Transients

The TPS3890-Q1 is immune to short voltage transient spikes on the input pins. Sensitivity to transients depends on both transient duration and overdrive (amplitude) of the transient. Overdrive is defined by how much  $V_{SENSE}$  exceeds the specified threshold, and is important to know because the smaller the overdrive, the slower the response of the outputs (that is, undervoltage and overvoltage). Threshold overdrive is calculated as a percent of the threshold in question, as shown in [Equation 4](#).

$$\text{Overdrive} = | (V_{SENSE} / V_{ITx} - 1) \times 100\% | \quad (4)$$

[Figure 17](#) to [Figure 20](#) illustrate the glitch immunity that the TPS3890-Q1 has versus temperature with three different overdrive voltages. The propagation delay versus overdrive curves ([Figure 13](#) to [Figure 16](#)) can be used to determine how sensitive the TPS3890-Q1 family of devices are across an even wider range of overdrive voltages.

## 8.4 Device Functional Modes

表 1 summarizes the various functional modes of the device.

表 1. Truth Table

$V_{DD}$	$\overline{MR}$	SENSE	$\overline{RESET}$
$V_{DD} < V_{POR}$	—	—	Undefined
$V_{POR} < V_{DD} < V_{DD(MIN)}^{(1)}$	—	—	L
$V_{DD} \geq V_{DD(MIN)}$	L	—	L
$V_{DD} \geq V_{DD(MIN)}$	H	$V_{SENSE} < V_{ITN}$	L
$V_{DD} \geq V_{DD(MIN)}$	H	$V_{SENSE} > V_{ITP}$	H

(1) When  $V_{DD}$  falls below  $V_{DD(MIN)}$ , undervoltage-lockout (UVLO) takes effect and  $\overline{RESET}$  is held low until  $V_{DD}$  falls below  $V_{POR}$ .

### 8.4.1 Normal Operation ( $V_{DD} > V_{DD(min)}$ )

When  $V_{DD}$  is greater than  $V_{DD(min)}$ , the  $\overline{RESET}$  signal is determined by the voltage on the SENSE pin and the logic state of  $\overline{MR}$ .

- $\overline{MR}$  high: when the voltage on  $V_{DD}$  is greater than 1.5 V, the  $\overline{RESET}$  signal corresponds to the voltage on the SENSE pin relative to the threshold voltage.
- $\overline{MR}$  low: in this mode,  $\overline{RESET}$  is held low regardless of the voltage on the SENSE pin.

### 8.4.2 Above Power-On-Reset But Less Than $V_{DD(min)}$ ( $V_{POR} < V_{DD} < V_{DD(min)}$ )

When the voltage on  $V_{DD}$  is less than the  $V_{DD(min)}$  voltage, and greater than the power-on-reset voltage ( $V_{POR}$ ), the  $\overline{RESET}$  signal is asserted regardless of the voltage on the SENSE pin.

### 8.4.3 Below Power-On-Reset ( $V_{DD} < V_{POR}$ )

When the voltage on  $V_{DD}$  is lower than  $V_{POR}$ , the device does not have enough voltage to internally pull the asserted output low and  $\overline{RESET}$  is undefined and must not be relied upon for proper device function.

## 9 Application and Implementation

### 注

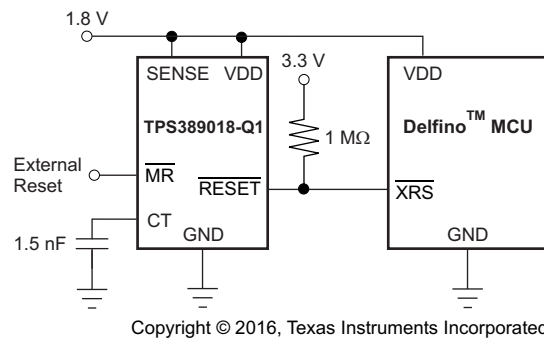
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

### 9.2 Typical Application

A typical application for the TPS389018-Q1 is shown in [Figure 25](#). The TPS389018-Q1 can be used to monitor the 1.8-V VDD rail required by the TI Delfino™ microprocessor family. The open-drain RESET output of the TPS389018-Q1 is connected to the XRS input of the microprocessor. A reset event is initiated when the VDD voltage is less than  $V_{ITN}$  or when MR is driven low by an external source.



**Figure 25. TPS3890-Q1 Monitoring the Supply Voltage for a Delfino Microprocessor**

#### 9.2.1 Design Requirements

The TPS3890-Q1 RESET output can be used to drive the reset (XRS) input of a microprocessor. The RESET pin of the TPS3890-Q1 is pulled high with a 1-MΩ resistor; the reset delay time is controlled by the CT capacitor and is set depending on the reset requirement times of the microprocessor. During power-up, XRS must remain low for at least 1 ms after VDD reaches 1.5 V for the C2000™ Delfino family of microprocessors. For 100-MHz operation, the Delfino TMS320F2833x microcontroller uses a supply voltage of 1.8 V that must be monitored by the TPS3890-Q1.

#### 9.2.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS389018-Q1 has a negative threshold of 1.73 V and a positive threshold of 1.74 V, making the device suitable for monitoring a 1.8-V rail. The secondary constraint for this application is the reset delay time that must be at least 1 ms to allow the Delfino microprocessor enough time to startup up correctly. Because a minimum time is required, the worst-case scenario is a supervisor with a high CT charging current ( $I_{CT}$ ) and a low CT comparator threshold ( $V_{CT}$ ). For applications with ambient temperatures ranging from  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ,  $C_{CT}$  can be calculated using  $I_{CT(\text{Max})}$ ,  $V_{CT(\text{MIN})}$ , and solving for  $C_{CT}$  in [Equation 1](#) such that the minimum capacitance required at the CT pin is 1.149 nF. If standard capacitors with  $\pm 20\%$  tolerances are used, then the CT capacitor must be 1.5 nF or larger to ensure that the 1-ms delay time is met.

A 0.1-μF decoupling capacitor is connected to the VDD pin as a good analog design practice and a 1-MΩ resistor is used as the RESET pullup resistor to minimize the current consumption when RESET is asserted. The MR pin can be connected to an external signal if desired or connected to VDD if not used.

## Typical Application (continued)

### 9.2.3 Application Curve

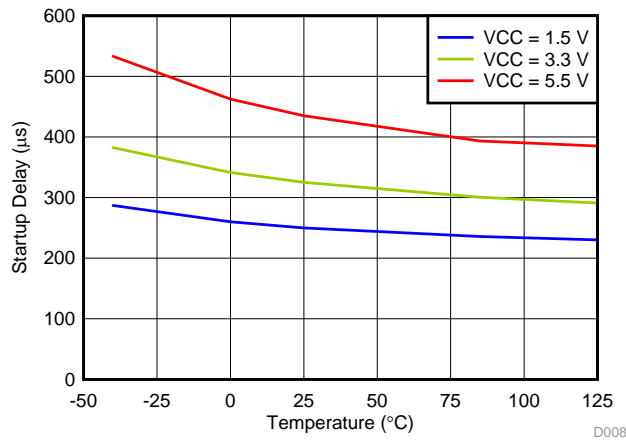


Figure 26. Startup Delay vs Temperature

## 10 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.5 V and 5.5 V. An input supply capacitor is not required for this device; however, if the input supply is noisy, then good analog practice is to place a 0.1- $\mu$ F capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.



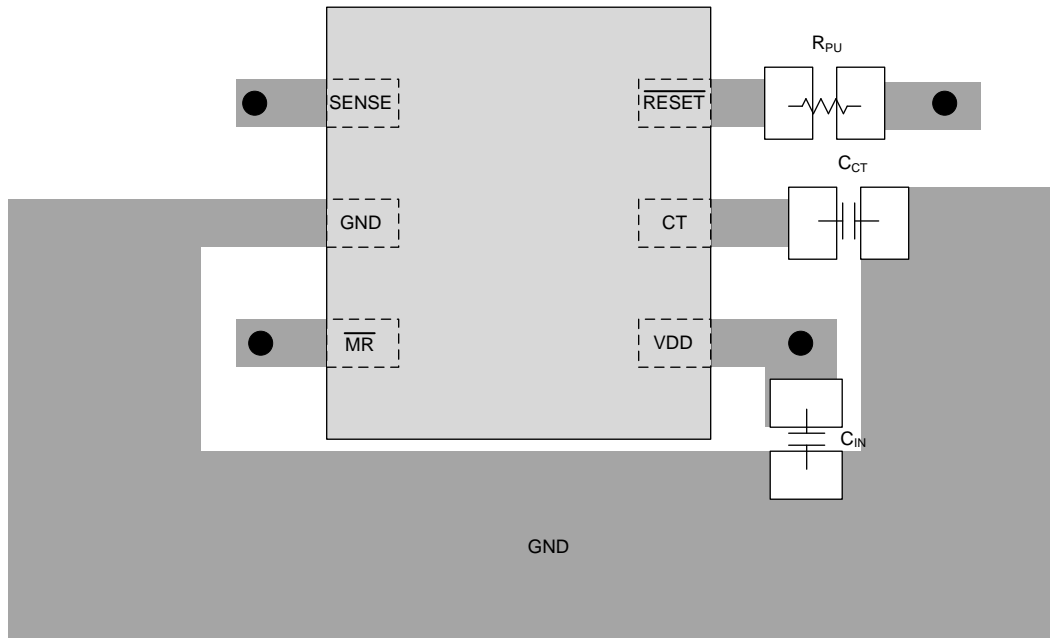
## 11 Layout

### 11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a 0.1- $\mu$ F ceramic capacitor near the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the  $\overline{\text{RESET}}$  delay time is not adversely affected.

### 11.2 Layout Example

The layout example in shows how the TPS3890-Q1 is laid out on a printed circuit board (PCB) with a user-defined delay.



● Vias used to connect pins for application-specific connections

### ☒ 27. Recommended Layout

## 12 デバイスおよびドキュメントのサポート

### 12.1 デバイス・サポート

#### 12.1.1 デバイスの項目表記

表 2 は、TPS389033G-Q1 を例として、部品番号からデバイスの機能を解読する方法を示しています。

表 2. デバイスの命名規則

説明	項目表記	値
TPS3890 (高精度のスーパーバイザ・ファミリ)	—	—
33 (監視対象の公称レール電圧)	10	1.0V
	12	1.2V
	18	1.8V
	33	3.3V
	50	5.0V
G ( $V_{ITN}$ が公称レール電圧の何%下か)	—	4%
	G	7%
	K	11%
	L	12%
Q1 (車載用バージョン)	—	—

### 12.2 ドキュメントのサポート

#### 12.2.1 関連資料

関連資料については、以下を参照してください。

- 『コンプレータ入力の分圧抵抗の最適化』
- 『電源設計用の感度分析』
- 『TMS320C28x デジタル信号コントローラの基礎』
- 『TPS3890EVM-775 評価モジュール・ユーザー・ガイド』
- 『C2000 Delfino ファミリのマイクロプロセッサ』
- 『TMS320F2833x デジタル信号コントローラ(DCS)』

#### 12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com) のデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ オンライン・コミュニティ** *TI の E2E (Engineer-to-Engineer) コミュニティ*。エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.com では、他のエンジニアに質問し、知識を共有し、アイデアを検討して、問題解決に役立てることができます。

**設計サポート** *TI の設計サポート* 役に立つ E2E フォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

## 12.5 商標

Delfino, C2000, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

## 12.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 12.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS389001QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2N	<a href="#">Samples</a>
TPS389012QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2O	<a href="#">Samples</a>
TPS389015QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2P	<a href="#">Samples</a>
TPS389018QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2Q	<a href="#">Samples</a>
TPS389025QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2R	<a href="#">Samples</a>
TPS389030QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2S	<a href="#">Samples</a>
TPS389033GQDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7V	<a href="#">Samples</a>
TPS389033KQDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7W	<a href="#">Samples</a>
TPS389033QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	2T	<a href="#">Samples</a>
TPS389050GQDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7T	<a href="#">Samples</a>
TPS389050LQDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7U	<a href="#">Samples</a>
TPS389050QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	7S	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

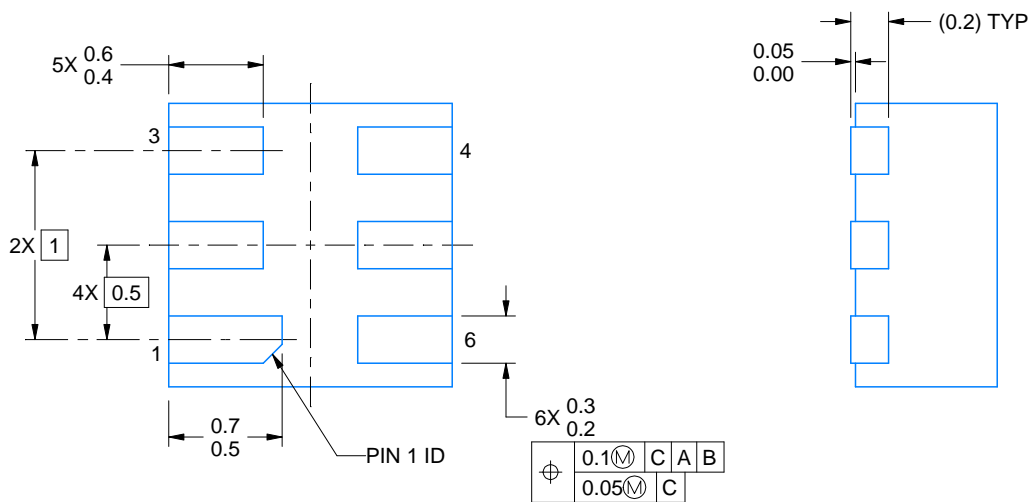
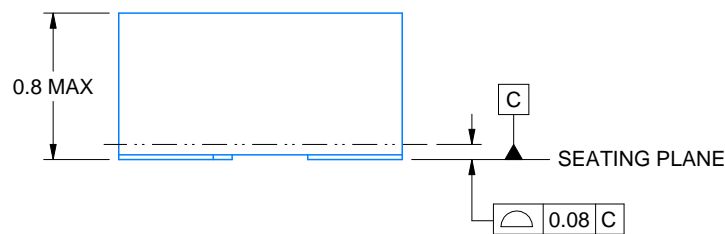
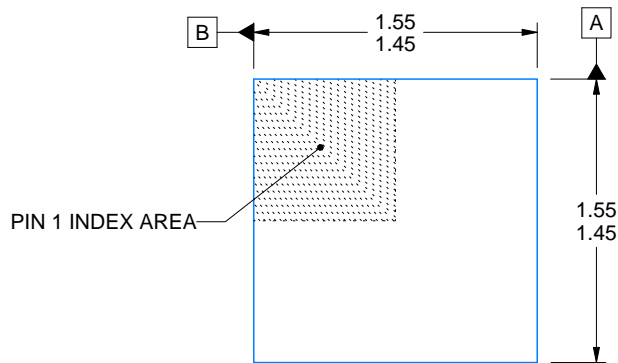
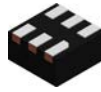

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS389001QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389012QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389015QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389018QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389025QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389030QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033GQDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033KQDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389033QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389050GQDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389050LQDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2
TPS389050QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.83	1.83	0.89	4.0	8.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS389001QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389012QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389015QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389018QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389025QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389030QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389033GQDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389033KQDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389033QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389050GQDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389050LQDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0
TPS389050QDSERQ1	WSON	DSE	6	3000	183.0	183.0	20.0



4220552/B 01/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

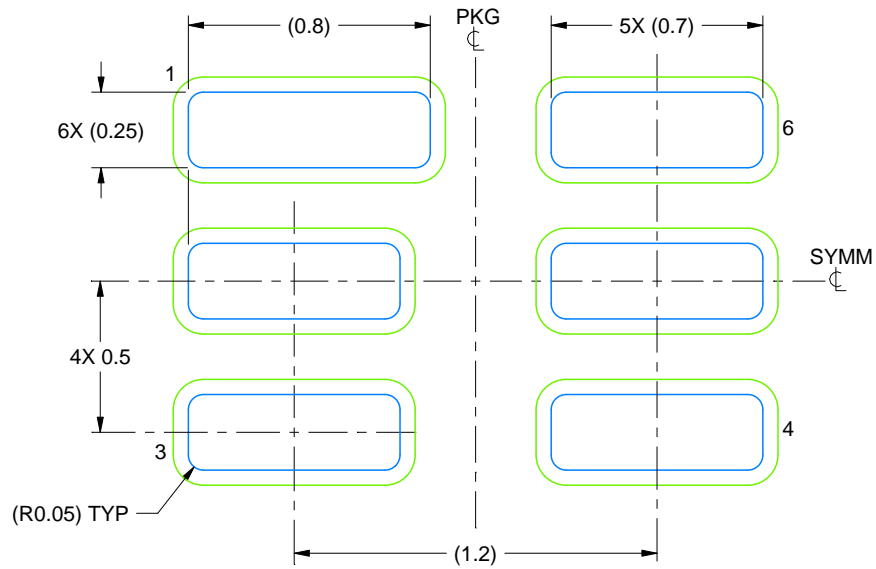


# EXAMPLE BOARD LAYOUT

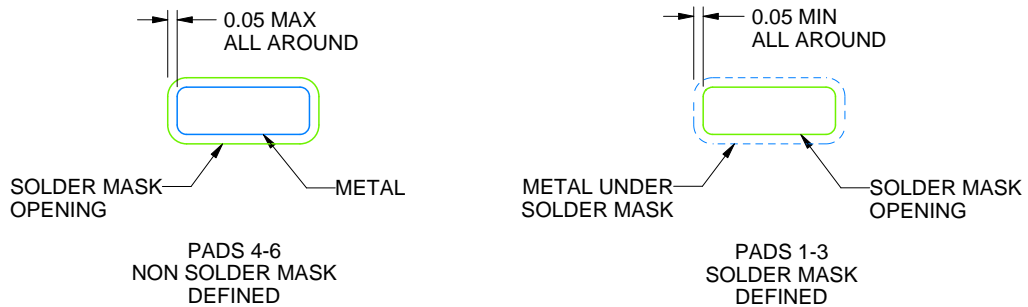
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

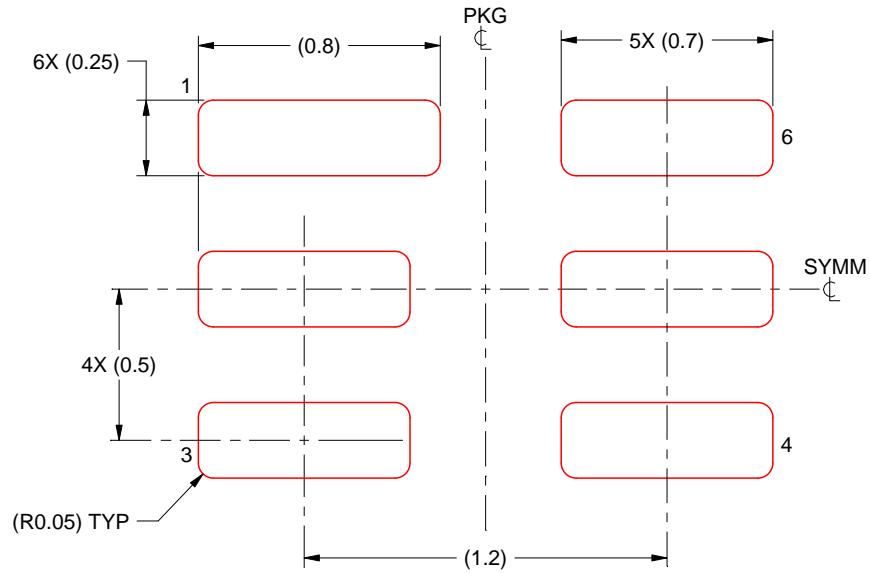
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要なお知らせと免責事項

TI は、技術データと信頼性データ（データシートを含みます）、設計リソース（リファレンス・デザインを含みます）、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとし、

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、[TI の販売条件](#)、または [ti.com](#) やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated