

## TPS386596 Quad Reset Supervisor With Manual Reset Input

### 1 Features

- Four Channel Voltage Detector
- Threshold Accuracy: 0.25% (typ)
- Fixed 50-ms  $\overline{\text{RESET}}$  Delay Time
- Active-Low Manual Reset Input
- Very Low Quiescent Current: 7  $\mu\text{A}$  (Typical)
- SVS-1: Fixed Threshold for Monitoring 3.3 V
- SVS-2/3/4: Adjustable Threshold Down to 0.4 V
- Open-Drain  $\overline{\text{RESET}}$  Output
- Space-Saving, 8-pin MSOP Package

### 2 Applications

- Notebook/Desktop Computers
- Industrial Equipment
- Telecom, Networking Infrastructure
- Server, Storage Equipment
- DSP and Microcontroller Applications
- FPGA/ASIC Applications

### 3 Description

The TPS386596 device monitors four power rails and asserts the  $\overline{\text{RESET}}$  signal when any of the SENSE inputs drop below the respective thresholds. SVS-1 can be used to monitor a 3.3-V nominal power supply with no external components required. SVS-2, SVS-3, and SVS-4 are adjustable using external resistors and can be used to monitor any power-supply voltage higher than 0.4 V. All SENSE inputs have a threshold accuracy of 0.25% (typical). The TPS386596L33 also has an active-low manual reset ( $\overline{\text{MR}}$ ) that can assert the  $\overline{\text{RESET}}$  signal as desired by the application. The open-drain, active-low  $\overline{\text{RESET}}$  output deasserts after a fixed 50-ms delay.

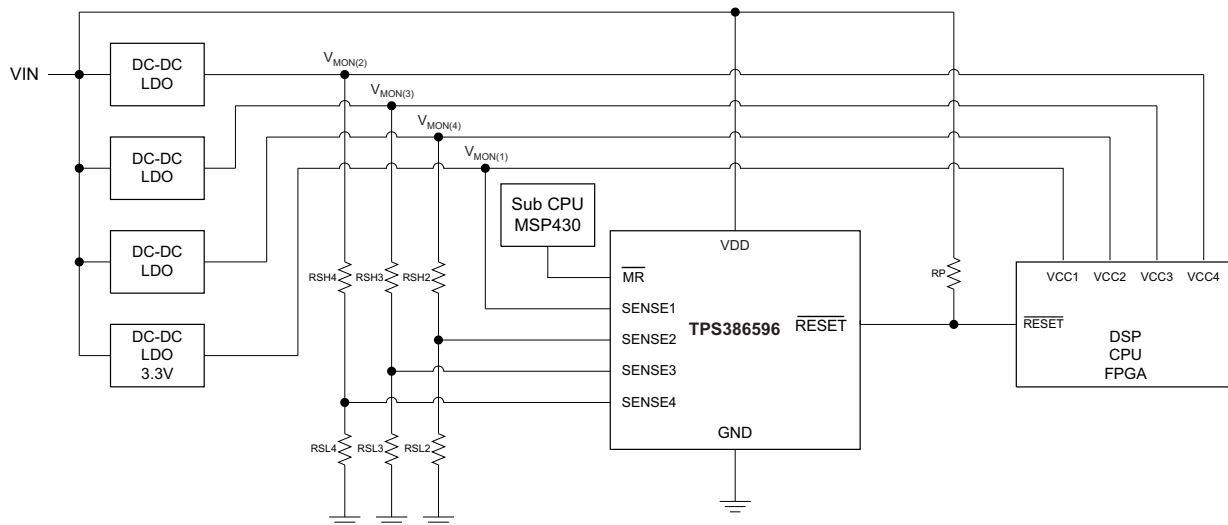
The TPS386596 has a low quiescent current of 7  $\mu\text{A}$  (typical) and is available in a space-saving, 8-pin MSOP package.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS386596	VSSOP (8)	5.00 mm x 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### TPS386596 Typical Application Circuit



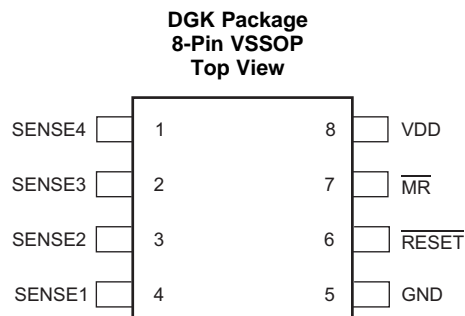
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## 4 Revision History

Changes from Original (July 2010) to Revision A	Page
• Changed references to <i>TPS386596L33</i> to <i>TPS386596</i> throughout document .....	<b>1</b>
• Changed <i>Pin Configuration and Functions</i> section; updated table format and pin drawing .....	<b>3</b>
• Changed "free-air temperature" to "junction temperature" in <i>Absolute Maximum Ratings</i> condition statement .....	<b>4</b>
• Changed <i>Absolute Maximum Ratings</i> table; moved ESD ratings to separate table .....	<b>4</b>
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>4</b>
• Changed <i>Thermal Information</i> table; updated thermal resistance values .....	<b>4</b>
• Changed <i>Electrical Characteristics</i> table; moved timing and switching parameters ( $t_W$ , $t_D$ ) to separate tables .....	<b>5</b>
• Changed input voltage range notation from $V_{VCC}$ to $V_{DD}$ throughout <i>Electrical Characteristics</i> table .....	<b>5</b>
• Changed supply current notation from $I_{VCC}$ to $I_{DD}$ in <i>Electrical Characteristics</i> table .....	<b>5</b>
• Changed VCC notation in <i>Functional Block Diagram</i> to VDD .....	<b>10</b>
• Deleted <i>Immunity to SENSE Pin Voltage Transients</i> section; rewrote content and added to <i>Voltage Monitoring</i> section .....	<b>11</b>
• Changed <i>Sense Inputs</i> section title to <i>Undervoltage Detection</i> .....	<b>12</b>
• Changed title and graphic for <a href="#">Figure 14</a> .....	<b>12</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	5	—	Ground
$\overline{\text{MR}}$	7	I	Manual reset input with internal 100-k $\Omega$ pullup to VDD and 50-ns deglitch. Logic low level of this pin asserts $\overline{\text{RESET}}$ .
$\overline{\text{RESET}}$	6	O	$\overline{\text{RESET}}$ is an open-drain output pin. When $\overline{\text{RESET}}$ is asserted, this pin remains in a low-impedance state. When $\overline{\text{RESET}}$ is deasserted, this pin goes to a high-impedance state after 50 ms. A pullup resistor to VDD or another voltage source is required.
SENSE1	4	I	Monitor voltage input for Supply 1 When the voltage at this terminal drops the threshold voltage ( $V_{IT1} = 2.9$ V), $\overline{\text{RESET}}$ is asserted.
SENSE2	3	I	Monitor voltage input for Supply 2 When the voltage at this terminal drops the threshold voltage ( $V_{IT2} = 0.4$ V), $\overline{\text{RESET}}$ is asserted.
SENSE3	2	I	Monitor voltage input for Supply 3 When the voltage at this terminal drops the threshold voltage ( $V_{IT3} = 0.4$ V), $\overline{\text{RESET}}$ is asserted.
SENSE4	1	I	Monitor voltage input for Supply 4 When the voltage at this terminal drops the threshold voltage ( $V_{IT4} = 0.4$ V), $\overline{\text{RESET}}$ is asserted.
VDD	8	I	Supply voltage. Connecting a 0.1- $\mu$ F ceramic capacitor close to this pin is recommended.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating junction temperature range (unless otherwise noted).<sup>(1) (2)</sup>

		MIN	MAX	UNIT
Voltage	Input, $V_{DD}$	-0.3	7	V
	$\overline{V_{MR}}$ , $V_{SENSE1}$ , $V_{SENSE2}$ , $V_{SENSE3}$ , $V_{SENSE4}$ , $\overline{V_{RESET}}$	-0.3	7	V
Current	$\overline{RESET}$ pin		5	mA
Power dissipation	Continuous total	See <a href="#">Thermal Information</a>		
Temperature	Operating virtual junction, $T_J$	-40	150	°C
	Operating ambient, $T_A$	-40	125	
	Storage, $T_{stg}$	-65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) As a result of the low dissipated power in this device, it is assumed that  $T_J = T_A$ .

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted).

	MIN	NOM	MAX	UNIT
$V_{DD}$	1.8		6.5	V
$V_{SENSE}$ <sup>(1)</sup>	0		$V_{DD}$	V
$V_{MR}$	0		$V_{DD}$	V
$\overline{V_{RESET}}$	0		6.5	V
$R_{PULL-UP}$	6.5	100	10,000	k $\Omega$
$T_J$	-40	25	125	°C

- (1) All sense inputs.

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS386596	UNIT
		DGK (VSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	174	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	94	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1.9	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	92.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Over the operating temperature range of  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ .  $1.8\text{ V} < V_{DD} < 6.5\text{ V}$ ,  $R_{\overline{\text{RESET}}} = 100\text{ k}\Omega$  to  $V_{DD}$ ,  $C_{\overline{\text{RESET}}} = 50\text{ pF}$  to GND, unless otherwise noted. Typical values are at  $T_J = 25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{DD}$	Input supply		1.8		6.5	V
$I_{DD}$	Supply current (current into VDD pin)	$V_{CC} = 3.3\text{ V}$ , $\overline{\text{RESET}}$ not asserted		7	19	$\mu\text{A}$
		$V_{CC} = 6.5\text{ V}$ , $\overline{\text{RESET}}$ not asserted		7.5	22	$\mu\text{A}$
	Power-on reset voltage <sup>(1) (2)</sup>	$V_{OL(max)} = 0.2\text{ V}$ , $I_{\overline{\text{RESET}}} = 15\text{ }\mu\text{A}$			0.9	V
$V_{ITn}$	Negative-going input threshold accuracy	SENSE1	2.87	2.90	2.93	V
		SENSE2, SENSE3, SENSE4	396	400	404	mV
$V_{HYS}$	Hysteresis (positive-going) on $V_{ITn}$	SENSE1		25	72	mV
		SENSE2, SENSE3, SENSE4		3.5	10	mV
$I_{SENSE1}$	Input current at SENSE1	$V_{SENSE1} = 3.3\text{ V}$	2.2	2.75	3.3	$\mu\text{A}$
$I_{SENSEn}$	Input current at SENSEn pin, n = 2, 3, 4	$V_{SENSEn} = 0.42\text{ V}$	-25		25	nA
$t_d$	$\overline{\text{RESET}}$ delay time		30	50	70	ms
$V_{IL}$	$\overline{\text{MR}}$ logic low input		0		$0.3V_{DD}$	V
$V_{IH}$	$\overline{\text{MR}}$ logic high input		$0.7V_{DD}$			V
$R_{MR\_Pullup}$	Internal pullup resistor on $\overline{\text{MR}}$ pin to $V_{DD}$			100		k $\Omega$
$V_{OL}$	Low-level $\overline{\text{RESET}}$ output voltage	$I_{OL} = 1\text{ mA}$			0.4	V
		SENSEn = 0 V, $1.3\text{ V} < V_{DD} < 1.8\text{ V}$ , $I_{OL} = 0.4\text{ mA}$ <sup>(1)</sup>			0.3	
$I_{LKG}$	$\overline{\text{RESET}}$ leakage current	$V_{\overline{\text{RESET}}} = 6.5\text{ V}$ , $\overline{\text{RESET}}$ not asserted	-300		300	nA
$C_{IN}$	Input pin capacitance			5		pF

(1) These specifications are out of recommended  $V_{DD}$  range and only define  $\overline{\text{RESET}}$  output performance during  $V_{DD}$  ramp up.

(2) The lowest supply voltage ( $V_{DD}$ ) at which  $\overline{\text{RESET}}$  becomes active.  $t_{RISE(VDD)} \geq 15\text{ }\mu\text{s/V}$ .

### 6.6 Timing Requirements

Over the operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .  $1.8\text{ V} < V_{DD} < 6.5\text{ V}$ ,  $R_{\overline{\text{RESET}}} = 100\text{ k}\Omega$  to  $V_{DD}$ ,  $C_{\overline{\text{RESET}}} = 50\text{ pF}$  to GND, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

		MIN	NOM	MAX	UNIT
$t_w$	Input pulse width to SENSEn and MR pins	SENSEm: $1.05 V_{IT} \geq 0.95 V_{IT}$		4	$\mu\text{s}$
		$\overline{\text{MR}}$ : $0.7 V_{DD} \geq 0.3 V_{DD}$		50	ns

### 6.7 Switching Characteristics

Over the operating temperature range of  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .  $1.8\text{ V} < V_{DD} < 6.5\text{ V}$ ,  $R_{\overline{\text{RESET}}} = 100\text{ k}\Omega$  to  $V_{DD}$ ,  $C_{\overline{\text{RESET}}} = 50\text{ pF}$  to GND, unless otherwise noted. Typical values are at  $T_J = 25^{\circ}\text{C}$ .

		MIN	TYP	MAX	UNIT
$t_D$	$\overline{\text{RESET}}$ delay time	30	50	70	ms

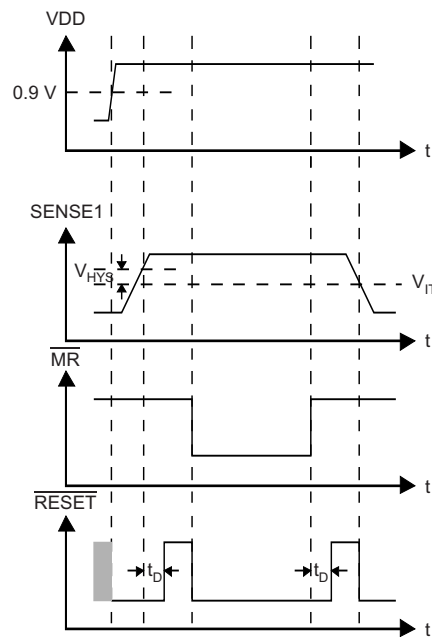
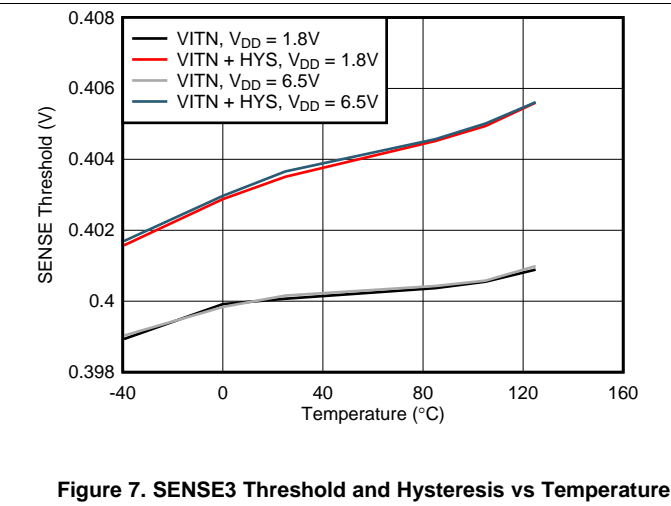
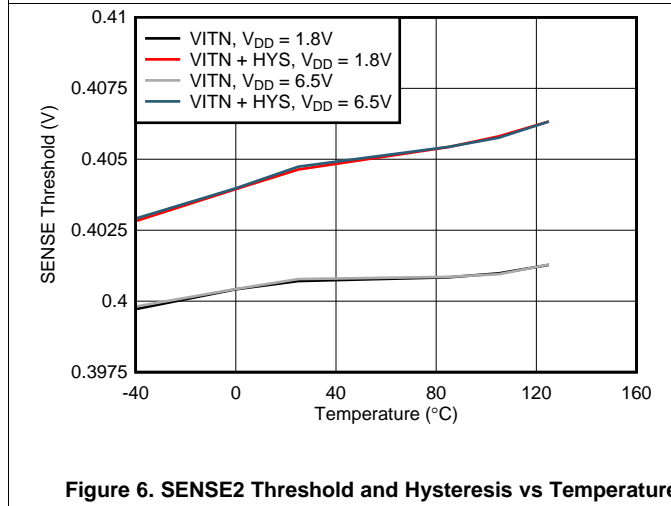
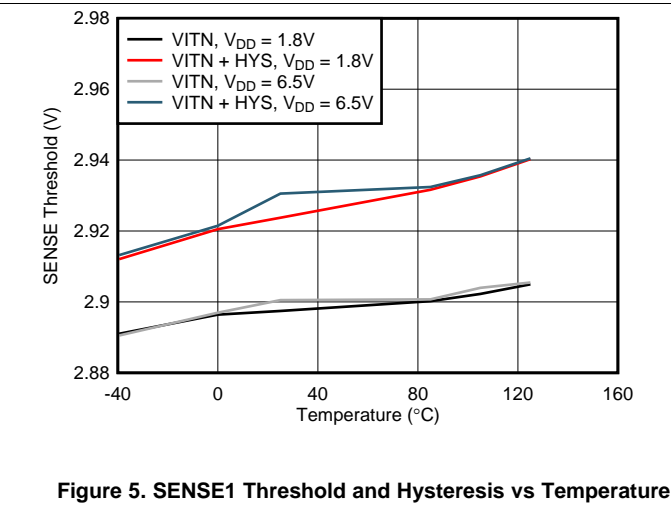
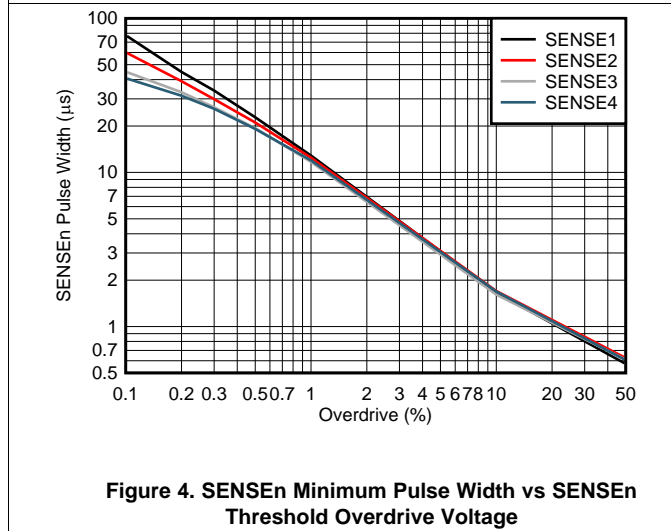
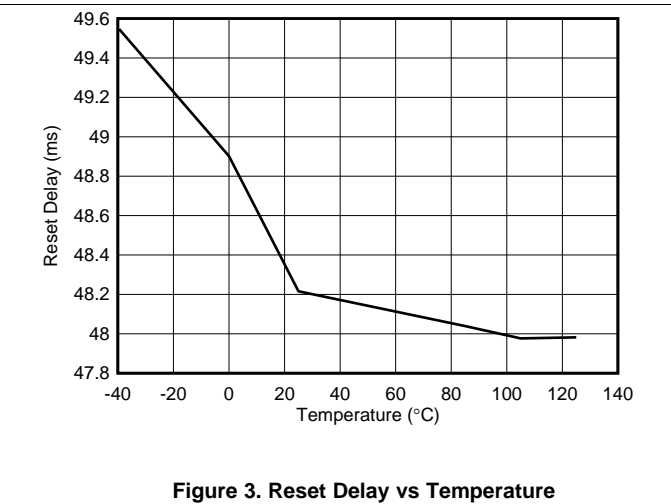
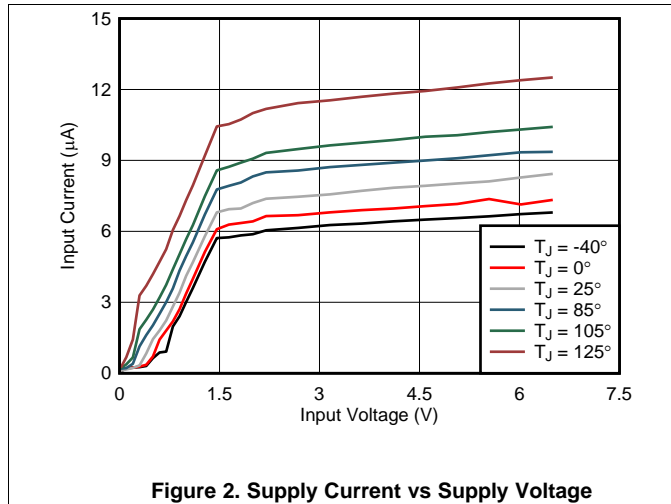


Figure 1. Timing Diagram

## 6.8 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ , and  $V_{DD} = 3.3\text{ V}$ , unless otherwise noted.



Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ , and  $V_{DD} = 3.3\text{ V}$ , unless otherwise noted.

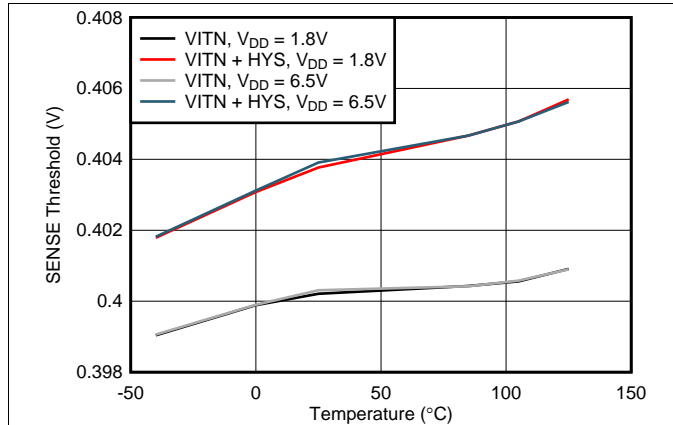


Figure 8. SENSE4 Threshold and Hysteresis vs Temperature

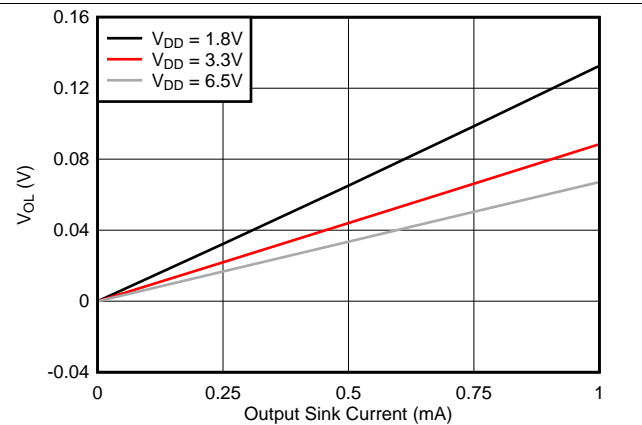


Figure 9. Output Voltage Low vs Output Current

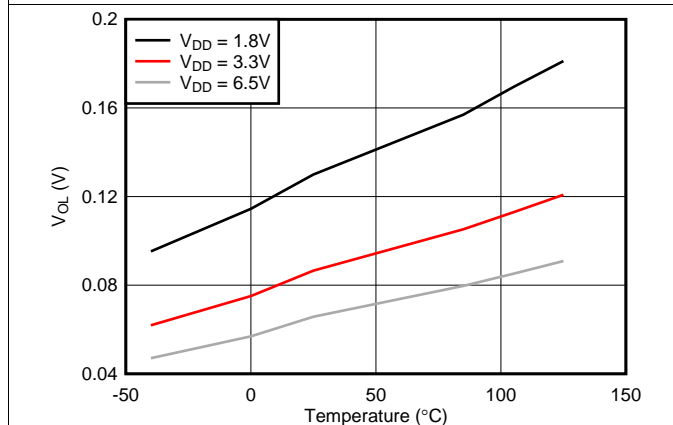


Figure 10. Output Voltage Low at 1 mA vs Temperature

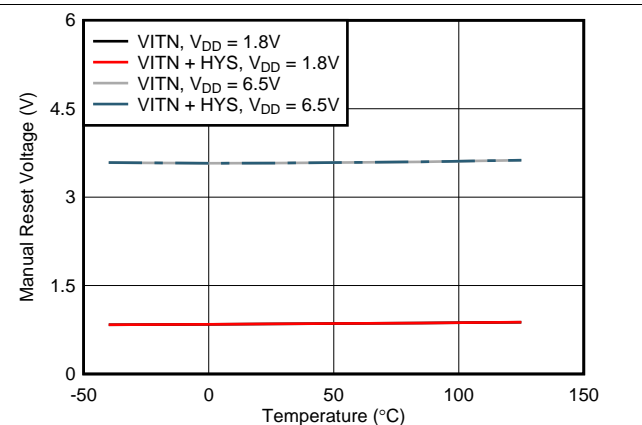


Figure 11.  $\overline{\text{MR}}$  Threshold vs Temperature

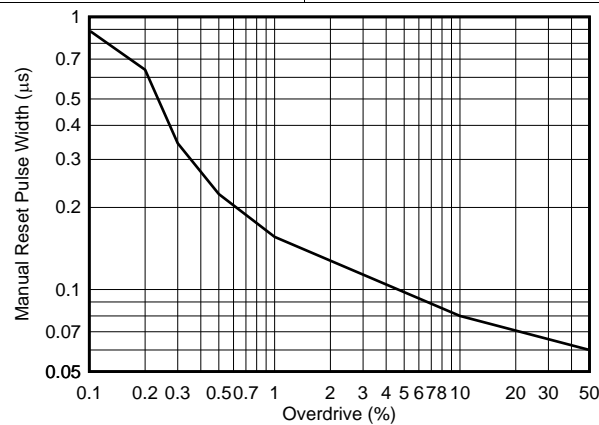
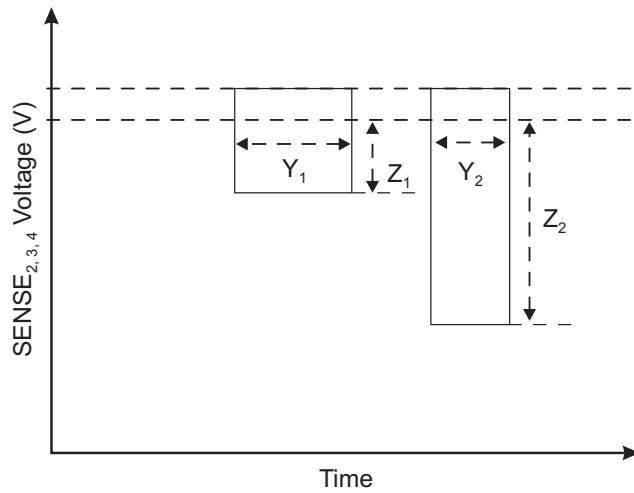


Figure 12.  $\overline{\text{MR}}$  Minimum Pulse Width vs  $\overline{\text{MR}}$  Threshold Overdrive Voltage



## 7 Parameter Measurement Information



$$X_1 = (Z_1/0.4) * 100(\%)$$

$$X_2 = (Z_2/0.4) * 100(\%)$$

$X_1 = X_2$  are overdrive (%) values calculated from actual  $SENSE_{2,3,4}$  voltage amplitudes measured as  $Z_1$  and  $Z_2$ .

$Y_N$  is the minimum pulse width that gives RESET transition. Greater  $Z_N$  produces shorter  $Y_N$ .

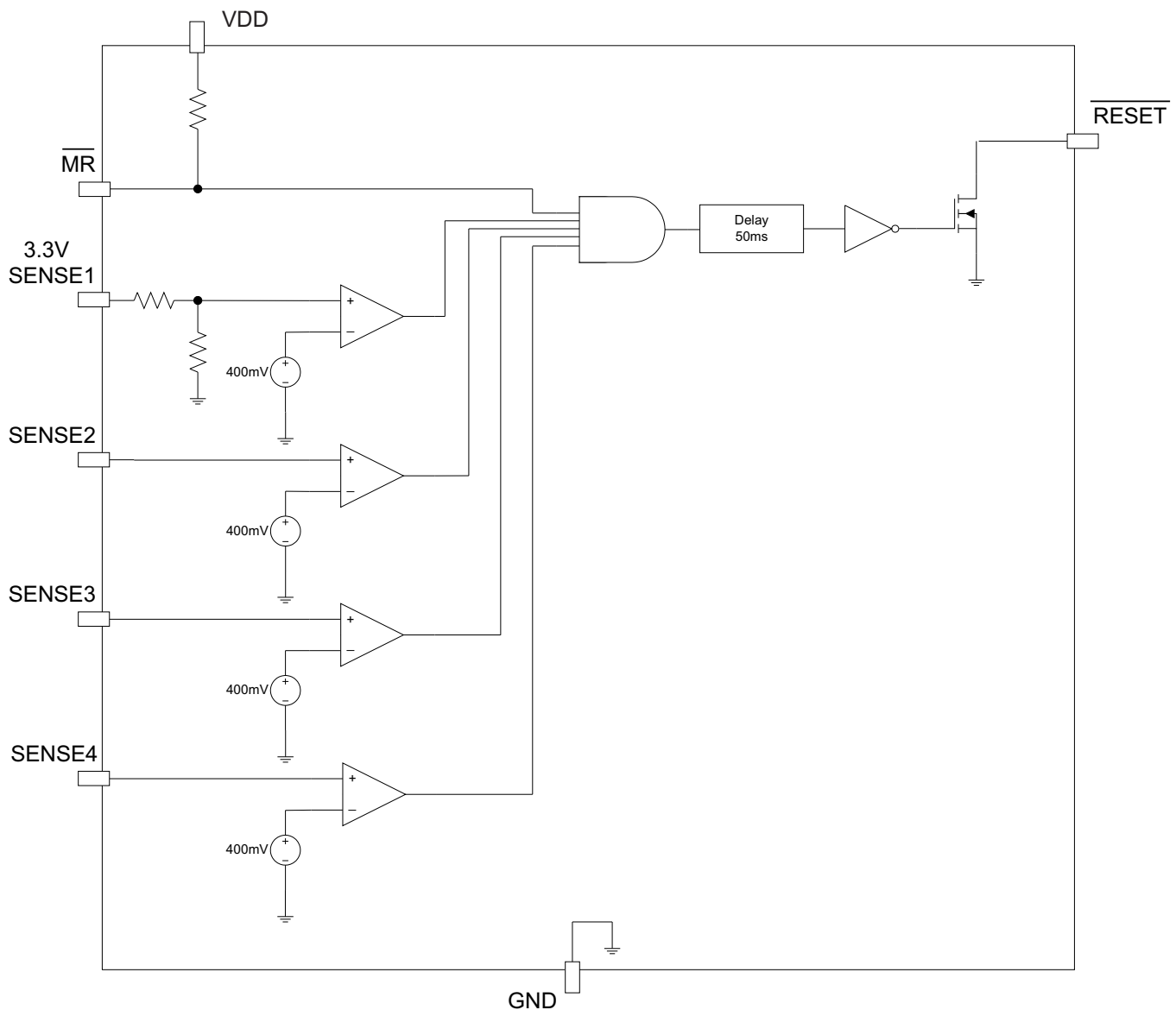
**Figure 13. Overdrive Measurement Method: Measurement Technique for Immunity to SENSE Pin Voltage Transient**

## 8 Detailed Description

### 8.1 Overview

The TPS386596L33 multi-channel reset supervisor provides a complete single reset function for a four power supply system. The design of the SVS is based on the TPS386000 quad supervisor device series. The TPS386596 is designed to assert the  $\overline{\text{RESET}}$  signal following the logic in Table 1. The  $\overline{\text{RESET}}$  output remains asserted for a 50-ms delay time ( $t_d$ ) after the event of reset release. The SENSE1 input has a fixed voltage threshold designed to monitor a 3.3-V nominal supply. The trip point,  $V_{IT1}$ , for SENSE1 is 2.90 V (typical). Each of the remaining SENSE $n$  inputs ( $n = 2, 3, 4$ ) can be set to any voltage threshold greater than 0.4 V using an external resistor divider. An active-low manual reset ( $\overline{\text{MR}}$ ) input is also provided for asserting the  $\overline{\text{RESET}}$  signal as desired by the system, regardless of the voltage on any of the SENSE pins.

### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Voltage Monitoring

Each SENSE<sub>n</sub> (n = 2, 3, 4) pin can be set to monitor any voltage threshold greater than 0.4 V using an external resistor divider. The SENSE1 pin is designed to monitor a 3.3-V supply with a 2.9-V threshold. A broad range of voltage thresholds can be supported, allowing these devices to be used in a wide array of applications.

The TPS386596 is relatively immune to short negative transients on the SENSE<sub>n</sub> pin. Sensitivity to transients depends on threshold overdrive, as shown in the typical performance graph *TPS386596 SENSE<sub>n</sub> Minimum Pulse Width vs SENSE<sub>n</sub> Threshold Overdrive Voltage* (Figure 4).

### 8.3.2 Manual Reset

The manual reset  $\overline{\text{MR}}$  input allows external logic signal from processors, other logic circuits, and/or discrete sensors to initiate a reset. The typical application of a TPS386596 has its  $\overline{\text{RESET}}$  output connected to processor. A logic low at  $\overline{\text{MR}}$  causes  $\overline{\text{RESET}}$  to assert. After  $\overline{\text{MR}}$  returns to a logic high and SENSE<sub>n</sub> are above the respective voltage thresholds,  $\overline{\text{RESET}}$  is released after a fixed 50-ms reset delay time. An internal 100-k $\Omega$  pullup to V<sub>DD</sub> is integrated on the  $\overline{\text{MR}}$  input. There is also an internal 50-ns (typical) deglitch circuit.

### 8.3.3 Reset Output

In a typical application of the TPS386596, the  $\overline{\text{RESET}}$  output is connected to the reset input of a processor (DSP, MCU, CPU, FPGA, ASIC, and so forth) or connected to the enable input of voltage regulators (DC-DC, LDO, and so forth).

The TPS386596 provides an open-drain reset output. Pullup resistors must be used to hold this line high when  $\overline{\text{RESET}}$  is not asserted. By connecting a pullup resistor to the proper voltage rail (up to 6.5 V), the  $\overline{\text{RESET}}$  output can be connected to other devices at the proper interface voltage level. The pullup resistor should be no smaller than 10 k $\Omega$  due to the finite impedance of the output transistor.

The  $\overline{\text{RESET}}$  output is defined for V<sub>DD</sub> > 0.9 V. To ensure that the target processor is properly reset, the V<sub>DD</sub> supply input should be fed by the power rail and be available as early as possible in the application.

Table 1 shows a truth table of how the  $\overline{\text{RESET}}$  output is asserted or released. Figure 1 provides a timing diagram that shows how  $\overline{\text{RESET}}$  is asserted and deasserted in relation to  $\overline{\text{MR}}$  and the SENSE<sub>n</sub> inputs. Once the conditions are met, the transitions from the asserted state to the release state are performed after a fixed 50-ms delay time.

## 8.4 Device Functional Modes

Table 1 shows the device functional modes.

Table 1.  $\overline{\text{RESET}}$  Truth Table

CONDITION		OUTPUT	
$\overline{\text{MR}} = \text{L}$	SENSE <sub>n</sub> < VIT <sub>n</sub>	$\overline{\text{RESET}} = \text{L}$	Reset asserted
$\overline{\text{MR}} = \text{L}$	SENSE <sub>n</sub> > VIT <sub>n</sub>	$\overline{\text{RESET}} = \text{L}$	Reset asserted
$\overline{\text{MR}} = \text{H}$	SENSE1 < VIT1 OR SENSE2 < VIT2 OR SENSE3 < VIT3 OR SENSE4 < VIT4	$\overline{\text{RESET}} = \text{L}$	Reset asserted
$\overline{\text{MR}} = \text{H}$	SENSE1 > VIT1 AND SENSE2 > VIT2 AND SENSE3 > VIT3 AND SENSE4 > VIT4	$\overline{\text{RESET}} = \text{H}$	Reset released

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

#### 9.1.1 Undervoltage Detection

The SENSEn inputs provide terminals at which the system voltages can be monitored. If the voltage at any one of the SENSEn pins drops the respective  $V_{ITn}$ , then the RESET output is asserted. The comparators have a built-in hysteresis to ensure smooth RESET transitions.

It is good analog design practice to use a 1-nF to 10-nF bypass capacitor at the SENSEn input to ground, to reduce sensitivity to transients, layout parasitics, and interference between power rails monitored by this device.

A typical connection of resistor dividers is show in Figure 14. SENSE1 is used to monitor a 3.3-V nominal power-supply voltage with a trip point equal to 2.90 V, and the remaining SENSEn (n = 2, 3, 4) inputs can be used to monitor voltage rails down to 0.4 V. Threshold voltages can be calculated using the following equations.

$$V_{MON(2)} = (1 + RS2H/RS2L) \times 0.4 \text{ (V)} \tag{1}$$

$$V_{MON(3)} = (1 + RS3H/RS3L) \times 0.4 \text{ (V)} \tag{2}$$

$$V_{MON(4)} = (1 + RS4H/RS4L) \times 0.4 \text{ (V)} \tag{3}$$

### 9.2 Typical Application

Figure 14 shows a typical application for the TPS386956.

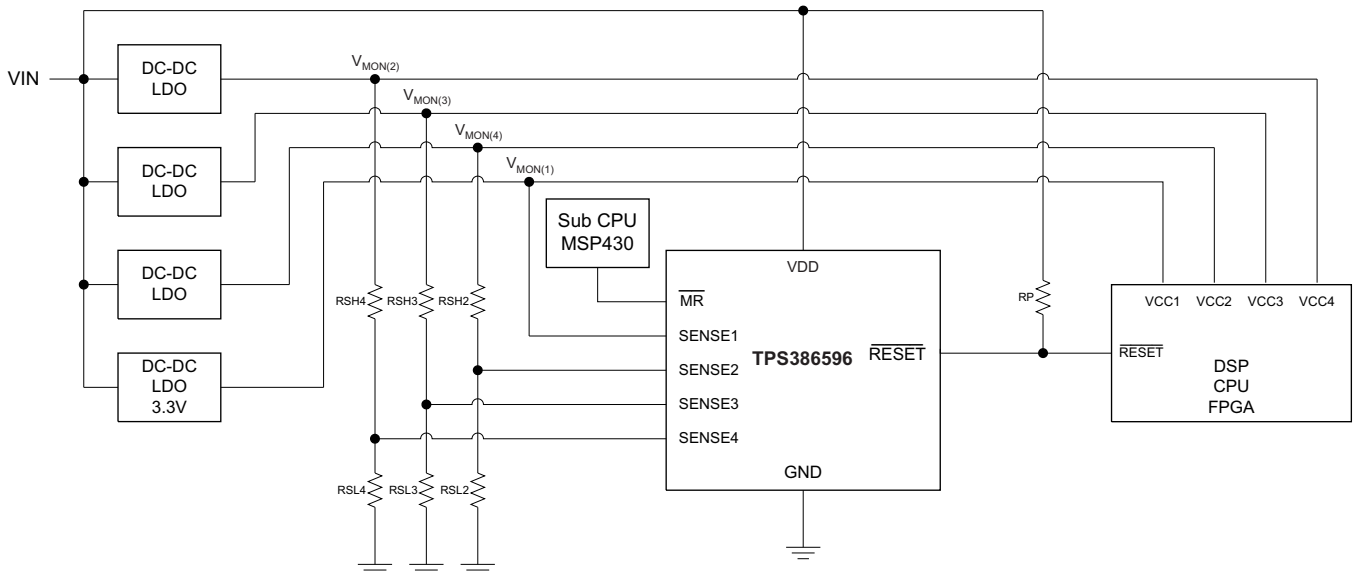


Figure 14. Typical Application Circuit

## Typical Application (continued)

### 9.2.1 Design Requirements

This design is intended to monitor the voltage rails for an FPGA. Table 2 summarizes the design requirements.

Table 2. Design Requirements

PARAMETER	DESIGN REQUIREMENT
V <sub>DD</sub>	5 V
V <sub>MON(1)</sub>	3.3 V –10%
V <sub>MON(2)</sub>	1.5 V –5%
V <sub>MON(3)</sub>	1.2 V –5%
V <sub>MON(4)</sub>	1 V –5%

### 9.2.2 Detailed Design Procedure

Select the pullup resistors to be 100 kΩ to ensure that V<sub>OL</sub> ≤ 0.4 V.

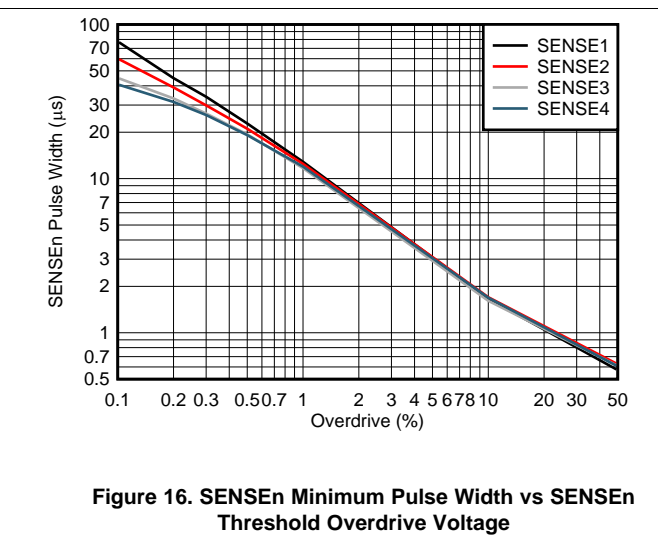
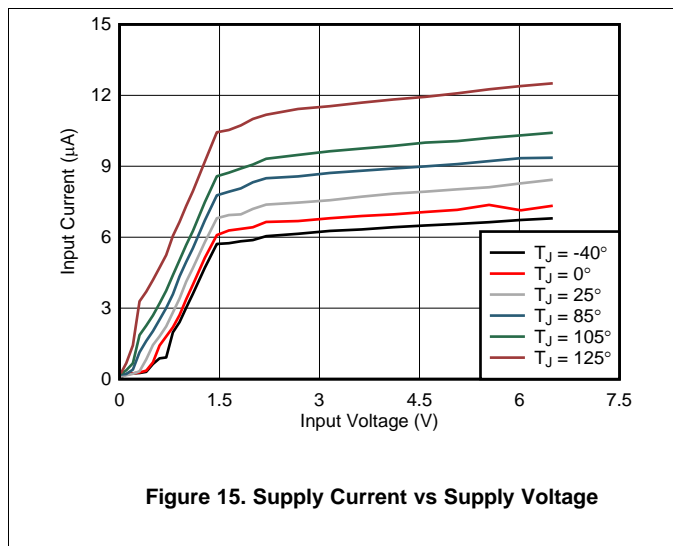
Select R<sub>SnL</sub> = 10 kΩ for all channels to ensure DC accuracy.

Use Equation 1 through Equation 3 to determine the values of R<sub>SnH</sub> and R<sub>S4M</sub>. Using standard 1% resistors, Table 3 shows the results:

Table 3. Design Results

RESISTOR	VALUE (kΩ)
RS1H	32.4
RS2H	25.5
RS3H	18.7
RS4H	14.3
RS4M	1

### 9.2.3 Application Curves



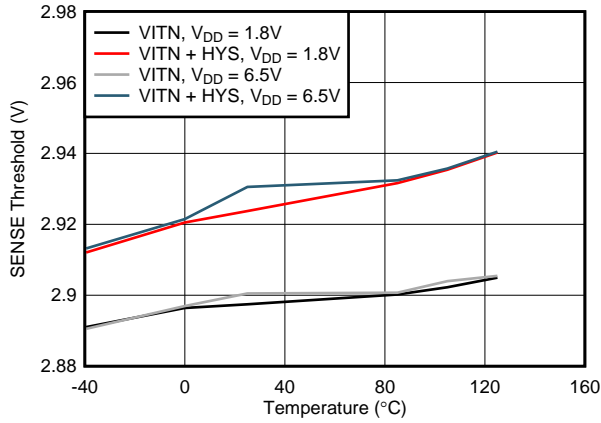


Figure 17. SENSE1 Threshold and Hysteresis vs Temperature

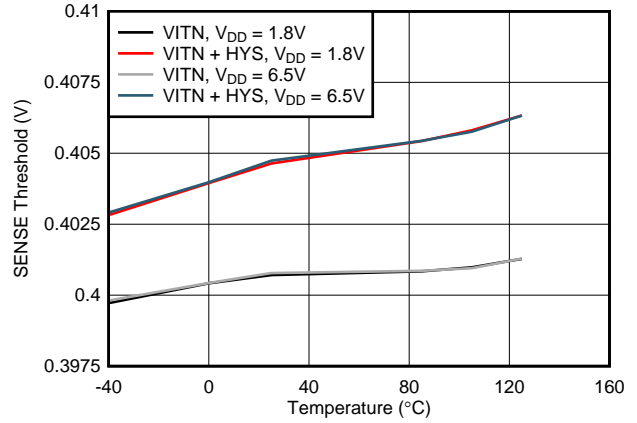


Figure 18. SENSE2 Threshold and Hysteresis vs Temperature

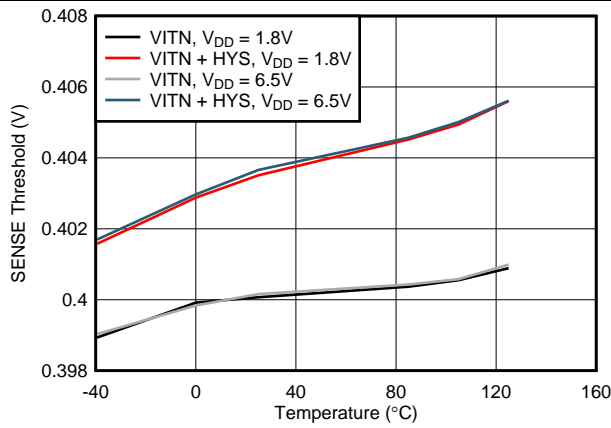


Figure 19. SENSE3 Threshold and Hysteresis vs Temperature

## 10 Power Supply Recommendations

The TPS386596 can operate from a 1.8-V to a 6.5-V input supply. A 0.1- $\mu$ F capacitor placed next to the VDD pin to the GND node is highly recommended. This power supply should not be less than 1.8 V in normal operation to ensure that the internal UVLO circuit does not assert reset.

## 11 Layout

### 11.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit-board (PCB) that is used for the TPS386596.

- Avoid long traces from the SENSE pin to the resistor divider. Instead, run the long traces from the RSnH to  $V_{MON(n)}$ .
- Place the  $V_{DD}$  decoupling capacitor ( $C_{VDD}$ ) close to the device.
- Avoid using long traces for the  $V_{DD}$  supply node. The  $V_{DD}$  capacitor ( $C_{VDD}$ ), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum  $V_{DD}$  voltage.

### 11.2 Layout Example

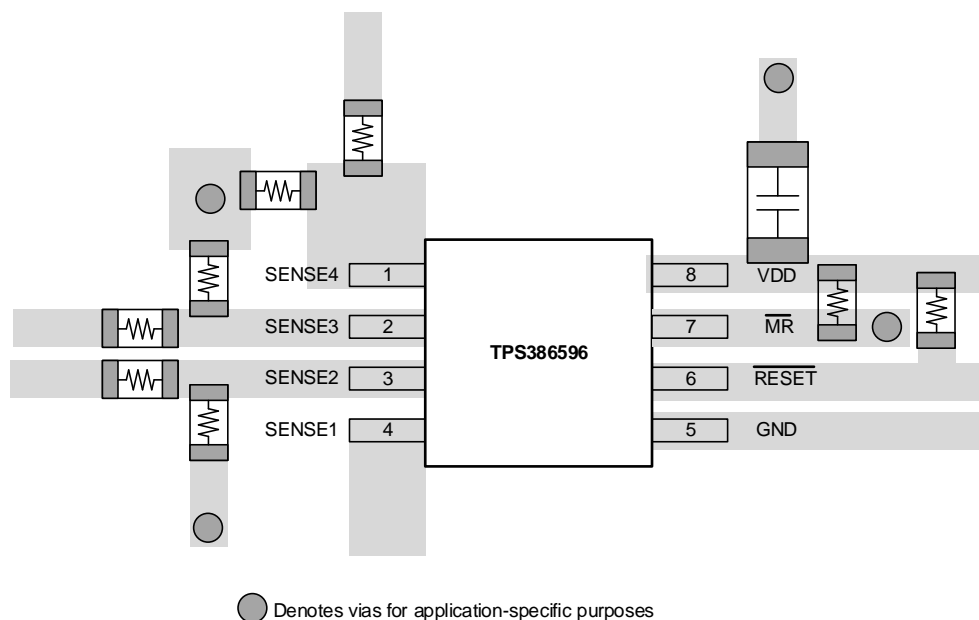


Figure 20. Example Layout (DGK Package)

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

##### 12.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS386596 is available through the device product folders under *Simulation Models*.

#### 12.1.2 Device Nomenclature

**Table 4. Device Nomenclature<sup>(1)</sup>**

PRODUCT	DESCRIPTION
TPS386596xxx yyy z	xxx is device voltage option (for example, L33 = 3.3 V option) yyy is package designator z is package quantity

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS386596L33DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PMXQ	<a href="#">Samples</a>
TPS386596L33DGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PMXQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS386596L33DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS386596L33DGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS386596L33DGKR	VSSOP	DGK	8	2500	367.0	367.0	38.0
TPS386596L33DGKT	VSSOP	DGK	8	250	213.0	191.0	35.0

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



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**NOTES:**

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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