TPS386000/TPS386040 クワッド電源電圧スーパーバイザ 遅延時間可変、ウォッチドッグ・タイマ搭載

1 特長

- 4つの独立した電圧スーパーバイザ
- チャネル1：
  - 可変スレッショルド：最小0.4V
  - マニュアル・リセット($\overline{MR}$)入力
- チャネル2、3：
  - 可変スレッショルド：最小0.4V
- チャネル4：
  - 可変スレッショルド：任意の正負電圧に設定可能
  - ウィンドウ・コンパレータ
- 遅延時間可変：1.4ms～10s
- スレッショルド精度：0.25%（標準値）
- 非常に低い静止電流：11µA（標準値）
- 専用出力を備えたウォッチドッグ・タイマ
- パワーアップ時の出力を適切に制御
- TPS386000：オープン・ドレイン$\overline{RESETn}$および$\overline{WDO}$
- TPS386040：プッシュプル$\overline{RESETn}$および$\overline{WDO}$
- パッケージ：4mm×4mm、20ピンVQFN

2 アプリケーション

- すべてのDSPとマイクロコントローラ
- すべてのFPGAとASIC
- 電気通信および無線インフラストラクチャ
- 産業用機器
- アナログ・シーケンシング

3 概要

TPS3860x0ファミリの電源電圧スーパーバイザ(SVS)は、0.4V以上の電源レール4つと、0.4V未満（負電圧を含む）の電源レール1つを0.25%（標準値）のスレッショルド精度で監視できます。4つのスーパーバイザ回路(SVS-n)は、それぞれSENSEm入力電圧が設定済みスレッショルドを下回ると$\overline{RESETn}$またはRESETn出力信号をアサートします。各SVS-nのスレッショルドは、外付け抵抗により設定できます（ここでn = 1、2、3、4およびm = 1、2、3、4L、4H）。

各SVS-nでは、$\overline{RESETn}$またはRESETnを解除するまでの遅延時間を設定できます。遅延時間は、CTnピンの接続によって、各SVSで個別に1.4ms～10sの範囲に設定可能です。SVS-1のみがアクティブLOWマニュアル・リセット($\overline{MR}$)入力を備えており、$\overline{MR}$への論理LOW入力により$\overline{RESET1}$またはRESET1をアサートします。

SVS-4は2つのコンパレータを使用してスレッショルド・ウィンドウを監視します。この追加のコンパレータを5つ目のSVSとすることで、基準電圧出力VREFにより負電圧を監視できます。

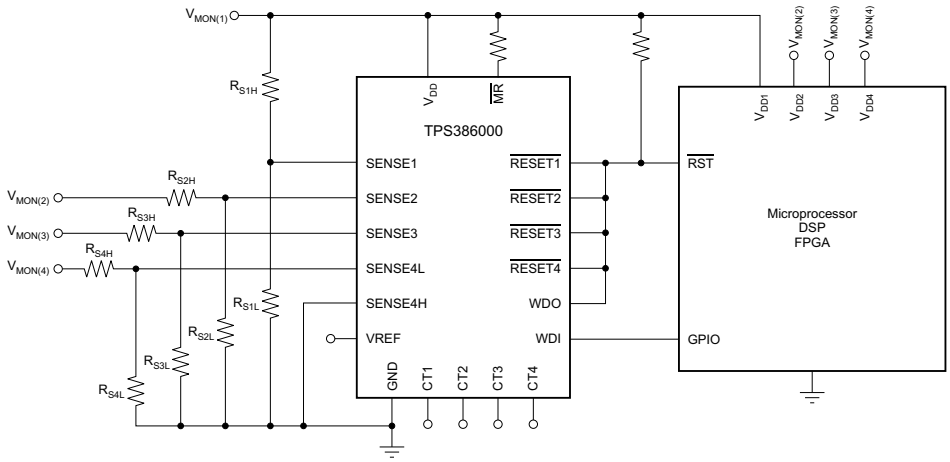
TPS3860x0は静止電流が11µA（標準値）と非常に低く、小型の4mm×4mm VQFN-20パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ（公称）
TPS3860x0	VQFN (20)	4.00mm×4.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

TPS386000代表的アプリケーション回路：
FPGA電源の監視



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (October 2015) から Revision F に変更 **Page**

- Changed the text in the *Power Supply Recommendations* section from: This power supply should be less than 1.8 V in normal operation to: This power supply should not be less than 1.8 V in normal operation ... 30

Revision D (September 2013) から Revision E に変更 **Page**

- 「*ESD定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- チャネル1、2、3、4に関する「特長」項目 変更 ... 1
- Changed all references of V_{CC} (and I_{CC}) to V_{DD} (and I_{DD}) throughout the document ... 5
- Changed the description of SENSE4L pin function ... 5
- Changed the description of SENSE4H pin function ... 5
- Changed the description of $\overline{MR}$ pin function ... 5
- Changed the description of WDI pin function ... 5
- Moved ESD ratings from the *Absolute Maximum Ratings* table to the *ESD Ratings* table ... 7
- Deleted the *Dissipation Ratings* table and added the *Thermal Information* table ... 7
- Moved timing and switching parameters (t_W, t_D, t_{WDT}) from the *Electrical Characteristics* table to the respective *Timing Requirements* and *Switching Characteristics* tables ... 9
- Changed the x-axis title notation from *CT* to *CTn* in the *TPS386040 $\overline{RESETn}$ Time-out Period vs CTn* graph ... 15
- Changed the *Watchdog Timer (WDT) Truth Table*; deleted *RESET* condition column heading ... 25
- Changed title of *SENSE INPUT* section to *Undervoltage Detection* ... 26
- Changed Equation 1, Equation 2, and Equation 3 VCC notations to V_{MON} ... 26
- Changed title of *Window Comparator* section to *Undervoltage and Overvoltage Detection* ... 26
- Changed *VCC4* reference in first paragraph of *Undervoltage and Overvoltage Detection* section to $V_{MON(4)}$ ... 26
- Changed Equation 4 and Equation 5 *VCC4* references to $V_{MON(4)}$ ... 26
- Changed the *SVS-4: Window Comparator* image ... 26

- Added VCC to $V_{MON(4)}$ in the *Window Comparator Operation* image 27
- Changed title of *Sensing Voltage Less Than 0.4 V* to *Sensing a Negative Voltage* 27
- Changed Equation 6 and Equation 7 references to *VCC4* to $V_{MON(4)}$ 27
- Changed the *SVS4: Negative Voltage Sensing* image 27

Revision C (August 2011) から Revision D に変更 **Page**

- TPS386020およびTPS386060をデータシートから削除 1

Revision B (March 2011) から Revision C に変更 **Page**

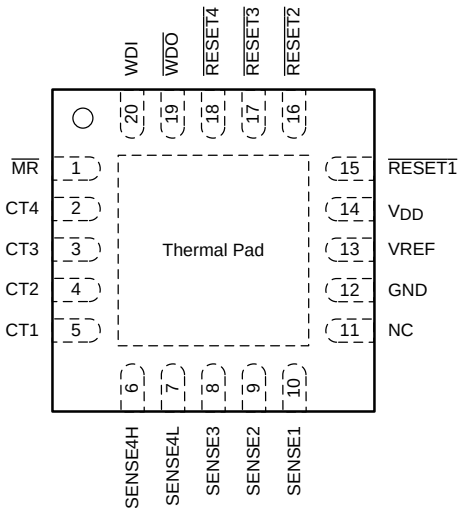
- Changed Figure 31 22

Revision A (January 2010) から Revision B に変更 **Page**

- データシート・タイトルを変更 1
- 「特長」項目を変更 1
- 「アプリケーション」項目を変更 1
- 「概要」テキストの第2段落第1文を変更 1
- 「概要」テキストで最終段落の「低い静止電流」の値を12µAから11µAに変更 1
- 先頭ページの代表的アプリケーション回路図を変更 2
- Added sentence to pin 6 description in Pin Assignments table 5
- Changed last sentence of pin 13 description in Pin Assignments table 5
- Added text to first sentence of first paragraph of *General Description* section. 23
- Changed link in *Window Comparator* section to new Figure 32 26
- Deleted typo in Equation 4 and moved Equation 4 to *Window Comparator* section 26
- Deleted typo in Equation 5 and moved Equation 5 to *Window Comparator* section 26
- Added Figure 32 26
- Changed link in *Sensing Voltage Less Than 0.4V* section to new Figure 34 27
- Added Figure 34 27
- Changed caption for Figure 35 29

5 Pin Configuration and Functions

RGP Package
20-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION	
NAME	NO.			
V_{DD}	14	I	Supply voltage. TI recommends connecting a 0.1-µF ceramic capacitor close to this pin.	
GND	12	—	Ground	
SENSE1	10	I	Monitor voltage input to SVS-1	When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{\text{RESET1}}$ is asserted.
SENSE2	9	I	Monitor voltage input to SVS-2	When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{\text{RESET2}}$ is asserted.
SENSE3	8	I	Monitor voltage input to SVS-3	When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{\text{RESET3}}$ is asserted.
SENSE4L	7	I	Falling monitor voltage input to SVS-4. When the voltage at this terminal drops below the threshold voltage (V_{ITN}), $\overline{\text{RESET4}}$ is asserted.	
SENSE4H	6	I	Rising monitor voltage input to SVS-4. When the voltage at this terminal exceeds the threshold voltage (V_{ITP}), $\overline{\text{RESET4}}$ is asserted. This pin can also be used to monitor the negative voltage rail in combination with VREF pin. Connect to GND if not being used.	
CT1	5	—	Reset delay programming pin for SVS-1	Connecting this pin to V_{DD} through a 40-kΩ to 200-kΩ resistor, or leaving it open, selects a fixed delay time (see the *Electrical Characteristics*). Connecting a capacitor > 220 pF between this pin and GND selects the programmable delay time (see the *Reset Delay Time* section).
CT2	4	—	Reset delay programming pin for SVS-2	
CT3	3	—	Reset delay programming pin for SVS-3	
CT4	2	—	Reset delay programming pin for SVS-4	
VREF	13	O	Reference voltage output. By connecting a resistor network between this pin and the negative power rail, SENSE4H can monitor the negative power rail. This pin is intended to only source current into resistor(s). Do not connect resistor(s) to a voltage higher than 1.2 V. Do not connect only a capacitor.	
$\overline{\text{MR}}$	1	I	Manual reset input for SVS-1. Logic low level of this pin asserts $\overline{\text{RESET1}}$.	
WDI	20	I	Watchdog timer (WDT) trigger input. Inputting either a positive or negative logic edge every 610 ms (typical) prevents WDT time out at the $\overline{\text{WDO}}$ or WDO pin. Timer starts from releasing event of $\overline{\text{RESET1}}$.	
NC	11	—	Not internal connection. TI recommends connecting this pin to the GND pin (pin 12), which is next to this pin.	
Thermal Pad	PAD	—	This pad is the IC substrate. This pad must be connected only to GND or to the floating thermal pattern on the printed-circuit board (PCB).	

Pin Functions (continued)

PIN		I/O	DESCRIPTION	
NAME	NO.			
TPS386000				
$\overline{\text{RESET1}}$	15	O	Active low reset output of SVS-1	$\overline{\text{RESETn}}$ is an open-drain output pin. When $\overline{\text{RESETn}}$ is asserted, this pin remains in a low-impedance state. When $\overline{\text{RESETn}}$ is released, this pin goes to a high-impedance state after the delay time programmed by CTn. A pullup resistor to V_{DD} or another voltage source is required.
$\overline{\text{RESET2}}$	16	O	Active low reset output of SVS-2	
$\overline{\text{RESET3}}$	17	O	Active low reset output of SVS-3	
$\overline{\text{RESET4}}$	18	O	Active low reset output of SVS-4	
$\overline{\text{WDO}}$	19	O	Watchdog timer output. This is an open-drain output pin. When WDT times out, this pin goes to a low-impedance state to GND. If there is no WDT time-out, this pin stays in a high-impedance state.	
TPS386040				
$\overline{\text{RESET1}}$	15	O	Active low reset output of SVS-1	$\overline{\text{RESETn}}$ is a push-pull logic buffer output pin. When $\overline{\text{RESETn}}$ is asserted, this pin remains logic low. When $\overline{\text{RESETn}}$ is released, this pin goes to logic high after the delay time programmed by CTn.
$\overline{\text{RESET2}}$	16	O	Active low reset output of SVS-2	
$\overline{\text{RESET3}}$	17	O	Active low reset output of SVS-3	
$\overline{\text{RESET4}}$	18	O	Active low reset output of SVS-4	
$\overline{\text{WDO}}$	19	O	Watchdog timer output. This is a push-pull output pin. When WDT times out, this pin goes to logic low. If there is no WDT time-out, this pin stays in logic high.	

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range, unless otherwise noted.(1)

		MIN	MAX	UNIT
Voltage	Input, V_{DD}	–0.3	7	V
	CT pin, V_{CT1}, V_{CT2}, V_{CT3}, V_{CT4}	–0.3	V_{DD} + 0.3	
	V_{RESET1}, V_{RESET2}, V_{RESET3}, V_{RESET4}, V_{MR}, V_{SENSE1}, V_{SENSE2}, V_{SENSE3}, $V_{SENSE4L}$, $V_{SENSE4H}$, V_{WDI}, V_{WDO}	–0.3	7	
Current	$\overline{\text{RESETn}}$, RESETn, $\overline{\text{WDO}}$, WDO, VREF pin		5	mA
Power dissipation	Continuous total	See *Thermal Information* table		
Temperature	Operating virtual junction, T_J(2)	–40	150	°C
	Operating ambient, T_A	–40	125	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over operating junction temperature range (unless otherwise noted).

	MIN	NOM	MAX	UNIT
V_{DD}	1.8		6.5	V
V_{SENSE}(1)	0		V_{DD}	V
$WDI_{(HI)}$	$0.7V_{DD}$		V_{DD}	V
$WDI_{(LO)}$	0		$0.3V_{DD}$	V
V_{MR}	0		V_{DD}	V
CTn	0.22		1000	nF
$R_{PULL-UP}$	6.5	100	10000	kΩ
T_J	–40	25	125	°C

(1) All sense inputs.

6.4 Thermal Information

THERMAL METRIC(1)		TPS3860x0 RGP (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to 125°C, 1.8 V < V_{DD} < 6.5 V, R_{RESETn} (*n* = 1, 2, 3, 4) = 100 kΩ to V_{DD} (TPS386000 only), C_{RESETn} (*n* = 1, 2, 3, 4L, 4H) = 50 pF to GND, R_{WDO} = 100 kΩ to V_{DD}, C_{WDO} = 50 pF to GND, V_{MR} = 100 kΩ to V_{DD}, WDI = GND, and CTn (*n* = 1, 2, 3, 4) = open, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Input supply range			1.8		6.5	V
I_{DD}	Supply current (current into V_{DD} pin)		V_{DD} = 3.3 V, $\overline{\text{RESETn}}$ or RESETn not asserted, WDI toggling(1), no output load, and VREF open		11	19	µA
			V_{DD} = 6.5 V, $\overline{\text{RESETn}}$ or RESETn not asserted, WDI toggling(1), no output load, and VREF open		13	22	
	Power-up reset voltage(2)(3)		V_{OL} (max) = 0.2 V, I_{RESETn} = 15 µA			0.9	V
V_{ITN}	Negative-going input threshold voltage		SENSE1, SENSE2, SENSE3, SENSE4L	396	400	404	mV
V_{ITP}	Positive-going input threshold voltage		SENSE4H	396	400	404	mV
V_{HYSN}	Hysteresis (positive-going) on V_{ITN}		SENSE1, SENSE2, SENSE3, SENSE4L		3.5	10	mV
V_{HYSP}	Hysteresis (negative-going) on V_{ITP}		SENSE4H		3.5	10	mV
I_{SENSE}	Input current at SENSEm pin		V_{SENSEm} = 0.42 V	–25	±1	+25	nA
I_{CT}	CTn pin charging current	CT1	C_{CT1} > 220 pF, V_{CT1} = 0.5 V(4)	245	300	355	nA
		CT2, CT3, CT4	C_{CTn} > 220 pF, V_{CTn} = 0.5 V(4)	235	300	365	
$V_{TH(CTn)}$	CTn pin threshold		C_{CTn} > 220 pF	1.18	1.238	1.299	V
V_{IL}	$\overline{\text{MR}}$ and WDI logic low input			0		0.3V_{DD}	V
V_{IH}	$\overline{\text{MR}}$ and WDI logic high input			0.7V_{DD}			V
V_{OL}	Low-level $\overline{\text{RESETn}}$ or RESETn output voltage		I_{OL} = 1 mA			0.4	V
			SENSEn = 0 V, 1.3 V < V_{DD} < 1.8 V, I_{OL} = 0.4 mA(2)			0.3	V
	Low-level WDO output voltage		I_{OL} = 1 mA			0.4	
V_{OH}	High-level $\overline{\text{RESETn}}$ or RESETn output voltage	TPS386040 only	I_{OL} = –1 mA	V_{DD} – 0.4			V
	High-level WDO output voltage	TPS386040 only	I_{OL} = –1 mA	V_{DD} – 0.4			V
			SENSEn = 0 V, 1.3 V < V_{DD} < 1.8 V, I_{OL} = –0.4 mA(2)	V_{DD} – 0.3			
I_{LKG}	$\overline{\text{RESETn}}$, RESETn, $\overline{\text{WDO}}$, and WDO leakage current	TPS386000 only	V_{RESETn} = 6.5 V, $\overline{\text{RESETn}}$, RESETn, $\overline{\text{WDO}}$, and WDO are logic high	–300		300	nA
V_{REF}	Reference voltage output		1 µA < I_{VREF} < 0.2 mA (source only, no sink)	1.18	1.2	1.22	V
C_{IN}	Input pin capacitance		CTn: 0 V to V_{DD}, other pins: 0 V to 6.5 V		5		pF

(1) Toggling WDI for a period less than t_{WDT} negatively affects I_{DD}.
(2) These specifications are beyond the recommended V_{DD} range, and only define $\overline{\text{RESETn}}$ or RESETn output performance during V_{DD} ramp up.
(3) The lowest supply voltage (V_{DD}) at which $\overline{\text{RESETn}}$ or RESETn becomes active; $t_{RISE(VDD)}$ ≥ 15 µs/V.
(4) CTn (where *n* = 1, 2, 3, or 4) are constant current charging sources working from a range of 0 V to $V_{TH(CTn)}$, and the device is tested at V_{CTn} = 0.5 V. For I_{CT} performance between 0 V and $V_{TH(CTn)}$, see Figure 28.

6.6 Timing Requirements

Over the operating temperature range of T_J = –40°C to 125°C, 1.8 V < V_{DD} < 6.5 V, R_{RESETn} (*n* = 1, 2, 3, 4) = 100 kΩ to V_{DD} (TPS386000 only), C_{RESETn} (*n* = 1, 2, 3, 4L, 4H) = 50 pF to GND, R_{WDO} = 100 kΩ to V_{DD}, C_{WDO} = 50 pF to GND, V_{MR} = 100 kΩ to V_{DD}, WDI = GND, and CTn (*n* = 1, 2, 3, 4) = open, unless otherwise noted. Nominal values are at T_J = 25°C.

			MIN	TYP	MAX	UNIT
t_W	Input pulse width to SENSEm and $\overline{MR}$ pins	SENSEm: 1.05 V_{ITN} → 0.95 V_{ITN} or 0.95 V_{ITP} → 1.05 V_{ITP}		4		µs
		$\overline{MR}$: 0.7 V_{DD} → 0.3 V_{DD}		1		ns

6.7 Switching Characteristics

Over the operating temperature range of T_J = –40°C to 125°C, 1.8 V < V_{DD} < 6.5 V, R_{RESETn} (*n* = 1, 2, 3, 4) = 100 kΩ to V_{DD} (TPS386000 only), C_{RESETn} (*n* = 1, 2, 3, 4L, 4H) = 50 pF to GND, R_{WDO} = 100 kΩ to V_{DD}, C_{WDO} = 50 pF to GND, V_{MR} = 100 kΩ to V_{DD}, WDI = GND, and CTn (*n* = 1, 2, 3, 4) = open, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_D	$\overline{RESETn}$ or RESETn delay time	CTn = Open	14	20	24	ms
		CTn = V_{DD}	225	300	375	
t_{WDT}	Watchdog timer time-out period(1)		450	600	750	ms

(1) Start from $\overline{RESET1}$ or RESET1 release or last WDI transition.

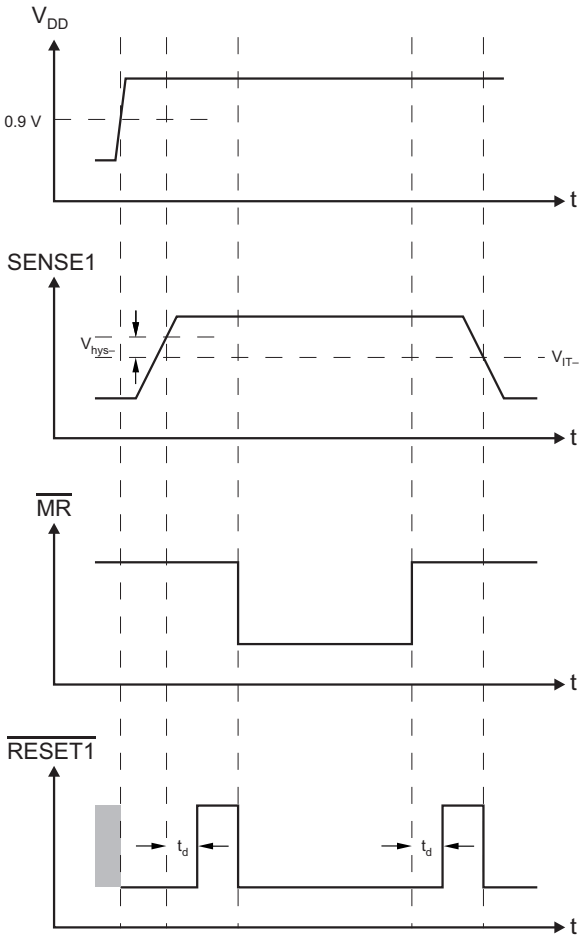


Figure 1. SVS-1 Timing Diagram

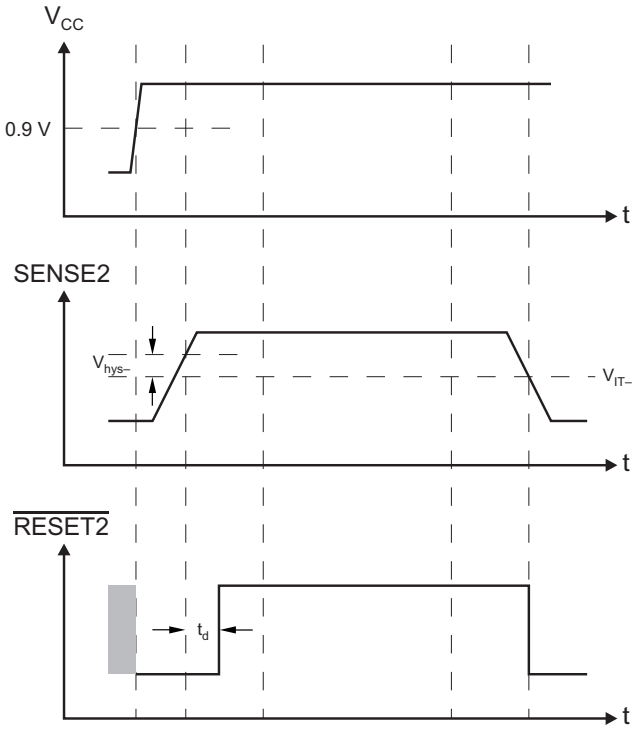


Figure 2. SVS-2 Timing Diagram

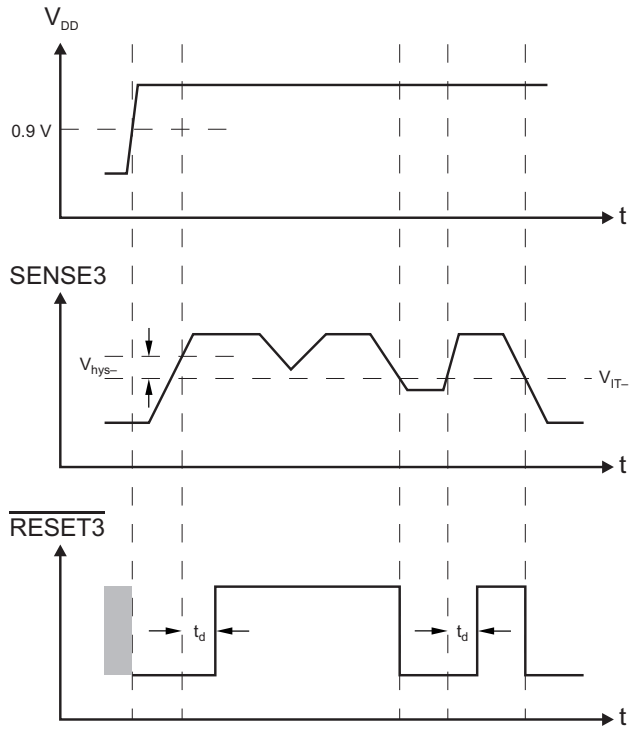


Figure 3. SVS-3 Timing Diagram

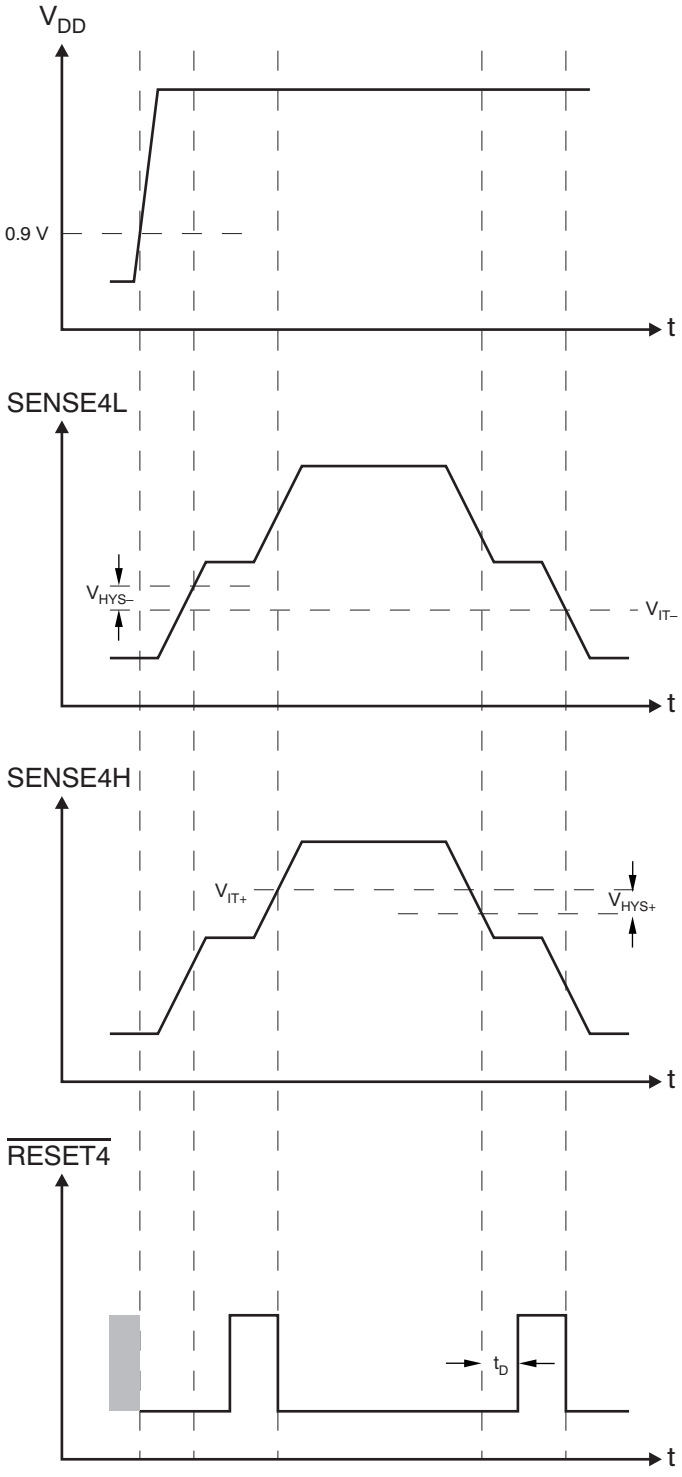


Figure 4. SVS-4 Timing Diagram

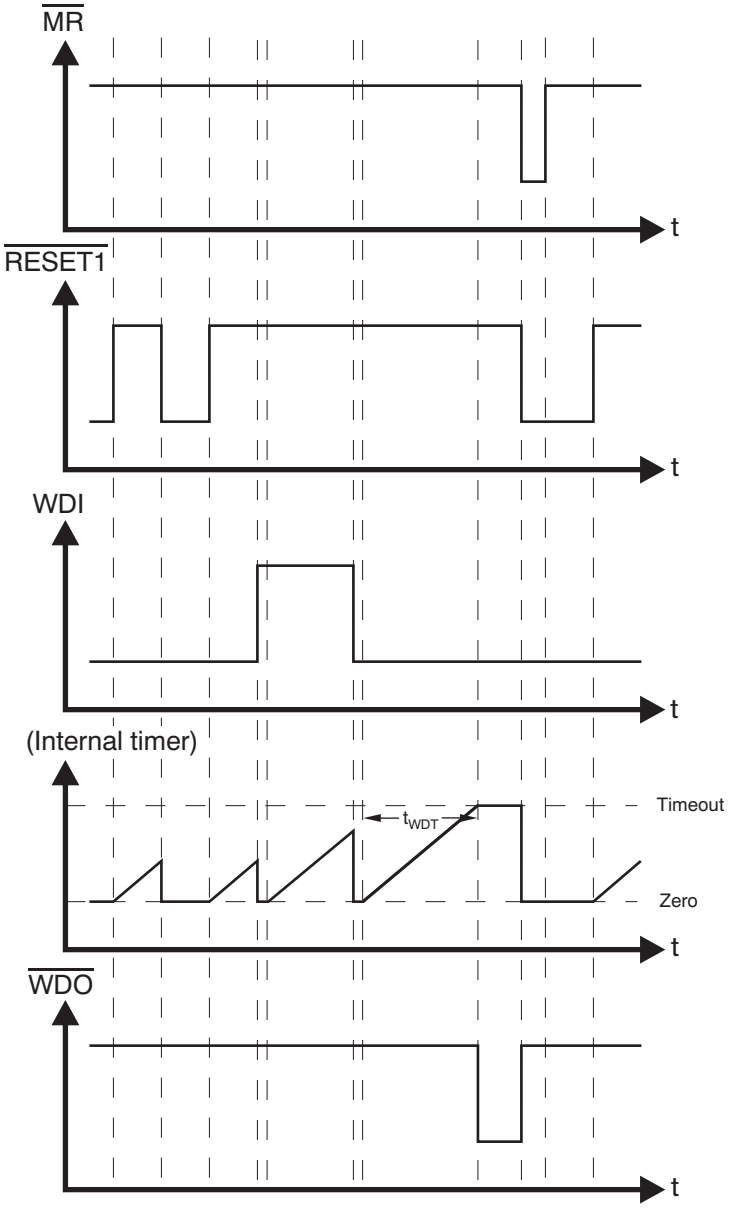


Figure 5. WDT Timing Diagram

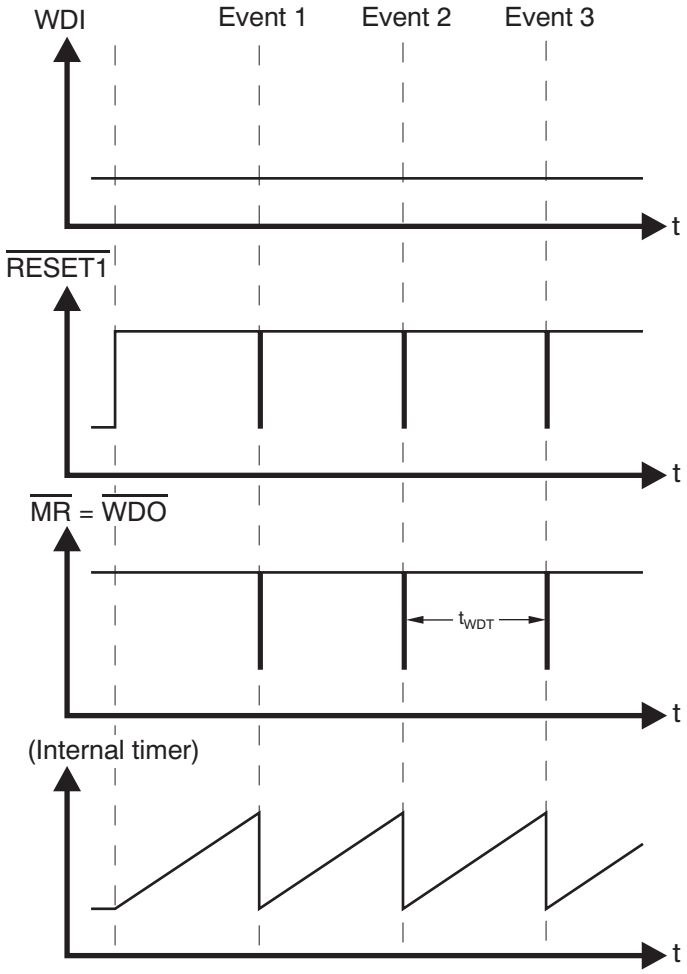


Figure 6. Legacy WDT Configuration Timing Diagram

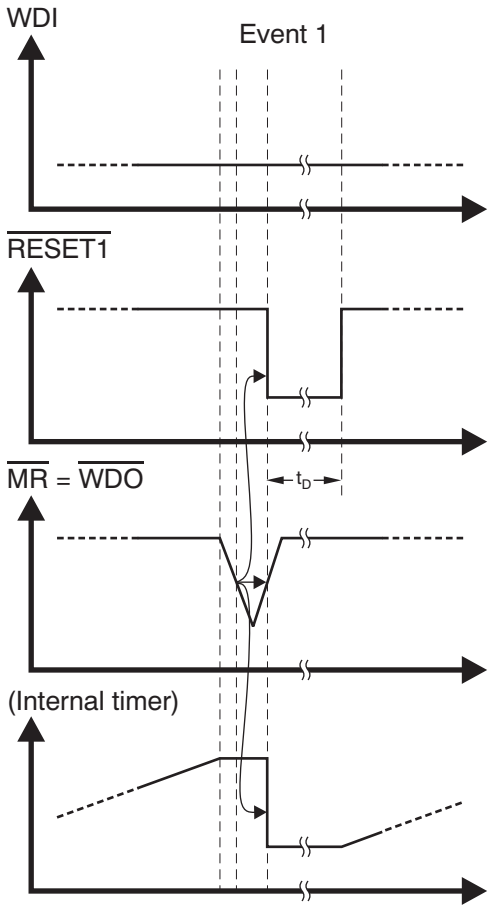


Figure 7. Enlarged View of Event 1 from Figure 6

6.8 Typical Characteristics

At T_A = 25°C, and V_{DD} = 3.3 V, with both options (TPS386000 and TPS386040) having the same characteristics, unless otherwise noted.

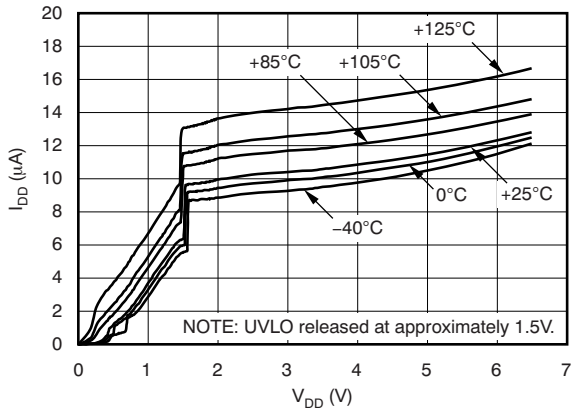


Figure 8. TPS386040 Supply Current vs Supply Voltage

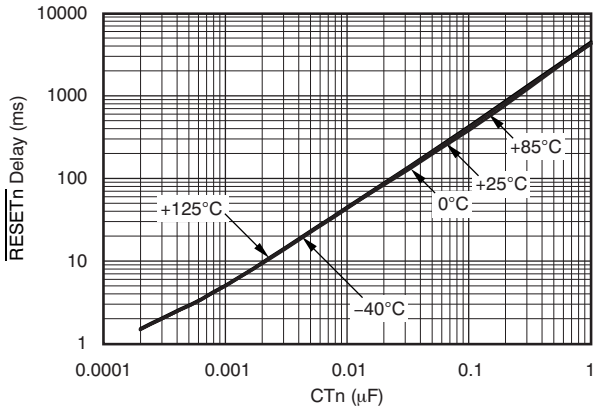


Figure 9. TPS386040 $\overline{\text{RESETn}}$ Time-out Period vs CTn

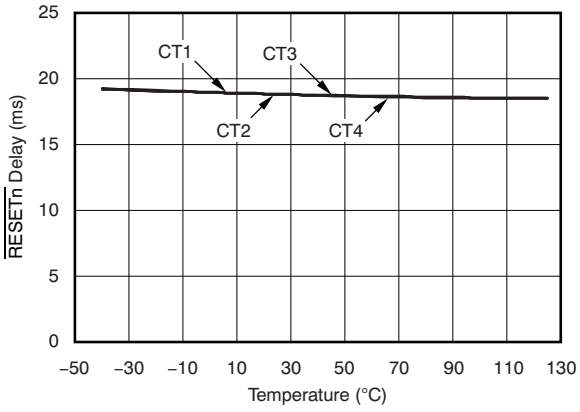


Figure 10. TPS386040 (CTn = Open) $\overline{\text{RESETn}}$ Time-out Period vs Temperature

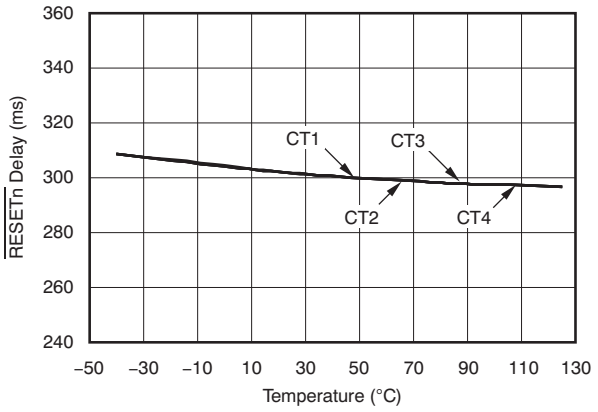


Figure 11. TPS386040 (CTn = V_{DD}) $\overline{\text{RESETn}}$ Time-out Period vs Temperature

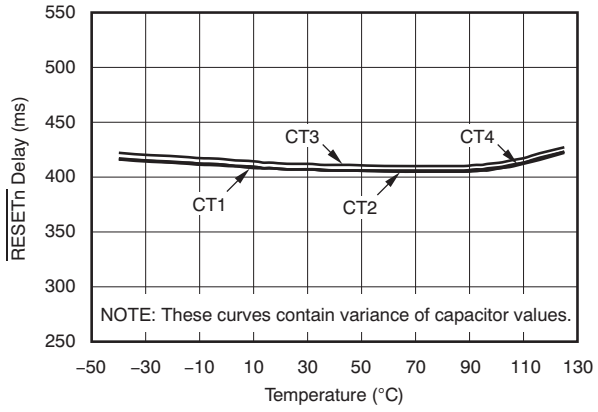


Figure 12. TPS386040 (CTn = 0.1 µF) $\overline{\text{RESETn}}$ Time-out Period vs Temperature

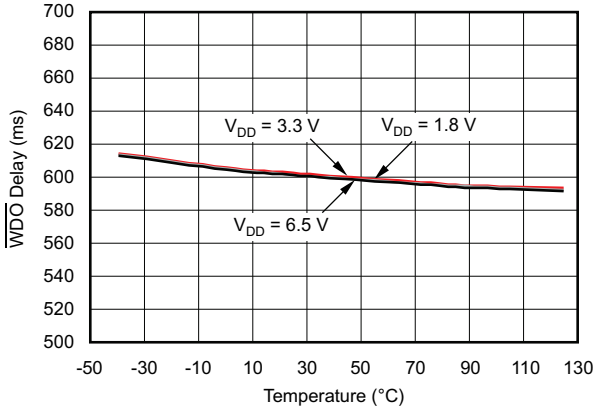
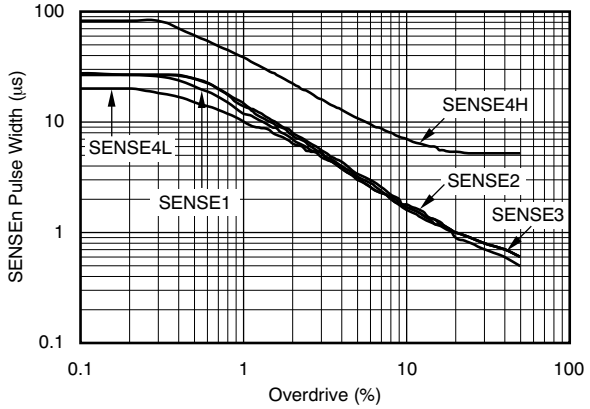


Figure 13. TPS386040 $\overline{\text{WDO}}$ Time-out Period vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, and V_{DD} = 3.3 V, with both options (TPS386000 and TPS386040) having the same characteristics, unless otherwise noted.



See *Figure 29* for measurement technique

Figure 14. TPS386040 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage

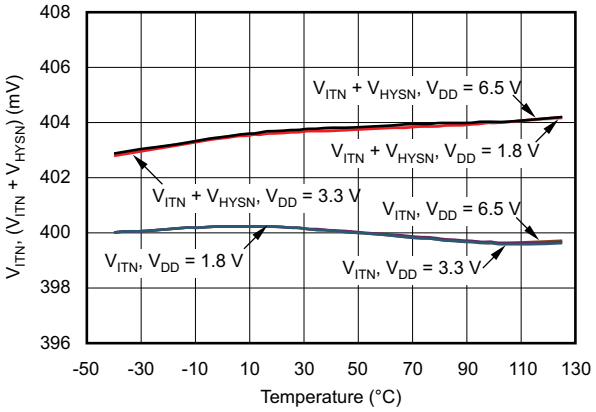


Figure 15. TPS386040 SENSE1 Threshold Voltage vs Temperature

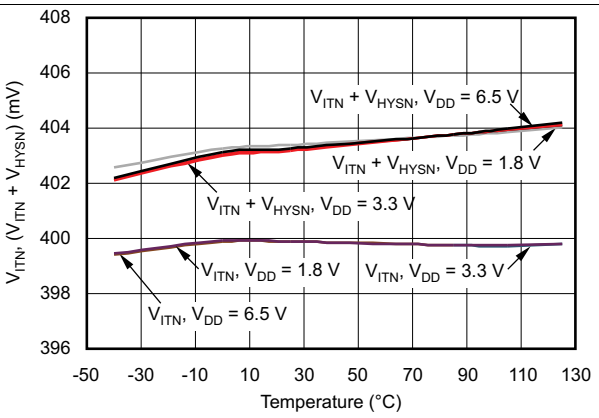


Figure 16. TPS386040 SENSE2 Threshold Voltage vs Temperature

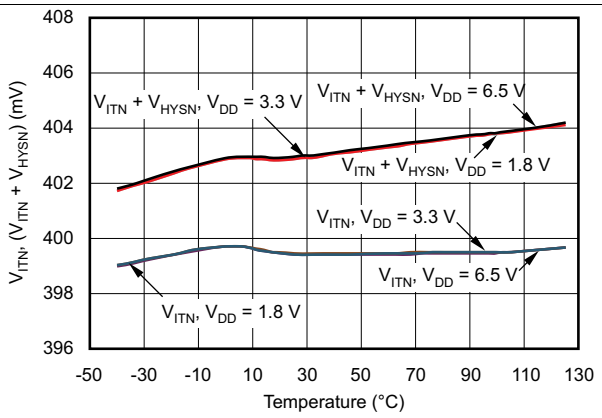


Figure 17. TPS386040 SENSE3 Threshold Voltage vs Temperature

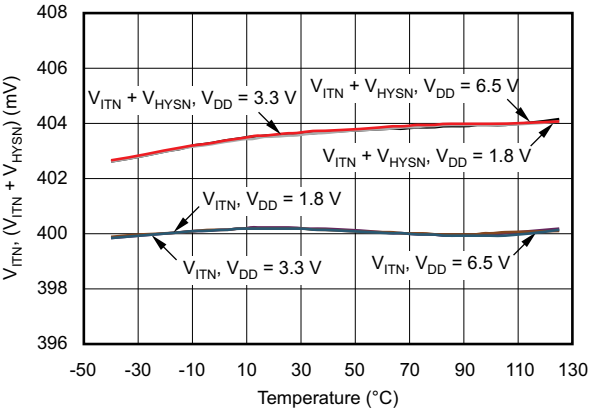


Figure 18. TPS386040 SENSE4L Threshold Voltage vs Temperature

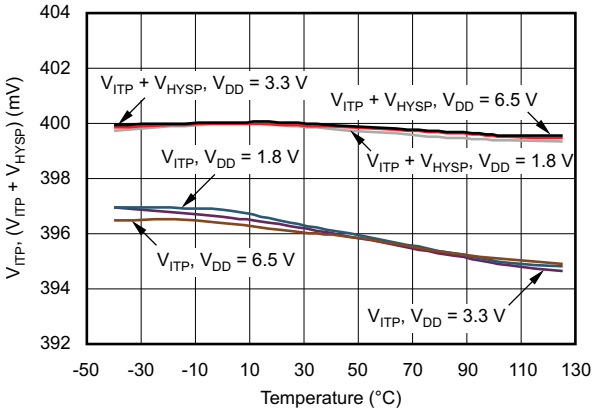


Figure 19. TPS386040 SENSE4H Threshold Voltage vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, and V_{DD} = 3.3 V, with both options (TPS386000 and TPS386040) having the same characteristics, unless otherwise noted.

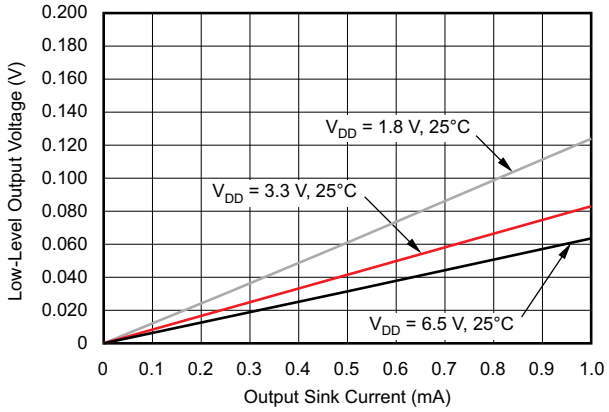


Figure 20. Output Voltage Low vs Output Current

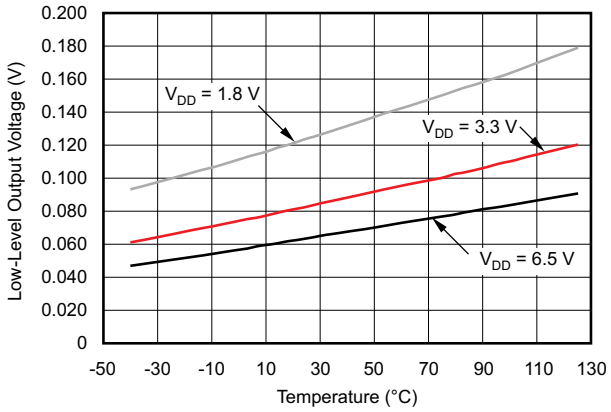


Figure 21. Output Voltage Low at 1 mA vs Temperature

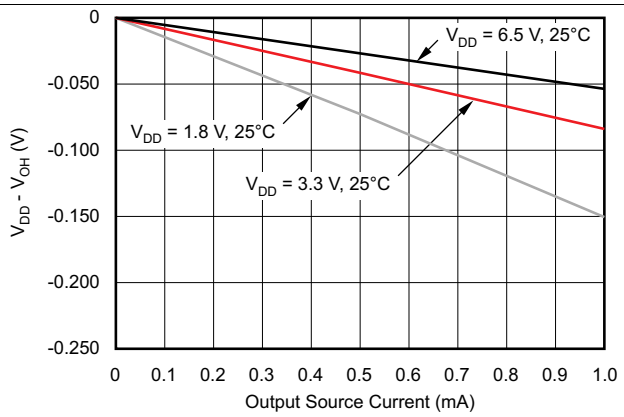


Figure 22. Output Voltage High vs Output Current

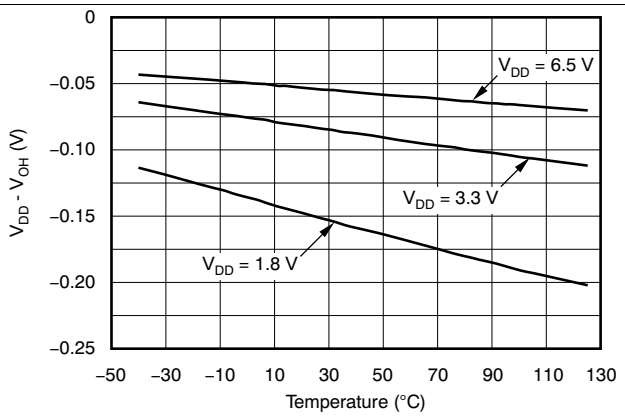


Figure 23. Output Voltage High at 1 mA vs Temperature

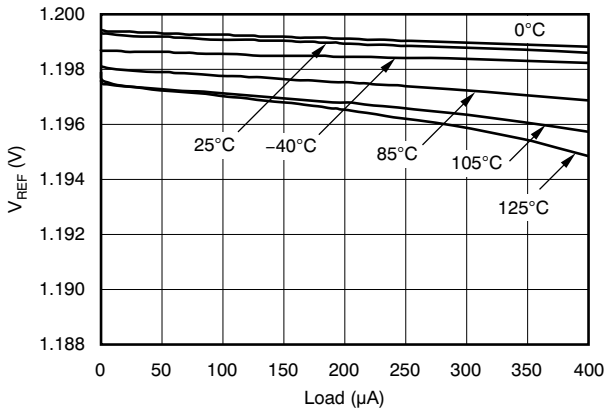


Figure 24. TPS386040 V_{REF} Output Load Regulation (V_{DD} = 1.8 V)

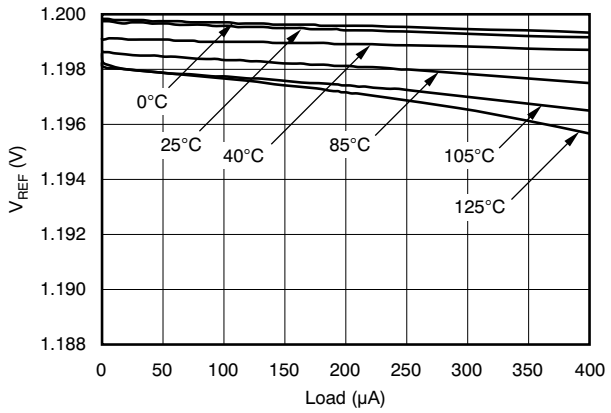


Figure 25. TPS386040 V_{REF} Output Load Regulation (V_{DD} = 3.3 V)

Typical Characteristics (continued)

At T_A = 25°C, and V_{DD} = 3.3 V, with both options (TPS386000 and TPS386040) having the same characteristics, unless otherwise noted.

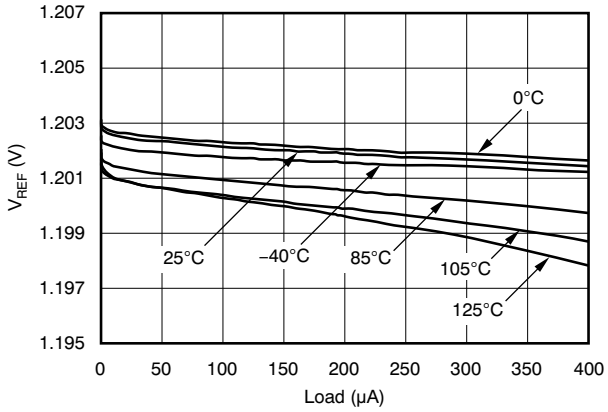


Figure 26. TPS386040 V_{REF} Output Load Regulation (V_{DD} = 6.5 V)

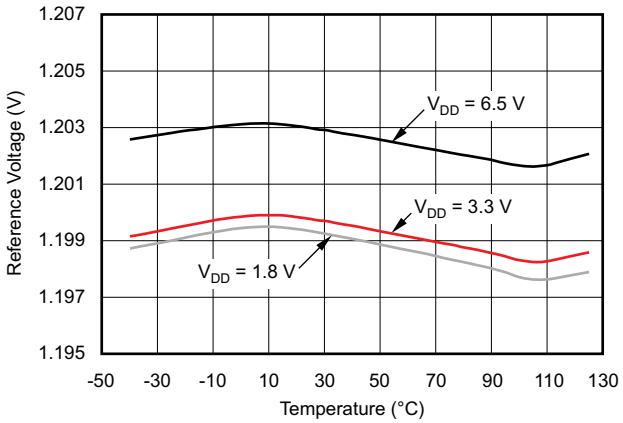


Figure 27. TPS386040 V_{REF} at 0 µA vs Temperature

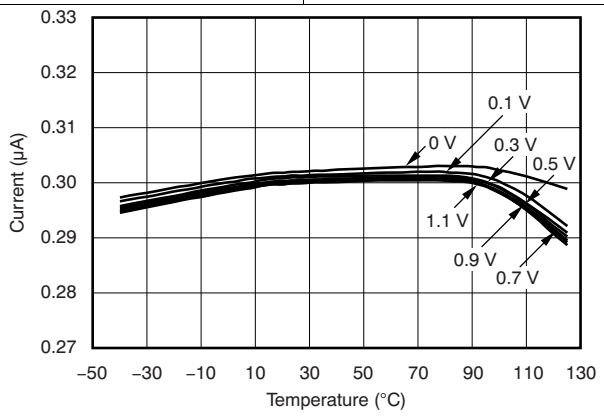
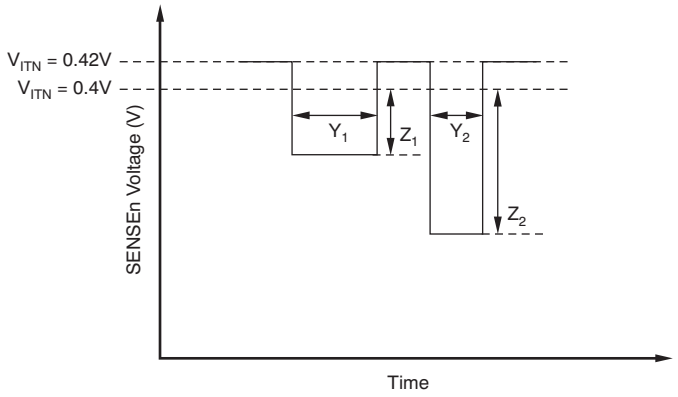


Figure 28. TPS386040 CT1 to CT4 Pin Charging Current vs Temperature Over CT Pin Voltage

7 Parameter Measurement Information



$$X_1 = \frac{Z_1}{0.4} \times 100\ (\%)$$

$$X_2 = \frac{Z_2}{0.4} \times 100\ (\%)$$

X_1 and X_2 are overdrive (%) values calculated from actual SENSEn voltage amplitudes measured as Z_1 and Z_2.
Y_N is the minimum pulse width that gives RESETn or $\overline{\text{RESETn}}$ transition.
Greater Z_N produces shorter Y_N.

For SENSE4H, this graph should be inverted 180 degrees on the voltage axis.

Figure 29. Overdrive Measurement Method

8 Detailed Description

8.1 Overview

The TPS3860x0 multi-channel supervisory family of devices combines four complete SVS function sets into one IC, along with a watchdog timer, a window comparator, and negative voltage sensing. The design of each SVS channel is based on the single-channel supervisory device series, TPS3808. The TPS3860x0 is designed to assert RESETn or RESETn signals, as shown in Table 1, Table 2, Table 3, and Table 4. The RESETn or RESETn outputs remain asserted during a user-configurable delay time after the event of reset release (see the *Reset Delay Time* section).

The TPS3860x0 has a very low quiescent current of 11 μA (typical) and is available in a small, 4-mm × 4-mm, 20-Pin VQFN package.

8.2 Functional Block Diagrams

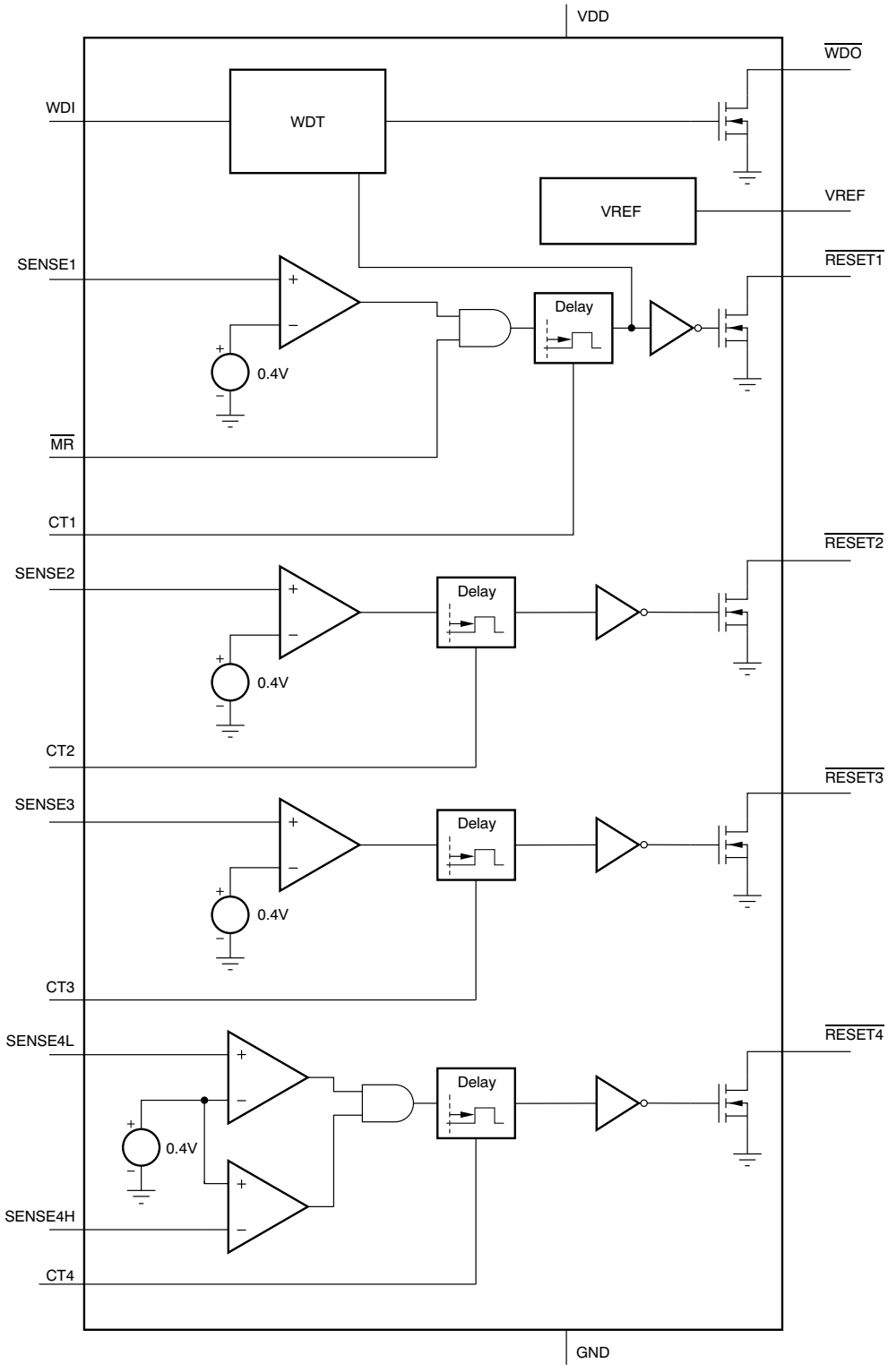


Figure 30. TPS386000 Block Diagram

Functional Block Diagrams (continued)

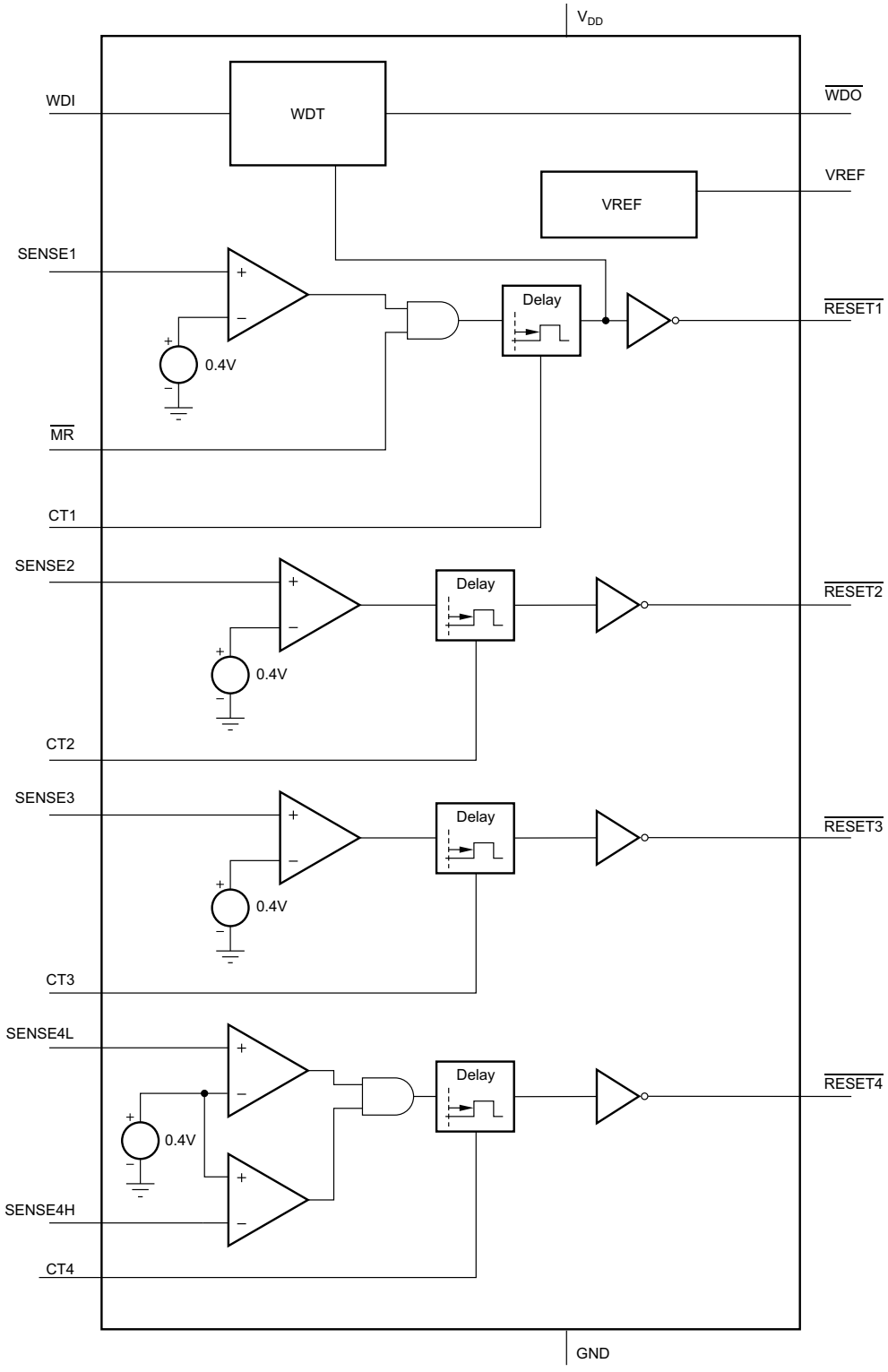


Figure 31. TPS386040 Block Diagram

8.3 Feature Description

8.3.1 Voltage Monitoring

Each SENSEm (m = 1, 2, 3, 4L) pin can be set to monitor any voltage threshold above 0.4 V using an external resistor divider. The SENSE4H pin can be used for any overvoltage detection greater than 0.4 V, or for negative voltage detection using an external resistor divider (see the *Sensing a Negative Voltage* section). A broad range of voltage threshold and reset delay time adjustments can be supported, allowing these devices to be used in a wide array of applications.

The TPS3860x0 is relatively immune to short negative transients on the SENSEn pin. Sensitivity to transients depends on threshold overdrive, as shown in (Figure 14).

8.3.2 Manual Reset

The manual reset ($\overline{MR}$) input allows external logic signal from other processors, logic circuits, and/or discrete sensors to initiate a device reset. Because $\overline{MR}$ is connected to SVS-1, the $\overline{RESET1}$ or RESET1 pin is intended to be connected to processor(s) as a primary reset source. A logic low at $\overline{MR}$ causes $\overline{RESET1}$ or RESET1 to assert. After $\overline{MR}$ returns to a logic high and SENSE1 is above its reset threshold, $\overline{RESET1}$ or RESET1 is released after the user-configured reset delay time. Unlike the TPS3808 series, the TPS3860x0 does not integrate an internal pullup resistor between $\overline{MR}$ and V_{DD}.

To control the $\overline{MR}$ function from more than one logic signal, the logic signals can be combined by wired-OR into the $\overline{MR}$ pin using multiple NMOS transistors and one pullup resistor.

8.3.3 Watchdog Timer

The TPS3860x0 provides a watchdog timer with a dedicated watchdog error output, $\overline{WDO}$ or WDO. The $\overline{WDO}$ or WDO output enables application board designers to easily detect and resolve the hang-up status of a processor. As with $\overline{MR}$, the watchdog timer function of the device is also tied to SVS-1. Figure 5 shows the timing diagram of the WDT function. Once $\overline{RESET1}$ or RESET1 is released, the internal watchdog timer starts its countdown. Inputting a logic level transition at WDI resets the internal timer count and the timer restarts the countdown. If the TPS3860x0 fails to receive any WDI rising or falling edge within the WDT period, the WDT times out and asserts $\overline{WDO}$ or WDO. After $\overline{WDO}$ or WDO is asserted, the device holds the status with the internal latch circuit. To clear this time-out status, a reset assertion of $\overline{RESET1}$ or RESET is required. That is, a negative pulse to $\overline{MR}$, a SENSE1 voltage less than V_{ITN}, or a V_{DD} power down is required.

To reset the processor by WDT time-out, $\overline{WDO}$ can be combined with $\overline{RESET1}$ by using the wired-OR with the TPS386000 option.

For legacy applications where the watchdog timer time-out causes $\overline{RESET1}$ to assert, connect $\overline{WDO}$ to $\overline{MR}$; see Figure 35 for the connections and see Figure 6 and Figure 7 for the timing diagrams.

Feature Description (continued)

8.3.4 Reset Output

In a typical TPS3860x0 application, $\overline{\text{RESETn}}$ or RESETn outputs are connected to the reset input of a processor (DSP, CPU, FPGA, ASIC, and so forth), or connected to the enable input of a voltage regulator (DC-DC, LDO, and so forth).

The TPS386000 provides open-drain reset outputs. Pullup resistors must be used to hold these lines high when $\overline{\text{RESETn}}$ is not asserted, or when RESETn is asserted. By connecting pullup resistors to the proper voltage rails (up to 6.5 V), $\overline{\text{RESETn}}$ or RESETn output nodes can be connected to the other devices at the correct interface voltage levels. The pullup resistor should be no smaller than 10 kΩ to ensure the safe operation of the output transistors. By using wired-OR logic, any combination of $\overline{\text{RESETn}}$ can be merged into one logic signal.

The TPS386040 provides pushpull reset outputs. The logic high level of the outputs is determined by the V_{DD} voltage. With this configuration, pullup resistors are not required and some board area can be saved. However, all the interface logic levels should be examined. All $\overline{\text{RESETn}}$ or RESETn connections must be compatible with the V_{DD} logic level.

The $\overline{\text{RESETn}}$ or RESETn outputs are defined for V_{DD} voltage higher than 0.9 V. To ensure that the target processor(s) are properly reset, the V_{DD} supply input should be fed by the available power rail as early as possible in application circuits. Table 1, Table 2, Table 3, and Table 4 are truth tables that describe how the outputs are asserted or released. Figure 1, Figure 2, Figure 3, and Figure 4 show the SVS-n timing diagrams. When the conditions are met, the device changes the state of SVS-n from asserted to released after a user-configurable delay time. However, the transitions from released-state to asserted-state are performed almost immediately with minimal propagation delay. Figure 3 describes the relationship between threshold voltages (V_{ITN} and V_{HYSN}) and SENSEm voltage; and all SVS-1, SVS-2, SVS-3, and SVS-4 have the same behavior of Figure 3.

8.4 Device Functional Modes

The following tables show the state of the output and the status of the part under various conditions.

Table 1. SVS-1 Truth Table

CONDITION		OUTPUT	STATUS
$\overline{\text{MR}}$ = Low	SENSE1 < V_{ITN}	$\overline{\text{RESET1}}$ = Low	Reset asserted
$\overline{\text{MR}}$ = Low	SENSE1 > V_{ITN}	$\overline{\text{RESET1}}$ = Low	Reset asserted
$\overline{\text{MR}}$ = High	SENSE1 < V_{ITN}	$\overline{\text{RESET1}}$ = Low	Reset asserted
$\overline{\text{MR}}$ = High	SENSE1 > V_{ITN}	$\overline{\text{RESET1}}$ = High	**Reset released after delay**

Table 2. SVS-2 Truth Table

CONDITION	OUTPUT	STATUS
SENSE2 < V_{ITN}	$\overline{\text{RESET2}}$ = Low	Reset asserted
SENSE2 > V_{ITN}	$\overline{\text{RESET2}}$ = High	**Reset released after delay**

Table 3. SVS-3 Truth Table

CONDITION	OUTPUT	STATUS
SENSE3 < V_{ITN}	$\overline{\text{RESET3}}$ = Low	Reset asserted
SENSE3 > V_{ITN}	$\overline{\text{RESET3}}$ = High	**Reset released after delay**

Table 4. SVS-4 Truth Table

CONDITION		OUTPUT	STATUS
SENSE4L < V_{ITN}	SENSE4H > V_{ITP}	$\overline{RESET4}$ = Low	Reset asserted
SENSE4L < V_{ITN}	SENSE4H < V_{ITP}	$\overline{RESET4}$ = Low	Reset asserted
SENSE4L > V_{ITN}	SENSE4H > V_{ITP}	$\overline{RESET4}$ = Low	Reset asserted
SENSE4L > V_{ITN}	SENSE4H < V_{ITP}	$\overline{RESET4}$ = High	**Reset released after delay**

Table 5. Watchdog Timer (WDT) Truth Table

CONDITION				OUTPUT	STATUS
$\overline{WDO}$	WDO	$\overline{RESET1}$	WDI PULSE INPUT		
Low	High	Asserted	Toggling	$\overline{WDO}$ = low	Remains in WDT time-out
Low	High	Asserted	610 ms after last WDI↑ or WDI↓	$\overline{WDO}$ = low	Remains in WDT time-out
Low	High	Released	Toggling	$\overline{WDO}$ = low	Remains in WDT time-out
Low	High	Released	610 ms after last WDI↑ or WDI↓	$\overline{WDO}$ = low	Remains in WDT time-out
High	Low	Asserted	Toggling	$\overline{WDO}$ = high	Normal operation
High	Low	Asserted	610 ms after last WDI↑ or WDI↓	$\overline{WDO}$ = high	Normal operation
High	Low	Released	Toggling	$\overline{WDO}$ = high	Normal operation
High	Low	Released	610 ms after last WDI↑ or WDI↓	$\overline{WDO}$ = low	Enters WDT timeout

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Undervoltage Detection

The SENSEm inputs are pins that allow any system voltages to be monitored. If the voltage at the SENSE1, SENSE2, SENSE3, or SENSE4L pins drops below V_{ITN}, then the corresponding reset outputs are asserted. If the voltage at the SENSE4H pin exceeds V_{ITP}, then $\overline{\text{RESET4}}$ or RESET4 is asserted. The comparators have a built-in hysteresis to ensure smooth reset output assertions and deassertions. In noisy applications, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the SENSEm input to reduce sensitivity to transients, layout parasitics, and interference between power rails monitored by this device. A typical connection of resistor dividers are shown in Figure 35. All the SENSEm pins can be used to monitor voltage rails down to 0.4 V. Threshold voltages can be calculated using Equation 1 to Equation 3.

$$V_{MON(1)} = (1 + R_{S1H}/R_{S1L}) \times 0.4\ (V) \quad (1)$$

$$V_{MON(2)} = (1 + R_{S2H}/R_{S2L}) \times 0.4\ (V) \quad (2)$$

$$V_{MON(3)} = (1 + R_{S3H}/R_{S3L}) \times 0.4\ (V) \quad (3)$$

9.1.2 Undervoltage and Overvoltage Detection

The comparator at the SENSE4H pin has the opposite comparison polarity to the other SENSEm pins. In the configuration shown in Figure 32, this comparator monitors overvoltage of the $V_{MON(4)}$ node; combined with the comparator at SENSE4L, SVS-4 forms a window comparator.

$$V_{MON(4,\ UV)} = \{1 + R_{S4H}/(R_{S4M} + R_{S4L})\} \times 0.4\ (V) \quad (4)$$

$$V_{MON(4,\ OV)} = \{1 + (R_{S4H} + R_{S4M})/R_{S4L}\} \times 0.4\ (V)$$

where

- $V_{MON(4,\ UV)}$ is the undervoltage threshold.
- $V_{MON(4,\ OV)}$ is the overvoltage threshold. (5)

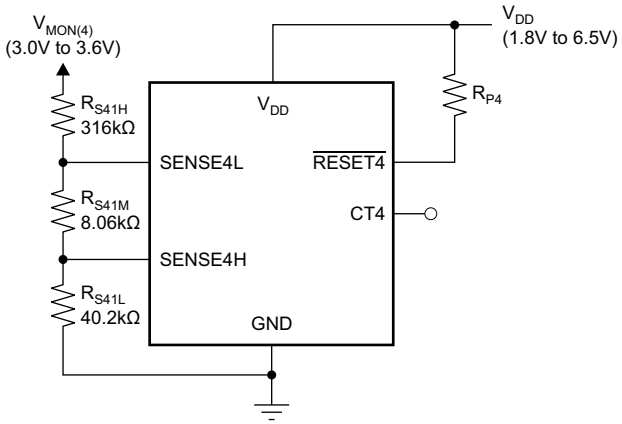


Figure 32. SVS-4: Window Comparator

Application Information (continued)

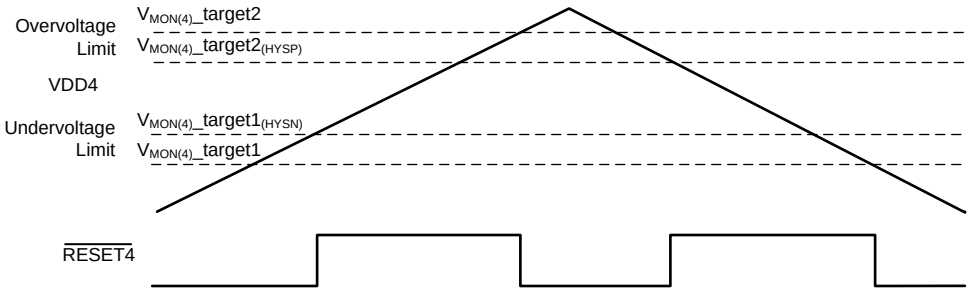


Figure 33. Window Comparator Operation

9.1.3 Sensing a Negative Voltage

By using voltage reference output VREF, the SVS-4 comparator can monitor negative voltage or positive voltage lower than 0.4V. Figure 34 shows this usage in an application circuit. SVS-4 monitors the positive and negative voltage power rail (for example, 15-V and –15-V supply to an op amp) and the $\overline{\text{RESET4}}$ or RESET4 output status continues to be as described in Table 4. R_{S42H} is located at higher voltage position than R_{S42L}. The threshold voltage calculations are shown in Equation 6 and Equation 7.

$$V_{MON(4,\ NEG)} = (1+R_{S41H}/R_{S41L}) \times 0.4\ (V) \quad (6)$$

$$V_{MON(4,\ POS)} = (1+R_{S42L}/R_{S42H}) \times 0.4 - R_{S42L}/R_{S42H} \times V_{REF} = 0.4 - [R_{S42L}/R_{S42H} \times 0.8\ (V)] \quad (7)$$

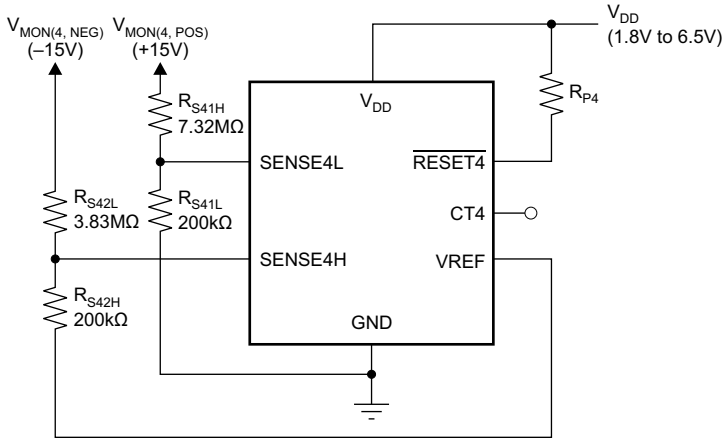


Figure 34. SVS4: Negative Voltage Sensing

Application Information (continued)

9.1.4 Reset Delay Time

Each of the SVS-n channels can be configured independently in one of three modes. Table 6 describes the delay time settings.

Table 6. Delay Timing Selection

CTn CONNECTION	DELAY TIME
Pullup to V_{DD}	300 ms (typical)
Open	20 ms (typical)
Capacitor to GND	Programmable

To select the 300-ms fixed delay time, the CTn pin should be pulled up to V_{DD} using a resistor from 40 kΩ to 200 kΩ. There is a pulldown transistor from CTn to GND that turns on every time the device powers on to determine and confirm CTn pin status; therefore, a direct connection of CTn to V_{DD} causes a large current flow. To select the 20-ms fixed delay time, the CTn pin should be left open. To program a user-defined adjustable delay time, an external capacitor must be connected between CTn and GND. The adjustable delay time can be calculated by the following equation:

$$C_{CT}\ (nF) = [t_{DELAY}\ (ms) – 0.5\ (ms)] \times 0.242 \quad (8)$$

Using this equation, a delay time can be set to between 1.4 ms to 10 s. The external capacitor should be greater than 220 pF (nominal) so that the TPS3860x0 can distinguish it from an open CT pin. The reset delay time is determined by the time it takes an on-chip, precision 300-nA current source to charge the external capacitor to 1.24 V. When the $\overline{\text{RESET}}$n or RESETn outputs are asserted, the corresponding capacitors are discharged. When the condition to release $\overline{\text{RESET}}$n or RESETn occurs, the internal current sources are enabled and begin to charge the external capacitors. When the CTn voltage on a capacitor reaches 1.24 V, the corresponding $\overline{\text{RESET}}$n or RESETn pins are released. A low leakage type capacitor (such as ceramic) should be used, and that stray capacitance around this pin may cause errors in the reset delay time.

9.2 Typical Application

Figure 35 shows a typical application circuit.

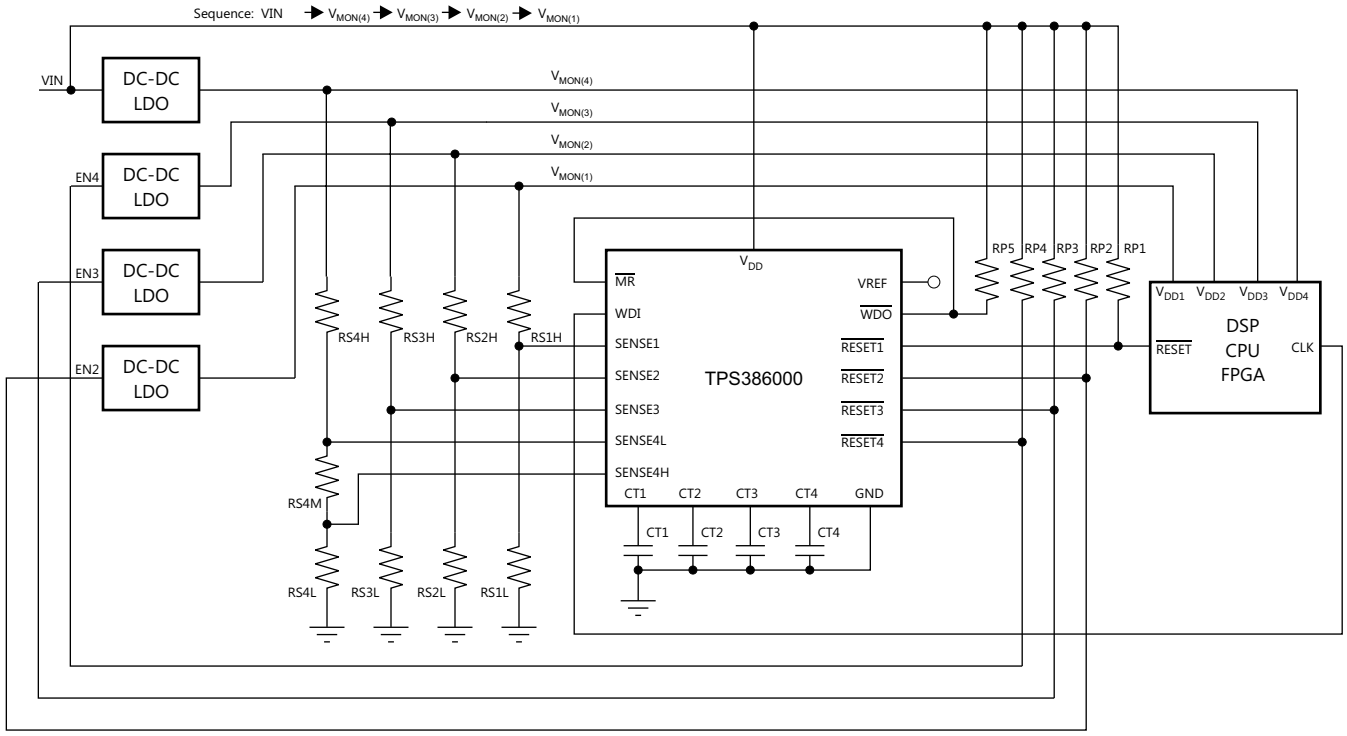


Figure 35. Typical Application Circuit

9.2.1 Design Requirements

This design is intended to monitor the voltage rails for an FPGA. Table 7 summarizes the design requirements.

Table 7. Design Requirements

PARAMETER	DESIGN REQUIREMENT
V_{DD}	5 V
$V_{MON(1)}$	1.8 V –5%
$V_{MON(2)}$	1.5 V –5%
$V_{MON(3)}$	1.2 V –5%
$V_{MON(4)}$	1 V ±5%
Approximate start-up time	100 ms

9.2.2 Detailed Design Procedure

Select the pullup resistors to be 100 kΩ to ensure that V_{OL} ≤ 0.4 V.

Use Equation 8 to set CT = 22 nF for all channels to obtain an approximate start-up delay of 100 ms.

Select RSnL = 10 kΩ for all channels to ensure DC accuracy.

Use Equation 1 through Equation 5 to determine the values of RSnH and RS4M. Using standard 1% resistors, Table 8 shows the results.

Table 8. Design Results

RESISTOR	VALUE (kΩ)
RS1H	32.4
RS2H	25.5
RS3H	18.7
RS4H	14.3
RS4M	1

The FPGA does not have a separate watchdog failure input, so a legacy connection is used by connecting $\overline{WDO}$ to $\overline{MR}$.

9.2.3 Application Curves

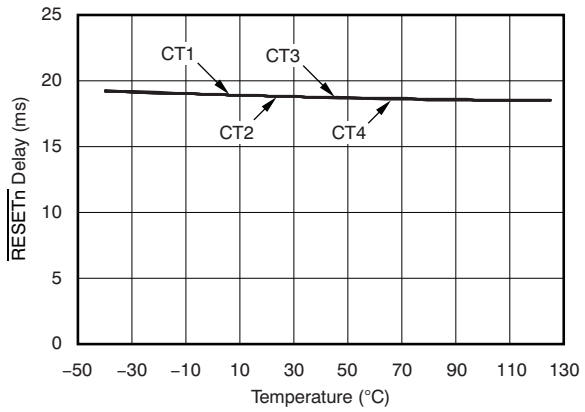
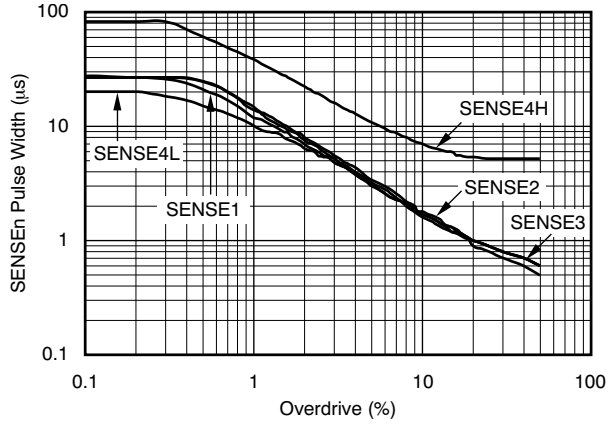


Figure 36. TPS386040 (CTn = Open) $\overline{RESETn}$ Time-Out Period vs Temperature



See Figure 29 for measurement technique

Figure 37. TPS386040 SENSEn Minimum Pulse Width vs SENSEn Threshold Overdrive Voltage

10 Power Supply Recommendations

The TPS386000 can operate from a 1.8-V to a 6.5-V input supply. TI recommends placing a 0.1-µF capacitor placed next to the V_{DD} pin to the GND node. This power supply should not be less than 1.8 V in normal operation to ensure that the internal UVLO circuit does not assert reset.

11 Layout

11.1 Layout Guidelines

Follow these guidelines to lay out the printed-circuit board (PCB) that is used for the TPS3860x family of devices.

- Keep the traces to the timer capacitors as short as possible to optimize accuracy.
- Avoid long traces from the SENSE pin to the resistor divider. Instead, run the long traces from the RSnH to $V_{MON(n)}$.
- Place the V_{DD} decoupling capacitor (C_{VDD}) close to the device.
- Avoid using long traces for the V_{DD} supply node. The V_{DD} capacitor (C_{VDD}), along with parasitic inductance from the supply to the capacitor, can form an LC tank and create ringing with peak voltages above the maximum V_{DD} voltage.

11.2 Layout Example

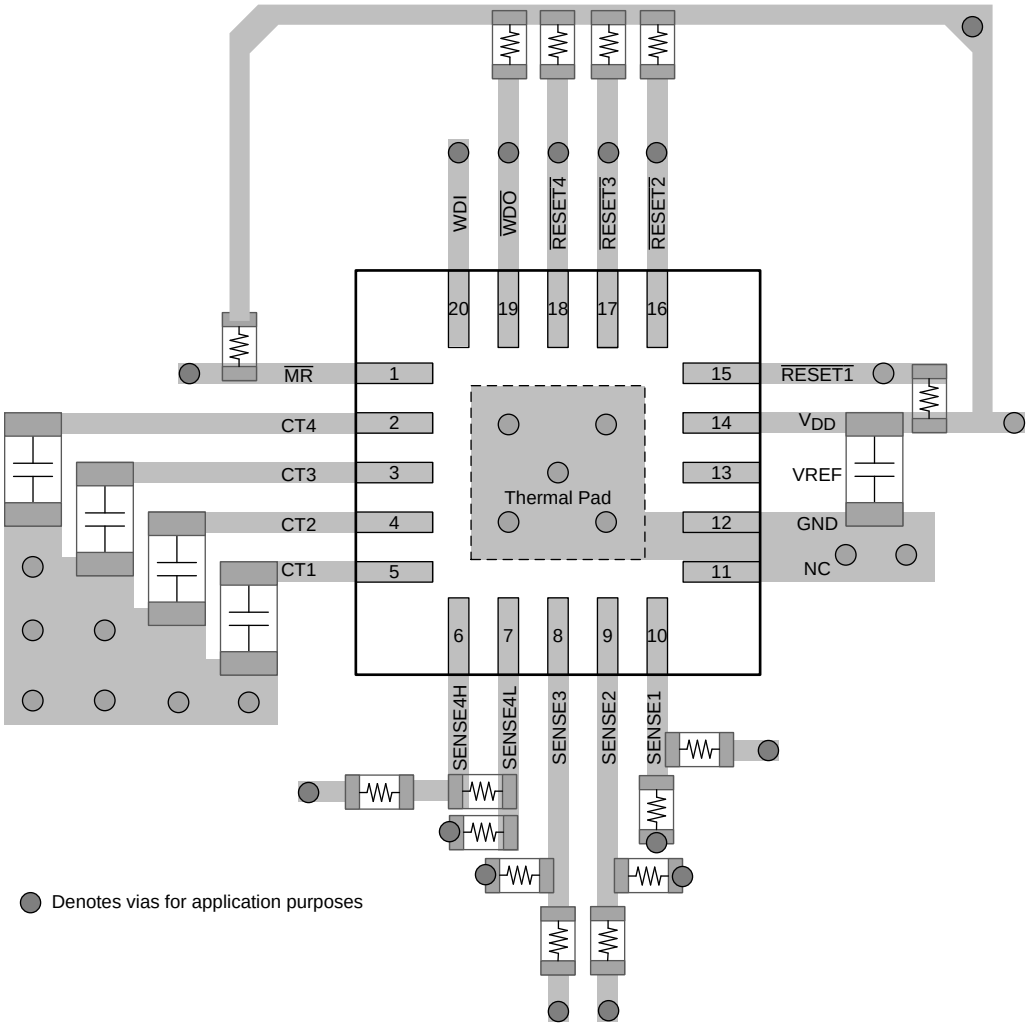


Figure 38. Example Layout (RGP Package)

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 評価モジュール

TPS3860x0を使用する回路の性能の初期評価に役立てるため、2つの評価モジュール(EVM)を利用可能です。TPS386000EVM-736評価モジュールおよびTPS386040EVM評価モジュールは、テキサス・インスツルメンツWebサイトのデバイス製品フォルダで請求するか、TI eStoreから直接お求めになれます。

12.1.1.2 SPICEモデル

SPICEを使用した回路パフォーマンスのコンピュータによるシミュレーションは、アナログ回路やシステムのパフォーマンスを分析するため多くの場合に有用です。TPS3860x0のSPICEモデルは、該当デバイスの製品フォルダで「シミュレーション・モデル」から入手できます。

12.1.2 デバイスの項目表記

表 9. デバイスの項目表記(1)

製品名	概要
TPS3860**x**0**yyy***z*	**x**はデバイス構成オプションです。 **x** = 0:オープン・ドレイン、アクティブLOW **x** = 4:プッシュプル、アクティブLOW **yyy**はパッケージ指定子です。 **z**はパッケージ数量です。

(1) 最新のパッケージ情報と注文情報については、このデータシートの末尾にあるパッケージ・オプションについての付録を参照するか、TIのWebサイト(www.ti.com)をご覧ください。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- 『*TPS3860xxEVM-736 ユーザー・ガイド*』、SLVU450
- 『*TPS386000およびTPS386040 EVM ユーザー・ガイド*』、SLVU341

12.3 関連リンク

表 10 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 10. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS386000	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS386040	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E (Engineer-to-Engineer) コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

12.5 商標

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12.6 静電気放電に関する注意事項

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS386000RGPR	ACTIVE	QFN	RGP	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 386000	Samples
TPS386000RGPT	ACTIVE	QFN	RGP	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 386000	Samples
TPS386040RGPR	ACTIVE	QFN	RGP	20	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 386040	Samples
TPS386040RGPT	ACTIVE	QFN	RGP	20	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TPS 386040	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
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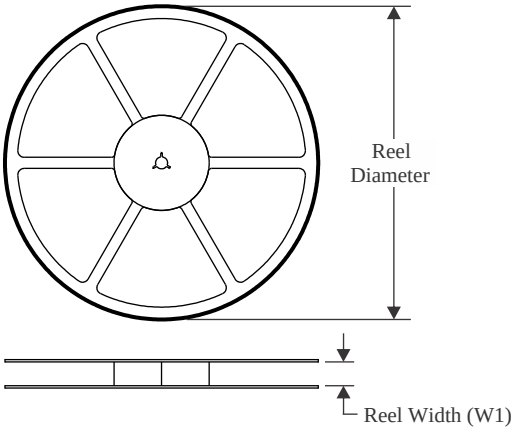
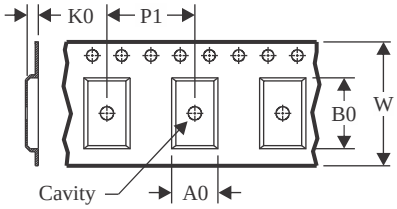
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

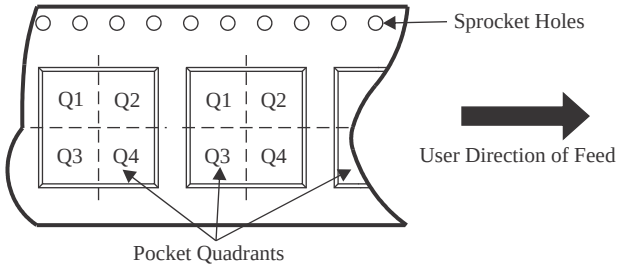


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

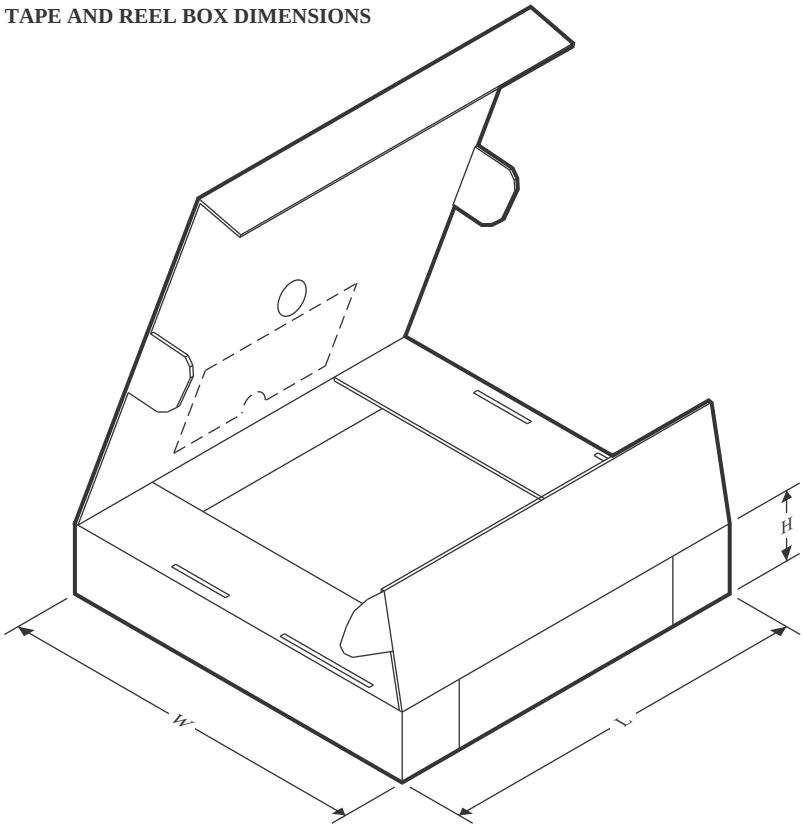
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS386000RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS386000RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS386040RGPR	QFN	RGP	20	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS386040RGPT	QFN	RGP	20	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS386000RGPR	QFN	RGP	20	3000	356.0	356.0	35.0
TPS386000RGPT	QFN	RGP	20	250	210.0	185.0	35.0
TPS386040RGPR	QFN	RGP	20	3000	356.0	356.0	35.0
TPS386040RGPT	QFN	RGP	20	250	210.0	185.0	35.0

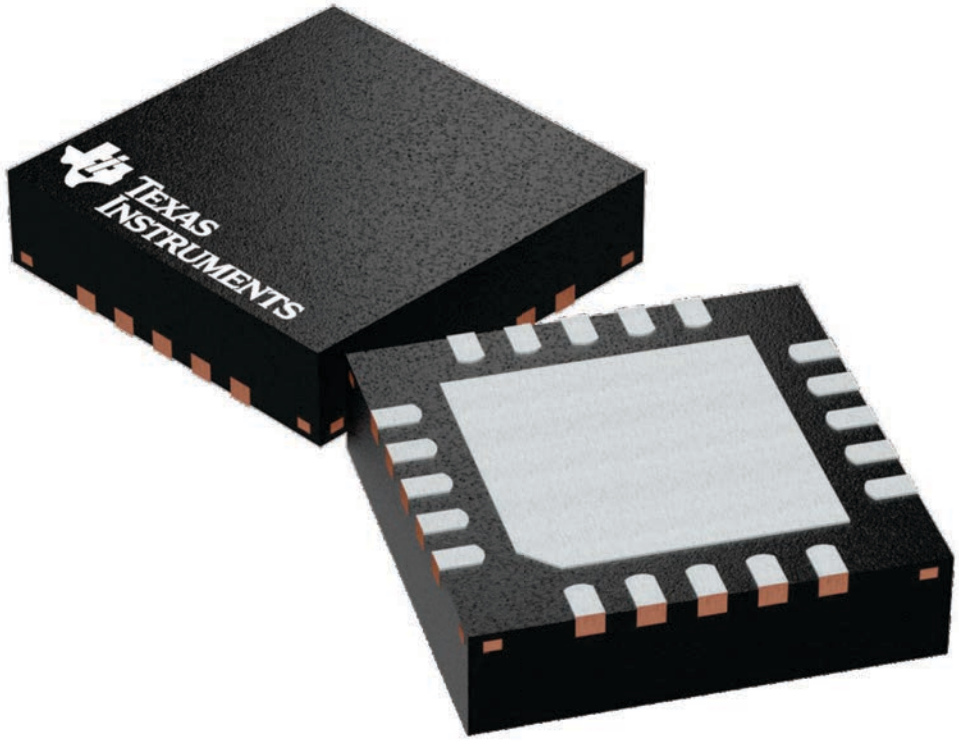
GENERIC PACKAGE VIEW

RGP 20

VQFN - 1 mm max height

4 x 4, 0.5 mm pitch

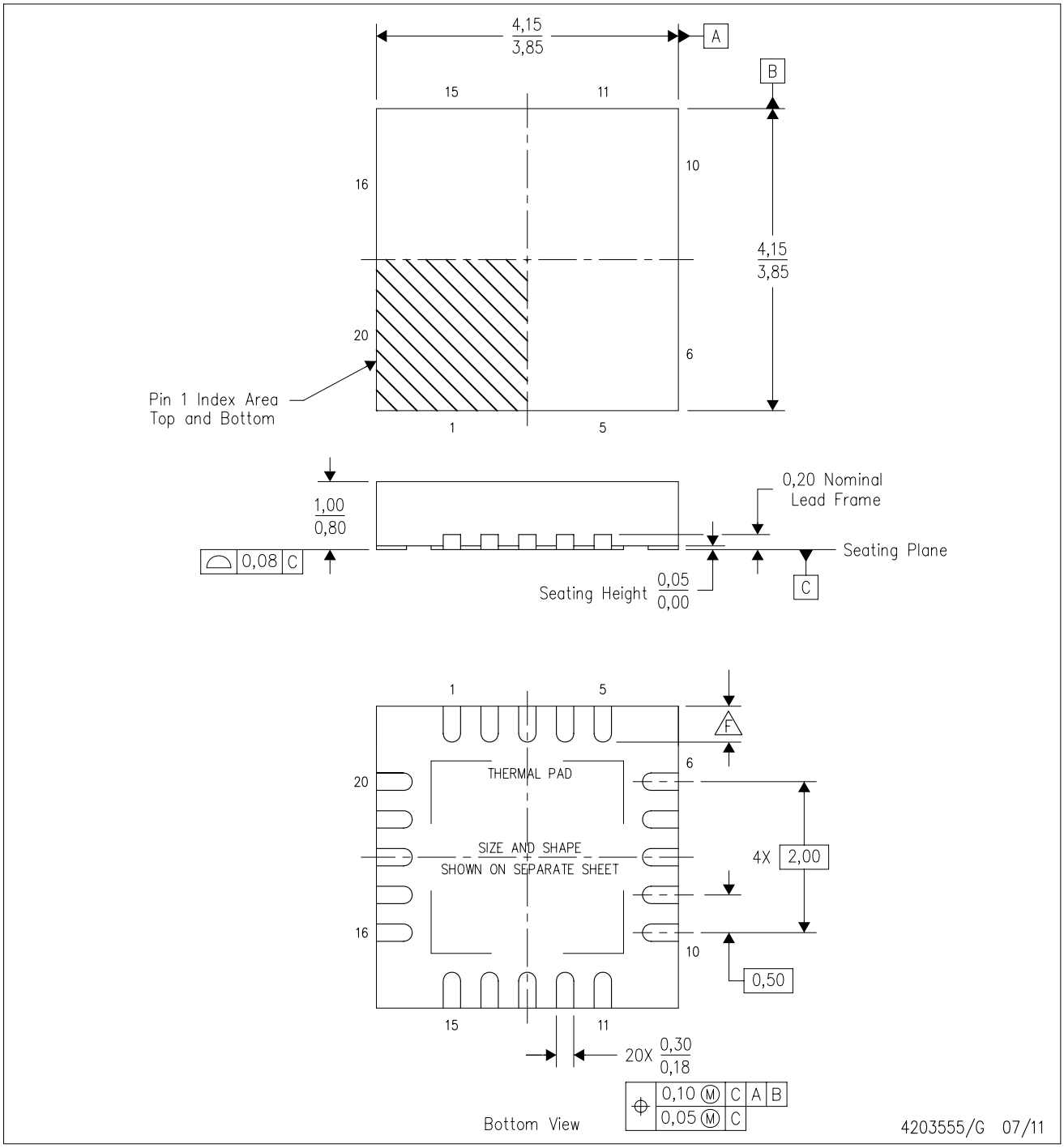
VERY THIN QUAD FLATPACK



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224735/A

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

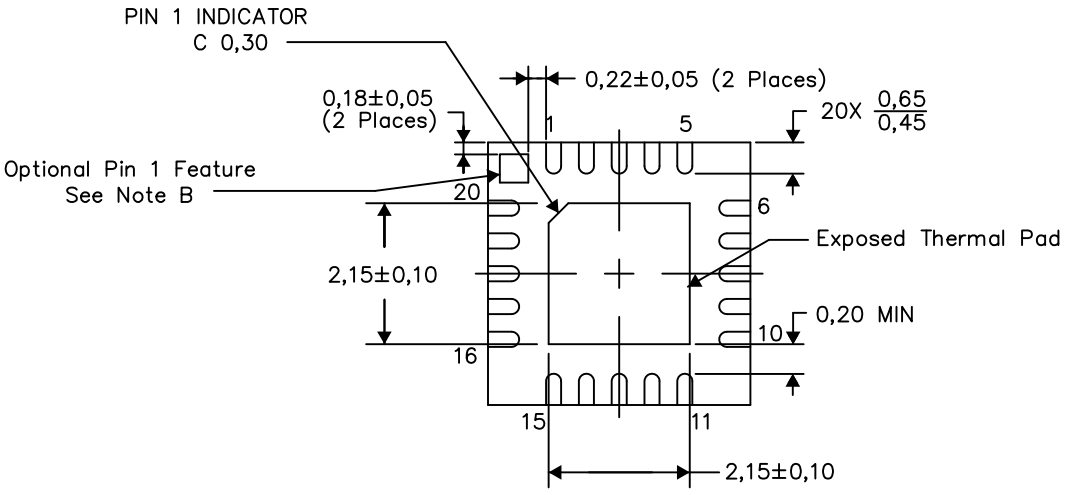
RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

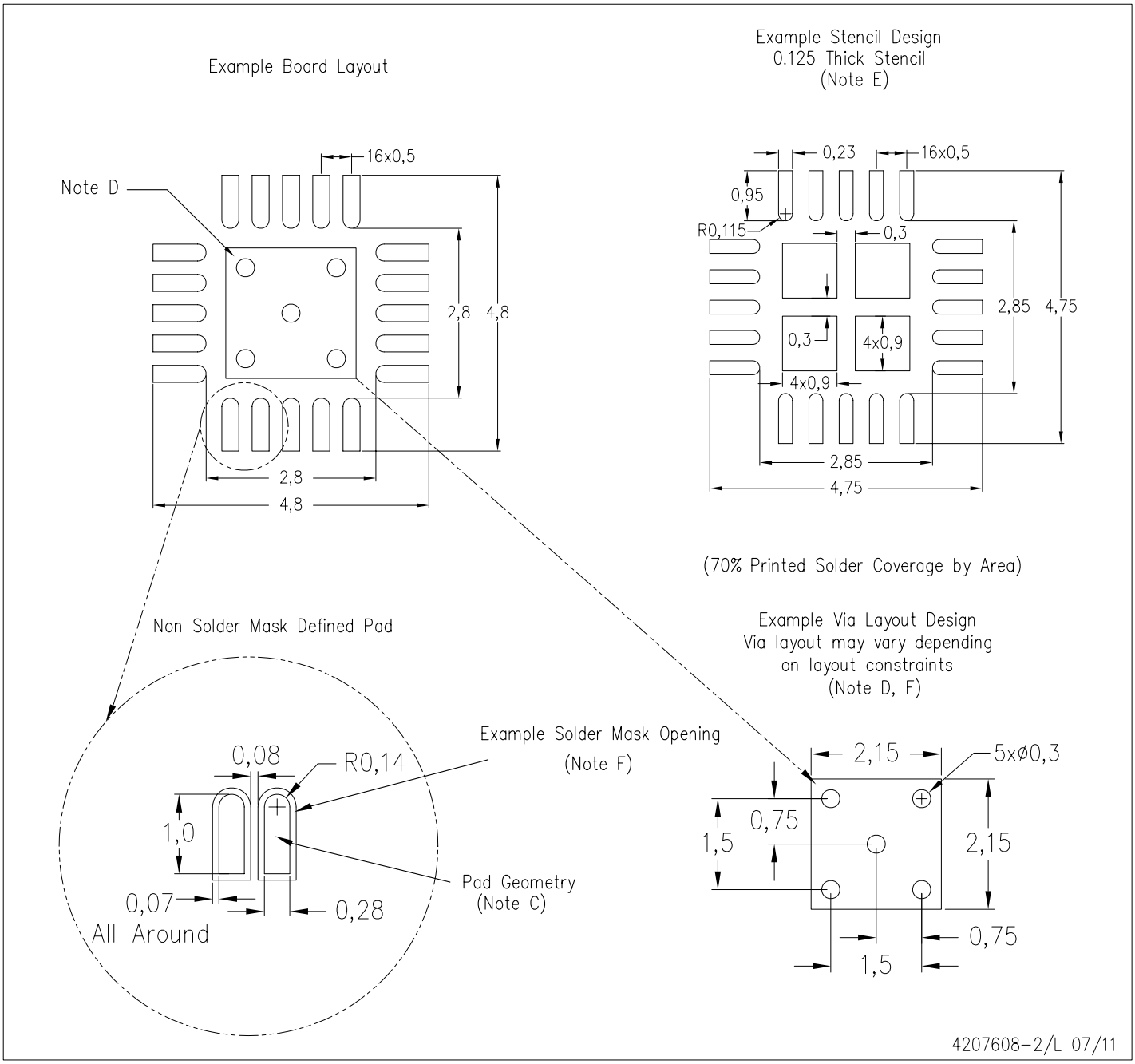
Exposed Thermal Pad Dimensions

4206346–2/AA 11/13

NOTES: A. All linear dimensions are in millimeters

B. The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGP (S–PVQFN–N20) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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