参考資料

TPS22996H-Q1 5.5V、4A、13mΩ オン抵抗、デュアル チャネル車載用ロード スイッチ

1 特長

- 統合型デュアル チャネル負荷スイッチ
- 入力電圧範囲：0.6V～V_{BIAS}
- V_{BIAS} 電圧範囲：2.5V～5.5V
- オン抵抗：
  - R_{ON} = 13mΩ (標準値) (V_{IN} = 0.6V～5V、V_{BIAS} = 5V)
- チャネルごとに 4A の最大連続スイッチング電流
- 静止電流：
  - 18μA (標準値、両チャネル) (V_{IN} = V_{BIAS} = 5V)
  - 13μA (標準値、単一チャネル) (V_{IN} = V_{BIAS} = 5V)
- 耐湿性：
  - 以下の条件において、デバイスは機能 (オン、オフ、保護) を維持しますが、タイミング仕様は影響を受けます。
    - グランドへ 100kΩ 短絡
    - 電源へ 100kΩ 短絡
- 制御入力スレッショルドにより、1.2V、1.8V、2.5V、3.3V ロジックを使用可能
- 立ち上がり時間を設定可能
- サーマル シャットダウン
- クイック出力放電 (QOD)

2 アプリケーション

- インフォテインメント
- クラスタ
- 先進運転支援システム (ADAS)

3 概要

TPS22996H-Q1 は、ターンオン制御付きのデュアル チャネル ロード スイッチです。入力電圧範囲 0.6V～5.5V で動作する 2 つの N チャネル MOSFET を備えており、各チャネル最大 4A の連続電流をサポートできます。各スイッチは、低電圧制御信号と直接インターフェイス可能なオン入力とオフ入力 (ON1 および ON2) により独立して制御されます。このデバイスは、接合部温度がスレッショルドを超えたときにサーマル シャットダウンでスイッチを切断できます。接合部温度が安全範囲で安定化すると、スイッチが再びオンになります。このデバイスは、スイッチがオフになったときクイック出力放電を行えるように、230Ω のオンチップ負荷抵抗を備えています。

TPS22996H-Q1 のピンは高湿度条件に耐性があるため、デバイスはどのピンからでも GND や電源に対して 100kΩ の短絡状態で機能できます。

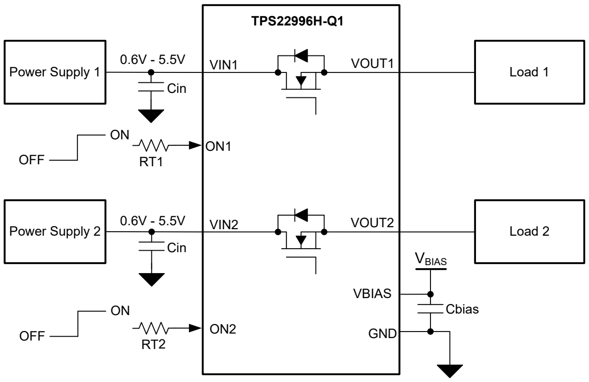
TPS22996H-Q1 は、省スペースの 2.1mm × 1.2mm 8-DYC パッケージで供給されます。周囲温度 –40℃～125℃での動作が規定されています。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TPS22996H	DYC (SOT、8)	2.1mm × 1.2mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション回路

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4 Pin Configuration and Functions

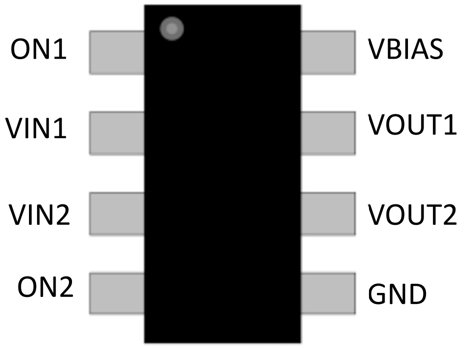


図 4-1. DYC Package, 8-Pin SOT (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ON1	Input	Active-high switch 1 control input. Connect series resistor to set Slew Rate. Do not leave floating. See セクション 7.3.7 for more information.
2	VIN1	Input	Switch 1 input. Recommended voltage range for these pins for optimal R_{ON} performance is 0.6V to V_{BIAS}. Place an optional decoupling capacitor between these pins and GND to reduce V_{IN1} dip during turnon of the channel. See セクション 8.2 for more information.
3	VIN2	Input	Switch 2 input. Recommended voltage range for these pins for optimal R_{ON} performance is 0.6V to V_{BIAS}. Place an optional decoupling capacitor between these pins and GND to reduce V_{IN2} dip during turnon of the channel. See セクション 8.2 for more information.
4	ON2	Input	Active-high switch 2 control input. Connect series resistor to set slew rate. Do not leave floating. See セクション 7.3.7 for more information.
5	GND	—	Device ground.
6	VOUT2	Output	Switch 2 output.
7	VOUT1	Output	Switch 1 output.
8	VBIAS	Input	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5V to 5.5V. See セクション 8.1.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
$V_{IN1 ,2}$	Input Voltage	–0.3	6	V
$V_{OUT1,2}$	Output Voltage	–0.3	6	V
$V_{ON1,2}$	ON Pin Voltage	–0.3	6	V
V_{BIAS}	Bias Voltage	–0.3	6	V
I_{MAX}	Maximum continuous current per channel		4	A
$I_{MAX,PLS}$	Maximum pulsed current switch per channel, pulse <300µs, 3% duty cycle		5.5	A
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD, VIN1,VIN2,VOUT1,VOUT2 pins	±500	
		Charged-device model (CDM), per AEC Q100-011 CDM ESD, ON1,ON2,VBIAS pins	±750	V

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN1,2}$	Input Voltage	0.6		V_{BIAS}	V
V_{BIAS}	Bias Voltage	2.5		5.5	V
$V_{ON1,2}$	ON Pin Voltage	0		5.5	V
$V_{OUT1,2}$	Output Voltage	0		V_{IN}	V
V_{IH}	High-Level Input Voltage, ON	1.2		5.5	V
V_{IL}	Low-Level Input Voltage, ON	0		0.5	V
T_A	Ambient Temperature	–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS22996H-Q1	UNIT
		DYC	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	73.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.3	°C/W

THERMAL METRIC[1]		TPS22996H-Q1 DYC 8 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
Power Supplies and Currents								
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (Both channels)	$I_{OUT1} = I_{OUT2}$ = 0mA, $V_{IN1,2} = V_{ON1,2}$ = 5V		25°C		18		µA
				-40°C to 85°C		18	22	µA
				-40°C to 125°C			25	µA
$I_{Q,VBIAS}$	V_{BIAS} Quiescent Current (Single-channel)	$I_{OUT1} = I_{OUT2}$ = 0mA, V_{ON2} = 0V, $V_{IN1,2} = V_{IN1}$ = 5V		25°C		13		µA
				-40°C to 85°C		13	17	µA
				-40°C to 125°C			19	µA
$I_{SD,VBIAS}$	V_{BIAS} Shutdown Current	$V_{ON1,2}$ = 0V, $V_{OUT1,2}$ = 0V		25°C		0.005	1	µA
				-40°C to 85°C		0.005	1	µA
				-40°C to 125°C		0.005	1	µA
$I_{SD,VIN}$	V_{IN} Shutdown Current (per channel)	V_{ON} = 0V, V_{OUT} = 0V	V_{IN} = 5V	25°C		0.002	0.8	µA
				-40°C to 85°C		0.002	0.8	µA
				-40°C to 125°C			1	µA
			V_{IN} = 3.3V	25°C		0.002	0.8	µA
				-40°C to 85°C		0.002	0.8	µA
				-40°C to 125°C			1	µA
			V_{IN} = 1.8V	25°C		0.002	0.8	µA
				-40°C to 85°C		0.002	0.8	µA
				-40°C to 125°C			1	µA
			V_{IN} = 0.6V	25°C		0.002	0.8	µA
				-40°C to 85°C		0.002	0.8	µA
				-40°C to 125°C			1	µA
I_{ON}	ON Pin Leakage Current		V_{ON} = 5.5V	-40°C to 125°C			0.1	µA
Resistance Characteristics								
R_{ON}	On-Resistance	I_{OUT} = -200mA	V_{IN} = 5V	25°C		13	15	mΩ
				-40°C to 85°C			18	mΩ
				-40°C to 125°C			22	mΩ
			V_{IN} = 3.3V	25°C		13	15	mΩ
				-40°C to 85°C			18	mΩ
				-40°C to 125°C			22	mΩ
			V_{IN} = 1.8V	25°C		13	15	mΩ
				-40°C to 85°C			18	mΩ
				-40°C to 125°C			22	mΩ
			V_{IN} = 0.6V	25°C		13	15	mΩ
				-40°C to 85°C			18	mΩ
				-40°C to 125°C			22	mΩ
$V_{ON,VIH}$	VIH	V_{IN} = 5V	V_{IN} = 5V	-55°C to 125°C	1.2			V

5.5 Electrical Characteristics (続き)

over operating free-air temperature range (unless otherwise noted)

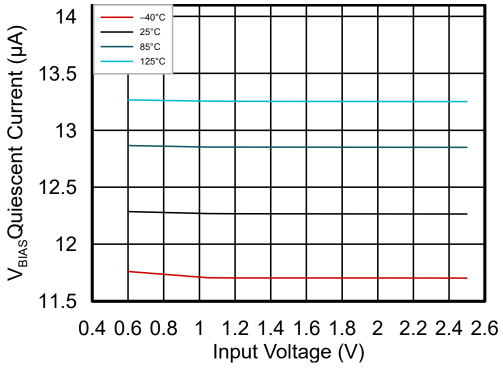
PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$V_{ON,VIL}$	VIL	V_{IN} = 5V	V_{IN} = 5V	-55°C to 125°C			0.65	V
$V_{ON,HYS}$	ON Pin Hysteresis	V_{IN} = 5V		-55°C to 125°C		90		mV
R_i	Internal On Pin Resistance	V_{ON} = 5V	V_{ON} = 5V	-55°C to 125°C		12.5		kΩ
R_{PD}	Output Pulldown Resistance	V_{IN} = V_{OUT} = 5V, VO_N = 0V		-40°C to 125°C		230	300	Ω
T_{SD}	Thermal Shutdown	Junction Temperature Rising		-		175		°C
$T_{SD,HYS}$	Thermal Shutdown Hysteresis	Junction Temperature Falling		-		20		°C

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

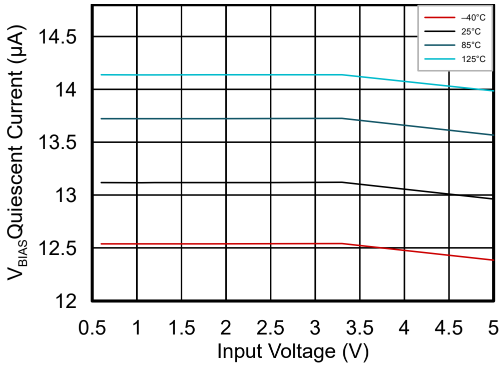
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN = VON = VBIAS = 5V						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA		946		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA		2.1		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA		626		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA		2.1		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA		320		µs
VIN = 0.6V, VON = VBIAS = 5V						
t_{ON}	Turn ON Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA,		587		µs
t_{OFF}	Turn OFF Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA		2.1		µs
t_R	Rise Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA		203		µs
t_F	Fall Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA		2.52		µs
t_D	Delay Time	R_L = 10Ω, C_L = 0.1uF, I_{ON} = 100 uA		384		µs

5.7 Typical DC Characteristics



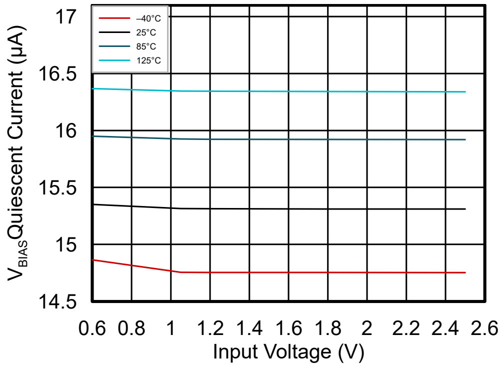
V_{BIAS} = 2.5 V

図 5-1. V_{BIAS} Quiescent Current vs Input Voltage Single Channel



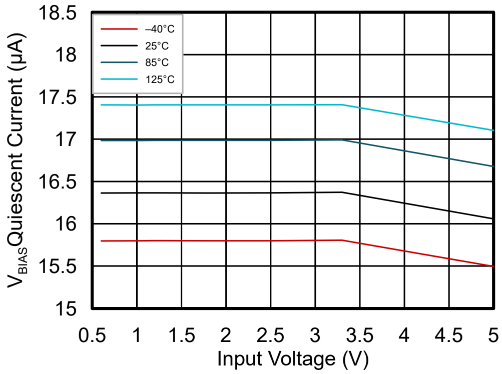
V_{BIAS} = 5 V

図 5-2. V_{BIAS} Quiescent Current vs Input Voltage Single Channel



V_{BIAS} = 2.5 V

図 5-3. V_{BIAS} Quiescent Current vs Input Voltage Both Channel



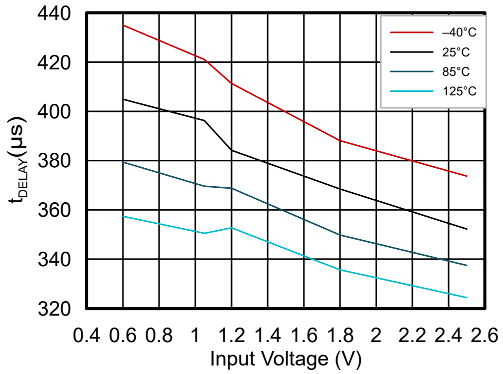
V_{BIAS} = 5 V

図 5-4. V_{BIAS} Quiescent Current vs Input Voltage Both Channel

5.8 Typical AC Characteristics

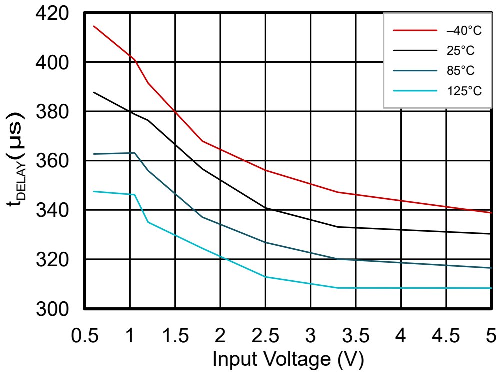
AC Characteristics

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, V_{ON} = 5 V, I_{ON} = 100 µA unless otherwise noticed



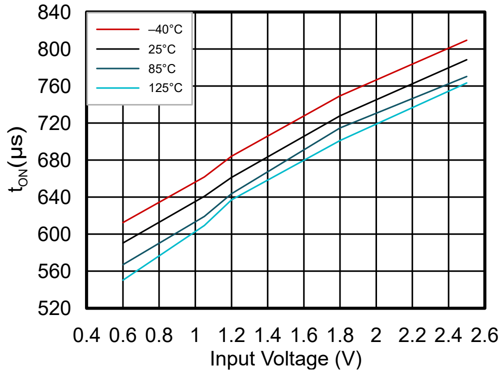
V_{BIAS} = 2.5 V

図 5-5. Delay Time vs Input Voltage



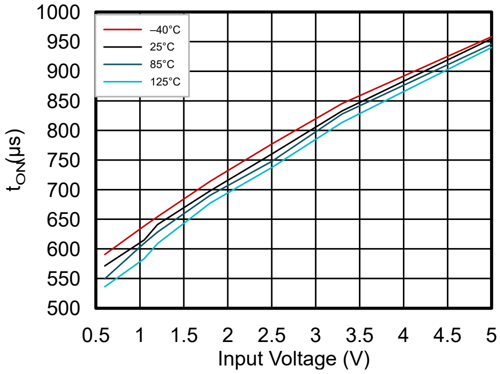
V_{BIAS} = 5 V

図 5-6. Delay Time vs Input Voltage



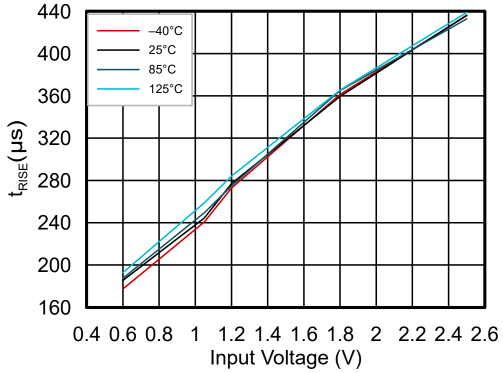
V_{BIAS} = 2.5 V

図 5-7. Turnon Time vs Input Voltage



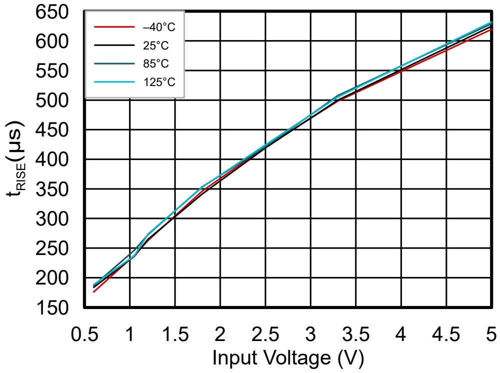
V_{BIAS} = 5 V

図 5-8. Turnon Time vs Input Voltage



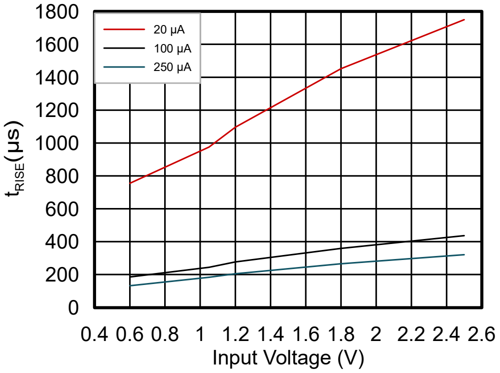
V_{BIAS} = 2.5 V

図 5-9. Rise Time vs Input Voltage



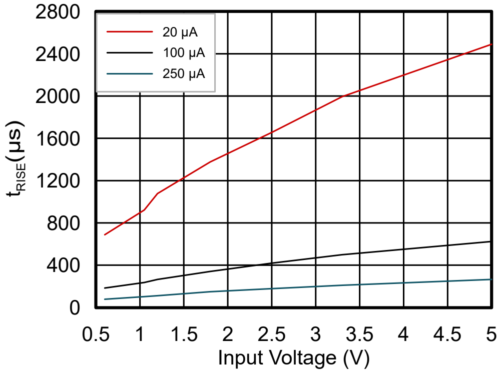
V_{BIAS} = 5 V

図 5-10. Rise Time vs Input Voltage



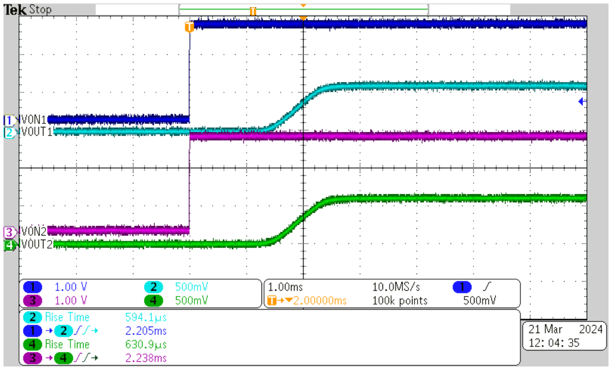
T_{AMB} = 25 ℃ V_{BIAS} = 2.5 V

図 5-11. Rise Time vs Input Voltage with Different I_{ON}



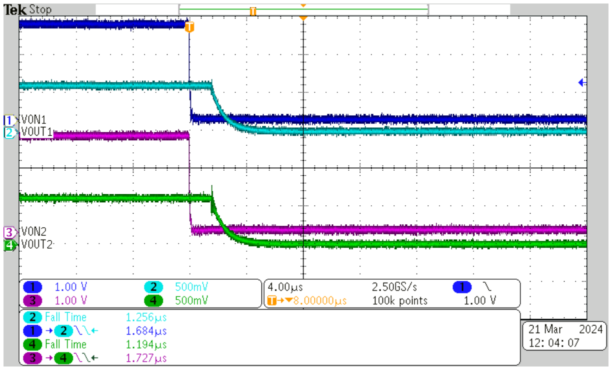
T_{AMB} = 25 ℃ V_{BIAS} = 5 V

図 5-12. Rise Time vs Input Voltage with Different I_{ON}



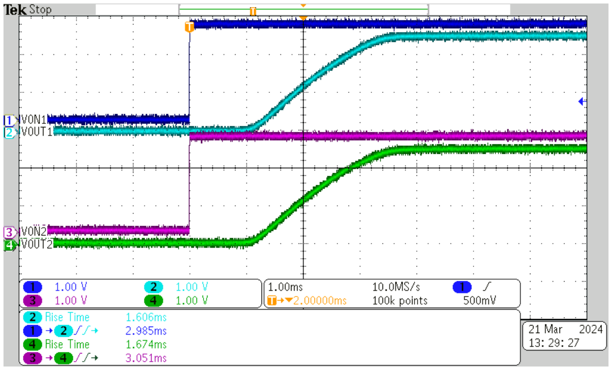
V_{BIAS} = 2.5 V V_{IN} = 0.6 V I_{ON} = 20 µA

図 5-13. Turnon Response Time



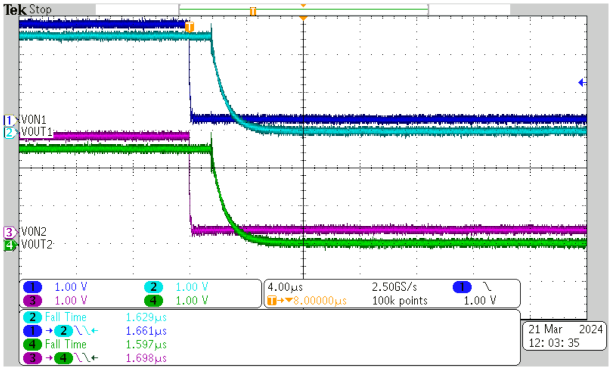
V_{BIAS} = 2.5 V V_{IN} = 0.6 V I_{ON} = 20 µA

図 5-14. Turnoff Response Time



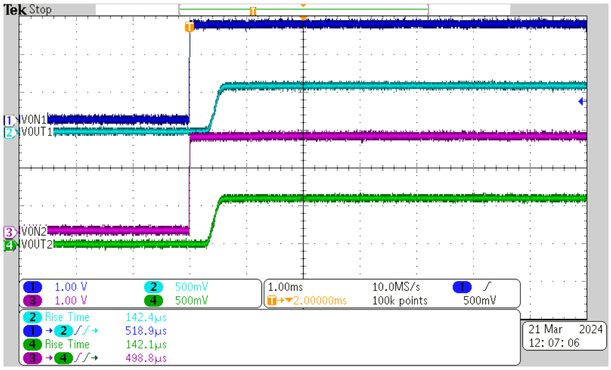
V_{BIAS} = 2.5 V V_{IN} = 2.5 V I_{ON} = 20 µA

図 5-15. Turnon Response Time



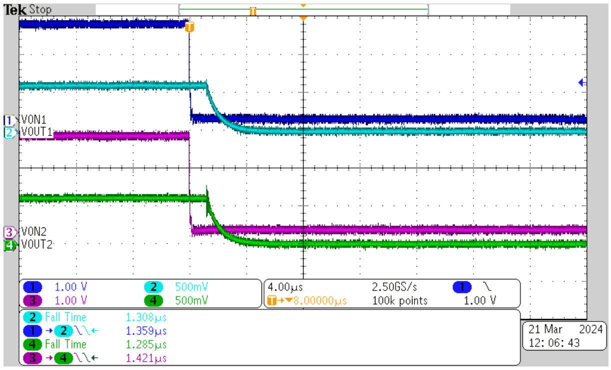
V_{BIAS} = 2.5 V V_{IN} = 2.5 V I_{ON} = 20 µA

図 5-16. Turnoff Response Time



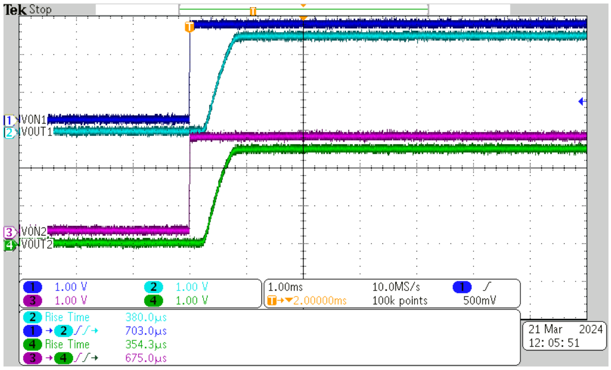
V_{BIAS} = 2.5 V V_{IN} = 0.6 V I_{ON} = 100 µA

図 5-17. Turnon Response Time



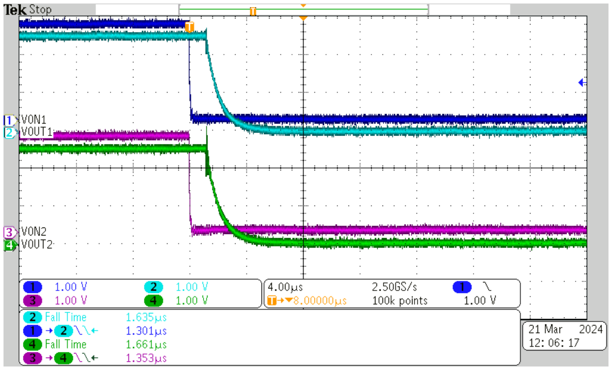
V_{BIAS} = 2.5 V V_{IN} = 0.6 V I_{ON} = 100 µA

図 5-18. Turnoff Response Time



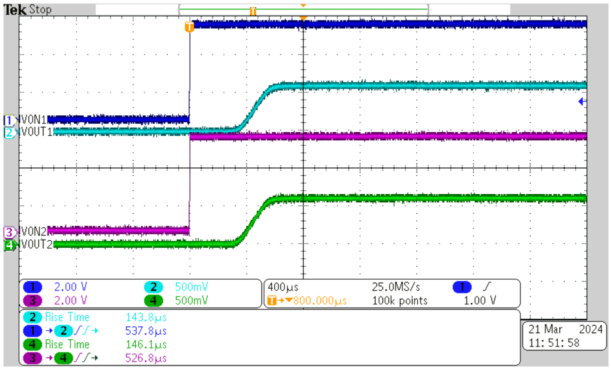
V_{BIAS} = 2.5 V V_{IN} = 2.5 V I_{ON} = 100 µA

図 5-19. Turnon Response Time



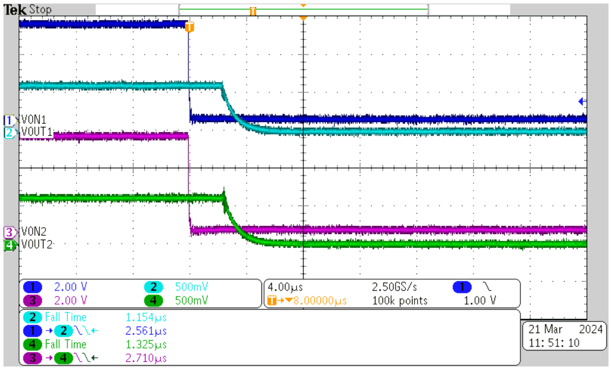
V_{BIAS} = 2.5 V V_{IN} = 2.5 V I_{ON} = 100 µA

図 5-20. Turnoff Response Time



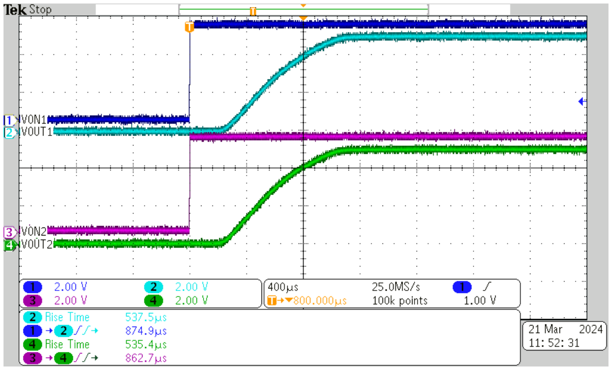
V_{BIAS} = 5 V V_{IN} = 0.6 V I_{ON} = 100 µA

図 5-21. Turnon Response Time



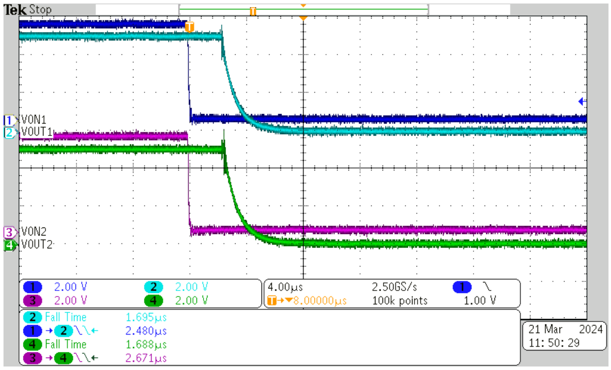
V_{BIAS} = 5 V V_{IN} = 0.6 V I_{ON} = 100 µA

図 5-22. Turnoff Response Time



V_{BIAS} = 5 V V_{IN} = 5 V I_{ON} = 100 µA

図 5-23. Turnon Response Time



V_{BIAS} = 5 V V_{IN} = 5 V I_{ON} = 100 µA

図 5-24. Turnoff Response Time

6 Parameter Measurement Information

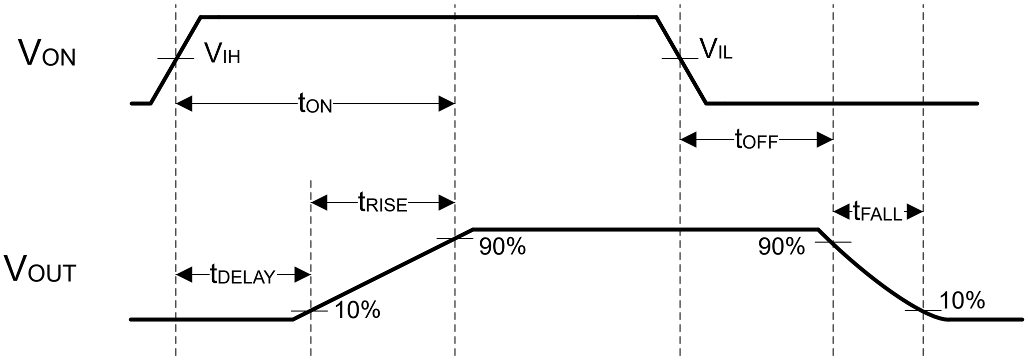


図 6-1. t_{ON} and t_{OFF} Waveforms

7 Detailed Description

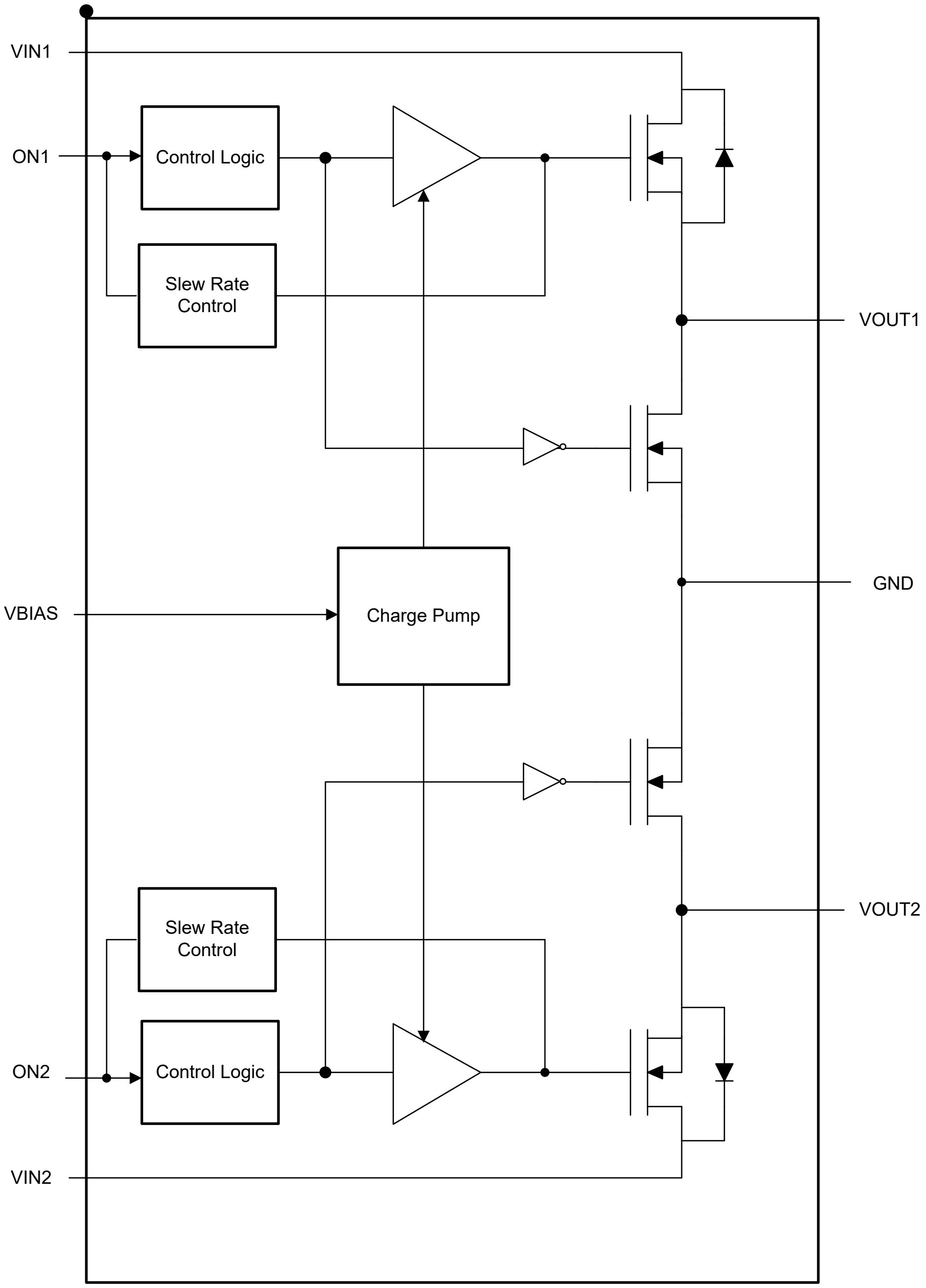
7.1 Overview

The TPS22996H-Q1 is a 5.5V, dual-channel, 13mΩ (typical) R_{ON} load switch in a 8-pin DYC package. Each channel can support a maximum continuous current of 4A and is controlled by an on and off GPIO-compatible input. To reduce the voltage drop in high current rails, the device implements N-channel MOSFETs. Note that the ON pins must be connected and cannot be left floating. The device has a configurable slew rate for applications that require specific rise-time, which controls the inrush current. By controlling the inrush current, power supply sag can be reduced during turnon. Furthermore, the slew rate is proportional to the series resistor used on the ONx pin. See セクション 7.3.7 to determine the correct resistor value for a desired rise time.

The internal circuitry is powered by the V_{BIAS} pin, which supports voltages from 2.5V to 5.5V. This circuitry includes the charge pump, QOD, and control logic. When a voltage is applied to V_{BIAS}, and the $ON_{1,2}$ pins transition to a low state, the QOD functionality is activated. This connects V_{OUT1} and V_{OUT2} to ground through the on-chip resistor. The typical pulldown resistance (R_{PD}) is 230Ω.

During the off state, the device prevents downstream circuits from pulling high standby current from the supply. The integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, reducing solution size and bill of materials (BOM) count.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 ON and OFF Control

The ON pins control the state of the switch. Asserting ON high enables the switch. ON is active high with a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

7.3.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

7.3.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from VOUT to VIN. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turnon due to inrush currents. This can be mitigated by increasing the RT resistance on the ON pin for a longer rise time (see セクション 7.3.7).

7.3.4 Quick Output Discharge

When the switch is disabled, an internal discharge resistance is connected between VOUT and GND to remove the remaining charge from the output. This resistance prevents the output from floating while the switch is disabled. For best results, it is recommended that the device gets disabled before V_{BIAS} falls below the minimum recommended voltage.

7.3.5 Humidity Resistance

TPS22996H-Q1 is designed to be resistant to humidity, which is replicated by 100kΩ short between any pin to either GND or power. Under such humidity conditions, our device is able to function correctly with ON, OFF and thermal shutdown. However, the timing parameter will be affected by the short condition, and will deviate from the typical value listed in the *Electrical Characteristics* table (see セクション 5.5).

7.3.6 Thermal Shutdown

Thermal shutdown protects the part from internally or externally generated excessive temperatures. When the device temperature exceeds T_{SD}, the switch is turned off. The switch automatically turns on again if the temperature of the die drops $T_{SD,HYS}$ below the T_{SD} threshold.

7.3.7 Adjustable Rise Time

TPS22996H-Q1 integrates a unique architecture for adjusting the rise time. The device senses the current flowing into the ON1 and ON2 (I_{ON}) pins and utilizes the information to set the rise time. This allows the user to adjust the rise time by connecting a series resistance that is determined by the ON pin voltage. Refer to 表 7-1 for reference on setting the resistor.

表 7-1. Typical Rise Time (VBIAS = 5V)

I_{ON}	V_{IN} = 0.6V	V_{IN} = 1.8V	V_{IN} = 2.5V	V_{IN} = 3.3V	V_{IN} = 5V
20µA	764µs	1380µs	1700µs	1955µs	2350µs
100µA	203µs	343µs	426µs	500µs	626µs
250µA	85µs	148µs	180µs	208µs	265µs

表 7-2. Typical Rise Time (VBIAS = 3.3V)

I_{ON}	V_{IN} = 0.6V	V_{IN} = 1.8V	V_{IN} = 2.5V	V_{IN} = 3.3V
20µA	738µs	1420µs	1735µs	2040µs
100µA	191µs	360µs	437µs	512µs
250µA	88µs	239µs	170µs	204µs

The following equation can be used to estimate the series resistance required to meet the desired rise time.

$$R_{Tx} = 1000 \times (V_{ONx\_GPIO} - 1.2V) / I_{ONx} - R_i \quad (1)$$

where:

- R_{Tx} = Channel × series resistance in kΩ.
- R_i = Internal ON pin resistance kΩ.
- V_{ONx_GPIO} = Channel × GPIO voltage connected to ONx pin in V.
- I_{ONx} = Current flowing into the ONx pin in µA.

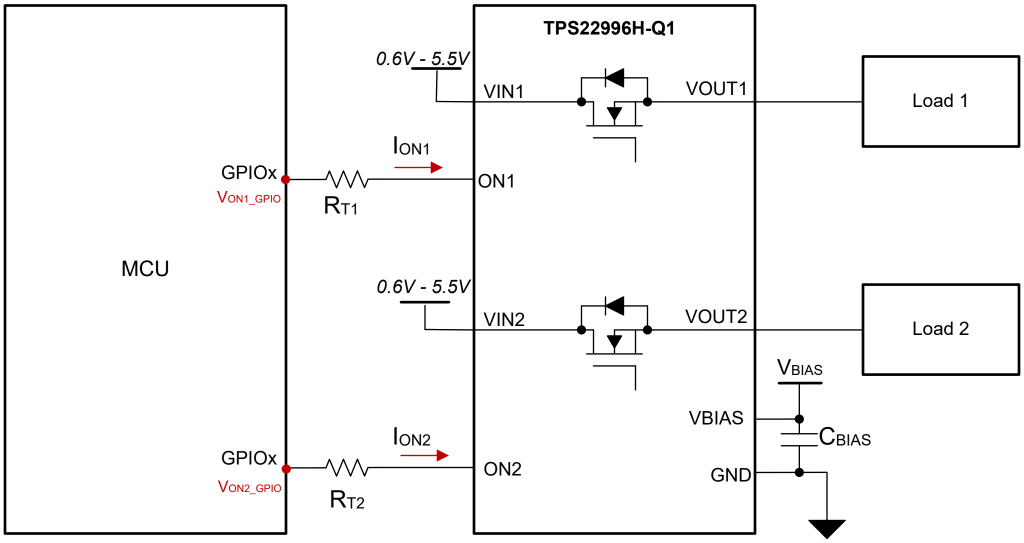


図 7-1. TPS22996H-Q1 Adjustable Rise Time Configuration

7.4 Device Functional Modes

表 7-3 lists the TPS22996H-Q1 functions.

表 7-3. TPS22996H-Q1 Functions Table

ON	VIN to VOUT	VOUT
L	Off	GND
H	On	VIN

8 Application and Implementation

注

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8.1 Application Information

This section highlights some of the design considerations for implementing the device in various applications.

8.2 Typical Application

This application demonstrates how the TPS22996H-Q1 can be used to limit the inrush current when powering on downstream modules.

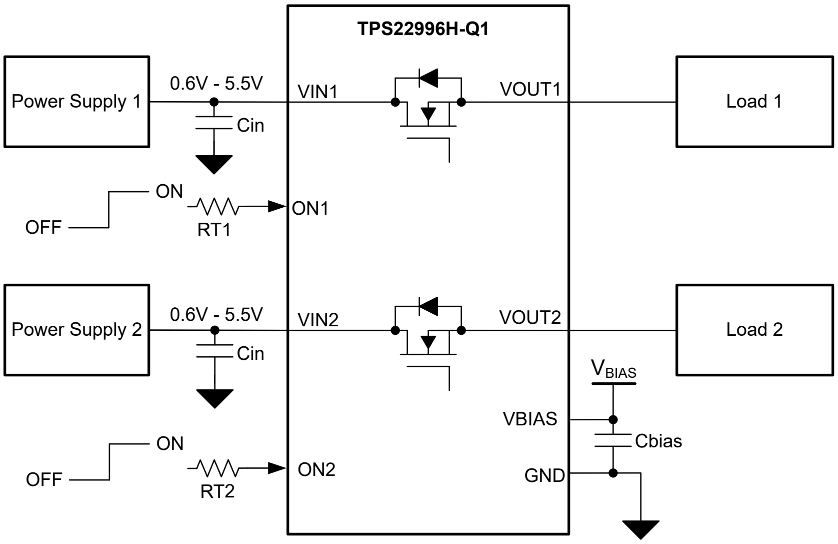

図 8-1. Typical Application Circuit

表 8-1. Component Descriptions

DESIGN PARAMETER	TYPICAL VALUES	DESCRIPTION
C_{IN}	1µF	Filtering voltage transients
C_{OUT}	100nF	Filtering voltage transients
C_{BIAS}	0.1µF	Filtering voltage transients
RT1, RT2	10kΩ	Series resistor for rise time control

8.2.1 Design Requirements

表 8-2 shows the TPS22996H-Q1 design parameters.

表 8-2. Design Parameters

DESIGN PARAMETER	VALUE
V_{BIAS}	5V
V_{IN}	5V
Rise Time	1000μs

8.2.2 Detailed Design Procedure

The design in this example is trying to achieve 1000µs rise time for power sequencing, with both V_{BIAS} and V_{IN} to be 5V. From 表 7-1, the I_{ON} needs to be between 20µA and 100µA. To find the I_{ON} needed to achieve 1000µs rise time, linear interpolation can be used to estimate as below:

$$T_R = (T_{R2} - T_{R1}) / (I_{ON2} - I_{ON1}) * (I_{ON} - I_{ON1}) + T_{R1} \tag{2}$$

where:

- T_R is the desired T_R, which is 1000µs
- I_{ON} is the desired I_{ON}
- T_{R1} is the first T_R used for linear interpolation, which is 2350µs
- T_{R2} is the second T_R used for linear interpolation, which is 626µs
- I_{ON1} is the first I_{ON} used for linear interpolation, which is 20µA
- I_{ON2} is the second I_{ON} used for linear interpolation, which is 100µA

I_{ON} is calculated to be 82.6µA. To find the R_T value, plug in the parameters in 式 1.

$R_T = 1000 \times (5V - 1.2V) / 82.6\mu A - 12.5k\Omega = 33.5k\Omega$

By using the standard resistor value closest to 33.5kΩ, the typical rise time can be calculated for the actual resistor value used on board.

8.3 Power Supply Recommendations

The device is designed to operate from a V_{BIAS} range of 2.5V to 5.5V and a V_{IN} range of 0.6V to V_{BIAS}.

8.4 Layout

8.4.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for V_{IN}, V_{OUT}, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

8.4.2 Layout Example

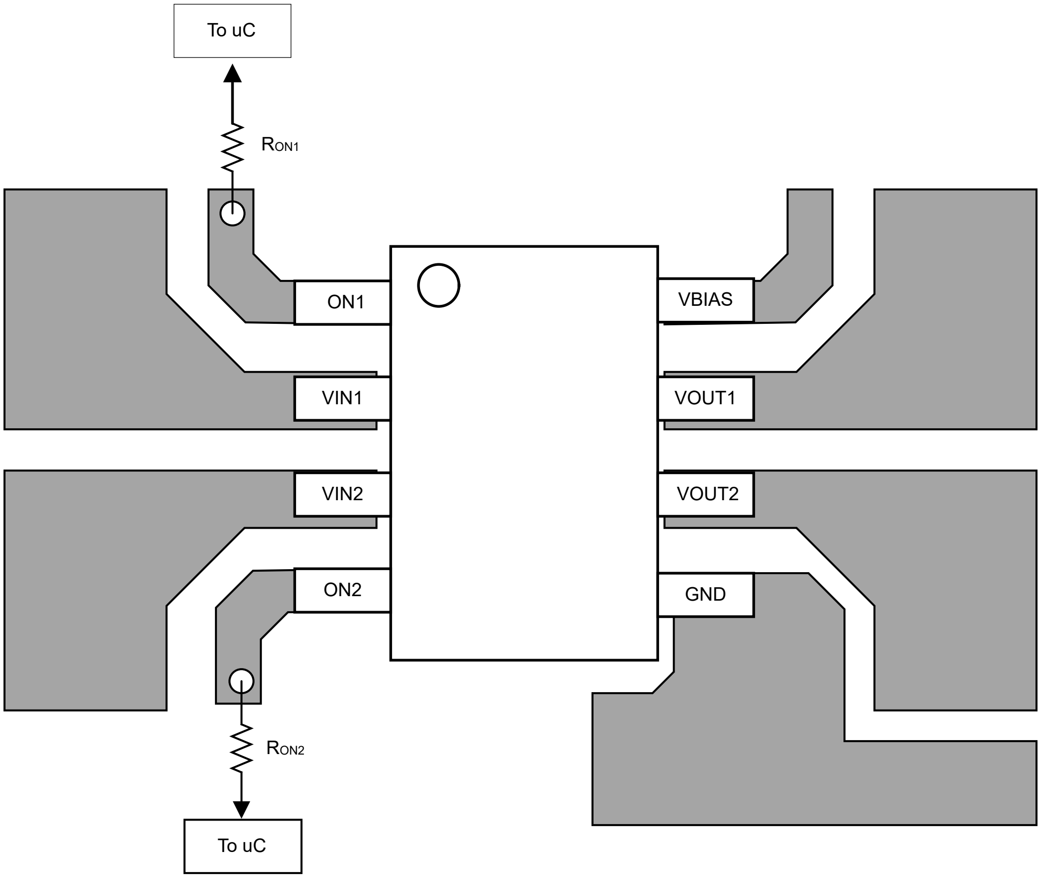

図 8-2. TPS22996H Layout Example

8.4.3 Power Dissipation

The maximum IC junction temperature must be restricted to 150°C under normal operating conditions. To calculate the maximum allowable power dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use 式 3.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \tag{3}$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation.

- $T_{J(max)}$ is the maximum allowable junction temperature (150°C for the TPS22996H).
- T_A is the ambient temperature of the device.
- θ_{JA} is the junction to air thermal impedance. See セクション 5.4. This parameter is highly dependent upon board layout.

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.5 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (March 2024) to Revision A (October 2024) **Page**

- ドキュメントのステータスを「事前情報」から*「量産データ」*... 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

重要なお知らせと免責事項

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22996HQDYCRQ1	ACTIVE	SOT-5X3	DYC	8	4000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	996HQ	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
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[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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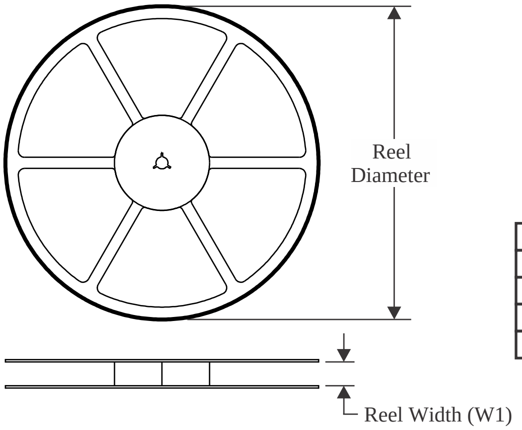
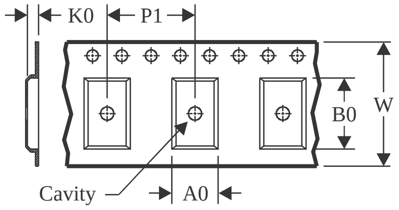
TAPE AND REEL INFORMATION

REEL DIMENSIONS

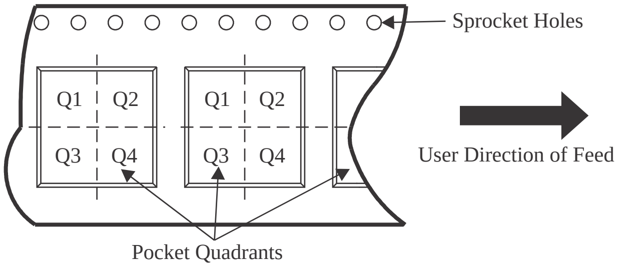


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

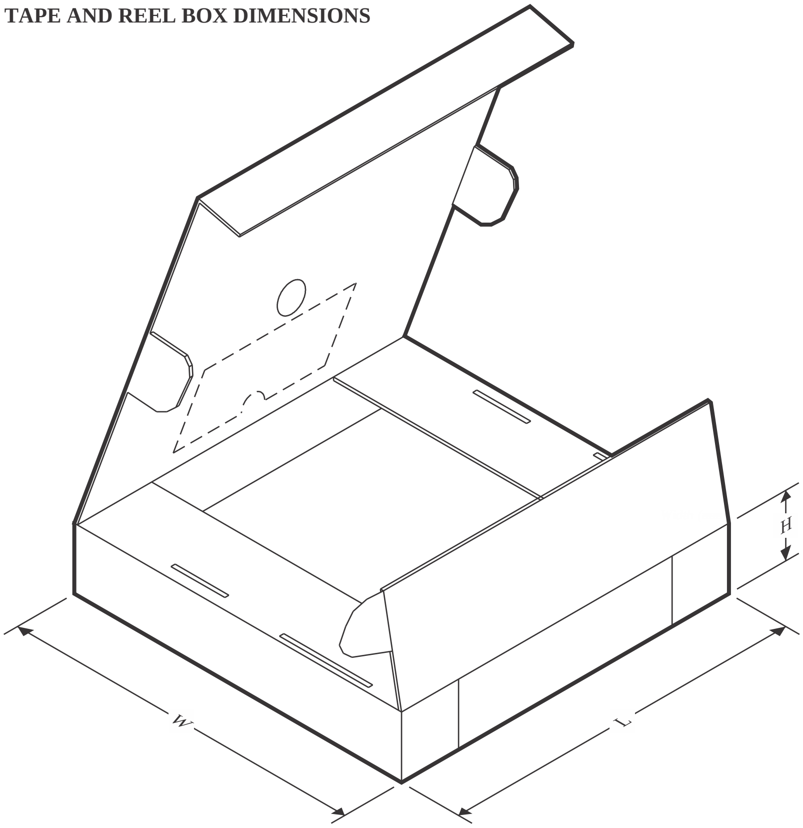
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

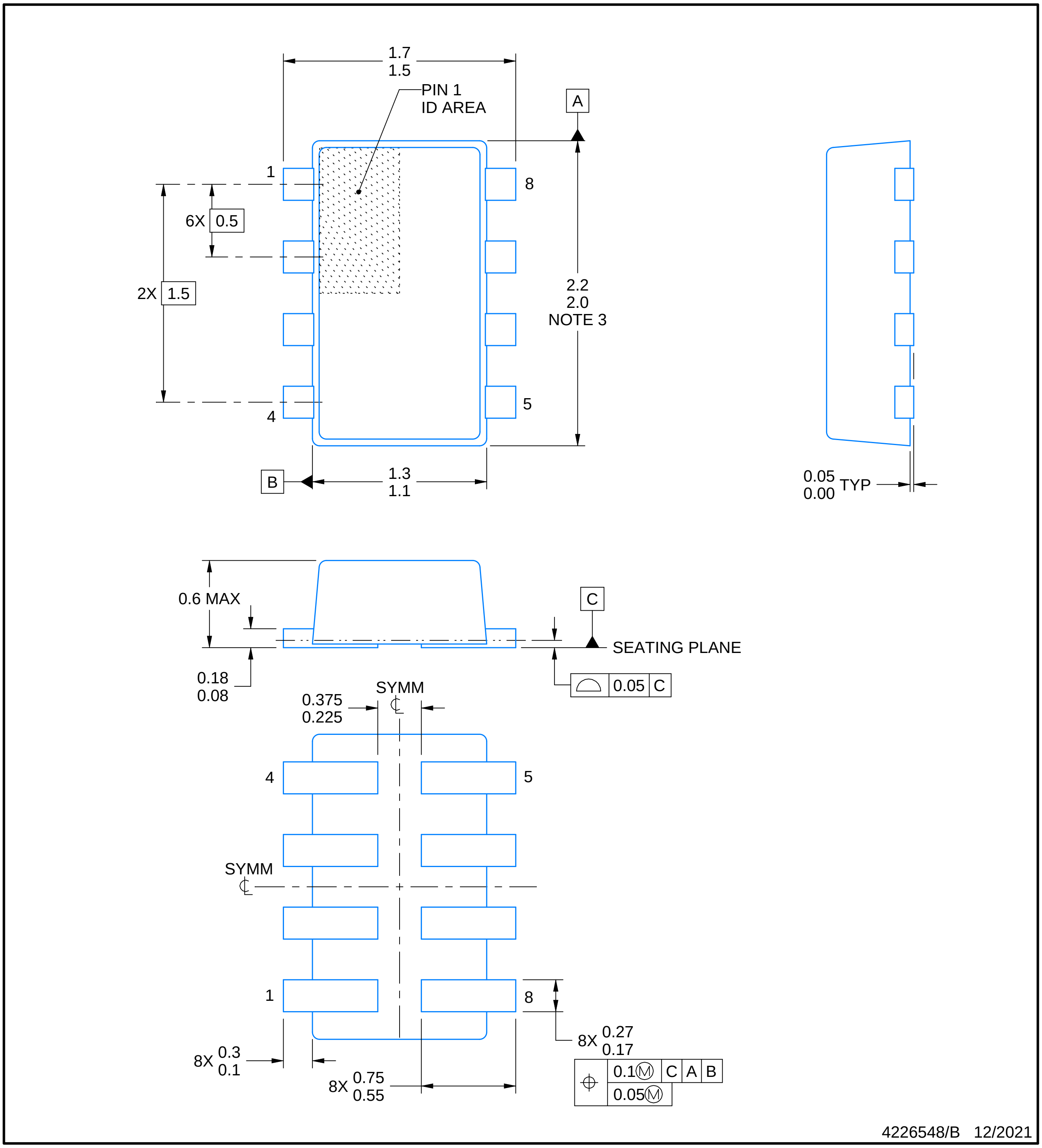
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22996HQDYCRQ1	SOT-5X3	DYC	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



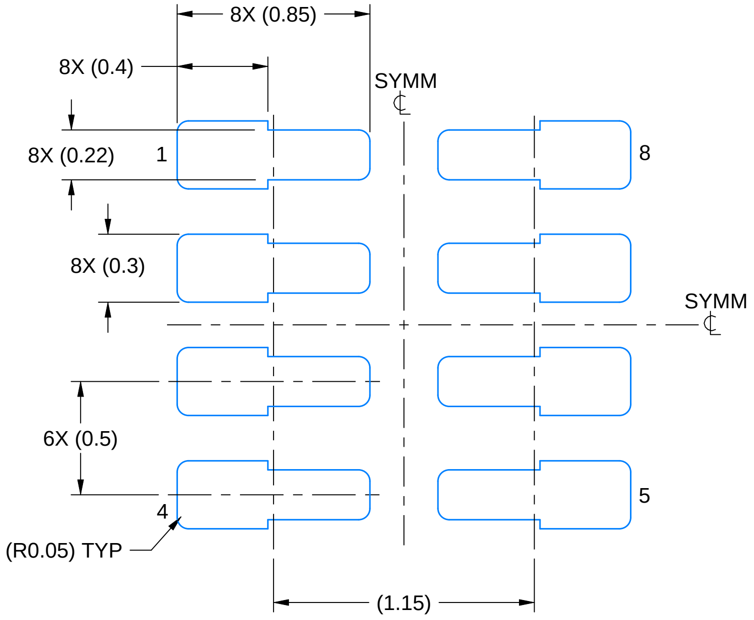
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22996HQDYCRQ1	SOT-5X3	DYC	8	4000	210.0	185.0	35.0

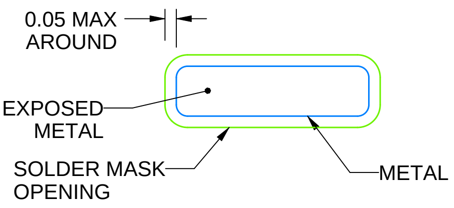


NOTES:

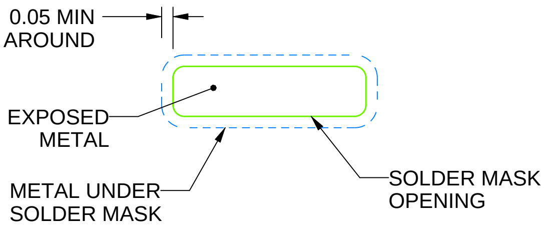
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)



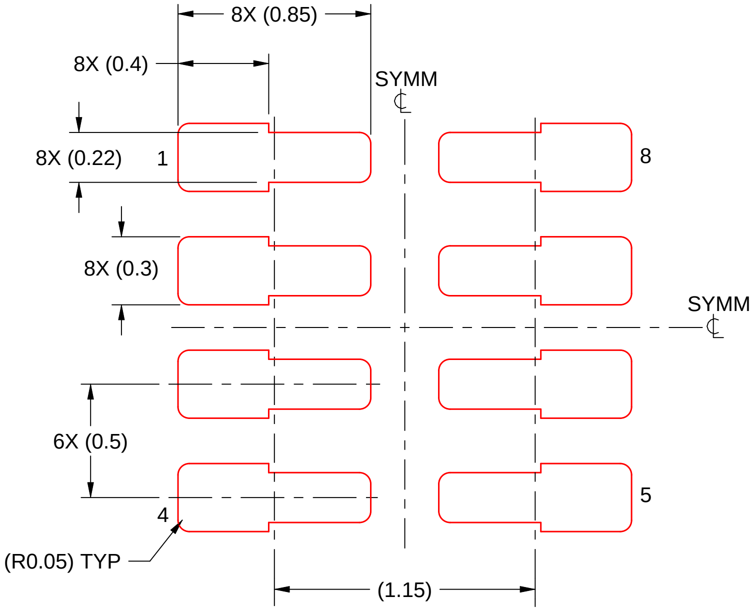
SOLDER MASK
DEFINED

SOLDERMASK DETAILS

4226548/B 12/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

NOTES: (continued)

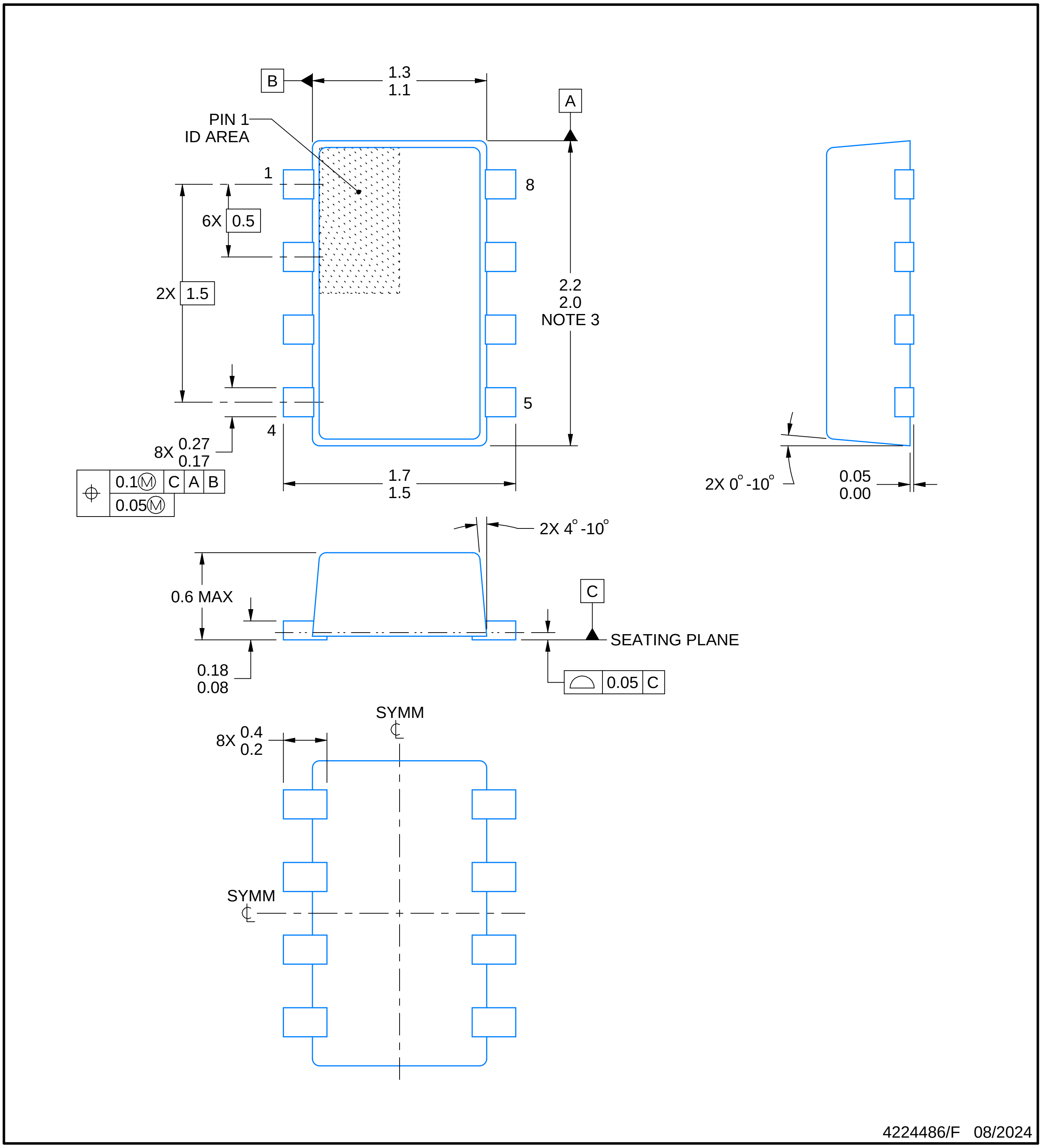
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



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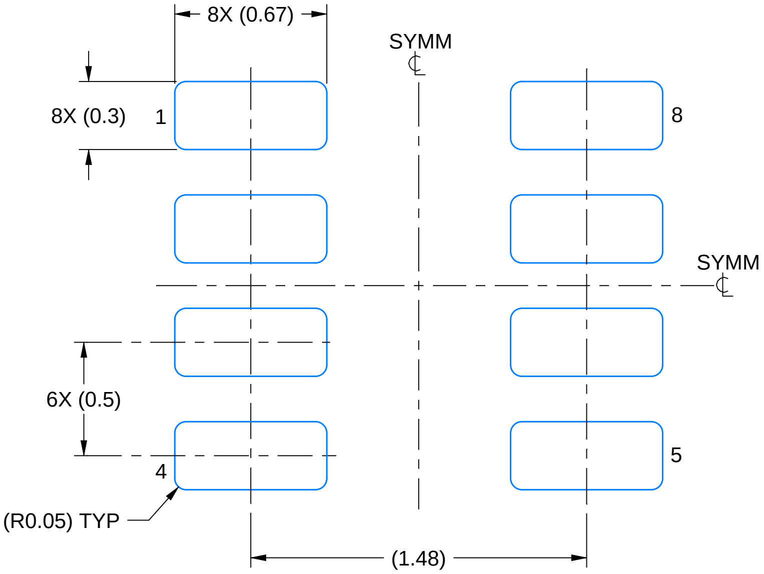
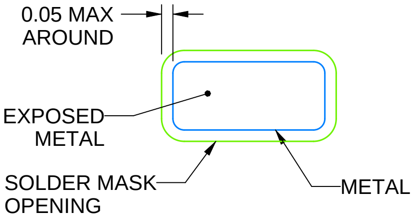
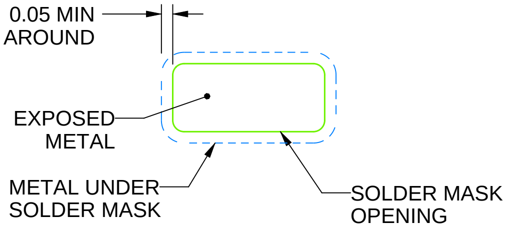
4. Reference JEDEC Registration MO-293, Variation UDAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDERMASK DETAILS

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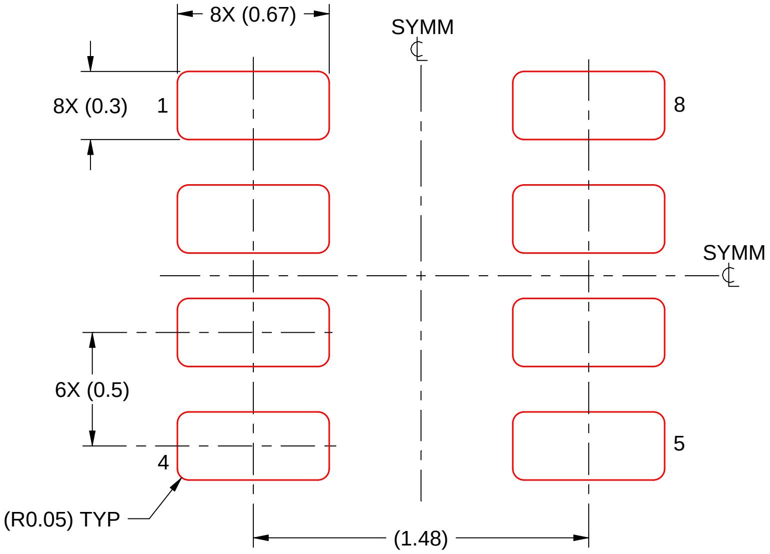
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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