

# TPS22996 5.5V、4A、14mΩ オン抵抗デュアルチャネル負荷スイッチ

## 1 特長

- 統合型デュアルチャネル負荷スイッチ
- $V_{IN}$  電圧範囲: 0.6V ~  $V_{BIAS}$
- $V_{BIAS}$  電圧範囲: 2.5V ~ 5.5V
- オン抵抗: 14mΩ (標準値)
- チャンネルごとに 4A の最大連続スイッチング電流
- 静止電流:
  - $I_Q = 16\mu A$  (標準値、両チャンネル) ( $V_{IN} = V_{BIAS} = 5V$ )
  - $I_Q = 13\mu A$  (標準値、単一チャンネル) ( $V_{IN} = V_{BIAS} = 5V$ )
- 制御入力スレッショルドにより、1.2、1.8、2.5、3.3V ロジックを使用可能
- 立ち上がり時間を設定可能
- サーマルシャットダウン
- クイック出力放電 (QOD) (オプション)

## 2 アプリケーション

- PC とノート PC
- セットトップボックス、住居用ゲートウェイ
- テレコムシステム
- SSD (ソリッドステートドライブ)

## 3 概要

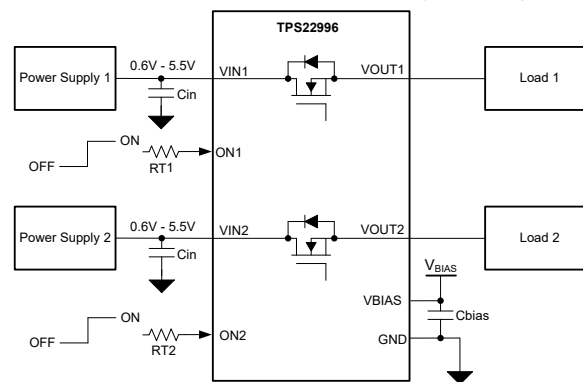
TPS22996 製品ファミリーは 2 つのデバイス (TPS22996、TPS22996N) で構成されています。各デバイスは、ターンオン制御付きのデュアルチャネル負荷スイッチです。入力電圧範囲 0.6V ~ 5.5V で動作する 2 つの N チャネル MOSFET を備えており、各チャンネル最大 4A の連続電流をサポートできます。各スイッチは、低電圧制御信号と直接インターフェイス可能なオン入力とオフ入力 (ON1 および ON2) により独立して制御されます。TPS22996 は接合部温度がしきい値を超えたときにサーマルシャットダウンでスイッチを切断できます。接合部温度が安全範囲で安定化すると、スイッチが再びオンになります。TPS22996 はオプションで、スイッチがオフのときにクイック出力放電を行えるよう、230Ω のオンチップ負荷抵抗を内蔵できます。

TPS22996 は、リード付きの小型で省スペースの 2.1mm × 1.6mm 8 DRL パッケージで供給されるため、低コストの製造が可能です。周囲温度  $-40^{\circ}C \sim 105^{\circ}C$  での動作が規定されています。

### パッケージ情報

部品番号	パッケージ (1)	パッケージサイズ (2)
TPS22996	DRL (SOT, 8)	2.10mm × 1.60mm

- 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- パッケージサイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーション回路



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## 4 Device Comparison Table

DEVICE	$R_{ON}$ AT $V_{IN} = V_{BIAS} = 5\text{ V}$ (TYPICAL)	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT
TPS22996	14 m $\Omega$	Yes	4 A
TPS22996N <sup>(1)</sup>	14 m $\Omega$	No	4 A

(1) Device in preview status. Please contact TI for more information.

## 5 Pin Configuration and Functions

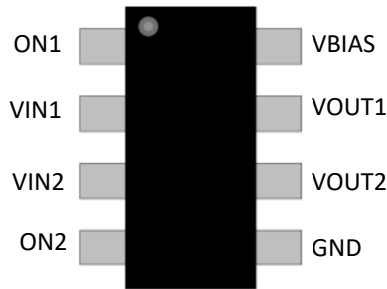


図 5-1. DRL Package, 8-Pin SOT (Top View)

### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ON1	I	Active-high switch 1 control input. Connect series resistor to set slew rate. Do not leave floating.
2	VIN1	I	Switch 1 input. Recommended voltage range for these pins for optimal $R_{ON}$ performance is 0.6 V to $V_{BIAS}$ . Place an optional decoupling capacitor between these pins and GND to reduce $V_{IN1}$ dip during turnon of the channel.
3	VIN2	I	Switch 2 input. Recommended voltage range for these pins for optimal $R_{ON}$ performance is 0.6 V to $V_{BIAS}$ . Place an optional decoupling capacitor between these pins and GND to reduce $V_{IN1}$ dip during turnon of the channel.
4	ON2	I	Active-high switch 2 control input. Connect series resistor to set Slew Rate. Do not leave floating.
5	GND	I	Device ground.
6	VOUT2	I	Switch 2 output.
7	VOUT1	I	Switch 1 output.
8	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.5 V.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{IN1,2}$	Input voltage	-0.3	6	V
$V_{OUT1,2}$	Output voltage	-0.3	6	V
$V_{ON1,2}$	ON pin voltage	-0.3	6	V
$V_{BIAS}$	Bias voltage	-0.3	6	V
$I_{MAX}$	Maximum continuous current per channel		4	A
$I_{MAX,PLS}$	Maximum pulsed current switch per channel, pulse <300 $\mu$ s, 3% duty cycle		5.5	A
$T_J$	Junction temperature		125	°C
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins <sup>(1)</sup>	$\pm 2000$	V
		Charged device model (CDM), per JEDEC specification JS-002, all pins <sup>(2)</sup>	$\pm 1000$	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{IN1,2}$	Input voltage	0.6		$V_{BIAS}$	V
$V_{BIAS}$	Bias voltage	2.5		5.5	V
$V_{ON1,2}$	ON pin voltage	0		5.5	V
$V_{OUT1,2}$	Output voltage	0		$V_{IN}$	V
$V_{IH}$	High-Level input voltage, ON	1.2		5.5	V
$V_{IL}$	Low-Level input voltage, ON	0		0.6	V
$T_A$	Ambient temperature	-40		105	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS22996	UNIT
		DRL (SOT)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.7	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	1	°C/W

## 6.4 Thermal Information (続き)

THERMAL METRIC <sup>(1)</sup>		TPS22996	UNIT
		DRL (SOT)	
		8 PINS	
$\Psi_{JB}$	Junction-to-board characterization parameter	20.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

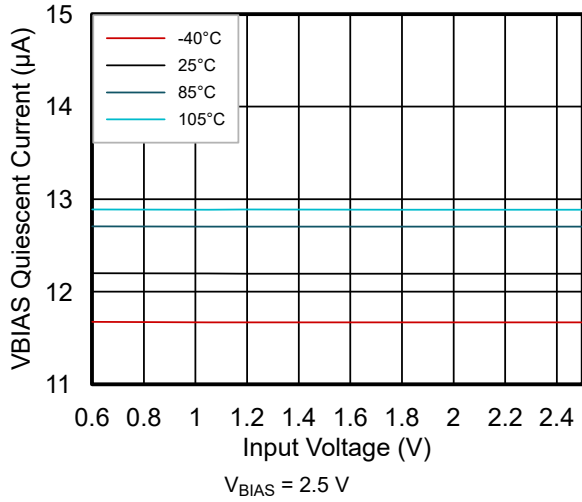
PARAMETER		TEST CONDITIONS	$T_A$	MIN	TYP	MAX	UNIT	
<b>Power Supplies and Currents</b>								
$I_{Q,VBIAS}$	$V_{BIAS}$ quiescent current (both channels)	$I_{OUT1} = I_{OUT2} = 0$ mA, $V_{IN1,2} = V_{ON1,2} = 5$ V	-40°C to 85°C	16	22		μA	
			-40°C to 105°C			23	μA	
	$V_{BIAS}$ quiescent current (single-channel)	$I_{OUT1} = I_{OUT2} = 0$ mA, $V_{ON2} = 0$ V, $V_{IN1,2} = V_{IN1} = 5$ V	-40°C to 85°C	13	20		μA	
			-40°C to 105°C			22	μA	
$I_{SD,VBIAS}$	$V_{BIAS}$ shutdown current	$V_{ON1,2} = 0$ V, $V_{OUT1,2} = 0$ V	-40°C to 105°C	0.1	0.5		μA	
$I_{SD,VIN}$	$V_{IN}$ shutdown current (per channel)	$V_{ON} = 0$ V, $V_{OUT} = 0$ V	$V_{IN} = 5$ V	-40°C to 85°C	0.010	0.5		μA
				-40°C to 105°C			0.8	μA
			$V_{IN} = 3.3$ V	-40°C to 85°C	0.010	0.5		μA
				-40°C to 105°C			0.8	μA
			$V_{IN} = 1.8$ V	-40°C to 85°C	0.010	0.5		μA
				-40°C to 105°C			0.8	μA
			$V_{IN} = 0.6$ V	-40°C to 85°C	0.001	0.3		μA
				-40°C to 105°C			0.8	μA
$I_{ON}$	ON pin leakage current	$V_{ON} = 5.5$ V	-40°C to 105°C			0.1	μA	
<b>Resistance Characteristics</b>								
$R_{ON}$	On-Resistance	$I_{OUT} = -200$ mA	$V_{IN} = 5$ V	25°C	14	18	mΩ	
				-40°C to 85°C			21	mΩ
				-40°C to 105°C			23	mΩ
			$V_{IN} = 3.3$ V	25°C	14	18	mΩ	
				-40°C to 85°C			21	mΩ
				-40°C to 105°C			23	mΩ
			$V_{IN} = 1.8$ V	25°C	14	18	mΩ	
				-40°C to 85°C			21	mΩ
				-40°C to 105°C			23	mΩ
			$V_{IN} = 0.6$ V	25°C	14	18	mΩ	
				-40°C to 85°C			21	mΩ
				-40°C to 105°C			23	mΩ
$R_i$	Internal on pin resistance	$V_{ON} = 5$ V	$V_{ON} = 5$ V	-40°C to 105°C	11.5		kΩ	
$R_{PD}$	Output pulldown resistance	$V_{IN} = V_{OUT} = 5$ V, $V_{ON} = 0$ V		-40°C to 105°C	230	280	Ω	
$T_{SD}$	Thermal shutdown	Junction temperature rising	-	150	175		°C	
$T_{SD,HYS}$	Thermal shutdown hysteresis	Junction temperature falling	-		20		°C	

## 6.6 Switching Characteristics (TPS22996, TPS22996N)

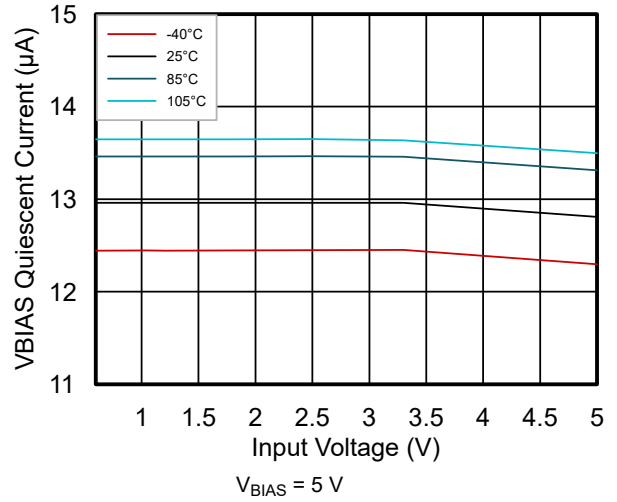
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VIN = VON = VBIAS = 5V</b>						
t <sub>ON</sub>	Turn ON time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		1000		μs
t <sub>OFF</sub>	Turn OFF time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		2.3		μs
t <sub>R</sub>	Rise time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		688		μs
t <sub>F</sub>	Fall time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		2.12		μs
t <sub>D</sub>	Delay time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		317		μs
<b>VIN = 0.6V, VON = VBIAS = 5V</b>						
t <sub>ON</sub>	Turn ON time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		588		μs
t <sub>OFF</sub>	Turn OFF time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		2.3		μs
t <sub>R</sub>	Rise time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		215		μs
t <sub>F</sub>	Fall time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		2.12		μs
t <sub>D</sub>	Delay time	R <sub>L</sub> = 10 Ω, C <sub>L</sub> = 0.1 μF, I <sub>ON</sub> = 100 μA		374		μs

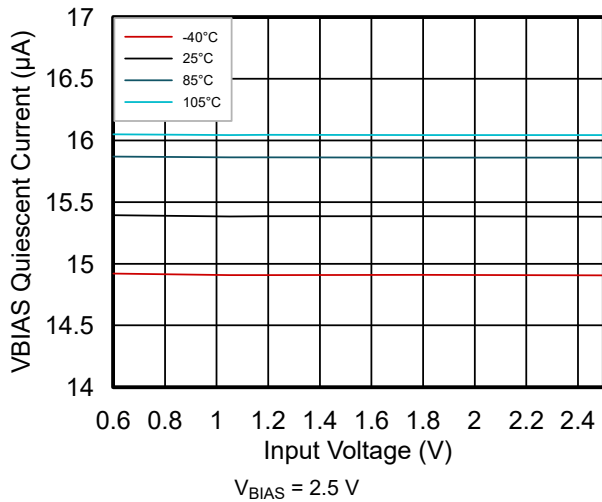
## 6.7 Typical Characteristics: DC



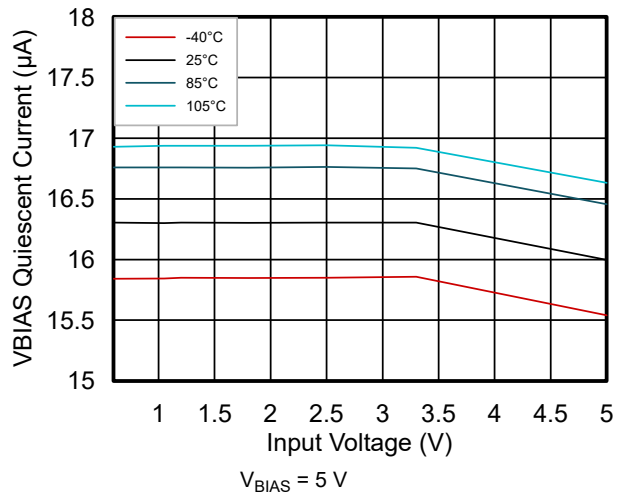
**6-1.  $V_{BIAS}$  Quiescent Current vs Input Voltage Single Channel**



**6-2.  $V_{BIAS}$  Quiescent Current vs Input Voltage Single Channel**



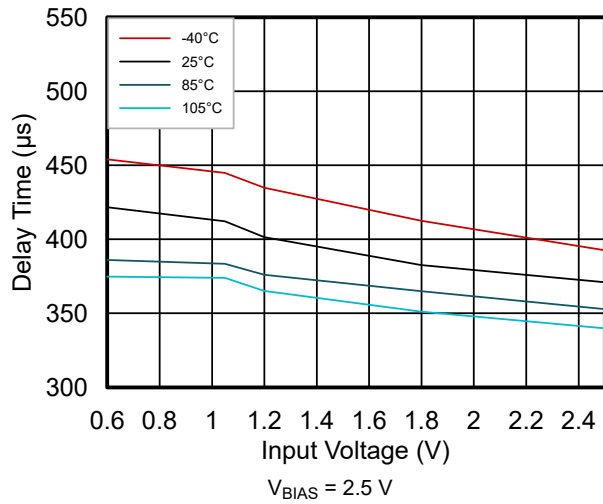
**6-3.  $V_{BIAS}$  Quiescent Current vs Input Voltage Both Channels**



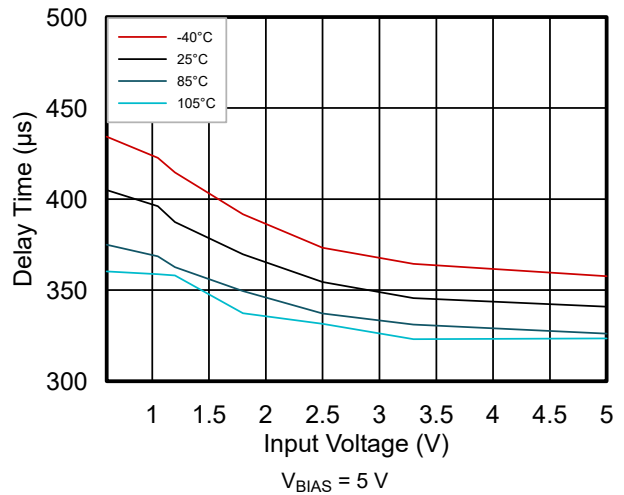
**6-4.  $V_{BIAS}$  Quiescent Current vs Input Voltage Both Channels**

## 6.8 Typical Characteristics: AC

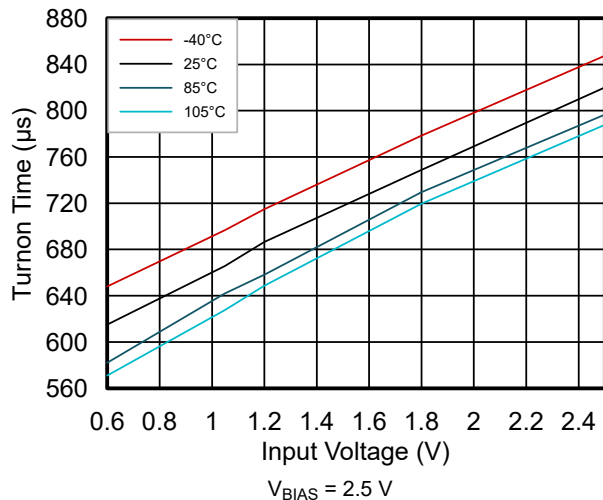
$C_{IN} = 1 \mu\text{F}$ ,  $C_L = 0.1 \mu\text{F}$ ,  $R_L = 10 \Omega$ ,  $V_{ON} = 5 \text{V}$ ,  $I_{ON} = 100 \mu\text{A}$  unless otherwise noticed



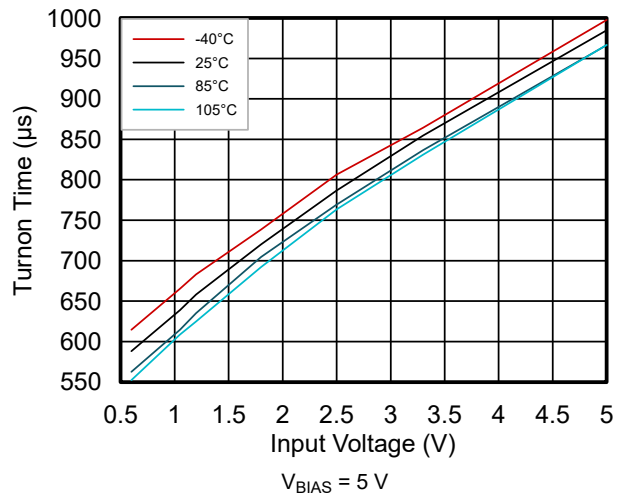
6-5. Delay Time vs Input Voltage



6-6. Delay Time vs Input Voltage



6-7. Turnon Time vs Input Voltage

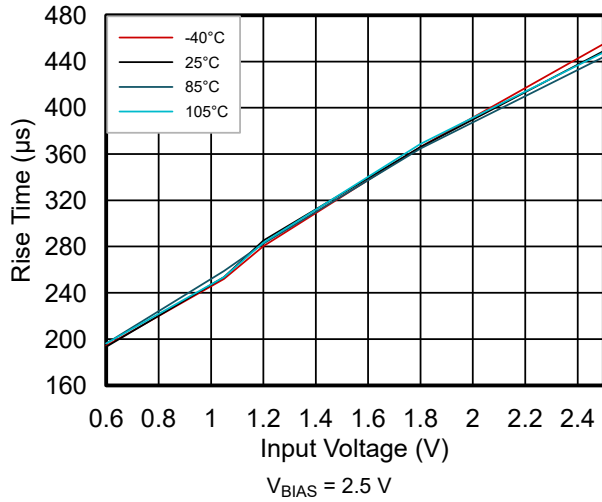


6-8. Turnon Time vs Input Voltage

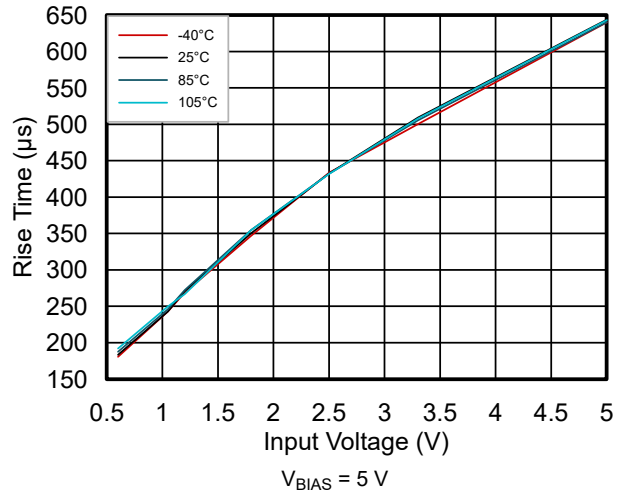


### 6.8 Typical Characteristics: AC (continued)

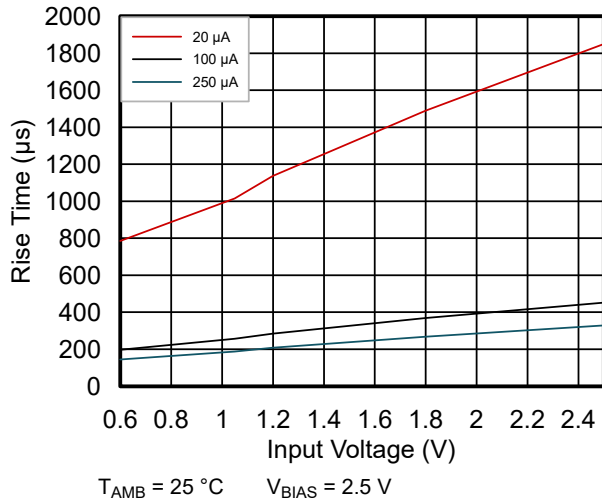
$C_{IN} = 1 \mu\text{F}$ ,  $C_L = 0.1 \mu\text{F}$ ,  $R_L = 10 \Omega$ ,  $V_{ON} = 5 \text{ V}$ ,  $I_{ON} = 100 \mu\text{A}$  unless otherwise noticed



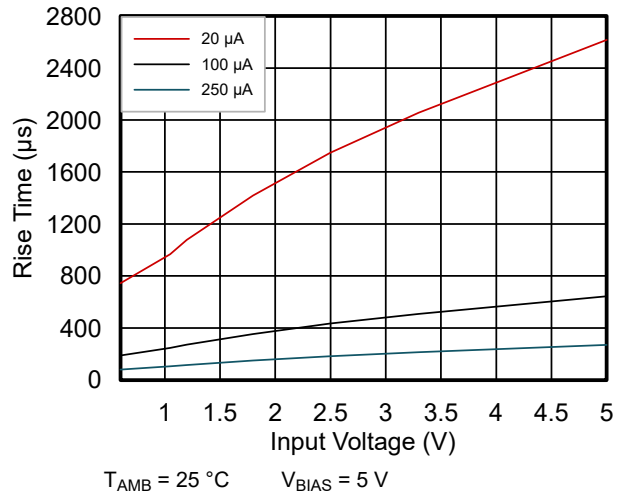
**6-9. Rise Time vs Input Voltage**



**6-10. Rise Time vs Input Voltage**



**6-11. Rise Time vs Input Voltage with Different  $I_{ON}$**



**6-12. Rise Time vs Input Voltage with Different  $I_{ON}$**

### 6.8 Typical Characteristics: AC (continued)

$C_{IN} = 1 \mu\text{F}$ ,  $C_L = 0.1 \mu\text{F}$ ,  $R_L = 10 \Omega$ ,  $V_{ON} = 5 \text{ V}$ ,  $I_{ON} = 100 \mu\text{A}$  unless otherwise noticed

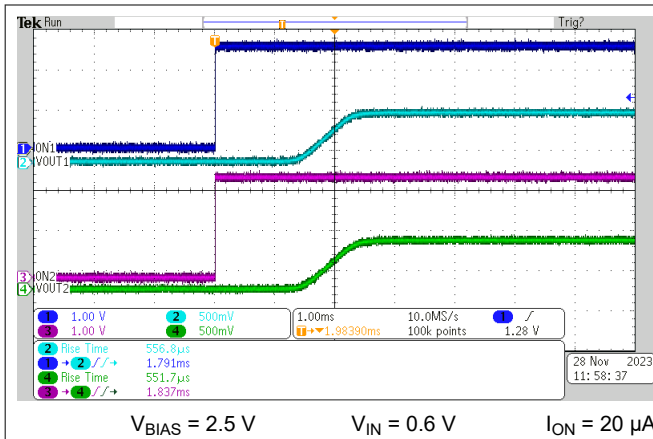


图 6-13. Turnon Response Time

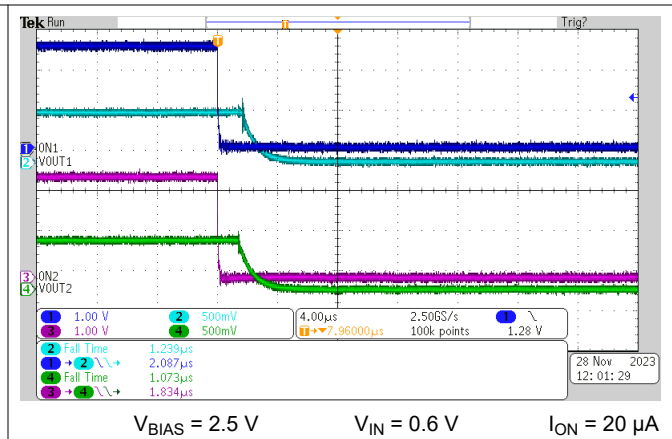


图 6-14. Turnoff Response Time

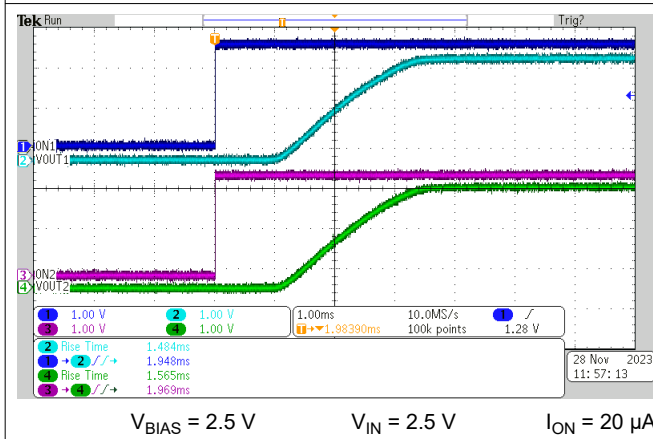


图 6-15. Turnon Response Time

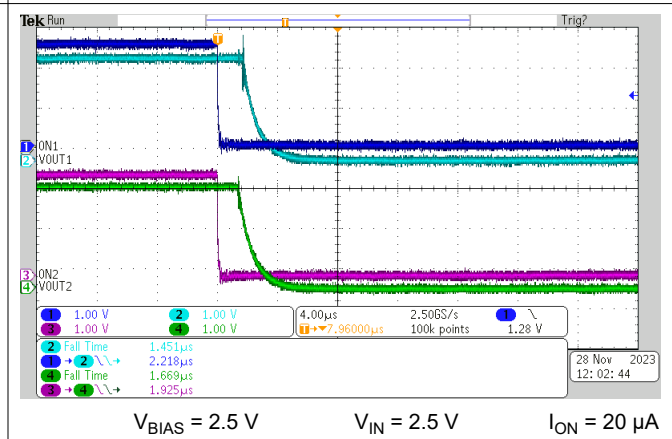


图 6-16. Turnoff Response Time

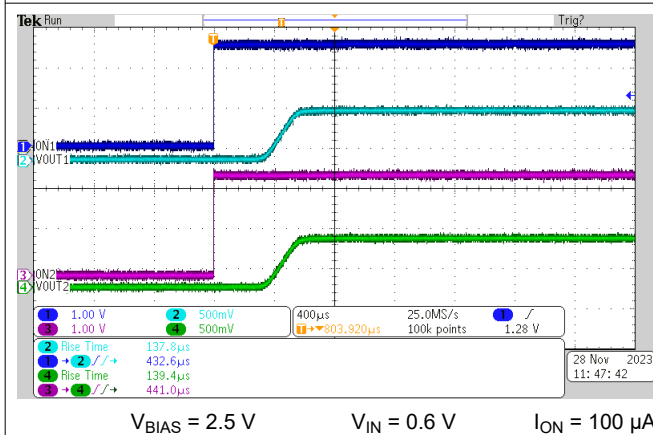


图 6-17. Turnon Response Time

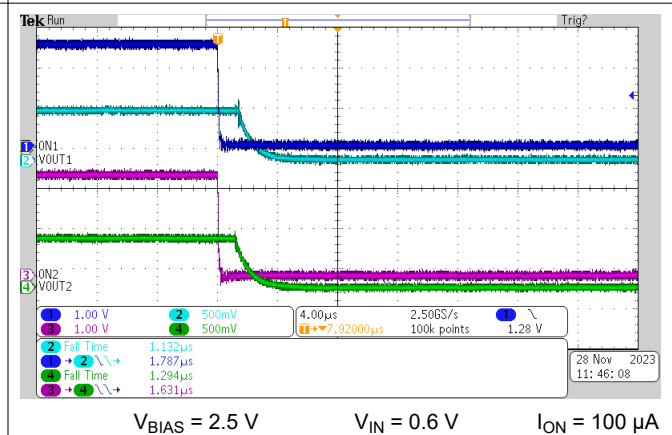
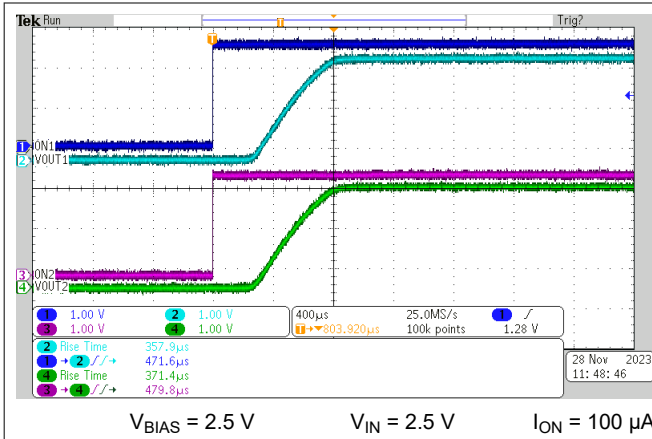


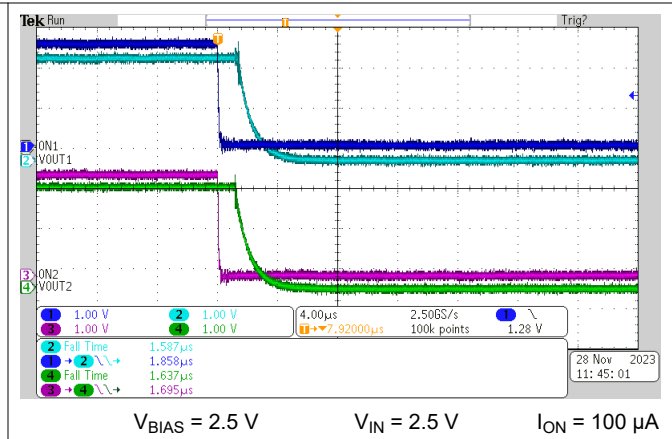
图 6-18. Turnoff Response Time

## 6.8 Typical Characteristics: AC (continued)

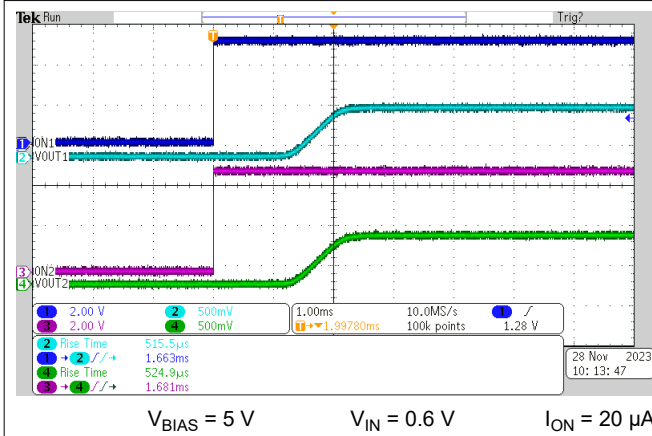
$C_{IN} = 1 \mu\text{F}$ ,  $C_L = 0.1 \mu\text{F}$ ,  $R_L = 10 \Omega$ ,  $V_{ON} = 5 \text{ V}$ ,  $I_{ON} = 100 \mu\text{A}$  unless otherwise noticed



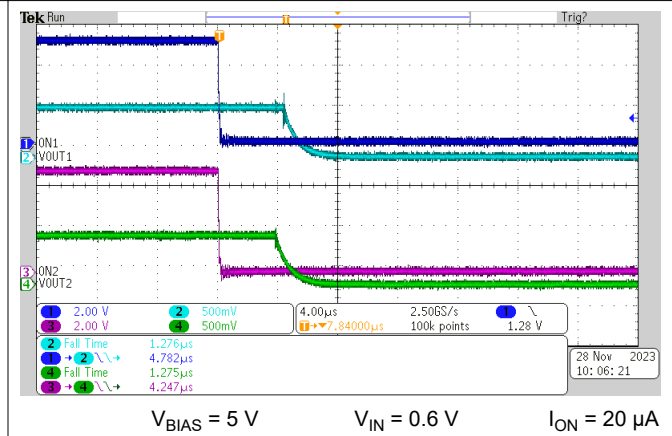
6-19. Turnon Response Time



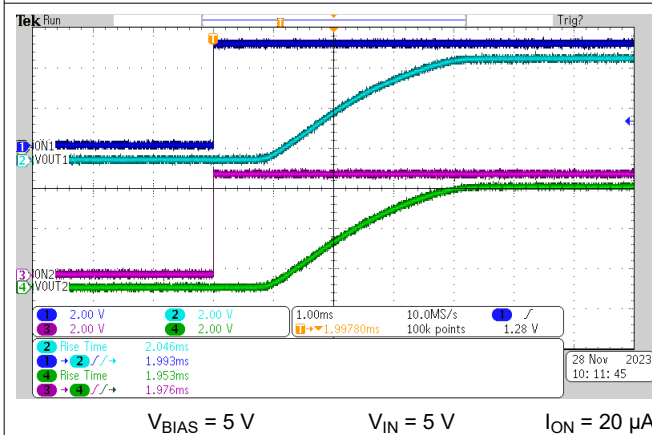
6-20. Turnoff Response Time



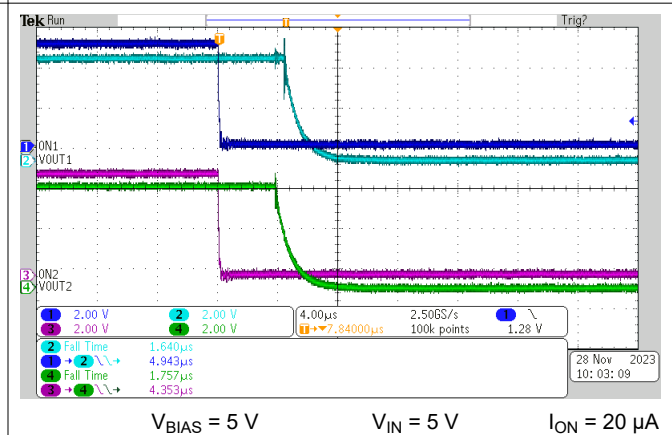
6-21. Turnon Response Time



6-22. Turnoff Response Time



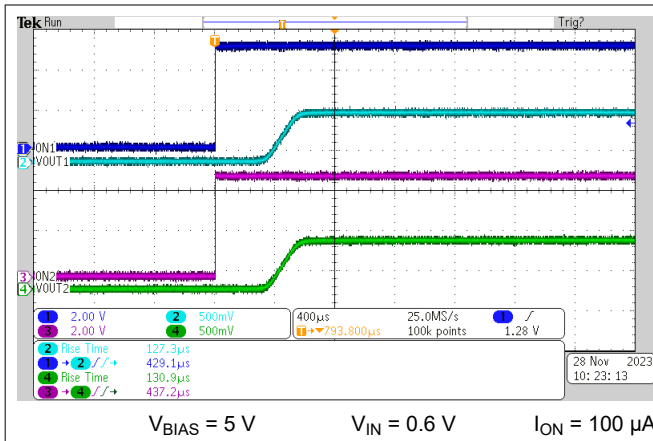
6-23. Turnon Response Time



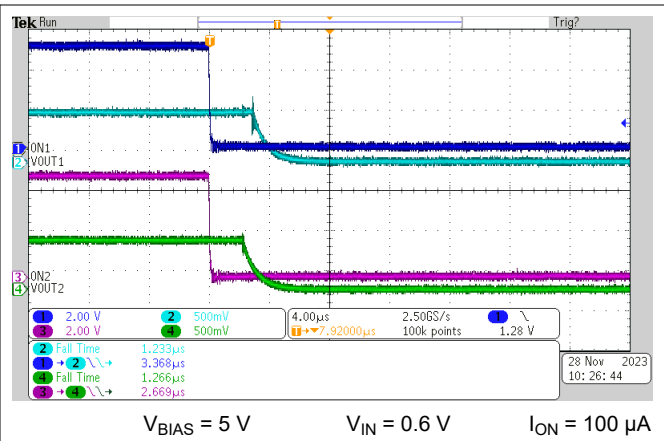
6-24. Turnoff Response Time

### 6.8 Typical Characteristics: AC (continued)

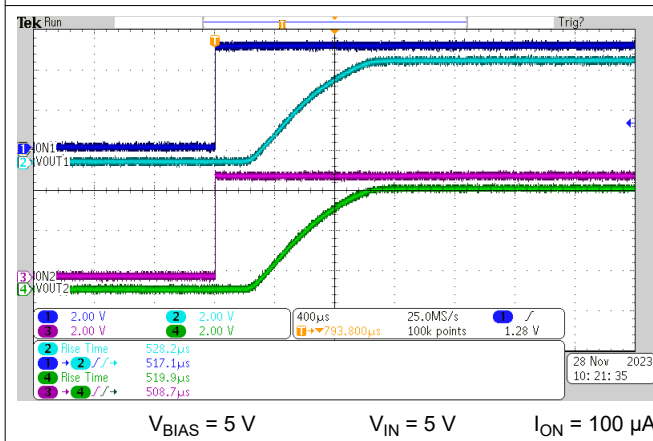
$C_{IN} = 1 \mu\text{F}$ ,  $C_L = 0.1 \mu\text{F}$ ,  $R_L = 10 \Omega$ ,  $V_{ON} = 5 \text{ V}$ ,  $I_{ON} = 100 \mu\text{A}$  unless otherwise noticed



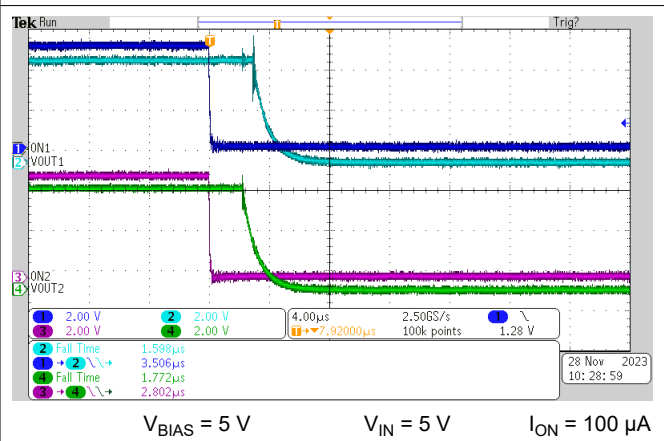
6-25. Turnon Response Time



6-26. Turnoff Response Time



6-27. Turnon Response Time



6-28. Turnoff Response Time

## 7 Parameter Measurement Information

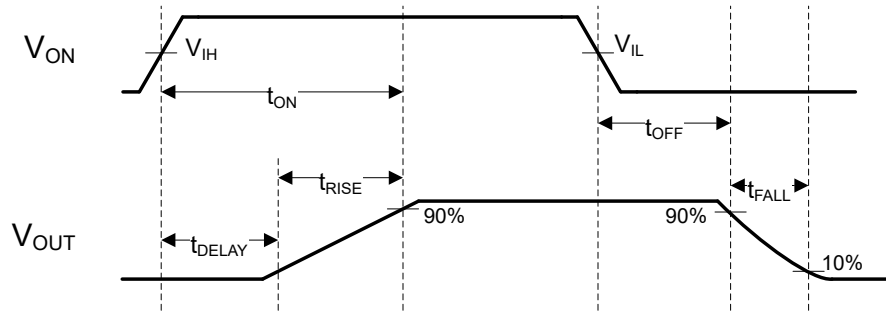


図 7-1.  $t_{ON}$  and  $t_{OFF}$  Waveforms

## 8 Detailed Description

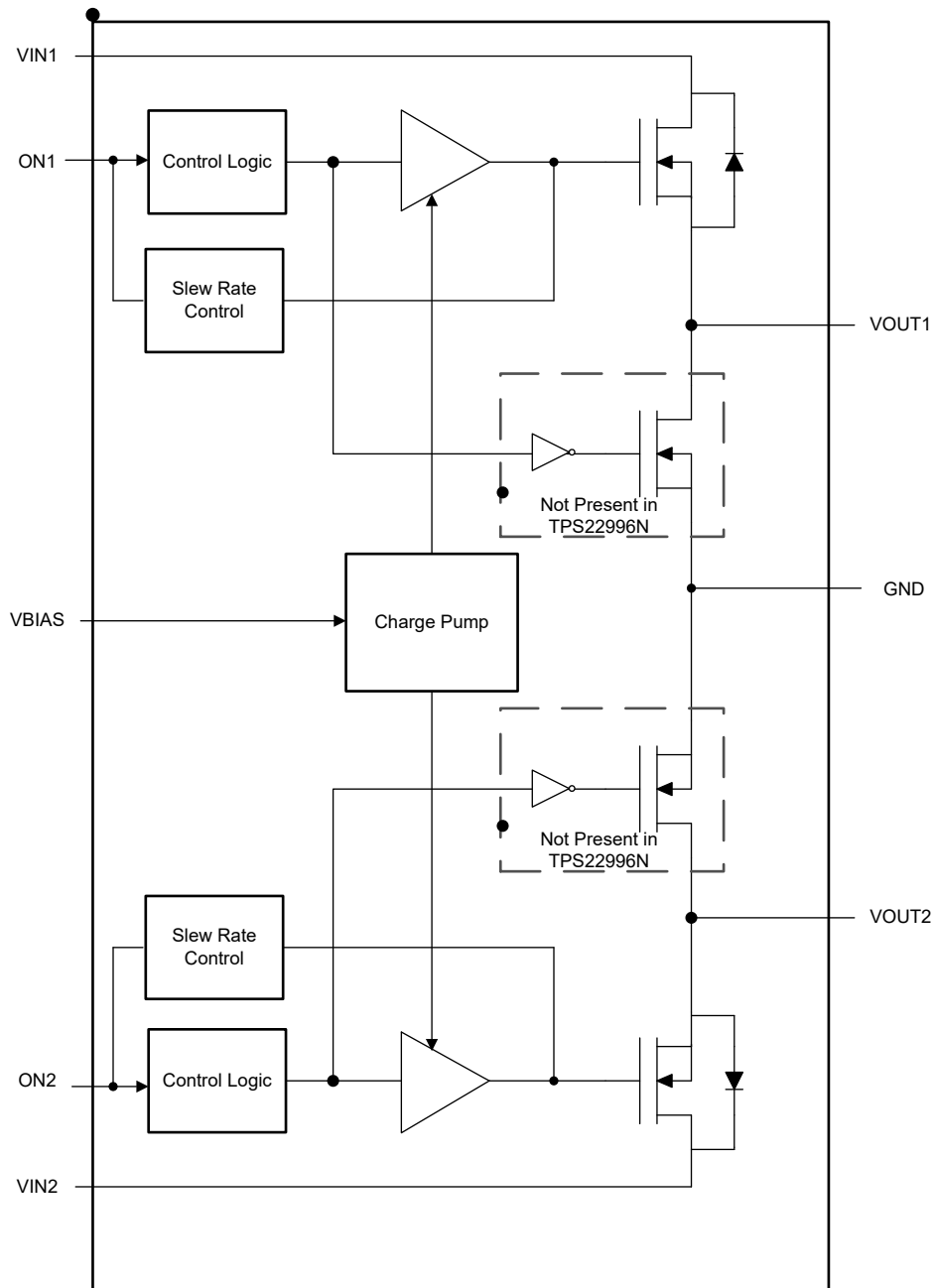
### 8.1 Overview

The TPS22996 is a 5.5-V, dual-channel, 14-m $\Omega$  (typical)  $R_{ON}$  load switch in a 8-pin DRL package. Each channel can support a maximum continuous current of 4 A and is controlled by an on and off GPIO-compatible input. To reduce the voltage drop in high current rails, the device implements N-channel MOSFETs. Note that the ON pins must be connected and cannot be left floating. The device has a configurable slew rate for applications that require specific rise-time, which controls the inrush current. By controlling the inrush current, power supply sag can be reduced during turnon. Furthermore, the slew rate is proportional to the series resistor used on the ONx pin. See [セクション 8.3.6](#) to determine the correct resistor value for a desired rise time.

The internal circuitry is powered by the  $V_{BIAS}$  pin, which supports voltages from 2.5 V to 5.5 V. This circuitry includes the charge pump, QOD (optional), and control logic. When a voltage is applied to  $V_{BIAS}$ , and the ONx pins transition to a low state, the QOD functionality is activated. This connects  $V_{OUTX}$  to ground through the on-chip resistor. The typical pulldown resistance ( $R_{PD}$ ) is 230  $\Omega$ .

During the off state, the device prevents downstream circuits from pulling high standby current from the supply. The integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, reducing solution size and bill of materials (BOM) count.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 ON and OFF Control

The ON pins control the state of the switch and also the rise time of the output. Asserting ON high enables the switch. ON is active high with a low threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic threshold. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be tied either high or low for proper functionality.

### 8.3.2 Input Capacitor (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, a capacitor needs to be placed between VIN and GND. A 1- $\mu$ F ceramic capacitor,

$C_{IN}$ , placed close to the pins is usually sufficient. Higher values of  $C_{IN}$  can be used to further reduce the voltage drop during high-current application. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor to avoid excessive voltage drop.

### 8.3.3 Output Capacitor (Optional)

Due to the integrated body diode in the NMOS switch, a  $C_{IN}$  greater than  $C_L$  is highly recommended. A  $C_L$  greater than  $C_{IN}$  can cause  $V_{OUT}$  to exceed  $V_{IN}$  when the system supply is removed. This could result in current flow through the body diode from  $V_{OUT}$  to  $V_{IN}$ . A  $C_{IN}$  to  $C_L$  ratio of 10 to 1 is recommended for minimizing  $V_{IN}$  dip caused by inrush currents during startup, however a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more  $V_{IN}$  dip upon turnon due to inrush currents. This can be mitigated by increasing the capacitance on the  $R_T$  resistor for a longer rise time (see [セクション 8.3.6](#)).

### 8.3.4 Quick Output Discharge (QOD)

The TPS22996 includes a QOD feature. When the switch  $V_{ONX}$  is disabled, an internal discharge resistance is connected between  $V_{OUTX}$  and GND to remove the remaining charge from the output. This resistance prevents the output from floating while the switch is disabled. For best results, it is recommended that the device gets disabled before  $V_{BIAS}$  falls below the minimum recommended voltage.

### 8.3.5 Thermal Shutdown

Thermal Shutdown protects the part from internally or externally generated excessive temperatures. When the device temperature exceeds  $T_{SD}$ , the switch is turned off. The switch automatically turns on again if the temperature of the die drops below hysteresis.

### 8.3.6 Adjustable Rise Time

TPS22996 integrates a unique architecture for adjusting the rise time. The device senses the current flowing into the ON1 and ON2 ( $I_{ON}$ ) pins and utilizes the information to set the rise time. This allows the user to adjust the rise time by connecting a series resistance that is determined by the ON Pin voltage. Refer to [表 8-1](#) and [表 8-2](#) for reference on setting the resistor.

**表 8-1. Typical Rise Time ( $V_{BIAS} = 5.0\text{ V}$ ,  $R_L = 10\ \Omega$ ,  $C_L = 0.1\ \mu\text{F}$ )**

$I_{ON}$	$V_{IN} = 0.6\text{ V}$	$V_{IN} = 1.8\text{ V}$	$V_{IN} = 2.5\text{ V}$	$V_{IN} = 3.3\text{ V}$	$V_{IN} = 5.0\text{ V}$
20 $\mu\text{A}$	810 $\mu\text{s}$	1434 $\mu\text{s}$	1760 $\mu\text{s}$	1986 $\mu\text{s}$	2580 $\mu\text{s}$
100 $\mu\text{A}$	215 $\mu\text{s}$	364 $\mu\text{s}$	445 $\mu\text{s}$	519 $\mu\text{s}$	688 $\mu\text{s}$
250 $\mu\text{A}$	90 $\mu\text{s}$	151 $\mu\text{s}$	185 $\mu\text{s}$	220 $\mu\text{s}$	291 $\mu\text{s}$

**表 8-2. Typical Rise Time ( $V_{BIAS} = 3.3\text{ V}$ ,  $R_L = 10\ \Omega$ ,  $C_L = 0.1\ \mu\text{F}$ )**

$I_{ON}$	$V_{IN} = 0.6\text{ V}$	$V_{IN} = 1.8\text{ V}$	$V_{IN} = 2.5\text{ V}$	$V_{IN} = 3.3\text{ V}$
20 $\mu\text{A}$	781 $\mu\text{s}$	1489 $\mu\text{s}$	1821 $\mu\text{s}$	2154 $\mu\text{s}$
100 $\mu\text{A}$	200 $\mu\text{s}$	374 $\mu\text{s}$	451 $\mu\text{s}$	536 $\mu\text{s}$
250 $\mu\text{A}$	93 $\mu\text{s}$	175 $\mu\text{s}$	207 $\mu\text{s}$	244 $\mu\text{s}$

The following equation can be used to estimate the series resistance required to meet the desired rise time.

$$R_T = 1000 \times (V_{ON} - 1.2\text{ V}) / I_{ON} - R_i \quad (1)$$

where:

- $R_T$  = Series resistance in  $\text{k}\Omega$ .
- $R_i$  = Internal On Pin resistance in  $\text{k}\Omega$ .
- $V_{ON}$  = ON pin voltage in V.
- $I_{ON}$  = Current flowing into the ON pin in  $\mu\text{A}$ .



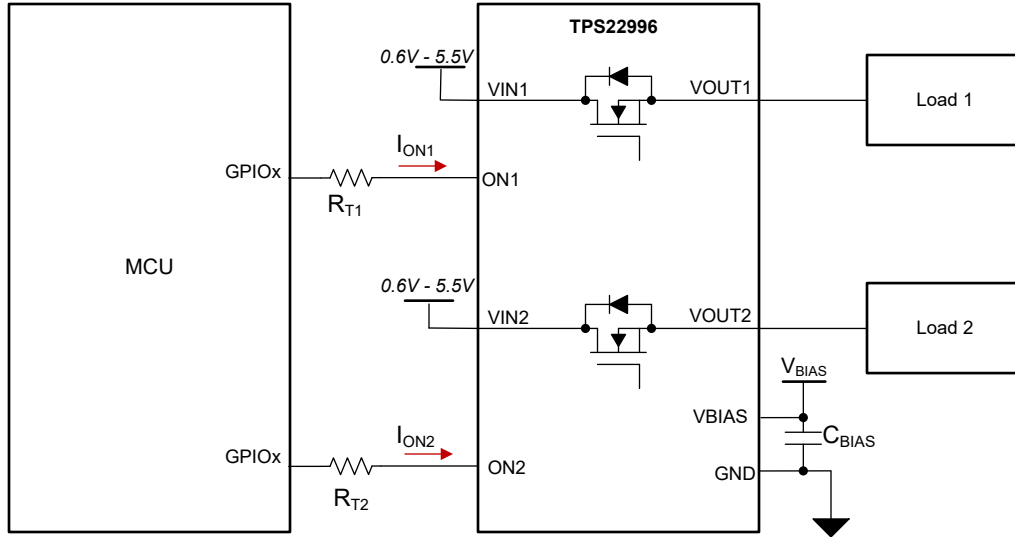


図 8-1. TPS22996 Adjustable Rise Time Configuration

## 8.4 Device Functional Modes

表 8-3 lists the TPS22996 functions.

表 8-3. TPS22996 Functions Table

ON	VIN to VOUT	VOUT
L	Off	GND
H	On	VIN

表 8-4 lists the TPS22996N functions.

表 8-4. TPS22996N Functions Table

ON	VIN to VOUT	VOUT
L	Off	Floating
H	On	VIN

## 9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

This section highlights some of the design considerations for implementing the device in various applications.

### 9.2 Typical Application

This application demonstrates how the TPS22996 can be used to limit the inrush current when powering on downstream modules.

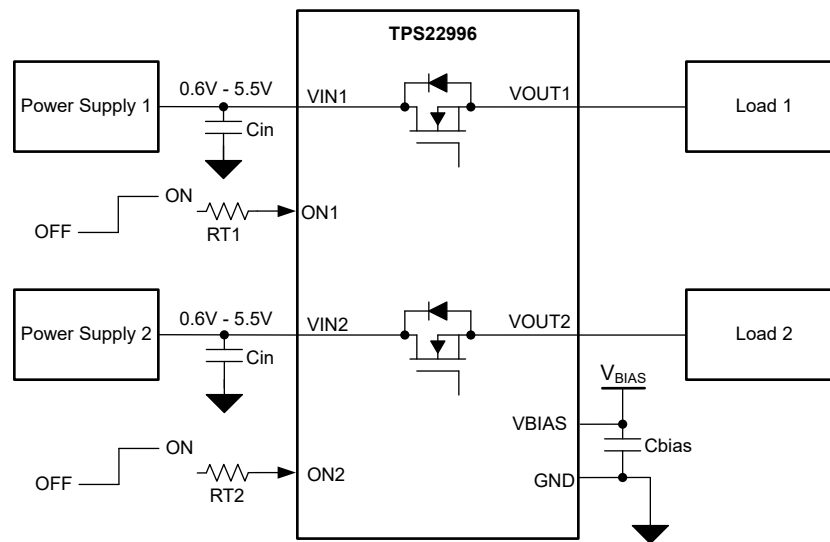


図 9-1. Typical Application Circuit

表 9-1. Component Descriptions

DESIGN PARAMETER	TYPICAL VALUES	DESCRIPTION
$C_{IN}$	1 $\mu$ F	Filtering voltage transients
$C_{OUT}$	100 nF	Filtering voltage transients
$C_{BIAS}$	0.1 $\mu$ F	Filtering voltage transients and noises
RT1, RT2	10 k $\Omega$	Series resistor for rise time control

#### 9.2.1 Design Requirements

For this example, the values below are used as the design parameters.

表 9-2. Design Parameters

PARAMETER	VALUE
$V_{BIAS}$	5 V
$V_{IN}$	5 V
Rise Time	1000 $\mu$ s

### 9.2.2 Detailed Design Procedure

The design in this example is trying to achieve 1000 μs rise time for power sequencing, with both  $V_{BIAS}$  and  $V_{IN}$  to be 5 V. From 表 8-1, the  $I_{ON}$  needs to be between 20 μA and 100 μA. To find the  $I_{ON}$  needed to achieve 1000 μs rise time, linear interpolation can be used to estimate as below:

$$T_R = (T_{R2} - T_{R1}) / (I_{ON2} - I_{ON1}) * (I_{ON} - I_{ON1}) + T_{R1} \quad (2)$$

where:

- $T_R$  is the desired  $T_R$ , which is 1000 μs
- $I_{ON}$  is the desired  $I_{ON}$
- $T_{R1}$  is the first  $T_R$  used for linear interpolation, which is 2580 μs
- $T_{R2}$  is the second  $T_R$  used for linear interpolation, which is 688 μs
- $I_{ON1}$  is the first  $I_{ON}$  used for linear interpolation, which is 20 μA
- $I_{ON2}$  is the second  $I_{ON}$  used for linear interpolation, which is 100 μA

$I_{ON}$  is calculated to be 86.8 μA. To find the  $R_T$  value, plug in the parameters in 式 1.

$$R_T = 1000 \times (5 \text{ V} - 1.2 \text{ V}) / 86.8 \text{ μA} - 11.5 \text{ k}\Omega = 32.2 \text{ k}\Omega$$

By using the standard resistor value closest to 32.2 kΩ, the typical rise time can be calculated for the actual resistor value used on board.

## 9.3 Power Supply Recommendations

The device is designed to operate from a  $V_{BIAS}$  range of 2.5 V to 5.7 V and a  $V_{IN}$  range of 0.6 V to  $V_{BIAS}$ .

## 9.4 Layout

### 9.4.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for  $V_{IN}$ ,  $V_{OUT}$ , and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

### 9.4.2 Layout Example

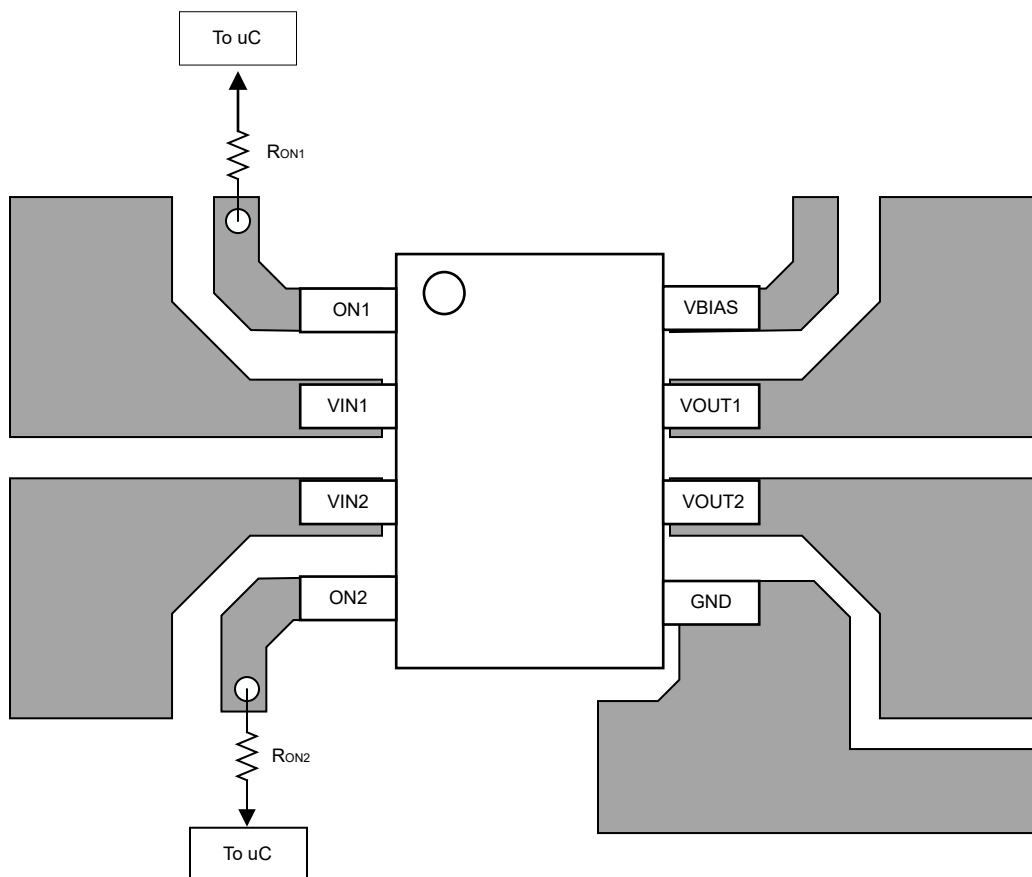


图 9-2. TPS22996 Layout Example

### 9.4.3 Power Dissipation

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable power dissipation,  $P_{D(max)}$  for a given output current and ambient temperature, use 式 3.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (3)$$

where

- $P_{D(max)}$  is the maximum allowable power dissipation.

- $T_{J(max)}$  is the maximum allowable junction temperature (125°C for the TPS22996).
- $T_A$  is the ambient temperature of the device.
- $\theta_{JA}$  is the junction to air thermal impedance. See the [Thermal Information](#) section. This parameter is highly dependent upon board layout.

## 10 Device and Documentation Support

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[www.tij.co.jp](http://www.tij.co.jp) のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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### 10.6 用語集

#### テキサス・インスツルメンツ用語集

この用語集には、用語や略語の一覧および定義が記載されています。

## 11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2023	*	Initial Release

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22996DRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI   SN	Level-1-260C-UNLIM	-40 to 105	22996	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

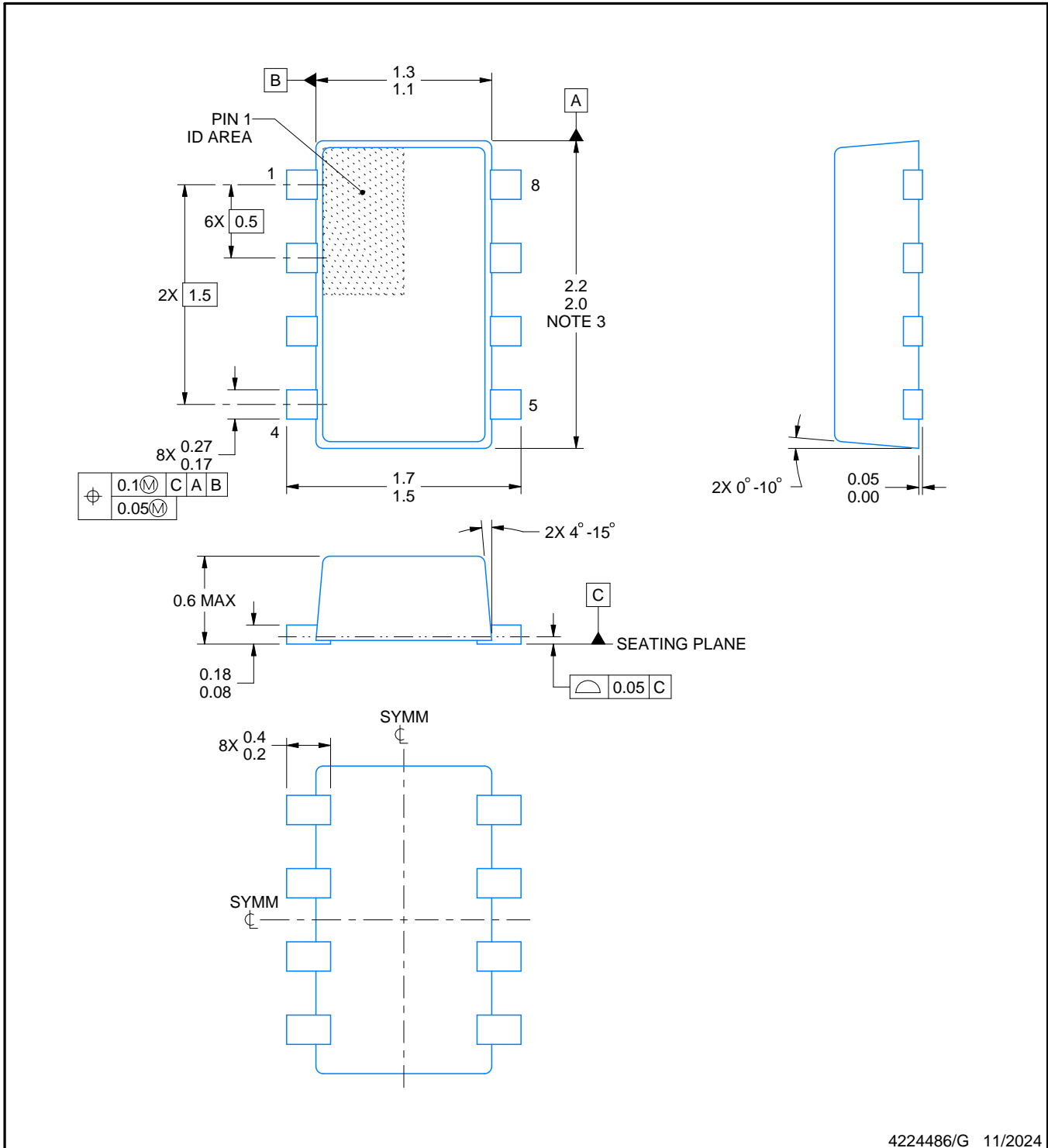
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22996DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22996DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0



4224486/G 11/2024

NOTES:

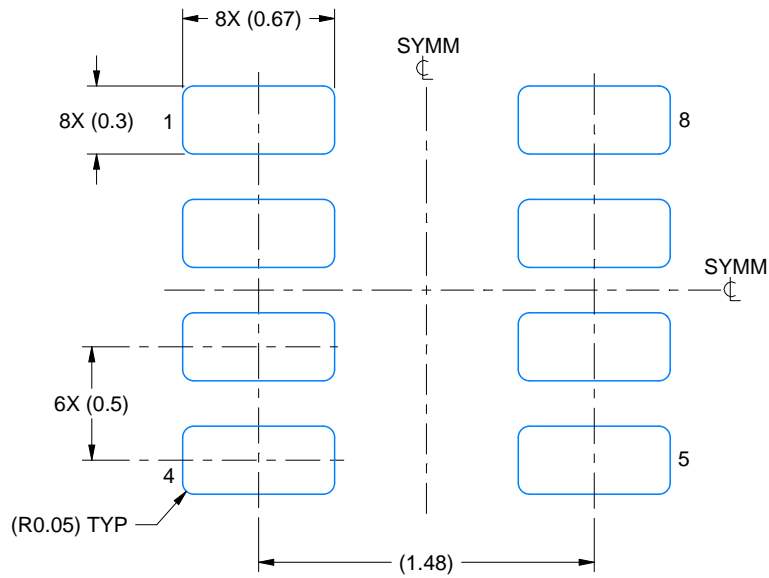
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

# EXAMPLE BOARD LAYOUT

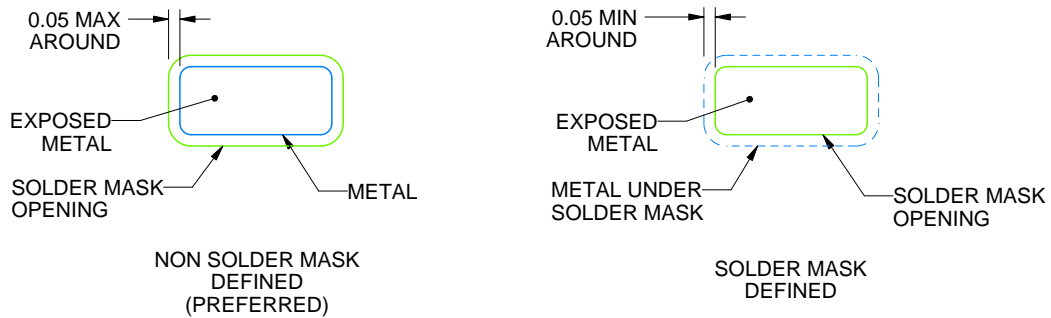
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

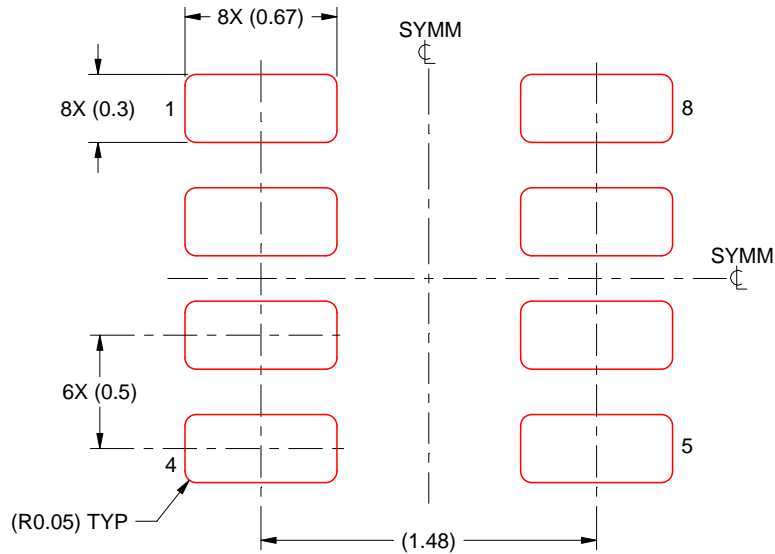
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4224486/G 11/2024

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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