TEXAS INSTRUMENTS
TPD4E02B04-Q1
JAJSDV1A – JUNE 2017 – REVISED SEPTEMBER 2017

TPD4E02B04-Q1 USB Type-CおよびHDMI 2.0用の4チャネルESD保護ダイオード

1 特長

- AEC-Q101認定済み
- IEC 61000-4-2 レベル4 ESD保護
  - 接触放電±12kV
  - エアギャップ放電±15kV
- ISO 10605 (330pF、330Ω) ESD保護
  - 接触放電±10kV
  - エアギャップ放電±10kV
- IEC 61000-4-4 EFT保護
  - 80A (5/50ns)
- IEC 61000-4-5 サージ保護
  - 2A (8/20µs)
- IO容量
  - 0.25pF (標準値)
- DCブレークダウン電圧: 5.5V (最小値)
- 非常に低いリーク電流: 10nA (最大値)
- 低いESDクランピング電圧: 5A TLPにおいて8.8V
- 最大10Gbpsの高速インターフェイスをサポート
- 工業用温度範囲: −40℃～＋125℃
- 使いやすいフロースルー配線パッケージ

2 アプリケーション

- 最終製品
  - ヘッド・ユニット
  - リアシート用エンターテイメント
  - テレマティクス
  - USBハブ
  - クラスタ
  - 車体制御モジュール
  - メディア・インターフェイス
- インターフェイス
  - USB Type-C
  - USB 3.1 Gen 2
  - HDMI 2.0/1.4
  - USB 3.0
  - DisplayPort 1.3
  - 10/100/1000Mbpsイーサネット

3 概要

TPD4E02B04-Q1は、USB Type-CおよびHDMI 2.0回路保護に対応した車載用双方向TVS ESD保護ダイオード・アレイです。TPD4E02B04-Q1は、ISO 10605 (330pF、330Ω) ESD規格に準拠し、最大10kVのESD衝撃を放散できます。またTPD4E02B04は、IEC 61000-4-2国際規格(レベル 4)で規定されている最大レベルのESD耐性を備えています。

このデバイスはチャネル当たりのIO容量が0.25pFであることから、USB 3.1 Gen2など、10Gbpsまでの高速インターフェイスの保護に理想的です。動的抵抗とクランピング電圧が低いため、過渡事象に対してシステム・レベルの保護が保証されます。

TPD4E02B04-Q1は、業界標準のUSON-10 (DQA)パッケージで供給されます。このパッケージはフロースルー配線と0.5mmピン・ピッチを採用しているため、実装が容易で、設計時間を短縮できます。

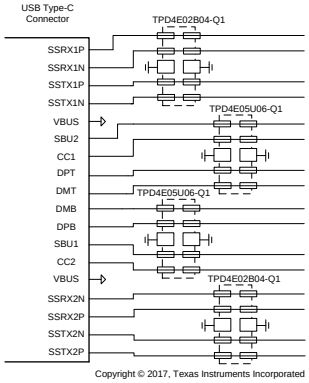
このデバイスには、車載用認定なしのバージョンとしてTPD4E02B04も用意されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPD4E02B04-Q1	USON (10)	2.50mm×1.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

代表的なアプリケーションの回路図



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4 改訂履歴

2017年6月発行のものから更新 **Page**

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- ISOエアギャップの定格を10kVに 変更 ... 1
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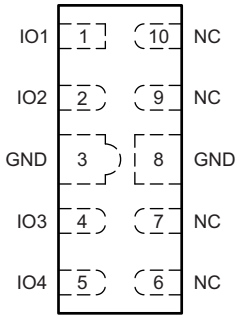
5 Pin Configuration and Functions

DQA Package
10-Pin USON
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	3	Ground	Ground. Connect to ground
GND	8		
IO1	1	I/O	ESD protected channel
IO2	2		
IO3	4		
IO4	5		
NC	6	NC	Not connected; Used for optional straight-through routing. Can be left floating or grounded
NC	7		
NC	9		
NC	10		

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-5 (5/50 ns) at 25°C		80	A
Peak pulse	IEC 61000-4-5 power (t_p - 8/20 µs) at 25°C		17	W
	IEC 61000-4-5 Ccurrent (t_p - 8/20 µs) at 25°C		2	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings—AEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±12000	V
		IEC 61000-4-2 air-gap discharge	±15000	

6.4 ESD Ratings—ISO Specification

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	ISO 10605 330 pF, 330 Ω, IO	Contact discharge	±10000	V
			Air-gap discharge	±10000	

6.5 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–3.6	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.6 Thermal Information

THERMAL METRIC(1)		TPD4E02B04-Q1 DQA (USON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	348.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	214.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	270.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	81.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	270.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.7 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 10 nA	–3.6		3.6	V
V_{BRF}	Breakdown voltage, any IO pin to GND(1)	I_{IO} = 1 mA, T_A = 25°C	5.5	6.4	7.5	V
V_{BRR}	Breakdown voltage, GND to any IO pin(1)	I_{IO} = 1 mA, T_A = 25°C	–5.5	–6.4	–7.5	V
V_{HOLD}	Holding voltage(2)	I_{IO} = 1 mA		5.8		V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		6.6		V
		I_{PP} = 5 A, TLP, from IO to GND		8.8		
		I_{PP} = 1 A, TLP, from GND to IO		6.6		
		I_{PP} = 5 A, TLP, from GND to IO		8.8		
I_{LEAK}	Leakage current, any IO to GND	V_{IO} = ±2.5 V			10	nA
R_{DYN}	Dynamic resistance	IO to GND		0.47		Ω
		GND to IO		0.47		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		0.25	0.33	pF
ΔC_L	Variation of line capacitance	Delta of capacitance between any two IO pins, V_{IO} = 0 V, f = 1 MHz, T_A = 25°C, GND = 0 V		0.01	0.07	pF
C_{CROSS}	Channel to channel capacitance	Capacitance from one IO to another, V_{IO} = 0 V, f = 1 MHz, GND = 0 V		0.13	0.16	pF

(1) V_{BRF} and V_{BRR} are defined as the voltage when 1 mA is applied in the positive-going direction, before the device latches into the snapback state.
(2) V_{HOLD} is defined as the voltage when 1 mA is applied in the negative-going direction, after the device has successfully latched into the snapback state.

6.8 Typical Characteristics

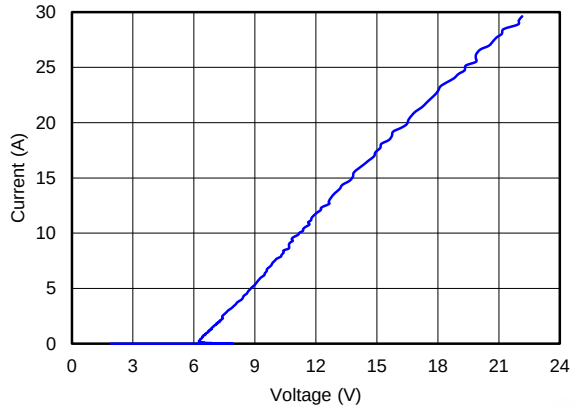


図 1. Positive TLP Curve

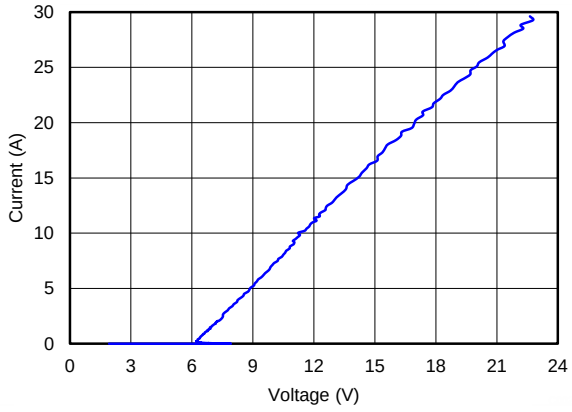


図 2. Negative TLP Curve

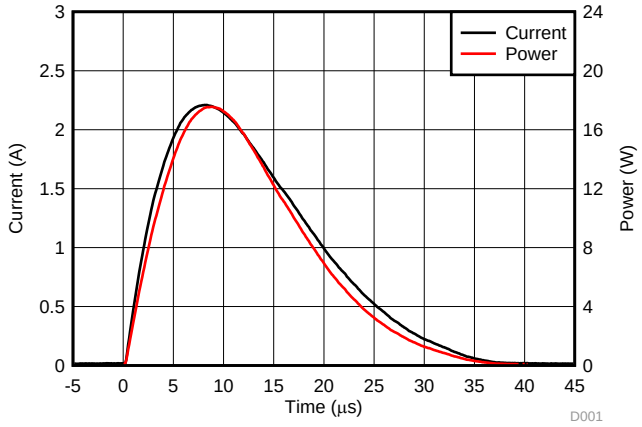


図 3. Surge Curve (t_p = 8/20 µs), any IO pin to GND

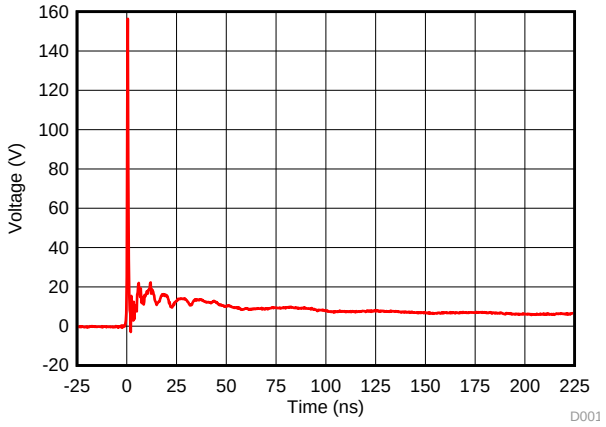


図 4. 8-kV IEC Waveform

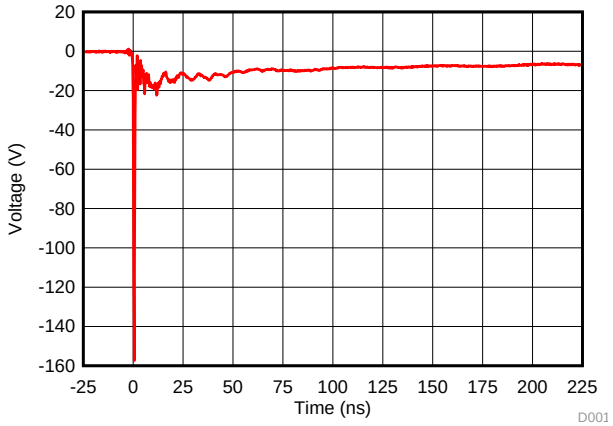


図 5. –8-kV IEC Waveform

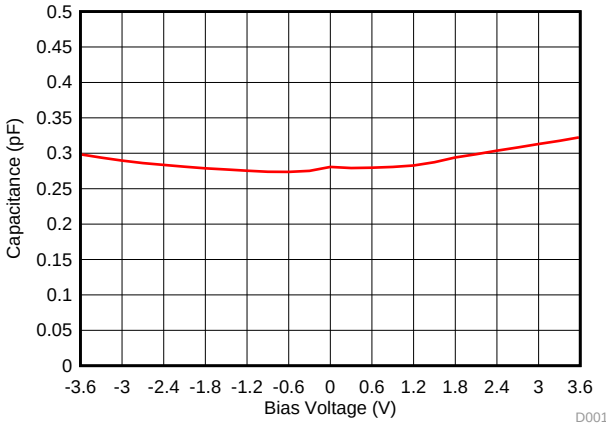


図 6. Capacitance vs Bias Voltage

Typical Characteristics (continued)

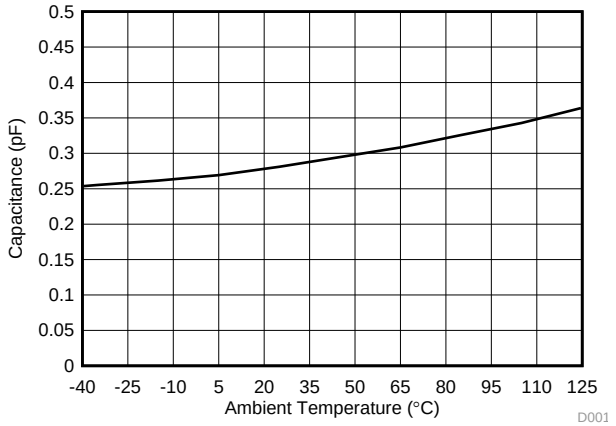


図 7. Capacitance vs Ambient Temperature

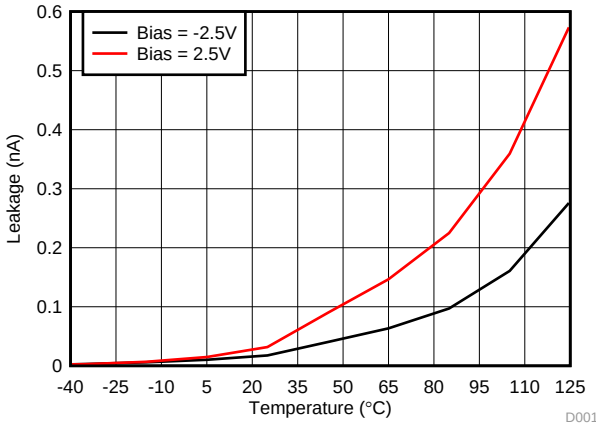


図 8. Leakage Current vs Temperature

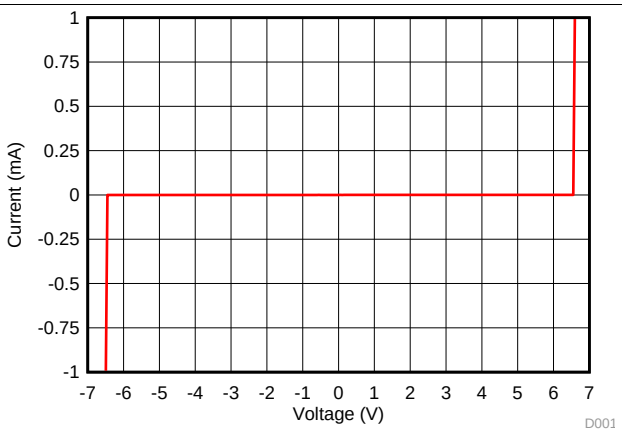


図 9. DC Voltage Sweep I-V Curve

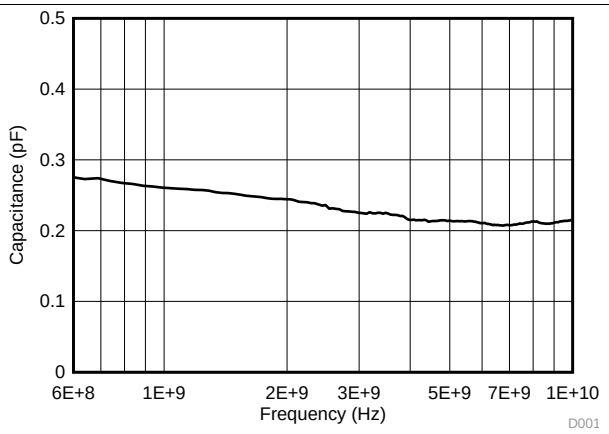


図 10. Capacitance vs Frequency

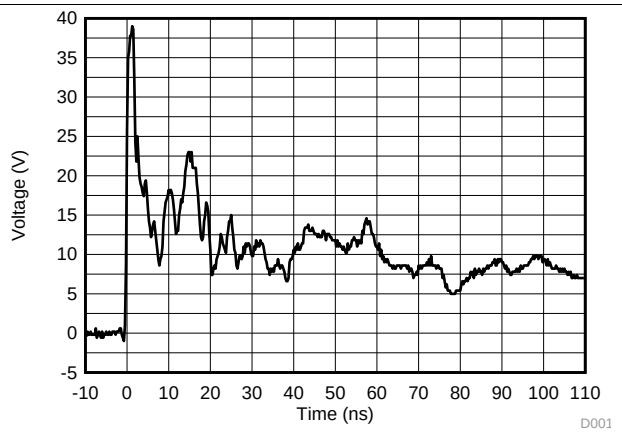


図 11. 8-kV IEC Waveform through 2-m HDMI Cable

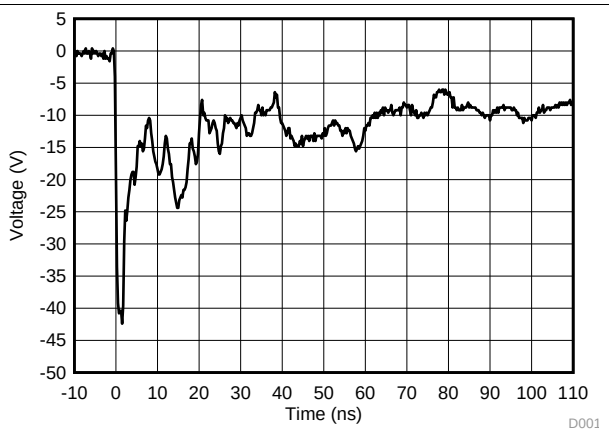


図 12. –8-kV IEC Waveform through 2-m HDMI Cable

Typical Characteristics (continued)

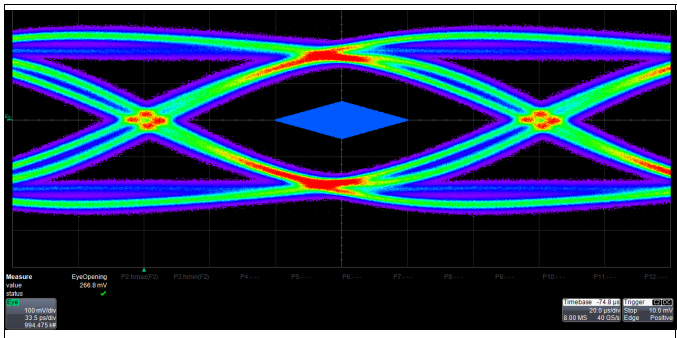


図 13. USB3.0 Eye Diagram (Bare Board)

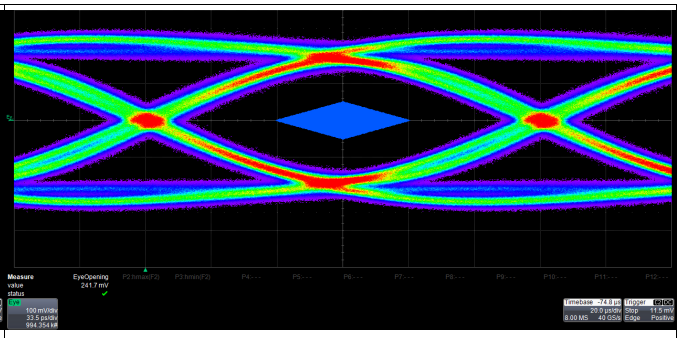


図 14. USB3.0 Eye Diagram (With TPD4E02B04-Q1)

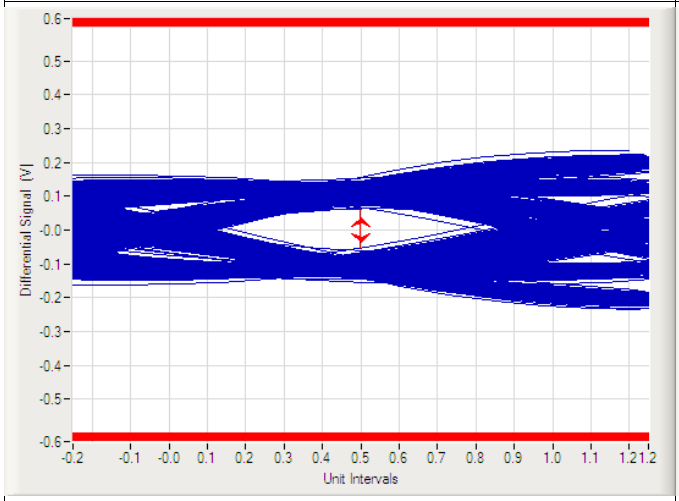


図 15. USB3.1 Gen 2 Eye Diagram (Bare Board)

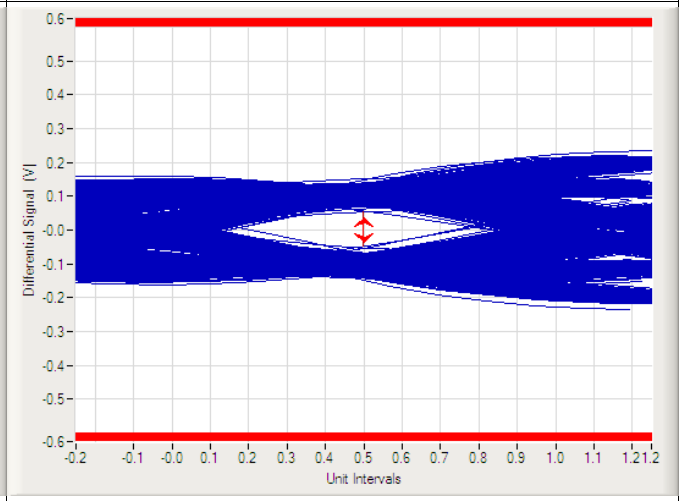


図 16. USB3.1 Gen 2 Eye Diagram (With TPD4E02B04-Q1)

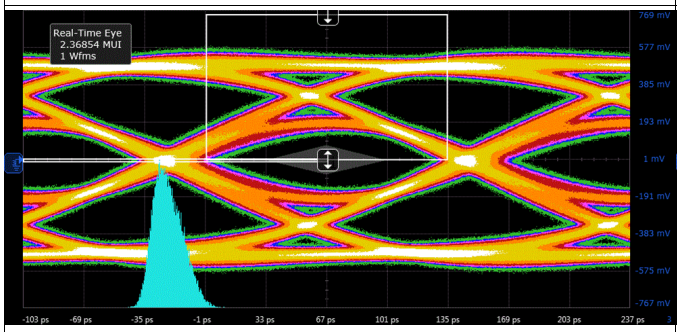


図 17. HDMI2.0 6-Gbps TP2 Eye Diagram (Bare Board)

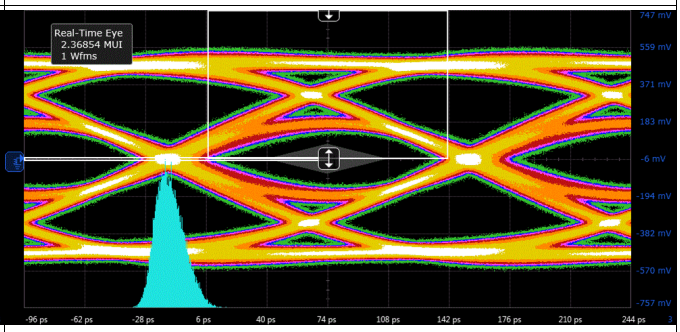


図 18. HDMI2.0 6-Gbps TP2 Eye Diagram (With TPD4E02B04-Q1)

Typical Characteristics (continued)

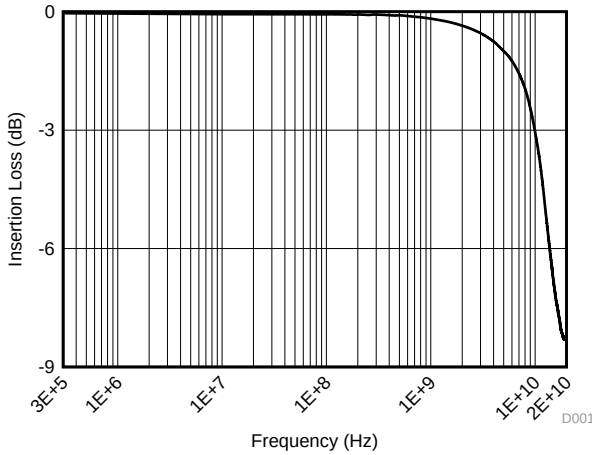


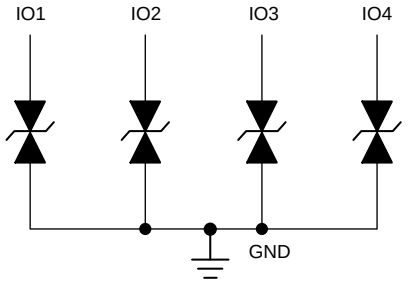
図 19. Differential Insertion Loss

7 Detailed Description

7.1 Overview

The TPD4E02B04-Q1 is an automotive-qualified bidirectional ESD Protection Diode with ultra-low capacitance. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 (Level 4) International Standard. The ultra-low capacitance makes this device ideal for protecting any super high-speed signal pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 AEC-Q101 Qualified

This device is qualified to AEC-Q101 standards and is qualified to operate from –40°C to +125°C.

7.3.2 ISO 10605 ESD Protection

The I/O pins can withstand ESD events of at least ±10-kV contact and ±10-kV air gap according to the ISO 10605 (330 pF, 330 Ω) standard. The device diverts the current to ground.

7.3.3 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±12-kV contact and ±15-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.4 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.5 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 2 A and 17 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.6 IO Capacitance

The capacitance between each I/O pin to ground is 0.25 pF (typical). This device supports data rates up to 10 Gbps.

7.3.7 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of ±5.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.8 Ultra Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (maximum) with a bias of ±2.5 V.

Feature Description (continued)

7.3.9 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.8 V (I_{PP} = 5 A).

7.3.10 Supports High Speed Interfaces

This device is capable of supporting high speed interfaces up to 10 Gbps, because of the extremely low IO capacitance.

7.3.11 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.12 Easy Flow-Through Routing Package

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD4E02B04-Q1 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±15 kV (air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of the TPD4E02B04-Q1 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD4E02B04-Q1 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

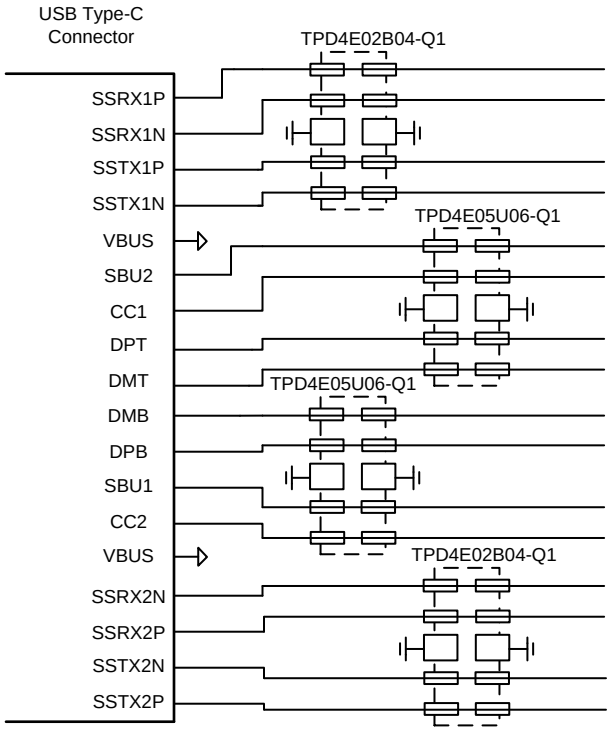


図 20. USB 3.1 Gen 2 Type-C ESD Schematic

Typical Application (continued)

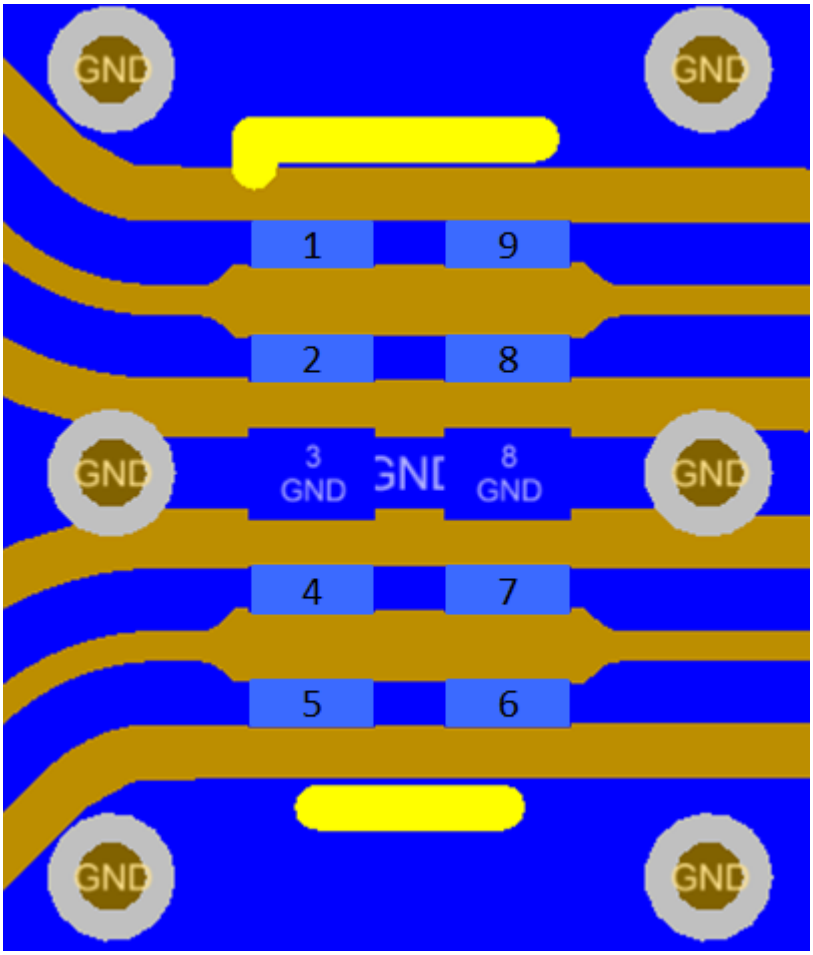


図 21. USB 3.1 Gen 2 SuperSpeed Layout

8.2.1 Design Requirements

For this design example two TPD4E02B04-Q1 devices and two TPD4E05U06 devices are being used in a USB 3.1 Gen 2 Type-C application. This provides a complete ESD protection scheme.

Given the USB 3.1 Gen 2 Type-C application, the parameters listed in 表 1 are known.

表 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal Range on SuperSpeed+ Lines	0 V to 3.6 V
Operating Frequency on SuperSpeed+ Lines	5 GHz
Signal Range on CC, SBU, and DP/DM Lines	0 V to 5 V
Operating Frequency on CC, SBU, and DP/DM Lines	up to 480 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD4E02B04-Q1 supports signal ranges between –3.6 V and 3.6 V, which supports the SuperSpeed+ pairs on the USB Type-C application. The TPD4E05U06 supports signal ranges between 0 V and 5.5 V, which supports the CC, SBU, and DP/DM lines.

8.2.2.2 Operating Frequency

The TPD4E02B04-Q1 has a 0.25 pF (typical) capacitance, which supports the USB3.1 Gen 2 data rates of 10 Gbps. The TPD4E05U06 has a 0.5 pF (typical) capacitance, which easily supports the CC, SBU, and DP/DM data rates.

8.2.3 Application Curves

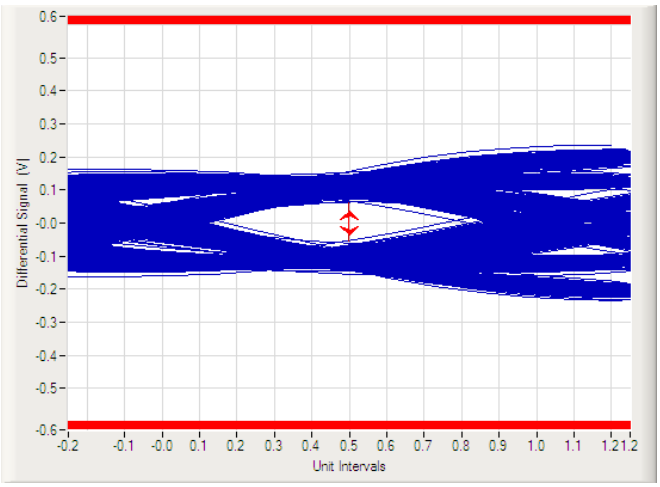


図 22. USB 3.1 Gen 2 10-Gbps Eye Diagram (Bare Board)

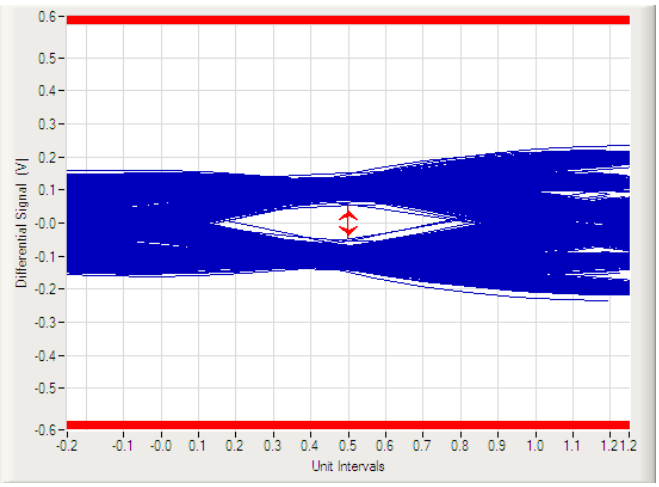


図 23. USB 3.1 Gen 2 10-Gbps Eye Diagram (With TPD4E02B04-Q1)

9 Power Supply Recommendations

This device is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Examples

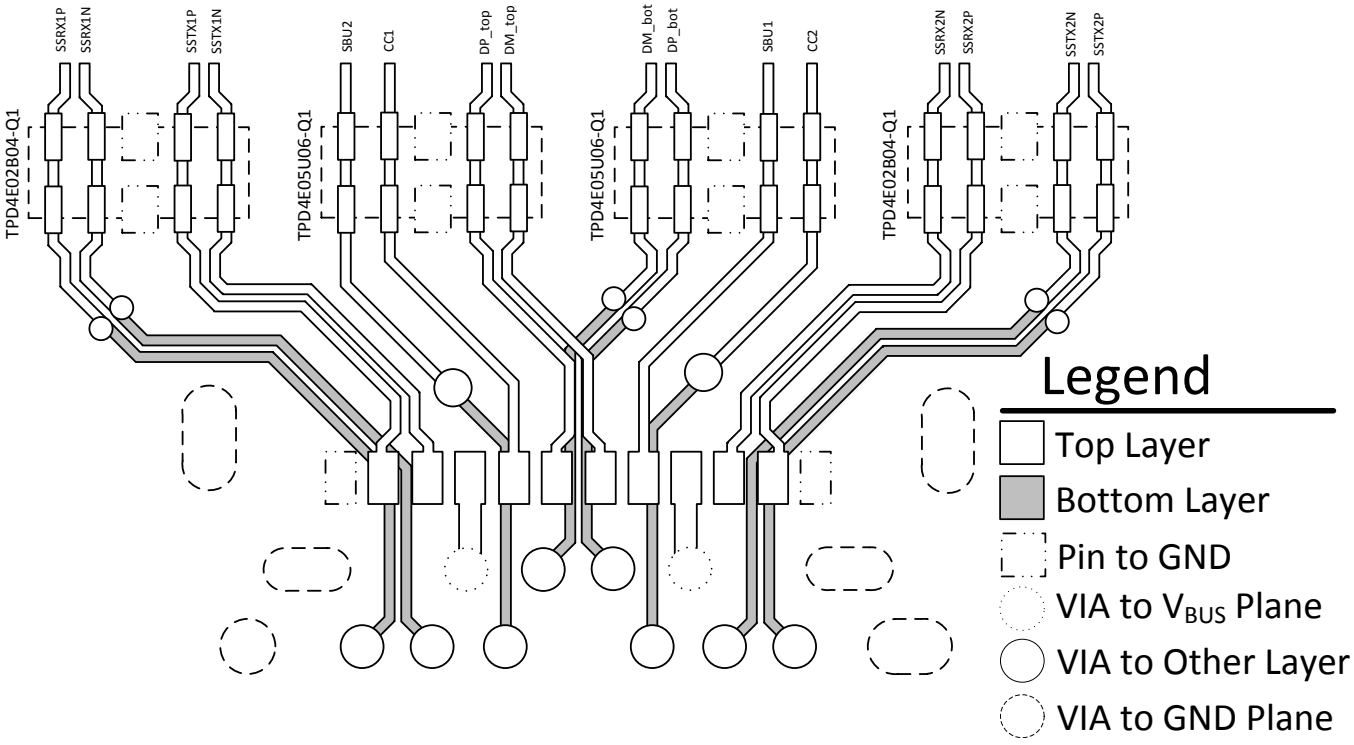


図 24. USB Type-C Mid-Mount, Hybrid Connector with One-Sided ESD Layout

Layout Examples (continued)

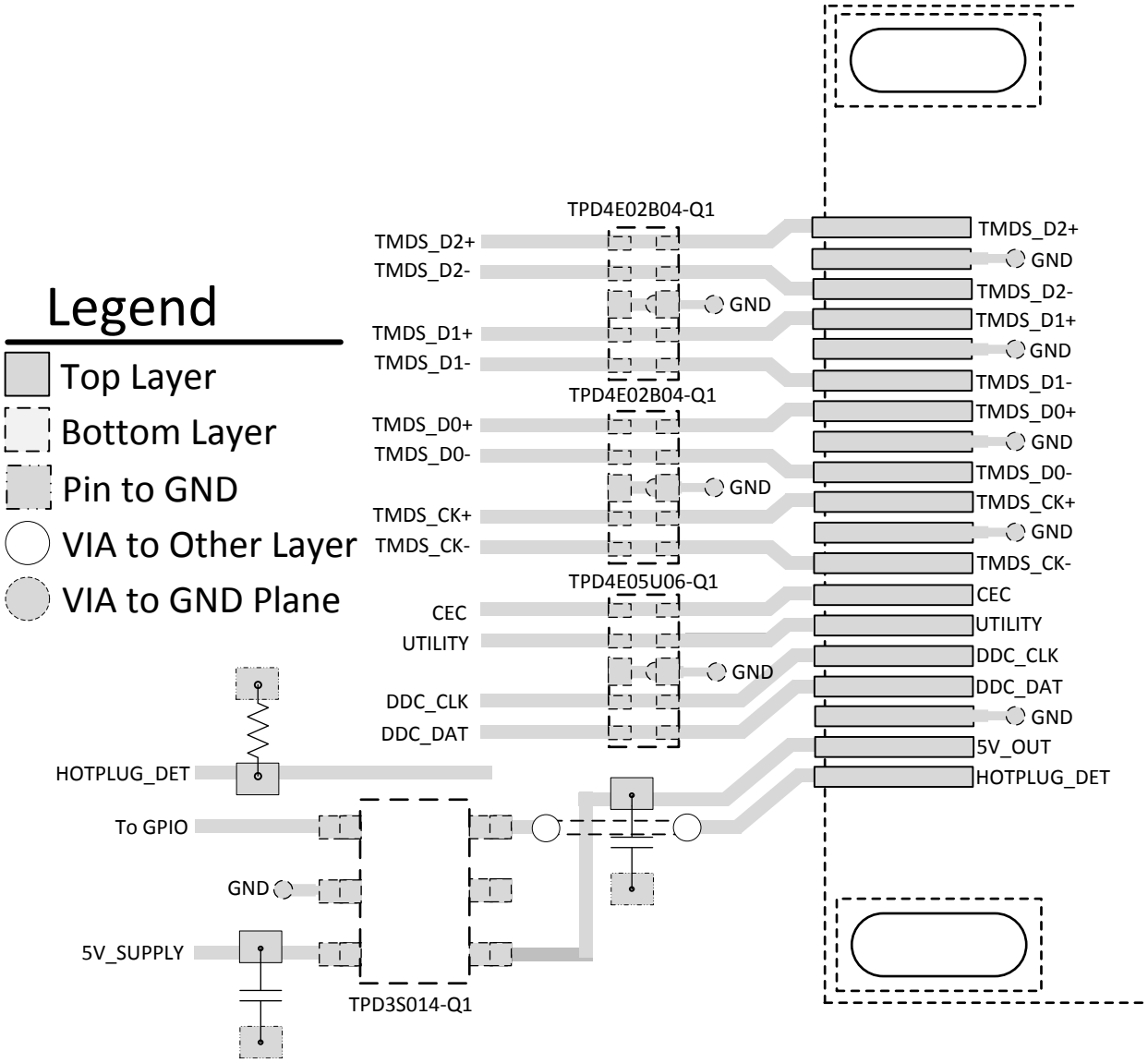


図 25. HDMI2.0 Type-A Transmitter Port Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- 『*ESD保護データシートの閲覧と理解*』、SLLA305
- 『*ESDレイアウト・ガイド*』、SLVA680
- 『*超高速データ・ライン用ESDダイオードの選択*』、SLVA785
- 『*TPD4E02B04EVM ユーザー・ガイド*』、SLVUAH6

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

11.4 商標

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11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E02B04QDQARQ1	ACTIVE	USON	DQA	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BQ1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

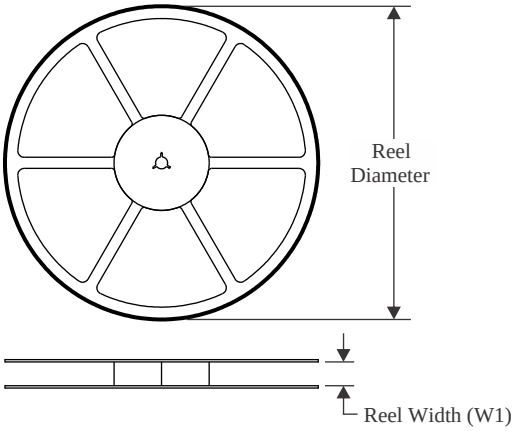
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

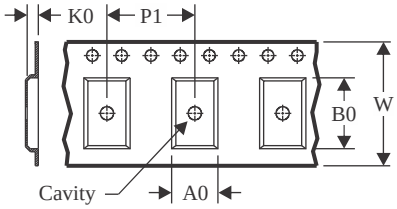
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

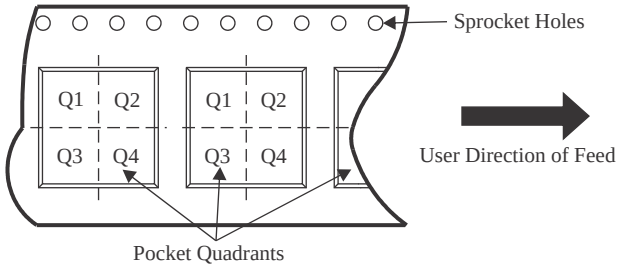


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

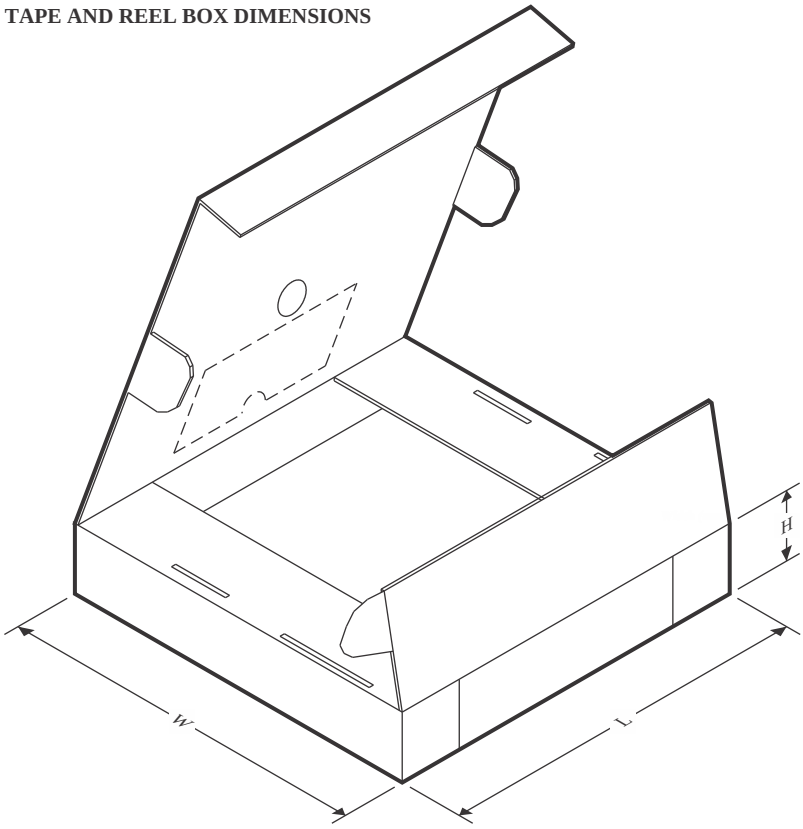
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E02B04QDQARQ1	USON	DQA	10	3000	180.0	9.5	1.18	2.68	0.72	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E02B04QDQARQ1	USON	DQA	10	3000	189.0	185.0	36.0

GENERIC PACKAGE VIEW

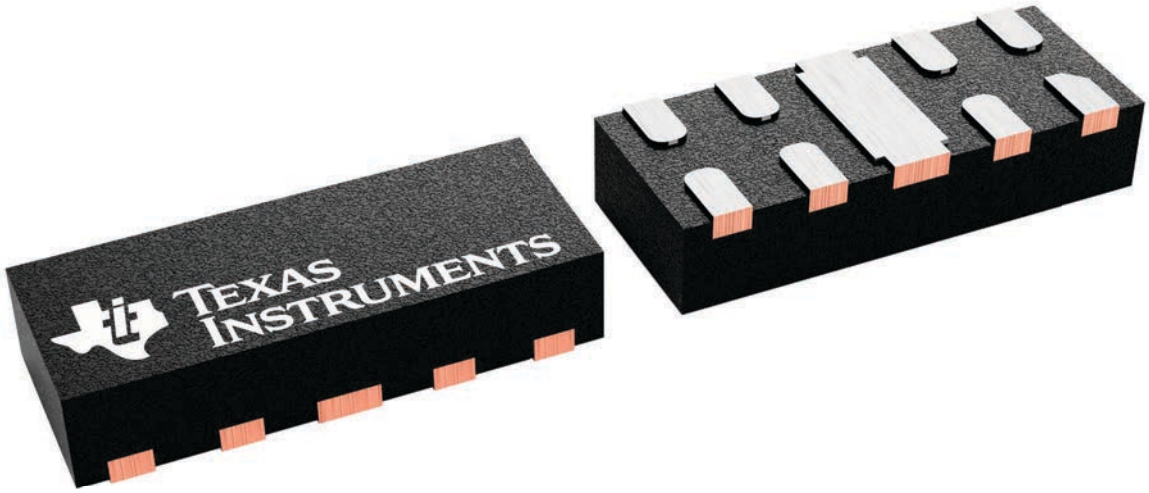
DQA 10

USON - 0.55 mm max height

1 x 2.5, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



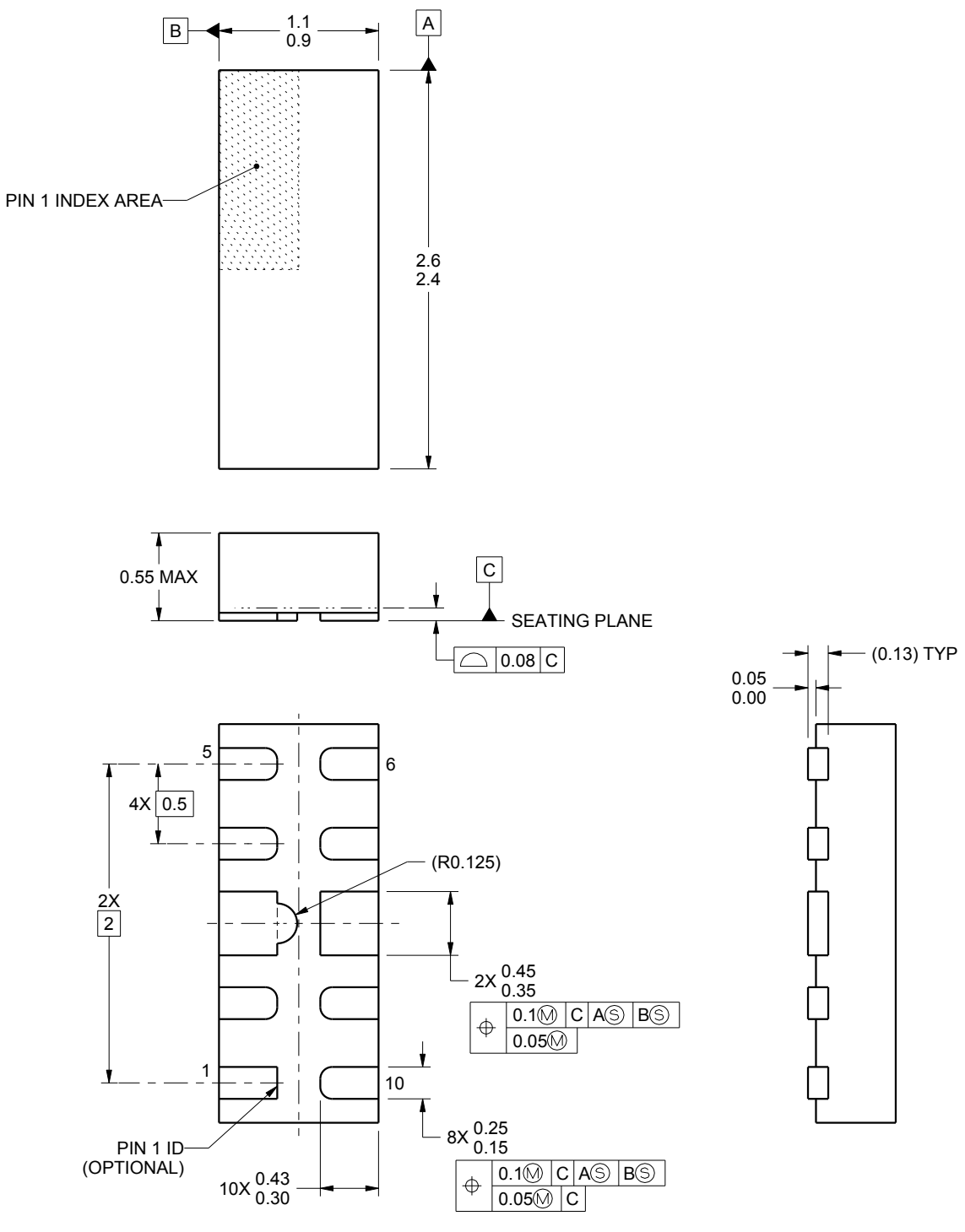
4230320/A

PACKAGE OUTLINE

DQA0010A

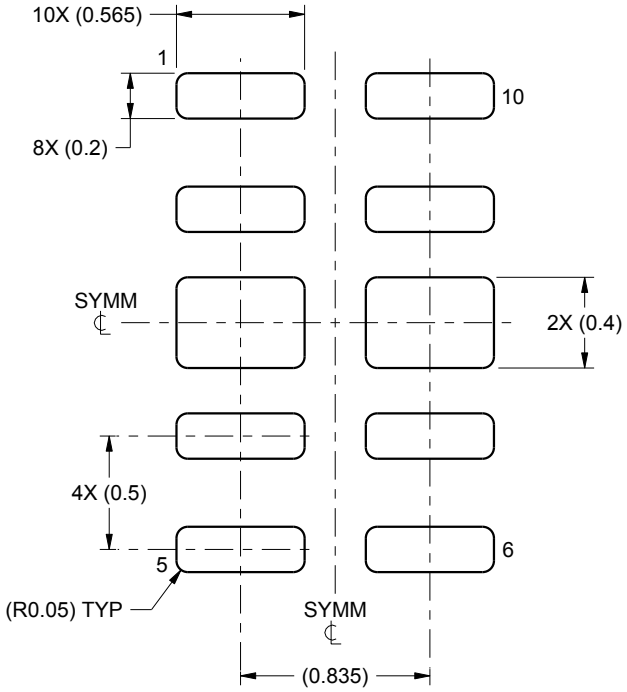
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

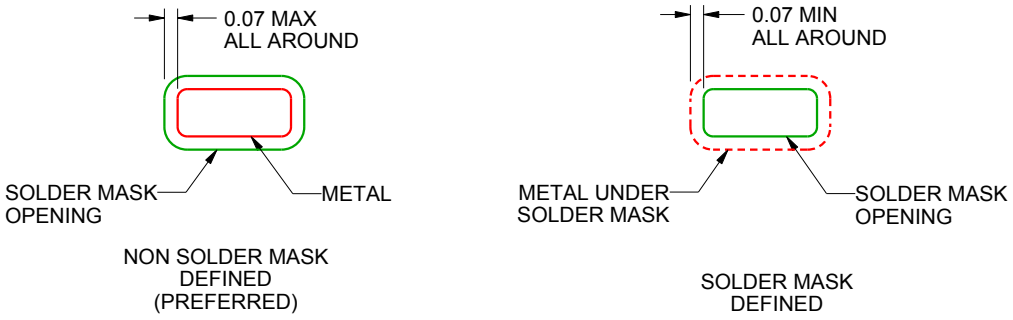


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS

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NOTES: (continued)

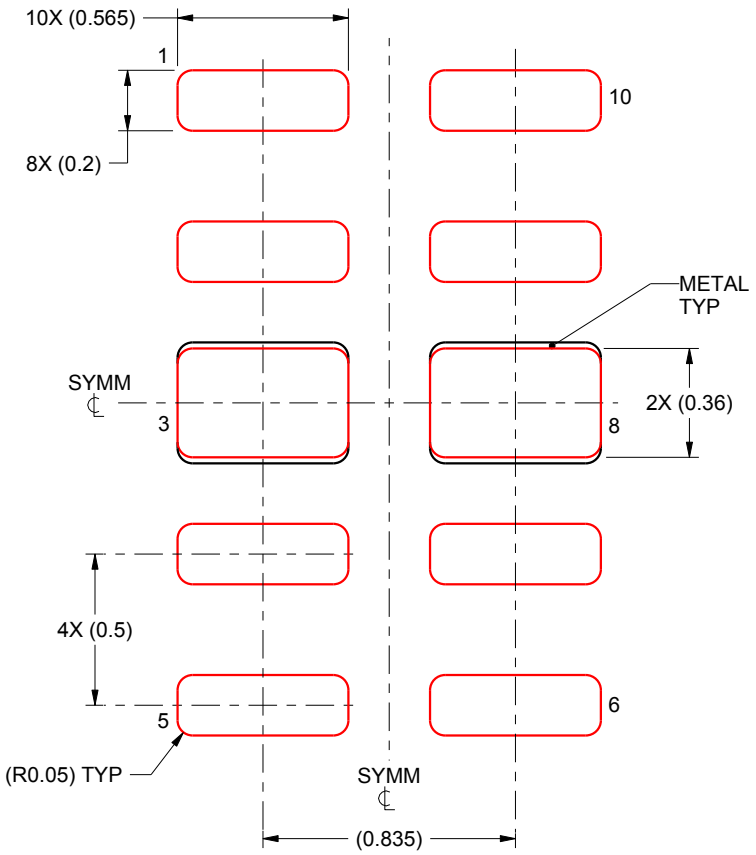
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DQA0010A

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PADS 3 & 8:
90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:40X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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