

## TPD2E2U06 2 チャンネル高速 ESD 保護デバイス

### 1 特長

- IEC 61000-4-2 レベル 4
  - ±25kV (接触放電)
  - ±30kV (エアギャップ放電)
- IEC 61000-4-5 サージ保護
  - 5.5A ピーク・パルス電流 (8/20 $\mu$ s のパルス)
- IO 容量: 1.5pF (標準値)
- DC 降伏電圧: 6.5V (最小値)
- 非常に低いリーク電流: 10nA (最大値)
- 低い ESD クランプ電圧
- 産業用温度範囲: -40°C ~ +125°C
- 小型で配線が容易な DRL および DCK パッケージ

### 2 アプリケーション

- 最終製品
  - セット・トップ・ボックス
  - ノート PC
  - サーバー
  - 電子 POS (EPOS)
- インターフェイス
  - USB 2.0
  - イーサネット
  - MIPI バス
  - LVDS
  - I2C

### 3 概要

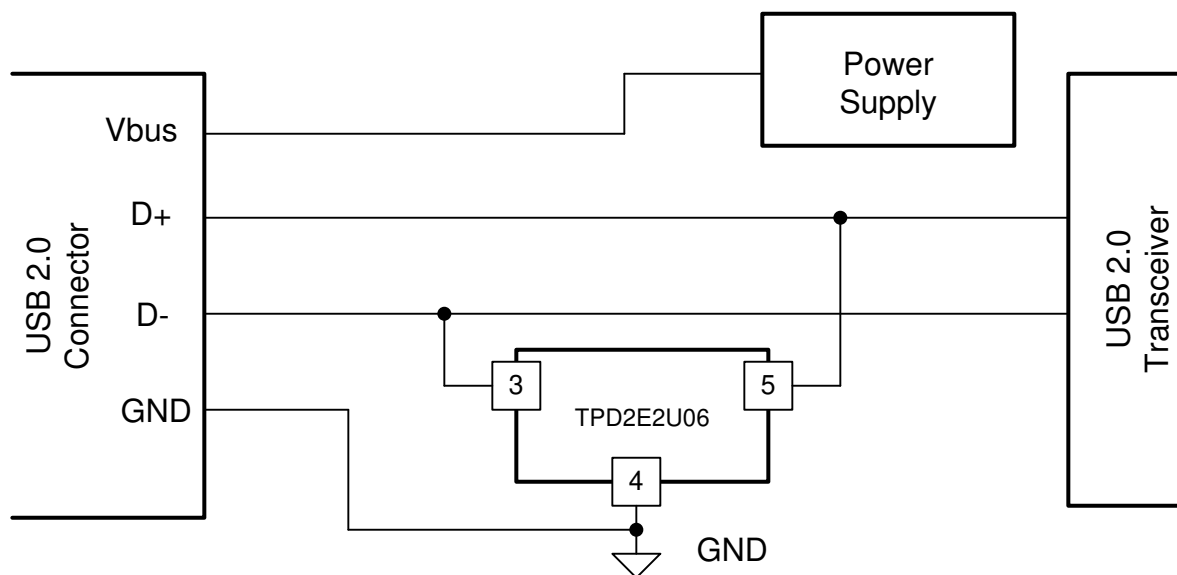
TPD2E2U06 はデュアル・チャンネルの低容量 TVS ダイオード ESD 保護デバイスです。IEC 61000-4-2 規格に準拠し、接触で ±25kV、エアギャップで ±30kV の ESD 保護を実現します。TPD2E2U06 は、ライン容量が 1.5pF であるため、幅広いアプリケーションに適しています。代表的なアプリケーション・インターフェイスは USB 2.0、LVDS、I<sup>2</sup>C™ です。

#### 製品情報<sup>(1)</sup>

型番	パッケージ	本体サイズ(公称)
TPD2E2U06DRL	SOT (5)	1.60mm×1.20mm
TPD2E2U06DCK	SC70 (3)	2.0mm × 1.25mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



## 目次

1	特長	1	7.3	Feature Description	8
2	アプリケーション	1	7.4	Device Functional Modes	9
3	概要	1	<b>8</b>	<b>Application and Implementation</b>	<b>10</b>
4	改訂履歴	2	8.1	Application Information	10
5	<b>Pin Configuration and Functions</b>	3	8.2	Typical Application	10
6	<b>Specifications</b>	3	<b>9</b>	<b>Power Supply Recommendations</b>	<b>11</b>
6.1	Absolute Maximum Ratings	3	<b>10</b>	<b>Layout</b>	<b>11</b>
6.2	ESD Ratings	4	10.1	Layout Guidelines	11
6.3	Recommended Operating Conditions	4	10.2	Layout Example	12
6.4	Thermal Information	4	<b>11</b>	<b>デバイスおよびドキュメントのサポート</b>	<b>12</b>
6.5	Electrical Characteristics	4	11.1	商標	12
6.6	Typical Characteristics	6	11.2	ドキュメントの更新通知を受け取る方法	12
<b>7</b>	<b>Detailed Description</b>	<b>8</b>	11.3	サポート・リソース	12
7.1	Overview	8	11.4	Glossary	12
7.2	Functional Block Diagram	8	<b>12</b>	<b>メカニカル、パッケージ、および注文情報</b>	<b>12</b>

## 4 改訂履歴

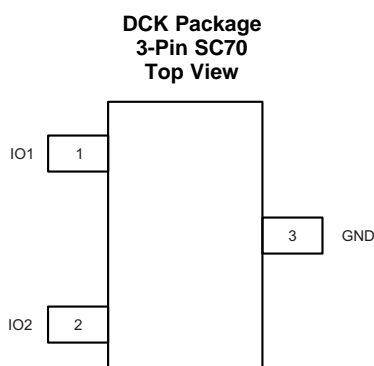
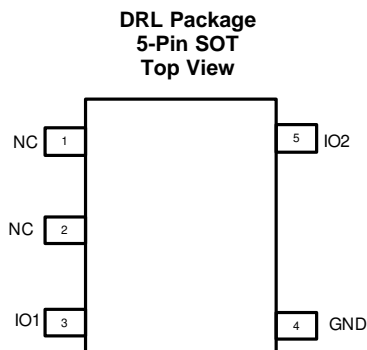
### Revision B (May 2015) から Revision C に変更 Page

- Added DCK Package to the [Pin Configuration and Functions](#) section..... **3**
- Added DCK Package to the [Electrical Characteristics](#) table ..... **4**

### Revision A (June 2013) から Revision B に変更 Page

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを 追加 ..... **1**

## 5 Pin Configuration and Functions



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DRL	DCK		
IO1	3	1	I/O	The IO1 and IO2 pins are an ESD protected channel. Connect these pins to the data line as close to the connector as possible.
IO2	5	2	I/O	
NC	1, 2	—	-	This pin is not connected and is left floating, grounded, or connected to VCC.
GND	4	3	G	The GND (ground) pin is connected to ground.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
$I_{PP}$ Peak pulse current ( $t_p = 8/20 \mu s$ )		5.5 <sup>(1)</sup>	A
$P_{PP}$ Peak pulse power ( $t_p = 8/20 \mu s$ ) DRL package		85 <sup>(1)</sup>	W
$P_{PP}$ Peak pulse power ( $t_p = 8/20 \mu s$ ) DCK package		75 <sup>(1)</sup>	W
Operating temperature	-40	125	°C
Storage temperature	-65	155	°C

(1) Measured at 25°C.

## 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500
		EC 61000-4-2 contact	±25000
		EC 61000-4-2 air-gap	±30000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IO</sub>	Input Pin Voltage	0		5.5	V
T <sub>A</sub>	Operating Free Air Temperature	-40		125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPD2E2U06		UNIT
		DRL	DCK	
		5 PINS	3 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	286.8	308.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	130.7	170.7	
R <sub>θJB</sub>	Junction-to-board thermal resistance	104.8	89.2	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	25.6	34.2	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	104.3	88.6	

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>RWM</sub>	Reverse stand-off voltage	I <sub>IO</sub> < 10 μA			5.5	V
V <sub>CLAMP</sub>	IO to GND	I <sub>PP</sub> = 1 A, TLP <sup>(1)</sup>		9.7		V
		I <sub>PP</sub> = 5 A, TLP <sup>(1)</sup>		12.4		
V <sub>CLAMP</sub>	GND to IO	I <sub>PP</sub> = 1 A, TLP <sup>(1)</sup>		1.9		V
		I <sub>PP</sub> = 5 A, TLP <sup>(1)</sup>		4		
R <sub>DYN</sub>	Dynamic resistance DRL package	IO to GND <sup>(2)</sup>		0.5		Ω
R <sub>DYN</sub>	Dynamic resistance DRL package	GND to IO <sup>(2)</sup>		0.25		Ω
R <sub>DYN</sub>	Dynamic resistance DCK package	IO to GND <sup>(2)</sup>		0.6		Ω
R <sub>DYN</sub>	Dynamic resistance DCK package	GND to IO <sup>(2)</sup>		0.4		Ω
CL	Line capacitance	f = 1 MHz, V <sub>BIAS</sub> = 2.5 V <sup>(3)</sup>		1.5	1.9	pF
C <sub>CROSS</sub>	Channel-to-channel input capacitance	Pin 4 = 0 V, f = 1 MHz, V <sub>BIAS</sub> = 2.5 V, between channel pins <sup>(3)</sup>		0.02	0.03	pF

- (1) Transmission Line Pulse with 10-ns rise time, 100-ns width.
- (2) Extraction of R<sub>DYN</sub> Using least squares fit of TLP characteristics between I = 20 A and I = 30 A.
- (3) Measured at 25°C.

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta C_{IO-TO-GND}$	Variation of channel input capacitance	Pin 4 = 0 V, $f = 1$ MHz, $V_{BIAS} = 2.5$ V, channel_x pin to GND – channel_y pin to GND <sup>(3)</sup>		0.03	0.1	pF
$V_{BR}$	Break-down voltage	$I_{IO} = 1$ mA	6.5		8.5	V
$I_{LEAK}$	Leakage current	$V_{IO} = 2.5$ V		1	10	nA

## 6.6 Typical Characteristics

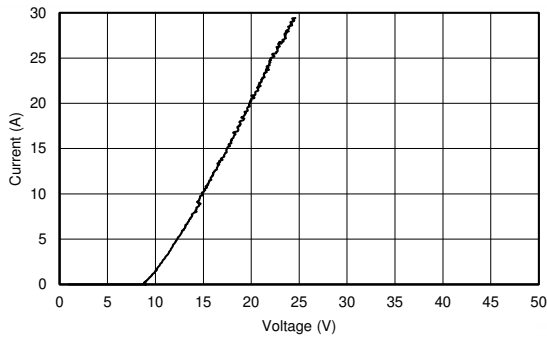


Figure 1. TLP, Data to GND

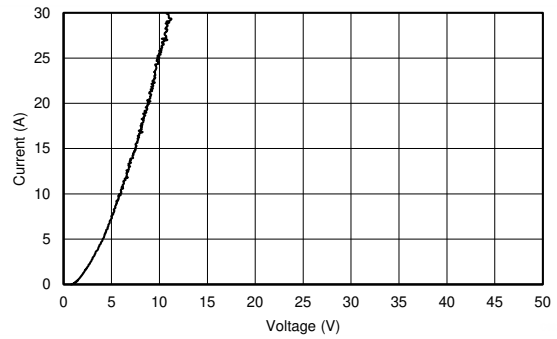


Figure 2. TLP, GND to Data

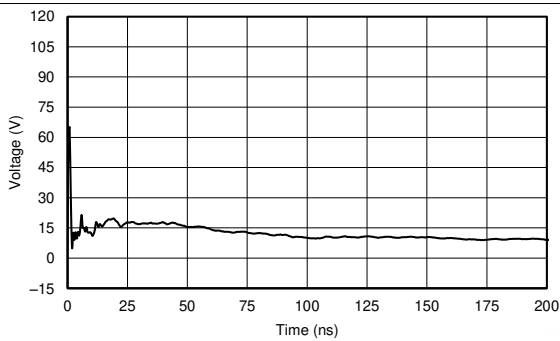


Figure 3. IEC 61000-4-2 Clamping Voltage, +8 kV Contact

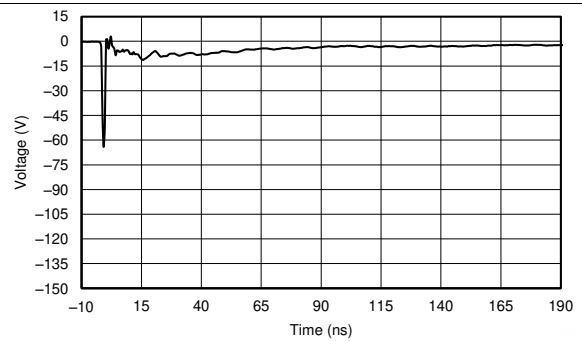
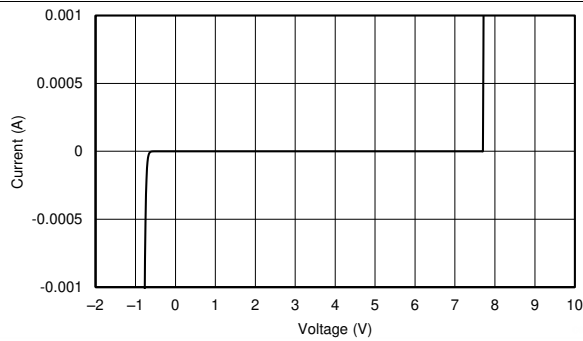
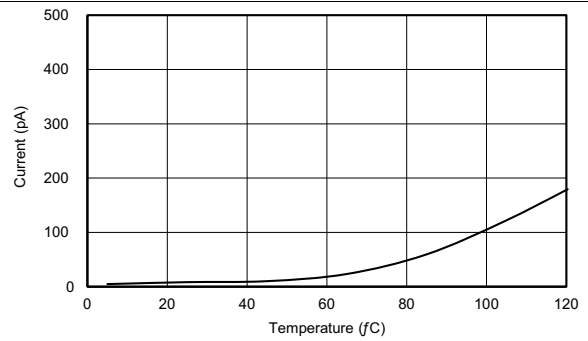


Figure 4. IEC 61000-4-2 Clamping Voltage, -8 kV Contact



$T_A = 25^\circ\text{C}$

Figure 5. IV Curve



$V_{IN} = 2.5\text{ V}$

Figure 6.  $I_{LEAK}$  vs Temperature

Typical Characteristics (continued)

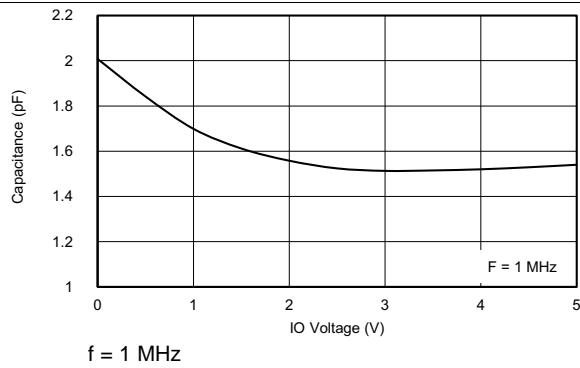


Figure 7. Capacitance Across V<sub>BIAS</sub>

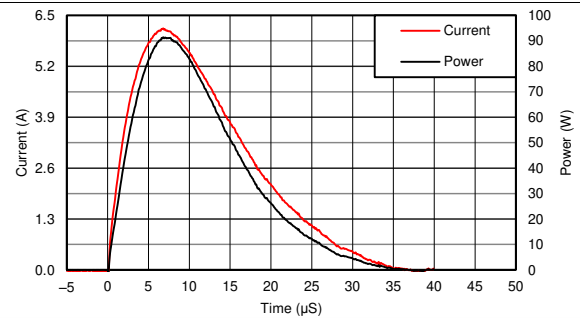


Figure 8. Surge Curve (tp = 8/20 μs) IO to GND

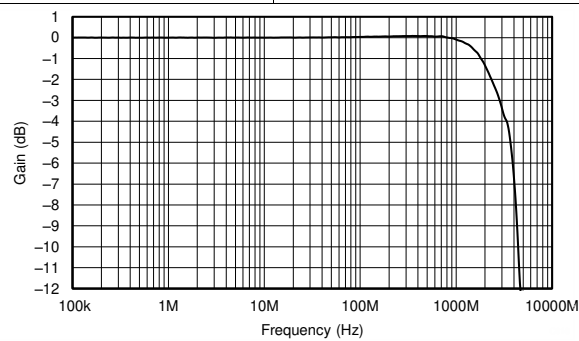


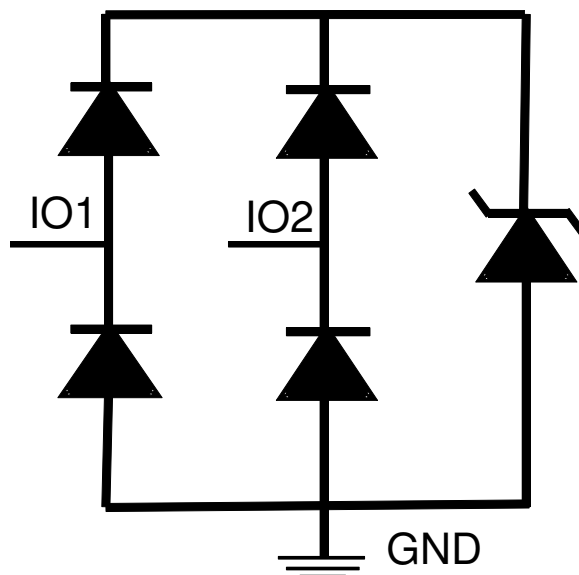
Figure 9. Insertion Loss

## 7 Detailed Description

### 7.1 Overview

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers  $\pm 25$ -kV contact and  $\pm 30$ -kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I2C.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The TPD2E2U06 is a dual-channel low capacitance TVS diode ESD protection device. The device offers  $\pm 25$ -kV contact and  $\pm 30$ -kV air-gap ESD protection in accordance with the IEC 61000-4-2 standard. The 1.5-pF line capacitance of the TPD2E2U06 makes the device suitable for a wide range of applications. Typical application interfaces are USB 2.0, LVDS, and I2C.

#### 7.3.1 IEC 61000-4-2 Level 4

The I/O pins can withstand ESD events up to  $\pm 25$ -kV contact and  $\pm 30$ -kV air. An ESD/surge clamp diverts the current to ground.

#### 7.3.2 IO Capacitance

The capacitance between each I/O pin to ground is 1.5 pF. These capacitances support data rates in excess of 1.5 Gbps.

#### 7.3.3 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is a minimum of 6.5 V. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of 5.5 V.

#### 7.3.4 Ultra-Low Leakage Current

The I/O pins feature an ultra-low leakage current of 10 nA (Max) with a bias of 2.5 V.

#### 7.3.5 Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 9.7 V ( $I_{PP} = 1$  A).



## Feature Description (continued)

### 7.3.6 Industrial Temperature Range

This device is designed to operate from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .

### 7.3.7 Small Easy-to-Route Package

The layout of this device makes it simple and easy to add protection to an existing layout. The package offers flow-through routing, requiring minimal modification to an existing layout.

## 7.4 Device Functional Modes

TPD2E2U06 is a passive integrated circuit that triggers when voltages are above  $V_{\text{BR}}$  or below the lower diodes  $V_f$  ( $-0.6\text{ V}$ ). During ESD events, voltages as high as  $\pm 30\text{ kV}$  (air) can be directed to ground via the internal diode network. Once the voltages on the protected line fall below the trigger levels of TPD2E2U06 (usually within 10's of nano-seconds) the device reverts to passive.

## 8 Application and Implementation

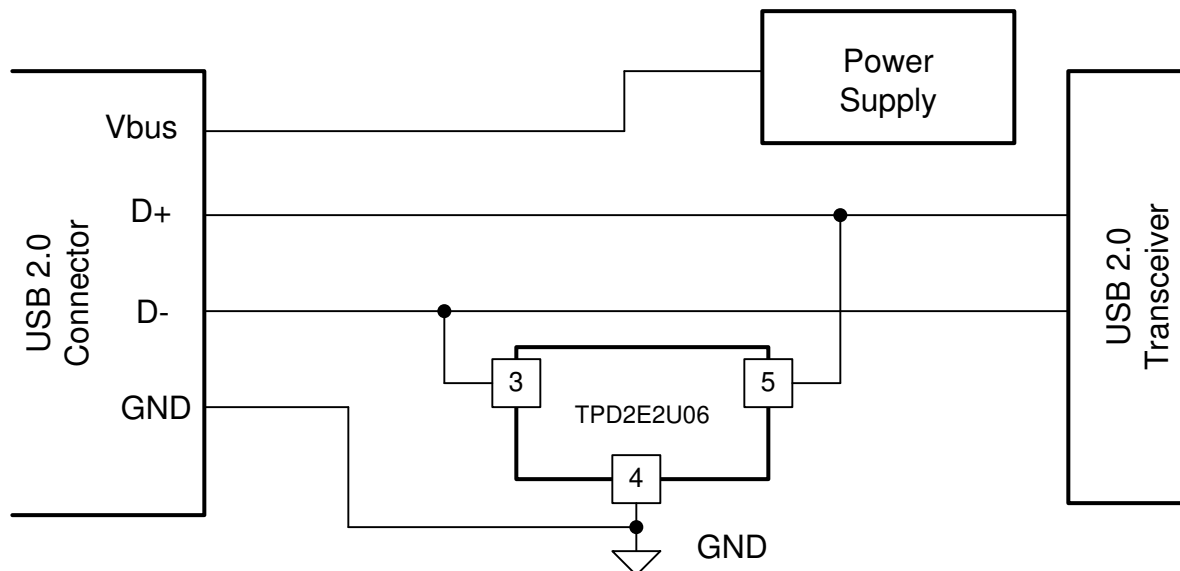
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

TPD2E2U06 is a diode type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low  $R_{DYN}$  of the triggered TVS holds this voltage,  $V_{CLAMP}$ , to a safe level for the protected IC.

### 8.2 Typical Application



**Figure 10. Typical USB Application Diagram**

#### 8.2.1 Design Requirements

For this design example, one TPD2E2U06 device will be used in a USB 2.0 application. This will provide complete port protection.

Given the USB 2.0 application, the following parameters are known.

DESIGN PARAMETER	VALUE
Signal range on Pins 3 or 5	0 V to 3.3 V
Operating Frequency	240 MHz

#### 8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer needs to know the following:

- Signal range of all the protected lines
- Operating frequency

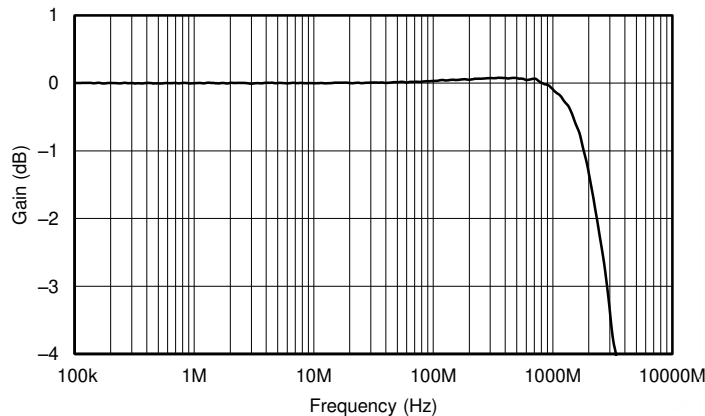
### 8.2.2.1 Signal Range

The TPD2E2U06 has 2 identical protection channels for signal lines. The symmetry of the device provides flexibility when selecting which of the 2 I/O channels will protect which signal lines. Any I/O will support a signal range of 0 to 5.5 V.

### 8.2.2.2 Operating Frequency

The TPD2E2U06 has a capacitance of 1.5 pF (Typ), supporting USB 2.0 data rates.

### 8.2.3 Application Curves



**Figure 11. Insertion Loss Graph**

## 9 Power Supply Recommendations

This device is a passive ESD protection device and there is no need to power it. Care should be taken to make sure that the maximum voltage specifications for each line are not violated.

## 10 Layout

### 10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

## 10.2 Layout Example

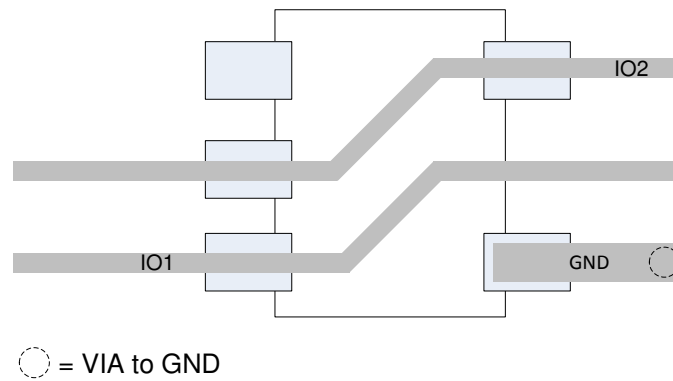


Figure 12. Routing with DRL Package

## 11 デバイスおよびドキュメントのサポート

### 11.1 商標

E2E is a trademark of Texas Instruments.  
 I<sup>2</sup>C is a trademark of NXP Semiconductors.  
 All other trademarks are the property of their respective owners.

### 11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](http://ti.com)のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

### 11.3 サポート・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD2E2U06DCKR	ACTIVE	SC70	DCK	3	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	1GH	<a href="#">Samples</a>
TPD2E2U06DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	DT	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TPD2E2U06 :**

- Automotive : [TPD2E2U06-Q1](#)

## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD2E2U06DCKR	SC70	DCK	3	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TPD2E2U06DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

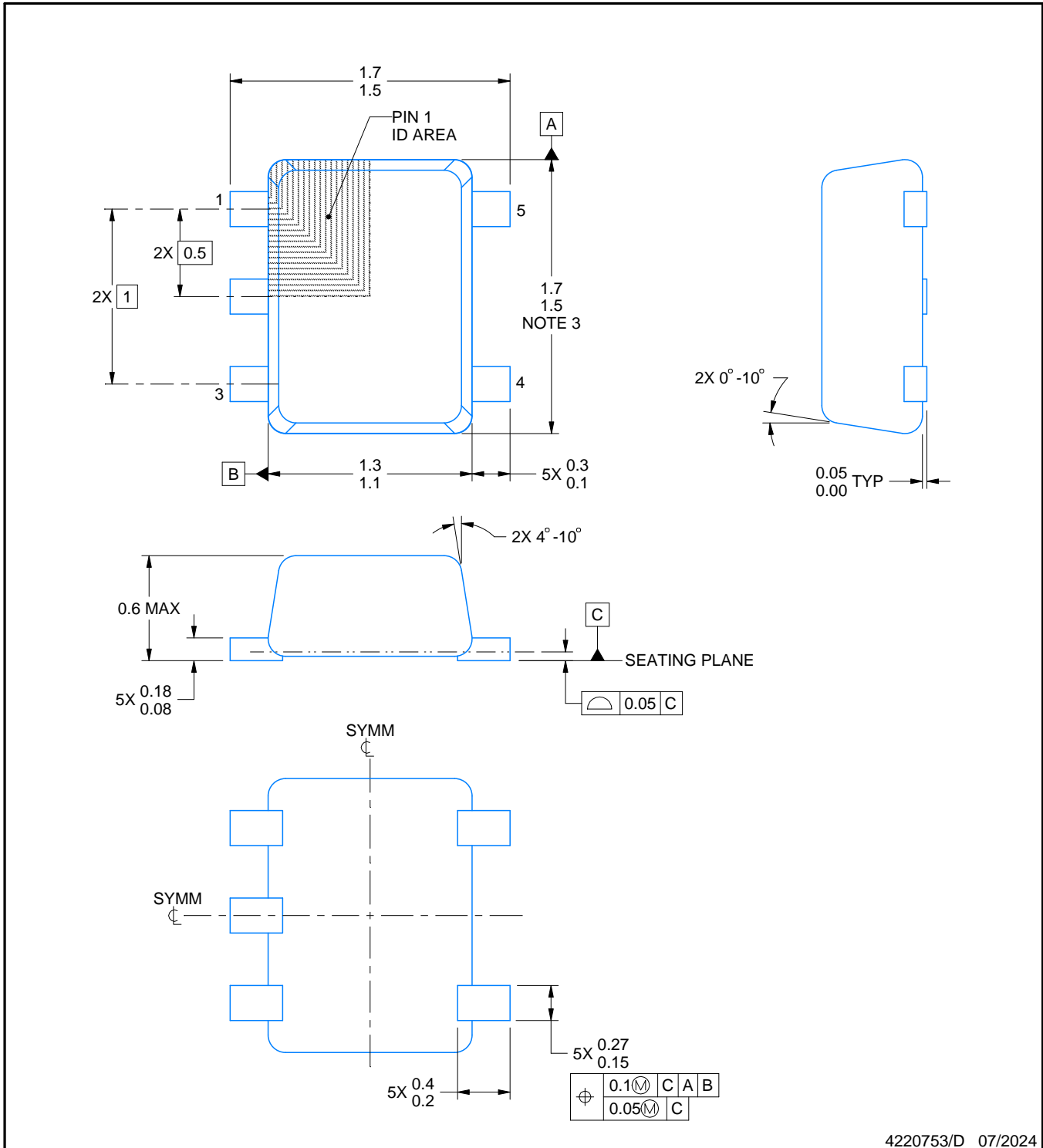
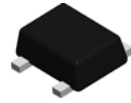
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD2E2U06DCKR	SC70	DCK	3	3000	180.0	180.0	18.0
TPD2E2U06DRLR	SOT-5X3	DRL	5	4000	183.0	183.0	20.0





4220753/D 07/2024

NOTES:

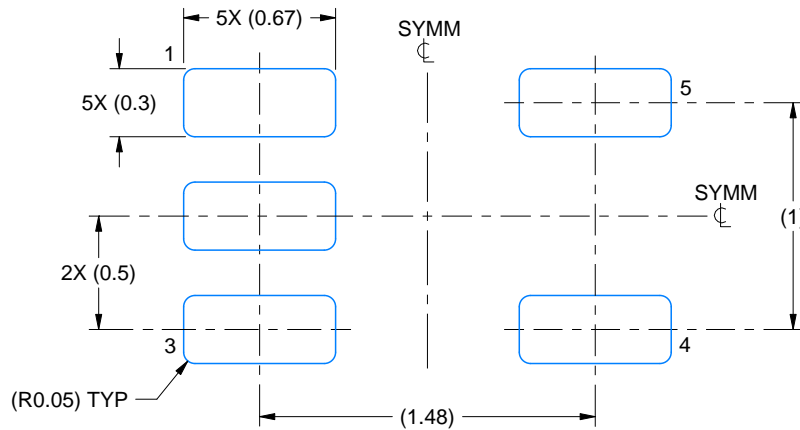
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

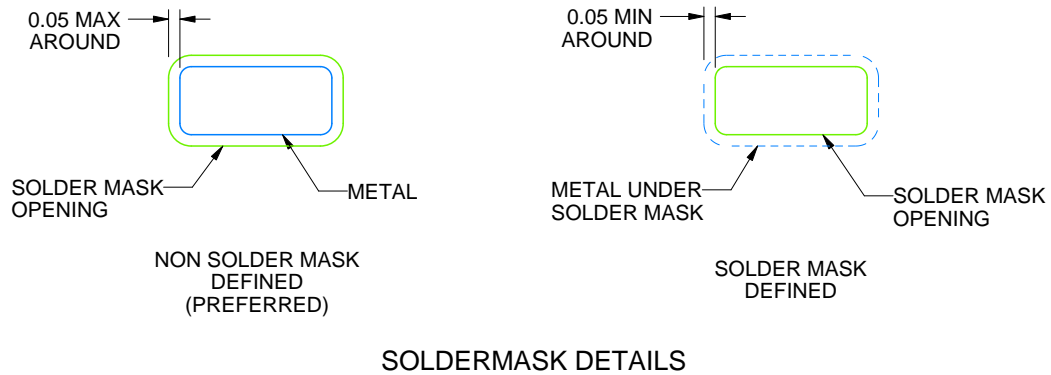
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/D 07/2024

NOTES: (continued)

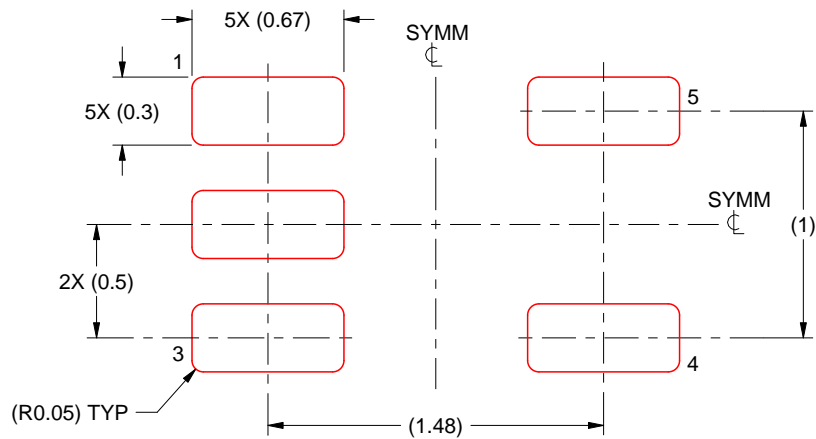
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



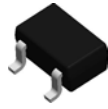
SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4220753/D 07/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

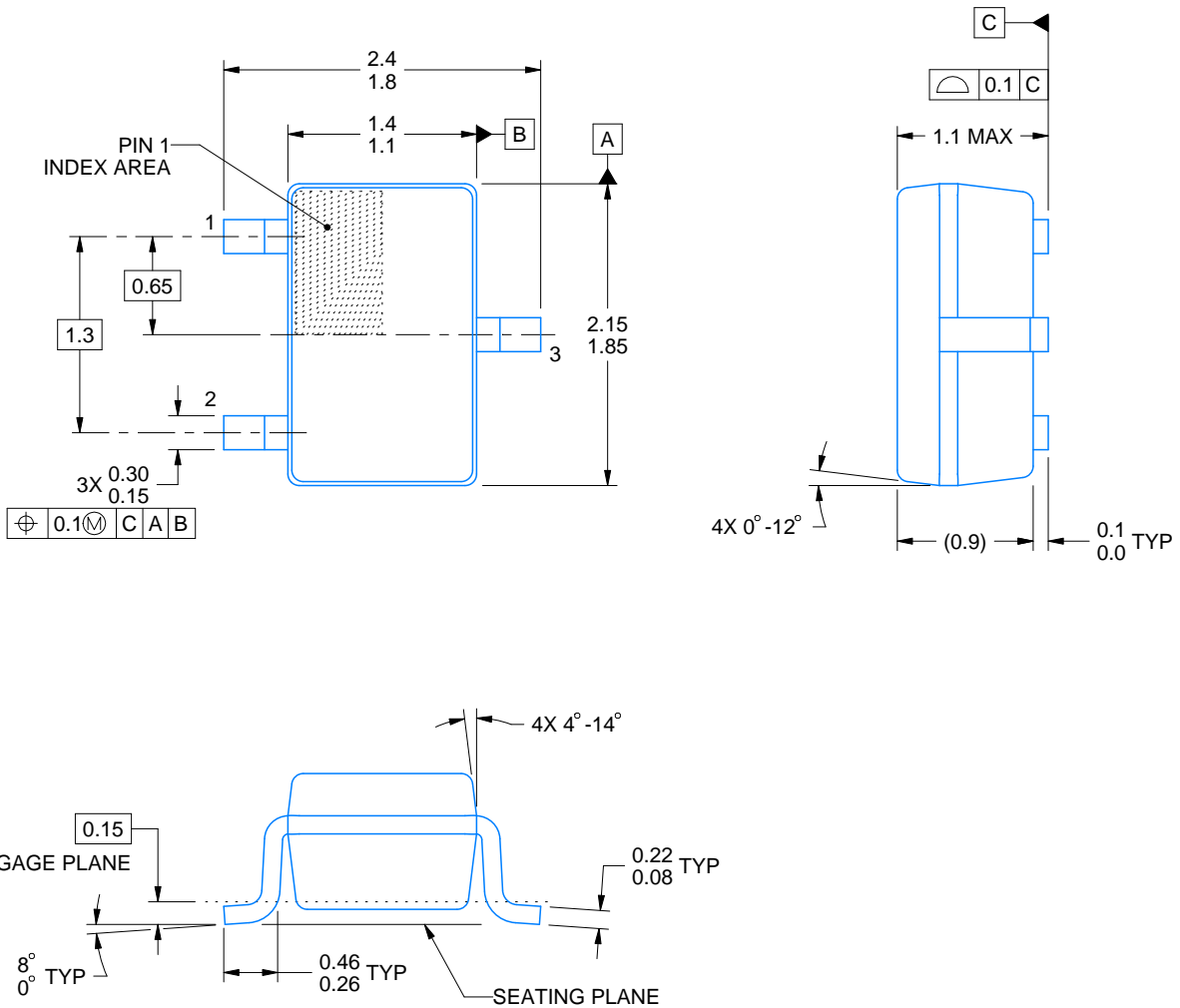
DCK0003A



# PACKAGE OUTLINE

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



4220745/E 08/2024

NOTES:

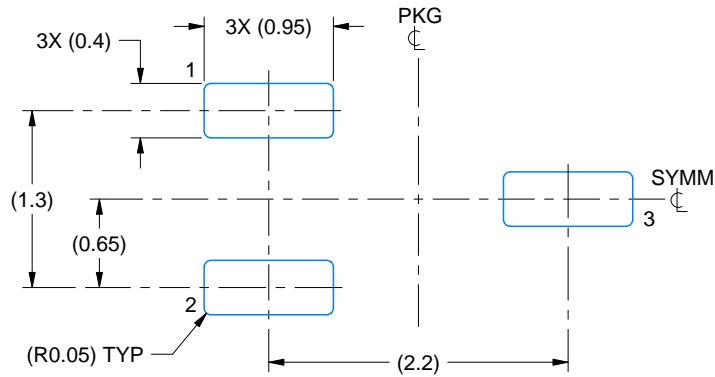
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

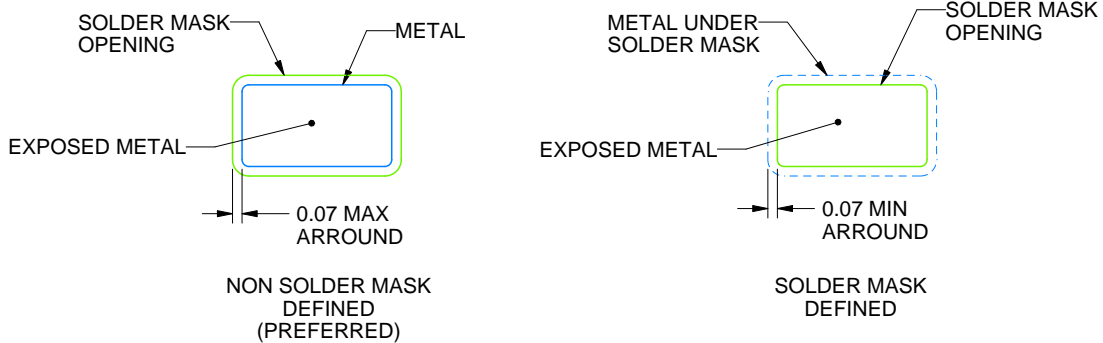
DCK0003A

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4220745/E 08/2024

NOTES: (continued)

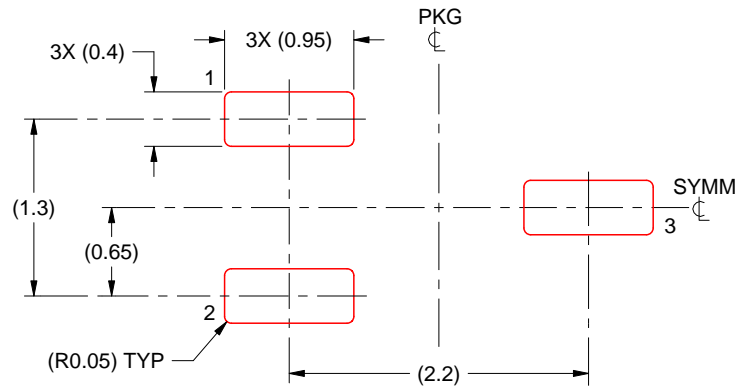
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0003A

SOT-SC70 - 1.1 max height

SMALL OUTLINE TRANSISTOR SC70



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4220745/E 08/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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