TEXAS INSTRUMENTS
TPD1E1B04
JAJSCB7A – MAY 2016 – REVISED JULY 2016

TPD1E1B04 低R_{DYN}、低クランプ電圧の1チャネルESD保護ダイオード

1 特長

- IEC 61000-4-2 レベル4 ESD保護
  - 接触放電 ±30kV
  - 空気ギャップ放電 ±30kV
- IEC 61000-4-4 EFT保護
  - 80A (5/50ns)
- IEC 61000-4-5 サージ保護
  - 6.3A (8/20µs)
- IO容量: 1pF (標準値)
- DCブレークダウン電圧: 6.4V (標準値)
- 低いリーク電流: 100nA (最大値)
- 非常に低いESDクランプ電圧
  - ±16A TLPにおいて8.5V
  - R_{DYN}: 0.15Ω
- 工業用温度範囲: -40℃～+125℃
- 業界標準の0402パッケージ

2 アプリケーション

- 最終製品
  - ウェアラブル
  - ラップトップおよびデスクトップPC
  - モバイルおよびタブレット
  - セットトップ・ボックス
  - DVRおよびNVR
  - TVおよびモニタ
  - EPOS (電子販売時点情報管理)
- インターフェイス
  - USB 2.0/1.1
  - GPIO
  - プッシュボタン
  - オーディオ

3 概要

TPD1E1B04は双方向TVS ESD保護ダイオードで、R_{DYN}とクランプ電圧が低いことが特長です。TPD1E1B04は、IEC 61000-4-2国際規格(レベル4)で規定されている最大レベルのESD耐性を備えています。

動的抵抗(0.15Ω)とクランプ電圧(16A TLPで8.5V)が非常に低いため、過渡事象に対するシステム・レベルの保護が保証されます。このデバイスのIO容量は1pFで、USB 2.0などのインターフェイスを保護するために理想的です。

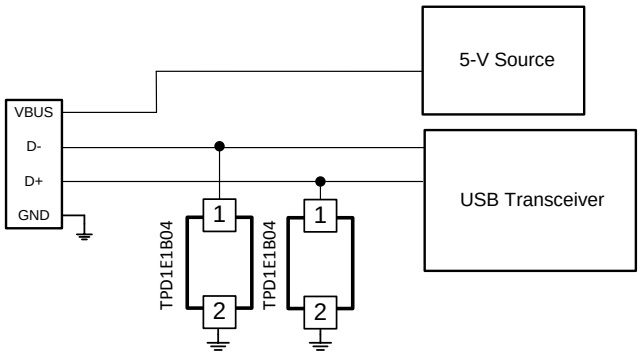
TPD1E1B04は、業界標準の0402 (DPY)パッケージで供給されます。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPD1E1B04	X1SON (2)	0.60mm×1.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なUSB 2.0アプリケーションの回路図



目次

4 改訂履歴

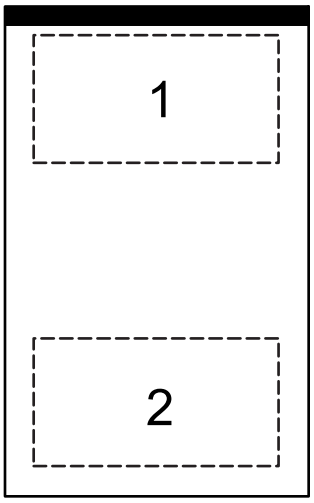
資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年5月発行のものから更新 **Page**

- デバイスのステータスを*製品プレビュー*から*量産データ*へ変更 ... 1

5 Pin Configuration and Functions

DPY Package
2-Pin X1SON
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 2 to ground
2	IO	I/O	ESD Protected Channel. If used as ESD IO, connect pin 1 to ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Electrical fast transient	IEC 61000-4-4 (5/50 ns)		80	A
Peak pulse	IEC 61000-4-5 Power (t_p - 8/20 µs)		50	W
	IEC 61000-4-5 Current (t_p - 8/20 µs)		6.3	A
T_A	Operating free-air temperature	–40	125	°C
T_{stg}	Storage temperature	–65	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings—IEC Specification

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	IEC 61000-4-2 contact discharge	±30000	V
		IEC 61000-4-2 air-gap discharge	±30000	

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IO}	Input pin voltage	–3.6	3.6	V
T_A	Operating free-air temperature	–40	125	°C

6.5 Thermal Information

THERMAL METRIC(1)		TPD1E1B04 DPY (X1SON) 2 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	420	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	169.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	276.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	122.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	157.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage	I_{IO} < 100 nA	–3.6		3.6	V
V_{BRF}	Breakdown voltage, any IO pin to GND	Measured as the maximum voltage before device snaps back into V_{HOLD} voltage		6.4		V
V_{BRR}	Breakdown voltage, GND to any IO pin	Measured as the maximum voltage before device snaps back into V_{HOLD} voltage		–6.4		V
V_{HOLD}	Holding voltage	I_{IO} = 1 mA, T_A = 25°C	5	6	6.6	V
V_{CLAMP}	Clamping voltage	I_{PP} = 1 A, TLP, from IO to GND		6.3		V
		I_{PP} = 5 A, TLP, from IO to GND		6.8		
		I_{PP} = 16 A, TLP, from IO to GND		8.5		
		I_{PP} = 1 A, TLP, from GND to IO		6.3		
		I_{PP} = 5 A, TLP, from GND to IO		6.8		
		I_{PP} = 16 A, TLP, from GND to IO		8.5		
I_{LEAK}	Leakage current, IO to GND	V_{IO} = ±2.5 V		0.2	100	nA
R_{DYN}	Dynamic resistance	IO to GND		0.15		Ω
		GND to IO		0.15		
C_L	Line capacitance	V_{IO} = 0 V, f = 1 MHz, IO to GND, T_A = 25°C		1	1.3	pF

6.7 Typical Characteristics

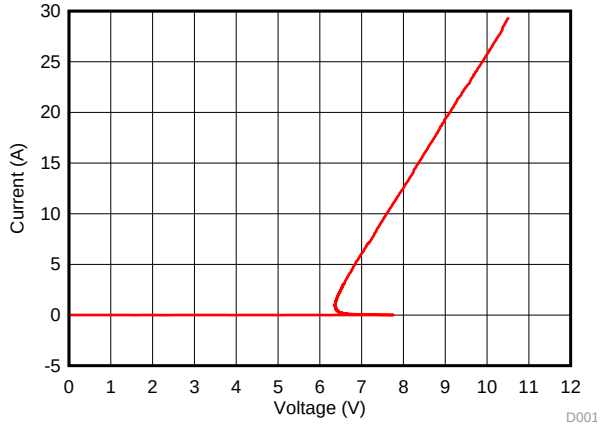


Figure 1. Positive TLP Curve

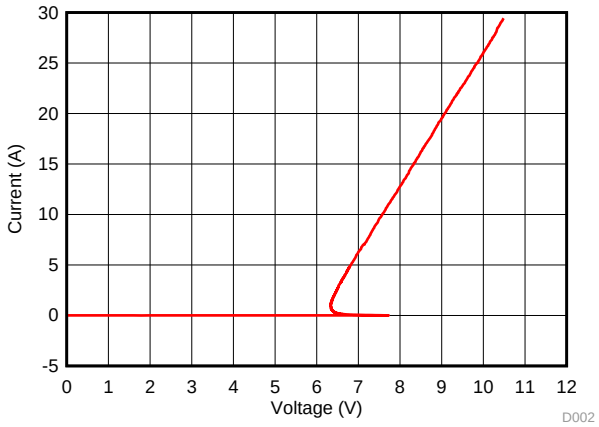


Figure 2. Negative TLP Curve

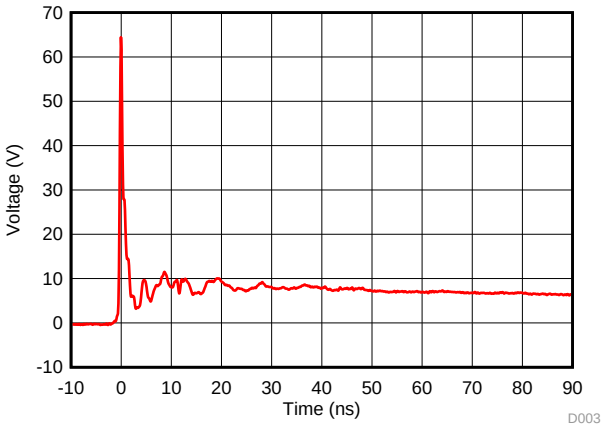


Figure 3. 8-kV IEC Waveform

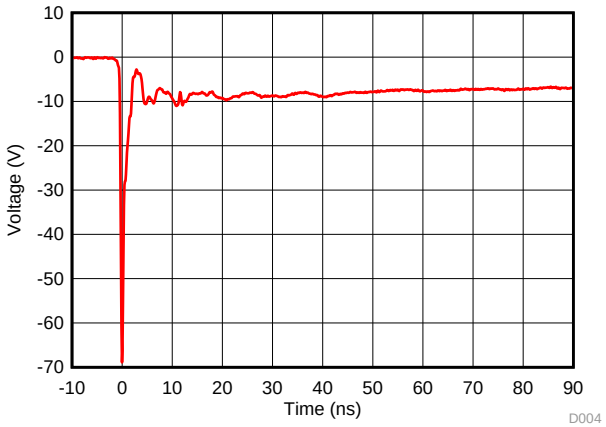


Figure 4. –8-kV IEC Waveform

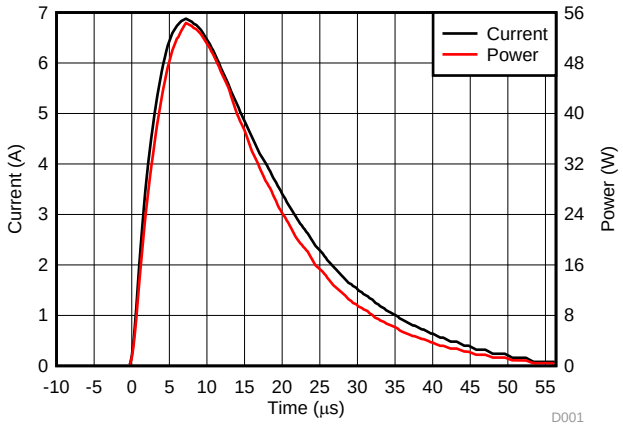


Figure 5. Surge Curve (t_p = 8/20 µs), Any IO Pin to GND

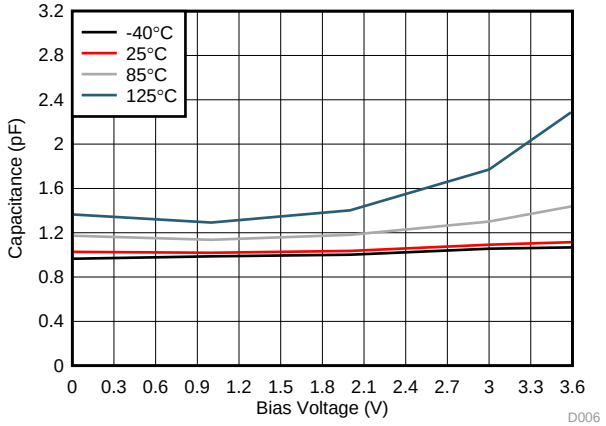


Figure 6. Capacitance vs. Bias Voltage

Typical Characteristics (continued)

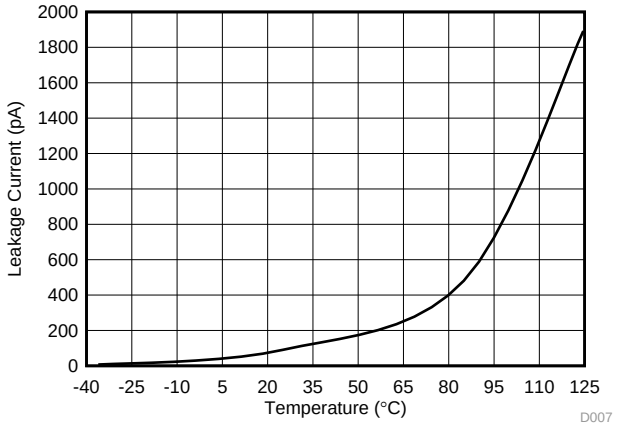


Figure 7. Leakage Current vs. Temperature

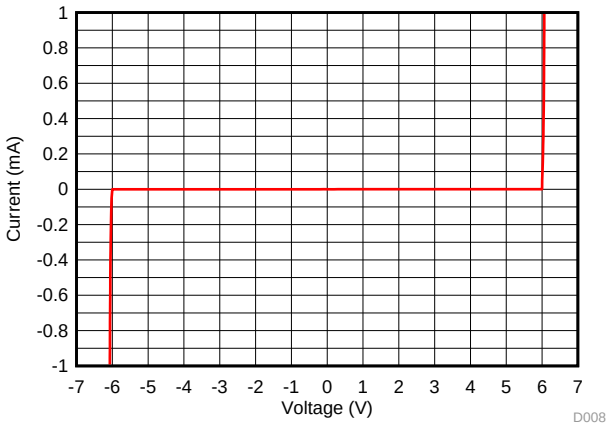


Figure 8. DC Voltage Sweep I-V Curve

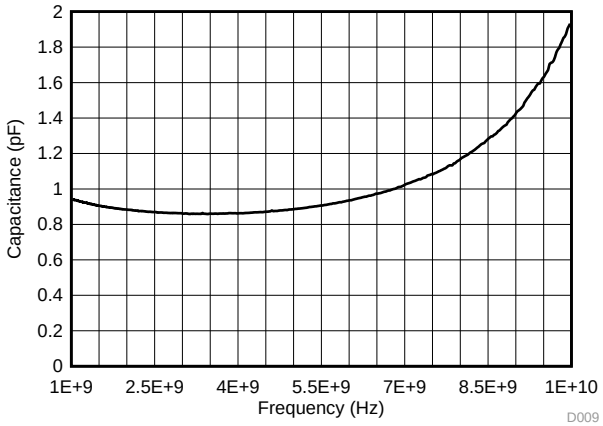


Figure 9. Capacitance vs. Frequency

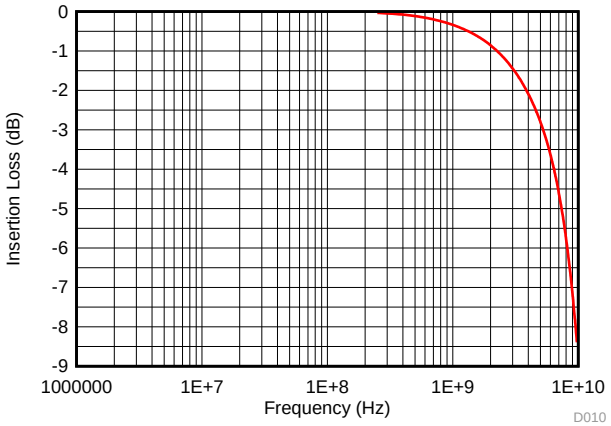


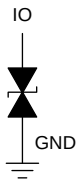
Figure 10. Insertion Loss

7 Detailed Description

7.1 Overview

The TPD1E1B04 is a bidirectional ESD Protection Diode with ultra-low clamping voltage. This device can dissipate ESD strikes above the maximum level specified by the IEC 61000-4-2 International Standard. The ultra-low clamping makes this device ideal for protecting any sensitive signal pins.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 IEC 61000-4-2 ESD Protection

The I/O pins can withstand ESD events up to ±30-kV contact and ±30-kV air gap. An ESD-surge clamp diverts the current to ground.

7.3.2 IEC 61000-4-4 EFT Protection

The I/O pins can withstand an electrical fast transient burst of up to 80 A (5/50 ns waveform, 4 kV with 50-Ω impedance). An ESD-surge clamp diverts the current to ground.

7.3.3 IEC 61000-4-5 Surge Protection

The I/O pins can withstand surge events up to 6.3 A and 50 W (8/20 µs waveform). An ESD-surge clamp diverts this current to ground.

7.3.4 IO Capacitance

The capacitance between each I/O pin to ground is 1 pF (typical) and 1.3 pF (maximum).

7.3.5 DC Breakdown Voltage

The DC breakdown voltage of each I/O pin is ±6.4 V typical. This ensures that sensitive equipment is protected from surges above the reverse standoff voltage of ±3.6 V.

7.3.6 Low Leakage Current

The I/O pins feature an low leakage current of 100 nA (maximum) with a bias of ±2.5 V.

7.3.7 Extremely Low ESD Clamping Voltage

The I/O pins feature an ESD clamp that is capable of clamping the voltage to 8.5 V (I_{PP} = 16 A).

7.3.8 Industrial Temperature Range

This device features an industrial operating range of –40°C to +125°C.

7.3.9 Industry Standard Footprint

The layout of this device makes it simple and easy to add protection to an existing layout. The packages offers flow-through routing, requiring minimal modification to an existing layout.

7.4 Device Functional Modes

The TPD1E1B04 is a passive integrated circuit that triggers when voltages are above V_{BRF} or below V_{BRR}. During ESD events, voltages as high as ±30 kV (contact or air) can be directed to ground via the internal diode network. When the voltages on the protected line fall below the trigger levels of TPD1E1B04 (usually within 10s of nano-seconds) the device reverts to passive.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPD1E1B04 is a diode type TVS which is used to provide a path to ground for dissipating ESD events on high-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a safe level for the protected IC.

8.2 Typical Application

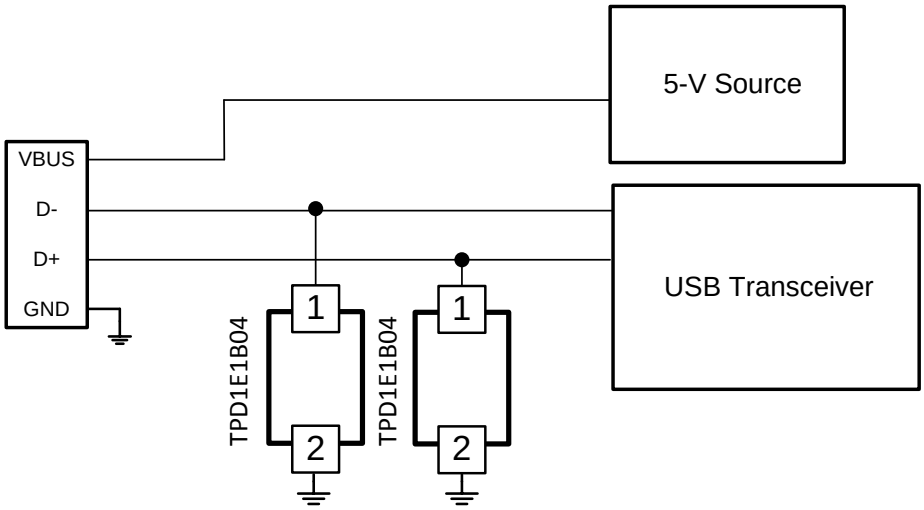


Figure 11. USB 2.0 ESD Schematic

8.2.1 Design Requirements

For this design example, two TPD1E1B04 devices are being used in a USB 2.0 application. This provides a complete ESD protection scheme.

Given the USB 2.0 application, the parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on DP-DM lines	0 V to 3.6 V
Operating frequency on DP-DM lines	up to 240 MHz

8.2.2 Detailed Design Procedure

8.2.2.1 Signal Range

The TPD1E1B04 supports signal ranges between –3.6 V and 3.6 V, which supports the USB 2.0 signal pair on the USB 2.0 application.

8.2.2.2 Operating Frequency

The TPD1E1B04 has a 1-pF (typical) capacitance, which supports the USB 2.0 data rates of 480 Mbps.

8.2.3 Application Curve

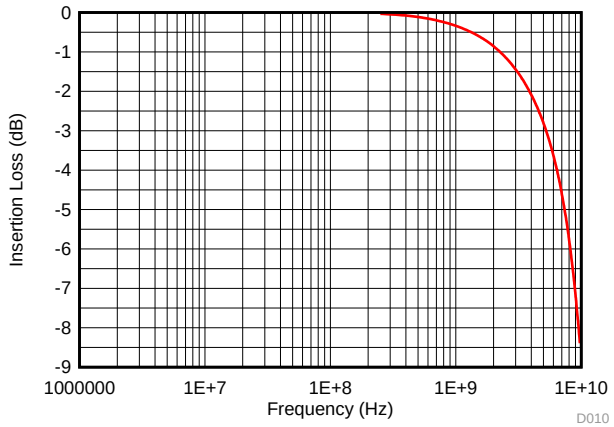


Figure 12. Insertion Loss

9 Power Supply Recommendations

The TPD1E1B04 is a passive ESD device so there is no need to power it. Take care not to violate the recommended I/O specification (–3.6 V to 3.6 V) to ensure the device functions properly.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example

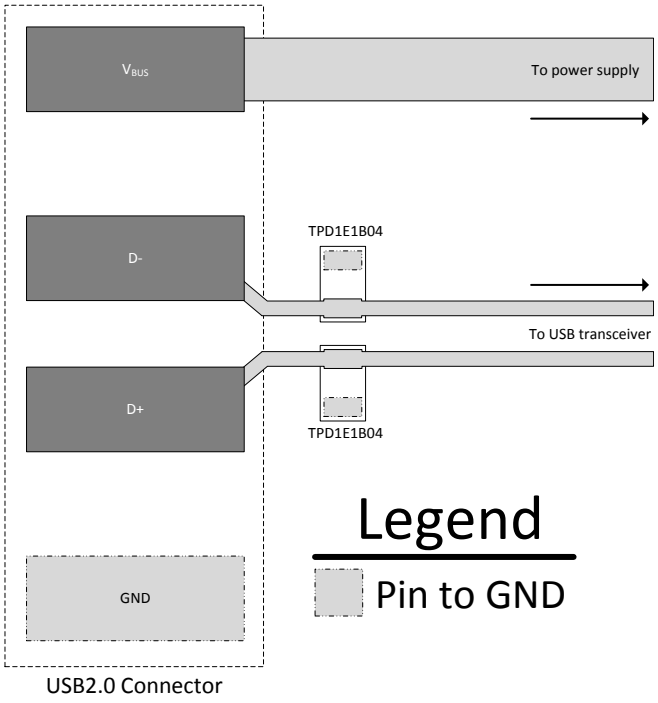


Figure 13. USB 2.0 ESD Layout

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

『TPD1E1B04評価モジュール』、SLVUAN7

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD1E1B04DPYR	ACTIVE	X1SON	DPY	2	10000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	4X	Samples
TPD1E1B04DPYT	ACTIVE	X1SON	DPY	2	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	4X	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

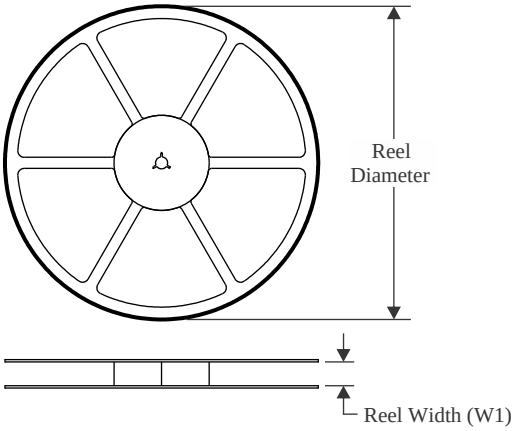
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

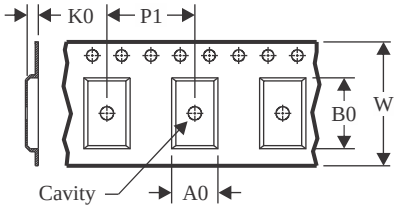
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

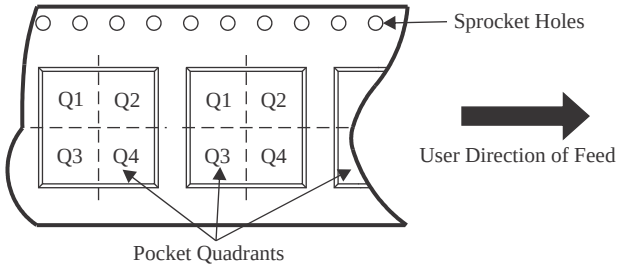


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

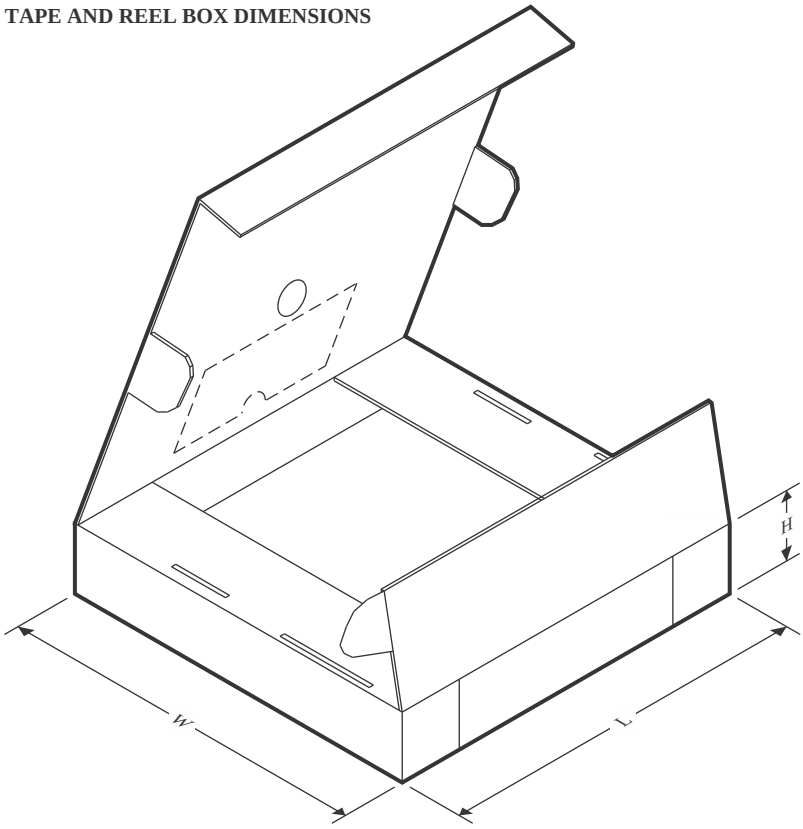
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD1E1B04DPYR	X1SON	DPY	2	10000	180.0	8.4	0.67	1.15	0.46	2.0	8.0	Q2
TPD1E1B04DPYT	X1SON	DPY	2	250	180.0	9.5	0.66	1.15	0.66	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD1E1B04DPYR	X1SON	DPY	2	10000	210.0	185.0	35.0
TPD1E1B04DPYT	X1SON	DPY	2	250	184.0	184.0	19.0

GENERIC PACKAGE VIEW

DPY 2

X1SON - 0.45 mm max height

1 x 0.6 mm

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

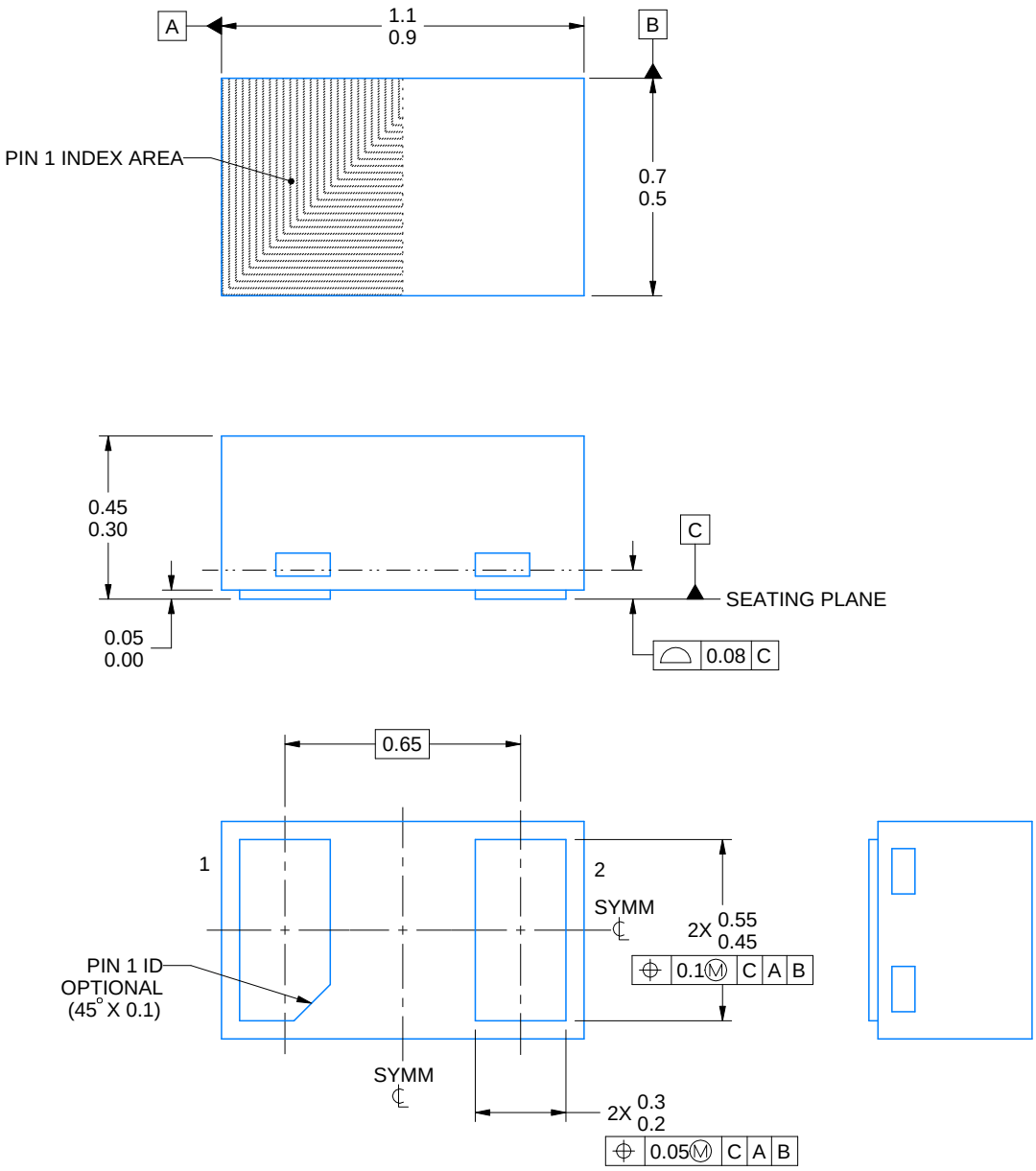
4231484/A

PACKAGE OUTLINE

DPY0002A

X1SON - 0.45 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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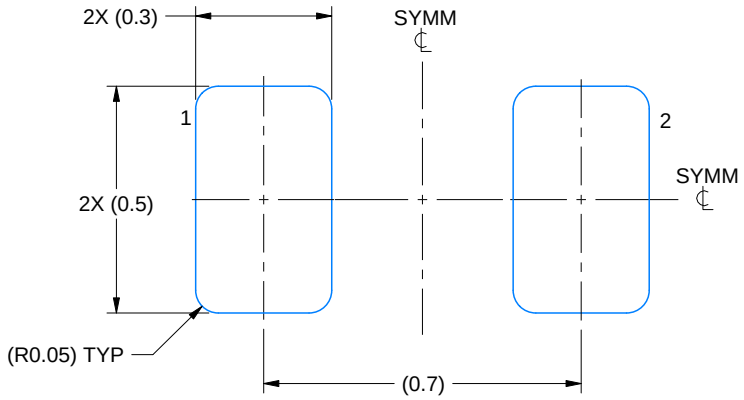
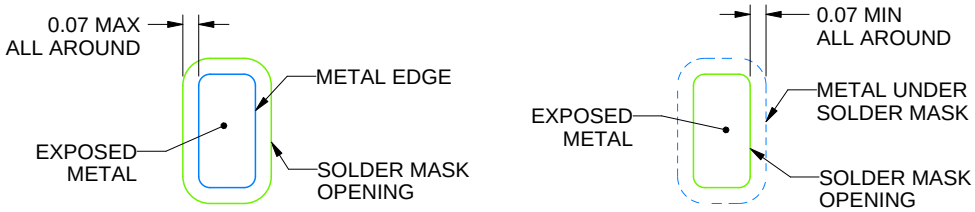
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:60X



SOLDER MASK DETAILS

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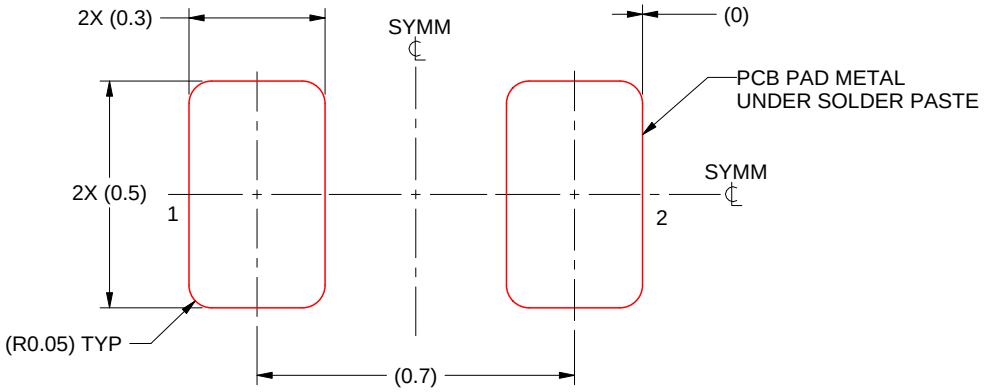
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:60X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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