TEXAS INSTRUMENTS

TPA3255

JAJSD69A – FEBRUARY 2016 – REVISED OCTOBER 2016

TPA3255 315Wステレオ、600Wモノラル、PurePath™ Ultra HDアナログ入力

1 特長

- 差動アナログ入力
- 10%THD+N時の総出力電力
  - BTL構成で4Ω へ315W (ステレオ)
  - BTL構成で8Ω へ185W (ステレオ)
  - PBTL構成で2Ω へ600W (モノラル)
- 1%THD+N時の総出力電力
  - BTL構成で4Ω へ260W (ステレオ)
  - BTL構成で8Ω へ150W (ステレオ)
  - PBTL構成で2Ω へ480W (モノラル)
- 高度な統合フィードバック設計と、高速なゲート・ドライバ・エラー訂正
  (PurePath™ Ultra-HD)
  - 最高100kHzの信号帯域幅によりHDソースからの高周波数のコンテンツに対応
  - 非常に低いTHD+N: 4Ω へ1Wで0.006%、クリッピングへ0.01%未満
  - PSRR 65dB超(BTL、1kHz、入力信号なし)
  - 出力ノイズ85µV未満(Aウェイト)
  - SNR 111dB超(Aウェイト)
- 複数の構成が可能:
  - ステレオ、モノラル、2.1、4xSE
- 開始時と停止時にクリック音やポップ音が発生しない
- 90%効率のClass-D動作(4Ω)
- 18V～53.5Vの広い電源電圧範囲での動作
- 自己保護設計(低電圧、過熱、クリッピング、短絡保護を含む)とエラー報告機能
- 推奨システム設計で使用時にEMI準拠

2 アプリケーション

- Blu-Ray Disc™/ DVDレシーバ
- ハイエンドHTiBシステム
- AVレシーバ
- ハイエンド・サウンドバー
- ミニ・コンポ・システム
- アクティブ・スピーカーおよびサブウーファー

3 概要

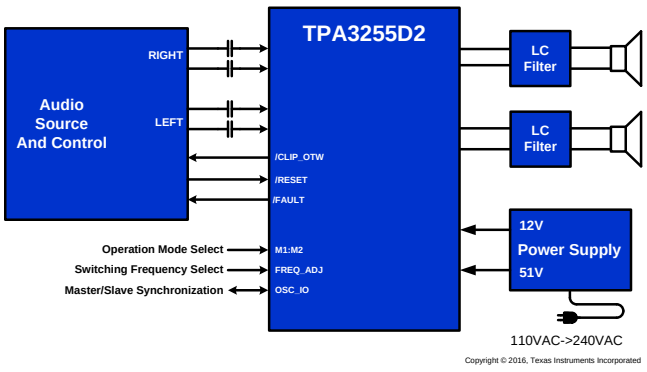
TPA3255は高性能のClass-Dパワー・アンプで、最高のサウンド品質をClass-Dの効率で実現します。高度な統合フィードバック設計と、独自の高速ゲート・ドライバ・エラー訂正機能(PurePath™ Ultra-HD)があります。このテクノロジにより、音声帯域全体にわたる歪みが非常に低い、優れたオーディオ品質を実現しています。このデバイスはADモードで動作し、4Ω負荷へ10% THDで最大315×2W、8Ω負荷へ最大2×150W (クリッピングなし)を駆動でき、2つのVRMSアナログ入力・インターフェイスが搭載されており、TIのPCM5242などの高性能DACとシームレスに動作します。非常に優れたオーディオ性能に加えて、TPA3255は高い電力効率と、2.5Wという非常に低いパワー段のアイドル損失も実現しています。これらは、85mΩ MOSFETの使用と、最適化されたゲート・ドライバ方式により、標準的なディスクリート実装よりもはるかに低いアイドル損失を実現することで達成されています。

製品情報(1)

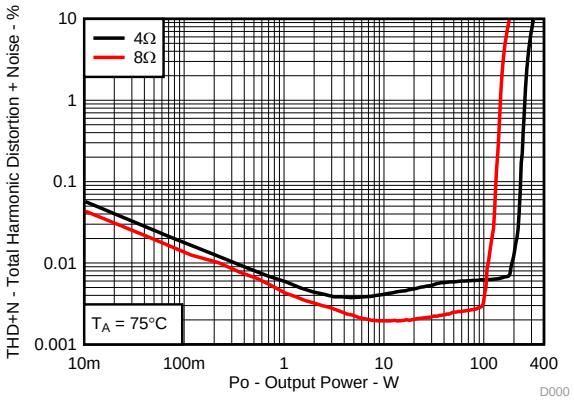
型番	パッケージ	本体サイズ(公称)
TPA3255	HTSSOP (44)	6.10mm×14.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



全高調波歪み



目次

4 改訂履歴

2016年2月発行のものから更新 **Page**

- デバイスのステータスを製品プレビューから量産データへ変更 ... 1

5 Device Comparison Table

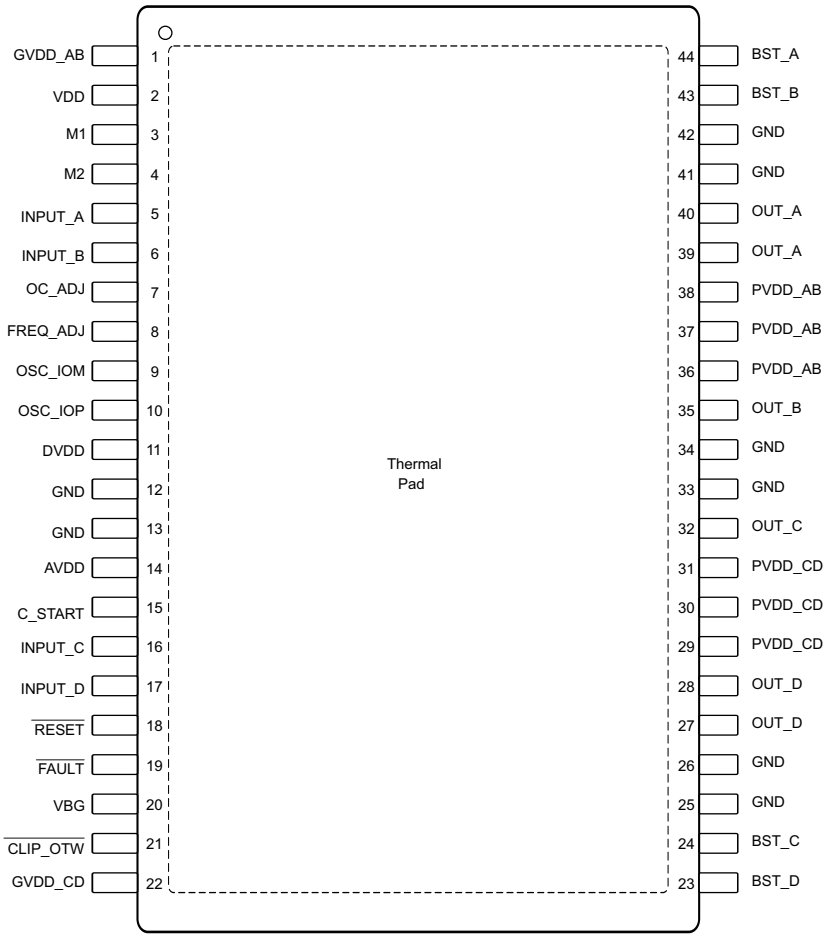
DEVICE NAME	DESCRIPTION
TPA3244	40-W Stereo, 100-W peak PurePath™ Ultra-HD Pad Down Class-D Amplifier
TPA3245	100-W Stereo, 200-W Mono PurePath™ Ultra-HD Analog-Input Class-D Amplifier
TPA3250	70-W Stereo, 130-W peak PurePath™ Ultra-HD Pad Down Class-D Amplifier
TPA3251	175-W Stereo, 350-W Mono PurePath™ Ultra-HD Analog-Input Class-D Amplifier

6 Pin Configuration and Functions

The TPA3255 is available in a thermally enhanced TSSOP package.

The package type contains a PowerPAD™ that is located on the top side of the device for convenient thermal coupling to the heat sink.

DDV Package
HTSSOP 44-Pin
(Top View)



Pin Functions

NAME	NO.	I/O	DESCRIPTION
AVDD	14	P	Internal voltage regulator, analog section
BST_A	44	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_A required.
BST_B	43	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_B required.
BST_C	24	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_C required.
BST_D	23	P	HS bootstrap supply (BST), external 0.033 μF capacitor to OUT_D required.
$\overline{\text{CLIP\_OTW}}$	21	O	Clipping warning and Over-temperature warning; open drain; active low. Do not connect if not used.
C_START	15	O	Startup ramp, requires a charging capacitor to GND
DVDD	11	P	Internal voltage regulator, digital section
$\overline{\text{FAULT}}$	19	O	Shutdown signal, open drain; active low. Do not connect if not used.
FREQ_ADJ	8	O	Oscillator freqency programming pin
GND	12, 13, 25, 26, 33, 34, 41, 42	P	Ground
GVDD_AB	1	P	Gate-drive voltage supply; AB-side, requires 0.1 μF capacitor to GND
GVDD_CD	22	P	Gate-drive voltage supply; CD-side, requires 0.1 μF capacitor to GND
INPUT_A	5	I	Input signal for half bridge A
INPUT_B	6	I	Input signal for half bridge B
INPUT_C	16	I	Input signal for half bridge C
INPUT_D	17	I	Input signal for half bridge D
M1	3	I	Mode selection 1 (LSB)
M2	4	I	Mode selection 2 (MSB)
OC_ADJ	7	I/O	Over-Current threshold programming pin
OSC_IOM	9	I/O	Oscillator synchronization interface. Do not connect if not used.
OSC_IOP	10	O	Oscillator synchronization interface. Do not connect if not used.
OUT_A	39, 40	O	Output, half bridge A
OUT_B	35	O	Output, half bridge B
OUT_C	32	O	Output, half bridge C
OUT_D	27, 28	O	Output, half bridge D
PVDD_AB	36, 37, 38	P	PVDD supply for half-bridge A and B
PVDD_CD	29, 30, 31	P	PVDD supply for half-bridge C and D
$\overline{\text{RESET}}$	18	I	Device reset Input; active low
VDD	2	P	Power supply for internal voltage regulator requires a 10-μF capacitor with a 0.1-μF capacitor to GND for decoupling.
VBG	20	P	Internal voltage reference requires a 1-μF capacitor to GND for decoupling.
PowerPad™		P	Ground, connect to grounded heat sink

Table 1. Mode Selection Pins

MODE PINS(1)		INPUT MODE(2)	OUTPUT CONFIGURATION	DESCRIPTION		
M2	M1					
0	0	2N + 1	2 × BTL	Stereo BTL output configuration		
0	1	2N/1N + 1	1 x BTL + 2 x SE	2.1 BTL + SE mode. Channel AB: BTL, channel C + D: SE		
1	0	2N + 1			INPUT_C	INPUT_D
			1 x PBTL	Parallelled BTL configuration. Connect INPUT_C and INPUT_D to GND.(1)	0	0
			1 x BTL	Mono BTL configuration. BTL channel AB active, channel CD not switching. Connect INPUT_C to DVDD and INPUT_D to GND.(1)	1	0
1	1	1N +1	4 x SE	Single ended output configuration		

(1) 1 refers to logic high (DVDD level), 0 refers to logic low (GND).
(2) 2N refers to differential input signal, 1N refers to single ended input signal. +1 refers to number of logic control (RESET) input pins.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage	BST_X to GVDD_X(2)	–0.3	69	V
	VDD to GND	–0.3	13.2	V
	GVDD_X to GND(2)	–0.3	13.2	V
	PVDD_X to GND(2)	–0.3	69	V
	DVDD to GND	–0.3	4.2	V
	AVDD to GND	–0.3	8.5	V
	VBG to GND	-0.3	4.2	V
Interface pins	OUT_X to GND(2)	–0.3	69	V
	BST_X to GND(2)	–0.3	81.5	V
	OC_ADJ, M1, M2, OSC_IOP, OSC_IOM, FREQ_ADJ, C_START, to GND	–0.3	4.2	V
	$\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, $\overline{\text{CLIP\_OTW}}$ to GND	–0.3	4.2	V
	INPUT_X to GND	–0.3	7	V
	Continuous sink current, $\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, $\overline{\text{CLIP\_OTW}}$ to GND		9	mA
T_J	Operating junction temperature range	0	150	°C
T_{stg}	Storage temperature range	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These voltages represents the DC voltage + peak AC waveform measured at the terminal of the device in all conditions.

7.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
PVDD_x	Half-bridge supply	DC supply voltage, R_L = 4Ω	18	51	53.5	V
		DC supply voltage, R_L ≥ 6Ω (1)	18	53.5	56.5	
GVDD_x	Supply for logic regulators and gate-drive circuitry	DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage	DC supply voltage	10.8	12	13.2	V
R_L(BTL)	Load impedance	Output filter inductance within recommended value range	3.4	4		Ω
R_L(SE)			1.7	3		
R_L(PBTL)			1.7	2		
L_{OUT}(BTL)	Output filter inductance	Minimum output inductance at I_{OC}	5			μH
L_{OUT}(SE)			5			
L_{OUT}(PBTL)			5			
F_{PWM}	PWM frame rate selectable for AM interference avoidance; 1% Resistor tolerance	Nominal	430	450	470	kHz
		AM1	475	500	525	
		AM2	575	600	625	
$R_{(FREQ\_ADJ)}$	PWM frame rate programming resistor	Nominal; Master mode	29.7	30	30.3	kΩ
		AM1; Master mode	19.8	20	20.2	
		AM2; Master mode	9.9	10	10.1	
C_{PVDD}	PVDD close decoupling capacitors			1		μF
R_{OC}	Over-current programming resistor	Resistor tolerance = 5%, R_L = 4Ω	22		30	kΩ
		Resistor tolerance = 5%, R_L ≥ 6Ω, PVDD = 53.5V (1)		30		
$R_{OC(LATCHED)}$	Over-current programming resistor	Resistor tolerance = 5%, R_L = 4Ω	47		64	kΩ
		Resistor tolerance = 5%, R_L ≥ 6Ω, PVDD = 53.5V (1)		64		
$V_{(FREQ\_ADJ)}$	Voltage on FREQ_ADJ pin for slave mode operation	Slave mode		3.3		V
T_J	Junction temperature		0		125	°C

(1) For load impedance ≥ 6Ω PVDD can be increased, provided a reduced over-current threshold is set

7.4 Thermal Information

THERMAL METRIC (1)		TPA3255 DDV 44-PINS HTSSOP		UNIT
		JEDEC STANDARD 4 LAYER PCB	FIXED 85°C HEATSINK TEMPERATURE (2)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	50.7	2.4 (2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.36	0.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	24.4	n/a	
ψ_{JT}	Junction-to-top characterization parameter	0.19	0.5	
ψ_{JB}	Junction-to-board characterization parameter	24.2	n/a	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Thermal data are obtained with 85°C heat sink temperature using thermal compound with 0.7W/mK thermal conductivity and 2mil thickness. In this model heat sink temperature is considered to be the ambient temperature and only path for dissipation is to the heatsink.

7.5 Electrical Characteristics

PVDD_X = 51 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 450 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
DVDD	Voltage regulator, only used as reference node	VDD = 12 V	3	3.3	3.6	V
AVDD	Voltage regulator, only used as reference node	VDD = 12 V		7.75		V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		30		mA
		Idle, reset mode		14		
I_{GVDD_X}	Gate-supply current per full-bridge	50% duty cycle		44		mA
		Reset mode		5		
I_{PVDD_X}	PVDD idle current per full bridge	50% duty cycle with recommended output filter		24		mA
		Reset mode, No switching		5		mA
		VDD = 0V, GVDD_X = 0V		1.25		mA
ANALOG INPUTS						
R_{IN}	Input resistance			20		kΩ
V_{IN}	Maximum input voltage swing, peak - peak				7	V
I_{IN}	Maximum input current				1	mA
G	Inverting voltage Gain	V_{OUT}/V_{IN}		21.5		dB
OSCILLATOR						
$f_{OSC(IO+)}$	Nominal, Master Mode	F_{PWM} × 6	2.58	2.7	2.82	MHz
	AM1, Master Mode		2.85	3	3.15	
	AM2, Master Mode		3.45	3.6	3.75	
V_{IH}	High level input voltage		1.86			V
V_{IL}	Low level input voltage				1.45	V
OUTPUT-STAGE MOSFETs						
$R_{DS(on)}$	Drain-to-source resistance, low side (LS)	T_J = 25°C, Includes metallization resistance, GVDD = 12 V		85	100	mΩ
	Drain-to-source resistance, high side (HS)			85	100	mΩ
I/O PROTECTION						
$V_{uvp,VDD,GVDD}$	Undervoltage protection limit, GVDD_x and VDD			8.7		V
$V_{uvp,VDD,\ GVDD,hyst}$ (1)				0.6		V
$V_{uvp,PVDD}$	Undervoltage protection limit, PVDD_x			14.5		V
$V_{uvp,PVDD,hyst}$ (1)				1.4		V
OTW	Overtemperature warning, $\overline{\text{CLIP\_OTW}}$(1)		110	120	130	°C
OTW_{hyst} (1)	Temperature drop needed below OTW temperature for $\overline{\text{CLIP\_OTW}}$ to be inactive after OTW event.			20		°C
OTE(1)	Overtemperature error		140	150	160	°C
OTE_{hyst} (1)	A reset needs to occur for $\overline{\text{FAULT}}$ to be released following an OTE event			15		°C
OTE-$OTW_{(differential)}$ (1)	OTE-OTW differential			30		°C
OLPC	Overload protection counter	f_{PWM} = 450 kHz (1024 PWM cycles)		2.3		ms
I_{OC}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 22 kΩ		17		A
		Resistor – programmable, nominal peak current in 1Ω load, R_{OCP} = 30 kΩ		13		
$I_{OC(LATCHED)}$	Overcurrent limit protection	Resistor – programmable, peak current in 1Ω load, R_{OCP} = 47kΩ		17		A
		Resistor – programmable, peak current in 1Ω load, R_{OCP} = 64kΩ		13		
I_{DCspkr}	DC Speaker Protection Current Threshold	BTL current imbalance threshold		1.5		A
I_{OCT}	Overcurrent response time	Time from switching transition to flip-state induced by overcurrent.		150		ns

(1) Specified by design.

Electrical Characteristics (continued)

PVDD_X = 51 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 450 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PD}	Output pulldown current of each half	Connected when $\overline{RESET}$ is active to provide bootstrap charge. Not used in SE mode.		3		mA
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High level input voltage	M1, M2, OSC_IOP, OSC_IOM, RESET	1.9			V
V_{IL}	Low level input voltage				0.8	V
I_{lkg}	Input leakage current				100	μA
OTW/SHUTDOWN (FAULT)						
R_{INT_PU}	Internal pullup resistance, $\overline{CLIP\_OTW}$ to DVDD, $\overline{FAULT}$ to DVDD		20	26	32	kΩ
V_{OH}	High level output voltage	Internal pullup resistor	3	3.3	3.6	V
V_{OL}	Low level output voltage	I_O = 4 mA		10	500	mV
Device fanout	$\overline{CLIP\_OTW}$, $\overline{FAULT}$	No external pullup		30		devices

7.6 Audio Characteristics (BTL)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 51 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 450 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 μH, C_{DEM} = 1 μF, mode = 00, AES17 + AUX-0025 measurement filters,unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 4 Ω, 10% THD+N		315		W
		R_L = 6 Ω, 10% THD+N, PVDD = 53.5V		250		
		R_L = 8 Ω, 10% THD+N, PVDD = 53.5V		195		
		R_L = 4 Ω, 1% THD+N		255		
		R_L = 6 Ω, 1% THD+N, PVDD = 53.5V		200		
		R_L = 8 Ω, 1% THD+N, PVDD = 53.5V		155		
THD+N	Total harmonic distortion + noise	1 W		0.006%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		85		μV
$\|V_{OS}\|$	Output offset voltage	Inputs AC coupled to GND		15	60	mV
SNR	Signal-to-noise ratio (1)			112		dB
DNR	Dynamic range			113		dB
P_{idle}	Power dissipation due to Idle losses (I_{PVDD})	P_O = 0, 4 channels switching (2)		2.5		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

7.7 Audio Characteristics (SE)

PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 51 V, GVDD_X = 12 V, R_L = 2 Ω, f_S = 450 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 15 μH, C_{DEM} = 1 μF, MODE = 11, AES17 + AUX-0025 measurement filters, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N		148		W
		R_L = 3 Ω, 10% THD+N, PVDD = 53.5V		120		
		R_L = 4 Ω, 10% THD+N, PVDD = 53.5V		95		
		R_L = 2 Ω, 1% THD+N		120		
		R_L = 3 Ω, 1% THD+N, PVDD = 53.5V		98		
		R_L = 4 Ω, 1% THD+N, PVDD = 53.5V		77		
THD+N	Total harmonic distortion + noise	1 W		0.04%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		160		μV
SNR	Signal to noise ratio(1)	A-weighted		101		dB
DNR	Dynamic range	A-weighted		101		dB
P_{idle}	Power dissipation due to idle losses (IPVDD)	P_O = 0, 4 channels switching(2)		2		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

7.8 Audio Characteristics (PBTL)

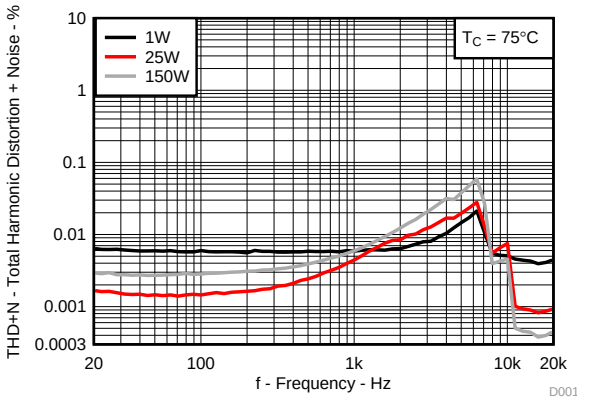
PCB and system configuration are in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 51 V, GVDD_X = 12 V, R_L = 2 Ω, f_S = 450 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 μH, C_{DEM} = 1 μF, MODE = 10, AES17 + AUX-0025 measurement filters, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 2 Ω, 10% THD+N		605		W
		R_L = 3 Ω, 10% THD+N, PVDD = 53.5V		500		
		R_L = 4 Ω, 10% THD+N, PVDD = 53.5V		390		
		R_L = 2 Ω, 1% THD+N		495		
		R_L = 3 Ω, 1% THD+N, PVDD = 53.5V		405		
		R_L = 4 Ω, 1% THD+N, PVDD = 53.5V		315		
THD+N	Total harmonic distortion + noise	1 W		0.008%		
V_n	Output integrated noise	A-weighted, AES17 filter, Input Capacitor Grounded		70		μV
SNR	Signal to noise ratio(1)	A-weighted		114		dB
DNR	Dynamic range	A-weighted		114		dB
P_{idle}	Power dissipation due to idle losses (IPVDD)	P_O = 0, 4 channels switching(2)		2.5		W

(1) SNR is calculated relative to 1% THD+N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

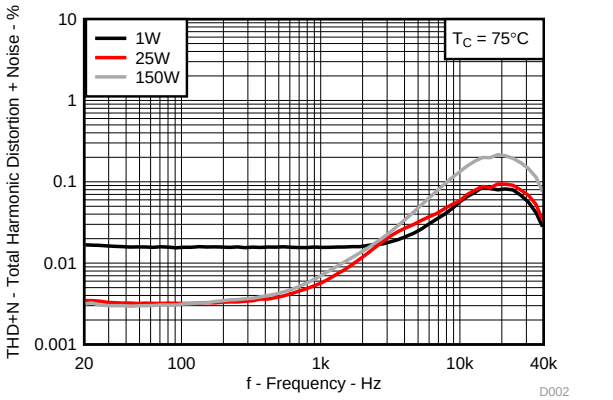
7.9 Typical Characteristics, BTL Configuration

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 51 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 450 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, mode = 00, AES17 + AUX-0025 measurement filters,unless otherwise noted.



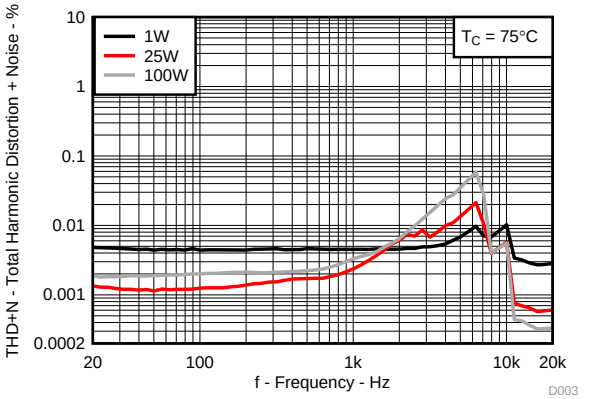
R_L = 4 Ω P = 1W, 25W, 150W T_C = 75°C PVDD = 51V

Figure 1. Total Harmonic Distortion+Noise vs Frequency



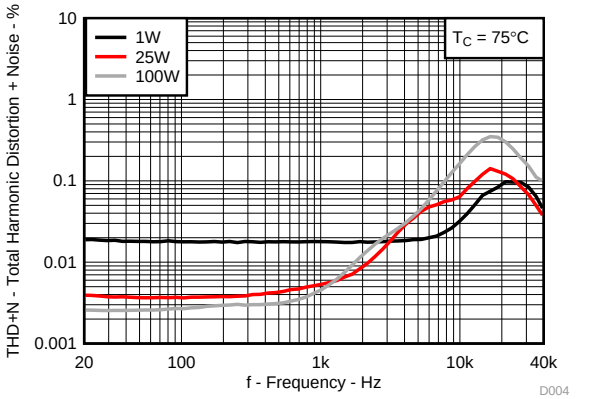
R_L = 4 Ω P = 1W, 25W, 150W T_C = 75°C AUX-0025 filter, 80 kHz analyzer BW PVDD = 51V

Figure 2. Total Harmonic Distortion+Noise vs Frequency



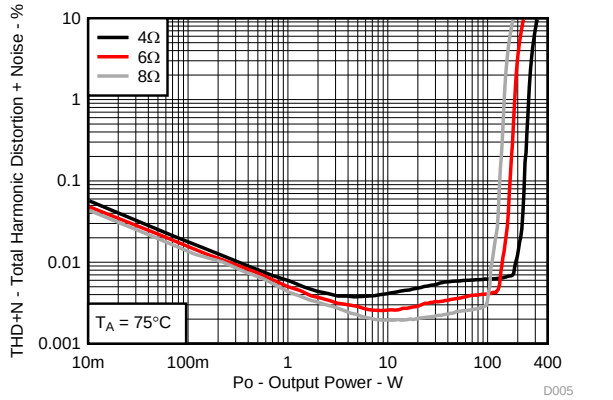
R_L = 8 Ω P = 1W, 25W, 100W T_C = 75°C PVDD = 53.5V

Figure 3. Total Harmonic Distortion+Noise vs Frequency



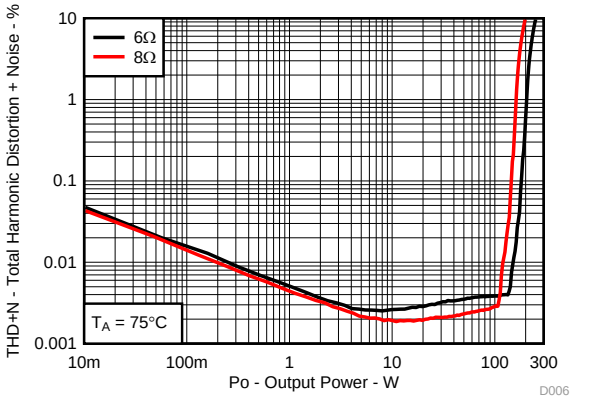
R_L = 8 Ω P = 1W, 25W, 100W T_C = 75°C AUX-0025 filter, 80 kHz analyzer BW PVDD = 53.5V

Figure 4. Total Harmonic Distortion+Noise vs Frequency



R_L = 4 Ω, 6 Ω, 8 Ω T_C = 75°C PVDD = 51V

Figure 5. Total Harmonic Distortion + Noise vs Output Power

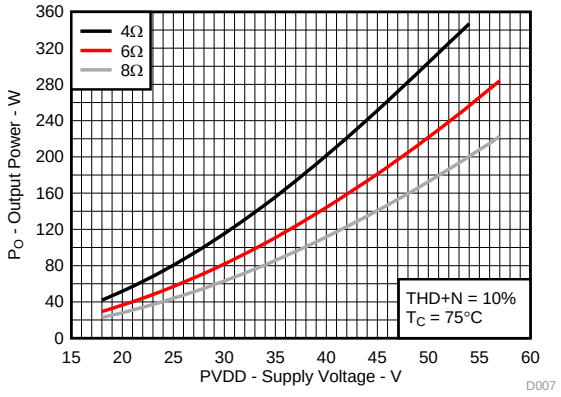


R_L = 6 Ω, 8 Ω T_C = 75°C PVDD = 53.5V

Figure 6. Total Harmonic Distortion + Noise vs Output Power

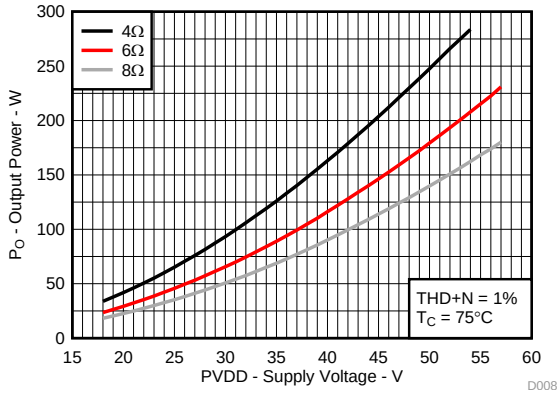
Typical Characteristics, BTL Configuration (continued)

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 51 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 450 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, mode = 00, AES17 + AUX-0025 measurement filters,unless otherwise noted.



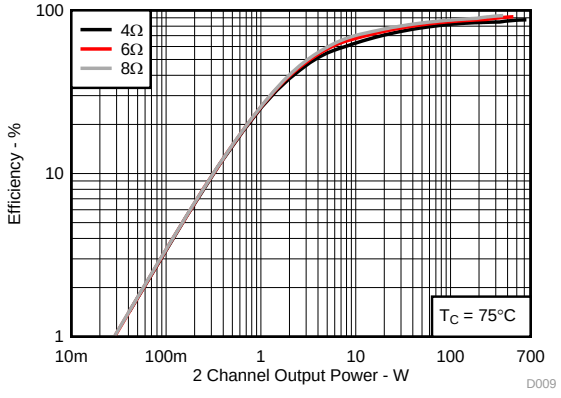
R_L = 4 Ω, 6 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 7. Output Power vs Supply Voltage



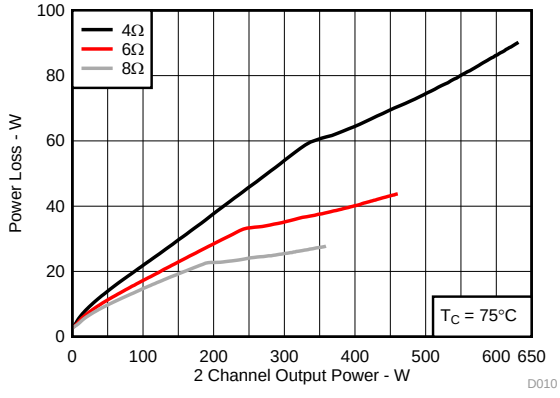
R_L = 4 Ω, 6 Ω, 8 Ω THD+N = 1% T_C = 75°C

Figure 8. Output Power vs Supply Voltage



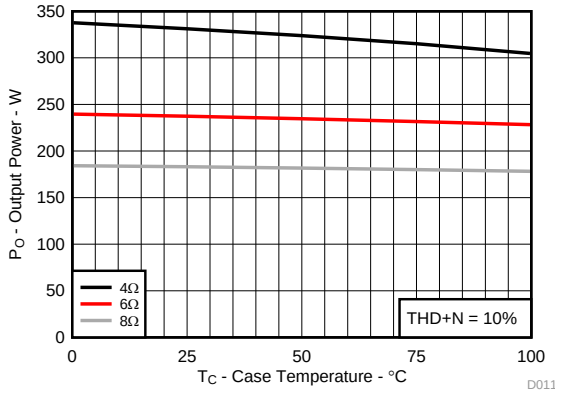
R_L = 4 Ω, 6 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 9. System Efficiency vs Output Power



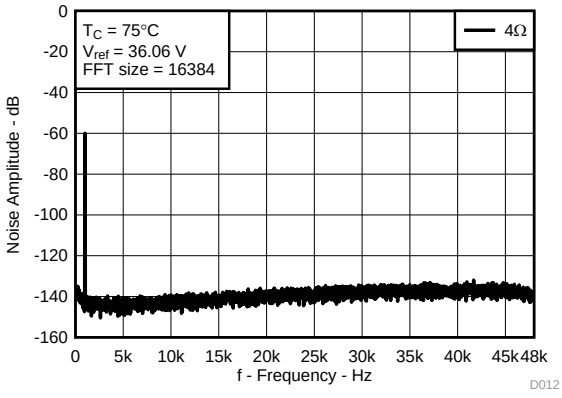
R_L = 4 Ω, 6 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 10. System Power Loss vs Output Power



R_L = 4 Ω, 6 Ω, 8 Ω THD+N = 10% T_C = 75°C

Figure 11. Output Power vs Case Temperature

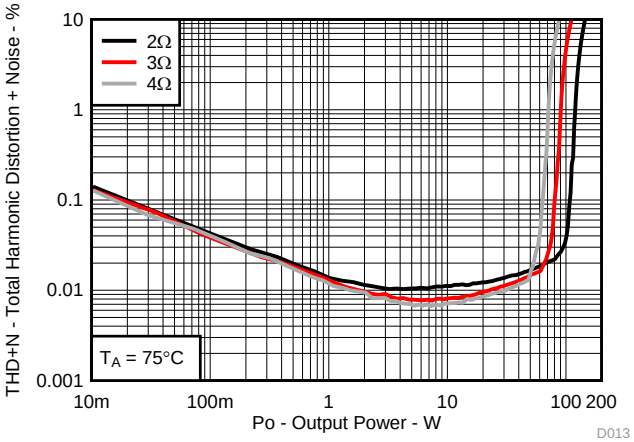


4 Ω, V_{REF} = 36.06 V (1% Output power) AUX-0025 filter, 80 kHz analyzer BW FFT = 16384 T_C = 75°C

Figure 12. Noise Amplitude vs Frequency

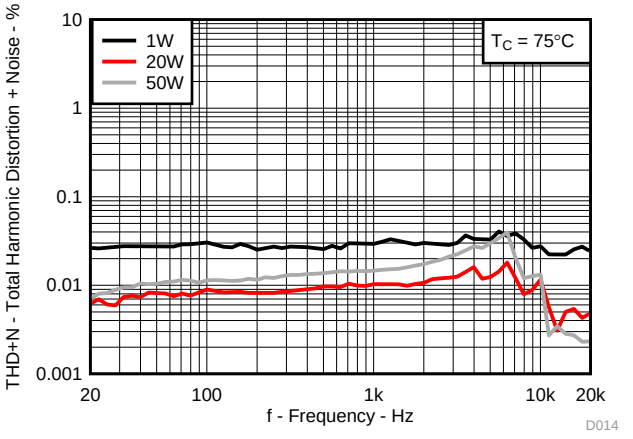
7.10 Typical Characteristics, SE Configuration

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 51 V, GVDD_X = 12 V, R_L = 3 Ω, f_S = 450 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 15 µH, C_{DEM} = 680 nF, MODE = 11, AES17 + AUX-0025 measurement filters, unless otherwise noted.



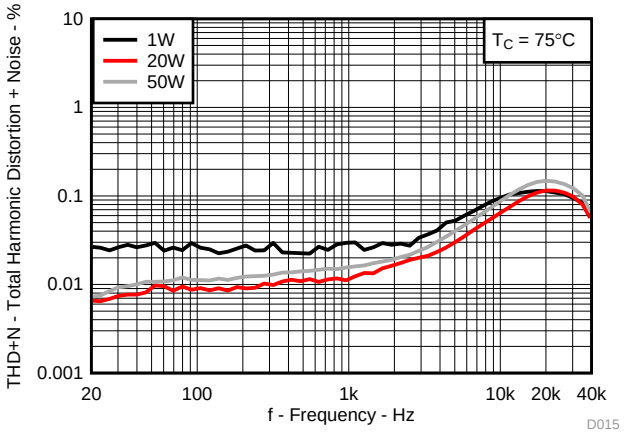
R_L = 2Ω, 3Ω, 4Ω T_C = 75°C

Figure 13. Total Harmonic Distortion+Noise vs Output Power



R_L = 3Ω P = 1W, 20W, 50W T_C = 75°C

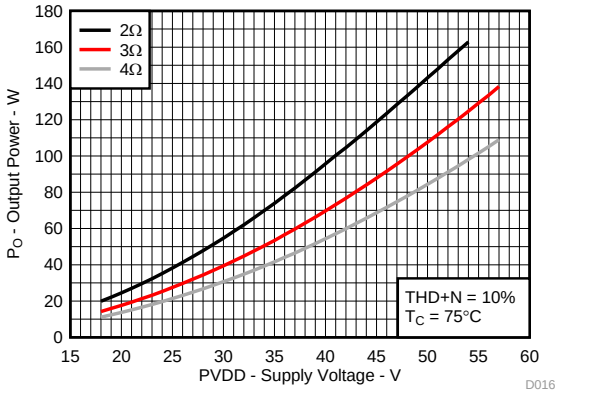
Figure 14. Total Harmonic Distortion+Noise vs Frequency



R_L = 3Ω P = 1W, 20W, 50W T_C = 75°C

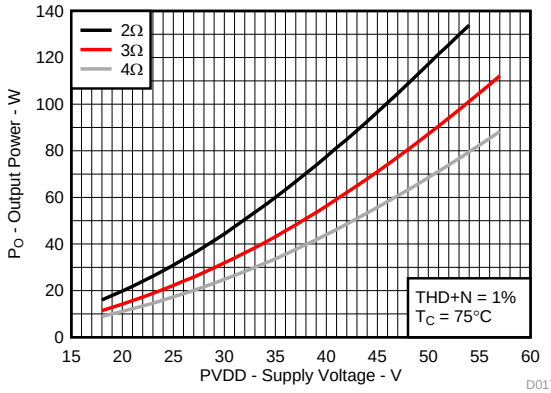
AUX-0025 filter, 80 kHz analyzer BW

Figure 15. Total Harmonic Distortion+Noise vs Frequency



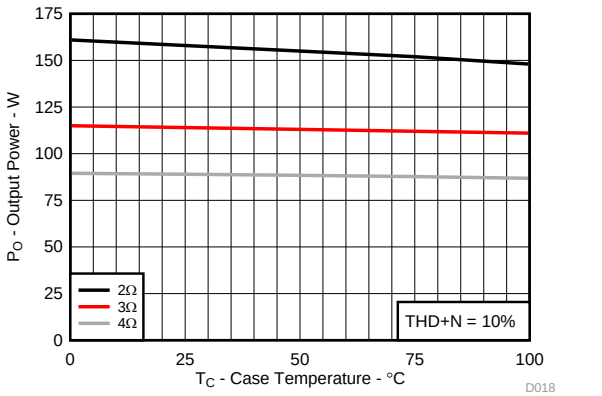
R_L = 2Ω, 3Ω, 4Ω THD+N = 10% T_C = 75°C

Figure 16. Output Power vs Supply Voltage



R_L = 2Ω, 3Ω, 4Ω THD+N = 1% T_C = 75°C

Figure 17. Output Power vs Supply Voltage

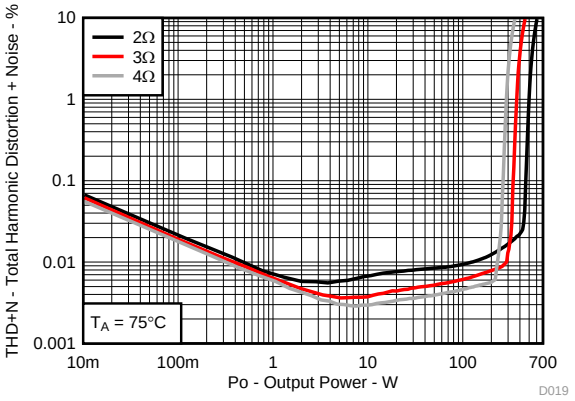


R_L = 2Ω, 3Ω, 4Ω THD+N = 10% T_C = 75°C

Figure 18. Output Power vs Case Temperature

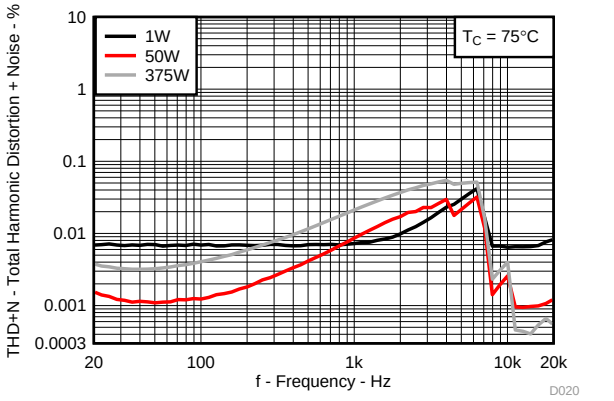
7.11 Typical Characteristics, PBTL Configuration

All Measurements taken at audio frequency = 1 kHz, PVDD_X = 51V, GVDD_X = 12 V, R_L = 2Ω, f_S = 450 kHz, R_{OC} = 22 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10µH, C_{DEM} = 1 µF, MODE = 10, AES17 + AUX-0025 measurement filters, unless otherwise noted.



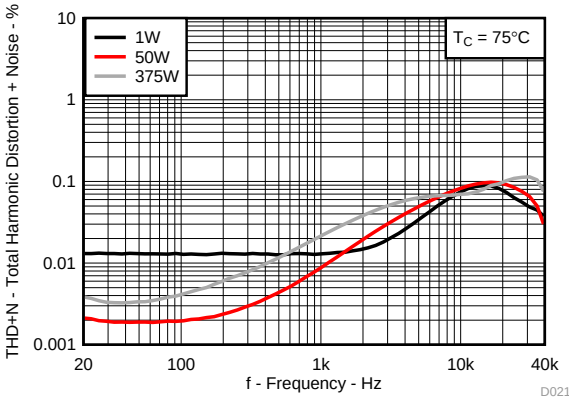
R_L = 2Ω, 3Ω, 4Ω T_C = 75°C

Figure 19. Total Harmonic Distortion+Noise vs Output Power



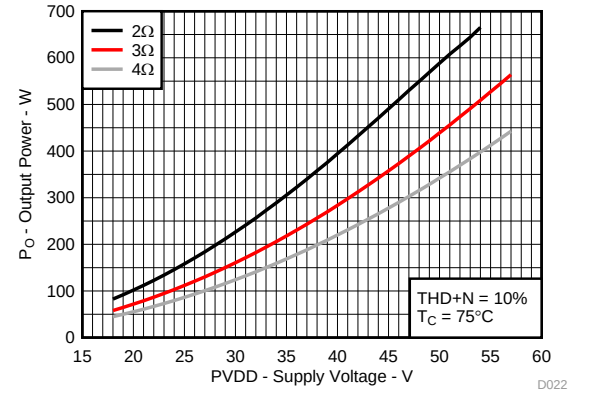
R_L = 2Ω P = 1W, 50W, 375W T_C = 75°C

Figure 20. Total Harmonic Distortion+Noise vs Frequency



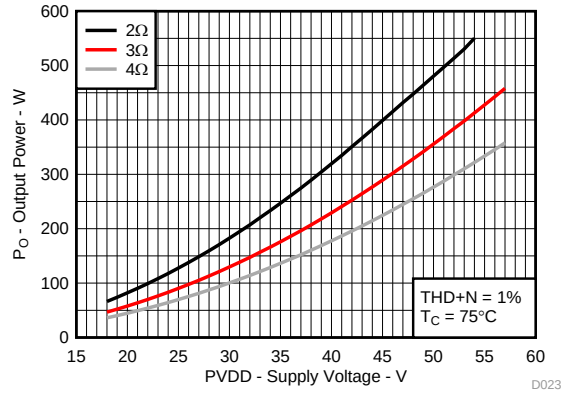
R_L = 2Ω P = 1W, 50W, 375W T_C = 75°C
AUX-0025 filter, 80 kHz analyzer BW

Figure 21. Total Harmonic Distortion+Noise vs Frequency



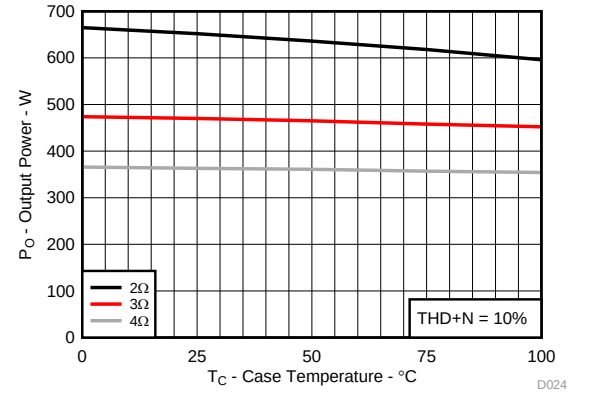
R_L = 2Ω, 3Ω, 4Ω THD+N = 10% T_C = 75°C

Figure 22. Output Power vs Supply Voltage



R_L = 2Ω, 3Ω, 4Ω THD+N = 1% T_C = 75°C

Figure 23. Output Power vs Supply Voltage



R_L = 2Ω, 3Ω, 4Ω THD+N = 10% T_C = 75°C

Figure 24. Output Power vs Case Temperature

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Recommended Operating Conditions*, *Typical Characteristics, BTL Configuration*, *Typical Characteristics, SE Configuration* and *Typical Characteristics, PBTL Configuration* sections.

Most audio analyzers will not give correct readings of Class-D amplifiers' performance due to their sensitivity to out of band noise present at the amplifier output. AES-17 + AUX-0025 pre-analyzer filters are recommended to use for Class-D amplifier measurements. In absence of such filters, a 30-kHz low-pass filter (10 Ω + 47 nF) can be used to reduce the out of band noise remaining on the amplifier outputs.

9 Detailed Description

9.1 Overview

To facilitate system design, the TPA3255 needs only a 12-V supply in addition to the (typical) 51-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry, AVDD and DVDD. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

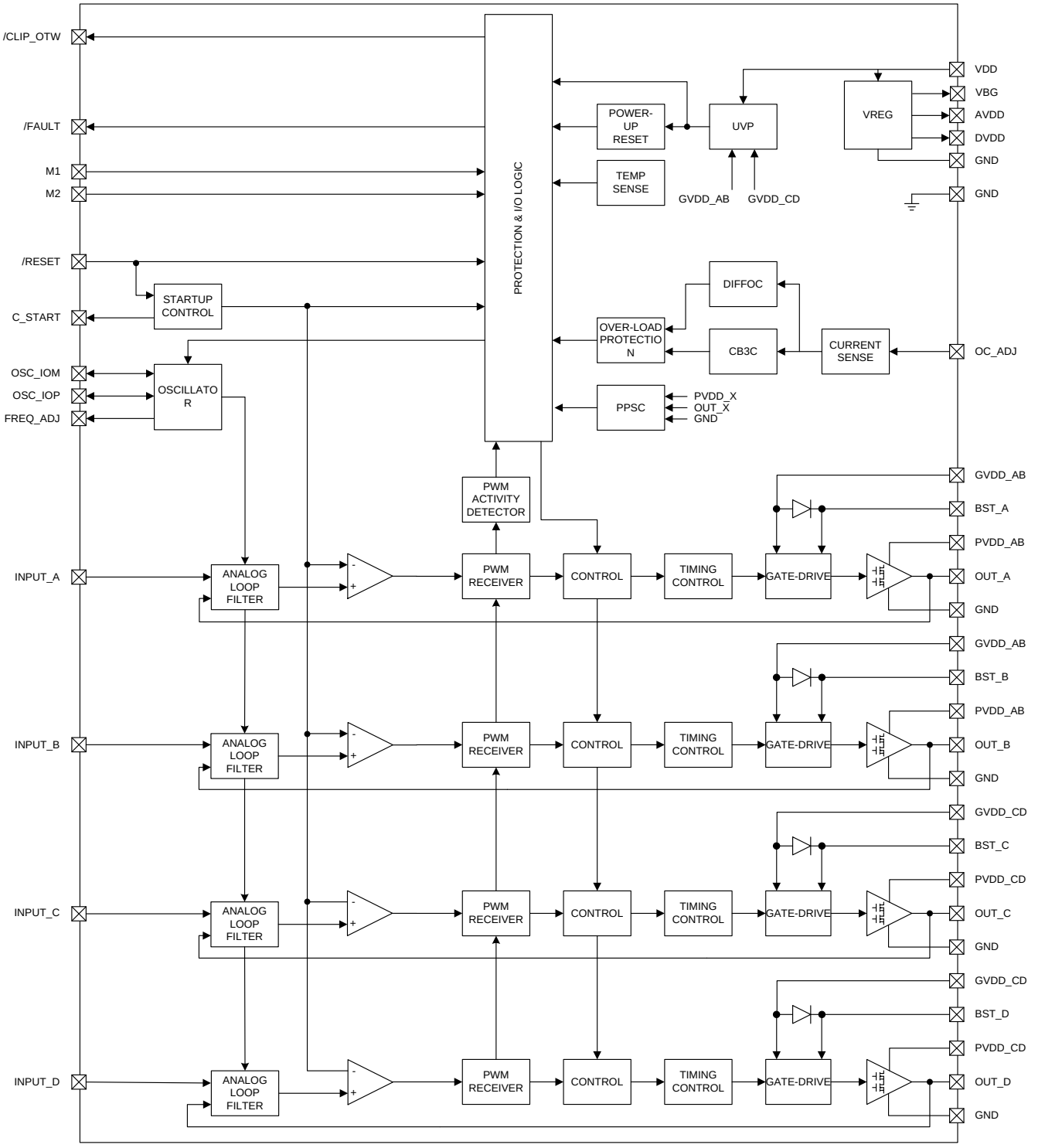
The audio signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X). Power-stage supply pins (PVDD_X) and gate drive supply pins (GVDD_X) are separate for each full bridge. Although supplied from the same 12-V source, separating to GVDD_AB, GVDD_CD, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details) is recommended. These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, the physical loop with the power supply pins, decoupling capacitors and GND return path to the device pins must be kept as short as possible and with as little area as possible to minimize induction (see reference board documentation for additional information).

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. It is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each full-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X node is decoupled with 1-μF ceramic capacitor placed as close as possible to the supply pins. It is recommended to follow the PCB layout of the TPA3255 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 51-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit, but it is recommended to release $\overline{\text{RESET}}$ after the power supply is settled for minimum turn on audible artefacts. Moreover, the TPA3255 is fully protected against erroneous power-stage turn on due to parasitic gate charging. Thus, voltage-supply ramp rates (dV/dt) are non-critical within the specified range (see the *Recommended Operating Conditions* table of this data sheet).

9.2 Functional Block Diagrams



Functional Block Diagrams (continued)

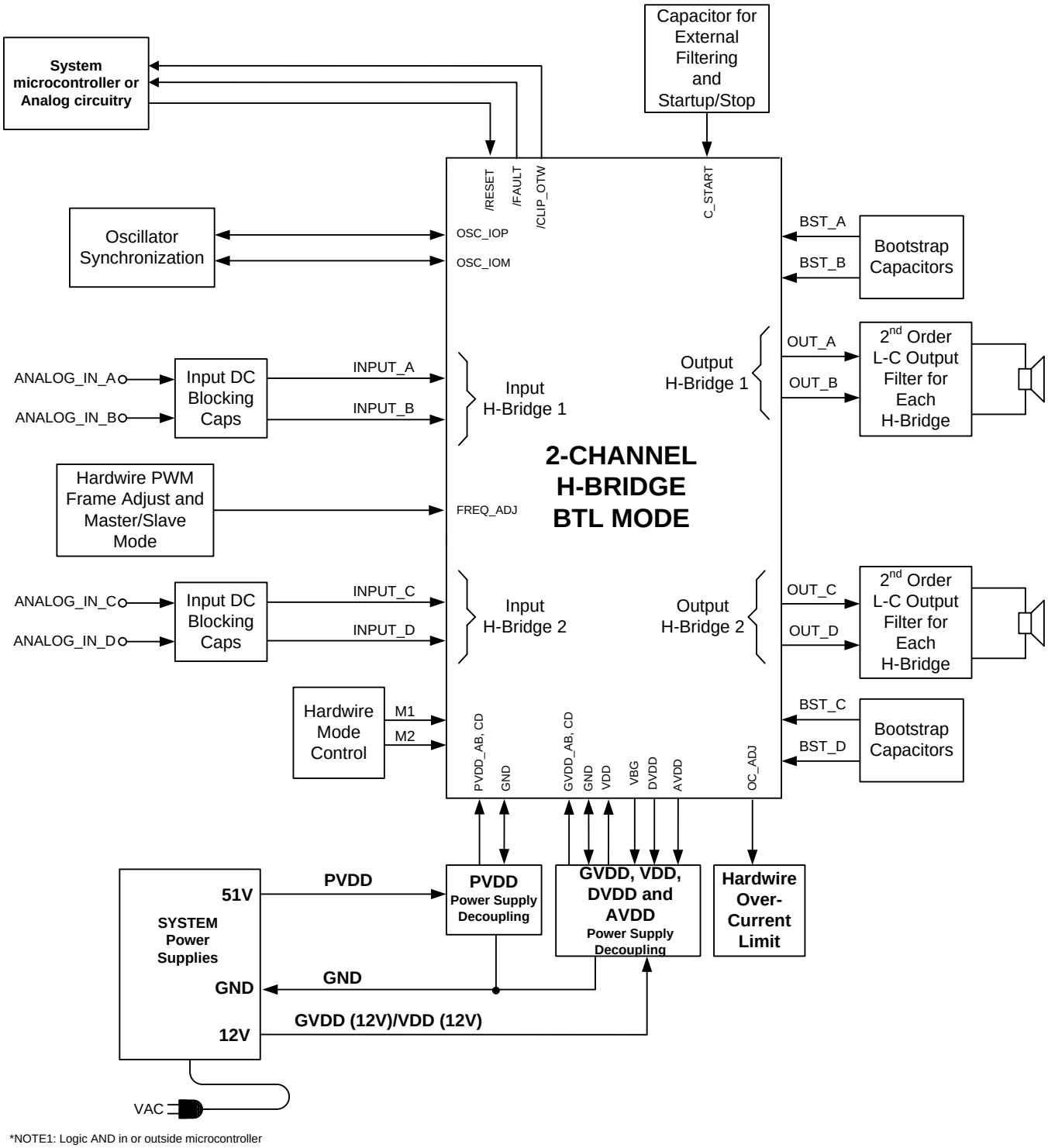


Figure 25. System Block Diagram

9.3 Feature Description

9.3.1 Error Reporting

The $\overline{\text{FAULT}}$, and $\overline{\text{CLIP\_OTW}}$, pins are active-low, open-drain outputs. The function is for protection-mode signaling to a system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{\text{FAULT}}$ pin going low. Also, $\overline{\text{CLIP\_OTW}}$ goes low when the device junction temperature exceeds 125°C (see Table 2).

Table 2. Error Reporting

$\overline{\text{FAULT}}$	$\overline{\text{CLIP\_OTW}}$	DESCRIPTION
0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP) Junction temperature higher than 125°C (overtemperature warning)
0	0	Overload (OLP) or undervoltage (UVP). Junction temperature higher than 125°C (overtemperature warning)
0	1	Overload (OLP) or undervoltage (UVP). Junction temperature lower than 125°C
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

Note that asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{\text{CLIP\_OTW}}$ signal using the system microcontroller and responding to an overtemperature warning signal by turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{\text{FAULT}}$ and $\overline{\text{CLIP\_OTW}}$ outputs.

9.4 Device Functional Modes

9.4.1 Device Protection System

The TPA3255 contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TPA3255 responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased.

The device will handle errors, as shown in Table 3.

Table 3. Device Protection

BTL MODE		PBTL MODE		SE MODE	
LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF	LOCAL ERROR IN	TURNS OFF
A	A+B	A	A+B+C+D	A	A+B
B		B		B	
C	C+D	C		C	C+D
D		D		D	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective halfbridge (non-latching, does not assert $\overline{\text{FAULT}}$).

9.4.1.1 Overload and Short Circuit Current Protection

TPA3255 has fast reacting current sensors with a programmable trip threshold (OC threshold) on all high-side and low-side FETs. To prevent output current from increasing beyond the programmed threshold, TPA3255 has the option of either limiting the output current for each switching cycle (Cycle By Cycle Current Control, CB3C) or to perform an immediate shutdown of the output in case of excess output current (Latching Shutdown). CB3C prevents premature shutdown due to high output current transients caused by high level music transients and a

drop of real speaker's load impedance, and allows the output current to be limited to a maximum programmed level. If the maximum output current persists, i.e. the power stage being overloaded with too low load impedance, the device will shut down the affected output channel and the affected output is put in a high-impedance (Hi- Z) state until a $\overline{\text{RESET}}$ cycle is initiated. CB3C works individually for each half bridge output. If an over current event is triggered, CB3C performs a state flip of the half bridge output that is cleared upon beginning of next PWM frame.

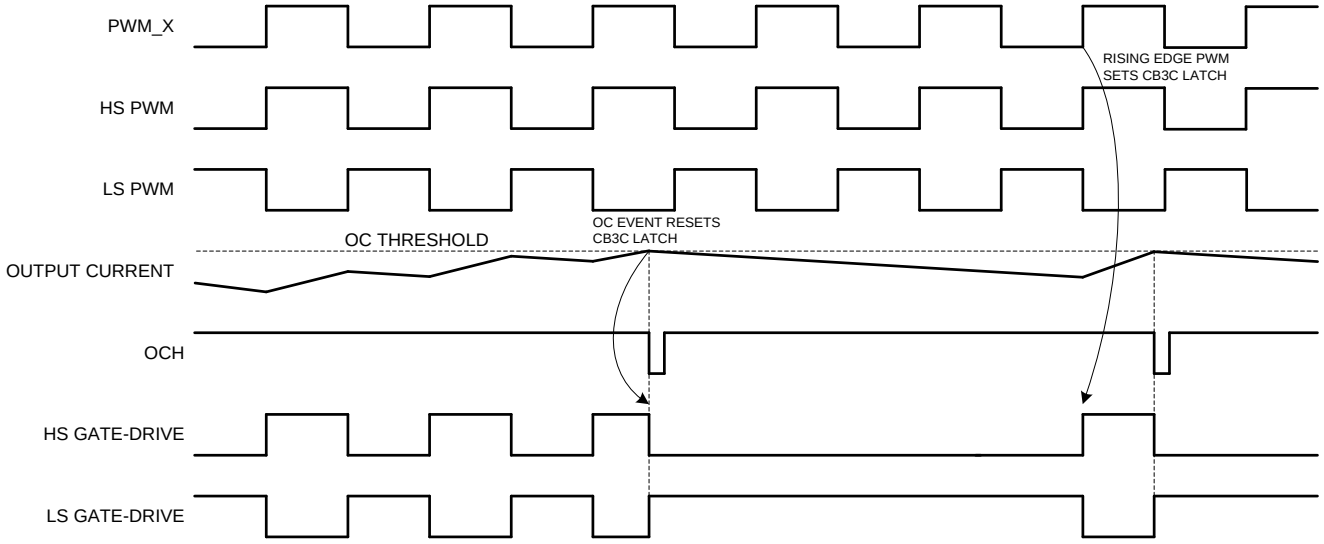


Figure 26. CB3C Timing Example

During CB3C an over load counter increments for each over current event and decrease for each non-over current PWM cycle. This allows full amplitude transients into a low speaker impedance without a shutdown protection action. In the event of a short circuit condition, the over current protection limits the output current by the CB3C operation and eventually shut down the affected output if the overload counter reaches its maximum value. If a latched OC operation is required such that the device shuts down the affected output immediately upon first detected over current event, this protection mode should be selected. The over current threshold and mode (CB3C or Latched OC) is programmed by the OC_ADJ resistor value. The OC_ADJ resistor needs to be within its intentional value range for either CB3C operation or Latched OC operation.

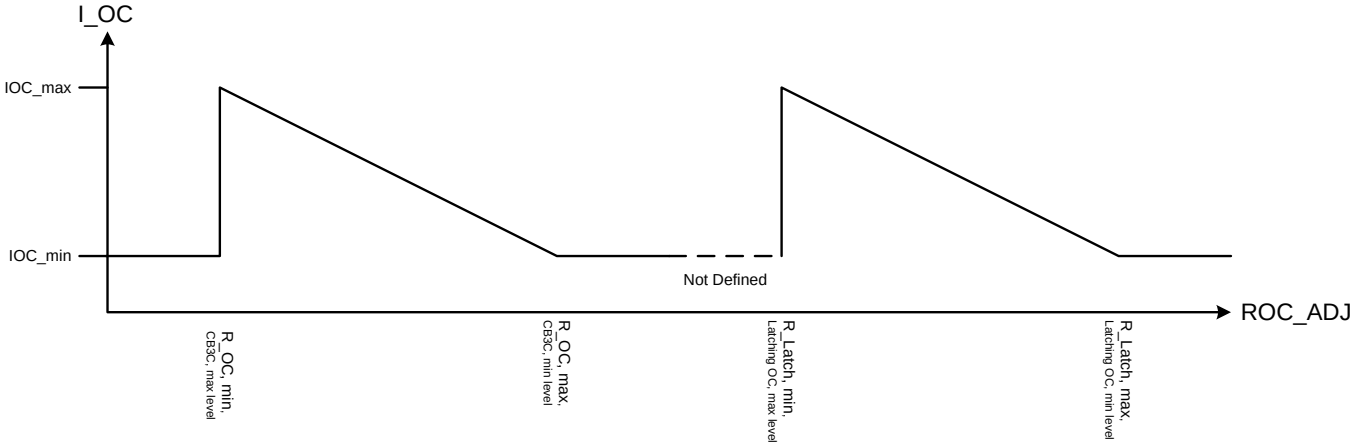


Figure 27. OC Threshold versus OC_ADJ Resistor Value Example

OC_ADJ values outside specified value range for either CB3C or latched OC operation will result in minimum OC threshold.

Table 4. Device Protection

OC_ADJ Resistor Value	Protection Mode	OC Threshold
22kΩ	CB3C	17.0A
24kΩ	CB3C	15.7A
27kΩ	CB3C	14.2A
30kΩ	CB3C	12.9A
47kΩ	Latched OC	17.0A
51kΩ	Latched OC	15.7A
56kΩ	Latched OC	14.2A
64kΩ	Latched OC	12.9A

9.4.1.2 Signal Clipping and Pulse Injector

A built in activity detector monitors the PWM activity of the OUT_X pins. TPA3255 is designed to drive unclipped output signals all the way to PVDD and GND rails. In case of audio signal clipping when applying excessive input signal voltage, or in case of CB3C current protection being active, the amplifier feedback loop of the audio channel will respond to this condition with a saturated state, and the output PWM signals would stop if the device did not have special circuitry implemented to handle this situation. To prevent the output PWM signals from stopping in a clipping or CB3C situation, narrow pulses are injected to the gate drive to maintain output activity. The injected narrow pulses are injected at every 4th PWM frame, and thus the effective switching frequency during this state is reduced to 1/4 of the normal switching frequency.

Signal clipping is signalled on the $\overline{\text{CLIP\_OTW}}$ pin and is self clearing when signal level reduces and the device reverts to normal operation. The $\overline{\text{CLIP\_OTW}}$ pulses start at the onset to output clipping, typically at a THD level around 0.01%, resulting in narrow $\overline{\text{CLIP\_OTW}}$ pulses starting with a pulse width of ~500 ns.

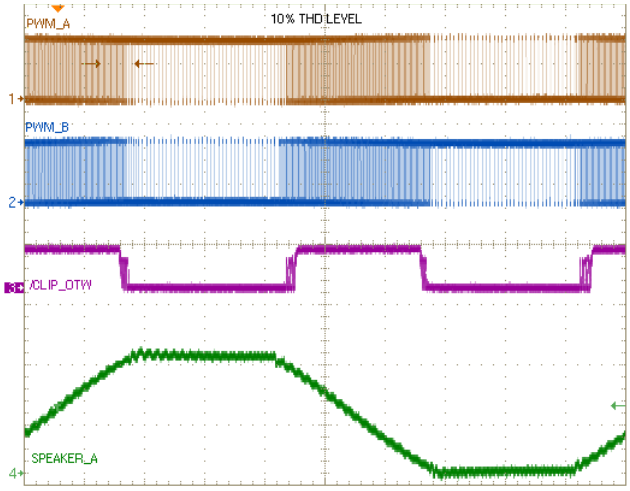


Figure 28. Signal Clipping PWM and Speaker Output Signals

9.4.1.3 DC Speaker Protection

The output DC protection scheme protects a speaker from excess DC current in case one terminal of the speaker is connected to the amplifier while the other is accidentally shorted to the chassis ground. Such a short circuit results in a DC voltage of PVDD/2 across the speaker, which potentially can result in destructive current levels. The output DC protection detects any unbalance of the output and input current of a BTL output, and in the event of the unbalance exceeding a programmed threshold, the overload counter increments until its maximum value and the affected output channel is shut down. DC Speaker Protection is disabled in SE mode operation.

9.4.1.4 Pin-to-Pin Short Circuit Protection (PPSC)

The PPSC detection system protects the device from permanent damage if a power output pin (OUT_X) is shorted to GND_X or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at startup that is, when VDD is supplied, consequently a short to either GND_X or PVDD_X after system startup does not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed; the device then continues the startup sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND_X, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is < 15ms/μF. While the PPSC detection is in progress, $\overline{\text{FAULT}}$ is kept low, and the device will not react to changes applied to the $\overline{\text{RESET}}$ pin. If no shorts are present the PPSC detection passes, and $\overline{\text{FAULT}}$ is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert a resistive load to GND_X or PVDD_X.

9.4.1.5 Overtemperature Protection OTW and OTE

TPA3255 has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{\text{CLIP\_OTW}}$) when the device junction temperature exceeds 120°C (typical) and, if the device junction temperature exceeds 155°C (typical), the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{\text{RESET}}$ must be asserted. Thereafter, the device resumes normal operation.

9.4.1.6 Undervoltage Protection (UVP) and Power-on Reset (POR)

The UVP and POR circuits of the TPA3255 fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach values stated in the *Electrical Characteristics* table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

9.4.1.7 Fault Handling

If a fault situation occurs while in operation, the device acts accordingly to the fault being a global or a channel fault. A global fault is a chip-wide fault situation and causes all PWM activity of the device to be shut down, and will assert $\overline{\text{FAULT}}$ low. A global fault is a latching fault and clearing $\overline{\text{FAULT}}$ and restarting operation requires resetting the device by toggling $\overline{\text{RESET}}$. Deasserting $\overline{\text{RESET}}$ should never be allowed with excessive system temperature, so it is advised to monitor $\overline{\text{RESET}}$ by a system microcontroller and only allow releasing $\overline{\text{RESET}}$ ($\overline{\text{RESET}}$ high) if the $\overline{\text{CLIP\_OTW}}$ signal is cleared (high). A channel fault results in shutdown of the PWM activity of the affected channel(s). Note that asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present.

Table 5. Error Reporting

Fault/Event	Fault/Event Description	Global or Channel	Reporting Method	Latched/Self Clearing	Action needed to Clear	Output FETs
PVDD_X UVP	Voltage Fault	Global	$\overline{\text{FAULT}}$ pin	Self Clearing	Increase affected supply voltage	HI-Z
VDD UVP						
AVDD UVP						
POR (DVDD UVP)	Power On Reset	Global	$\overline{\text{FAULT}}$ pin	Self Clearing	Allow DVDD to rise	HI-Z
BST_X UVP	Voltage Fault	Channel (Half Bridge)	None	Self Clearing	Allow BST cap to recharge (lowside ON, VDD 12V)	HighSide off
OTW	Thermal Warning	Global	$\overline{\text{OTW}}$ pin	Self Clearing	Cool below OTW threshold	Normal operation
OTE	Thermal Shutdown	Global	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
OLP (CB3C>1.7ms)	OC Shutdown	Channel	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
Latched OC (47kΩ<ROC_ADJ<68 kΩ)	OC Shutdown	Channel	$\overline{\text{FAULT}}$ pin	Latched	Toggle $\overline{\text{RESET}}$	HI-Z
CB3C (22kΩ<ROC_ADJ<30 kΩ)	OC Limiting	Channel	None	Self Clearing	Reduce signal level or remove short	Flip state, cycle by cycle at fs/3
Stuck at Fault(1)	No OSC_IO activity in Slave Mode	Global	None	Self Clearing	Resume OSC_IO activity	HI-Z

(1) Stuck at Fault occurs when input OSC_IO input signal frequency drops below minimum frequency given in the *Electrical Characteristics* table of this data sheet.

9.4.1.8 Device Reset

Asserting $\overline{\text{RESET}}$ low initiates the device ramp down. The output FETs go into a Hi-Z state after the ramp down is complete. Output pull downs are active both in SE mode and BTL mode with $\overline{\text{RESET}}$ low.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs.

Asserting reset input low removes any fault information to be signaled on the $\overline{\text{FAULT}}$ output, that is, $\overline{\text{FAULT}}$ is forced high. A rising-edge transition on reset input allows the device to resume operation after a fault. To ensure thermal reliability, the rising edge of reset must occur no sooner than 4 ms after the falling edge of $\overline{\text{FAULT}}$.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

TPA3255 can be configured either in stereo BTL mode, 4 channel SE mode, mono PBTL mode, or in 2.1 mixed 1x BTL + 2x SE mode depending on output power conditions and system design.

10.2 Typical Applications

10.2.1 Stereo BTL Application

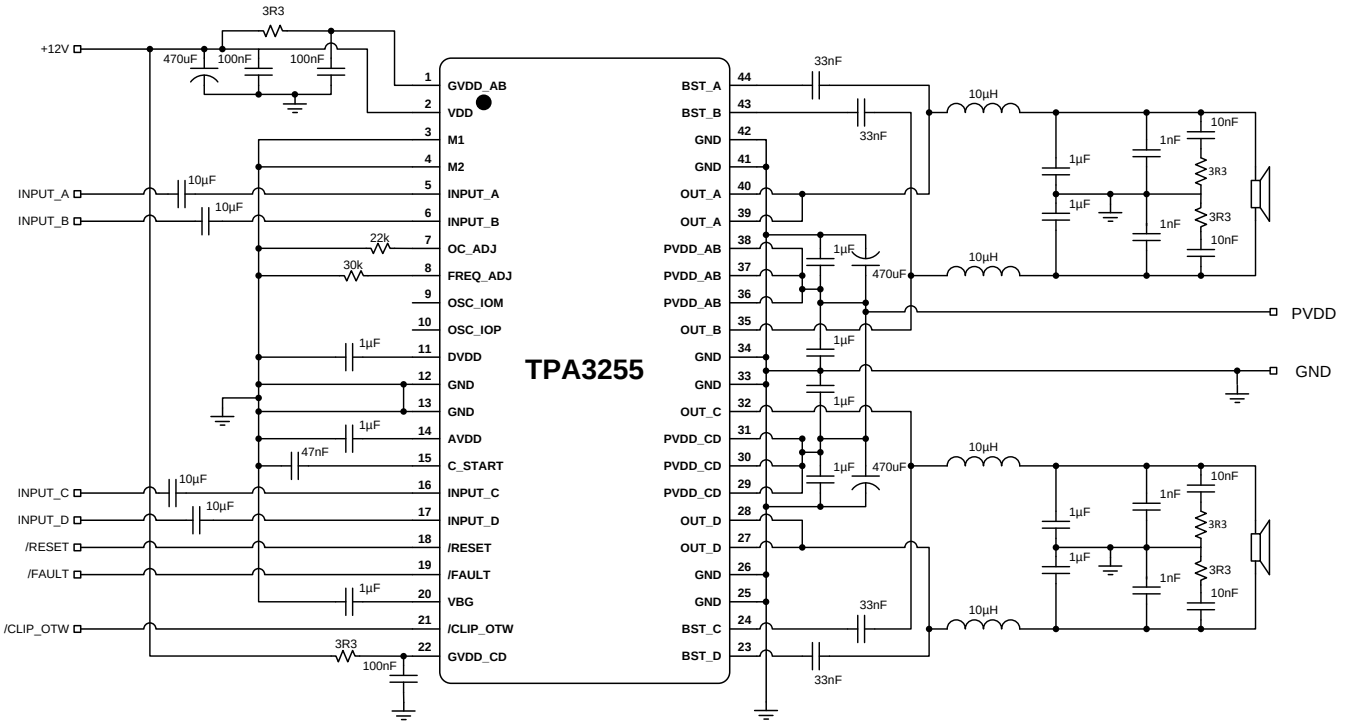


Figure 29. Typical Differential (2N) BTL Application

Typical Applications (continued)

10.2.1.1 Design Requirements

For this design example, use the parameters in Table 6.

Table 6. Design Requirements, BTL Application

DESIGN PARAMETER	EXAMPLE
Low Power (Pull-up) Supply	3.3 V
Mid Power Supply 12 V	12 V
High Power Supply	18 - 51 V
Mode Selection	M2 = L
	M1 = L
Analog Inputs	INPUT_A = ±3.9 V (peak, max)
	INPUT_B = ± 3.9V (peak, max)
	INPUT_C = ±3.9 V (peak, max)
	INPUT_D = ±3.9 V (peak, max)
Output Filters	Inductor-Capacitor Low Pass FIlter (10 µH + 1 µF)
Speaker Impedance	3-8 Ω

10.2.1.2 Detailed Design Procedures

A rising-edge transition on reset input allows the device to execute the startup sequence and starts switching.

The CLIP signal is indicating that the output is approaching clipping. The signal can be used either to decrease audio volume or to control an intelligent power supply nominally operating at a low rail adjusting to a higher supply rail.

The device is inverting the audio signal from input to output.

The DVDD and AVDD pins are not recommended to be used as a voltage sources for external circuitry.

10.2.1.2.1 Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

10.2.1.2.2 PVDD Capacitor Recommendation

The PVDD decoupling capacitors must be placed as close to the device pins a possible to insure short trace length and low a low inductance path. Likewise the ground path for these capacitors must provide a good reference and should be substantial. This will keep voltage ringing on PVDD to a minimum.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the 1µF that is placed on the power supply to each full-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 100 V is required for use with a 51-V power supply.

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 1000 µF, 80 V supports most applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

10.2.1.2.3 PCB Material Recommendation

FR-4 Glass Epoxy material with 2 oz. (70 µm) copper is recommended for use with the TPA3255. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

10.2.1.2.4 Oscillator

The built in oscillator frequency can be trimmed by an external resistor from the FREQ_ADJ pin to GND. Changes in the oscillator frequency should be made with resistor values specified in *Recommended Operating Conditions* while $\overline{\text{RESET}}$ is low.

To reduce interference problems while using a radio receiver tuned within the AM band, the switching frequency can be changed from nominal to lower or higher values. These values should be chosen such that the nominal and the alternate switching frequencies together result in the fewest cases of interference throughout the AM band. The oscillator frequency can be selected by the value of the FREQ_ADJ resistor connected to GND in master mode.

For slave mode operation, turn off the oscillator by pulling the FREQ_ADJ pin to DVDD. This configures the OSC_I/O pins as inputs to be slaved from an external differential clock. In a master/slave system inter-channel delay is automatically set up between the switching of the audio channels, which can be illustrated by no idle channels switching at the same time. This will not influence the audio output, but only the switch timing to minimize noise coupling between audio channels through the power supply. Inter-channel delay is needed to optimize audio performance and to get better operating conditions for the power supply. The inter-channel delay will be set up for a slave device depending on the polarity of the OSC_I/O connection as follows:

- Slave 1 mode has normal polarity (master + to slave + and master - to slave -)
- Slave 2 mode has reverse polarity (master + to slave - and master - to slave +)

The interchannel delay for interleaved channel idle switching is given in the table below for the master/slave and output configuration modes in degrees relative to the PWM frame.

Table 7. Master/Slave Inter Channel Delay Settings

Master	M1 = 0, M2 = 0, 2 x BTL mode	M1 = 1, M2 = 0, 1 x BTL + 2 x SE mode	M1 = 0, M2 = 1, 1 x PBTL mode	M1 = 1, M2 = 1, 4 x SE mode
OUT_A	0°	0°	0°	0°
OUT_B	180°	180°	180°	60°
OUT_C	60°	60°	0°	0°
OUT_D	240°	120°	180°	60°
Slave 1				
OUT_A	60°	60°	60°	60°
OUT_B	240°	240°	240°	120°
OUT_C	120°	120°	60°	60°
OUT_D	300°	180°	240°	120°
Slave 2				
OUT_A	30°	30°	30°	30°
OUT_B	210°	210°	210°	90°
OUT_C	90°	90°	30°	30°
OUT_D	270°	150°	210°	90°

10.2.2 Application Curves

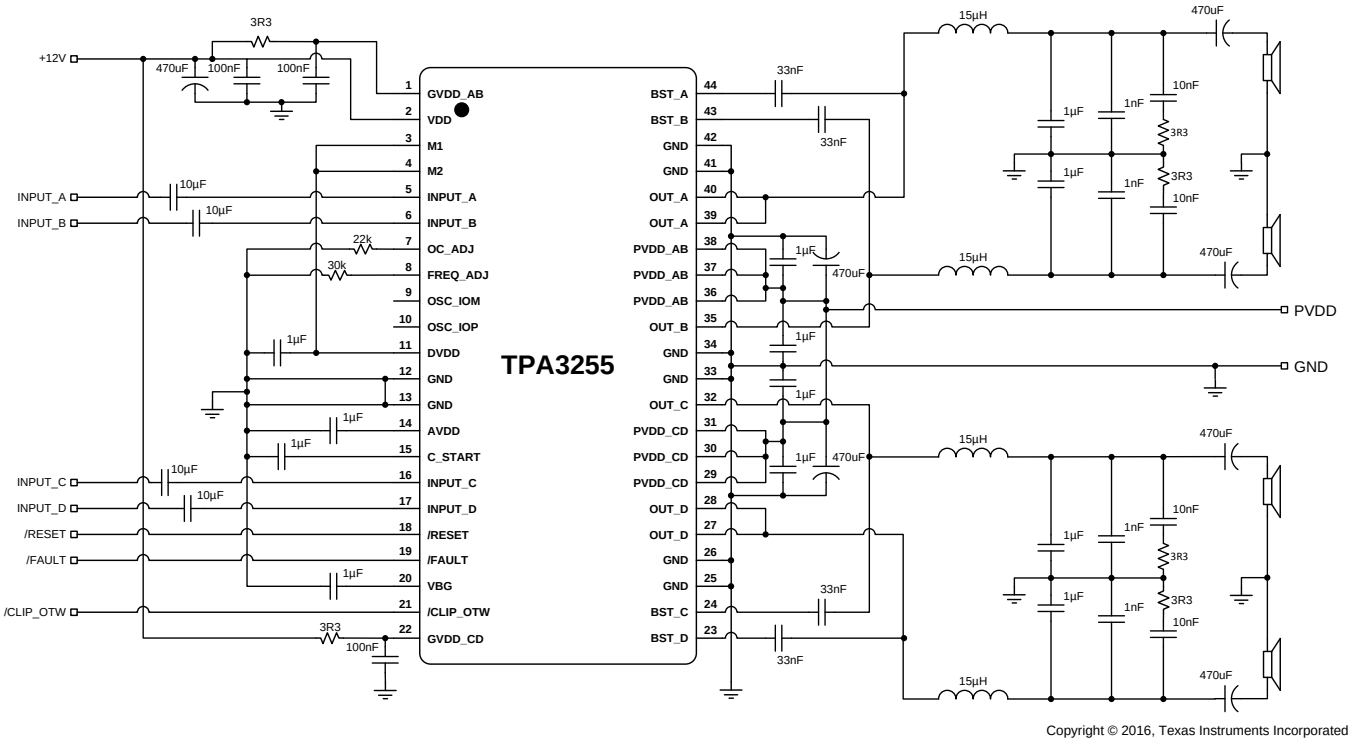
Relevant performance plots for TPA3255 in BTL configuration are shown in *Typical Characteristics, BTL Configuration*

Table 8. Relevant Performance Plots, BTL Configuration

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion+Noise vs Frequency	Figure 1
Total Harmonic Distortion+Noise vs Frequency, 80kHz analyzer BW	Figure 2
Total Harmonic Distortion + Noise vs Output Power	Figure 5
Output Power vs Supply Voltage, 10% THD+N	Figure 7
Output Power vs Supply Voltage, 10% THD+N	Figure 9
System Efficiency vs Output Power	Figure 9
System Power Loss vs Output Power	Figure 10
Output Power vs Case Temperature	Figure 11
Noise Amplitude vs Frequency	Figure 12

10.2.3 Typical Application, Single Ended (1N) SE

TPA3255 can be configured either in stereo BTL mode, 4 channel SE mode, mono PBTL mode, or in 2.1 mixed 1x BTL + 2x SE mode depending on output power conditions and system design.



Copyright © 2016, Texas Instruments Incorporated

Figure 30. Typical Single Ended (1N) SE Application

10.2.3.1 Design Requirements

Refer to *Stereo BTL Application* for the Design Requirements.

Table 9. Design Requirements, SE Application

DESIGN PARAMETER	EXAMPLE
Low Power (Pull-up) Supply	3.3 V
Mid Power Supply 12 V	12 V
High Power Supply	18 - 51 V
Mode Selection	M2 = H
	M1 = H
Analog Inputs	INPUT_A = ±3.9 V (peak, max)
	INPUT_B = ±3.9 V (peak, max)
	INPUT_C = ±3.9 V (peak, max)
	INPUT_D = ±3.9 V (peak, max)
Output Filters	Inductor-Capacitor Low Pass FIlter (15 µH + 680 nF)
Speaker Impedance	2 - 8 Ω

10.2.3.2 Detailed Design Procedures

Refer to *Stereo BTL Application* for the Detailed Design Procedures.

10.2.3.3 Application Curves

Relevant performance plots for TPA3255 in PBTL configuration are shown in *Typical Characteristics, SE Configuration*

Table 10. Relevant Performance Plots, SE Configuration

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion+Noise vs Output Power	Figure 13
Total Harmonic Distortion+Noise vs Frequency	Figure 14
Total Harmonic Distortion+Noise vs Frequency, 80kHz analyzer BW	Figure 15
Output Power vs Supply Voltage, 10% THD+N	Figure 16
Output Power vs Supply Voltage, 1% THD+N	Figure 17
Output Power vs Case Temperature	Figure 18

10.2.4 Typical Application, Differential (2N) PBTL

TPA3255 can be configured either in stereo BTL mode, 4 channel SE mode, mono PBTL mode, or in 2.1 mixed 1x BTL + 2x SE mode depending on output power conditions and system design.

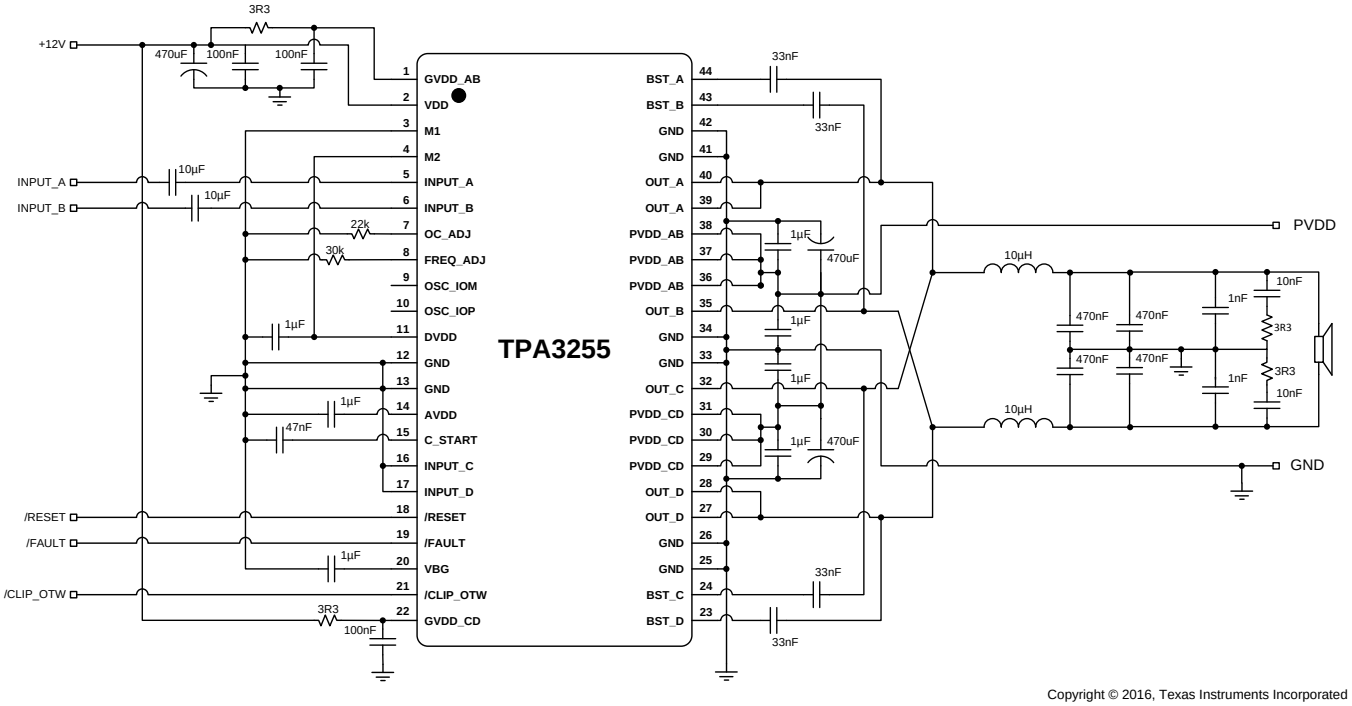


Figure 31. Typical Differential (2N) PBTL Application

10.2.4.1 Design Requirements

Refer to *Stereo BTL Application* for the Design Requirements.

Table 11. Design Requirements, PBTL Application

DESIGN PARAMETER	EXAMPLE
Low Power (Pull-up) Supply	3.3 V
Mid Power Supply 12 V	12 V
High Power Supply	18 - 51 V
Mode Selection	M2 = H
	M1 = L
Analog Inputs	INPUT_A = ±3.9V (peak, max)
	INPUT_B = ±3.9V (peak, max)
	INPUT_C = Grounded
	INPUT_D = Grounded
Output Filters	Inductor-Capacitor Low Pass FIlter (10 µH + 1 µF)
Speaker Impedance	2 - 4 Ω

10.2.4.2 Detailed Design Procedures

Refer to *Stereo BTL Application* for the Detailed Design Procedures.

10.2.4.3 Application Curves

Relevant performance plots for TPA3255 in PBTL configuration are shown in *Typical Characteristics, PBTL Configuration*

Table 12. Relevant Performance Plots, PBTL Configuration

PLOT TITLE	FIGURE NUMBER
Total Harmonic Distortion+Noise vs Output Power	Figure 19
Total Harmonic Distortion+Noise vs Frequency	Figure 20
Total Harmonic Distortion+Noise vs Frequency, 80kHz analyzer BW	Figure 21
Output Power vs Supply Voltage, 10% THD+N	Figure 22
Output Power vs Supply Voltage, 1% THD+N	Figure 23
Output Power vs Case Temperature	Figure 24

11 Power Supply Recommendations

11.1 Power Supplies

The TPA3255 device requires two external power supplies for proper operation. A high-voltage supply called PVDD is required to power the output stage of the speaker amplifier and its associated circuitry. Additionally, one mid-voltage power supply for GVDD_X and VDD is required to power the gate-drive and other internal digital and analog portions of the device. The allowable voltage range for both the PVDD and the GVDD_X/VDD supplies are listed in the *Recommended Operating Conditions* table. Ensure both the PVDD and the GVDD_X/VDD supplies can deliver more current than listed in the *Electrical Characteristics* table.

11.1.1 VDD Supply

The VDD supply required from the system is used to power several portions of the device. It provides power to internal regulators DVDD and AVDD that are used to power digital and analog sections of the device, respectively. Proper connection, routing, and decoupling techniques are highlighted in the TPA3255 device EVM User's Guide SLOU441 (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3255 device EVM User's Guide, which followed the same techniques as those shown in the *Application Information* section, may result in reduced performance, errant functionality, or even damage to the TPA3255 device. Some portions of the device also require a separate power supply which is a lower voltage than the VDD supply. To simplify the power supply requirements for the system, the TPA3255 device includes integrated low-dropout (LDO) linear regulators to create these supplies. These linear regulators are internally connected to the VDD supply and their outputs are presented on AVDD and DVDD pins, providing a connection point for an external bypass capacitors. It is important to note that the linear regulators integrated in the device have only been designed to support the current requirements of the internal circuitry, and should not be used to power any additional external circuitry. Additional loading on these pins could cause the voltage to sag and increase noise injection, which negatively affects the performance and operation of the device.

11.1.2 GVDD_X Supply

The GVDD_X supply required from the system is used to power the gate-drives for the output H-bridges. Proper connection, routing, and decoupling techniques are highlighted in the TPA3255 device EVM User's Guide SLOU441 (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Deviation from the guidance offered in the TPA3255 device EVM User's Guide, which followed the same techniques as those shown in the *Application Information* section, may result in reduced performance, errant functionality, or even damage to the TPA3255 device.

Power Supplies (continued)

11.1.3 PVDD Supply

The output stage of the amplifier drives the load using the PVDD supply. This is the power supply which provides the drive current to the load during playback. Proper connection, routing, and decoupling techniques are highlighted in the TPA3255 device EVM User's Guide SLOU441 (as well as the *Application Information* section and *Layout Examples* section) and must be followed as closely as possible for proper operation and performance. Due the high-voltage switching of the output stage, it is particularly important to properly decouple the output power stages in the manner described in the TPA3255 device EVM User's Guide SLOU441. The lack of proper decoupling, like that shown in the EVM User's Guide, can results in voltage spikes which can damage the device, or cause poor audio performance and device shutdown faults.

11.2 Powering Up

The TPA3255 does not require a power-up sequence, but it is recommended to hold $\overline{\text{RESET}}$ low for at least 250 ms after PVDD supply voltage is turned ON. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltages are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output as well as initiating a controlled ramp up sequence of the output voltage.

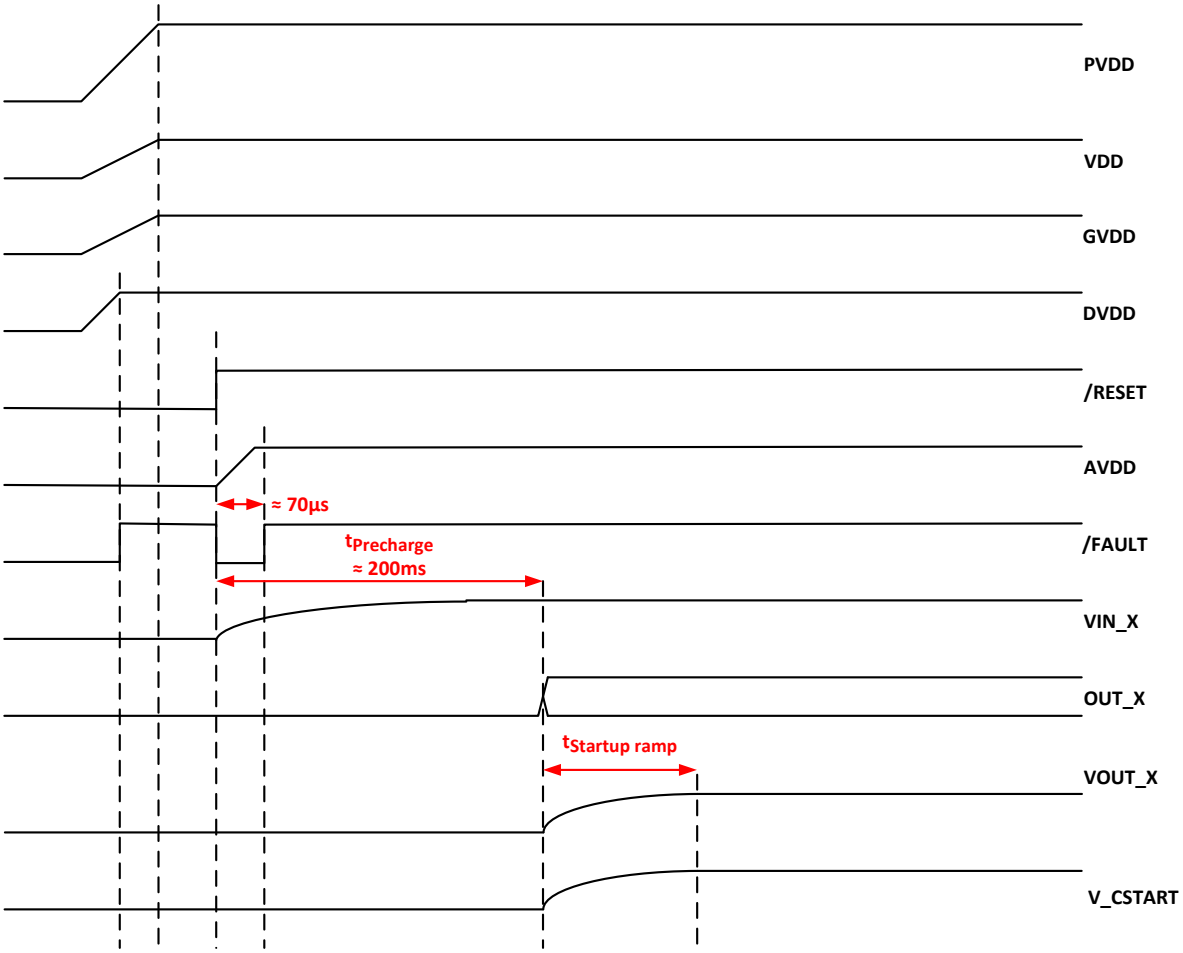


Figure 32. Startup Timing

When $\overline{\text{RESET}}$ is released to turn on TPA3255, $\overline{\text{FAULT}}$ signal will turn low and AVDD voltage regulator will be enabled. $\overline{\text{FAULT}}$ will stay low until AVDD reaches the undervoltage protection (UVP) voltage threshold (see the Electrical Characteristics table of this data sheet). After a precharge time to stabilize the DC voltage across the input AC coupling capacitors, the ramp up sequence starts.

11.3 Powering Down

The TPA3255 does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see the *Electrical Characteristics* table of this data sheet). Although not specifically required, it is a good practice to hold RESET low during power down, thus preventing audible artifacts including pops or clicks by initiating a controlled ramp down sequence of the output voltage.

11.4 Thermal Design

11.4.1 Thermal Performance

TPA3255 thermal performance is dependent on the design of the thermal system, which is the heatsink design and surrounding conditions including system enclosure (closed box with no air flow, or a fanned system etc.). As a result, the maximum continuous output power attainable will be influenced by the thermal design.

To mitigate thermal limitations in systems with the device operated at continuous high power it is advised to increase the cooling capability of the thermal system, or to operate the device in PBTL operation mode.

11.4.2 Thermal Performance with Continuous Output Power

It is recommended to operate TPA3255 below the OTW threshold. In most systems normal use conditions will safely keep the device temperature with margin to the OTW threshold. However in some systems and use cases the device tempertaure can run high, dependent on the actual output power, operating voltage, and thermal system. At high operating temperature some thermal limitations for continuous output power may occur at low audio frequencies due to increased heating of the output MOSFETs. Figure 33 shows maximum attainable continuous output power with a heatsink temperature of 75ºC and maximum 10% THD.

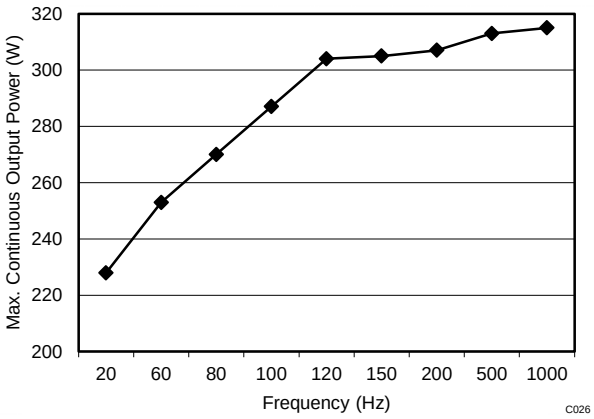


Figure 33. Maximum Continuous Output Power vs Frequency, BTL, 4Ω Load, Each Channel, T_C = 75°C

11.4.3 Thermal Performance with Non-Continuous Output Power

As audio signals often have a peak to average ratio larger than one (average level below maximum peak output), the thermal performance for audio signals can be illustrated using burst signals with different burst ratios.

Thermal Design (continued)

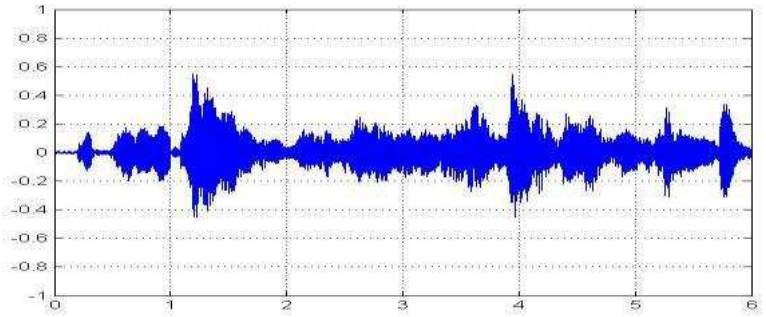


Figure 34. Example of audio signal

A burst signal is characterized by the high-level to low-level ratio as well as the duration of the high level and low level, e.g. a burst 1:4 stimuli is a single period of high level followed by 4 cycles of low level.

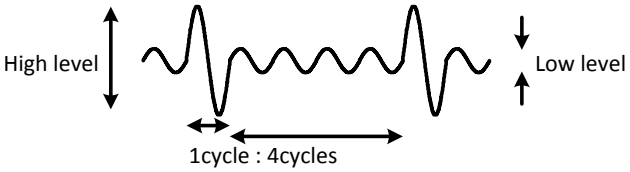


Figure 35. Example of 1:4 Burst Signal

The following analysis of thermal performance for TPA3255 is made with the heatsink temperature controlled to 75°C.

The device is not thermally limited with 8-Ω load, but depending on the burst stimuli for operation at 75ºC heatsink temperature some thermal limitations may occur with a lower load impedance, depending on switching frequency and average to maximum power ratio. The figure below shows burst performance with a signal power ratio of 1:16 (low cycles power level 1/16 of the high cycles power level) and 1:8 .

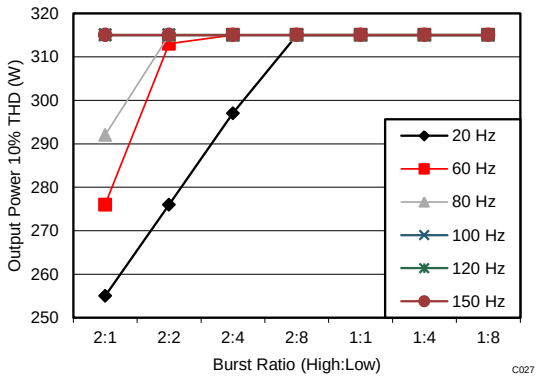


Figure 36. Maximum Burst Output Power vs Frequency, BTL, 4Ω Load, Each Channel, T_C = 75°C, Power Ratio 1:16

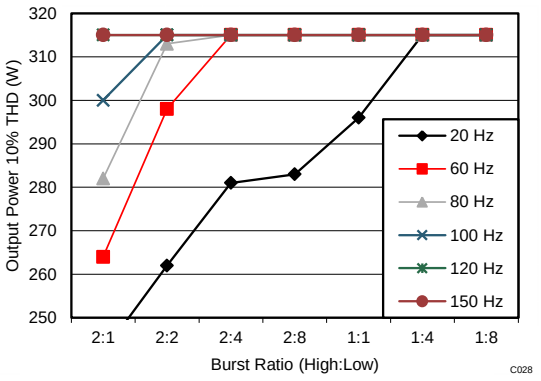


Figure 37. Maximum Burst Output Power vs Frequency, BTL, 4Ω Load, Each Channel, T_C = 75°C, Power Ratio 1:8

12 Layout

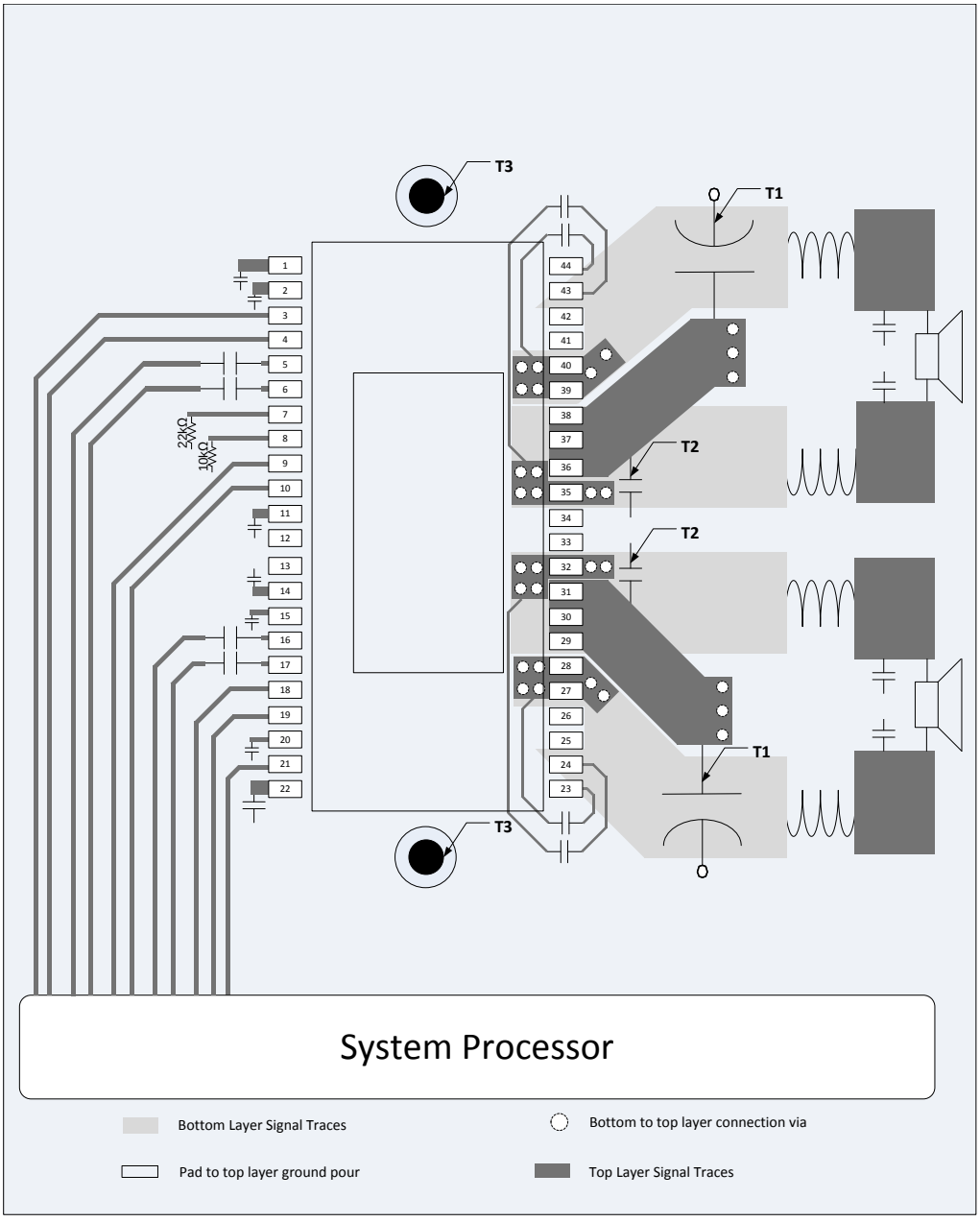
12.1 Layout Guidelines

- Use an unbroken ground plane to have good low impedance and inductance return path to the power supply for power and audio signals.
- Maintain a contiguous ground plane from the ground pins to the PCB area surrounding the device for as many of the ground pins as possible, since the ground pins are the best conductors of heat in the package.
- PCB layout, audio performance and EMI are linked closely together.
- Routing the audio input should be kept short and together with the accompanied audio source ground.
- The small bypass capacitors on the PVDD lines of the DUT be placed as close the PVDD pins as possible.
- A local ground area underneath the device is important to keep solid to minimize ground bounce.
- Orient the passive component so that the narrow end of the passive component is facing the TPA3255 device, unless the area between two pads of a passive component is large enough to allow copper to flow in between the two pads.
- Avoid placing other heat producing components or structures near the TPA3255 device.
- Avoid cutting off the flow of heat from the TPA3255 device to the surrounding ground areas with traces or via strings, especially on output side of device.

Netlist for this printed circuit board is generated from the schematic in Figure 38.

12.2 Layout Examples

12.2.1 BTL Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

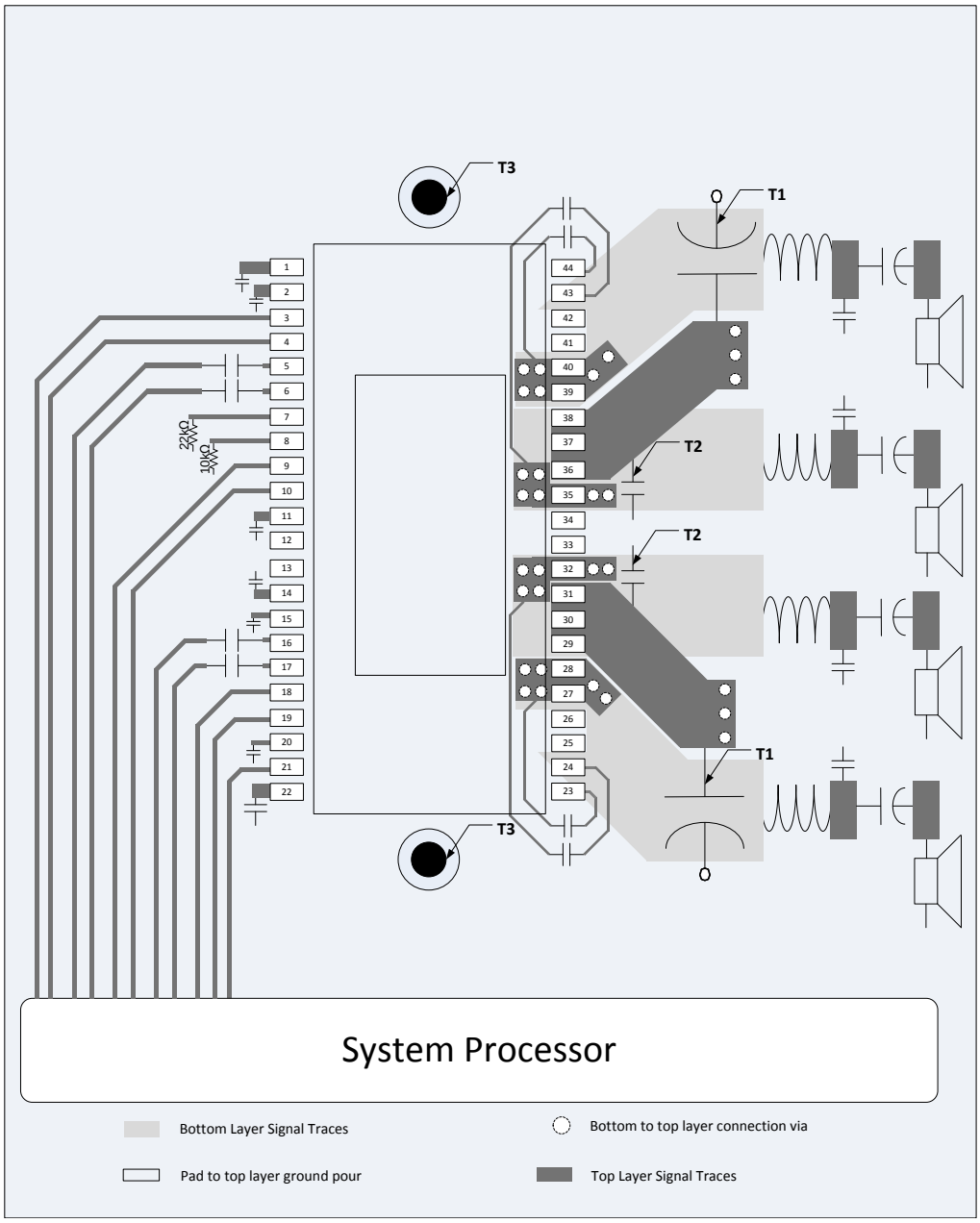
C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **Note T3**: Heat sink needs to have a good connection to PCB ground.

Figure 38. BTL Application Printed Circuit Board - Composite

Layout Examples (continued)

12.2.2 SE Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

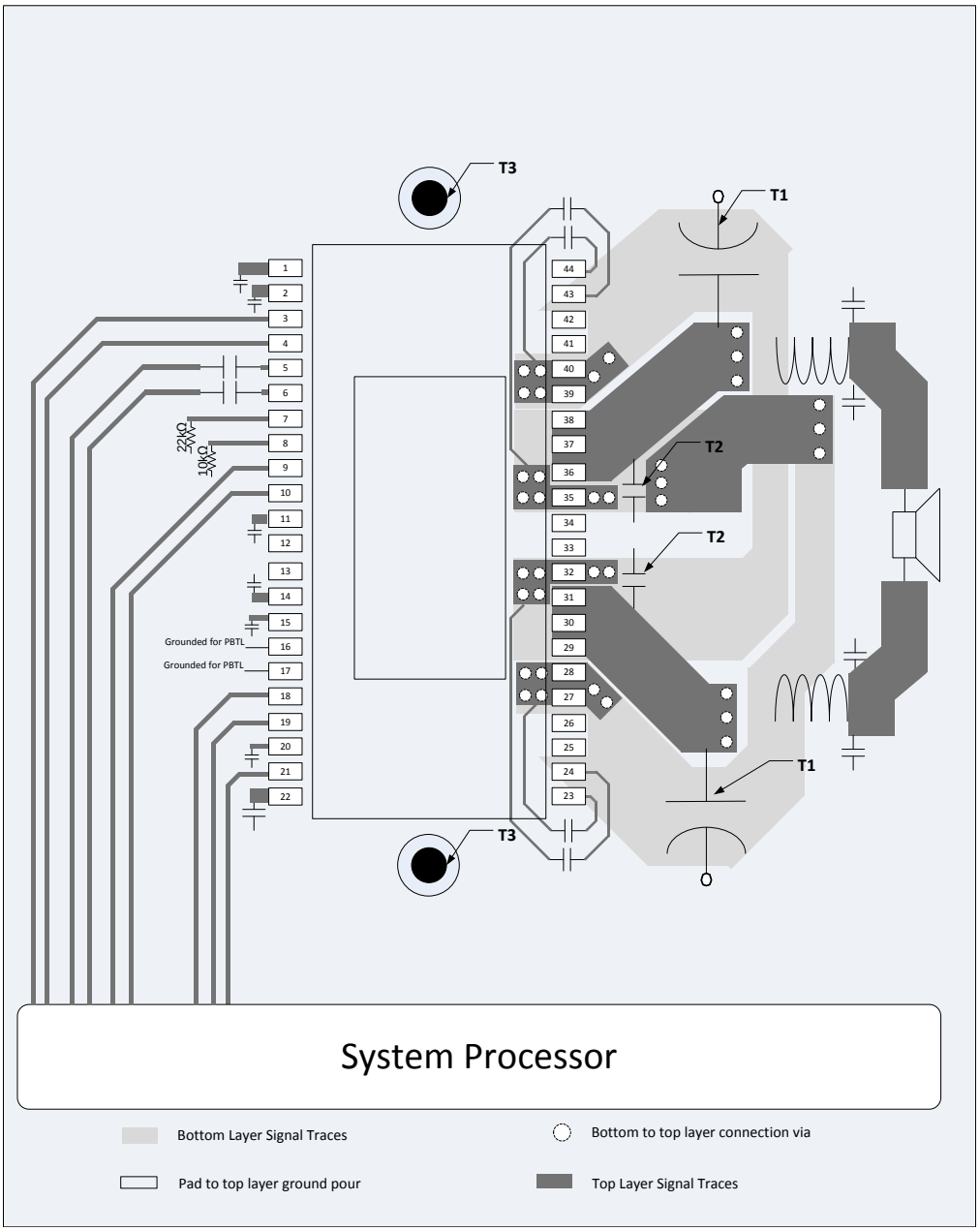
C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **Note T3**: Heat sink needs to have a good connection to PCB ground.

Figure 39. SE Application Printed Circuit Board - Composite

Layout Examples (continued)

12.2.3 PBTL Application Printed Circuit Board Layout Example



A. Note: PCB layout example shows composite layout. Dark grey: Top layer copper traces, light gray: Bottom layer copper traces. All PCB area not used for traces should be GND copper pour (transparent on example image)

B. **Note T1**: PVDD decoupling bulk capacitors should be as close as possible to the PVDD and GND_X pins, the heat sink sets the distance. Wide traces should be routed on the top layer with direct connection to the pins and without going through vias. No vias or traces should be blocking the current path.

C. **Note T2**: Close decoupling of PVDD with low impedance X7R ceramic capacitors is placed under the heat sink and close to the pins.

D. **ote T3**: Heat sink needs to have a good connection to PCB ground.

Figure 40. PBTL Application Printed Circuit Board - Composite

13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

『TPA3255D2EVMユーザー・ガイド』、SLOU441

13.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™オンライン・コミュニティ ***TIのE2E（Engineer-to-Engineer）コミュニティ。*** エンジニア間の共同作業を促進するために開設されたものです。e2e.ti.comでは、他のエンジニアに質問し、知識を共有し、アイディアを検討して、問題解決に役立てることができます。

設計サポート ***TIの設計サポート*** 役に立つE2Eフォーラムや、設計サポート・ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。

13.4 商標

PurePath, E2E are trademarks of Texas Instruments.
Blu-Ray Disc is a trademark of Blu-ray Disc Association.
All other trademarks are the property of their respective owners.

13.5 静電気放電に関する注意事項

これらのデバイスは、限定的なESD（静電破壊）保護機能を内 蔵しています。保存時または取り扱い時は、MOSゲートに対す る静電破壊を防止するために、リード線同士をショートさせて おくか、デバイスを導電フォームに入れる必要があります。

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3255DDV	ACTIVE	HTSSOP	DDV	44	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	3255	Samples
TPA3255DDVR	ACTIVE	HTSSOP	DDV	44	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	0 to 70	3255	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

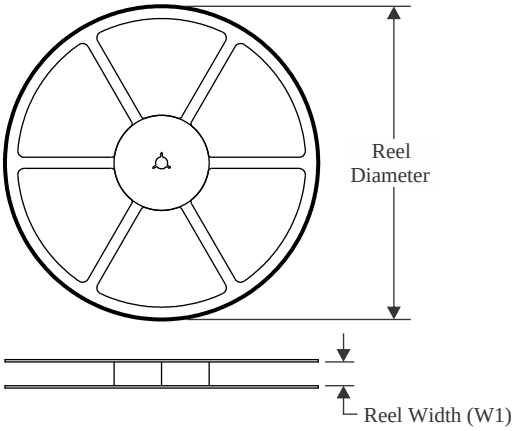
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

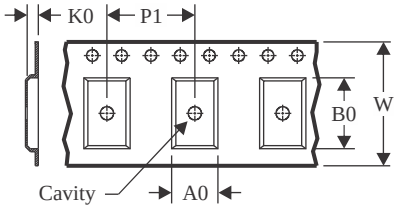
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

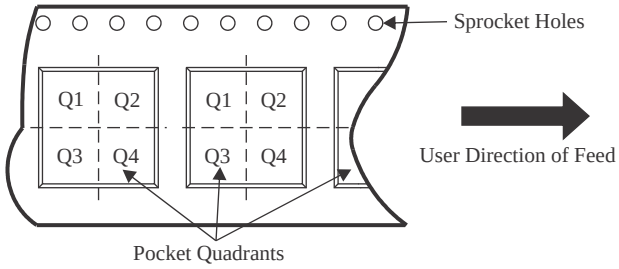


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

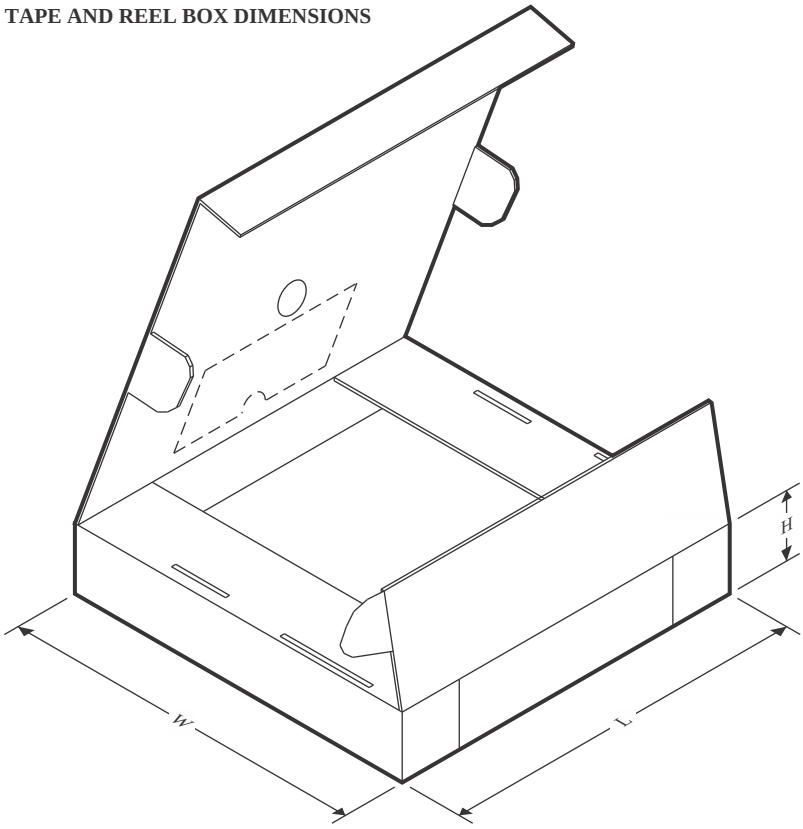
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3255DDVR	HTSSOP	DDV	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

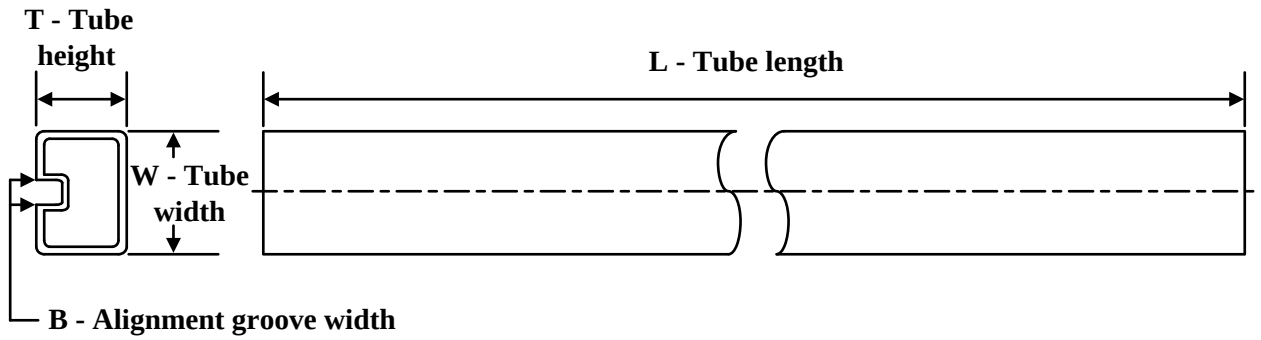
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3255DDVR	HTSSOP	DDV	44	2000	350.0	350.0	43.0

TUBE

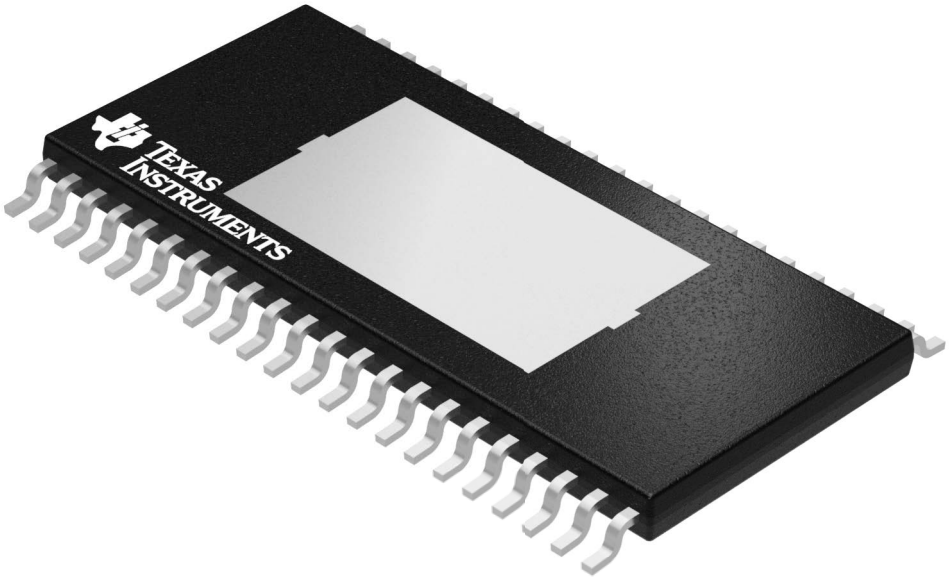


*All dimensions are nominal

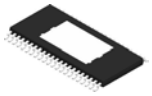
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3255DDV	DDV	HTSSOP	44	35	530	11.89	3600	4.9

DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

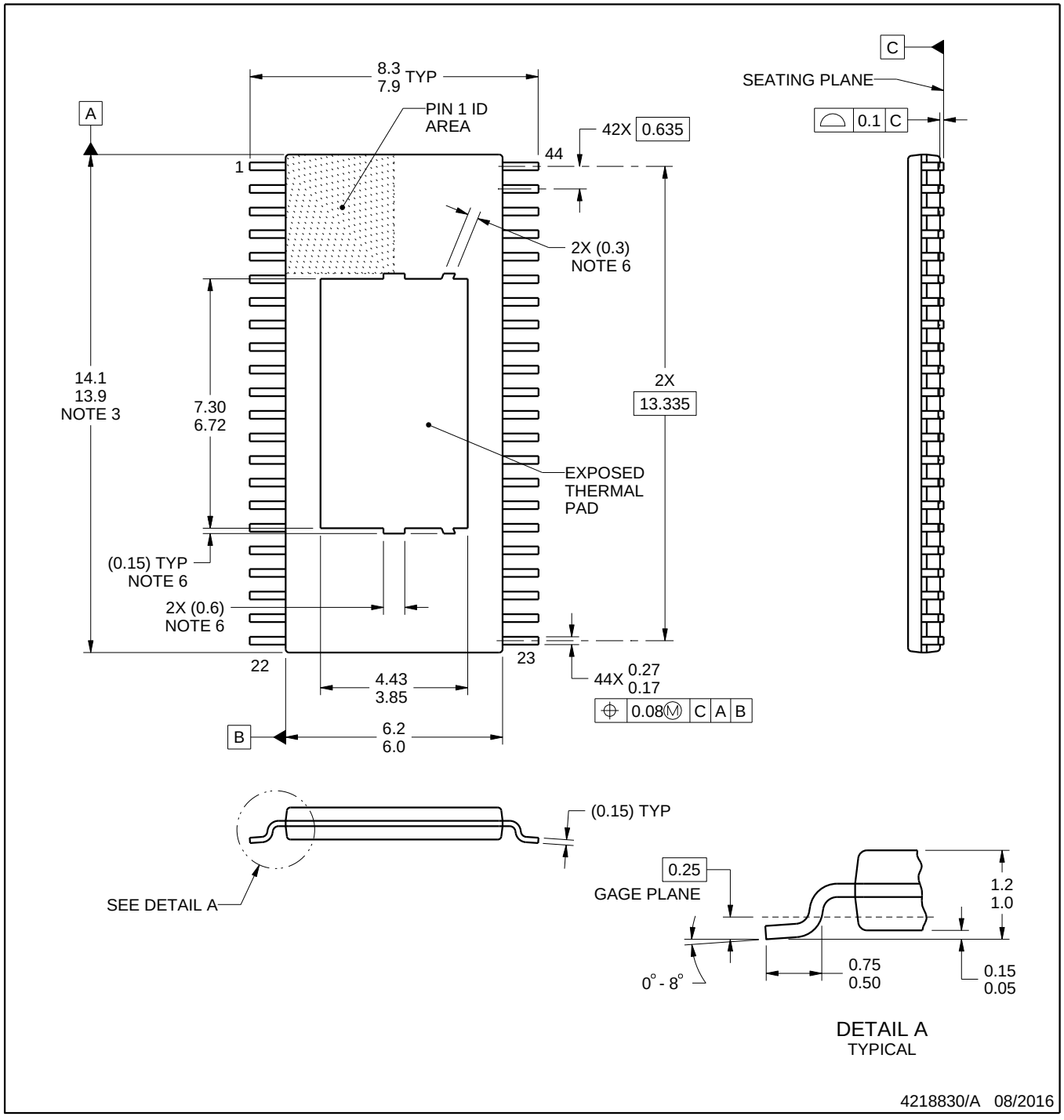


PACKAGE OUTLINE

DDV0044D

PowerPAD™ TSSOP - 1.2 mm max height

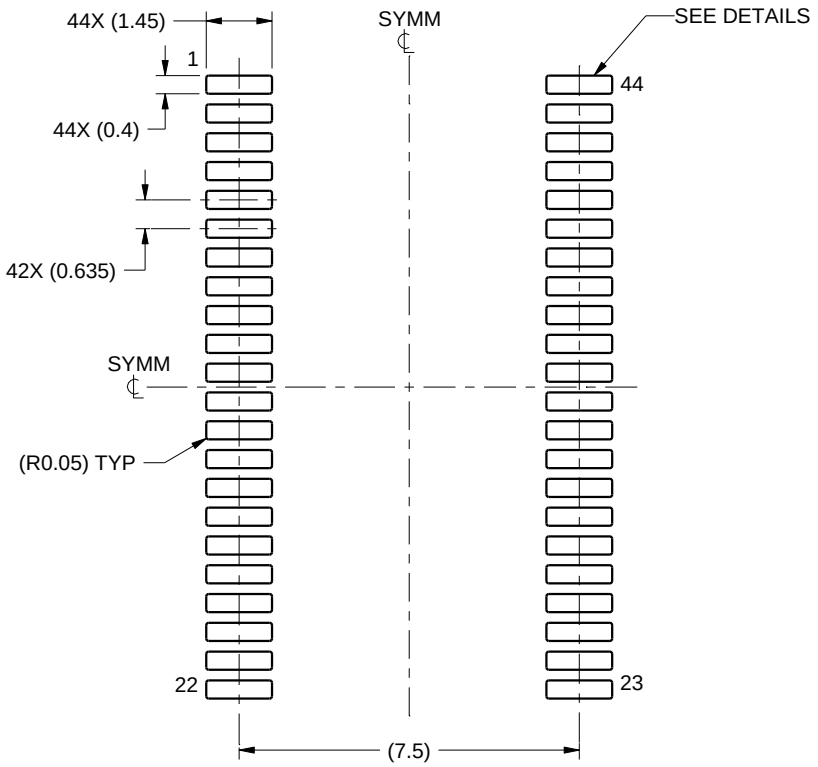
PLASTIC SMALL OUTLINE



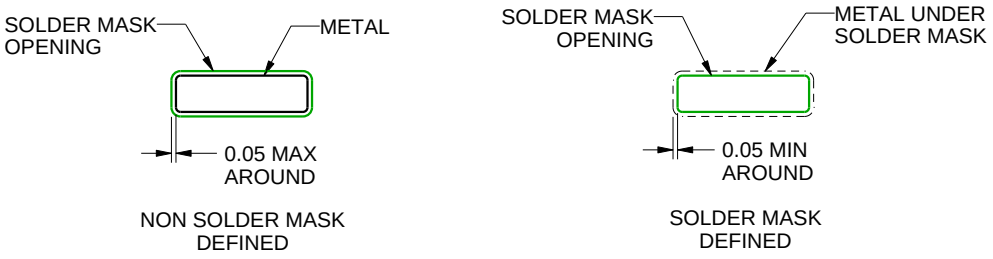
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X

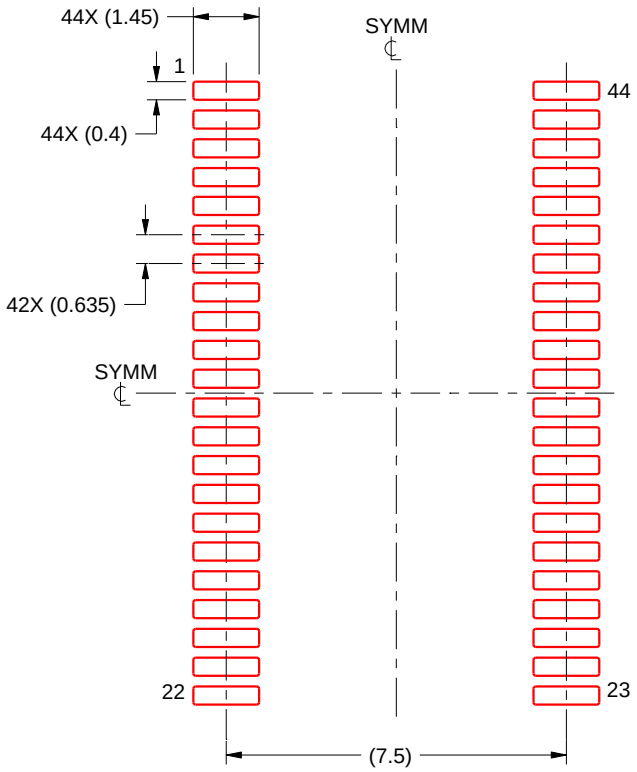


SOLDER MASK DETAILS
NOT TO SCALE

4218830/A 08/2016

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE :6X

4218830/A 08/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265