参考資料

TEXAS INSTRUMENTS

TMUX6111, TMUX6112, TMUX6113

JAJSFY5E –AUGUST 2018–REVISED DECEMBER 2019

TMUX611x ±17V、低容量、低リーク電流、高精度のクワッド SPST スイッチ

1 特長

- 広い電源電圧範囲：±5V～±17V (デュアル)、10V～17V (シングル)
- すべてのピンで、JESD78 Class II Level A準拠の100mAを満たすラッチアップ性能
- 小さいオン容量: 4.2pF
- 低い入力リーク電流: 0.5pA
- 低い電荷注入: 0.6pC
- レール・ツー・レール動作
- 低いオン抵抗: 120Ω
- 高速なスイッチのターンオン時間: 66ns
- Break-Before-Makeのスイッチング動作 (TMUX6113)
- V_{DD}に接続可能なENピン
- 低い消費電流: 17µA
- 人体モデル (HBM) ESD 保護：すべてのピンで±2 kV
- 業界標準のTSSOPと小型のWQFNパッケージ

2 アプリケーション

- ファクトリ・オートメーションと産業プロセス制御
- プログラマブル・ロジック・コントローラ (PLC)
- アナログ入力モジュール
- 半導体試験機器
- バッテリ・テスト機器

3 概要

TMUX6111、TMUX6112、TMUX6113デバイスは、最新のCMOS（相補型金属酸化膜半導体）デバイスで、4つのSPST（単極単投）スイッチを独立に選択可能です。このデバイスは、デュアル電源 (±5V～±17V)、シングル電源 (10V～17V)、非対称電源のいずれでも適切に動作します。すべてのデジタル入力はスレッショルドがTTL (Transistor-Transistor Logic)互換で、TTLおよびCMOS両方のロジックとの互換性が保証されています。

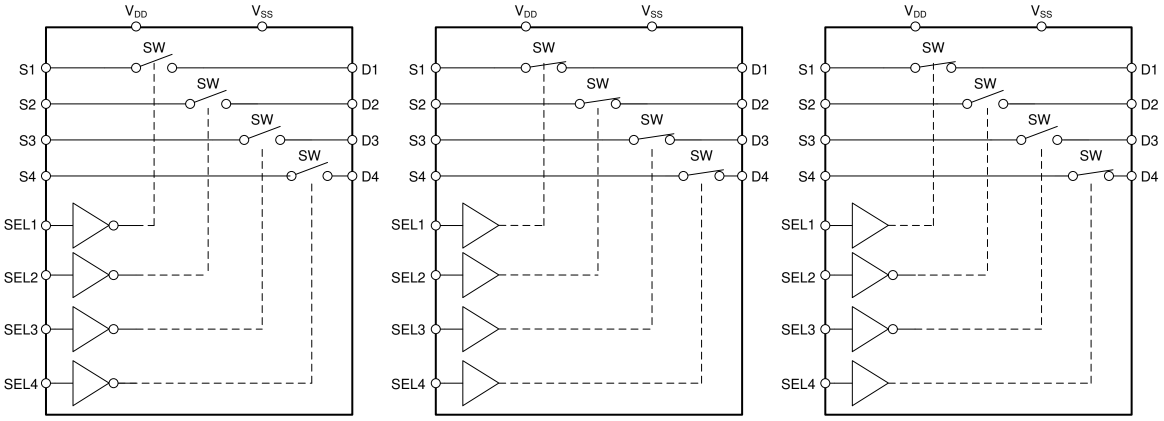
スイッチは、TMUX6111ではデジタル制御入力のロジック0でオンになります。TMUX6112のスイッチをオンにするには、ロジック1が必要です。TMUX6113のスイッチのうち2つはTMUX6111と同様のデジタル制御ロジックで、もう2つのスイッチはロジックが反転しています。TMUX6113は、Break-Before-Makeのスイッチングを行うため、クロスポイントのスイッチング・アプリケーションに使用できます。

製品情報[1]

型番	パッケージ	本体サイズ（公称）
TMUX6111 TMUX6112 TMUX6113	TSSOP (16)	5.00mm×4.40mm
	WQFN (16)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

概略回路図



TMUX6111　TMUX6112　TMUX6113

English Data Sheet: SCDS383

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (January 2019) から Revision E に変更 — Page

- タイトルの「TMUX611x ±16.5V」を「TMUX611x ±17V」に変更 ... 1
- 「特長」の「広い電源電圧範囲:±5V～±16.5V (デュアル)、10V～16.5V (シングル)」を「広い電源電圧範囲:±5V～±17V (デュアル)、10V～17V (シングル)」に変更 ... 1
- 「概要」の「デュアル電源 (±5V～±16.5V)、シングル電源 (10V～16.5V)」を「デュアル電源 (±5V～±17V)、シングル電源 (10V～17V)」に変更 ... 1
- Changed ±16.5-V to ±17.5-V in the Description of the *Device Comparison Table* ... 5
- Changed recommended power supply voltage differential from 33 V to 34 V ... 6
- Changed recommended single supply voltage from 16.5 V to 17 V ... 6
- Changed positive and negative power supply voltage to +17 V and -17V ... 6
- The *Overview* From: dual supplies (±5 V to ±16.5 V) or single supply (10 V to 16.5 V) To: dual supplies (±5 V to ±17 V) or single supply (10 V to 17 V) ... 14
- Changed the *Application Information* From: 16.5 V (single supply) To: 17 V (single supply) ... 21
- The *Power Supply Recommendations* From: wide supply range of of ±5 V to ±16.5 V (10 V to 16.5 V in single-supply mode) To: wide supply range of of ±5 V to ±17 V (10 V to 17 V in single-supply mode) ... 23

Revision C (December 2018) から Revision D に変更 — Page

- Changed descriptions in the *Device Comparison Table* to match the data sheet title ... 5
- 変更 図 30 to correct Op-Amp terminal polarities. ... 21

Revision B (November 2018) から Revision C に変更 — Page

- Changed units for channel current and ambient temperature. ... 7

Revision A (November 2018) から Revision B に変更 **Page**

- TMUX6111 および TMUX6113 のドキュメント・ステータスを製品プレビューから量産データに変更 1

2018年8月発行のものから更新 **Page**

- TMUX6112 のドキュメント・ステータスを事前情報から量産データに変更 1

5 概要（続き）

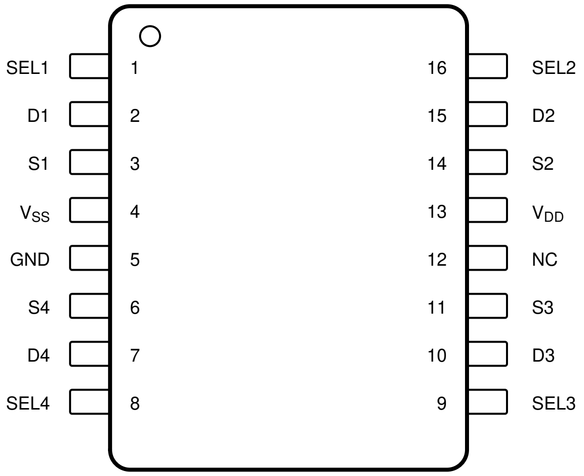
TMUX611xデバイスは、テキサス・インスツルメンツの高精度スイッチおよびマルチプレクサ・ファミリの製品です。これらのデバイスはリーク電流と電荷注入が非常に小さいため、高精度の測定アプリケーションに使用可能です。消費電流が17µAと低いため、携帯型アプリケーションにも使用できます。

6 Device Comparison Table

PRODUCT	DESCRIPTION
TMUX6111	±17-V, Low-Capacitance, Low-Leakage-Current, Precision, Quad SPST Switches (Normally Closed)
TMUX6112	±17-V, Low-Capacitance, Low-Leakage-Current, Precision, Quad SPST Switches (Normally Open)
TMUX6113	±17-V, Low-Capacitance, Low-Leakage-Current, Precision, Quad SPST Switches (Dual Open + Dual Closed)

7 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



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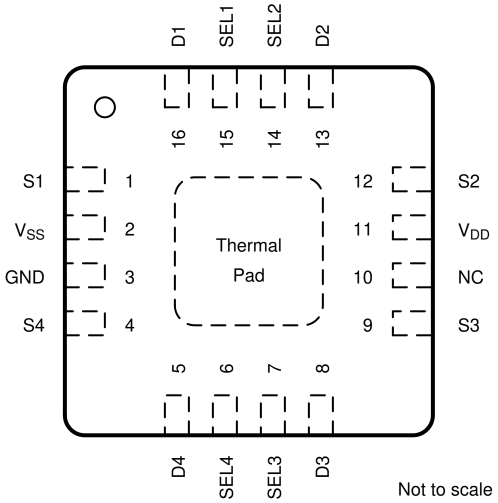
RTE Package
16-Pin WQFN
Top View



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Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	TSSOP	WQFN		
SEL1	1	15	I	Logic control input 1.
D1	2	16	I/O	Drain pin 1. Can be an input or output.
S1	3	1	I/O	Source pin 1. Can be an input or output.
V_{SS}	4	2	P	Negative power supply. This pin is the most negative power-supply potential. In single-supply applications, this pin can be connected to ground. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
GND	5	3	P	Ground (0 V) reference
S4	6	4	I/O	Source pin 4. Can be an input or output.
D4	7	5	I/O	Drain pin 4. Can be an input or output.
SEL4	8	6	I	Logic control input 4.
SEL3	9	7	I	Logic control input 3.
D3	10	8	I/O	Drain pin 3. Can be an input or output.
S3	11	9	I/O	Source pin 3. Can be an input or output.
NC	12	10	–	No internal connection.
V_{DD}	13	11	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
S2	14	12	I/O	Source pin 2. Can be an input or output.
D2	15	13	I/O	Drain pin 2. Can be an input or output.
SEL2	16	14	I	Logic control input 2.
–	-	EP	–	Exposed Pad. The exposed pad is electrically connected to V_{SS} internally. Connect EP to V_{SS} to achieve rated thermal and ESD performance.

(1) I = input, O = output, I/O = input and output, P = power

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		36	V
V_{DD} to GND		–0.3	18	V
V_{SS} to GND		–18	0.3	V
V_{DIG}	Digital input pin (SEL1, SEL2, SEL3, SEL4) voltage	GND –0.3	V_{DD}+0.3	V
I_{DIG}	Digital input pin (SEL1, SEL2, SEL3, SEL4) current	–30	30	mA
V_{ANA_IN}	Analog input pin (Sx) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_IN}	Analog input pin (Sx) current	–30	30	mA
V_{ANA_OUT}	Analog output pin (D) voltage	V_{SS}–0.3	V_{DD}+0.3	V
I_{ANA_OUT}	Analog output pin (D) current	–30	30	mA
T_A	Ambient temperature	–55	140	°C
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Thermal Information

THERMAL METRIC		TMUX6111/ TMUX6112/ TMUX6113		UNIT
		PW (TSSOP)	RTE (QFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	111.0	51.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	53.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.2	26.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.1	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.6	26.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	11.6	°C/W

8.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD} to V_{SS}(1)	Power supply voltage differential	10		34	V
V_{DD} to GND	Positive power supply voltage (singlle supply, V_{SS} = 0 V)	10		17	V
V_{DD} to GND	Positive power supply voltage (dual supply)	5		17	V
V_{SS} to GND	Negative power supply voltage (dual supply)	–5		–17	V
V_S(2)	Source pins voltage	V_{SS}		V_{DD}	V

(1) V_{DD} and V_{SS} can be any value as long as $10\ V \le (V_{DD} – V_{SS}) \le 34\ V$.
(2) V_S is the voltage on all the S pins.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_D	Drain pin voltage	V_{SS}		V_{DD}	V
V_{DIG}	Digital input pin (SEL1, SEL2, SEL3, SEL4) voltage	0		V_{DD}	V
I_{CH}	Channel current (T_A = 25°C)	–25		25	mA
T_A	Ambient temperature	–40		125	°C

8.5 Electrical Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range		T_A = –40°C to +125°C	V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_S = 1 mA			120	135	Ω
		V_S = ±10 V, I_S = 1 mA			140	160	Ω
			T_A = –40°C to +85°C			210	Ω
			T_A = –40°C to +125°C			245	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = ±10 V, I_S = 1 mA			2.5	6	Ω
			T_A = –40°C to +85°C			9	Ω
			T_A = –40°C to +125°C			11	Ω
R_{ON_FLAT}	On-resistance flatness	V_S = –10 V, 0 V, +10 V, I_S = 1 mA			23	33	Ω
			T_A = –40°C to +85°C			37	Ω
			T_A = –40°C to +125°C			38	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.52		%/°C
$I_{S(OFF)}$	Source off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ + 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	-0.14		0.05	nA
			T_A = –40°C to +125°C	–1.3		0.25	nA
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.14		0.05	nA
			T_A = –40°C to +125°C	–1.3		0.25	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = +10 V/ –10 V, V_D = –10 V/ +10 V		–0.04	0.01	0.04	nA
			T_A = –40°C to +85°C	–0.25		0.1	nA
			T_A = –40°C to +125°C	–1.8		0.5	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(IN)}$	Pull-down resistance on SELx pins				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			17	21	μA
			T_A = –40°C to +85°C			22	μA
			T_A = –40°C to +125°C			23	μA
I_{SS}	V_{SS} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			8	10	μA
			T_A = –40°C to +85°C			11	μA
			T_A = –40°C to +125°C			12	μA

(1) When V_S is positive, V_D is negative, and vice versa.

8.6 Switching Characteristics (Dual Supplies: ±15 V)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = -15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		66	78	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			107	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			117	ns
t_{OFF}	Enable turn-off time	V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF		56	68	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			77	ns
		V_S = ±10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			81	ns
tBBM	Break-before-make time delay (TMUX6113 Only)	V_S = 10 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	8	40		ns
Q_J	Charge injection	V_S = 0 V, R_S = 0 Ω , C_L = 1 nF		0.6		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–85		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, adjacent channel		–100		dB
		R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, non-adjacentchannel		–115		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–7.0		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{DD}, f= 1 MHz		–59		dB
		R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V on V_{SS}, f= 1 MHz		–59		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		800		MHz
THD	Total harmonic distortion + noise	R_L = 10k Ω , C_L = 5 pF, f= 20Hz to 20kHz		0.08		%
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.5		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 0 V, f = 1 MHz (PW package)		1.9	3.0	pF
		V_S = 0 V, f = 1 MHz (RTE package)		2.5	3.6	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 0 V, f = 1 MHz		2.4	3.1	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 0 V, f = 1 MHz		4.2	6.0	pF

8.7 Electrical Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_A	Analog signal range	T_A = –40°C to +125°C		V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 10 V, I_S = 1 mA			230	265	Ω
			T_A = –40°C to +85°C			355	Ω
			T_A = –40°C to +125°C			405	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 10 V, I_S = 1 mA			5	12	Ω
			T_A = –40°C to +85°C			19	Ω
			T_A = –40°C to +125°C			23	Ω
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V			0.5		%/°C
$I_{S(OFF)}$	Source off leakage current[1]	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.1		0.04	nA
			T_A = –40°C to +125°C	-1		0.2	nA

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[1] When V_S is positive, V_D is negative, and vice versa.

Electrical Characteristics (Single Supply: 12 V) (continued)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{D(OFF)}$	Drain off leakage current(1)	Switch state is off, V_S = 10 V/ 1 V, V_D = 1 V/ 10 V		–0.02	0.005	0.02	nA
			T_A = –40°C to +85°C	–0.1		0.04	nA
			T_A = –40°C to +125°C	–1		0.2	nA
$I_{D(ON)}$	Drain on leakage current	Switch state is on, V_S = floating, V_D = 1 V/ 10 V		–0.04	0.01	0.04	nA
			T_A = –40°C to +85°C	–0.16		0.08	nA
			T_A = –40°C to +125°C	–1.4		0.4	nA
DIGITAL INPUT (SELx pins)							
V_{IH}	Logic voltage high			2			V
V_{IL}	Logic voltage low					0.8	V
$R_{PD(EN)}$	Pull-down resistance on SELx pins				6		MΩ
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_A = 0 V or 3.3 V, V_S = 0 V			13	16	µA
			T_A = –40°C to +85°C			17	µA
			T_A = –40°C to +125°C			18	µA

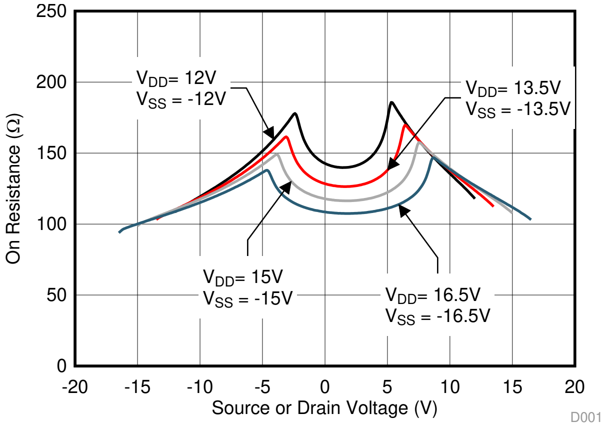
8.8 Switching Characteristics (Single Supply: 12 V)

at T_A = 25°C, V_{DD} = 12 V, and V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Enable turn-on time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		72	84	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			117	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			128	ns
t_{OFF}	Enable turn-off time	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF		57	66	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +85°C			78	ns
		V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C			84	ns
t_{BBM}	Break-before-make time delay (TMUX6113 only)	V_S = 8 V, R_L = 300 Ω , C_L = 35 pF, T_A = –40°C to +125°C	17	47		ns
Q_J	Charge injection	V_S = 0 V to 12 V, R_S = 0 Ω , C_L = 1 nF		0.6		pC
O_{ISO}	Off-isolation	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		–86		dB
X_{TALK}	Channel-to-channel crosstalk	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, adjacent channel		–98		dB
		R_L = 50 Ω , C_L = 5 pF, f = 1 MHz, non-adjacent channel		–117		dB
I_L	Insertion loss	R_L = 50 Ω , C_L = 5 pF, f = 1 MHz		-14		dB
ACPSRR	AC Power Supply Rejection Ratio	R_L = 10 kΩ , C_L = 5 pF, V_{PP}= 0.62 V, f= 1 MHz		–59		dB
BW	-3dB Bandwidth	R_L = 50 Ω , C_L = 5 pF		750		MHz
C_{IN}	Digital input capacitance	V_{IN} = 0 V or V_{DD}		1.6		pF
$C_{S(OFF)}$	Source off-capacitance	V_S = 6 V, f = 1 MHz (PW package)		2.2	3.1	pF
		V_S = 6 V, f = 1 MHz (RTE package)		2.9	4.0	pF
$C_{D(OFF)}$	Drain off-capacitance	V_S = 6 V, f = 1 MHz		2.8	3.5	pF
$C_{S(ON)}$, $C_{D(ON)}$	Source and drain on-capacitance	V_S = 6 V, f = 1 MHz		4.6	6.3	pF

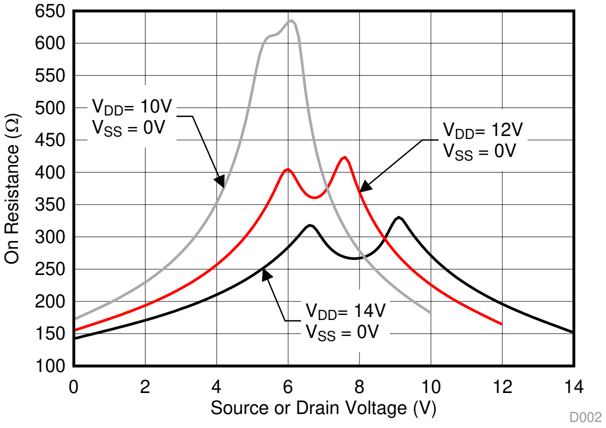
8.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



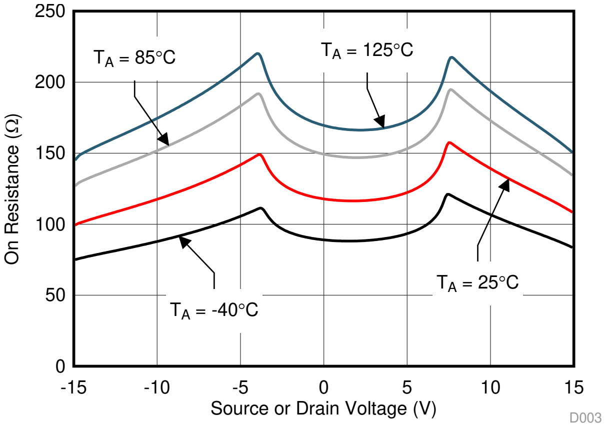
Dual Supply Operation (T_A = 25°C)

図 1. On-Resistance vs Source or Drain Voltage



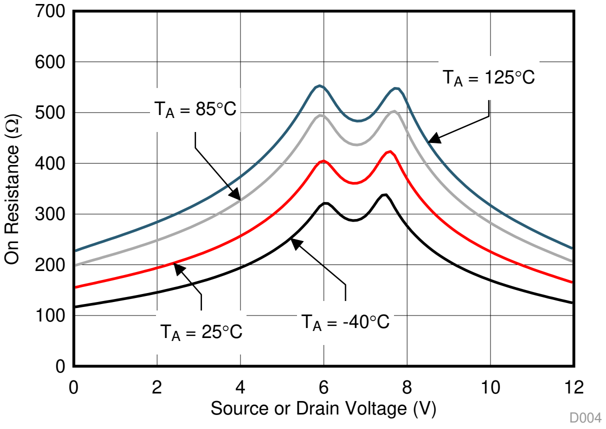
Single Supply Operation (T_A = 25°C)

図 2. On-Resistance vs Source or Drain Voltage



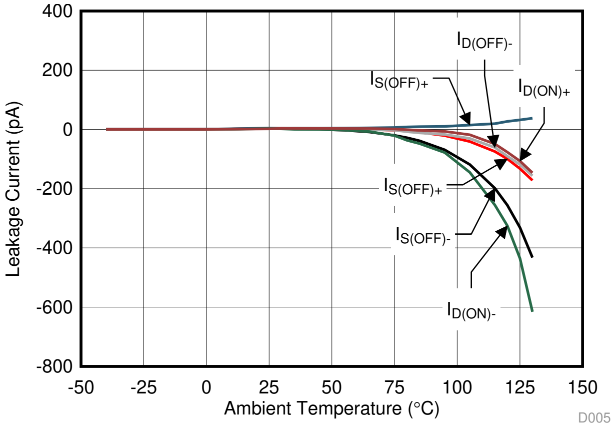
V_{DD} = 15 V, V_{SS} = –15 V

図 3. On-Resistance vs Source or Drain Voltage



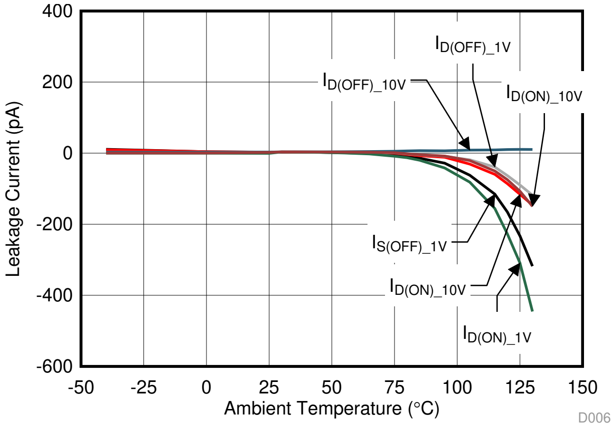
V_{DD} = 12 V, V_{SS} = 0 V

図 4. On-Resistance vs Source or Drain Voltage



V_{DD} = 15 V, V_{SS} = –15 V

図 5. Leakage Current vs Temperature

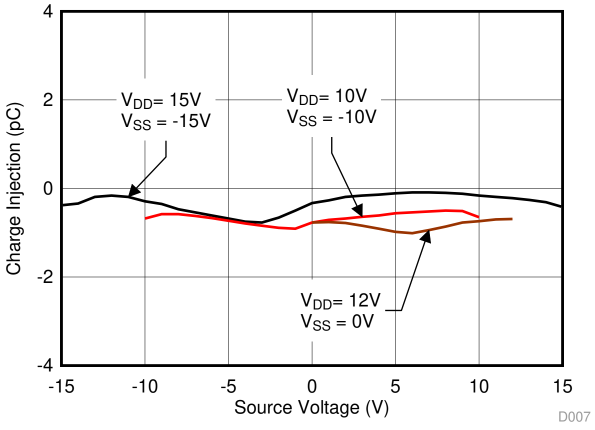


V_{DD} = 12 V, V_{SS} = 0 V

図 6. Leakage Current vs Temperature

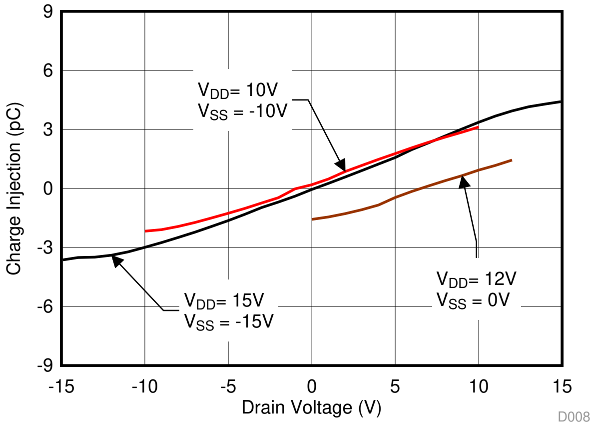
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



T_A = 25°C

図 7. Charge Injection vs Source Voltage



T_A = 25°C

図 8. Charge Injection vs Drain Voltage

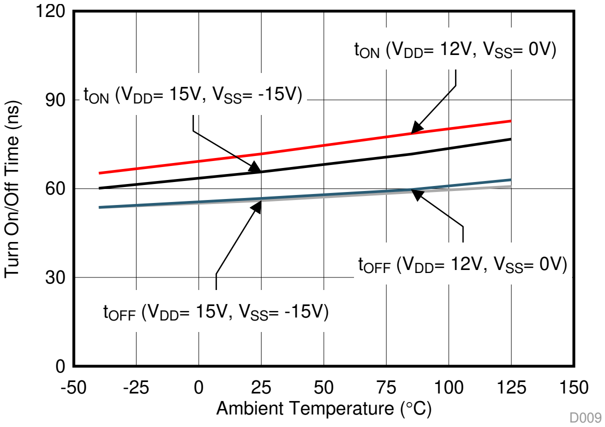
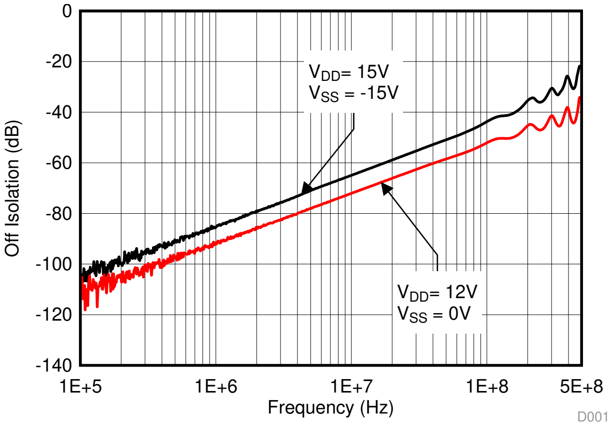
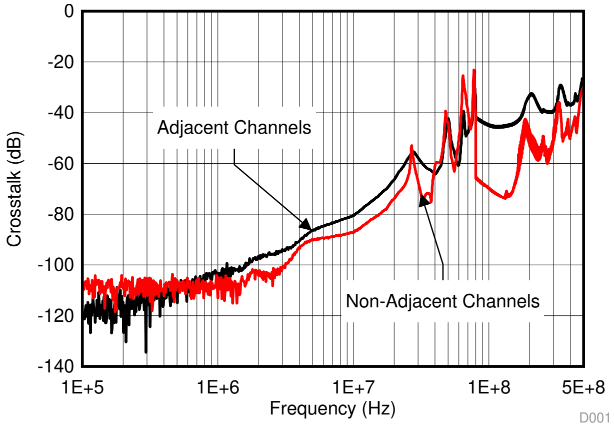


図 9. Turn-On and Turn-Off Times vs Temperature



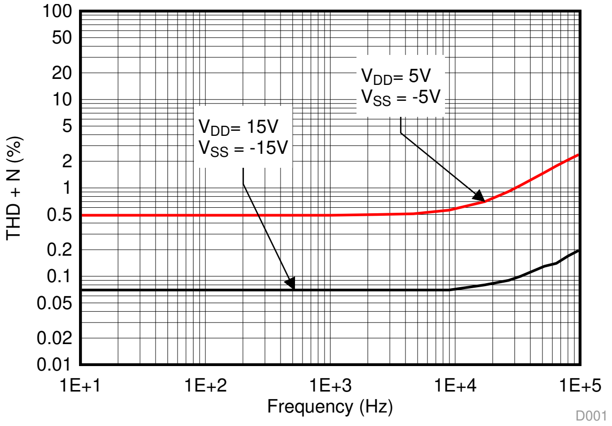
T_A = 25°C

図 10. Off Isolation vs Frequency



V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 11. Crosstalk vs Frequency

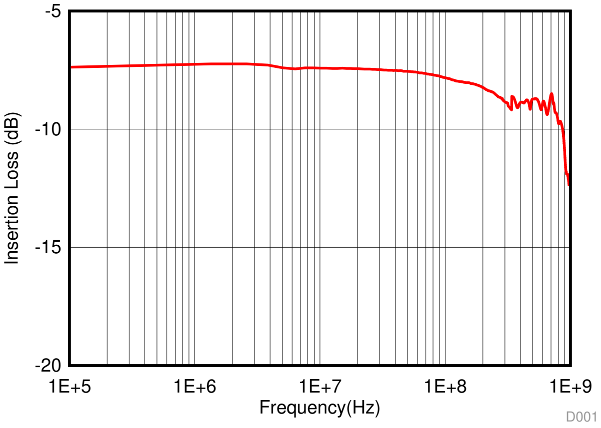


T_A = 25°C

図 12. THD+N vs Frequency

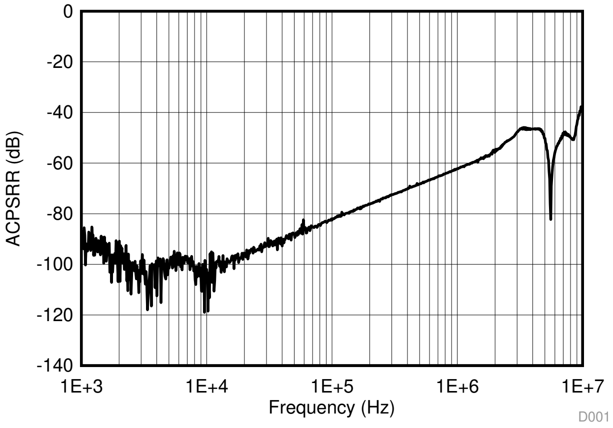
Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



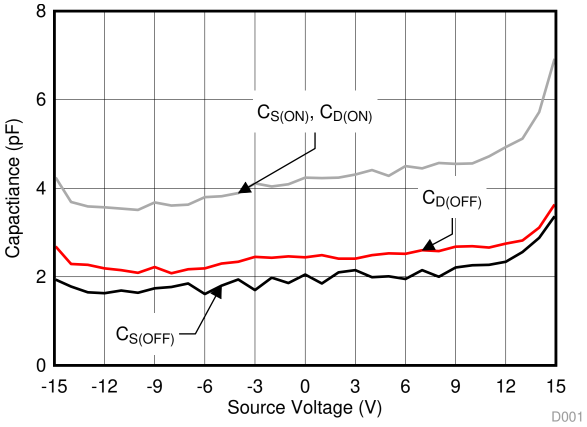
V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 13. On Response vs Frequency



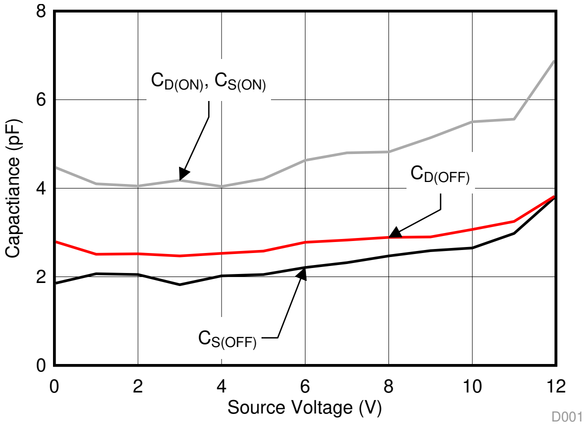
V_{DD} = 15 V, V_{SS} = –15 V, V_{PP}= 0.62 V, T_A = 25°C

図 14. ACPSRR vs Frequency



V_{DD} = 15 V, V_{SS} = –15 V, T_A = 25°C

図 15. Capacitance vs Source Voltage



V_{DD} = 12 V, V_{SS} = 0 V, T_A = 25°C

図 16. Capacitance vs Source Voltage

9 Parameter Measurement Information

9.1 Truth Tables

表 1, 表 2, 表 3and show the truth tables for the TMUX6111, TMUX6112, and TMUX6113, respectively.

表 1. TMUX6111 Truth Table

SELx	STATE
0	All Switch ON
1	All Switch OFF

表 2. TMUX6112 Truth Table

SELx	STATE
0	All Switch OFF
1	All Switch ON

表 3. TUMUX6113 Truth Table

SELx	STATE
0	Switch 1, 4 OFF Switch 2, 3 ON
1	Switch 1, 4 ON Switch 2, 3 OFF

10 Detailed Description

10.1 Overview

The TMUX6111, TMUX6112, and TMUX6113 are 4-channel single-pole/ single-throw (SPDT) switches that supports dual supplies (±5 V to ±17 V) or single supply (10 V to 17 V) operation. Each channel of the switch is turned on or turned off based on the state of its corresponding SELx pin. The Functional Block Diagram section provides a top-level block diagram of the switches.

10.1.1 On-Resistance

The on-resistance of the TMUX6111, TMUX6112, and TMUX6113 is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 図 17. Voltage (V) and current (I_{CH}) are measured using this setup, and R_{ON} is computed as shown in 式 1:

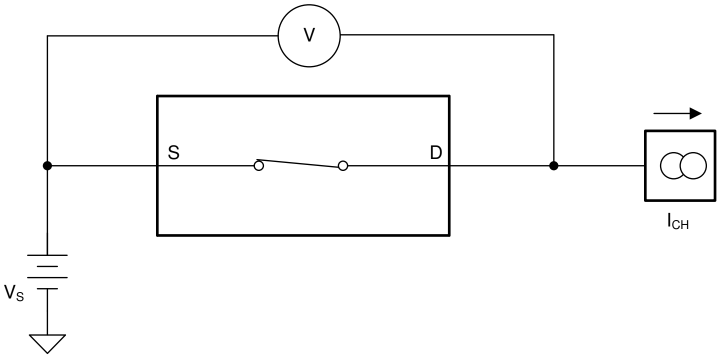


図 17. On-Resistance Measurement Setup

$$R_{ON} = V / I_{CH} \tag{1}$$

10.1.2 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current
2. Drain off-leakage current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

Drain leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is off. This current is denoted by the symbol $I_{D(OFF)}$.

The setup used to measure both off-leakage currents is shown in 図 18

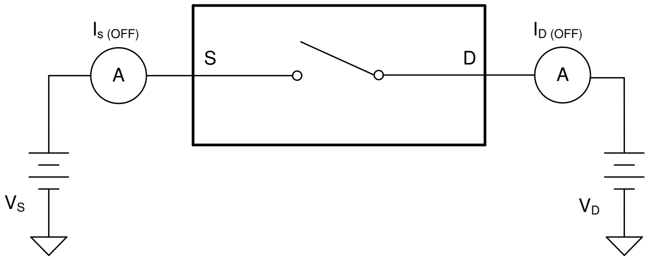


図 18. Off-Leakage Measurement Setup

Overview (continued)

10.1.3 On-Leakage Current

On-leakage current is defined as the leakage current that flows into or out of the drain pin when the switch is in the on state. The source pin is left floating during the measurement. 図 19 shows the circuit used for measuring the on-leakage current, denoted by $I_{D(ON)}$.

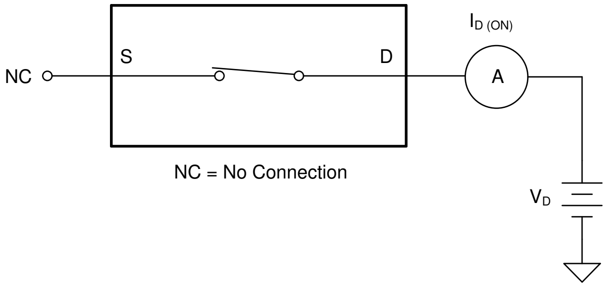


図 19. On-Leakage Measurement Setup

10.1.4 Break-Before-Make Delay

The break-before-make delay is a safety feature of the TMUX6113 switch. The TMUX6113's ON switches first break the connection before the OFF switches make connection. The time delay between the *break* and the *make* is known as break-before-make delay. 図 20 shows the setup used to measure break-before-make delay, denoted by the symbol t_{BBM}.

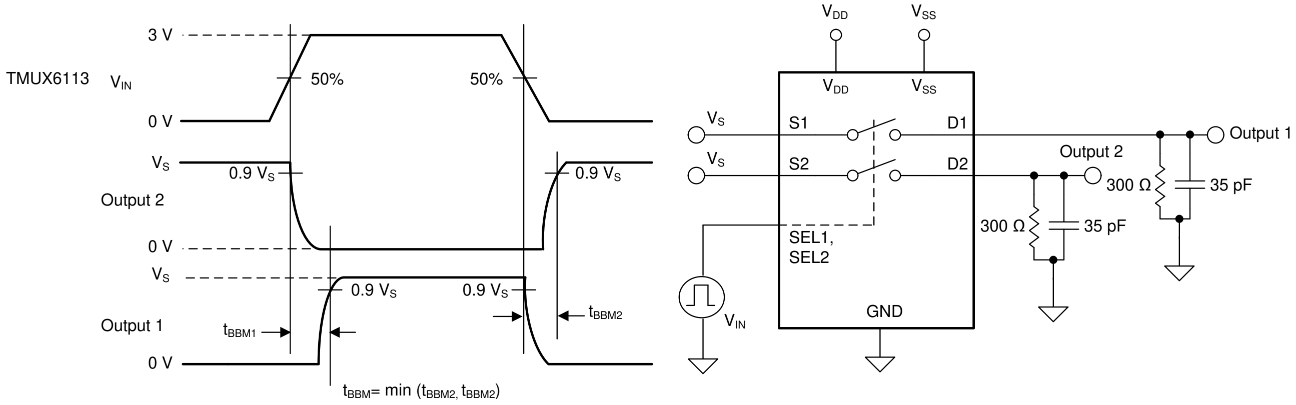


図 20. Break-Before-Make Delay Measurement Setup

10.1.5 Turn-On and Turn-Off Time

Turn-on time is defined as the time taken by the output of the TMUX6111, TMUX6112, and TMUX6113 to rise to a 90% final value after the SELx signal has risen (for NC switches) or fallen (for NO switches) to a 50% final value. 図 21 shows the setup used to measure turn-on time. Turn-on time is denoted by the symbol t_{ON}.

Turn off time is defined as the time taken by the output of the TMUX6111, TMUX6112, and TMUX6113 to fall to a 10% initial value after the SELx signal has fallen (for NC switches) or risen (for NO switches) to a 50% initial value. 図 21 shows the setup used to measure turn-off time. Turn-off time is denoted by the symbol t_{OFF}.

Overview (continued)

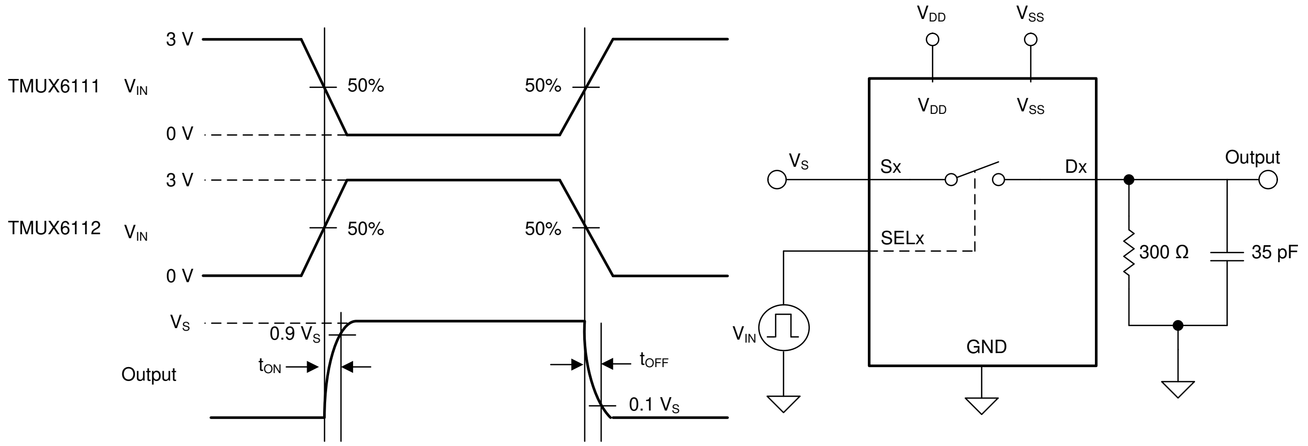


図 21. Turn-On and Turn-Off Time Measurement Setup

10.1.6 Charge Injection

The TMUX6111, TMUX6112, and TMUX6113 have a simple transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_{INJ}. 図 22 shows the setup used to measure charge injection.

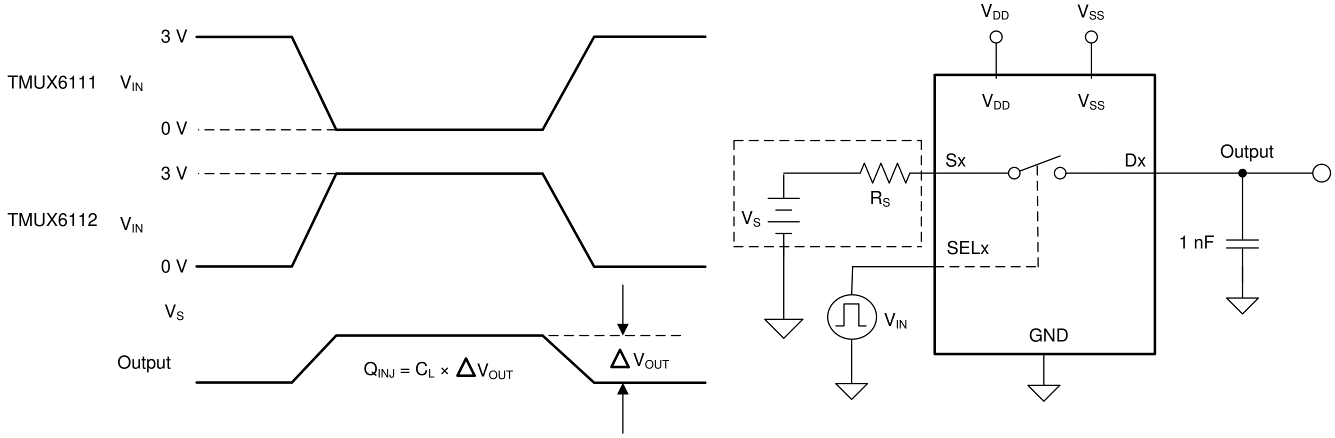


図 22. Charge-Injection Measurement Setup

10.1.7 Off Isolation

Off isolation is defined as the voltage at the drain pin (Dx) of the TMUX6111, TMUX6112, and TMUX6113 when a 1-V_{RMS} signal is applied to the source pin (Sx) of an OFF switch. 図 23 shows the setup used to measure off isolation. Use 式 2 to compute off isolation.

Overview (continued)

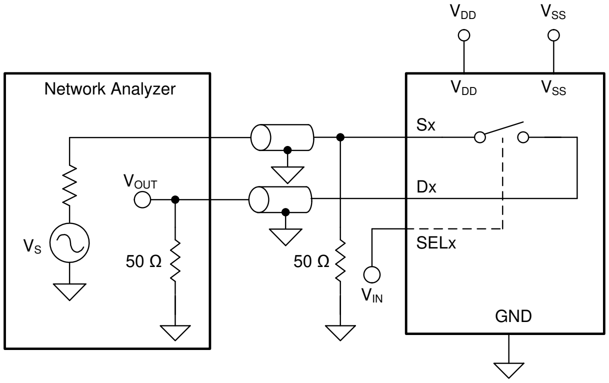


図 23. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{2}$$

10.1.8 Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is defined as the voltage at the source pin (Sx) of an off-channel, when a 1-V_{RMS} signal is applied at the source pin of an on-channel. 図 24 shows the setup used to measure, and 式 3 is the equation used to compute, channel-to-channel crosstalk.

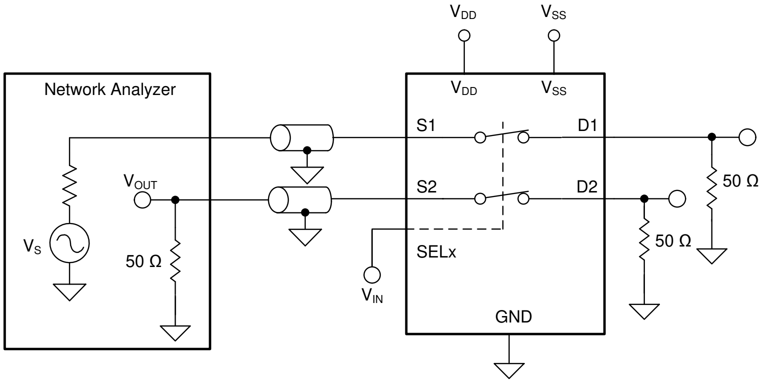


図 24. Channel-to-Channel Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \tag{3}$$

10.1.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (Dx) of the TMUX6111, TMUX6112, and TMUX6113. 図 25 shows the setup used to measure bandwidth of the switch. Use 式 4 to compute the attenuation.

Overview (continued)

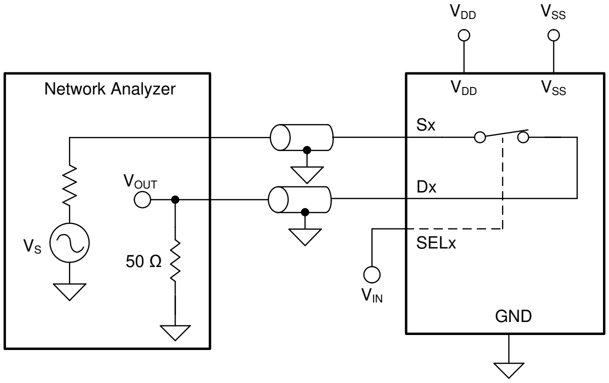


図 25. Bandwidth Measurement Setup

$$\text{Attenuation} = 20 \cdot \text{Log}\left(\frac{V_2}{V_1}\right) \tag{4}$$

10.1.10 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the mux output. The on-resistance of the TMUX6111, TMUX6112, and TMUX6113 varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. 図 26 shows the setup used to measure THD+N of the TMUX6111, TMUX6112, and TMUX6113.

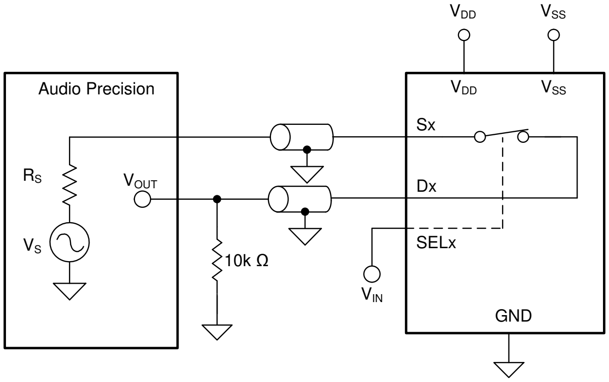
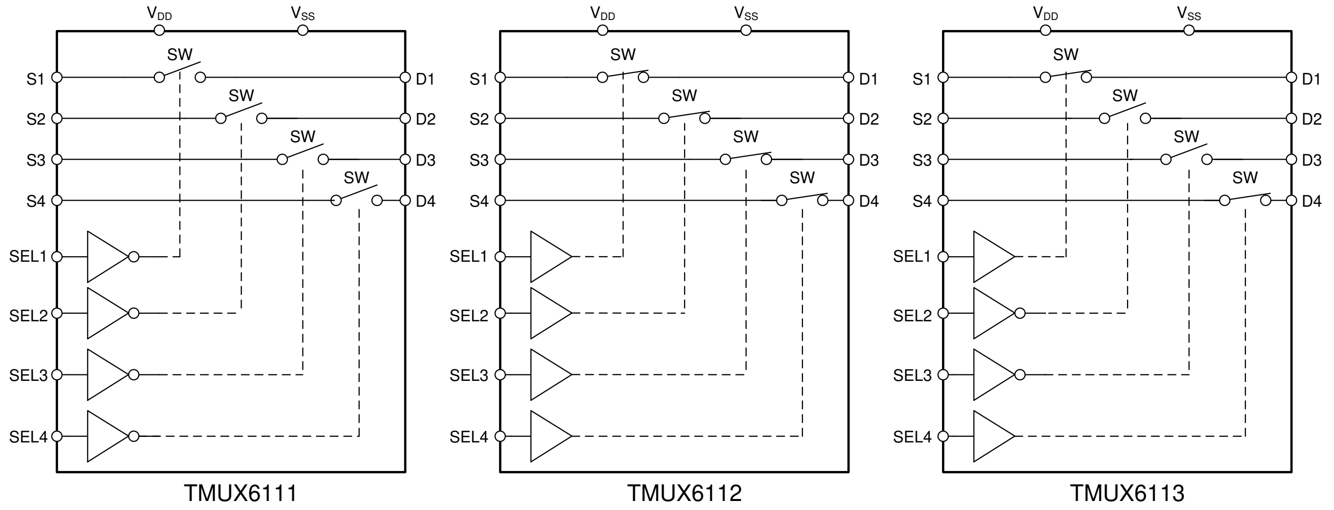


図 26. THD+N Measurement Setup

10.2 Functional Block Diagram



10.3 Feature Description

10.3.1 Ultra-low Leakage Current

The TMUX6111, TMUX6112, and TMUX6113 provide extremely low on- and off-leakage currents. The devices are capable of switching signals from high source-impedance inputs into a high input-impedance op amp with minimal offset error because of the ultralow leakage currents. 図 27 shows typical leakage currents of the devices versus temperature.

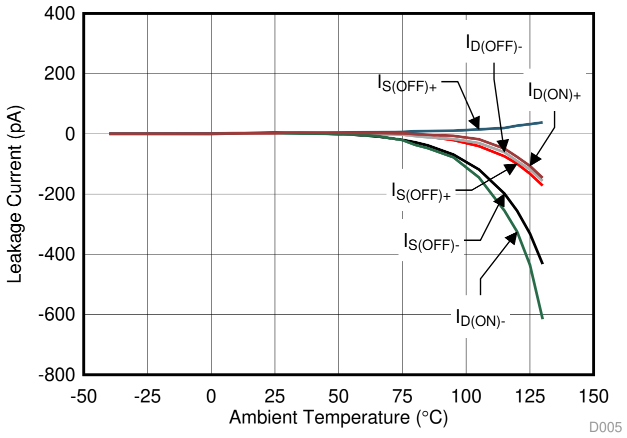


図 27. Leakage Current vs Temperature

10.3.2 Ultra-low Charge Injection

The TMUX6111, TMUX6112, and TMUX6113 are implemented with simple transmission gate topology, as shown in 図 28. Any mismatch in the stray capacitance associated with the NMOS and PMOS causes an output level change whenever the switch is opened or closed. The devices utilize special charge-injection cancellation circuitry that reduces the source (Sx)-to-drain (Dx) charge injection to as low as 0.6 pC at V_S = 0 V, as shown in 図 29.

Feature Description (continued)

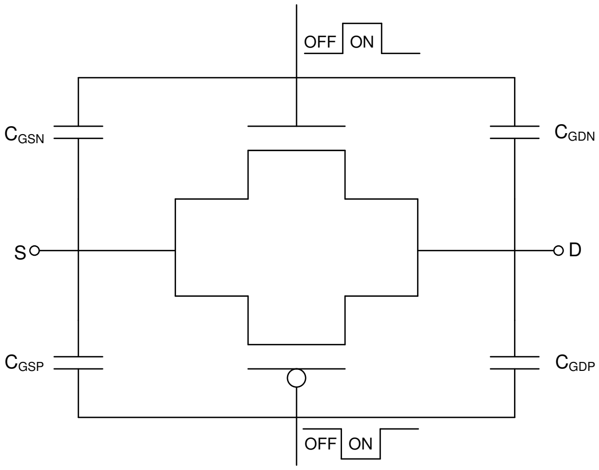


図 28. Transmission Gate Topology

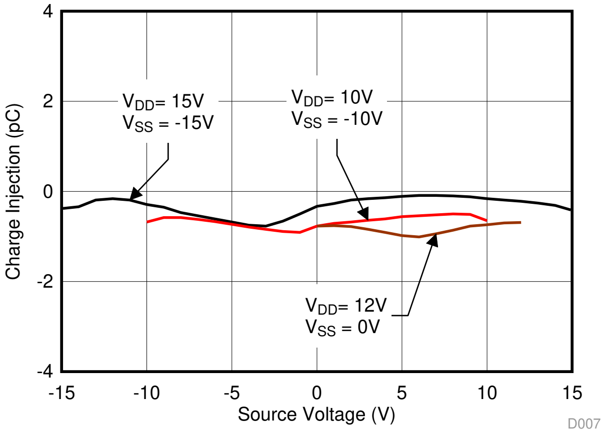


図 29. Source-to-Drain Charge Injection vs Source or Drain Voltage

10.3.3 Bidirectional and Rail-to-Rail Operation

The TMUX6111, TMUX6112, and TMUX6113 conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each channel of the switches has very similar characteristics in both directions. The input signal to the devices swings from V_{SS} to V_{DD} without any significant degradation in performance. The on-resistance of these devices varies with input signal.

10.4 Device Functional Modes

Each channel of the TMUX6111, TMUX6112, and TMUX6113 is turned on or turned off based on the state of its corresponding SELx pin. The SELx pins are weakly pulled-down through an internal 6 MΩ resistor, allowing the switches to stay in a determined state when power is applies to the devices. The SELx pins can be connected to V_{DD}.

11 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The TMUX6111, TMUX6112, and TMUX6113 offer outstanding input/output leakage currents and ultralow charge injection. These devices operate up to 34 (dual supply) or 17 V (single supply), and offer true rail-to-rail input and output. The on-capacitance of the TMUX6111, TMUX6112, and TMUX6113 is low. These features makes the TMUX6111, TMUX6112, and TMUX6113 a family of precision, robust, high-performance analog multiplexer for high-voltage, industrial applications.

11.2 Typical Application

One useful application to take advantage of TMUX6111, TMUX6112, and TMUX6113's precision performance is the sample and hold circuit. A sample and hold circuit can be useful for an analog to digital converter (ADC) to sample a varying input voltage with improved reliability and stability. It can also be used to store the output samples from a single digital-to-analog converter (DAC) in a multi-output application. A simple sample and hold circuit can be realized using an analog switch like one of the TMUX6111, TMUX6112, and TMUX6113 analog switches.

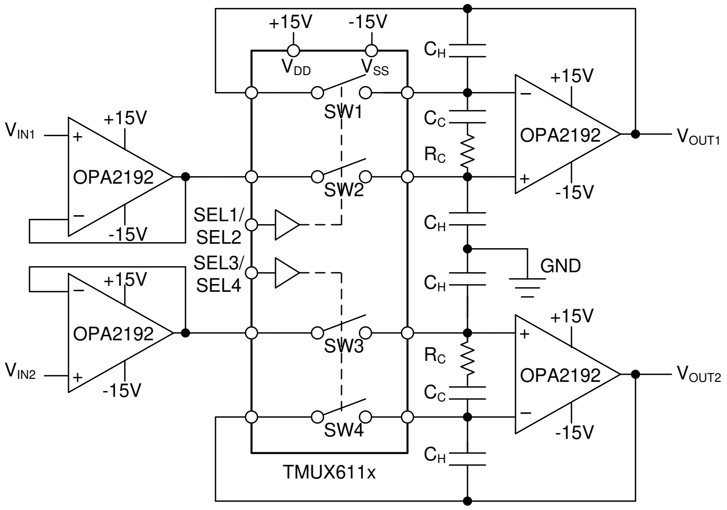


図 30. A 2-output Sample and Hold Circuit Realized Using the TMUX611x Analog Switch

Typical Application (continued)

11.2.1 Design Requirements

The purpose of this precision design is to implement an optimized 2-output sample and hold circuit using a 4-channel SPST switch. The sample and hold circuit needs to be capable of supporting high voltage output swing up to ± 15V with minimized pedestal error and fast settling time. The overall system block diagram is illustrated in 図 30.

11.2.2 Detailed Design Procedure

The TMUX6111, TMUX6112, or TMUX6113 switch is used in conjunction with the voltage holding capacitors (C_H) to implement the sample and hold circuit. The basic operation is:

1. When the switch (SW2 or SW3) is closed, it samples the input voltage and charges the holding capacitors (C_H) to the input voltages values.
2. When the switch (SW2 or SW3) is open, the holding capacitors (C_H) holds its previous value, maintaining stable voltage at the amplifier output (V_{OUT}).

Ideally, the switch delivers only the input signals to the holding capacitors. However, when the switch gets toggled, some amount of charge also gets transferred to the switch output in the form of charge injection, resulting slight sampling error. The TMUX6111, TMUX6112, and TMUX6113 switches have excellent charge injection performance of only 0.6 pC, making them ideal choices for this implementation to minimize sampling error.

Due to switch and capacitor leakage current, the voltage on the hold capacitors droops with time. The TMUX6111, TMUX6112, and TMUX6113 minimize the droops due to its ultra-low leakage performance. At 25°C, the TMUX6111, TMUX6112, and TMUX6113 have extremely tiny leakage current at 1 pA typical and 20 pA max.

The TMUX6111, TMUX6112, and TMUX6113 devices also support high voltage capability. The devices support up to ± 17 V dual supply operation, making it an ideal solution in this high voltage sample and hold application.

A second switch SW1 (or SW4) is also included to operate in parallel with SW2 (or SW3) to reduce pedestal error during switch toggling. Because both switches are driven at the same potential, they act as common-mode signal to the op-amp, thereby minimizing the charge injection effects caused by the switch toggling action. Compensation network consisting of R_C and C_C is also added to further reduce the pedestal error, whiling reducing the hold-time glitch and improving the settling time of the circuit.

11.3 Application Curves

TMUX6111, TMUX6112, and TMUX6113 have excellent charge injection performance of only 0.6 pC (typical), making them ideal choices to minimize sampling error for the sample and hold application. 図 31 shows the plot for the charge injection vs. source input voltage for TMUX6111, TMUX6112, and TMUX6113.

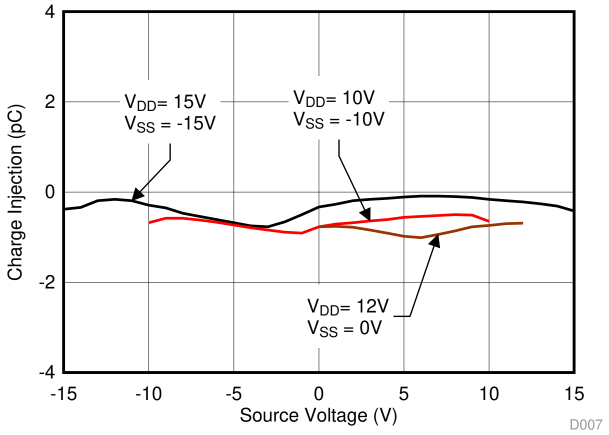


図 31. Charge injection vs. Source Voltage for TMUX6111, TMUX6112 and TMUX6113

12 Power Supply Recommendations

The TMUX6111, TMUX6112, and TMUX6113 operate across a wide supply range of ±5 V to ±17 V (10 V to 17 V in single-supply mode). They also perform well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF at both the V_{DD} and V_{SS} pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped. As a best practice, it is recommended to ramp V_{SS} first before V_{DD} in dual or asymmetrical supply applications.

The on-resistance of the devices varies with supply voltage, as illustrated in 図 32

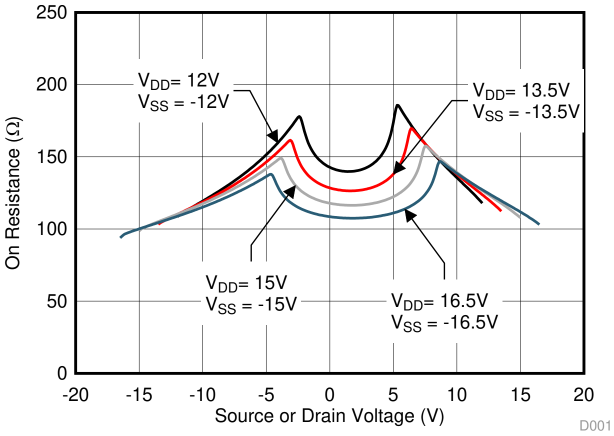


図 32. On-Resistance Variation With Supply and Input Voltage

13 Layout

13.1 Layout Guidelines

図 33 illustrates an example of a PCB layout with the TMUX6112PW. Some key considerations are:

- Decouple the V_{DD} and V_{SS} pins with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} and V_{SS} supplies.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

13.2 Layout Example

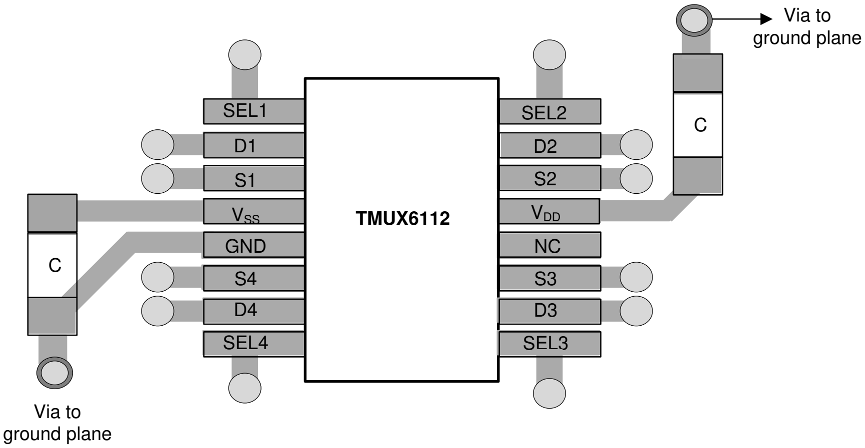


図 33. TMUX6112PW Layout Example

14 デバイスおよびドキュメントのサポート

14.1 ドキュメントのサポート

14.1.1 関連資料

- *『OPAx192 36V、レール・ツー・レール入力/出力、低オフセット電圧、低入力バイアス電流オペアンプ、e-trim™搭載』* (SBOS620E)

14.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TMUX6111	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TMUX6112	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TMUX6113	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

14.3 ドキュメントの更新通知を受け取る方法

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14.4 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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14.5 商標

E2E is a trademark of Texas Instruments.

14.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

14.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

15 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX6111PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6111	Samples
TMUX6111RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM6111	Samples
TMUX6112PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6112	Samples
TMUX6112RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM6112	Samples
TMUX6113PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MUX6113	Samples
TMUX6113RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM6113	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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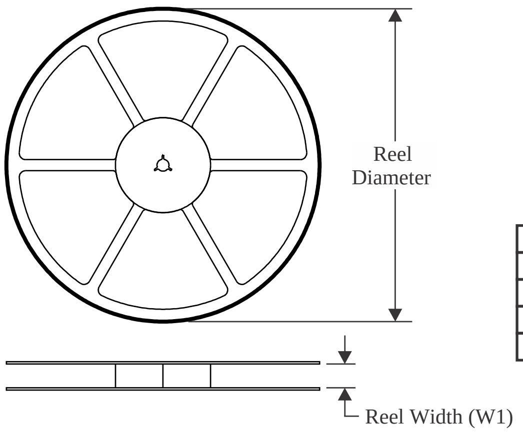
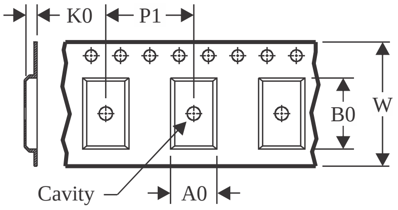
TAPE AND REEL INFORMATION

REEL DIMENSIONS

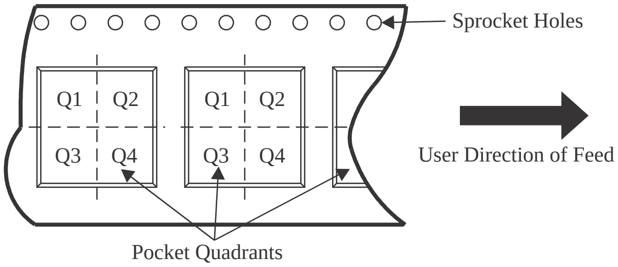


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

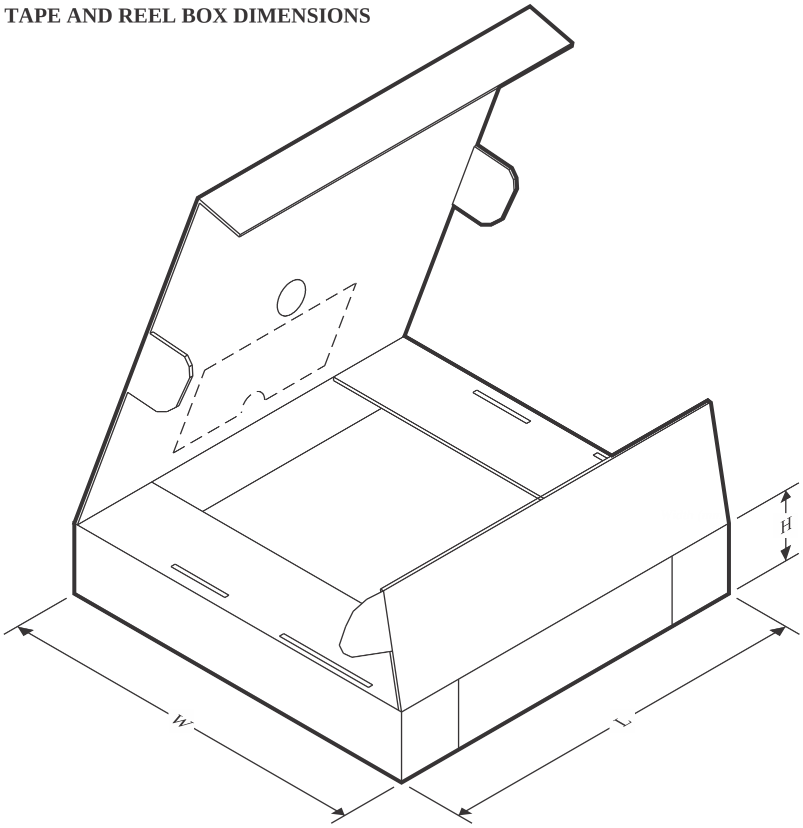
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX6111PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX6111RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TMUX6112PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX6112RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TMUX6113PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TMUX6113RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

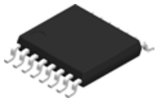
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX6111PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TMUX6111RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TMUX6112PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TMUX6112RTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TMUX6113PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TMUX6113RTER	WQFN	RTE	16	3000	367.0	367.0	35.0

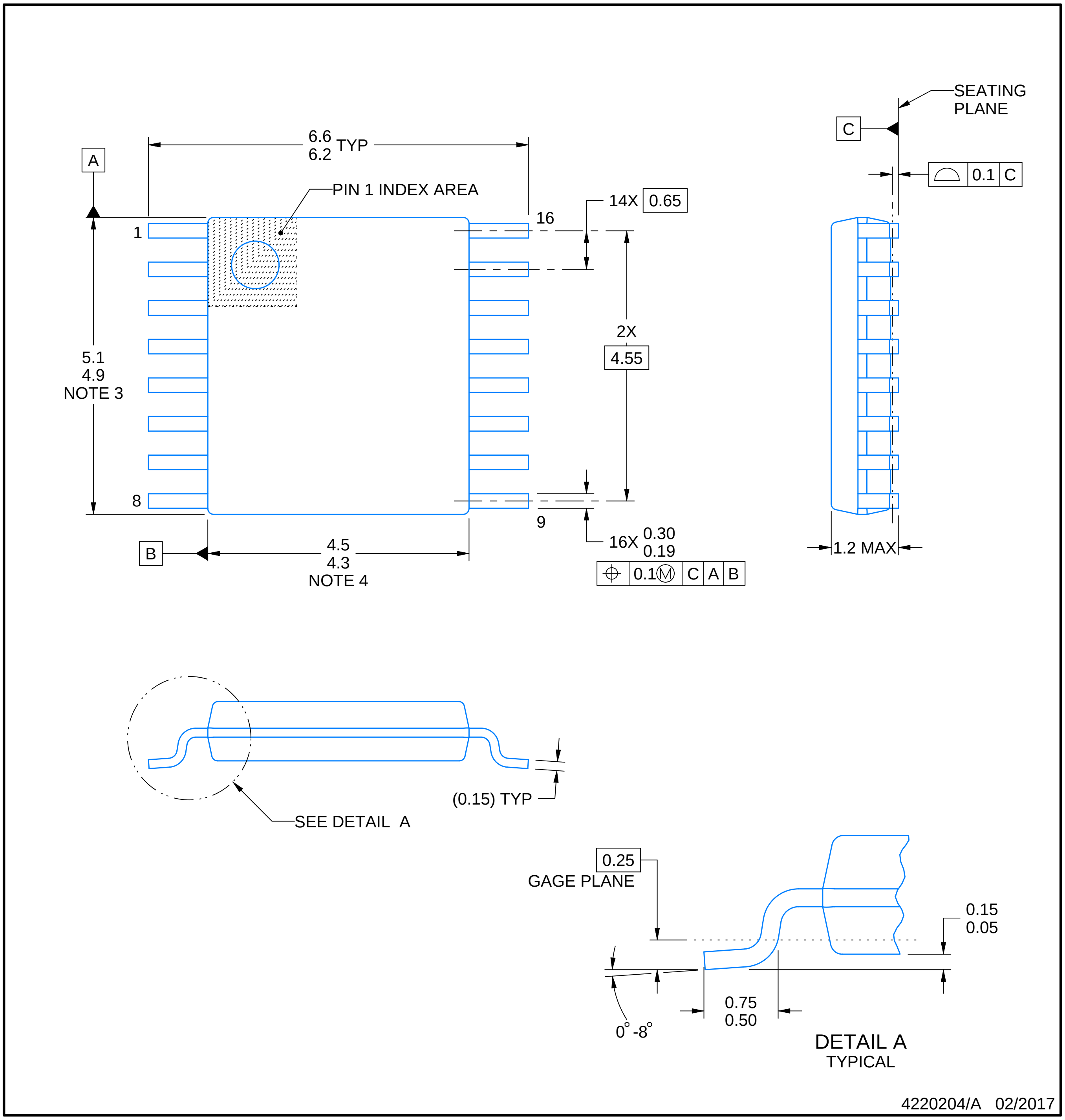
PACKAGE OUTLINE



PW0016A

TSSOP - 1.2 mm max height

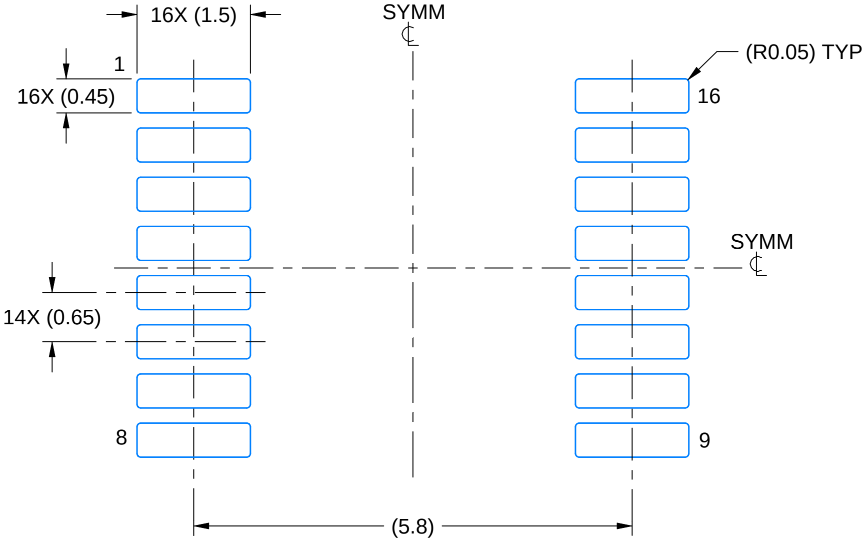
SMALL OUTLINE PACKAGE



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

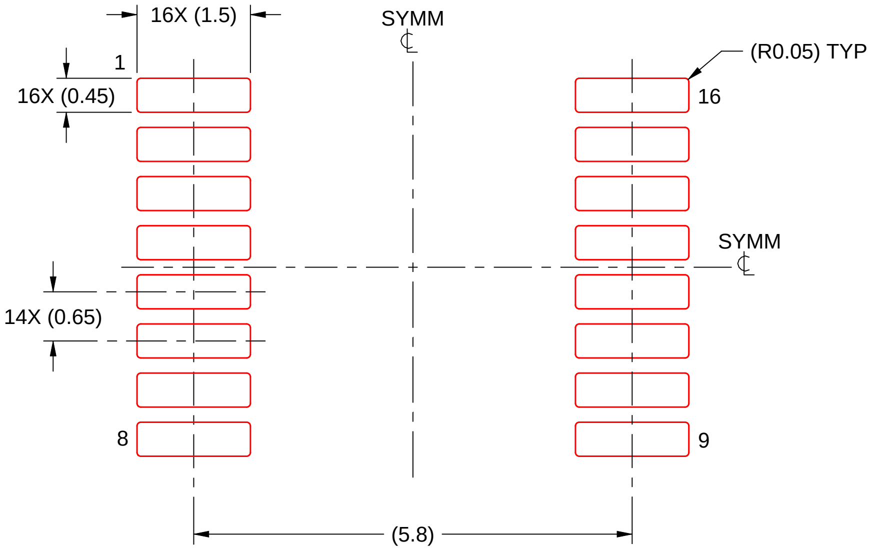
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

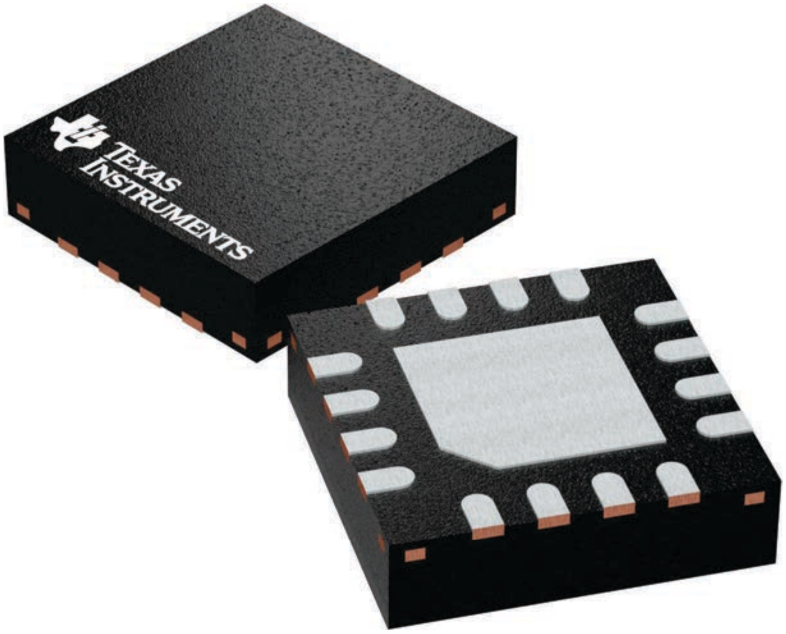
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

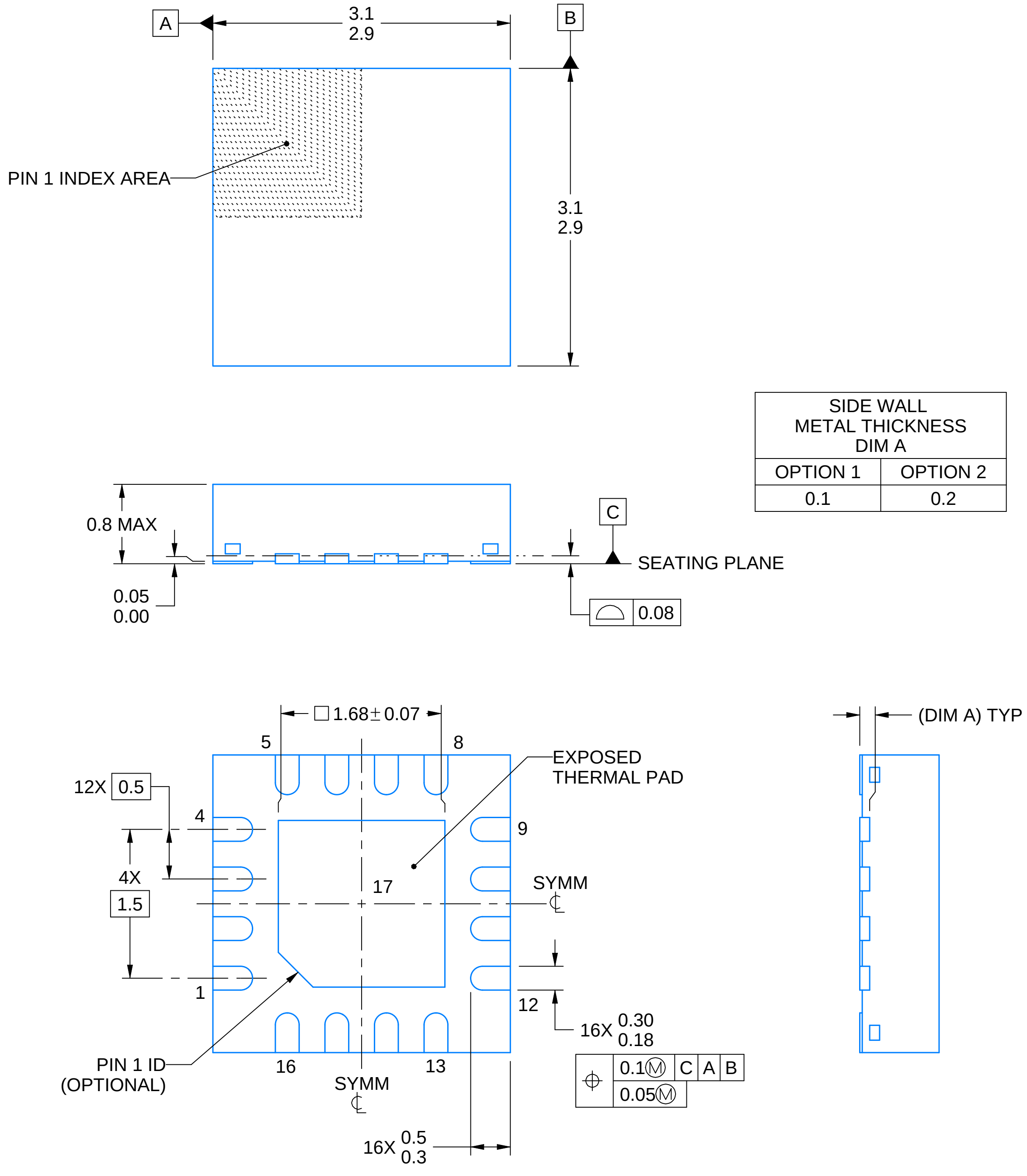
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

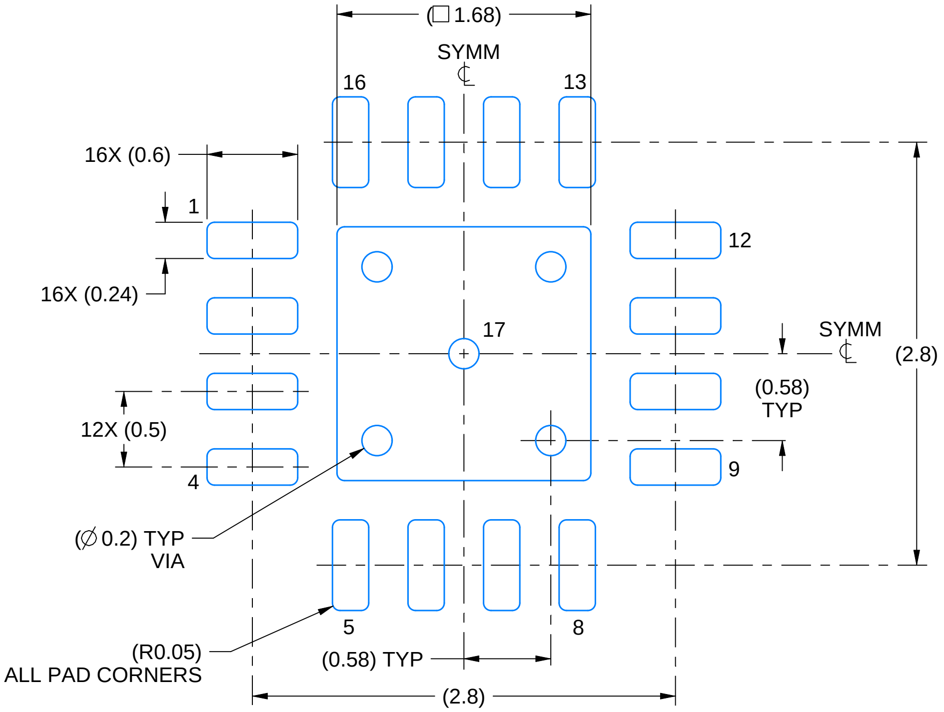


SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

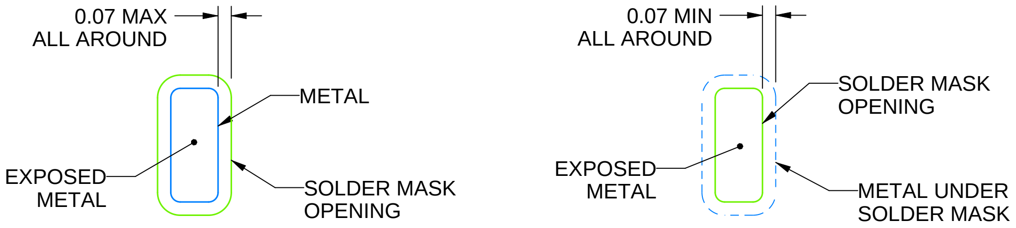
4219117/B 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



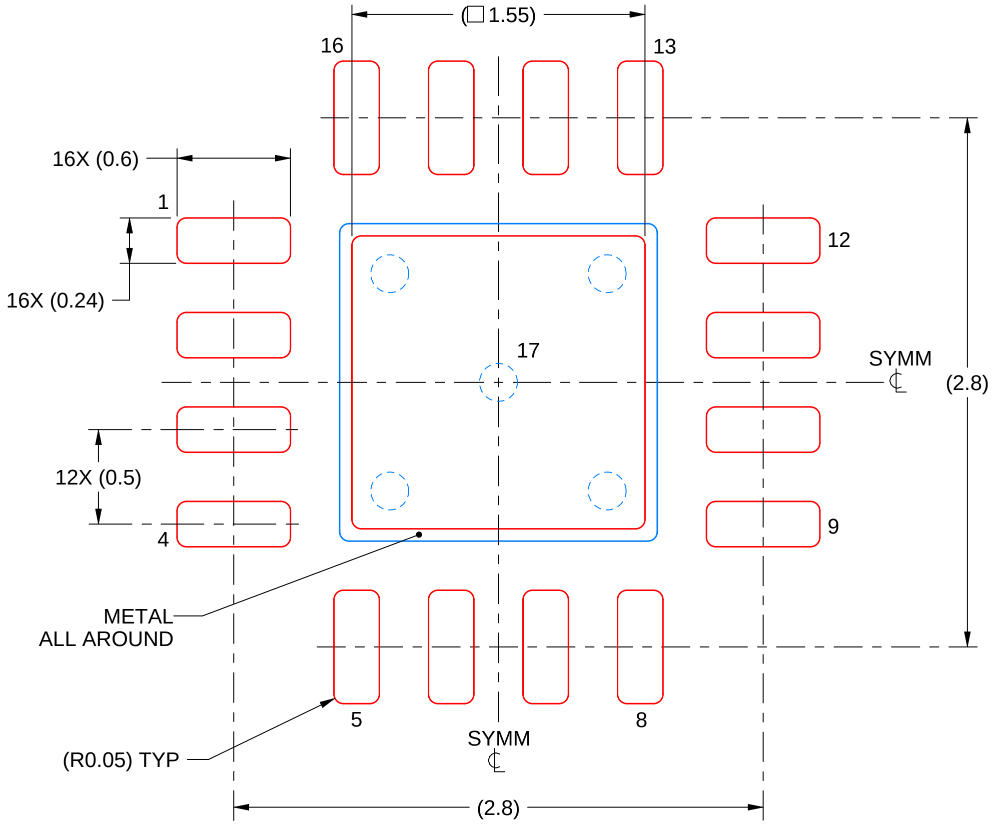
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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