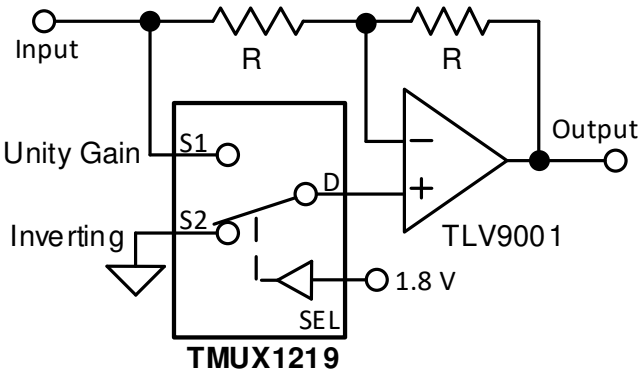
# TMUX1219-Q1 5V、双方向、2:1 汎用スイッチ

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定済み
  - デバイス温度グレード 1:-40℃～125℃の動作時周囲温度範囲
  - デバイス HBM 分類レベル H1C
  - デバイス CDM 分類レベル C3
- レール ツー レールの動作
- 双方向の信号パス
- 1.8V ロジック互換
- フェイルセーフ ロジック
- 低いオン抵抗:3Ω
- 幅広い電源電圧範囲:1.08V～5.5V
- –40℃～+125℃の動作温度
- 低い消費電流:4nA
- 遷移時間:14ns
- ブレイク ビフォー メイクのスイッチング動作
- ESD 保護 (HBM):2000V

## 2 アプリケーション

- アナログおよびデジタル スイッチング
- I2C および SPI バスの多重化
- 先進運転支援システム (ADAS)
- ボディ エレクトロニクスとライティング
- インフォテインメントおよびクラスタ
- ゾーン アーキテクチャ
- 車体制御モジュール
- バッテリ管理システム
- テレマティクス
- 車載ヘッド ユニット




**TMUX1219**
**アプリケーションの例**

## 3 概要

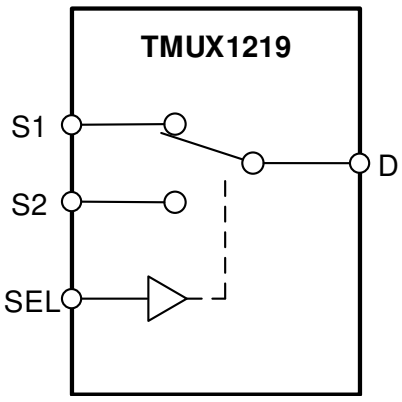
TMUX1219-Q1 は、汎用の CMOS (相補型金属酸化膜半導体) 単極双投 (SPDT) スイッチです。TMUX1219-Q1 は、SEL ピンの状態に基づいて、2 つのソース入力間のスイッチングを行います。1.08V～5.5V の広い動作電源電圧範囲で、幅広い車載用アプリケーションに使用可能です。このデバイスは、ソース (Sx) およびドレイン (D) ピンで、GND から $V_{DD}$ までの範囲の双方向アナログおよびデジタル信号をサポートします。消費電流が 4nA と低いため、携帯型アプリケーションで使用できます。

すべてのロジック入力のスレッショルドは 1.8V ロジック互換で、有効な電源電圧範囲で動作していれば、TTL と CMOS の両方のロジックと互換性が保証されます。フェイルセーフ ロジック回路により、電源ピンよりも先に制御ピンに電圧が印加されるため、デバイスへの損傷の可能性が避けられます。

**製品情報**

| 部品番号 | パッケージ (1) | 本体サイズ (公称) |
|---|---|---|
| TMUX1219-Q1 | SOT-23 (6) | 2.90 mm × 1.60mm |

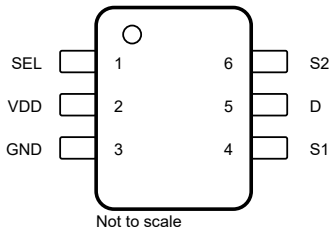
(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ オプションについての付録を参照してください。




**ブロック図**

# Table of Contents

# 4 Pin Configuration and Functions




Product Preview

**図 4-1. DBV Package 6-Pin SOT-23 Top View**

**表 4-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SEL | 1 | I | Select pin: controls state of the switch according to 表 7-1. (Logic Low = S1 to D, Logic High = S2 to D) |
| VDD | 2 | P | Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between $V_{DD}$ and GND. |
| GND | 3 | P | Ground (0 V) reference |
| S1 | 4 | I/O | Source pin 1. Can be an input or output. |
| D | 5 | I/O | Drain pin. Can be an input or output. |
| S2 | 6 | I/O | Source pin 2. Can be an input or output. |

(1) I = input, O = output, I/O = input and output, P = power

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | –0.5 | 6 | V |
| $V_{SEL}$ | Logic control input pin voltage (SEL) | –0.5 | 6 | V |
| $I_{SEL}$ | Logic control input pin current (SEL) | –30 | 30 | mA |
| $V_S$ or $V_D$ | Source or drain voltage (Sx, D) | –0.5 | $V_{DD}$+0.5 | V |
| $I_S$ or $I_{D\ (CONT)}$ | Source or drain continuous current (Sx, D) | –30 | 30 | mA |
| $T_{stg}$ | Storage temperature | –65 | 150 | °C |
| $T_J$ | Junction temperature | | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1) | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins(2) | ±750 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 1.08 | | 5.5 | V |
| $V_S$ or $V_D$ | Signal path input/output voltage (source or drain pin) (Sx, D) | 0 | | $V_{DD}$ | V |
| $V_{SEL}$ | Logic control input pin voltage (SEL) | 0 | | 5.5 | V |
| $T_A$ | Ambient temperature | –40 | | 125 | °C |

## 5.4 Thermal Information

| THERMAL METRIC(1) | | TMUX1219-Q1 DBV (SOT-23) 6 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 212.3 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 156.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 96.5 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 80.7 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 96.2 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

## 5.5 Electrical Characteristics ($V_{DD}$ = 5V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 5V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 3 | | Ω |
| | | | –40°C to +85°C | | | 5 | Ω |
| | | | –40°C to +125°C | | | 6 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 0.15 | | Ω |
| | | | –40°C to +85°C | | | 0.4 | Ω |
| | | | –40°C to +125°C | | | 1 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 1.5 | | Ω |
| | | | –40°C to +85°C | | 2 | | Ω |
| | | | –40°C to +125°C | | 3 | | Ω |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 5 V<br>Switch Off<br>$V_D$ = 4.5 V / 1.5 V<br>$V_S$ = 1.5 V / 4.5 V<br>Refer to (1) | 25°C | | ±5 | | nA |
| | | | –40°C to +85°C | –25 | | 25 | nA |
| | | | –40°C to +125°C | –40 | | 40 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 5 V<br>Switch On<br>$V_D$ = $V_S$ = 4.5 V / 1.5 V<br>Refer to (1) | 25°C | | ±15 | | nA |
| | | | –40°C to +85°C | –50 | | 50 | nA |
| | | | –40°C to +125°C | –80 | | 80 | nA |
| **LOGIC INPUTS (SEL)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 1.49 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.87 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0 V or 5.5 V | 25°C | | 0.003 | | µA |
| | | | –40°C to +125°C | | | 1.5 | µA |

at $T_A$ = 25°C, $V_{DD}$ = 5V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Switching time between channels | $V_S$ = 3 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to (1) | 25°C | | 12 | | ns |
| | | | –40°C to +85°C | | | 18 | ns |
| | | | –40°C to +125°C | | | 19 | ns |
| $t_{OPEN}$ (BBM) | Break before make time | $V_S$ = 3 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to (1) | 25°C | | 8 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_D$ = 1 V<br>$R_S$ = 0 Ω, $C_L$ = 1 nF<br>Refer to (1) | 25°C | | –10 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to (1) | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to (1) | 25°C | | –45 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to (1) | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to (1) | 25°C | | –45 | | dB |
| BW | Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>Refer to (1) | 25°C | | 250 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1 MHz | 25°C | | 7 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1 MHz | 25°C | | 23 | | pF |

(1) When $V_S$ is 4.5V, $V_D$ is 1.5V or when $V_S$ is 1.5V, $V_D$ is 4.5V.

## 5.6 Electrical Characteristics ($V_{DD}$ = 3.3V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 3.3V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 5 | | Ω |
| | | | –40°C to +85°C | | | 10 | Ω |
| | | | –40°C to +125°C | | | 12 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 0.15 | | Ω |
| | | | –40°C to +85°C | | | 1 | Ω |
| | | | –40°C to +125°C | | | 1 | Ω |
| $R_{ON\ FLAT}$ | On-resistance flatness | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 3.5 | | Ω |
| | | | –40°C to +85°C | | 4 | | Ω |
| | | | –40°C to +125°C | | 5 | | Ω |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 3.3 V<br>Switch Off<br>$V_D$ = 3 V / 1 V<br>$V_S$ = 1 V / 3 V<br>Refer to (1) | 25°C | | ±5 | | nA |
| | | | –40°C to +85°C | –25 | | 25 | nA |
| | | | –40°C to +125°C | –40 | | 40 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 3.3 V<br>Switch On<br>$V_D$ = $V_S$ = 3 V / 1 V<br>Refer to (1) | 25°C | | ±15 | | nA |
| | | | –40°C to +85°C | –50 | | 50 | nA |
| | | | –40°C to +125°C | –80 | | 80 | nA |
| **LOGIC INPUTS (SEL)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 1.35 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.8 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | -40°C to 125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0 V or 5.5 V | 25°C | | 0.003 | | µA |
| | | | –40°C to +125°C | | | 0.8 | µA |

at $T_A$ = 25°C, $V_{DD}$ = 3.3V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Switching time between channels | $V_S$ = 2 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to (1) | 25°C | | 14 | | ns |
| | | | –40°C to +85°C | | | 20 | ns |
| | | | –40°C to +125°C | | | 21 | ns |
| $t_{OPEN}$ (BBM) | Break before make time | $V_S$ = 2 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to (1) | 25°C | | 9 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_D$ = 1 V<br>$R_S$ = 0 Ω, $C_L$ = 1 nF<br>Refer to (1) | 25°C | | –6 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to (1) | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to (1) | 25°C | | –45 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to (1) | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to (1) | 25°C | | –45 | | dB |
| BW | Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>Refer to (1) | 25°C | | 250 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1 MHz | 25°C | | 7 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1 MHz | 25°C | | 23 | | pF |

(1) When $V_S$ is 3V, $V_D$ is 1V or when $V_S$ is 1V, $V_D$ is 3V.

## 5.7 Electrical Characteristics ($V_{DD}$ = 1.8V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 1.8V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 40 | | Ω |
| | | | –40°C to +85°C | | | 80 | Ω |
| | | | –40°C to +125°C | | | 80 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 0.4 | | Ω |
| | | | –40°C to +85°C | | | 1.5 | Ω |
| | | | –40°C to +125°C | | | 1.5 | Ω |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 1.98 V<br>Switch Off<br>$V_D$ = 1.62 V / 1 V<br>$V_S$ = 1 V / 1.62 V<br>Refer to (1) | 25°C | | ±5 | | nA |
| | | | –40°C to +85°C | –25 | | 25 | nA |
| | | | –40°C to +125°C | –40 | | 40 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 1.98 V<br>Switch On<br>$V_D$ = $V_S$ = 1.62 V / 1 V<br>Refer to (1) | 25°C | | ±15 | | nA |
| | | | –40°C to +85°C | –50 | | 50 | nA |
| | | | –40°C to +125°C | –80 | | 80 | nA |
| **LOGIC INPUTS (SEL)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 1.07 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.68 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0 V or 5.5 V | 25°C | | 0.001 | | µA |
| | | | –40°C to +125°C | | | 0.6 | µA |

at $T_A$ = 25°C, $V_{DD}$ = 1.8V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Transition time between channels | $V_S$ = 1 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to (1) | 25°C | | 28 | | ns |
| | | | –40°C to +85°C | | | 44 | ns |
| | | | –40°C to +125°C | | | 44 | ns |
| $t_{OPEN}$ (BBM) | Break before make time | $V_S$ = 1 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to (1) | 25°C | | 16 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_D$ = 1 V<br>$R_S$ = 0 Ω, $C_L$ = 1 nF<br>Refer to (1) | 25°C | | –3 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to (1) | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to (1) | 25°C | | –45 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to (1) | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to (1) | 25°C | | –45 | | dB |
| BW | Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF | 25°C | | 250 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1 MHz | 25°C | | 7 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1 MHz | 25°C | | 23 | | pF |

(1) When $V_S$ is 1.62V, $V_D$ is 1V or when $V_S$ is 1V, $V_D$ is 1.62V.

## 5.8 Electrical Characteristics ($V_{DD}$ = 1.2V ±10 %)

at $T_A$ = 25°C, $V_{DD}$ = 1.2V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG SWITCH** | | | | | | | |
| $R_{ON}$ | On-resistance | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 70 | | Ω |
| | | | –40°C to +85°C | | | 105 | Ω |
| | | | –40°C to +125°C | | | 105 | Ω |
| $\Delta R_{ON}$ | On-resistance matching between channels | $V_S$ = 0 V to $V_{DD}$<br>$I_{SD}$ = 10 mA<br>Refer to (1) | 25°C | | 0.4 | | Ω |
| | | | –40°C to +85°C | | | 1.5 | Ω |
| | | | –40°C to +125°C | | | 1.5 | Ω |
| $I_{S(OFF)}$ | Source off leakage current(1) | $V_{DD}$ = 1.32 V<br>Switch Off<br>$V_D$ = 1 V / 0.8 V<br>$V_S$ = 0.8 V / 1 V<br>Refer to (1) | 25°C | | ±5 | | nA |
| | | | –40°C to +85°C | –25 | | 25 | nA |
| | | | –40°C to +125°C | –40 | | 40 | nA |
| $I_{D(ON)}$<br>$I_{S(ON)}$ | Channel on leakage current | $V_{DD}$ = 1.32 V<br>Switch On<br>$V_D$ = $V_S$ = 1 V / 0.8 V<br>Refer to (1) | 25°C | | ±15 | | nA |
| | | | –40°C to +85°C | –50 | | 50 | nA |
| | | | –40°C to +125°C | –80 | | 80 | nA |
| **LOGIC INPUTS (SEL)** | | | | | | | |
| $V_{IH}$ | Input logic high | | –40°C to +125°C | 0.96 | | 5.5 | V |
| $V_{IL}$ | Input logic low | | –40°C to +125°C | 0 | | 0.36 | V |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | 25°C | | ±0.005 | | µA |
| $I_{IH}$<br>$I_{IL}$ | Input leakage current | | –40°C to +125°C | | | ±0.05 | µA |
| $C_{IN}$ | Logic input capacitance | | 25°C | | 1 | | pF |
| $C_{IN}$ | Logic input capacitance | | –40°C to +125°C | | | 2 | pF |
| **POWER SUPPLY** | | | | | | | |
| $I_{DD}$ | $V_{DD}$ supply current | Logic inputs = 0 V or 5.5 V | 25°C | | 0.003 | | µA |
| | | | –40°C to +125°C | | | 0.5 | µA |

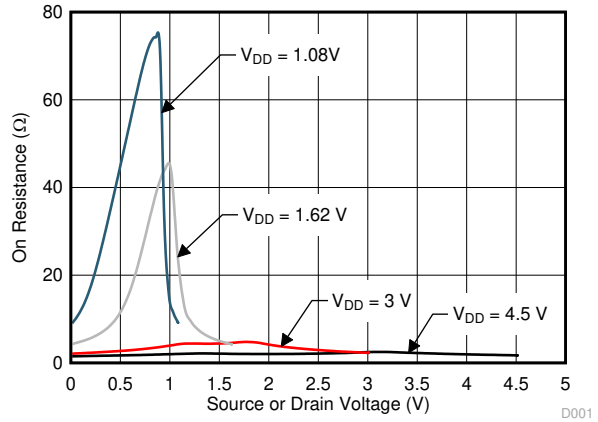
at $T_A$ = 25°C, $V_{DD}$ = 1.2V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | TA | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| $t_{TRAN}$ | Transition time between channels | $V_S$ = 1 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to (1) | 25°C | | 55 | | ns |
| | | | –40°C to +85°C | | | 190 | ns |
| | | | –40°C to +125°C | | | 190 | ns |
| $t_{OPEN}$ (BBM) | Break before make time | $V_S$ = 1 V<br>$R_L$ = 200 Ω, $C_L$ = 15 pF<br>Refer to (1) | 25°C | | 28 | | ns |
| | | | –40°C to +85°C | 1 | | | ns |
| | | | –40°C to +125°C | 1 | | | ns |
| $Q_C$ | Charge Injection | $V_D$ = 1 V<br>$R_S$ = 0 Ω, $C_L$ = 1 nF<br>Refer to (1) | 25°C | | –2 | | pC |
| $O_{ISO}$ | Off Isolation | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to (1) | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to (1) | 25°C | | –45 | | dB |
| $X_{TALK}$ | Crosstalk | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 1 MHz<br>Refer to (1) | 25°C | | –65 | | dB |
| | | $R_L$ = 50 Ω, $C_L$ = 5 pF<br>f = 10 MHz<br>Refer to (1) | 25°C | | –45 | | dB |
| BW | Bandwidth | $R_L$ = 50 Ω, $C_L$ = 5 pF | 25°C | | 250 | | MHz |
| $C_{SOFF}$ | Source off capacitance | f = 1 MHz | 25°C | | 7 | | pF |
| $C_{SON}$<br>$C_{DON}$ | On capacitance | f = 1 MHz | 25°C | | 23 | | pF |

(1) When $V_S$ is 1V, $V_D$ is 0.8V or when $V_S$ is 0.8V, $V_D$ is 1V.

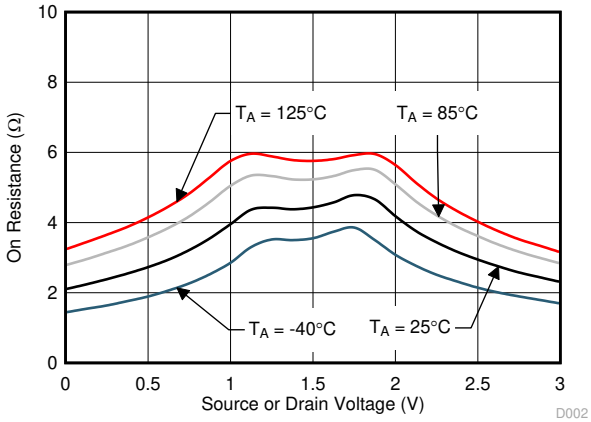
## 5.9 Typical Characteristics

at $T_A$ = 25°C, $V_{DD}$ = 5 V (unless otherwise noted)



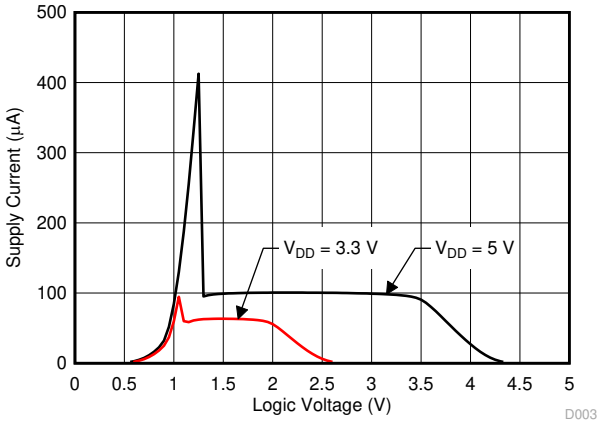

$T_A$ = 25°C

**図 5-1. On-Resistance vs Source or Drain Voltage**



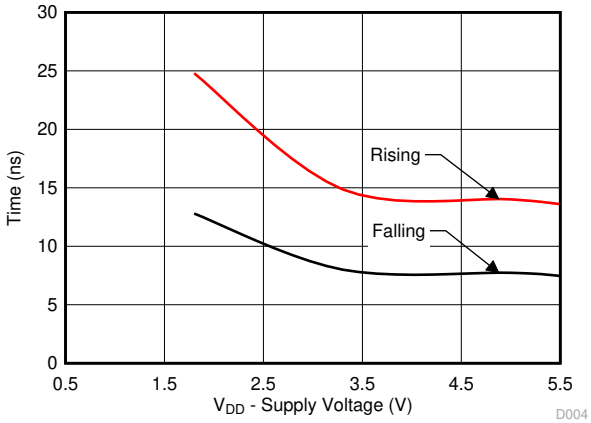

$V_{DD}$ = 3 V

**図 5-2. On-Resistance vs Source or Drain Voltage**



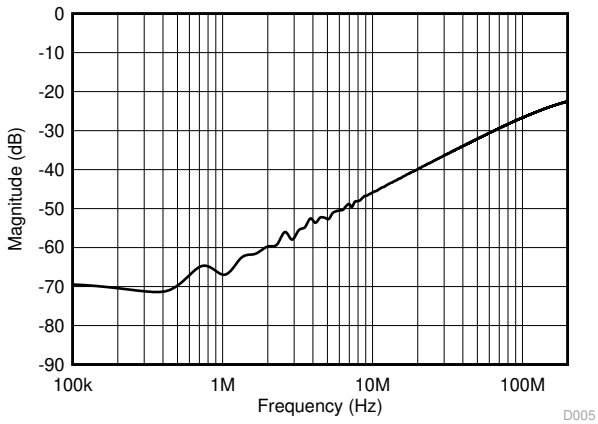

$T_A$ = 25°C

**図 5-3. Supply Current vs Logic Voltage**



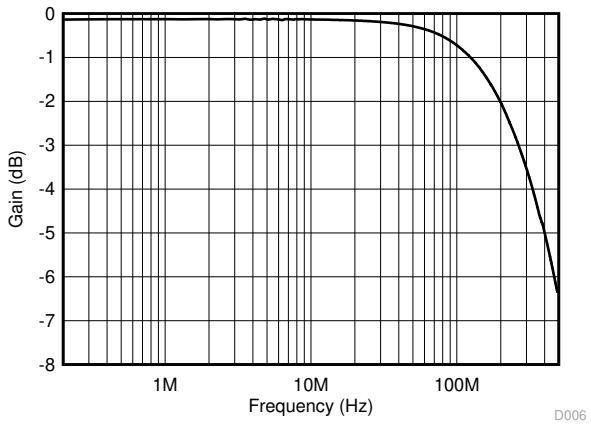

$T_A$ = 25°C

**図 5-4. $T_{transition}$ vs Supply Voltage**




$T_A$ = 25°C

**図 5-5. Crosstalk and Off-Isolation vs Frequency**




$T_A$ = 25°C

**図 5-6. Frequency Response**

# 6 Parameter Measurement Information

## 6.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol $R_{ON}$ is used to denote on-resistance. The measurement setup used to measure $R_{ON}$ is shown in 図 6-1. Voltage (V) and current ($I_{SD}$) are measured using this setup, and $R_{ON}$ is computed with $R_{ON} = V / I_{SD}$:

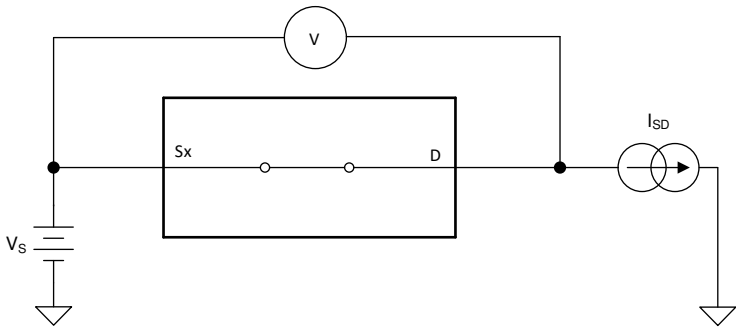



**図 6-1. On-Resistance Measurement Setup**

## 6.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

The setup used to measure off-leakage current is shown in 図 6-2.

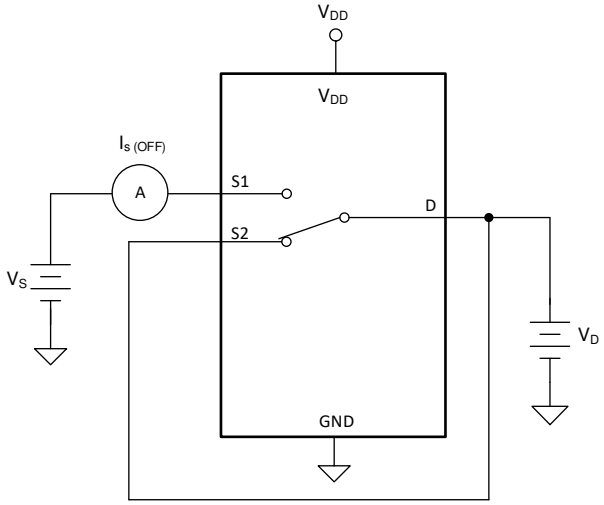



**図 6-2. Off-Leakage Measurement Setup**

## 6.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. 図 6-3 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

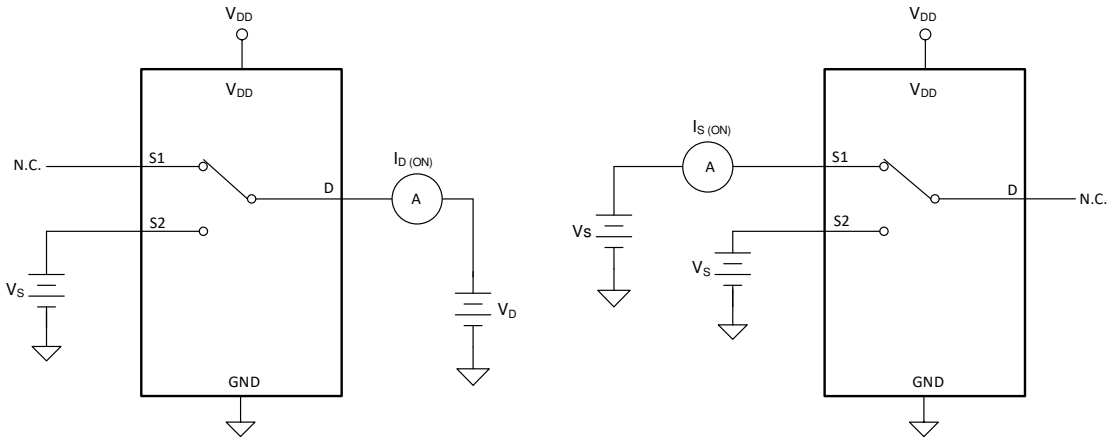



**図 6-3. On-Leakage Measurement Setup**

## 6.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the logic control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. 図 6-4 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

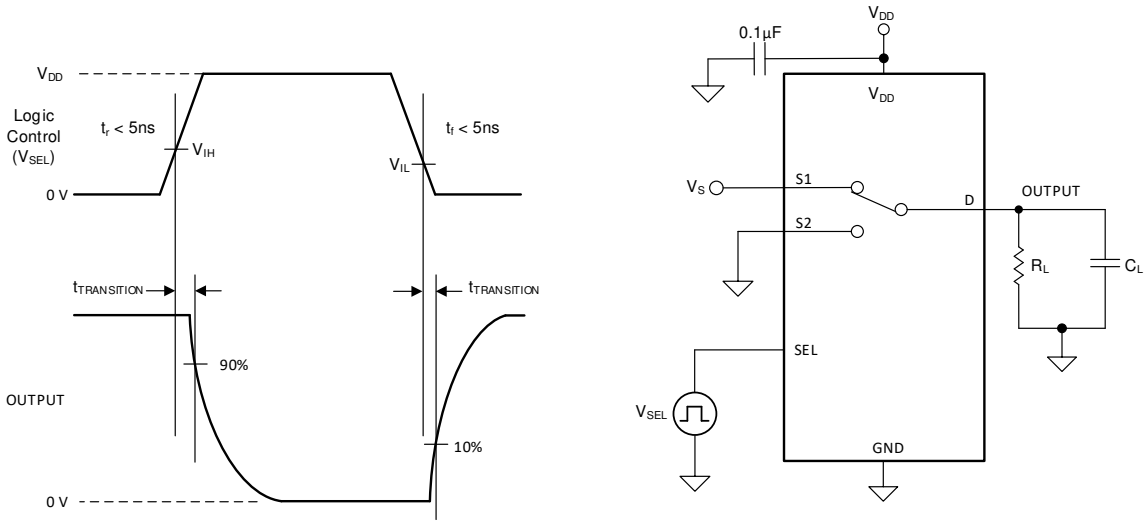



**図 6-4. Transition-Time Measurement Setup**

## 6.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. 図 6-5 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

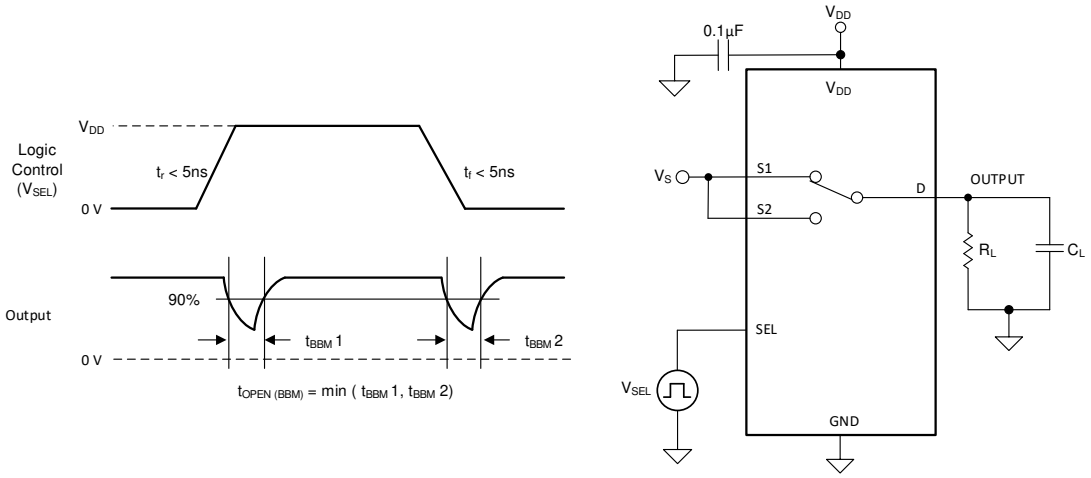



**図 6-5. Break-Before-Make Delay Measurement Setup**

## 6.6 Charge Injection

The TMUX1219-Q1 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol $Q_C$. 図 6-6 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

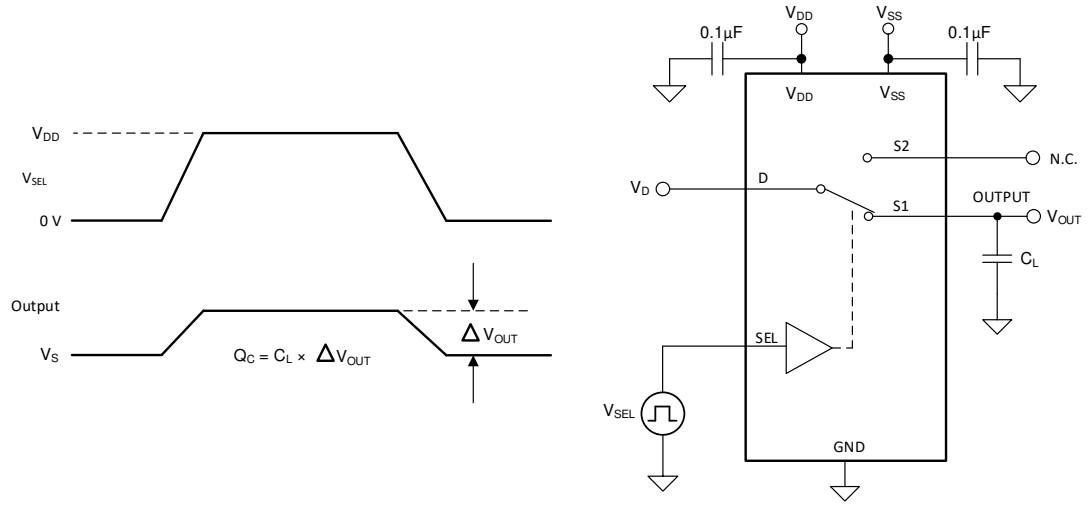



**図 6-6. Charge-Injection Measurement Setup**

## 6.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. 図 6-7 shows the setup used to measure, and the equation used to calculate off isolation.

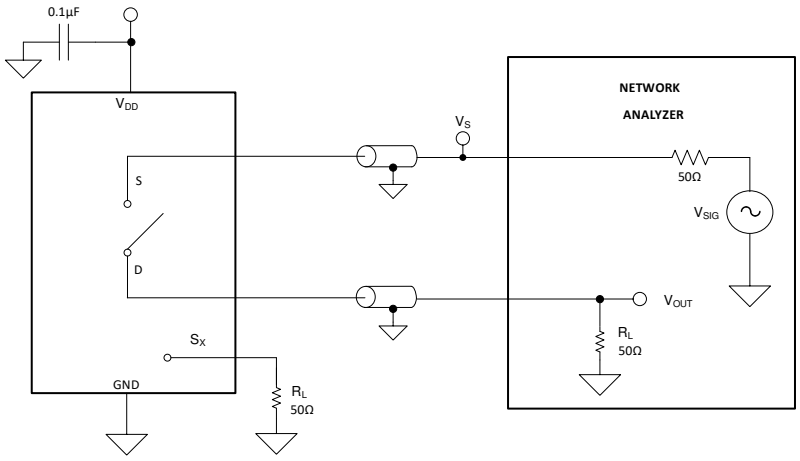



**図 6-7. Off Isolation Measurement Setup**

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

## 6.8 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. 図 6-8 shows the setup used to measure, and the equation used to calculate crosstalk.

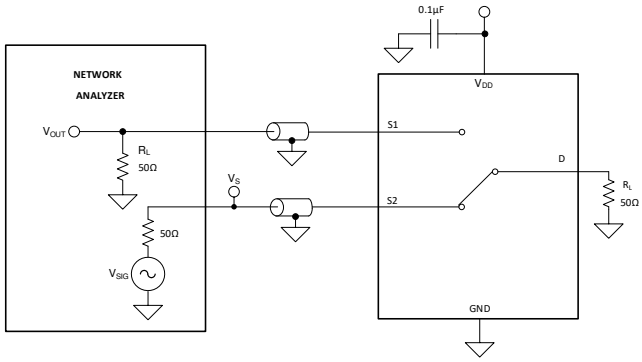



**図 6-8. Crosstalk Measurement Setup**

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

## 6.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. 図 6-9 shows the setup used to measure bandwidth.

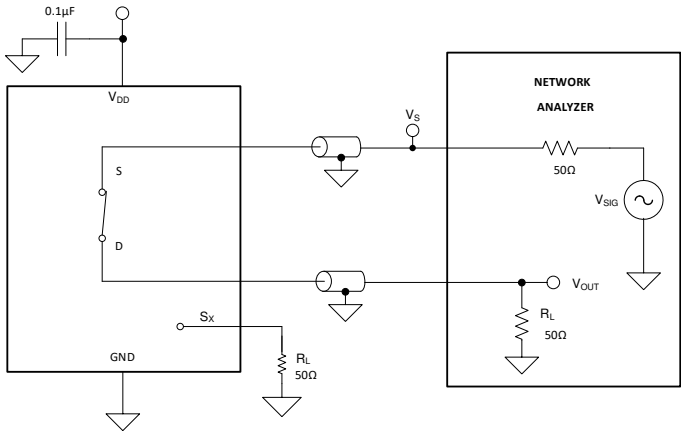



**図 6-9. Bandwidth Measurement Setup**

# 7 Detailed Description

## 7.1 Functional Block Diagram

The TMUX1219-Q1 is an 2:1 (SPDT), 1-channel switch where the input is controlled with a single select (SEL) control pin.

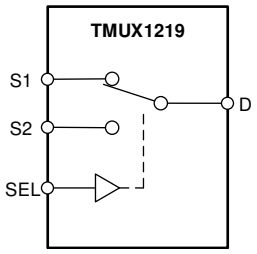



**図 7-1. TMUX1219-Q1 Functional Block Diagram**

## 7.2 Feature Description

### *7.2.1 Bidirectional Operation*

The TMUX1219-Q1 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

### *7.2.2 Rail to Rail Operation*

The valid signal path input/output voltage for TMUX1219-Q1 ranges from GND to $V_{DD}$.

### *7.2.3 1.8 V Logic Compatible Inputs*

The TMUX1219-Q1 has 1.8-V logic compatible control for the logic control input (SEL). The logic input threshold scales with supply but still provides 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allow the TMUX1219-Q1 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*

### *7.2.4 Fail-Safe Logic*

The TMUX1219-Q1 supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the TMUX1219-Q1 to be ramped to 5.5 V while $V_{DD}$ = 0 V. Additionally, the feature enables operation of the TMUX1219-Q1 with $V_{DD}$ = 1.2 V while allowing the select pin to interface with a logic level of another device up to 5.5 V.

## 7.3 Device Functional Modes

The select (SEL) pin of the TMUX1219-Q1 controls which source channel is connected to the drain of the device. When a signal path is not selected, that source pin is in high impedance mode (HI-Z). The control pin can be as high as 5.5 V.

## 7.4 Truth Tables

**表 7-1. TMUX1219-Q1 Truth Table**

| CONTROL LOGIC (SEL) | Selected Source (Sx) Connected To Drain (D) Pin |
|---|---|
| 0 | S1 |
| 1 | S2 |

# 8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The TMUX12xx family offers good system performance across a wide operating supply (1.08V to 5.5V). These devices include 1.8V logic compatible control input pins that enable operation in systems with 1.8V I/O rails. Additionally, the control input pin supports Fail-Safe Logic which allows for operation up to 5.5V, regardless of the state of the supply pin. This protection stops the logic pins from back-powering the supply rail. These features of the TMUX12xx, a family of general purpose multiplexers and switches, reduce system complexity, board size, and overall system cost.

## 8.2 Typical Application

### *8.2.1 Switchable Operational Amplifier Gain Setting*

One example application of the TMUX1219-Q1 is to change an Op Amp from unity gain setting to an inverting amplifier configuration. Utilizing a switch allows a system to have a configurable gain and allows the same architecture to be utilized across the board for various inputs to the system. 図 8-1 shows the TMUX1219-Q1 configured for gain setting application.

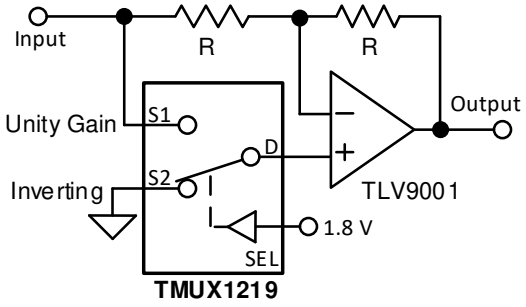



**図 8-1. Switchable Op Amp Gain Setting**

#### 8.2.1.1 Design Requirements

This design example uses the parameters listed in 表 8-1.

**表 8-1. Design Parameters**

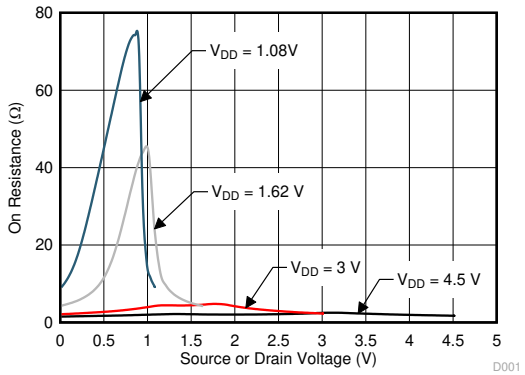
| PARAMETERS | VALUES |
|---|---|
| Input Signal | 0 V to 2.75 V |
| Mux Supply ($V_{DD}$) | 2.75 V |
| Op Amp Supply ($V_+$/ $V_-$) | ±2.75 V |
| Mux I/O signal range | 0 V to $V_{DD}$ (Rail to Rail) |
| Control logic thresholds | 1.8 V compatible (up to 5.5V) |

#### 8.2.1.2 Detailed Design Procedure

The application shown in 図 8-1 demonstrates how to use a single control input and toggle between gain settings of -1 and +1. If switching between inverting and unity gain is not required, the TMUX1219-Q1 can be utilized in the feedback path to select different feedback resistors and provide scalable gain settings for configurable signal conditioning.

The TMUX1219-Q1 can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a weak pull-down or pull-up resistor to ensure the input is in a known state. All inputs to the switch must fall within the recommend operating conditions of the TMUX1219-Q1 including signal range and continuous current. For this design with a supply of 2.75 V the signal range can be 0 V to 2.75 V and the max continuous current can be 30 mA.

#### 8.2.1.3 Application Curve




$T_A$ = 25°C

**図 8-2. On-Resistance vs Source or Drain Voltage**

### *8.2.2 Input Control for Power Amplifier*

Another application of the TMUX1219-Q1 is for input control of a power amplifier. Utilizing a switch allows a system to control when the DAC is connected to the power amplifier, and can stop biasing the power amplifier by switching the gate to GND. 図 8-3 shows the TMUX1219-Q1 configured for control of the power amplifier.

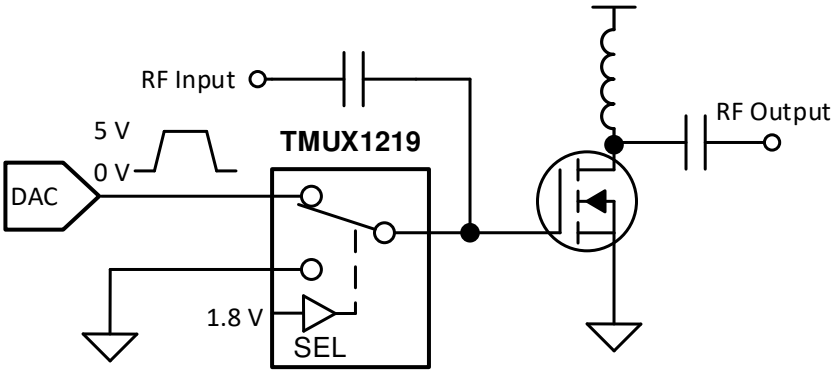



**図 8-3. Input Control of Power Amplifier**

#### 8.2.2.1 Design Requirements

This design example uses the parameters listed in 表 8-1.

**表 8-2. Design Parameters**

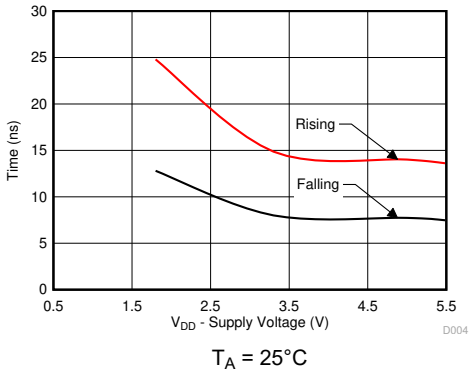
| PARAMETERS | VALUES |
|---|---|
| Supply ($V_{DD}$) | 5 V |
| Mux I/O signal range | 0 V to $V_{DD}$ (Rail to Rail) |
| Control logic thresholds | 1.8 V compatible (up to 5.5V) |

#### 8.2.2.2 Detailed Design Procedure

The application shown in 図 8-3 demonstrates how to toggle between the DAC output and GND for control of a power amplifier using a single control input. The DAC output is utilized to bias the gate of the power amplifier and can be disconnected from the circuit using the select pin of the switch. The TMUX1219-Q1 can support 1.8-V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX1219-Q1 can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a weak pull-down or pull-up resistor to ensure the input is in a known state. All inputs to the switch must fall within the recommend operating conditions of the TMUX1219-Q1 including signal range and continuous current. For this design with a supply of 5 V the signal range can be 0 V to 5 V and the max continuous current can be 30 mA.

#### 8.2.2.3 Application Curve

A key parameter for this application is the transition time of the device. Faster transition time allows the system to toggle between input sources at a faster rate and allows the output to settle to the final value. The TMUX1219-Q1 has a transition time that varies with supply voltage and is shown in 図 8-4




$T_A$ = 25°C

**図 8-4. $T_{transition}$ vs Supply Voltage**

## 9 Power Supply Recommendations

The TMUX1219-Q1 operates across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the $V_{DD}$ supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF from $V_{DD}$ to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

# 10 Layout

## 10.1 Layout Guidelines

### *10.1.1 Layout Information*

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. 図 10-1 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

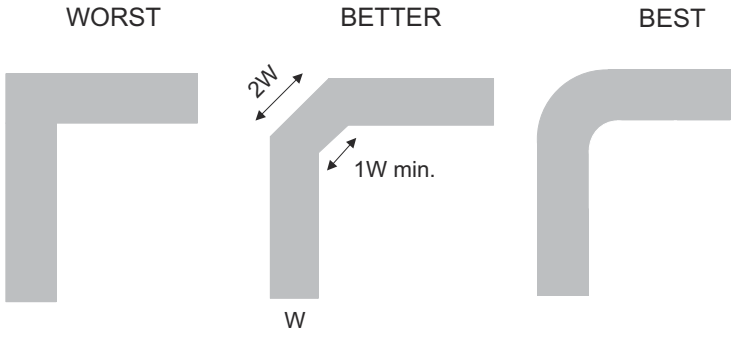



**図 10-1. Trace Example**

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

図 10-2 illustrates an example of a PCB layout with the TMUX1219-Q1. Some key considerations are:

- Decouple the $V_{DD}$ pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the $V_{DD}$ supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

## 10.2 Layout Example

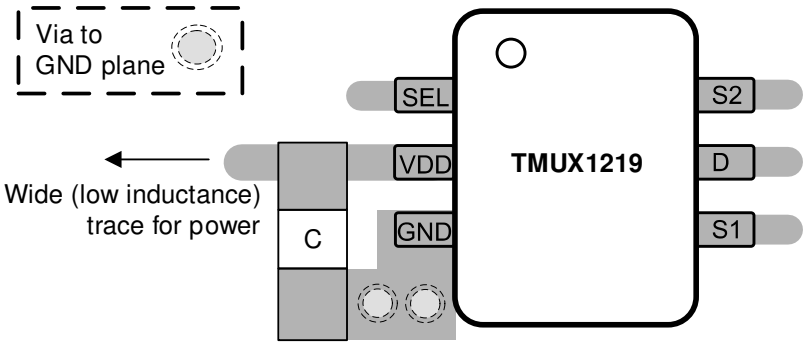



**図 10-2. TMUX1219-Q1 Layout Example**

# 11 Device and Documentation Support

## 11.1 Documentation Support

### *11.1.1 Related Documentation*

Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.

Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.

Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.

## 11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

## 11.3 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

## 11.4 Trademarks

テキサス・インスツルメンツ E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

## 11.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

## 11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

# 12 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| DATE | REVISION | NOTES |
|---|---|---|
| September 2024 | * | Initial Release |

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# 重要なお知らせと免責事項

テキサス・インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、テキサス・インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス・インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス・インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、テキサス・インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。テキサス・インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、テキサス・インスツルメンツおよびその代理人を完全に補償するものとし、テキサス・インスツルメンツは一切の責任を拒否します。

テキサス・インスツルメンツの製品は、テキサス・インスツルメンツの販売条件、または ti.com やかかる テキサス・インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。テキサス・インスツルメンツがこれらのリソースを提供することは、適用されるテキサス・インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、テキサス・インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所:Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TMUX1219DBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 3GUT | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

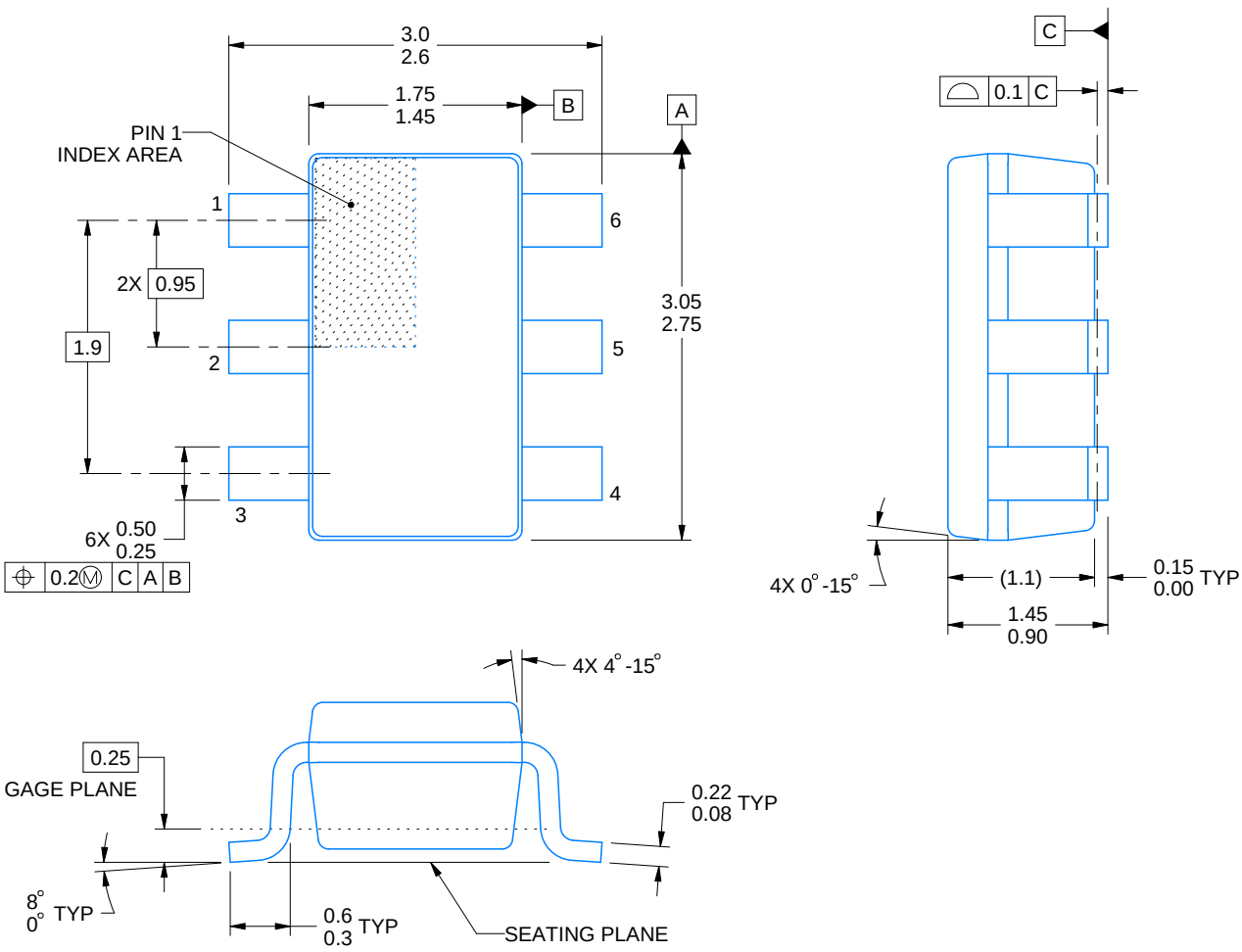
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

# PACKAGE OUTLINE

## DBV0006A

## SOT-23 - 1.45 mm max height

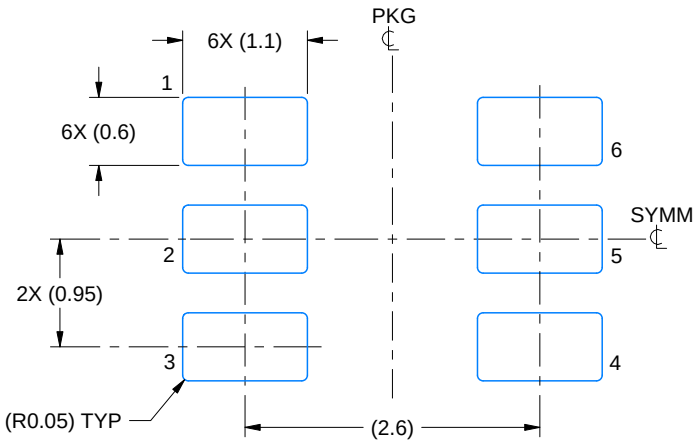
SMALL OUTLINE TRANSISTOR



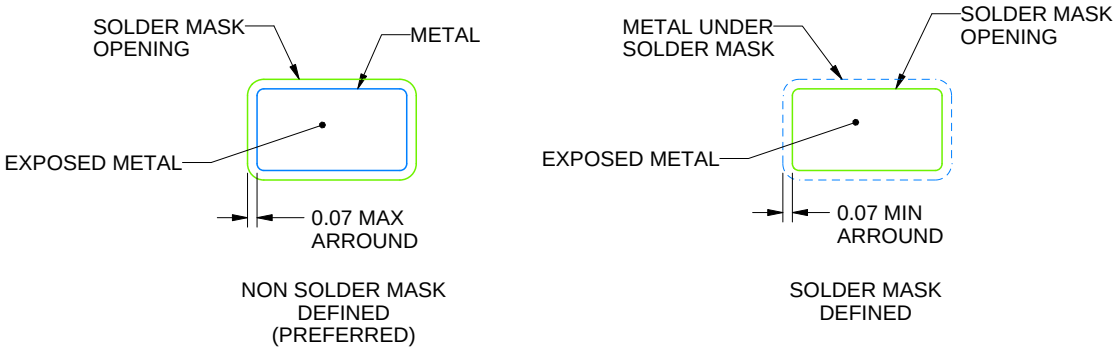

4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

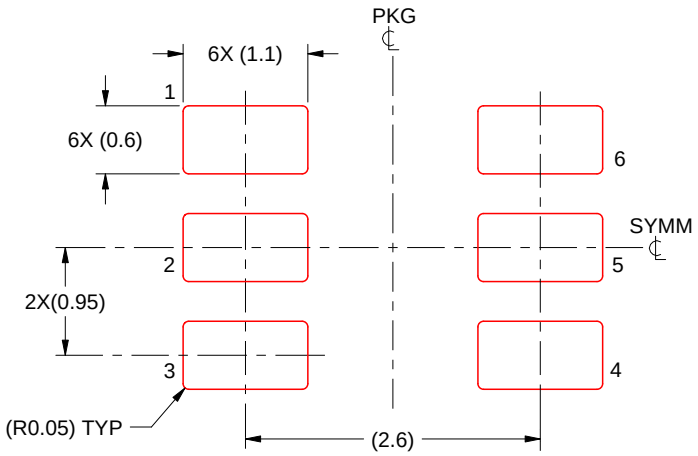



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265